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Development of a DAQ system for the CMS ECAL Phase 2 recommissioning

M. CHIUSI on behalf of the CMS COLLABORATION
LLR, École polytechnique - Palaiseau, France

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Summary. — In view of the High-Luminosity phase of the Large Hadron Collider (LHC), in the barrel region of the CMS electromagnetic calorimeter (ECAL) the entire readout electronics will be replaced to cope with the more stringent requirements in terms of trigger latency, acquisition rate, and radiation and pileup resilience. The configuration sequence for the new on-detector electronics, involving both the improved very-front-end and front-end cards, is reported. The sequence of commands and parameters to load in the electronics is controlled by a software developed at CERN by the ECAL upgrade group and it will be the base on which to build the new data acquisition system (DAQ).

1. – Introduction

The Electromagnetic Calorimeter (ECAL) is a homogeneous calorimeter made of 75848 lead tungstate ($PbWO_4$) scintillating crystals. The crystals are divided into a barrel part (EB) with 61200 of them, covering the pseudorapidity region $|\eta| < 1.48$, and two endcap parts with 7324 crystals each extending the coverage to $|\eta| < 3.0$.

ECAL measures with high accuracy the energies of electrons and photons by absorbing them: the energy resolution achieved during past years ranges from 1.1 to 2.6% in the barrel and 2.2 to 5% in the endcaps for photons from the Higgs boson decay [1].

The main objective of the High-Luminosity LHC (HL-LHC) upgrade [2] of the LHC accelerator is to deliver a much larger data set to the LHC experiments, for new physics searches, Higgs boson coupling measurements, and precision tests of the standard model. The goals include reaching an instantaneous luminosity of 5×10^{34} $\mathrm{cm^2 s^{-1}}$ after 2029 and an integrated luminosity of $250\,\mathrm{fb^{-1}}$ per year, with the goal of $3000\,\mathrm{fb^{-1}}$ in 12 years of operations.

The main requirement of the EB upgrade is to maintain the Run 1 physics performance for photons and electrons at the higher luminosity and pileup of the HL-LHC. In order to accomplish this, the EB electronics must accommodate the Level-1 trigger requirements on latency and rate, in particular a latency up to 12.5 μs and an increased Level-1 trigger rate of up to 750 kHz.

The current crystals and avalanche photo-diode (APD) detectors will remain, while the upgrade will affect the front-end and off-detector read-out electronics of EB. The new front-end electronics will provide single crystal information to the off-detector electronics, where the trigger primitives will be formed in powerful FPGAs, and will guarantee a more

precise matching between the electromagnetic showers and tracks in order to improve background reduction.

The very-front-end card, which provides pulse amplification, shaping, and digitization functions of the signals, will be replaced. The chosen technology is a trans-impedance amplifier (TIA), a device that generates an image of the APD photocurrent in output of this latter. The pulse shaping will be shortened for a better filter of the increased APD noise and the sampling rate will be increased to 160 MHz, to provide better timing resolution and spikes suppression ([1]) in the Level-1 trigger. TIA signals are sampled at 160 MHz —compared to the current 40 MHz— by two identical 12-bit ADCs (4096 ADC channels available). The digitized signals, or *patterns*, are transmitted to the front-end cards. Each card reads five independent channels, each controlling a single ECAL crystal.

The front-end card transmits single crystal data to the back-end electronics system using four Low power Giga-Bit Transceiver (LpGBT), a radiation tolerant and multi-purpose ASIC, able to simultaneously execute the data readout, timing measurements, and to monitor the status of other electronic components. A Versatile Link plus (VTRx) which converts electrical signals into optical and viceversa is integrated in the board.

The readout tower (RT), the simplest CMS ECAL data acquisition block, is composed of five very-front-end cards and a single front-end card. A low-voltage regulator provides precise and stable values of voltage and current to the tower. Each tower —managed by four LpGBT chips— controls a matrix of 5×5 crystals of the ECAL barrel, *i.e.*, 25 different channels.

2. – The configuration of the RT

Many tests have been carried out at CERN by the ECAL upgrade group, whose main purpose is to assemble the new front-end electronics cards prototypes and perform data readout with the first model of the back-end electronics card, named Barrel Calorimeter Processor (BCP), to find the best and more stable configuration chain of an RT.

The experimental setup allows to control the whole RT ASICs making use of Python scripts executed on the laboratory computers. These computers can communicate via optical fibers to the BCP, which forwards each command to the LpGBTs installed in the front-end cards via the optical Link and TCLink protocol [3]. A single configuration command allows the user to access one or more chip registers for basic reading or writing operations. During data acquisition, the off-detector electronics receives and buffers data from the detector front-end cards and implements functions for data integrity checks and alignment of event data to the provided clock. At the moment of writing, no $PbWO_4$ crystal is present in the setup, therefore the acquired raw data from the RT read, collected and stored in the laboratory computers, are mainly electronic noise.

Table I shows the entire RT configuration chain as it has been built by the ECAL upgrade group. The procedure can be executed from a computer installed in the CERN laboratory and takes ∼9 minutes. This procedure has to be executed every time the RT is powered on. Nevertheless, the basic configuration of the tower, executed periodically during data acquisition, lasts ∼4 minutes. Indeed, the Phase-locked scan (PLL)([2]) can be avoided.

([1]) Spikes are signals generated by hadron-APD direct interaction. They have to be separated from the signals and rejected.

([2]) A PLL is an electronic circuit able to match its own oscillation frequency with the one from an input signal. For correct data acquisition, the RT chips have to be synchronized with the BCP clock frequency.

TABLE I. – *The RT configuration chain. Configuration time is given in the third column.*

Step	Description	Time
LpGBTs configuration	A basic ASICs configuration —followed by a general reset of the boards— is performed. Mainly, clocks and e-links (radiation-hard and low-power electrical interfaces for chip-to-chip data transmission) are enabled in the LpGBTs and distributed in the RT.	20 s
ADCs PLL scan	The ADCs are forced to send a specific pattern instead of APD data. Then, a reference voltage for the ADC PLL circuit is set, and the data read by the BCP are checked to see if the pattern is recognised. If it is the case, the ADC has locked the external clock and VFEs are synchronised. If not, a new PLL value is set repeating the test.	5 min
RT channels bit alignment	The good PLL values found in the previous step are set. Each ADC is forced to send a specific pattern and the BCP to look for it among the acquired data. If not found, 1-bit shift is applied at BCP level and this process is repeated.	40 s
ADCs calibration	TIAs are forced to send a reference voltage ($\sim$1V) to the ADCs, which perform self-calibration.	10 s
Pedestals optimization	A specific value of current is sent by TIAs to the ADCs. The peaks positions are collected and checked by the BCP. If the average value is not in the desired range (around 20th ADC channel), higher current is provided.	3 min

3. – Results

Figure 1 shows data acquisition before and after the RT configuration performed using the ECAL group software. Since crystals are not yet installed in the setup, data acquisitions show the electronic noise. On the left, before the ADCs calibration, the sampled data distribution of each channel is reported in blue. Moreover, since the same dataset has been divided into two different parts based on the sampling ADC of each data, two peaks (corresponding to two different ADCs of each channel, named ADC *even* and *odd*) are visible. The position of each peak is higher than ADC channel 300 and the ADCs odd and even mean values are not always matching. On the right, the same blue peaks are presented as they appear after the RT calibration: the two ADCs are well calibrated and the corresponding peaks have compatible mean values. Moreover, the blue peak standard deviations are significantly reduced with values around $\sim$1.9 ADC channels. Their positions lie around ADC channel 20, in order to maximise the available dynamic range composed of 4096 channels.

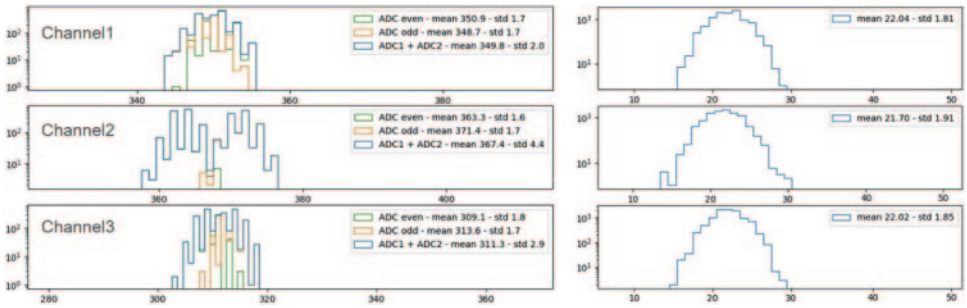

Fig. 1. – Electronic noise peaks from 3 channels of the RT as appearing during data acquisition before (right) and after (left) the boards configuration. Distributions in blue (left and right) have been built including sampled data in their totality, whether they were sampled by ADC odd or even. Green and orange distributions (left) have been built using data respectively from ADC even and odd. For each peak, mean and standard deviation are reported.

4. – Conclusion

The CMS barrel electromagnetic calorimeter will be upgraded for the HL-LHC Phase. The lead tungstate crystals and APD photodetectors will be retained. Both the on-detector and off-detector electronics will be replaced to cope with more demanding Phase-2 CMS trigger requirements, to maintain the best possible energy resolution, and to provide improved capabilities for pileup and spike suppression necessary for the HL-LHC Phase. The software to configure the new front-end boards and to acquire raw data, unpack, and visualize them was tested. It will be embedded in a more formal and operative code and it will allow the future detector to efficiently control each RT. Efforts will be done to reduce the time required for a full configuration of the RT.

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