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Forming-Free Grain Boundary Engineered Hafnium Oxide Resistive Random Access Memory Devices

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A model device based on an epitaxial stack combination of titanium nitride (111) and monoclinic hafnia ($11\bar{1}$) is grown onto a *c*-cut Al_2O_3-substrate to target the role of grain boundaries in resistive switching. The texture transfer results in 120° in-plane rotated *m*-HfO_2 grains, and thus, in a defined subset of allowed grain boundary orientations of high symmetry. These engineered grain boundaries thread the whole dielectric layer, thereby providing predefined breakdown paths for electroforming-free resistive random access memory devices. Combining X-ray diffraction and scanning transmission electron microscopy (STEM)–based localized automated crystal orientation mapping (ACOM), a nanoscale picture of crystal growth and grain boundary orientation is obtained. High-resolution STEM reveals low-energy grain boundaries with facing ($\bar{1}\bar{1}2$) and ($\bar{1}21$) surfaces. The uniform distribution of forming voltages below 2 V—within the operation regime—and the stable switching voltages indicates reduced intra- and device-to-device variation in grain boundary engineered hafnium-oxide-based random access memory devices.

1. Introduction

Resistive random access memory (RRAM) devices based on binary metal oxides, for example, HfO_x, TaO_x, YO_x, are promising candidates for next generation non-volatile memory due to their potential for high-density, high-speed, ultimate scalability, resilience toward ionizing radiation and low-power consumption.[1–14] The proven complementary metal-oxide-semiconductor (CMOS) compatibility of hafnium and tantalum oxide has greatly increased the interest in these material candidates. The intra- and device-to-device variability exhibited by RRAM devices due to the random nature of the forming and switching processes necessitates a more detailed understanding of the role of defects such as oxygen vacancies[15,16] and grain boundaries.[17–20]

In general, the switching mechanism in oxide-based resistive memory structures is due to the formation and rupture of localized conducting filaments.[21–26] These conductive filaments are described as local oxygen deficient/metal enriched conductive pathways which are attributed to the creation of oxygen vacancies due to field and temperature induced local depletion of oxygen.[2] The electrode material participates in the filament formation process by accepting oxygen and acting as an oxygen reservoir in the reset process.[27,28] Electrode roughness or an increased local defect density may lead to an accelerated dielectric breakdown, for example, due to an increased local field. These high local fields are accompanied by increased local current densities and Joule heating resulting in temperatures that can be as high as 1000 K.[29] At these high temperatures, diffusion processes along concentration and temperature gradients are activated.[2] Therefore, the filament will preferentially form at sites of high local defect density or roughness. The random nature of the forming and switching processes resulting in a large inter and intra device variability is the main challenge for the here described type of RRAM.[28,30–33] Additionally, the described complex forming and switching processes are constrained to nanometer-sized-regions and may occur on a sub-nanosecond time-scale,[34] making it difficult to control the mechanism.

Most experimental approaches toward identifying conductive filaments in such devices are limited to indirect methods,

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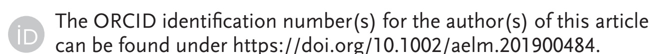
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such as locally probing the electrical conductivity by (spatially resolved/lateral/top view) conductive atomic force microscopy or, as in the case of TiO_2, the detection of conducting substoichiometric Magnéli-Phases.[35] In the case of hafnium oxide, the nature and structure of the oxygen deficient conducting region is not well understood. The conducting filamentary pathways may consist of oxygen intercalated hexagonal Hf, substoichiometric HfO_{2-x}, or as regions enriched with oxygen vacancies. In addition, conductance quantization phenomena have been observed indicating point contact behavior at the switching position.[36] Although promising advances in filament identification have been reported,[37–42] a clear atomistic picture of the involved defects and a correlation to the electric device characteristics is still missing.

So far, the role of grain boundaries in the switching process has been scarcely considered. In the case of high-*k* dielectrics, grain boundaries have been identified as leakage paths for electrical stress-induced breakdown.[43–47] For RRAM, previous investigations that take into account the presence of grain boundaries are rare and mainly rely on density functional theory (DFT) calculations[17–19,48,49] and conductive atomic force microscopy measurements.[19,20,50] The results suggest that grain boundaries in dielectric materials are the preferred locations of oxygen vacancy and interstitial formation, and provide a path of lowered diffusion barrier for oxygen ions.[51] Grain boundaries will naturally occur in resistive switching devices and have been correlated with non-uniformity of forming voltages due to randomized grain boundary networks in polycrystalline dielectric layers.[52,53]

Although literature suggests grain boundary formation only for growth temperatures above 320 °C,[15] experimentally, we have found that crystallization can also be induced at temperatures as low as 200 °C, far below the typical back end of line processing temperatures. Additionally, it is known that the switching process in the electroforming as well as in the set and reset operation is accompanied by Joule heating effects exceeding local temperatures of at least 350 °C.[54] At this temperature, a local (uncontrolled) crystallization of the dielectric layer is expected. Here, we suggest ($TiN/HfO_2/Pt$) RRAM model devices in which well-defined grain boundaries connecting top and bottom electrode are introduced in a controlled way allowing to pinpoint the role of grain boundaries in the forming and switching processes.

In current devices, oxygen engineering is being utilized for reducing electroforming voltages, and, as a consequence, device-to-device variation. Oxygen engineering approaches can be divided in two types: In the first type, the oxygen content is controlled during the growth process of the dielectric layer itself, resulting in a homogeneous vacancy distribution within the dielectric.[15,55] In the second type, a metallic scavenger layer is inserted in the device stack, resulting in a vacancy gradient starting at the metal interface.[52,56–59] Oxygen engineering allows for almost or completely forming-free devices (defined as devices where the operating voltage is close or identical to the forming voltage). It has been shown, that the forming voltage in highly oxygen deficient hafnia stacks does not scale with the layer thickness, but is more or less constant, independent of layer thickness.[16] This indicates that oxygen vacancies in highly deficient layers need not be newly created, but are merely redistributed to form a conducting filament.[3,60,61] One hallmark of forming-free hafnia-based devices is the coexistence of two switching modes (so called counter-figure eight and figure eight according to the applied voltage polarities while performing a switching cycle), corresponding to the formation and rupture of the filament taking place at one or the other electrode.[3] It is likely that the redistribution, as well as the creation, of oxygen vacancies is supported by the presence of defects. Our idea of grain boundary engineering is to provide a perfect predefined nucleation path for oxygen defects necessary to form a conducting filament, thereby, creating along the grain boundary plane similar conditions as in an oxygen engineered device. In this study, we demonstrate the tailored growth of high-symmetry grain boundaries in hafnia that thread the whole dielectric layer and, thus, connect both electrodes. In this way, not only the creation of oxygen vacancies is facilitated and controlled, but also a highway for their transport is predefined. This study not only provides insight in the significant role of grain boundaries in resistive switching devices, but also shows how grain boundary engineering paves the way toward reduced device variability.

2. Results and Discussion

Two samples with different bottom electrode thickness (45 and 300 nm) were grown. The growth conditions of the hafnia layer were chosen such that the grain size was of the order of the layer thickness to achieve threading grain boundaries. The epitaxial texture transfer as described below ensured the growth of well-defined low-energy grain boundaries. A thick bottom electrode is favorable for on-chip heat management during electrical switching of TEM lamellae. To achieve resistive switching in electron transparent TEM lamellae, a low series resistance in combination with a good thermal anchor is important to reduce local current densities and detrimental Joule heating. The structural investigation of the device under test (DUT) (*c*-cut Al_2O_3/TiN/Hafnia/Pt) by X-ray diffraction (XRD), X-ray reflectometry (XRR), und bright-field scanning transmission electron microscopy (BF-STEM), and reflection high-energy electron diffraction (RHEED) is shown in **Figure 1**. In Figure 1a, the X-ray diffraction patterns of the two DUT are shown. The upper (blue) curve (TiN45) represents the stack combination with 45 nm TiN and the lower (green) curve (TiN300) that with 300 nm TiN. Note that the polycrystalline Pt top electrode was deposited after the XRD measurements. Both samples show Laue oscillations for the monoclinic $(11\bar{1})$ orientation of hafnia which indicates an epitaxial relation to the underlying TiN layer. *m*-HfO_2 exhibits the space group $P21/c$ with the lattice parameters $a = 5.1187$ Å, $b = 5.1693$ Å, $c = 5.297$ Å and a non rectilinear angle $\beta = 99.18°$ (reference: ICDD 00-034-0104). For the TiN45 sample, Laue oscillations of the cubic (111) TiN layer are also visible (but not for TiN300 due its thickness), indicating an epitaxial relation to the hexagonal (0001) alumina substrate. The fits of the XRR measurements shown as black curves in Figure 1b reveal a hafnia thickness of 10.1 nm, roughness of 1.22 nm, and a relative density of 1.01 (assuming 9.68 g cm^{-3} for HfO_2).[62] The TiN thickness was fitted to be 45 nm and 298 nm with a roughness of 0.80 nm and a relative density of 1.01 (assuming 5.388 g cm^{-3}

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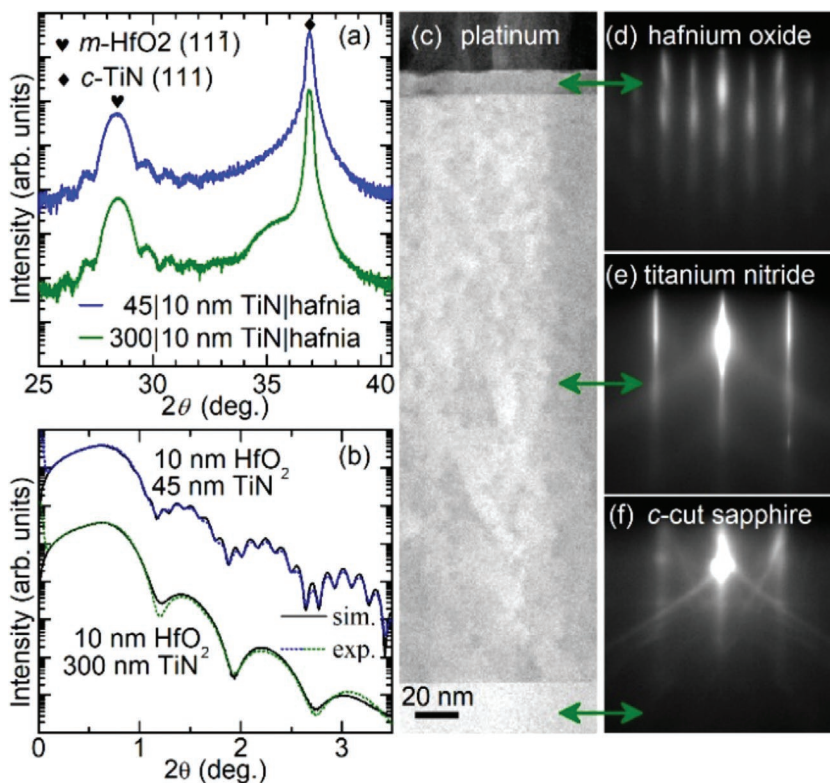

Figure 1. Structural analysis of a device stack: *c*-cut sapphire | 300 nm TiN | 10 nm HfO_2 | Pt. a) θ-2θ XRD pattern, and b) XRR data including corresponding fits for varying TiN electrode thickness, respectively (note that the Pt TE is deposited after acquiring the XRD scans). c) BF-STEM-image of the whole device stack. d-f) RHEED images recorded for hafnia, titanium nitride, and *c*-cut sapphire substrate, respectively.

for TiN),[63] respectively. Figure 1c shows an overview BF-STEM micrograph of the TEM lamella (TiN300) confirming the XRR results. The image also reveals the low roughness of the corresponding hafnia and TiN interfaces, as well as the high crystallinity of all layers. The RHEED patterns (Figure 1d–f) provide crystallographic information of the consecutive growth of hafnium oxide on TiN on *c*-cut sapphire, indicating epitaxial layer-by-layer growth. This is again consistent with the observed Laue oscillations in XRD as well as the low roughness as measured by SEM and XRR. The additional streaks in the RHEED pattern of hafnia as compared to TiN indicate larger in-plane lattice spacings for hafnia (see Figure 1d vs Figure 1e).

The global crystal structure and orientation (pole figure) versus the local microstructure as revealed by automated crystal orientation mapping (ACOM) in a transmission electron microscope is shown in **Figure 2**. The pole figures of the {111} TiN planes ($2\theta = 36.82°$) and the {11$\bar{1}$} hafnia planes ($2\theta = 28.68°$) are shown in Figure 2a,b, respectively. The growth directions are (111) for the TiN layer, and (11$\bar{1}$) for the hafnia layer. The sampled area in this setup covers the full surface of the 5 × 5 mm^2 sample, thus, yielding global information about microstructure and crystal orientation. The pole figures for TiN and hafnia only show a few distinct spots confirming the highly textured growth of both layers with preferential crystal orientations. For both layers, the pole figures show peaks in the center and a sixfold symmetry being locked to the same φ angles indicating a texture transfer from TiN to hafnium oxide, and thus, showing an epitaxial relation to the (0001) sapphire substrate. Note that for TiN, the three additional peaks close to the center of the pole figure can be attributed to the {$\bar{1}$2•4} planes of the *c*-cut sapphire substrate. Due to the cubic structure of TiN, a single-crystalline layer would result in a threefold symmetry for the (111) direction (for all {111}-type lattice planes). The sixfold rotation observed in this stack combination therefore allows for two interpretations: i) two defined in-plane rotated (by 60°) growth directions of the TiN in the (111) direction, or ii) a stacking fault (ABCACB instead of ABC) as suggested by Beck et al.[64]

Due to the monoclinic crystal structure of hafnia, the sixfold symmetry implies six preferred crystal orientations within the hafnia layer. We implemented ACOM to collect crystallographic information at higher resolution to reveal the texture transfer between TiN and hafnia. In this configuration, a nanometer-sized beam of quasi-parallel electrons is scanned across the sample, and an electron diffraction pattern is recorded for every pixel of a map. By fitting a calculated set of diffraction patterns to the experimental data, the phase and orientation of the sample were analyzed for each pixel (similar to electron backscatter diffraction). The resulting dataset (as shown in Figure 2f) can further be used to generate pole figures for selected 2θ angles. For the region shown in Figure 2e, a 170 by 36 pixel (≈0.6 nm per px) dataset has been acquired. A color coded rendering of the respective Euler angles is shown in Figure 2f as well as in the corresponding pole figures of Figure 2c,d. For the TiN thin film, it becomes evident that the ACOM dataset only includes one of the grain orientations found by the macroscopic XRD approach (also indicated by the uniform color in Figure 2f) and only one set of {111} orientations are observed. For the oxide layer, a set of three differently in-plane rotated HfO_2 is observed (again indicated by three predominant colored areas in the ACOM map). Therefore, the unambiguous interpretation of the observed sixfold symmetry in the pole figure of TiN is given by assuming two differently oriented in-plane rotated grain types rather than a stacking fault. For each TiN orientation, three differently in-plane rotated HfO_2 grains are crystallographically preferred. This results in a finite number of allowed grain boundaries within the hafnia layer, providing the stage for controlled grain boundary engineering.

A more detailed insight into the grain boundary types was directly accessed by high-resolution (HR)-STEM as shown in **Figure 3**. The highly textured growth of the stack combination thereby facilitates STEM-imaging on the atomic scale. The selected mode of image contrast is high-angle annular dark-field (HAADF), which allows the identification of high-Z atom columns in the structure (in this case, ^{72}Hf). Figure 3a proves exemplary for three adjoining HfO_2 grains, that the

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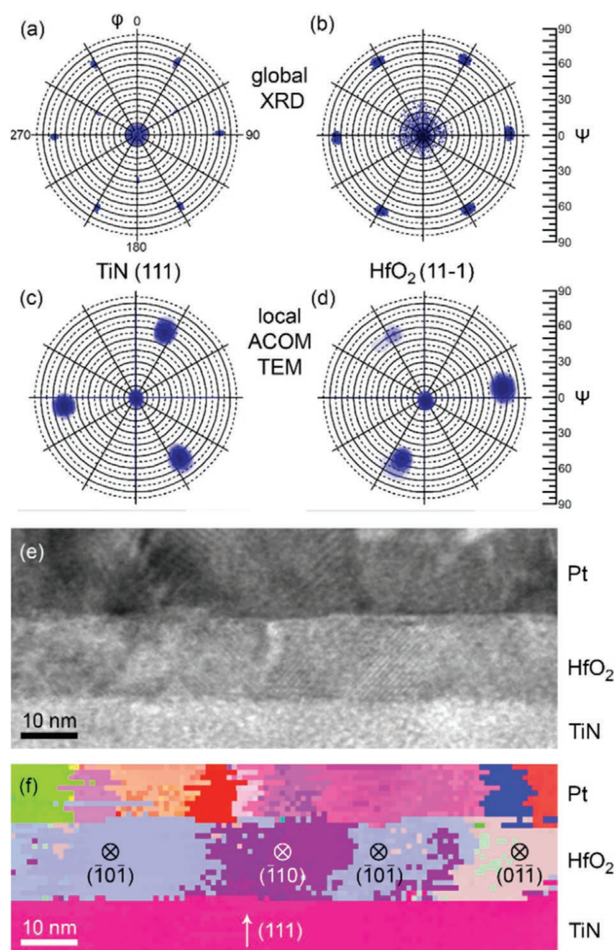

Figure 2. Pole figure and crystal orientation map of a TiN/HfO_2/Pt MIM stack. a,b) XRD pole figures of the TiN {111} and the *m*-HfO_2 {11$\bar{1}$} planes. c,d) The pole figures for the same orientations derived from the ACOM dataset. e) TEM image of the TiN/HfO_2/Pt MIM stack. f) ACOM orientation mapping of the same area, the orientations for the HfO_2 grains and TiN BE are indicated.

growth conditions indeed were such that the grain size was in the order of the film thickness (10 nm). The texture transfer in combination with film thickness and grain size matching results in grains and grain boundaries that perfectly interconnect both electrodes. The average crystal size in the hafnia layer is 10 nm from all the observed grain boundaries aligned along the growth direction of the film. We conclude that the shown microstructure is indeed representative for the whole device stack. Further crystallographic analysis was performed on the HfO_2 grains that exhibit high-resolution contrast, marked in Figure 2a as grains 1 and 2. As shown previously, all hafnia grains grow in the (11$\bar{1}$) direction. The set of grains above is separated by a high-symmetry grain boundary, with grain 1 terminating in a ($\bar{1}\bar{1}\bar{2}$) plane and grain 2 terminating in a ($\bar{1}$21) plane.

In the coincidence site lattice (CSL) model, grain boundaries exhibiting low density of coincident sites, Σ, are obviously low-energy grain boundaries with Σ = 1 representing a single crystal and Σ = 3 a twin boundary. For grain boundaries that form between in-plane rotated grains, as they are observed in this work, Σ can be calculated by dividing the basic unit cell area at the boundary interface with the periodically repeating lattice points of the grain surfaces when overlaid[65] as shown in **Figure 4**. This analysis yields a value of Σ = 11 for the grain boundary shown in Figure 3a, indicating indeed a low-energy grain boundary. Due to computational limitations, usually simplified model systems are implemented in ab-initio simulations of grain boundaries in monoclinic systems, such as hafnia.[17,48] Here, we observe a real grain boundary at atomic resolution giving a realistic picture of defect densities within grain boundaries in hafnium oxide.

From the experimental dataset shown in Figure 3, the distances of the ending (11$\bar{1}$) lattice planes of grain 2 in the inverse fast Fourier transformation (IFFT) shown in Figure 2b exhibit an average distance of 9.5 Å with a standard deviation of 0.8 Å. These sites can also be understood as dislocations cores of the ending half-planes. Similar to the CSL model, periodically repeating sites are observed for the single grains when cut along the ($\bar{1}\bar{1}\bar{2}$) and ($\bar{1}$21) planes, respectively. The spacing for this periodicity is given as 9.45 Å, as marked in Figure 4.

First principles density functional theory (DFT) calculations are performed to predict the atomic structure of the interface between the ($\bar{1}\bar{1}\bar{2}$) and ($\bar{1}$21) terminated grains (see Section 4 for details). As shown in Figure 3c, the structure that is predicted to be most stable shows a good semi-quantitative agreement with the experimental HAADF-STEM image (the GB structure is visualized using VESTA[67]). There are relatively few undercoordinated oxygen or hafnium ions at the grain boundary helping to explain its high stability.

For the case of gate insulators, grain boundaries including the high-*k* material hafnium oxide, have been identified as preferential leakage paths with increased mobility of vacancies and reduced diffusion barriers for charged species.[17,19,20,48,50,68] Here, we use this major disadvantage of a gate dielectric as a key advantage of resistive switching materials toward control of the soft electric breakdown, pinning of the conducting filament, and defining the switching position. In the rest of the paper, we show how the microstructure of the hafnia-based stack correlates with the electric switching behavior. The first striking result is that all devices with similar grain structure (as expected from the growth conditions), show indeed forming-free behavior. An exemplary forming step (dotted olive curve) shown in **Figure 5**a exhibits a low forming voltage of –1.975 V although the initial resistance of the DUT is as high as 11.5 GΩ at –0.1 V. The empirical cumulative probability of forming voltages of all 88 tested devices is plotted in Figure 5c proving a narrow distribution of forming voltages around –2 V (average of –1.94 V with a standard deviation of 0.21 V). This value is below the maximal voltages found for the set (V_{set}) and reset (V_{reset}) voltages, hence, the devices can be considered as forming-free for practical application in memories. On the other hand, a change in current levels is observed, indicating that a weak forming process is taking place at voltages approaching V_{set}, and therefore, the devices could also be considered as weakly forming devices. Usually, highly crystalline or single crystalline dielectrics show a high breakdown voltage. Only in highly oxygen deficient devices, similar low forming voltages were achieved.[3] With the help of grain boundary engineering, even in highly crystalline samples,

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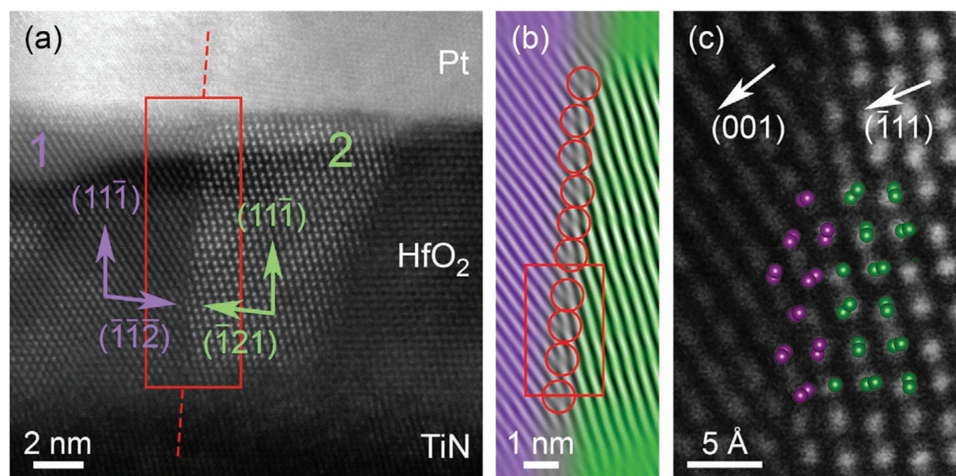

Figure 3. HAADF analysis of a Pt/HfO_2/TiN stack. a) HAADF-STEM image of the stack. In the dielectric layer, a grain boundary between a ($\bar{1}$10) oriented grain (1) and a ($\bar{1}0\bar{1}$) oriented grain (2) is marked, the orientation is given along the direction of view (note: length of vectors is not normalized). The dashed line indicates the grain boundary plane depicted in Figure 4c. b) Inverse Fast Fourier Transformation (IFFT) of the d_{001} and d_{-111}-filtered FFT of grains 1 and 2, the discontinued (001)/($\bar{1}$11) lattice planes are identified for the adjoining grains. Coincident site lattice (CSL) points are marked. c) HAADF-STEM image of the area marked in (b) with inset showing the density functional theory model of the grain boundary. Hf-ions in grains 1 and 2 are represented as purple and green spheres, respectively.

forming-free devices can be achieved due to the well-defined continuous grain boundaries connecting bottom and top electrode. Grain boundaries are known to act as sinks for defects, for example, oxygen vacancies, and thereby are accompanied by increased local conductivity, thus, being preferential sites for filament formation[20,50] leading to the observed reproducible low forming voltage. As visible in the discussed scanning transmission electron microscopy image (see Figure 3b), a high-defect density in the hafnium cation sublattice is evident in the grain boundary vicinity. Considering charge neutrality, this is probably accompanied by an increased local defect density in the oxygen anion sublattice, namely oxygen vacancies. Additionally, dislocations and grain boundaries have been correlated to a local oxygen deficiency or accelerated diffusivity in hafnium oxide and other oxide materials.[69–74]

Complementary, our investigations on forming voltages of less textured polycrystalline (with random grain boundary network) and amorphous HfO_2 layers are included in Figure S1, Supporting Information to highlight the effect of the grain boundary engineering on the forming voltage distribution.

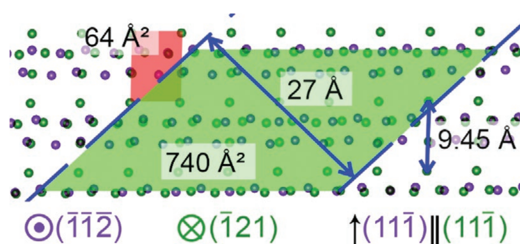

Figure 4. VESTA model of the grain boundary interface. The viewing direction is the grain boundary plane normal ($\bar{1}\bar{1}\bar{2}$) for grain 1 (also indicated in Figure 3a). The distance of the Moiré fringes is marked with dashed blue lines and the periodic distance is 27 Å. This spacing is used for the definition of the CSL unit cell (shaded in light green) which is then compared to the smallest unit cell of the periodicity along the cutting plane (red). Also, the periodic spacing in growth direction of 9.45 Å is given. Additional information is available in the Supporting Information.[66]

As can be seen in Figure 5a, the samples show stable bipolar resistive switching (BRS) for over 1000 DC cycles with high on/off-ratios of ≈50. The color coding from dark to bright (red) indicates steps of 100 cycles showing abrupt set and reset characteristics. The resistance distribution of high-resistance (HRS) and low-resistance states (LRS) of over 1000 DC cycles are plotted in Figure 5b. The high-resistive state starts in the MΩ region, and settles down at around 20 kΩ. The exact nature of this training effect is not yet understood and probably involves the interaction of the electrode material with the grain boundary. The LRS splits into two distinct resistance levels. This is a hallmark of the superposition of two different switching modes, a figure eight-wise (f8) and counter figure eight-wise (cf8) BRS of opposite polarity, which was attributed to switching at both electrode interfaces and appeared in highly oxygen deficient devices.[3,75] In our case, the low forming voltage in combination with the predefined path for filament formation along low-energy grain boundaries leads to a uniform filament, thus, both interfaces remain active in the switching process leading to two switching modes of opposite polarity resulting in the observed f8 and cf8 BRS.[75] The similarity of the here observed switching characteristics with previously reported RRAM devices[3,75] suggests the same underlying switching mechanism being based on an oxygen vacancy mediated current path. This is further corroborated by the refined current–voltage characteristics of the LRS and HRS consistent with a space charge limited charge transport (see Figure S3, Supporting Information).[76]

In Figure 5c, the empirical cumulative distribution for the set and reset voltages of the 1000 BRS cycles (Figure 5b) are shown. Considering the distribution of set and reset voltages with an average of −1.31 and 1.54 V, a maximum of −2.05 V and 2.35 V, and a standard deviation of 0.15 and 0.27 V, respectively, the predefined breakdown path provided by the well-defined grain boundaries has a positive effect on cycle-to-cycle

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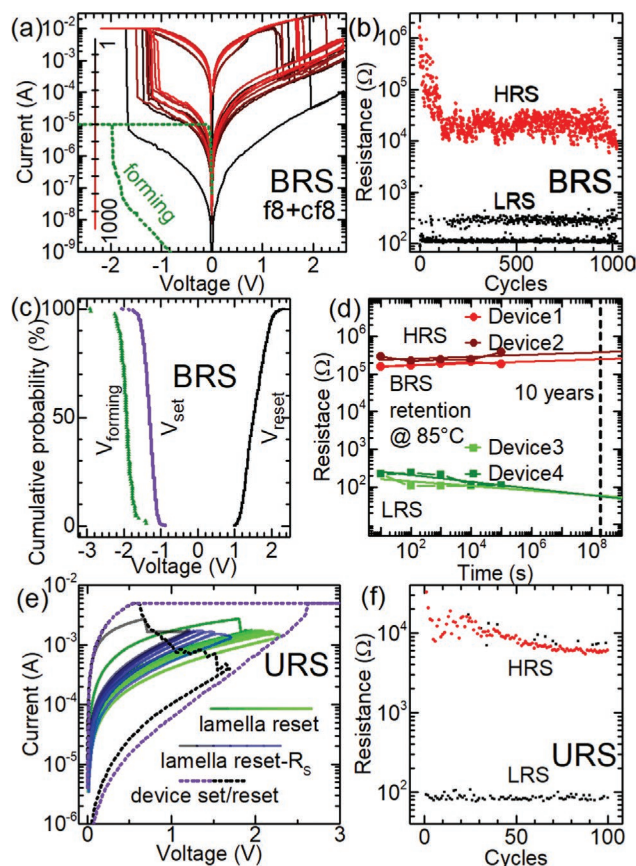

Figure 5. Electric characterization of the Pt/HfO_2/TiN stack. a) Bipolar resistive switching cycles of 1000 DC cycles—exemplary curves of every 100 cycles are shown. The dotted line (olive) represents the initial forming step. b) HRS and LRS resistance versus BRS DC cycles for 1024 cycles. c) Set, reset, and electroforming voltage distribution. d) BRS data retention characteristics of different devices set to either HRS or LRS obtained through exposure to elevated temperature (85 °C) for different time periods. e) Unipolar resistive switching behavior of a planar device (light [purple]/dark [black] dotted curve for set/reset) in comparison to the obtained unipolar reset of the prepared lamella device (light green curves). By calculating the series resistance, R_S, attributed to the contacts to the lamella, the voltage drop and resistance of the lamella "device" was obtained (full dark blueish curve). f) HRS and LRS resistance versus URS DC cycles for 100 cycles.

variation[77] compared to similar device stacks reported in literature.[78–82] For the effect of different degrees of crystallinity on the forming voltage, refer to Figure S1, Supporting Information. High-temperature data retention measurements were carried out at 85 °C, as depicted in Figure 5d. Both the LRS, as well as the HRS resistance shows promising characteristics and data is retained in both states as shown by the 10-year extrapolation.

Figure 5f shows that for 100 cycles, the LRS and HRS can be obtained also in the URS switching mode with some cycles exhibiting threshold switching.[3]

Finally, we give an outlook on how the here described devices will be used in future to obtain an atomistic correlation between switching behavior and microstructure in a device observed *operando* inside a transmission electron microscope. We prepared a TEM lamella of the TiN300 sample and electrically connected bottom and top electrode on a DENSsolutions electrical biasing chip in the same manner as reported previously.[38] In Figure 5e, the curves represent the step-wisely performed unipolar reset process on the lamella while the dark (purple and black) dotted lines represent the unipolar set and reset operation on the planar reference device. Although the current levels of the step-wise reset in the lamella coincide with the gradual steps of the reset of the reference device reset, the reset voltages are shifted by about 1 V. This can be explained by an additional serial resistance due to the electrical contact of the lamella on chip. By assuming that the same amount of current passes through an additionnal constant contact resistance, R_s, and through the device structure, as well as that the lamella and the reference device have a similar reset voltage, R_s was estimated to be 420 Ω. By this, the actual voltage drop over the lamella and the resistance of the lamella device could be recalculated as shown in Figure 5e resulting in a convincing match between the lamella and the reference device. Thus, the lamella switching behavior reproduces the switching behavior observed in a real device—a first big step toward *operando* TEM investigations, which might finally resolve highly debated questions as, for example, the exact rupture region during the reset process.[39,83–85]

3. Conclusion

To summarize, we described a novel way to achieve forming-free RRAM devices by grain boundary engineering. We demonstrated the growth of highly textured hafnia on the industrially relevant electrode material TiN, which itself was also grown in a highly textured manner onto (0001) orientated Al_2O_3 substrates. It was shown that the threefold symmetry of the substrate was transmuted to a sixfold system in the TiN layer due to an in-plane rotation of 60° of the (111) oriented TiN grains. To each orientation of the TiN, three preferred in-plane rotated hafnia growth orientations have been correlated, which resulted in a defined subset of possible grain boundaries of high symmetry. When choosing the growth conditions such that the grain size is of the order of the film thickness, these well-defined grain boundaries interconnect both electrodes. This novel way of grain boundary engineering was utilized to fabricate RRAM devices with forming-free behavior and low variation of forming voltages. The devices show stable resistive switching characteristics in both, unipolar and bipolar resistive switching mode. Due to the epitaxial relation of the hafnia and the TiN layer, an atomic-resolution scanning TEM-based characterization of the system was achieved giving additional information about the microstructure and defect density at the grain boundaries. Therefore, the demonstrated system is proposed as an ideal system for *operando* TEM investigations of the resistive switching process in hafnium-oxide-based devices. A first working and contacted TEM lamella was demonstrated showing excellent comparability to the planar reference devices. Grain boundary engineering in resistive switching devices is a novel route that contributes to a better understanding and precise control of the conducting filaments in RRAM devices.

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4. Experimental Section

Grain boundary engineered metal–insulator–metal (MIM) stacks of TiN/HfO_2/Pt had been grown onto *c*-cut sapphire substrates using molecular beam epitaxy (MBE) in a custom designed ultra-high vacuum chamber with a base pressure of 10^{-9} mbar. TiN and hafnium oxide layers had been grown by elemental electron beam evaporation of Ti and Hf, respectively. In situ nitridation and oxidation was performed using radio frequency (rf)-activated nitrogen and oxygen radicals from a radical source, respectively. Gas purity was 5N in both cases, 3N Hf from MaTeck and 4.5N Ti from Lesker were used. The growth temperature for the TiN bottom electrode was 810 °C, at 0.3 Å s^{-1} growth rate, whereas the nitrogen flow through the radical source was constant at a flow rate of 0.8 standard cubic centimeter per second (sccm) of nitrogen and an rf-power of 330 W. The growth of the hafnium oxide layer was performed at 525 °C at 0.7 Å s^{-1} growth rate, utilizing a flow rate of 1 sccm of oxygen and 200 W rf-power. The stack combinations with amorphous and polycrystalline hafnium oxide have been grown with identical deposition conditions by only varying the substrate temperature in the growth process of the hafnia layer to room temperature and 320 °C, respectively. For all samples, the top electrode was deposited by sputtering 100 nm of platinum using a Quorum sputter coater. After sputtering the top electrode, the samples were subjected to a standard lithography step using a lift-off process in order to produce MIM devices of 30×30 μm^2 size. The amorphously grown hafnium oxide layers were found to crystallize to a polycrystalline state after being exposed to a heating procedure at 200 °C under ambient atmosphere and a duration of 20 min. Structural characterization utilizing X-ray diffraction (XRD) was performed using a Rigaku SmartLab diffractometer in parallel beam geometry employing copper K_α radiation. Film thicknesses were calculated by fitting X-ray reflectivity (XRR) data using RCRefSim.[86] Film growth was monitored by in situ reflection high-energy electron diffraction (RHEED) performed at 25 kV acceleration voltage. Electrical characterization was done using a Keithley 4200 semiconductor characterization system (SCS). For the device under test (DUT), the top electrode was biased while the bottom electrode was grounded. The internal current compliance (CC) of the SCS was used to prevent device hard breakdown.

HAADF and bright-field scanning transmission electron microscopy (BF-STEM) was performed on a JEOL JEM-ARM200F, while spatially resolved electron diffraction pattern acquisition for orientation mappings (ASTAR) was performed on a JEOL JEM-2100F, both operated at 200 kV. TEM sample preparation was performed in a JEOL JIB-4600F focused ion beam (FIB) system. The TEM lamella was then electrically contacted onto to a MEMS-based chip sample carrier device as described by Zintler et al.[38] The defined electrical contacts allowed the application of an electrical stimulus directly on the lamella while inside the transmission electron microscope.

Density functional calculations were performed using the projector augmented wave (PAW) method and the generalized gradient approximation of Perdew, Burke, and Ernzerhof (PBE)[87] as implemented in the Vienna Ab-Initio Simulation Package (VASP).[88,89] The bulk structure of *m*-HfO_2 is optimized using a 400 eV plane wave cut-off (standard Hf and soft oxygen PAW potentials) and a Monkhorst–Pack k-point grid of $11 \times 11 \times 11$ yielding lattice constants within 0.5% of experimental values (Table S2, Supporting Information). To model the grain boundary, a supercell containing the $(\bar{1}\bar{1}\bar{2})$ and $(\bar{1}21)$ oriented *m*-HfO_2 grains is constructed as shown in Figure S2, Supporting Information. In order to make a commensurate supercell, strain is applied to both grains parallel to the interface (<10%). We verified this does not have a significant effect on the structure or electronic properties. It is common practice to include two grain boundaries in the supercell to make it three dimensionally periodic.[17,90,91] However, for this asymmetric grain boundary, it is difficult to construct a supercell with two equivalent interfaces making assessment of stability difficult. Therefore, instead we include only one grain boundary and a 10 Å vacuum gap separating the two free surfaces. The relaxation of the surfaces is found to be well localized to the surface region and therefore does not impact on the grain boundary structure. To determine the most stable configuration, a gamma-surface scan of grain boundary translation states is carried out (in steps of around 1 Å in both directions parallel to the grain boundary). The most stable structure obtained is shown in Figure S2, Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

grain boundary engineering, hafnium oxide, resistive switching memory, texture transfer, transmission electron microscopy

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