DESIGN OF CLASS F-BASED DOHERTY POWER AMPLIFIER FOR S-BAND APPLICATIONS

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ABSTRACT

Design of Class F-based Doherty Power Amplifier for S-Band Applications

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Modern RF and millimeter-wave communication links call for high-efficiency front end systems with high output power and high linearity to meet minimum transmission requirements. Advanced modulation techniques, such as orthogonal frequency-division multiplexing (OFDM) require a large power amplifier (PA) dynamic range due to the high peak-to-average power ratio (PAPR). This thesis provides the analysis, design, and experimental verification of a high-efficiency, high-linearity S-band Doherty power amplifier (DPA) based on the Class F PA. Traditional Class F PAs use harmonically tuned output matching networks to obtain up to 88.4% power-added efficiency (PAE) theoretically, however the amplifier experiences poor linearity performance due to switched mode operation, typically yielding less than 30dB C/I ratio [1]. The DPA overcomes this linearity limitation by using an auxiliary amplifier to boost output power when the amplifier is subject to a high input power due to its limited conduction cycle. The DPA also provides improved saturated output power back-off performance to maintain high PAE during operation.

The DPA presented in this thesis optimizes PAE while maintaining linearity by employing harmonically tuned Class F amplifier topology on a primary and an auxiliary amplifier. A Class F PA is first designed and fabricated to optimize output network linearity – this is followed by a DPA design based on the fabricated Class F PA. A GaN HEMT Class F PA and DPA operating at 2.2GHz are implemented with the PAs measuring 40% and 45% PAE respectively while maintaining a 30dB carrier-to-intermodulation (C/I) ratio on a two-tone test. The PAE is characterized at maximum 21dBm input power per tone and 20MHz tone spacing. When subject to a single 24dBm continuous wave input tone, the Class F PA and DPA output 37dBm and 35.5dBm respectively. The PAs presented in the thesis provide over 30dB C/I ratio up to 21dBm input tones while maintaining over 40% PAE suitable for base station applications.

Keywords: Doherty Power Amplifier, Class F Amplifier, S-Band, GaN HEMT, PAE, Linearity

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1. INTRODUCTION

The Doherty power amplifier (DPA) has seen increased use in the last several years, particularly in base stations for cellular telecommunication systems. As mobile communications continue to expand, array-based communication systems with multiple input, multiple output (MIMO) has become a prevalent topology. Modern wireless communications standards, such as 4G and 5G, employ complex modulation schemes, such as orthogonal frequency-division multiplexing (OFDM), where digital predistortion (DPD) is unable to meet demands for massive MIMO and wide bandwidth. Unfortunately, OFDM inherently suffers from high peak-to-average power ratio (PAPR) due to wide output power swings caused by constructive and destructive sinusoidal interference. Power amplifier (PA) nonlinearities also degrade high PAPR signals and increase in-band distortion leading to decreased system performance [2]. Therefore, modern wireless systems impose stringent linearity and efficiency requirements on amplifiers – these systems call for large dynamic range to minimize signal distortion are require maximum efficiency for mobile applications.

Traditional amplifier topologies (such as Class AB) achieve high efficiency by driving the amplifier well into compression. However, amplitude-to-phase modulation and intermodulation products degrade linearity. High PAPR signals potentially cause signal clipping (distortion) which inhibits spectral reconstruction. Class F amplifier biasing issues degrade linearity, however harmonic frequency control minimizes power dissipation. The DPA maintains high efficiency by operating at output power back-off (OPBO) where the amplifier is typically 3-6dB below the output power saturation point. When faced with a high peak power, the DPA uses an auxiliary amplifier to boost the output power and maintain linearity. This thesis explores the design, fabrication, and tests on a Class F PA and a Class F-based DPA for use in a high-efficiency, high-linearity competition.

1.1 Statement of Problem

Each year, the IEEE Microwave Theory and Techniques Society (MTT-S) International Microwave Symposium (IMS) hosts a Student Design Competition (SDC) focusing on the design and implementation of a High-Efficiency Power Amplifier (HEPA). Undergraduate and graduate students are invited to build and compete for the highest figure of merit (FOM) score based on the measured PAE and operating frequency.

The goal of this thesis is to design and test a high-efficiency PA meeting the design requirements listed by the HEPA-SDC competition rules [3]. The PA must output at least 4W (up to 40W) when excited by a single input tone no greater than 24dBm at a selected frequency between 1-10GHz. Additionally, the PA must maintain at least 30dB carrier-to-intermodulation (C/I) ratio as the input power tones are swept from 0dBm up to 21dBm per tone with 20MHz spacing about a chosen center frequency.

1.2 Detailed Competition Rules

The SDC-HEPA competition rules are listed as follows [3]:

a. The power amplifier (PA) design may use any type of technology, but must be the result of new effort, both in the amplifier design and fabrication.

b. The PA mechanical design should allow for internal inspection of all relevant components and circuit elements. The RF ports should be SMA female connectors. Bias connections should be banana plugs.

c. The PA should require a maximum of two dc supply voltages for operation.

d. The PA must operate at a frequency in the range of 1GHz to 10GHz and have an output power level when excited by a single carrier of at least 4 watts, but no more than 40 watts at the frequency of test.

e. All PAs should require less than 24dBm of input power to reach the minimum 4-watt output power when excited with a single carrier.

f. All linearity measurements will be performed under CW (continuous wave) two-tone operation with two equal amplitude carriers spaced 20MHz apart at room ambient

conditions into a 50-ohm load. Only the power at the two fundamental carrier frequencies will be included in the measurement of output.

g. Linearity measurements will be conducted with a maximum of 21dBm input power per tone. The tone power will be swept from 0dBm to 21dBm and the C/I ratio measured.

h. The winner will be based on the amplifier's PAE measured during official testing at the lowest power level for which the C/I ratio equals 30dB. If the C/I ratio is better than 30dB over the entire testing range, the measurement at 21dBm input power per tone will be used. The figure of merit for scoring will be the PAE multiplied by a frequency weighting factor having the form (GHz)^0.25.

The final measurement results are performed by the IMS-SDC committee members with drain and gate biasing and center frequency selected by the student.

1.3 Thesis Organization

The thesis is organized as follows:

Chapter II introduces common PA figures-of-merit, PA topologies, and the high-frequency PA transistor technologies.

Chapter III presents the Class F amplifier design methodology. This will cover the Class F operational theory and common design considerations for amplifier design.

Chapter IV presents the DPA designed and implemented including DPA architecture background and recent linearity and efficiency enhancements.

Chapter V provides the simulation results for the designed Class F and DPA.

Chapter VI covers the PCB fabrication and amplifier assembly instructions.

Chapter VII provides experimental performance of the designed Class F and Doherty power amplifiers. The lab bench test configuration is presented along with the experimental results.

Chapter VIII concludes the thesis with project results and suggestions for improvement.

2. BACKGROUND

2.1 Power Amplifier Figures-of-Merit

The primary function of an RF power amplifier is to increase electrical signal amplitude through gain, which is defined as the ratio of output power to input power (expressed in dB). An ideal amplifier amplifies the input signal and outputs an undistorted, unclipped signal [4].

PA electrical performance is characterized by the following figures-of-merit (FOM): gain saturation, linearity, and efficiency. Gain saturation is defined by the 1dB compression point (P1dB) and the saturated output power (P_{sat}) in dBm or Watts, the maximum output power produced for a given frequency, bias, and output load. P_{sat} is characterized by a constant output power over a defined input power range. P1dB (dBm) is the output power where the input power deviates by 1dB from the low-power gain slope. Figure 2.1 provides the typical gain, output power, and PAE curves over input power for an ideal PA.

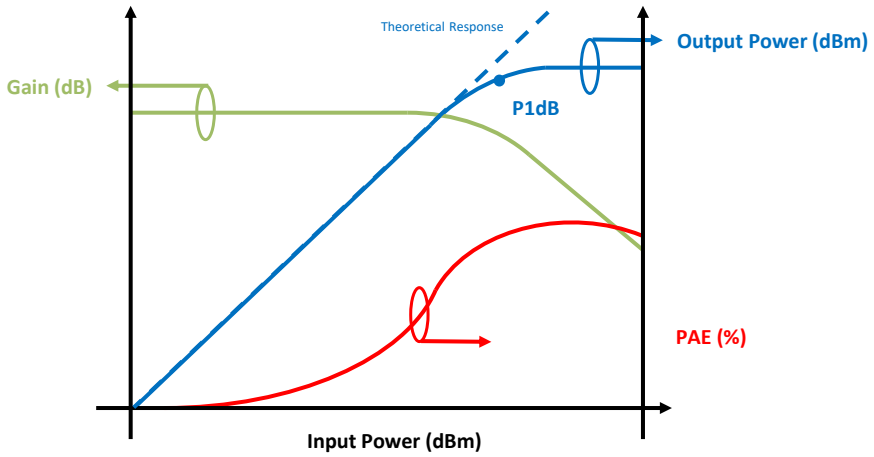


Figure 2.1: Typical Amplifier Output Power (dBm), Gain (dB), and PAE (%) vs Input Power.

Driving amplifiers into gain compression causes signal distortion, harmonics, and intermodulation products. Single input tone non-linear products (such as $2f_0$ and $3f_0$) are well outside of the operating frequency range and can be filtered out. However, multi-tone distortion products can occur near the two fundamental frequencies resulting in intermodulation distortion (IMD). When presented with a two-tone input, IMD is realized as the third-order intermodulation products (IM3) which are seen at $2f_1$-f_2 and $2f_2$-f_1 and as the second-order intermodulation product (IM2) which are seen at f_1+f_2 and f_1-f_2. The IM3

products typically fall within a PA's operating bandwidth – any products outside of this bandwidth can be filtered out. The two-tone carrier-to-intermodulation ratio (C/I), expressed in dBc relative to the fundamental tone power, represents the ratio between one fundamental frequency power and the one of the IM3 products. Figure 2.2 provides the typical output spectrum for two-tone tests on a PA:

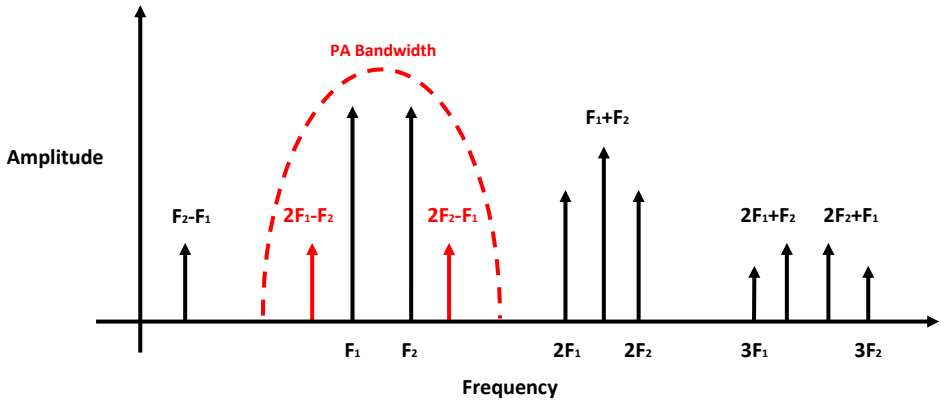


Figure 2.2: Two-Tone 2nd and 3rd Order Harmonic Intermodulation.

As two-tone input power increases, the IM3 ratio decreases until the IMD products equal the fundamental tone power at the third-order intercept (TOI) point or IP3. Figure 2.3 shows the relation between fundamental output power, 3rd-order IMD output power, and the TOI point:

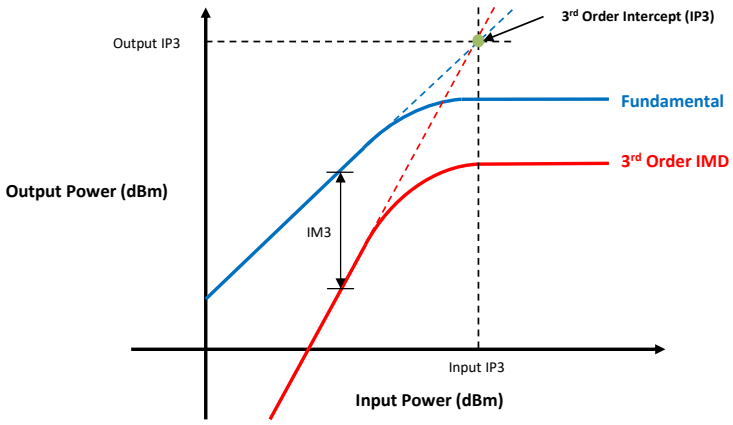


Figure 2.3: Fundamental and 3rd-Order IMD vs. Input Power.

Amplifiers with large IP3 exhibit enhanced linearity; the device maintains linearity over a wider input power range [5]. In other words, high linearity allows for high gain without signal distortion.

Efficiency (η) the ratio of signal power delivered to the load over the DC power supplied to the circuit:

$$\eta = \frac{P_{RF,Output}}{P_{DC}} * 100\% \quad (2.1)$$

In FET devices, η is drain efficiency and provides how much DC power is converted to RF power. Efficiency defines a DC-powered device's effectiveness. In mobile applications, such as mobile radar systems, maximized efficiency extends the effective range.

Power added efficiency (PAE) is more commonly used to define RF amplifier efficiency::

$$\text{PAE} = \frac{P_{RF,Output} - P_{RF,Input}}{P_{DC}} * 100\% \quad (2.2)$$

where $P_{RF,Output}$ - $P_{RF,Input}$ is known as the added power. PAE is preferred since it includes amplifier gain and DC bias power. All RF and DC power input not converted into RF power is dissipated as heat which can degrade component reliability and decrease the mean time to failure (MTTF). While decreasing the DC power seems simplest in increasing efficiency, biasing limitations for transistors limit the minimum practical DC power consumption. In addition, decreasing the drain supply voltage limits the transistor's dynamic range which may lead to signal clipping and distortion.

When the amplifier gain is relatively high, the PAE becomes approximately equal to the drain efficiency. For amplifiers with moderate gain, a high input RF power will result in increased PAE - driving the amplifier well into saturation improves efficiency since the added power is minimized. However, IMD increases significantly as 3rd order products increase by a factor of 3 over an increase in fundamental power.

2.2 Power Amplifier Topologies

Amplifiers operating from very low frequency (VLF) through microwave frequencies are grouped into the following classes: A, B, AB, C, and D through F [6]. Amplifier class performance is based on operating modes and bias conditions. Figure 2.4 shows the amplifier classes divided into two categories based on their operation method: biasing amplifiers and switching amplifiers [6].

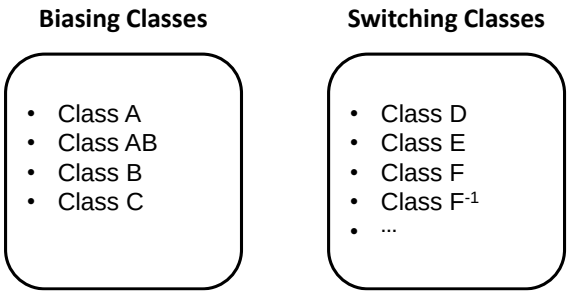


Figure 2.4: PA Classes and Classifications.

Class A, B, AB, and C amplifiers are defined by input signal conduction angle, or the ratio of ON to OFF times. Alternatively, they are categorized by quiescent bias conditions which limit the output current conduction angle. In general, biasing amplifiers have limited efficiency due to large conduction angles, however output signals have less distortion through improved linearity [6]. On the other hand, switching-type amplifiers maximize efficiency with reduced linearity due to switching. These amplifiers employ pulse width modulation (PWM) or output network harmonic tuning to maximize efficiency.

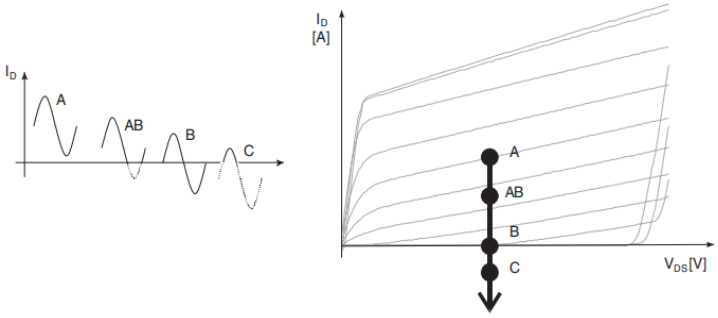


Figure 2.5: Biasing Class Amplifier Conduction Angle and Quiescent Biasing Points [6].

Figure 2.5 shows the conduction angle and quiescent biasing points for Class A, AB, B, and C PAs. Class A amplifiers are biased at half of the rail voltage allowing full conduction throughout the waveform

cycle. This allows the input signal amplification without distortion, however it is inherently inefficient at maximum 50% efficiency due to the constant DC power supply biasing the transistor [6].

Class B amplifiers conduct for half the cycle leading to increased efficiency (theoretically 78.5% maximum) [6], however there is increased harmonic and cross-over distortion due to operation near the transistor's cutoff region. These amplifiers have poor linearity; low-amplitude input signals are often distorted by push-pull amplifiers operating near the cross-over region.

Class AB amplifiers optimize efficiency and linearity between Class A and Class B amplifiers. These amplifiers conduct over 180° to 360° of the input cycle [6]. Class AB amplifiers overcome Class B cross-over distortion by overlapping "on-times" between the push-pull amplifiers. This significantly improves efficiency with a slight increase in power consumption.

Class C amplifiers conduct less than 50% of the input cycle for maximum efficiency among biasing class amplifiers. However significant signal distortion occurs due to non-linear operation. Class C amplifiers minimize DC power consumption by minimizing conduction angle, which increases nonlinearity. Additionally, Class C amplifiers risk damage from transistor reverse breakdown due to biasing [6].

Class D through T are non-linear amplifiers designed to maximize efficiency at the cost of increased signal distortion. Switching-mode amplifiers, such as Class D amplifiers, operate via pulse-width modulation (PWM). An analog signal is input into a comparator alongside a triangle wave to create a PWM signal. The PWM signal drives the gates of two output MOSFETs that pull the output to either the supply rail or ground, creating a square wave proportional to the input signal level. This is fed through a series lowpass filter to recover an amplified input signal. Class D amplifiers have theoretically 100% efficiency since current only conducts to the load when the switch is fully on [6].

Class E also falls into switching-mode amplifiers. The goal for Class E amplifiers is to maintain two conditions for ideal switch behavior: zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) [6]. During ZVS, the voltage across the active device must be minimized while current is flowing. ZVDS requires minimum switching time to eliminate overlapping non-zero voltage and current waveforms [6]. The output tuning circuit is designed to resonate at the fundamental frequency such that any harmonic power is delivered as reactive power to the load. Figure 2.6 shows the ideal Class E

schematic and ideal drain current and voltage waveforms to minimize active device power dissipation:

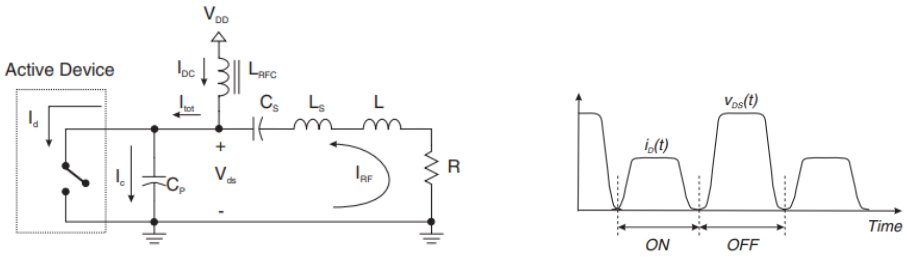


Figure 2.6: Simplified Class E Topology and Idealized Drain Current and Voltage Waveform [6].

Class E amplifiers are simpler than harmonically tuned amplifiers, but must be overdriven into compression which limits large-signal gain and maximum operating frequency [6].

Current-mode amplifiers, such as Class F, rely on harmonic generation to manipulate the drain voltage and current waveforms. For low frequency applications, harmonics generated by non-linear operation can be effectively controlled to maximize efficiency. By Fourier analysis, the output voltage waveform is transformed into a 50% duty cycle square wave while the current waveform is converted to a half-cycle sinusoid 180° out of phase from the voltage. This effectively minimizes power dissipated by the active device similar to Class E operation. Further discussion of the Class F amplifier topology and operational theory will be discussed in Chapter 3. Table 2.1 below summarizes key parameters for the different amplifier classes:

Table 2.1: Amplifier Topology Theoretical Efficiency and Linearity [1], [6].

Class	Theoretical Maximum Efficiency (%)	Linearity
A	50	Good
B	78.5	Poor
AB	50-78.5	Moderate
C	100	Poor
D	100	Poor
E	100	Poor
F	88.4%	Poor

Based on these "traditional" topologies, the efficiency vs. linearity tradeoff presents a design challenge: maximizing linearity while maintaining high efficiency. Modern wireless communications systems require maximum efficiency for mobile applications and maximum linearity to accommodate complex modulation schemes.

The Doherty amplifier, invented by William H. Doherty in 1936, uses a high-linearity amplifier (such as Class B) and boosts the output power and efficiency using an auxiliary amplifier in parallel with the primary amplifier [7]. The auxiliary amplifier typically uses a switched bias to maximize output power when on and minimize power consumption when off. Modern Doherty configurations use a parallel carrier and peaking amplifier: the carrier amplifier provides the required gain and output power, while the peaking amplifier operates on a limited basis to increase power throughput and improve system efficiency. At low input power, the carrier amplifier provides consistent, linear gain. However, the bias is often optimized for low average power operation. Distortion (clipping) occurs for relatively large input signal amplitudes. The peaking amplifier operates when the carrier amplifier reaches compression to increase output power and maintain output signal linearity. The peaking amplifier biases allows conduction for a short input power duration, therefore maximizing efficiency when the input power is backed off and maintaining efficiency when the input power is relatively high [7]. Figure 2.7 shows the simplified DPA schematic:

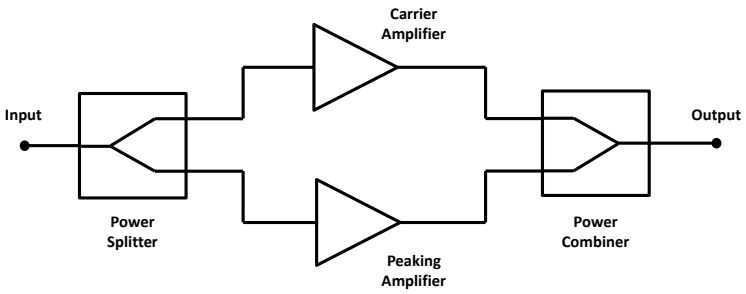


Figure 2.7: Simplified Doherty Amplifier Schematic.

In recent years, IMS HEPA-SDC winners have consistently demonstrated the Doherty amplifier's linearity and efficiency capabilities, typically maintaining at least 30dB C/I ratio with PAE of over 50% [8]. Doherty amplifier topology analysis is discussed in Chapter 4.

2.3 Power Amplifier Technologies

Modern monolithic microwave integrated circuits (MMIC) devices are constructed on gallium arsenide (GaAs) semiconductor for a variety of components from amplifiers to filters and to switches. GaAs offers low intrinsic noise figure and are commonly found on RF front end systems. The low 1.42eV bandgap energy, compared to GaN's 3.425eV, [9] makes GaAs an ideal solution for low-power applications in portable wireless devices.

Table 2.2: Semiconductor Substrate Material Properties [9].

Parameter	**Si**	**GaAs**	**GaN**
Bandgap Energy (eV)	1.12	1.42	3.425
Thermal Conductivity (W/m*k)	150	43	130
Electron Mobility (m^2/V*s)	0.15 (bulk) 0.3 (inversion)	0.85	0.125 (bulk) 0.2 (inversion)

Gallium nitride (GaN) has become a standard substrate for PAs due to its wider bandgap energy (3.425eV), high thermal conductivity (130W/m*K), and high electron mobility [9]. The high electron mobility enables high gain, high operating frequency, and low loss due to the fast electron movement [9]. The wide bandgap maximizes transistor output power due to increased breakdown voltage. Transistor operating temperatures increase through enhanced thermal conductivity, which transports heat

away from semiconductor junctions [9]. GaN devices are preferred for base station and microcell applications [11] due to greater power density and efficiency.

Figure 2.8 below defines output power vs. frequency regions for multiple semiconductor materials. GaAs offers wide frequency performance up to 100GHz; however, GaAs amplifiers typically are unable to output more than 5W in the 1-10GHz region. Within the 1-10GHz region, GaN PAs offer output powers well into the 10s and 100s of watts region. This makes GaN transistor a preferred material for a high-power, high-efficiency PA design meeting the HEPA-SDC design rules.

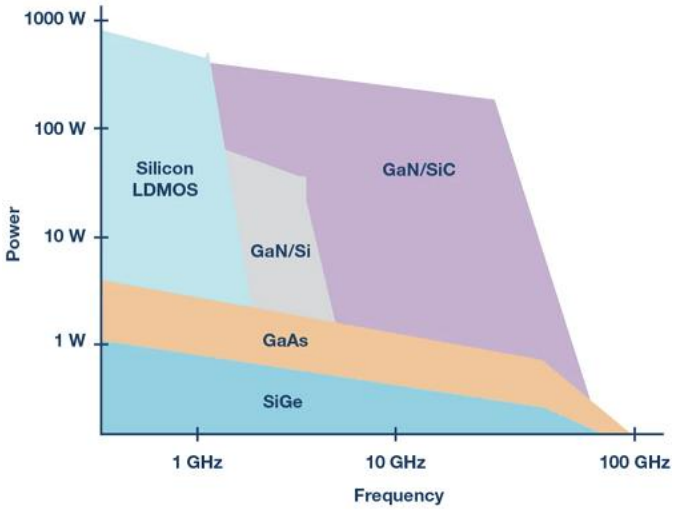


Figure 2.8: Semiconductor Material Output Power vs Frequency Regions [9].

Traditional semiconductors are typically metal-oxide semiconductor field-effect transistors (MOSFET). MOSFETs include a doped channel between drain and source. Channel width is controlled by the gate voltage. These transistors are suitable for mW-range, low frequency applications due to the low electron mobility. High-mobility transistor electrons (HEMT) build upon this structure by using two different materials with different band gaps in place of a doped-region channel. Figure 2.9 shows the typical stackup for a typical MOSFET compared to a GaAs HEMT:

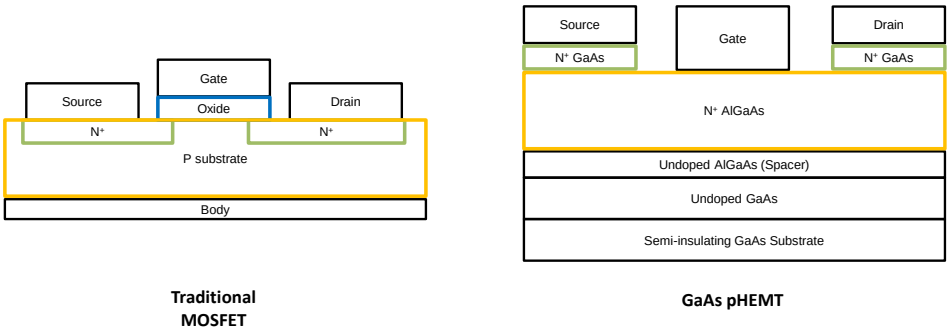


Figure 2.9: Standard MOSFET vs GaAs HEMT Structure.

The heterojunction formed by the HEMT structure enables high carrier mobility and switching speeds suitable for microwave applications [6]. Combined with the high power density and thermal conductivity of GaN, GaN HEMTs provide a compact, high-power transistor with excellent thermal and electrical efficiency. As a result, a GaN HEMT transistor is sought for the Class F PA and the Class F-based DPA.

3. CLASS F POWER AMPLIFIER DESIGN

This section details the operation and design of a Class F PA. The topology and operation theory are first defined, then general PA design procedures are presented. The final circuit schematic and layout are provided along with manufacturing details.

3.1 Class F Amplifier Topology

Class F amplifiers are biased slightly above Class B biasing in the "deep AB-biasing" region near the transistor's pinch-off point. This enables conduction during half of the input cycle. Half-cycle conduction generates significant harmonic frequency content undesirable for high-linearity PA operation, however Class F amplifiers control the 2nd and 3rd harmonics to prevent harmonic leakage, increase fundamental frequency throughput, and maintain high efficiency. In theory, Class F amplifiers can achieve 100% efficiency if an infinite number of harmonics are controlled, however harmonic control beyond the 2nd and 3rd harmonics results in higher circuit losses and increased design complexity [6]. Additionally, switching device parasitic capacitance limits the maximum frequency for output resonant circuits, hence an infinite number of harmonics cannot be controlled. Typical Class F topologies feature only 2nd and 3rd harmonic trapping.

The implemented output matching network generates an ideal square wave output voltage and half-sinusoidal output current, depicted in Figure 3.1. Equations 3.1 and 3.2 describe the drain voltage and current waveforms. Since non-zero voltage and current waveforms do not overlap, active device power consumption is minimized and power efficiency is maximized [6].

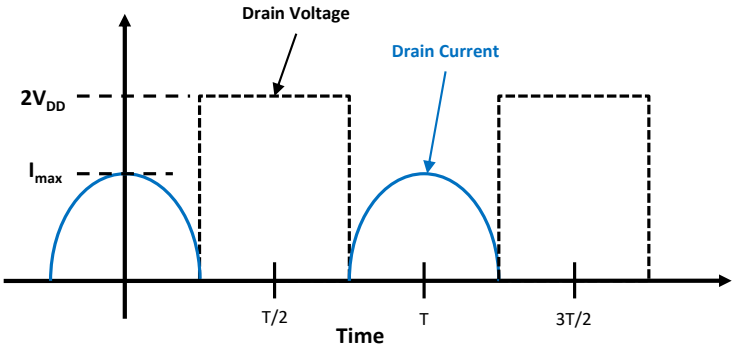


Figure 3.1: Ideal Class F Amplifier Drain Voltage and Current Waveforms.

Ideal drain current and voltage waveforms are defined as follows:

$$i_D(\theta) = \begin{cases} I_{max} \cdot cos(\theta) & if -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & otherwise \end{cases} \quad (3.1)$$

$$v_{DS}(\theta) = \begin{cases} 0, & if -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 2 \cdot V_{DD} & otherwise \end{cases} \quad (3.2)$$

To generate idealized waveforms, Fourier analysis defines waveform harmonic components. Fourier series expansion coefficients are:

$$v_{DS}(\theta) = \sum_{n=0}^{\infty} V_n \cdot cos(n\theta) \quad (3.3)$$

where V_n is described as:

$$V_n = \begin{cases} V_{DD} & n = 0 \\ -\frac{4 \cdot V_{DD}}{\pi} & n = 1 \\ 0 & n\ even \\ \frac{4 \cdot V_{DD}}{\pi} \frac{(-1)^{\frac{n+1}{2}}}{\pi} & n\ odd \end{cases} \quad (3.4)$$

Fourier series drain current waveform expansion is:

$$i_D(\theta) = \sum_{n=0}^{\infty} I_n \cdot cos(n\theta) \quad (3.5)$$

$$I_n = \begin{cases} \frac{I_{Max}}{\pi} & n = 0 \\ \frac{I_{Max}}{2} & n = 1 \\ \frac{2 \cdot I_{Max}}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2 - 1} & n\ even \\ 0 & n\ odd \end{cases} \quad (3.6)$$

A square wave voltage waveform requires only odd harmonics, while the half-cycle sinusoidal current waveform requires only even harmonics. The output termination impedance is:

$$Z_n = \frac{V_n}{I_n} = \begin{cases} \frac{8}{\pi} \cdot \frac{V_{DD}}{I_{Max}} & n = 1 \\ 0 & n\ even \\ \infty & n\ odd \end{cases} \tag{3.7}$$

This specifies that output matching terminations require even harmonic short circuits and odd harmonic open circuits. The fundamental frequency terminating impedance must be resistive and scaled by 4/π:

$$R_F = \frac{4}{\pi} \cdot \frac{2 \cdot V_{DD}}{I_{Max}} = \frac{4}{\pi} \cdot R_{TL} \tag{3.8}$$

where R_{TL} is the impedance for a tuned load condition described in [6]. The ideal Class F amplifier topology by [6] is drawn as:

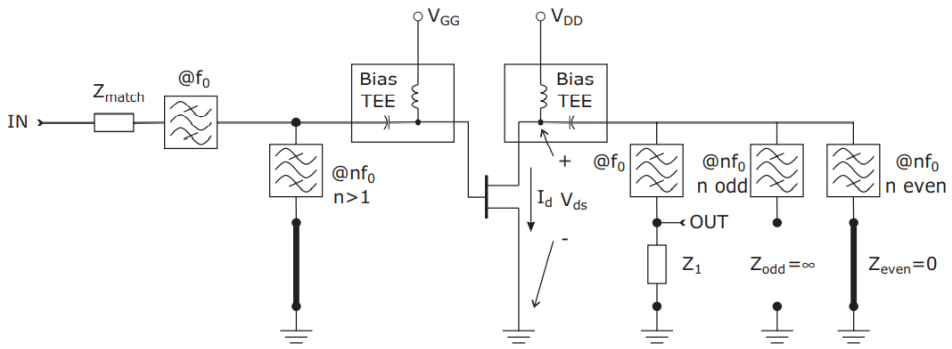


Figure 3.2: Ideal Class F Amplifier Schematic [6].

Figure 3.2 shows the ideal Class F amplifier schematic with a well-matched output for the fundamental frequency, an open circuit for odd harmonics, and a short circuit for even harmonics. Additionally, the input network is matched for the fundamental frequency with all harmonics shorted.

A transposed version can also be realized; the current is transformed into a 50% duty cycle square wave and the voltage into a half-sinusoidal waveform; the inverse Class F amplifier. The Class F^{-1} topology relies on a second harmonic open and third harmonic short termination, the opposite of the

Class F. Previous works by [12] and [13] have demonstrated 10% improved efficiency in the Class F^{-1} topology over the Class F.

3.2 Transistor Selection

For high-power, ultra-high frequency (UHF) band applications, GaN is the preferred technology as discussed previously. Several transistors were considered, including the following:

Table 3.1: PA Transistor Selection.

Transistor	**Pros**	**Cons**
CGH40010F	Used consistently in HEPA-SDC competitions	Not recommended for new designs by manufacturer (legacy part)
CG2H40010F	Updated CGH40010F model with higher gain and saturated output power	Out of stock at time of selection
CGH40006P	Good IM3 performance (based on eval board)	Lower gain and saturated output power than CGH40010F

CGH40010F was selected due to availability and its consistent use in previous winning designs. The transistor offers a typical saturated output power of 13W up to 6GHz. The transistor also has up to 16dB gain at 2GHz, 65% drain efficiency, and 28V drain bias operation. These traits are suitable to meet the HEPA-SDC contest rules provided the input and output networks are well designed. The ADS model for CGH40010F is compared to datasheet specifications [14] to confirm the model's accuracy as seen in Figures 3.3 and 3.4. Input and output impedances are idealized with values provided from the datasheet to match the CGH40010F evaluation circuit as closely as possible. Using ideal impedances, the following responses were simulated with transistor biasing at V_d = 28V and V_g set for I_{dq} = 200mA:

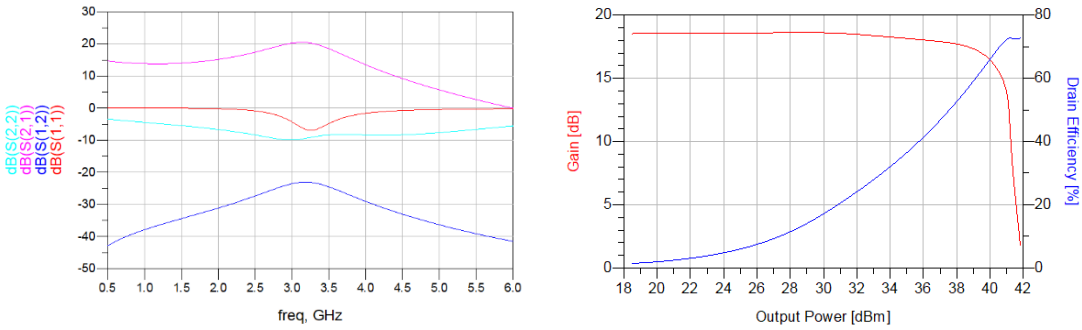


Figure 3.3: Simulated CGH40010F S-parameters, Gain vs Pout, and Drain Efficiency with Ideal Input/Output Impedances for 3.5GHz.

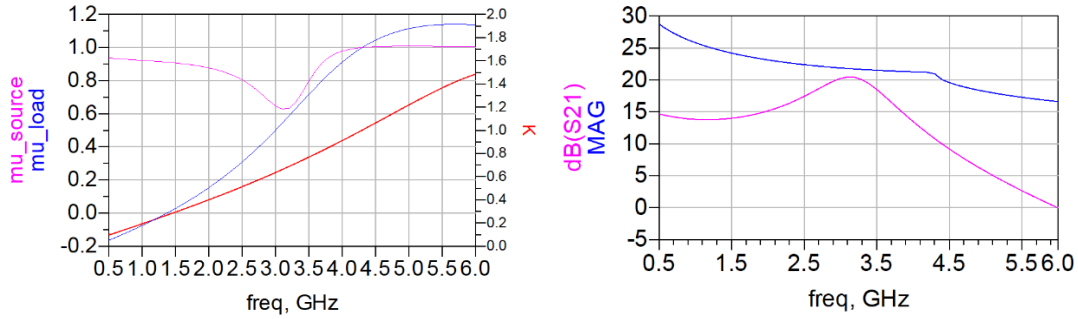


Figure 3.4: Simulated K Factor, Stability Analysis, Small Signal Gain, and Max Available Gain with Ideal Input/Output Impedances for 3.5GHz.

The simulated gain shows 5dB improvement compared to the datasheet [14] measurement when the input and output impedances are optimized for operating at 3.5GHz – this is attributed to circuit losses that were not modeled in simulation. The input power sweeps show a gain curve and drain efficiency curve similar to the data presented on the datasheet with the 5dB offset on the gain from missing circuit losses.

The maximum available gain curve in Figure 3.4 shows ~22dB at 3.5GHz which matches the datasheet plots. The simulated K factor is 0.8 compared to the datasheet's 1.1 K factor which implies the amplifier is conditionally stable in simulation. Although the simulated data shows improved performance compared to the datasheet, the simulations did not model circuit losses shown on the measured datasheet plots. In design, care should be taken to model circuit losses to ensure simulation meets expected experimental results.

3.3 Transistor Biasing

As stated in previous sections, Class F amplifiers are biased in the "deep AB biasing" region near transistor pinchoff. Figure 3.5 shows an I-V characteristic curve simulated for the CHG40010F to determine a gate bias yielding a drain current slightly above cutoff.

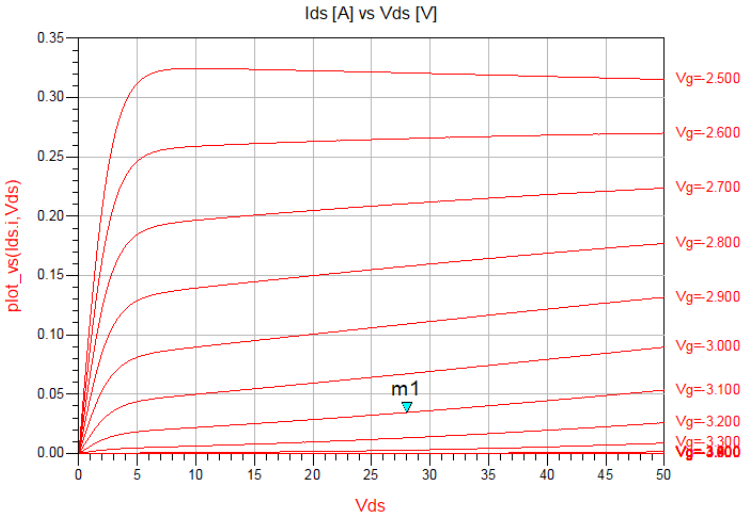


Figure 3.5: CGH40010F Simulated IV Characteristic Curves.

The datasheet specifies a gate threshold voltage of -3.0V typical and gate quiescent voltage of -2.7V for an I_{dq} of 200mA. The gate bias was initially set at -2.75V with a simulated Idq of ~200mA with a 28V drain bias. The gate voltage is further tuned in simulations and experimentation to determine optimal PAE and linearity.

3.4 Stability Analysis

The two-port active device must be unconditionally stable. In this case, the CGH40010F must undergo stability analysis as simulation results yielded a 0.8 K factor. Previous work with CGH40010F demonstrated low frequency due to transistor instability [10]. Typically, oscillations occur if input port signals reflect towards the source and the source reflects the incoming signal. In other words, oscillation occurs if the source reflection coefficient Γ_S and input reflection coefficient Γ_{IN} satisfy the following equation from [15]:

$$|\Gamma_S \Gamma_{IN}| > 1 \qquad (3.9)$$

Similarly, the load reflection coefficient Γ_L and output reflection coefficient will cause oscillation if the equation is satisfied:

$$|\Gamma_L \Gamma_{OUT}| > 1 \qquad (3.10)$$

Analysis from [15] concludes that for a passive source and load (where $|\Gamma_s| < 1$ and $|\Gamma_L| < 1$), the transistor will be unconditionally stable if:

$$|\Gamma_{IN}| < 1 \text{ and } |\Gamma_{OUT}| < 1 \qquad (3.11)$$

On a Smith chart, the unstable region is represented by a circular region representing impedances that cause instability. For unconditional stability, the stability circles should be relocated outside the unit circle using a stability network. Figure 3.6 shows a stability analysis simulation for the CGH40010F only:

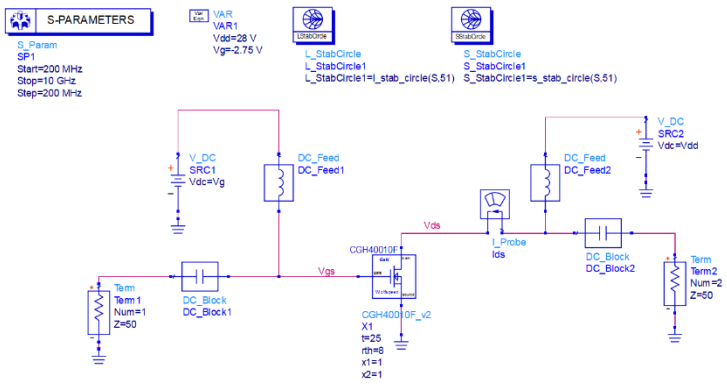


Figure 3.6: CGH40010F Amplifier Stability Analysis Simulation Schematic.

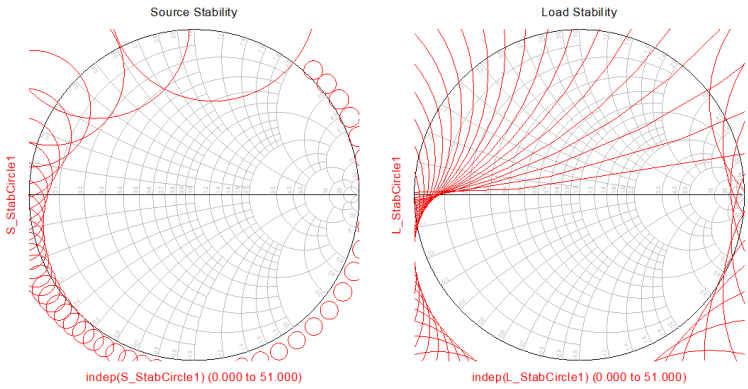


Figure 3.7: Source/Load Stability for CGH40010F with Significant Conditionally Stable Regions.

At frequencies below 2GHz, stability circles in Figure 3.7 show substantial unstable regions at multiple frequencies. Additionally, the low frequency instability regions can cause oscillations below 600MHz as observed by [10]. Transistors also have greater gain at lower frequencies which leads to greater instabilities. Figure 3.5 below shows the S_{21} plot with gain trending towards infinity below 1GHz – this behavior is not realistic.

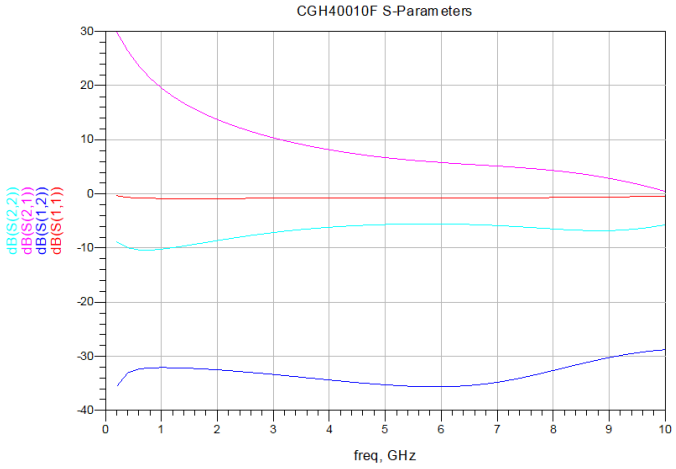


Figure 3.8: CGH40010F Amplifier S-Parameter Simulation.

A parallel 2.2pF capacitor and 47 Ohm resistor were added in series to the transistor gate, seen in Figure 3.9. Figure 3.10 shows the simulated source and load stability circles with the parallel RC circuit added.

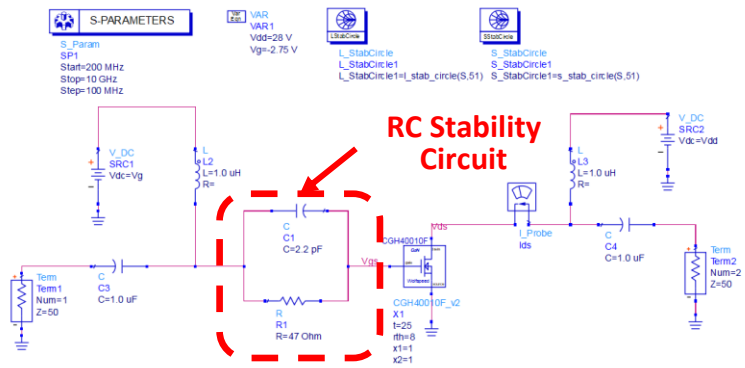


Figure 3.9: Stability Analysis Simulation with RC Stability Network.

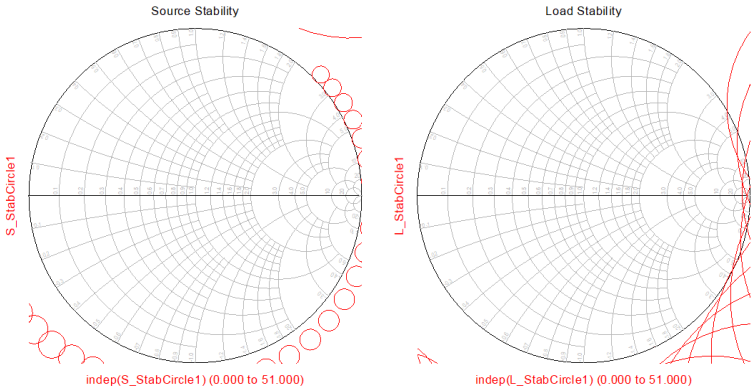


Figure 3.10: Smith Chart Source and Load Stability Analysis with RC Stability Network, Unconditionally Stable.

3.5 Source-Pull and Load-Pull Analysis

To determine the expected amplifier output power and efficiency, source-pull and load-pull analysis is necessary to optimize source and load impedances. Traditionally, source and load pull analysis is completed manually by varying device under test (DUT) impedance and measuring output power. Alternatively, source and load pull ADS simulations were completed [10].

ADS offers source and load pull analysis templates which includes harmonic analysis to create a 2nd harmonic short and a 3rd harmonic open necessary for Class F operation. Source and load pull simulations generate output power and PAE contours to optimize amplifier performance. Source and load pull templates include two-tone simulations to quantify IM3 performance, see Fig. 3.11:

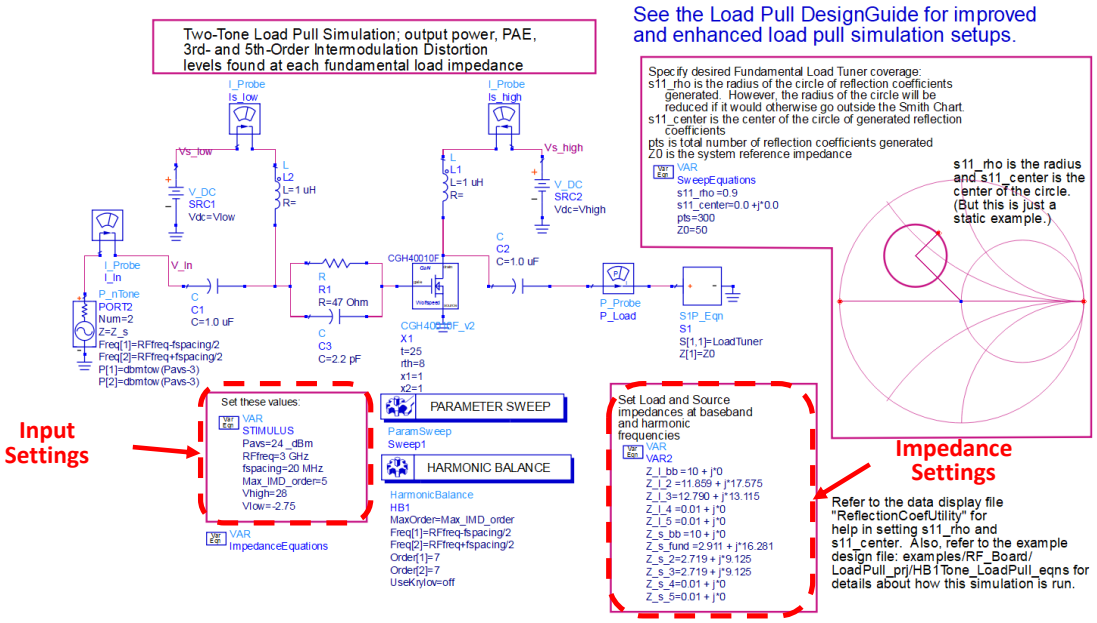


Figure 3.11: Example Two-Tone Load-Pull Simulation Schematic for CGH40010F.

The input settings are configured for a total input power of 24dBm with two tones set 20MHz apart at 3GHz center frequency. The amplifier is biased with Vd = 28V and Vg = -2.75V. The fundamental, 2nd harmonic, and 3rd harmonic impedances are adjusted following the procedures from [10]. The PAE and IM3 performance were monitored in the simulation results as seen in Figure 3.12:

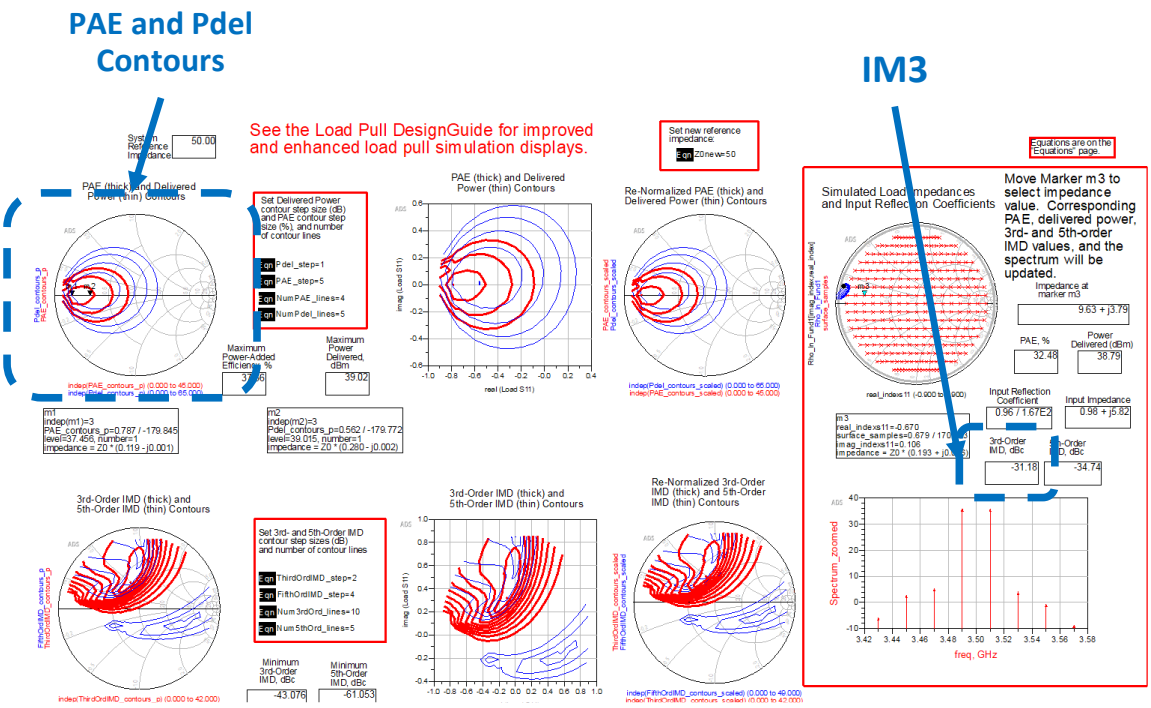


Figure 3.12: Example Two Tone Load-Pull Simulation Results for CGH40010F with Optimized Fundamental, 2nd Harmonic, and 3rd Harmonic Impedances.

At each step, the impedances were adjusted such that the 3rd-order IMD was at least -30dBc while maximizing PAE. Impedances were selected based on the PAE contour seen on the left of Figure 3.12 while IM3 is monitored graphically and numerical on the right-hand side of Figure 3.12. After selecting an optimal impedance at the given harmonic, the value is saved in the impedance settings section shown in Figure 3.11. If the next harmonic simulation resulted in IM3 less than -30dBc, the simulation was returned to the previous harmonic, and the impedance was adjusted to yield a higher IM3 at the cost of lower PAE. Table 3.2 shows the impedances derived from the source-/load-pull simulation results:

Table 3.2: Optimal Simulated Source and Load Impedances.

	Source Impedance [Ω]	**Load Impedance [Ω]**
Fundamental Frequency	2.9+j16.3	1+j5.8
2nd Harmonic	2.7+j9.1	11.9+j17.6
3rd Harmonic	2.7+j9.1	12.8+j13.1

When the impedances are set for each harmonic termination, the transistor achieved 38.8dBm output power at 37.6% PAE while maintaining -31dBc C/I ratio. The 2nd and 3rd harmonic impedances do not

follow the conventional short-circuited 2nd harmonic and open-circuited 3rd harmonic impedances due to the linearity optimization. In previous works traditional load-pull analysis did not optimize for linearity, therefore some deviation from ideal 2^{nd} and 3^{rd} harmonic terminations are expected [17]. The load-pull analysis for impedances shown in Table 3.2 balances linearity, efficiency, gain, and output power rather than maximizing PAE using traditional Class-F harmonic terminations.

3.6 Substrate Selection

With the transistor selected and the optimal impedances determined, a substrate must be selected to design the microstrips on. The PA substrate should have low dissipation factor and high thermal conductivity. Low dissipation factor minimizes losses to maximize power handling which is essential for high-power applications. High thermal conductivity enables rapid and efficient thermal dissipation. The first selected substrate is Rogers Corporation's RO4003C with a process dielectric constant of 3.38 (at 10GHz), a dissipation factor of 0.0027 (up to 10GHz), and thermal conductivity of 0.71 W/m·K [18]. An 8mil thickness was selected for the Class F PA due to low cost when fabricated alongside a large-scale production panel sponsored by Marki Microwave. Additionally, the thin substrate allows smaller feature size designs which in turn enables smaller form-factor amplifier assemblies.

The second substrate selected was a 31 mil RT5880 with a process dielectric constant of 2.20 (up to 10GHz), a dissipation factor of 0.0004, and a thermal conductivity of 0.2W/m·K [19]. A 31 mil substrate was selected for use on the DPA due to manufacturing issues encountered with the Class F PA on the thinner 8 mil RO4003C substrate. Thermal conductivity is not considered as the transistor dissipates heat through an external heat sink.

3.7 Output Matching Network Design

Figure 3.13 [6] defines a third-order harmonic trap network modeled with series and shunt lumped elements. The L_1 and C_1 output shunt tank circuit forms a short-circuit for the $2f_o$ harmonic. The L_3/C_3 creates an open circuit for $3f_o$.

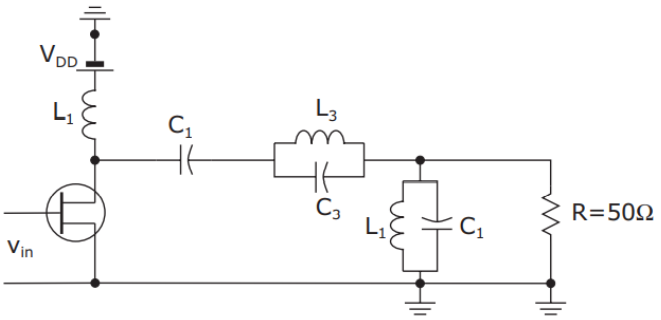


Figure 3.13: Simplified Class F Output Harmonic Regulation Circuit [6].

Alternatively, the L3/C3 tank circuit can be replaced with a quarter-wave transmission line that transforms the L0/C0 tank circuit into a short-circuit for even harmonics and open-circuit for odd harmonics at the transistor's drain, seen in Figure 3.14.

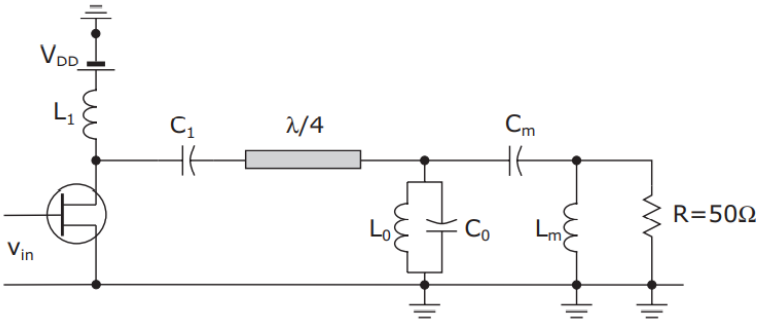


Figure 3.14: Example Distributed and Lumped Class F Output Harmonic Regulation Circuit [6].

PAE is increased by input and output L-section harmonic control networks (Figure 3.15) to compensate for packaging parasitics [20, 21]. These studies have shown up to 10% PAE improvement due to the parasitic compensating improving the impedance match up to the transistor's impedance plane. However, the transistor model provided by Wolfspeed models the packaging parasitics. Therefore, a parasitic compensation network was not required in this design as the impedance from load-pull analysis was optimized up to the package's impedance plane.

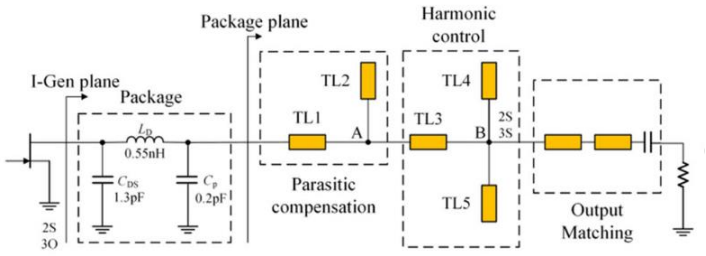


Figure 3.15: Example Parasitic Compensation and Harmonic Control Circuit [20].

Radial stubs instead of open-circuit stubs increase harmonic control circuit bandwidth and harmonic frequency trapped power, which increases PAE [10, 22]. Radial stubs are not used for harmonic regulation (space constraints) but are implemented in the bias network to improve RF choke performance. The 8 mil RO4003 substrate required features that were not within standard PCB fabricator capabilities. Alternatively, radial stubs are placed in the bias network to expand the harmonic trapping capability as seen Figure 3.16:

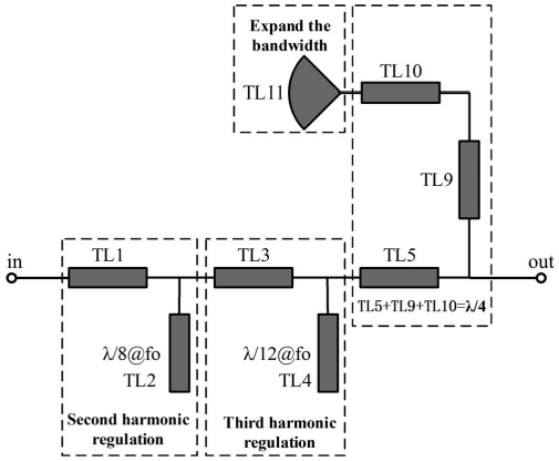


Figure 3.16: Improved Harmonic Regulation Circuit to Increase Trapping Bandwidth [22].

Fig. 3.13 defines a 2.6GHz output harmonic regulation circuit [22] that demonstrates over 30dBc IM3 suppression with 50% PAE. TL1 and TL2 provide a second harmonic short at the network input. TL1, TL3, and TL4 provide the third harmonic open at the network input. This satisfies Class F operation requirements. The radial stub at the end of the quarter-wave line expands the trapping bandwidth and effectively controls higher order harmonics to further improve PAE [22]. The impedances derived from load-pull were initially used to generate the harmonic matching network shown in Figure 3.13. Further

tuning via simulation adjusted the impedances to optimize for linearity and PAE. The implemented harmonic regulation network is provided below in Figure 3.17:

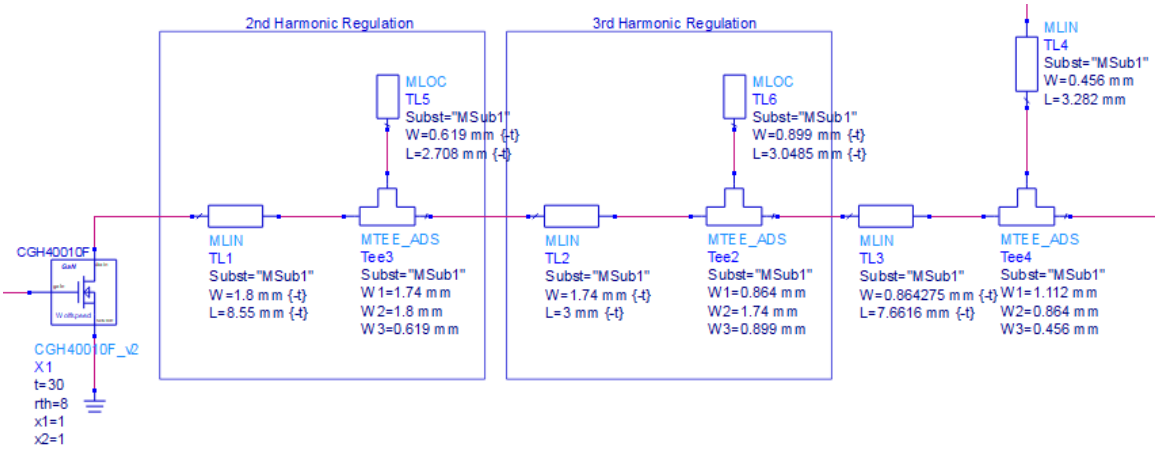


Figure 3.17: Implemented Class F Harmonic Regulation Circuit Schematic.

PCB microstrip width at the transistor ports matches the 1.4mm lead width to enable soldering. At 2.5GHz, the transistor output presents a relatively low output impedance (19+j9.2Ω) [14], which transformed to meet the 50Ω input/output match as specified in the design rules. A three-step Klopfenstein taper that transforms the harmonic regulation circuit output impedance to 50Ω at the network output. An additional 10mm 50Ω line provides a PCB launch for the Southwest Microwave edge launch connector. The impedance matching network is provided below in Figure 3.18:

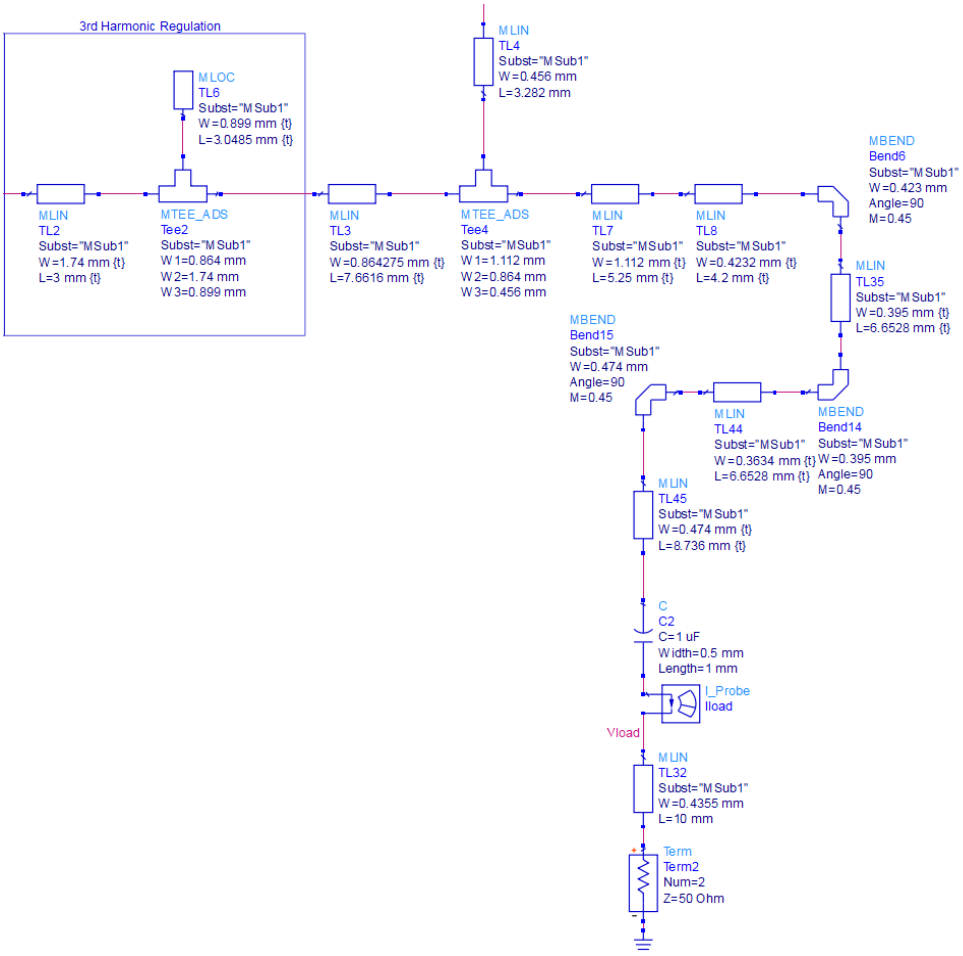


Figure 3.18: Implemented Class F Output Impedance Matching Network.

3.8 Input Matching Network Design

Following source-/load-pull procedures from [10], the optimal source impedance was determined to be 2.9+j16.3Ω. Similar to the output matching network, a Klopfenstein taper transforms the transistor's input impedance up to a 50Ω match. The RC circuit determined from stability analysis is included to prevent low-frequency oscillation – the resistor and capacitor values were adjusted in simulation to optimize input impedance and stability. The implemented input matching is provided below in Figure 3.19:

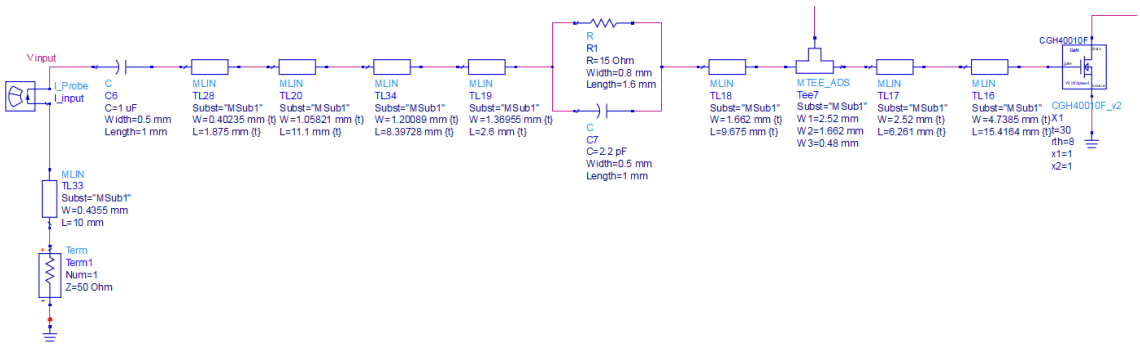


Figure 3.19: Implemented Class F Input Impedance Matching Network.

3.9 Drain and Gate Biasing Networks

According to IMS HEPA-SDC rules, participants are limited to a maximum of two supply voltages. Additionally, the DC connections must use banana plug interfaces [3]. For Class F biasing, the two supply voltages bias the transistor drain and gate. The drain voltage was set at V_{ds} = 28V per datasheet specifications while the gate voltage was set for a quiescent current of ~200mA (V_{gs} = -2.75V). The gate voltage is further tuned experimentally to optimize for linearity and PAE – contestants are permitted 10 minutes to adjust biasing during the competition.

The drain biasing network uses a quarter-wave line terminated with an open stub to act as a transmission zero at the fundamental frequency – this effectively shorts to ground any fundamental leakage. The stub is placed a quarter-wave away from the RF path to prevent loading and a radial stub increases the stop bandwidth [23]. Additional bypass capacitors are placed along the bias line to remove power supply noise and prevent loss from the RF path – these act as high-frequency shorts to ground.

Due to the limited PCB size, bends are incorporated into the bias lines to fit the banana plug connector, bypass capacitors, and quarter-wave lines. Figures 3.20 and 3.21 show the implemented drain and gate bias circuits for the Class F amplifier.

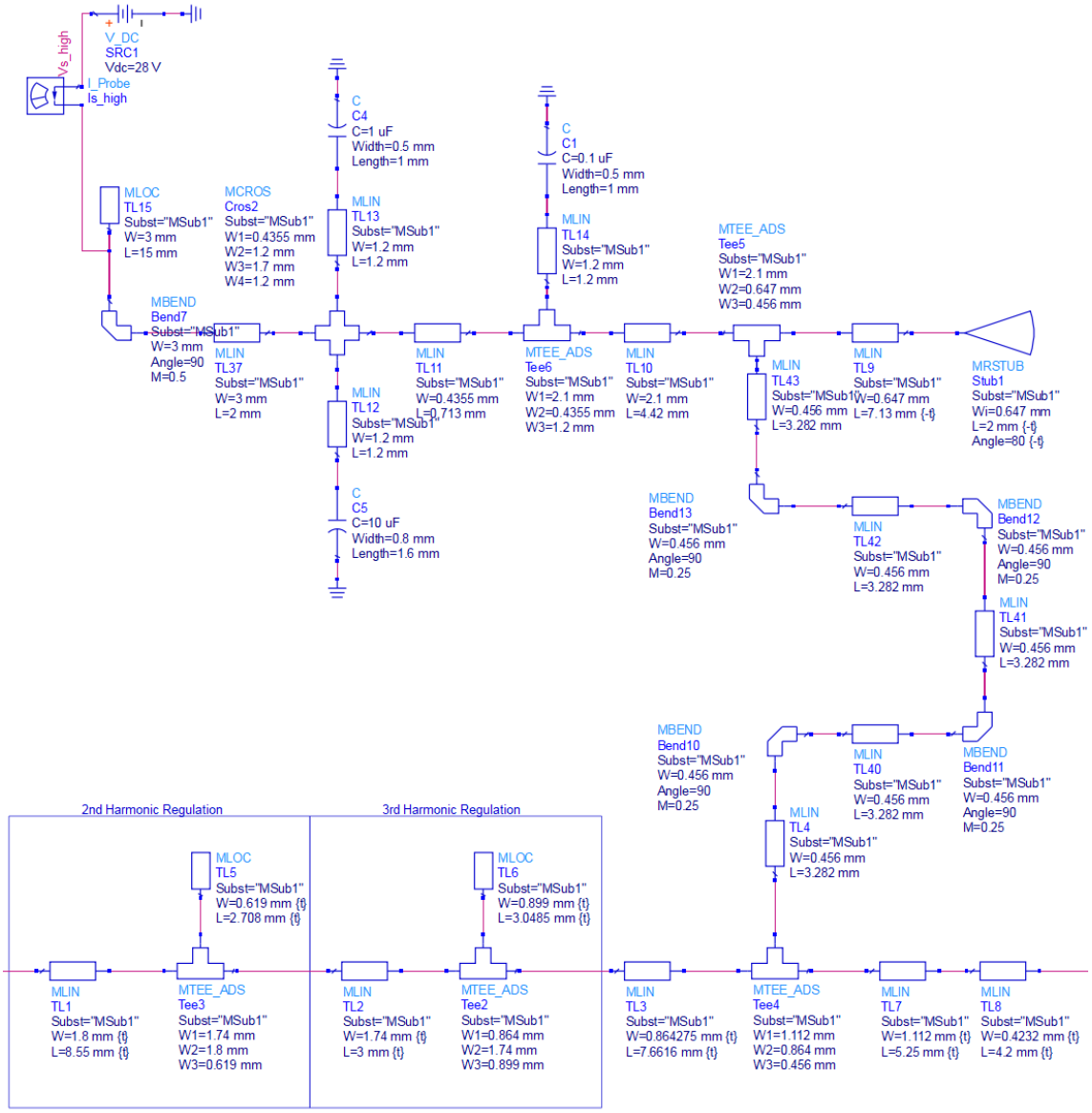


Figure 3.20: Implemented Class F Drain Bias Circuit.

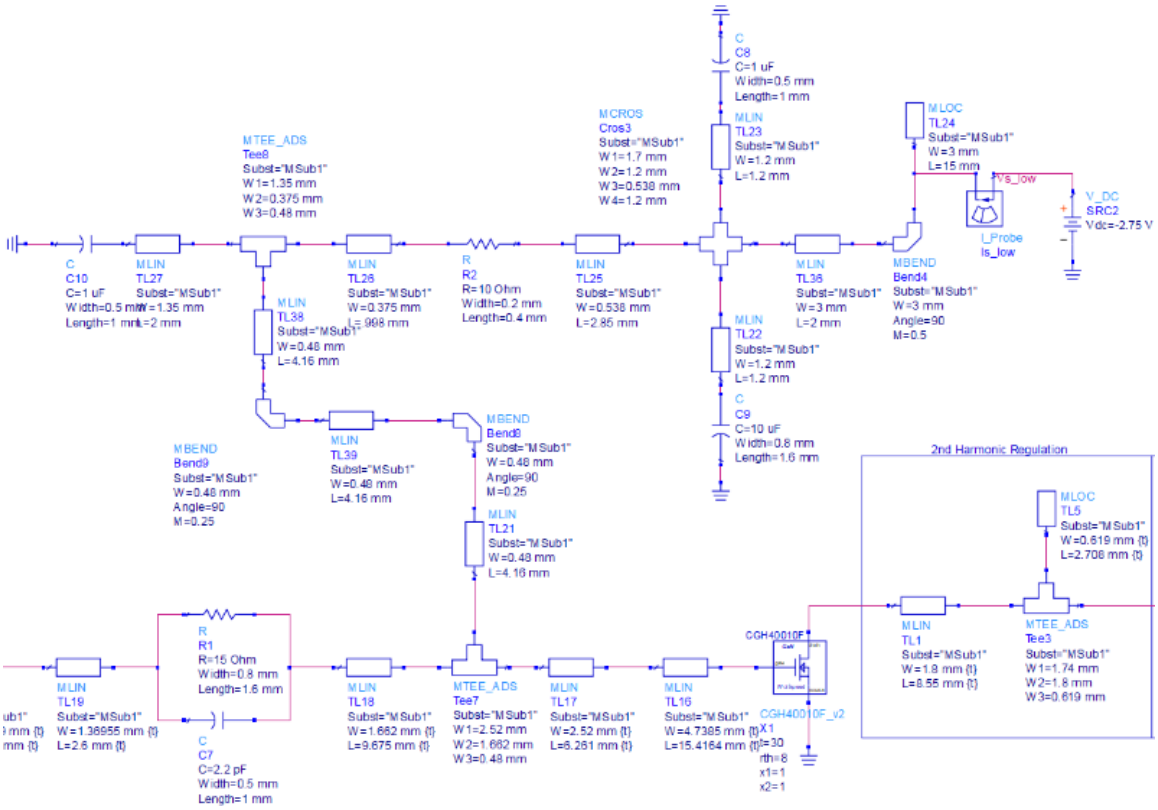


Figure 3.21: Implemented Class F Gate Bias Circuit.

3.10 Class F Amplifier Schematic Design

A complete schematic of the designed Class F amplifier is provided below (Figure 3.22):

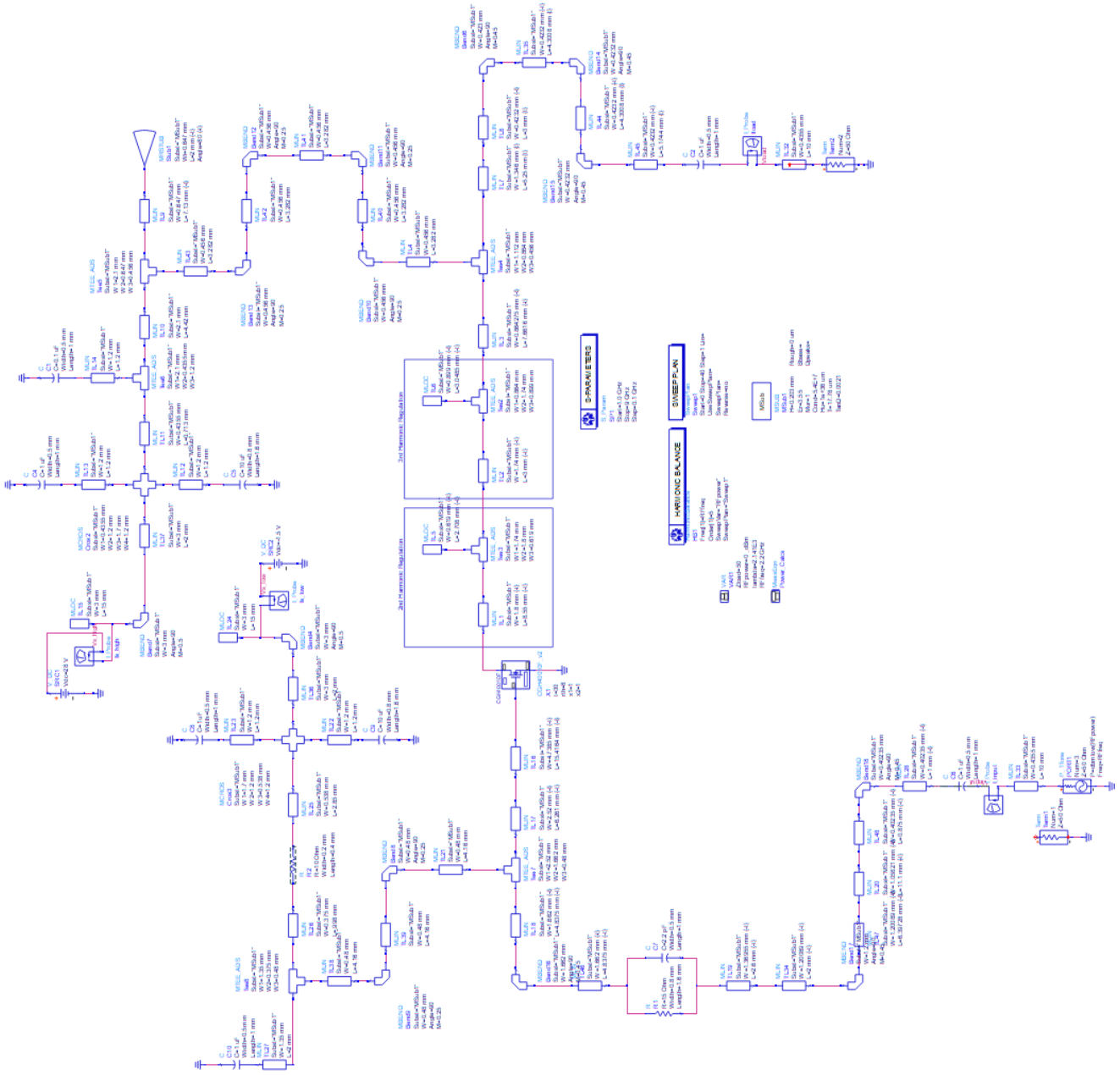


Figure 3.22: Class F Amplifier Design Schematic.

4. DOHERTY AMPLIFIER DESIGN

To maximize linearity in a Class F amplifier, the output power must be reduced to avoid gain compression. Simulation results (Figure 5.4) from the Class F amplifier show <40% PAE while maintaining 30dB C/I ratio in the backed off region. An alternative approach is to design the amplifier for maximum linearity, then improve efficiency. This section details the operation and design of a Class F-based Doherty amplifier.

4.1 Doherty Amplifier Topology

The DPA is divided into 3 main sections: input power dividing, amplifier stage, and output power combining. Figure 4.1 defines the DPA block diagram:

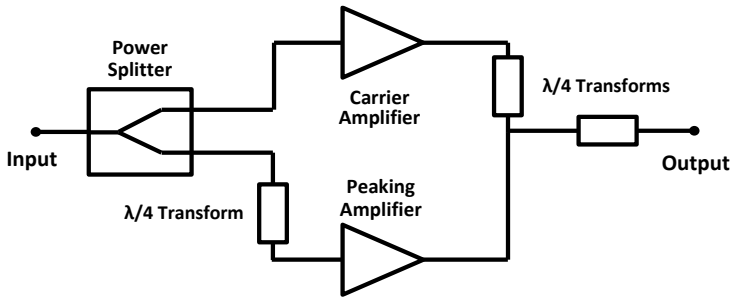


Figure 4.1: Simplified DPA Schematic.

The amplifier stage (Figure 4.1) requires two amplifiers which are typically in two different bias conditions; the carrier and peaking amplifiers are biased as Class AB and Class C amplifiers, respectively [17]. The carrier amplifier provides consistent average output power while the peaking amplifier operates only at peak input power levels. Carrier and peaking amplifier topologies can vary; however, some configurations use identical topologies with different bias conditions [17]. Individual branch efficiency can be improved through harmonic control as shown in Class F amplifier design, Chapter 3. When output matching networks are Class F-1 for both the carrier and peaking amplifiers, DPA drain efficiency is 82.2% with a 42.4dBm P_{sat} at 2.4GHz center frequency [24]. Implementing Class F for the peaking amplifier, experimental drain efficiency is 86.7% when excited by a single-tone carrier, reaching a 44dBm P_{sat} at 2.4GHz center frequency [24].

The input power dividing splits the incoming RF power between the carrier and peaking amplifiers typically through a power divider or quadrature splitter. In low-frequency narrow-band applications, the

input split utilizes a Wilkinson power divider, [24, 25], to evenly split power while isolating the two amplifiers. However, the DPA's operating bandwidth is limited by the narrow operating range of common power splitters. Alternatively, using a quadrature hybrid presents wider bandwidth and solves the phase mismatch at the output by introducing the 90° at the peaking amplifier input. This eliminates the additional quarter-wave transform to impose a phase shift on the input of the peaking amplifier. All output reflections are absorbed by the 50Ω terminated isolated port. Figure 4.2 defines the Wilkinson divider and quadrature hybrid:

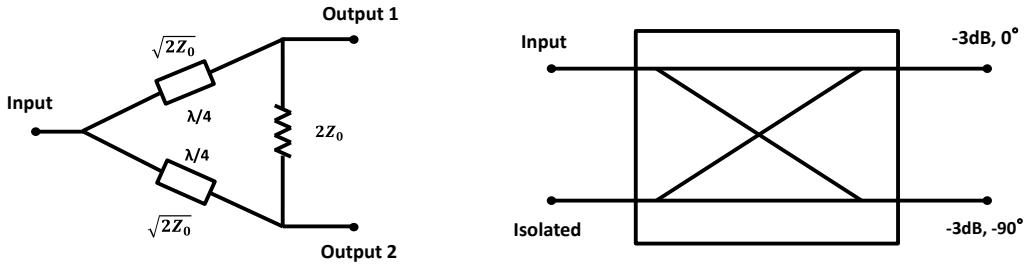


Figure 4.2: Wilkinson Power Divider and Quadrature Hybrid Schematics.

At the output power combining stage, a quarter-wave impedance transformer is required on the carrier amplifier output - the 90° phase shift caused by this impedance transform is matched by a phase delay line at the peaking amplifier input [7]. Due to the parallel output combining, $Z_0/2$ is seen at the output thus requiring an impedance transformer from the combining node to the output. The traditional DPA output power combining topology provides poor isolation between the carrier and peaking amplifier - load modulation occurs when either amplifier is in operation therefore further consideration is required to improve impedance matching during amplifier operation [7]. Typically, the output of the peaking amplifier should present an open load when not in operation to maximize power throughput from the carrier amplifier on the output line [26]. Further improvements to the Doherty combiner are presented in Section 4.4.

4.2 Doherty Amplifier Operation

Figure 4.3 shows how power is amplified through the DPA: the carrier amplifier output provides the majority of the gain for a high average power while the peaking amplifier conducts only at high input powers to provide a high peaking power. When summed, the two amplifier outputs combine to form a linearly gained output waveform. Typically, the carrier amplifier is optimized for efficiency with lower input power levels, however this operates at the cost of potential compression due to the bias limitation when subject to a high (peaking) input power. The low conduction angle of the peaking amplifier provides gain for high power levels; the resulting output allows the DPA to accommodate signals with high peak-to-average power ratio (PAPR).

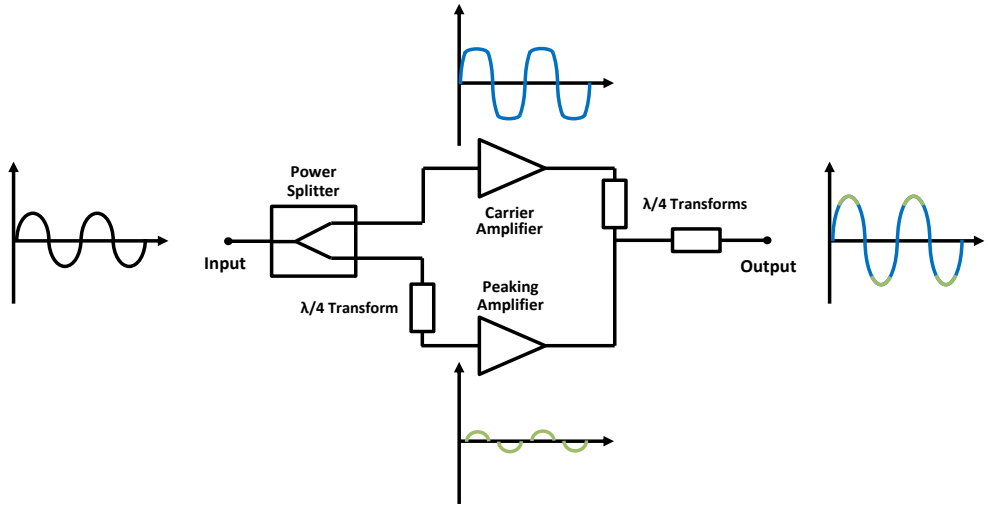


Figure 4.3: DPA Carrier and Peaking Amplifier Waveform Combined as Total Output Waveform.

Based on equation 2.2, maximizing output power at a given input power increases the power added (or gain) of the amplifier therefore maximizing drain efficiency and PAE. However, compared to a conventional PA (such as Class B or Class F), the DPA's efficiency in output power back-off (OPBO) from output power saturation is significantly improved due to its Class AB bias and keeping the peaking amplifier normally off - this allows the amplifier to be driven below compression and avoid harmonic generation. Figure 4.4 (below) compares the DPA's efficiency to a Class B amplifier – t high DPA efficiency is achieved while in OPBO and maintained when input power increases:

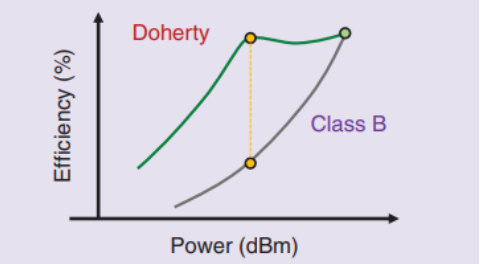


Figure 4.4: Ideal DPA Efficiency vs Output Power Showing Improved Efficiency at OPBO (yellow) [27].

4.3 Improved Doherty Amplifier

Previous work done by [24] demonstrated that DPA configured with a Class F^{-1} carrier amplifier and a Class-F peaking amplifier 4% efficiency improvement and 2dB average output power improvement. The design obtained a peak power of 44dBm with a drain efficiency of 86.7%. Additionally, the measured adjacent channel leakage ratio (ACLR) was -30dBc using a 10MHz local thermal equilibrium (LTE) signal with 6.6dB PAPR [24]. Furthermore, Class F^{-1} minimizes power dissipation since the square-wave current waveform has lower magnitude than a half-sinusoidal waveform [24]. Class F-1 amplifiers can obtain 10% higher PAE compared to Class F amplifiers when biased and operated at identical output powers [12]. An improved DPA using a Class F-1 carrier amplifier and Class F peaking amplifier is shown in Figure 4.5:

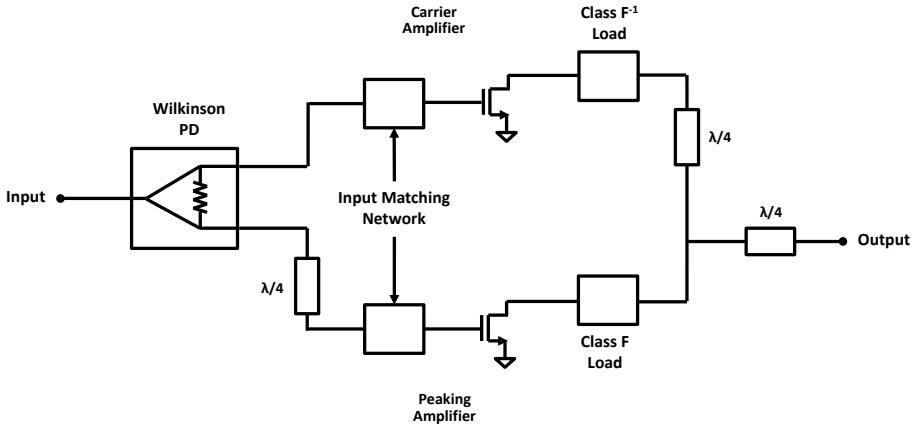


Figure 4.5: Implemented Class F^{-1}/F DPA Block Diagram.

Initially, the Class F output network designed in Chapter 3 was inverted to create the Class F^{-1} output network. Additionally, a Wilkinson power divider was created for input power splitting while a

conventional Doherty combiner was used. Based on preliminary 2-tone simulation results, the implemented design shown in Figure 4.5 did not meet the two-tone linearity requirement outlined in [24], therefore further optimization was required to meet the 30dBc C/I ratio requirement. A linearity-enhanced DPA used a quadrature hybrid as the Doherty combiner [8] to meet the 30dB C/I ratio requirement. Figure 4.6 shows the improved DPA combiner compared to the classical combiner:

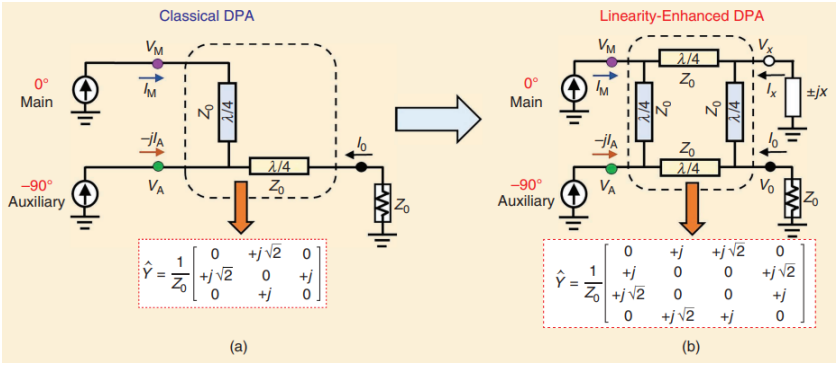


Figure 4.6: Conventional (a) vs Quadrature Hybrid (b) Doherty Combiner [8].

The isolation port was terminated to ground to emulate a classic DPA output combiner; adding a capacitor to ground allows output load modulation to optimize efficiency [8]. This capacitor value is tuned in simulation to increase linearity. The quadrature hybrid DPA combiner was implemented on the Class-F^{-1}/Class-F DPA as shown below in Figure 4.7:

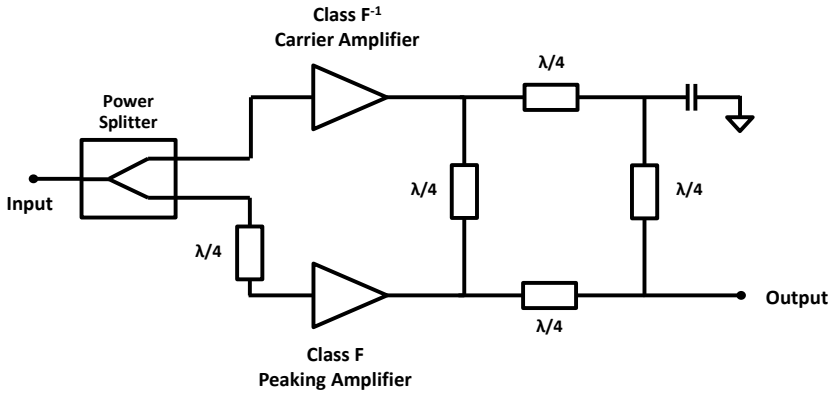


Figure 4.7: Improved Class F^{-1}/F DPA Block Diagram.

Simulations show the Class-F^{-1}/Class-F DPA performs with least -30dBc IM3 with at least 50% PAE compared to the sub-30% PAE seen on the Class F amplifier. The complete linearity-enhanced DPA schematic is presented below in Figure 4.8:

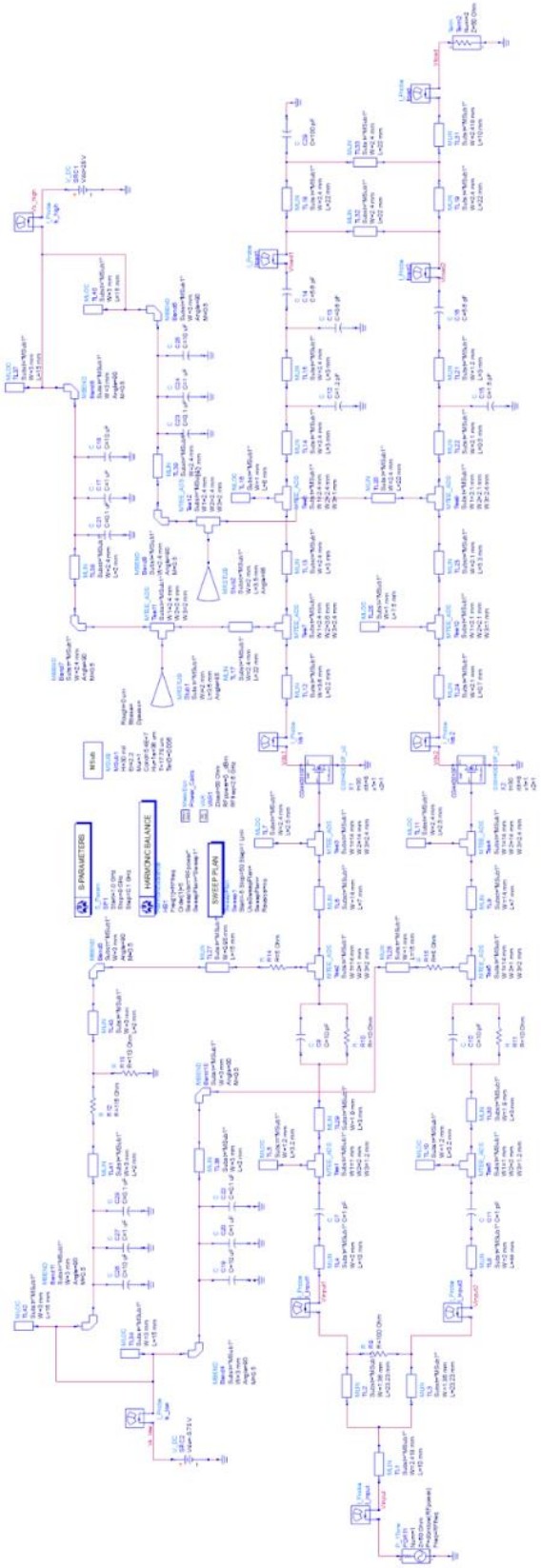


Figure 4.8: Implemented Doherty Amplifier Schematic.

5. SIMULATION RESULTS

This section presents the simulation results and analysis for the designed Class F PA and DPA. Finalized simulations are presented after optimizing the circuits with the tune function in ADS.

5.1 Class F Amplifier Simulations

The Class F PA is first presented – simulation results show optimal performance about 2GHz which deviates from the originally planned 3GHz. Simulated s-parameters confirm where maximum gain and minimum return loss is. The device is characterized with Vd = 28V, Vg = -2.75V, and -15dBm input power in Figure 5.1:

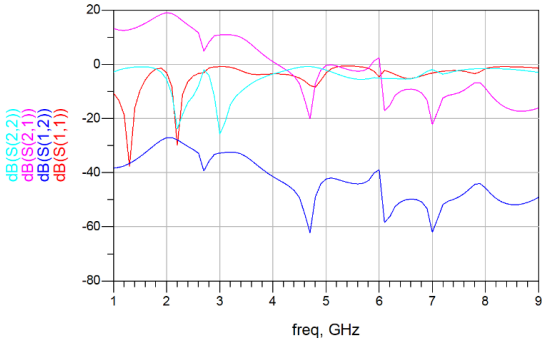


Figure 5.1: Simulated Class F PA S-Parameters, V_d = 28V, V_g = -2.75V, -15dBm Input Power.

The Class F PA achieves a maximum gain of 19dB at 2.0GHz and a minimum input return loss of 30dB at 2.2GHz. The PA shows at least 30dB reverse isolation across 1.5 to 2.4GHz band. Although the design was specified for 2.5GHz, 2.2GHz was chosen as the center frequency to maximize gain. Figure 5.2 shows the simulated single-tone power sweep for gain, output power, and PAE:

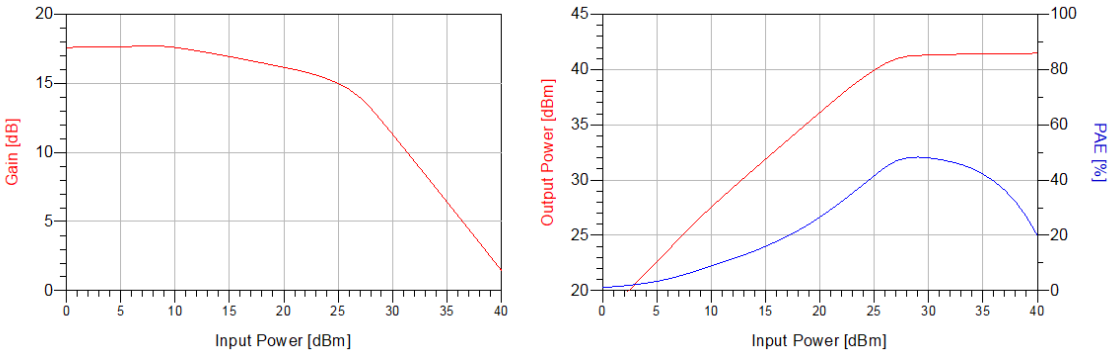


Figure 5.2: Simulated Class F PA Single-Tone Gain, P_{out}, and PAE at 2.2GHz, V_d = 28V, V_g = -2.75V.

With a single carrier input, the Class F PA outputs 39dBm with a 24dBm input tone at 2.2GHz. This corresponds to a simulated PAE of 35%. A 5-10% decrease in measured PAE is expected due to system loss. With a 41dBm output (saturation), the peak PAE is 42% at 42dBm output power in simulation. However, this requires a 28dBm input which is beyond the competition rule limits (24dBm total input). In addition, the amplifier will have less than 30dB C/I in the saturated region. The gain versus input power curve (Figure 6.2) shows gain roll off starting at 10dBm input and reaches P1dB at 17dBm input. This is attributed to soft compression seen in GaN which is typical in continuous wave operation [28]. The drain voltage and current, seen in Figure 5.3, are probed from the transistor's drain pin on the ADS schematic:

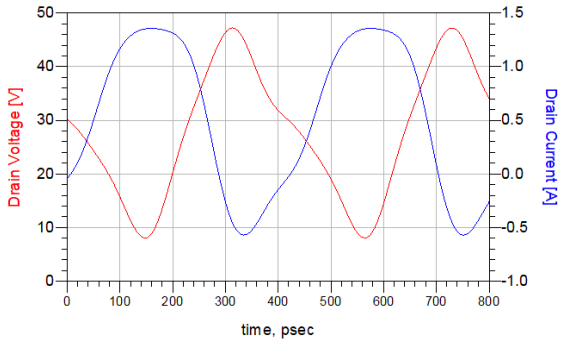


Figure 5.3: Class F Simulated Drain Voltage and Current Waveforms, V_d = 28V, V_g = -2.75V.

The drain voltage and current are simulated and show minimal cross over between waveforms, indicating very little power dissipated by the transistor. The current is in the desired half-sinusoidal waveform while the voltage is not quite the ideal square wave.

The Class F PA two-tone simulation results are shown below in Figure 5.4:

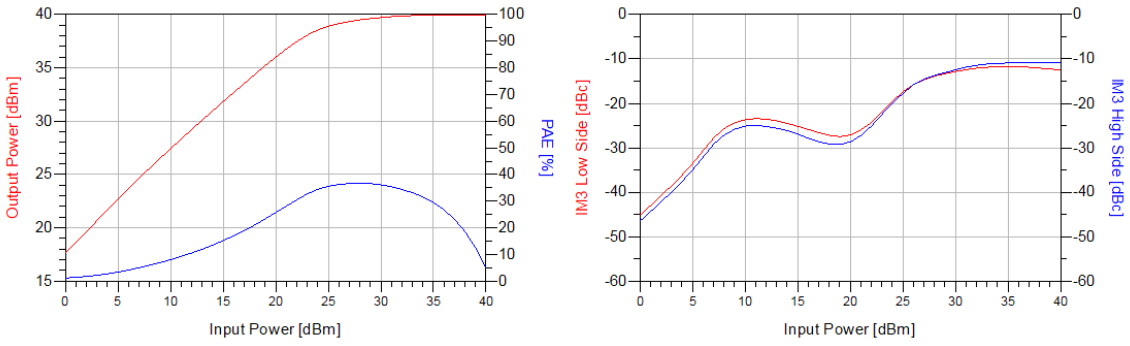


Figure 5.4: Simulated Class F PA Two-Tone P_{out}, PAE, and IM3 at 2.2GHz V_d = 28V, V_g = -2.75V.

When subject to a two-tone input with 20MHz spacing centered around 2.2GHz, the PAE drops to less than 40% when the PA is saturated at 27dBm total input power. At 24dBm total input, the PA achieves 34.5% PAE with a 20dBc C/I ratio. When sweeping the total input power from 0dBm to 24dBm, the 30dBc C/I ratio is reached at 7dBm, corresponding to an 8% PAE. Although this is poor performance, it is expected for a Class F amplifier due to its high harmonic generation.

Due to the poor performance at 2.2GHz, the operating frequency is increased up to 2.4GHz where the PA has slightly less gain resulting in lower IM3. The large-signal performance plots are shown below for single-tone (Figure 5.5) and two-tone tests (Figure 5.6).

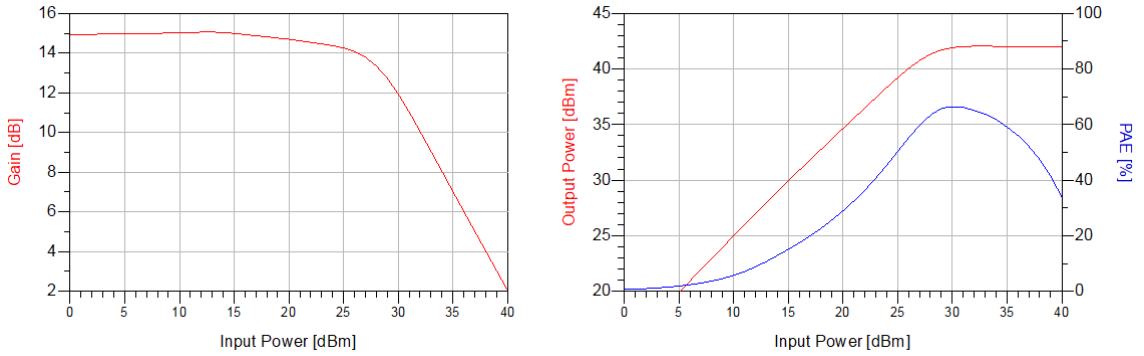


Figure 5.5: Simulated Class F PA Single-Tone Gain, P_{out}, and PAE at 2.4GHz, V_d = 28V, V_g = -2.75V.

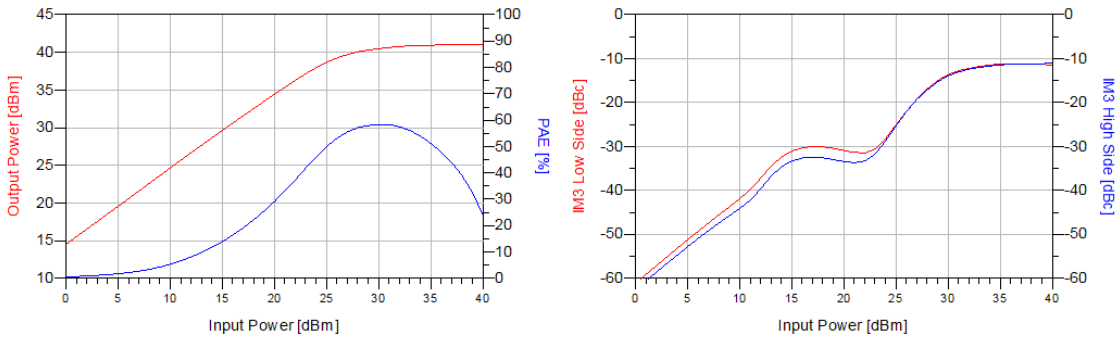


Figure 5.6: Simulated Class F PA Two-Tone P_{out}, PAE, and IM3 at 2.4GHz V_d = 28V, V_g = -2.75V.

At a 2.4GHz center frequency, the single-tone test yields an output power of 38dBm with 24dBm input corresponding to a 14dB gain. The PA achieves 46% PAE at 24dBm input and peaks at 66.5% PAE with 30dBm input. When the total input power is swept from 0dBc to 24dBc, the PA maintains over 30dB C/I ratio up to 23dBm input power. The PA has a 31dBc C/I ratio with 22dBm total input power which corresponds to a 37% PAE – this is slightly improved from operating at 2.2GHz.

5.2 Doherty Amplifier Simulations

To improve linearity and PAE at OPBO, a DPA was designed with a Class F^{-1} carrier amplifier and a Class F peaking amplifier. Additionally, a quadrature hybrid output with a capacitive terminated isolated port was used to tune the amplifier's load and adjust for improved linearity. The DPA's drain is biased at 28V. The carrier amplifier is biased at -2.75V near the transistor pinch-off point while the peaking amplifier is biased at -5.75V well into the Class C bias point.

The simulated s-parameters for the Class F^{-1}/F DPA are presented below in Figure 5.7:

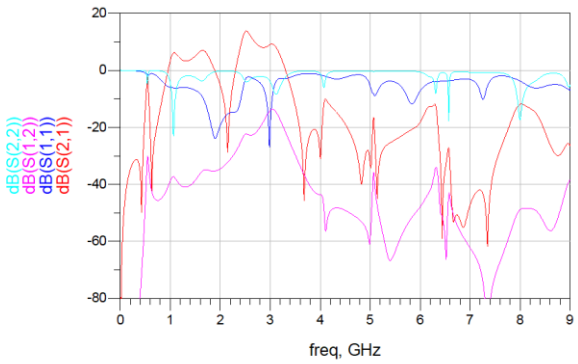


Figure 5.7: Simulated Class F^{-1}/F DPA S-Parameters, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

The simulated s-parameters in Figure 6.7 show maximum 16dB gain at 2.6GHz, however the gain at 20MHz spacing about 2.6GHz falls to 15dB on each side. The input return loss shows ~10dB return loss and over 20dB reverse isolation at 2.6GHz.

The single-tone simulations for the Class F^{-1}/F DPA are presented below in Figure 5.8 with a continuous wave (CW) input power sweep from 0 to 40dBm at 2.6GHz:

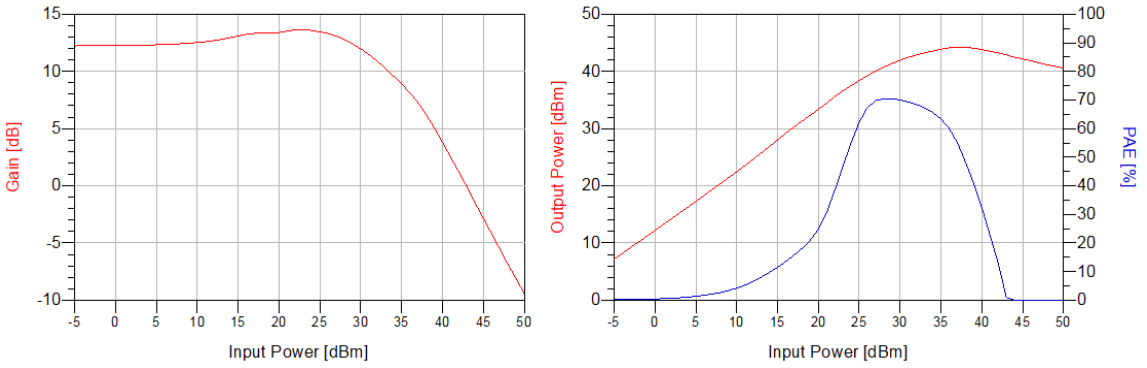


Figure 5.8: Simulated Class F^{-1}/F DPA Single-Tone Gain, P_{out}, PAE, and DE at 2.6GHz, V_d = 28V, $V_{g,carrier}$ = - 2.75V, $V_{g,peaking}$ = -5.75V.

The Class F^{-1}/F DPA has a peak output power at 44dBm with a 37dBm input. The peak PAE is 70.5% with 28dBm input power and 41dBm output power. With a single 24dBm input tone, the output power is 37dBm and the PAE is 55%. Compared to the Class F amplifier, the peak PAE on the DPA occurs well below saturation at ~6dB OPBO. When driven into saturation, the DPA outputs 43dBm maximum output power when subject to a 37dBm input.

Similar to the Class F amplifier, two-tone simulations are run with equal amplitude tones at 20MHz spacing. Two-tone simulations are presented in Figure 5.9 for the DPA at 2.6GHz center frequency:

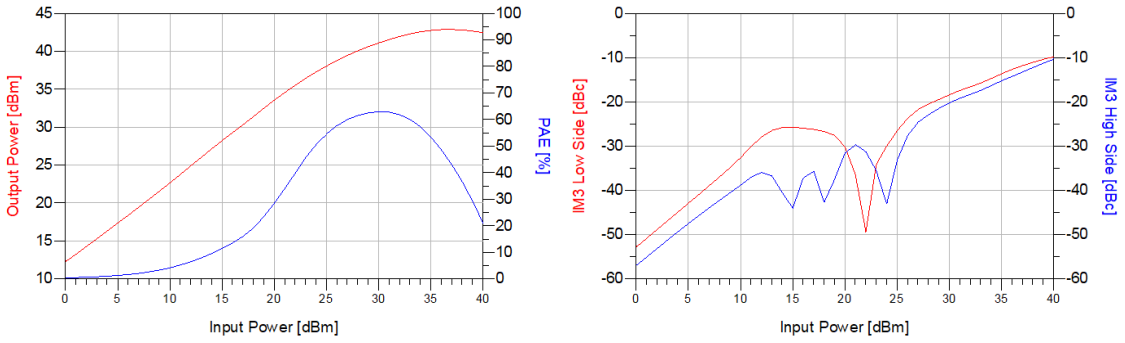


Figure 5.9: Simulated Class F^{-1}/F DPA Two-Tone P_{out}, PAE, and IM3 at 2.6GHz, V_d = 28V, $V_{g,carrier}$ = - 2.75V, $V_{g,peaking}$ = -5.75V.

Based on the simulated two-tone tests, the DPA sees slightly lower PAE vs input power sweep compared to a single CW input tone. At 24dBm total input power, the DPA outputs 37dBm with 51% PAE, a 4% decrease from the single-tone test. The high-side and low-side IM3 are below -30dBc at 24dBm input power, however the low-side IM3 peaks above -30dBc when the input power sweeps from 11 to 20dBm. Further tuning in center frequency, gate voltages, and output coupler isolation port termination is completed in experiment further reduce low-side IM3.

6. AMPLIFIER FABRICATION

6.1 Class F Assembly

The fabricated PCB is 2 x 3" with an 8 mil substrate thickness. The thin substrate results in smaller design features allowing the compact form-factor. The design is restricted to this material thickness since the sponsor uses this material frequently allowing low-cost circuit board production. However, a thinner substrate does not provide enough rigidity and will bend due to the connector weight. A brass plate was manufactured and epoxied to the backside of the PCB to provide mechanical rigidity, circuit grounding, and thermal relief for the active components. The brass plate is 2mm thick and provides excellent thermal and electrical conductivity to act as a common ground and heat sink for the transistor.

The CGH40010F package is a screw-down flange mount device where the leads on the package are soldered down to the PCB and the flanges are screwed into a heat sink. Originally, the brass plate was designed with screw holes, however, miscommunication with the vendor resulted in missing drill holes. Instead, the transistor flanges are soldered onto the brass plate and the drain and gate leads are bent slightly down to solder onto the PCB traces.

The following Figure 6.1 shows the outline drawing and fabrication file used to manufacture the PCB:

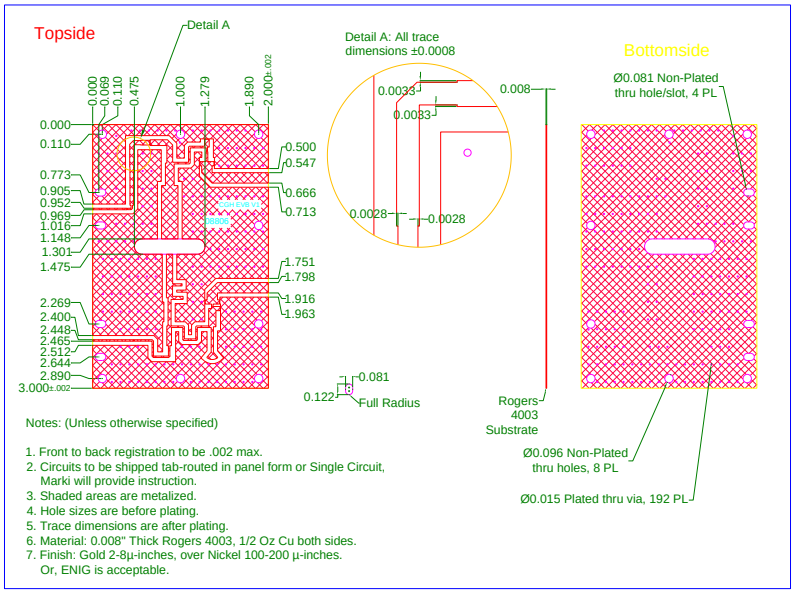


Figure 6.1: Class F Amplifier Outline Drawing.

The drawing is converted to a Gerber file and sent to a PCB fabricator for manufacturing. A separate brass plate was machined by an external vendor. Figures 6.2 and 6.3 show the Class F amplifier unit 1 assembly, top-down and side views.

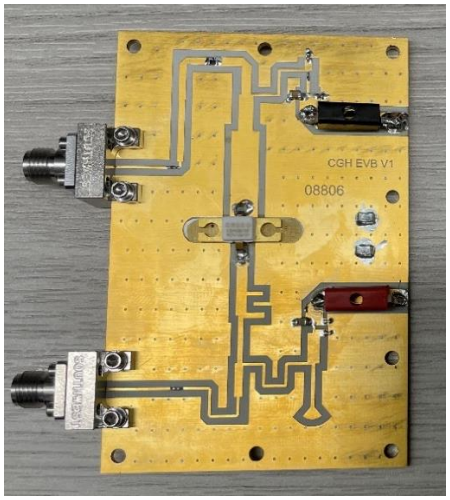


Figure 6.2: Photograph of Class F Amplifier Assembly, Top-Down.

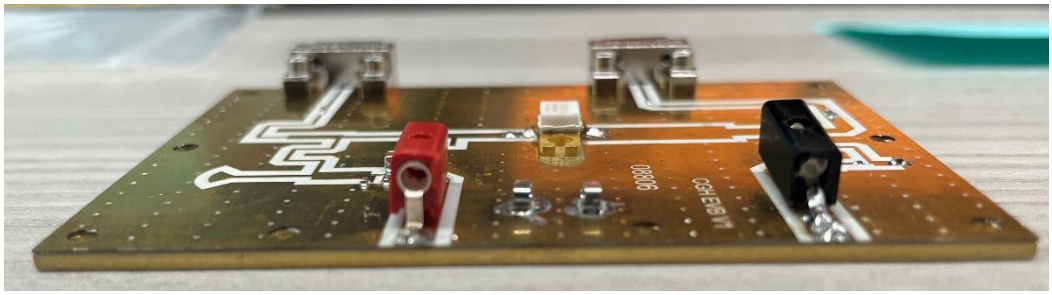


Figure 6.3: Photograph of Class F Amplifier Assembly, Side-Profile – Unit 1.

In addition, a second unit was fabricated to improve PCB trace to transistor drain and gate transition. The updated Class F amplifier has decreased lead length and solder to minimize parasitic inductances and capacitances to improve input and output matching. Figure 6.4 shows Class F – Unit 2 assembled:

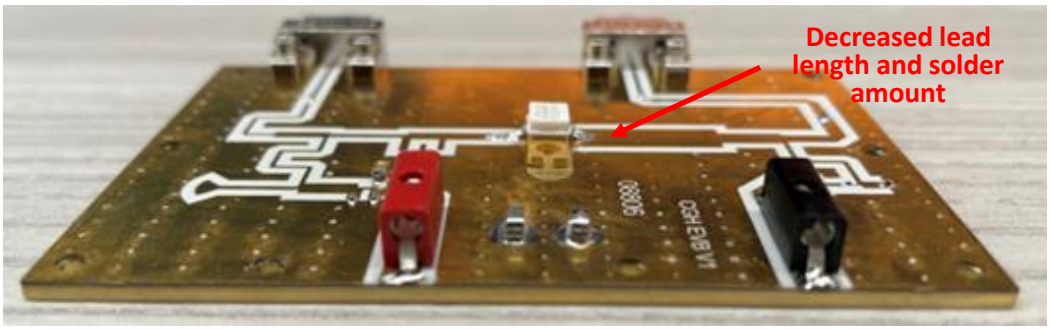


Figure 6.4: Photograph of Class F Amplifier Assembly, Side-Profile - Unit 2.

6.2 DPA Assembly

For the DPA design, a 31 mil thick RT5880 from Rogers Corp was selected over the 8 mil thick RO4003C due to the manufacturing complexities with a thinner substrate. Although the substrate thickness was increased, the DPA transistors were not fully recessed within their cavities similar to the Class F design. The leads are bent down to be soldered on the top layer traces, and due to this non-planar transition, there is increased inductance from the leads acting as wirebonds. The ADS schematic was converted to a layout, exported to a .dxf, and optimized in AutoCAD. The final DPA assembly drawing is provided below, Figure 6.5:

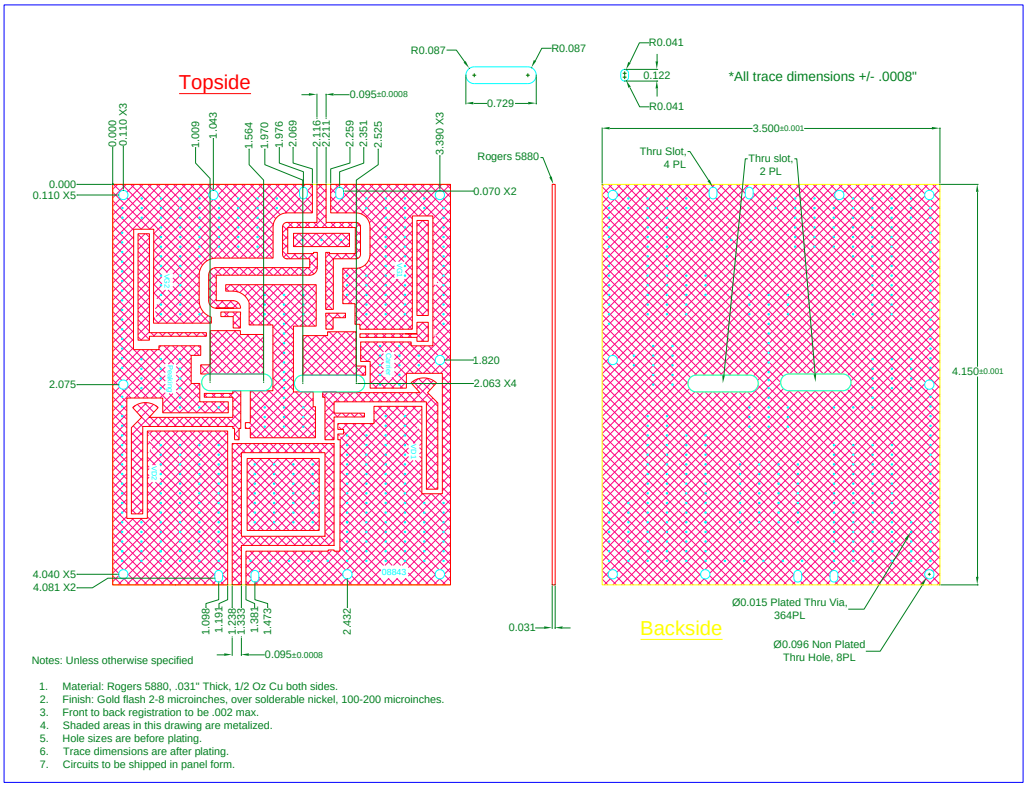


Figure 6.5: Doherty Amplifier Assembly Drawing.

The PCB is screwed on an additional 20 mil thick RT5880 sheet to provide thermal relief and common grounding. This is selected over the brass plate since the PCB is a non-standard size for the sponsor, therefore brass plates were not readily available. The transistors source pads are soldered onto the second RT5880 layer while the gate and drain leads are soldered flush with the top layer traces. The two substrates are screwed together to provide additional rigidity and ensure good grounding between the two layers. Figure 6.6 and 6.7 shows the DPA assembly photographs, top-down and side-profile:

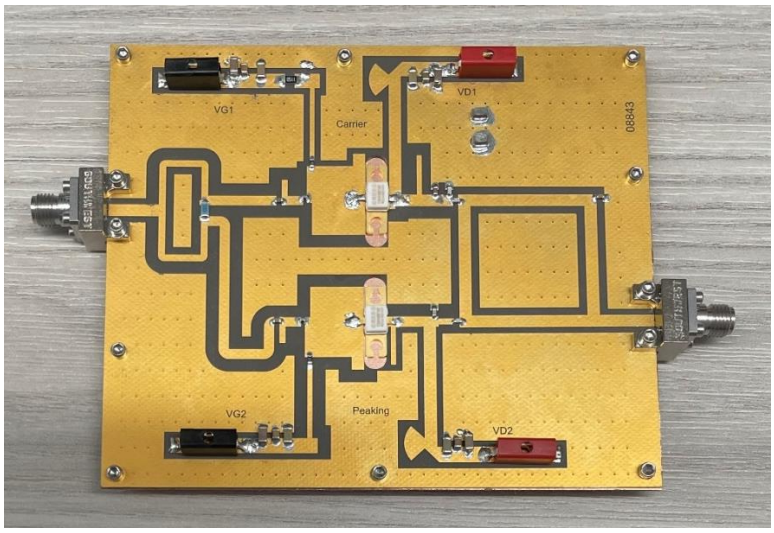


Figure 6.6: Photograph of DPA Assembly, Top-Down – Unit 1.

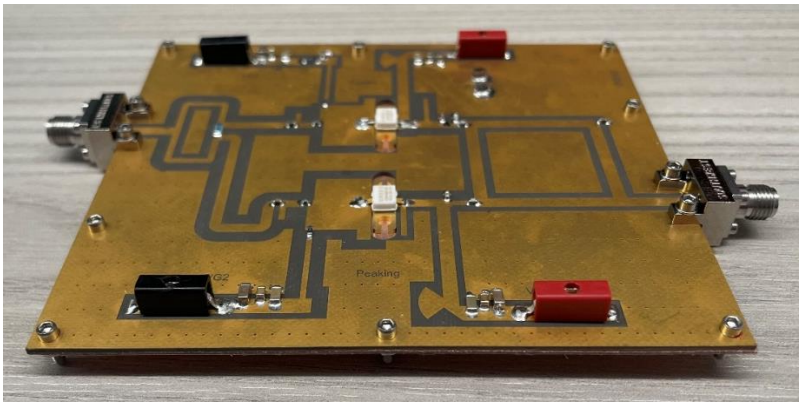


Figure 6.7: Photograph of DPA Assembly, Side-Profile – Unit 1.

7. MEASUREMENT RESULTS

This section defines test benches used for amplifier characterization and Class F PA and Class F^{-1}/F DPA measurements.

7.1 Experimental Set Up

S-parameters are characterized to determine maximum gain and minimum return loss using a Keysight PNA-X. The PNA-X ports are calibrated for power and cable loss using an external 40GHz power sensor and electronic calibration module (ECal). The DUT is then connected to the PNA-X as shown in Figure 7.1:

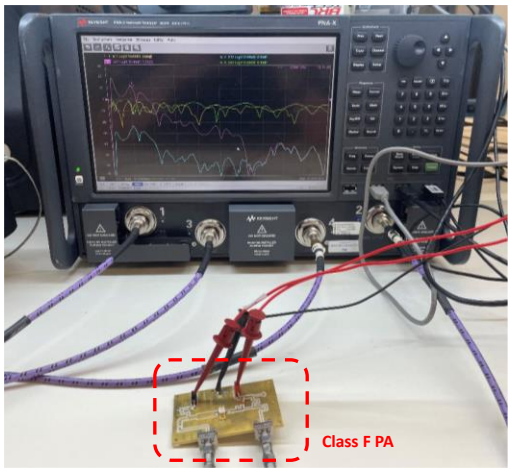


Figure 7.1: Photograph of Class F Amplifier S-parameter Characterization.

Basic output power vs input power sweeps are also characterized on the PNA-X using the differential I/Q measurement class. The following Figures 7.2 and 7.3 show the schematic and photograph of the test set up used to generate an input/output power sweep on the PNA-X:

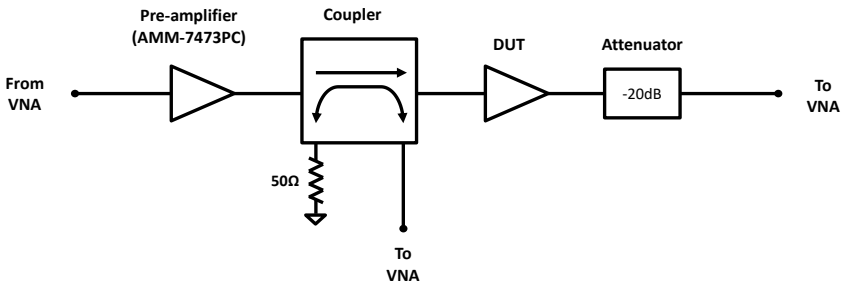


Figure 7.2: VNA Output Power Sweep Test Circuit Schematic with AMM-7473PC Pre-Amplifier.

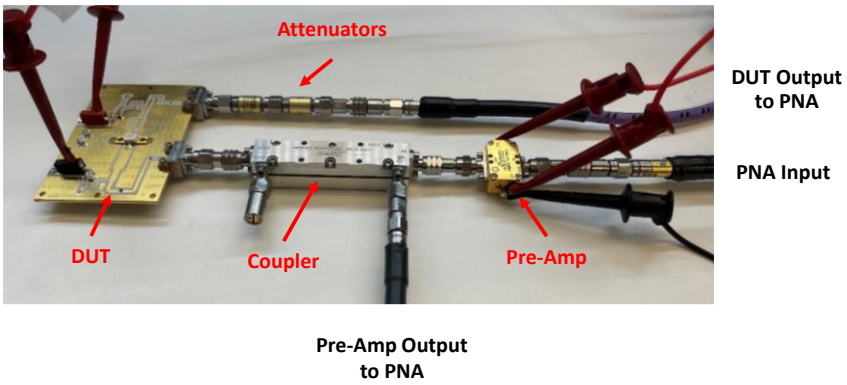
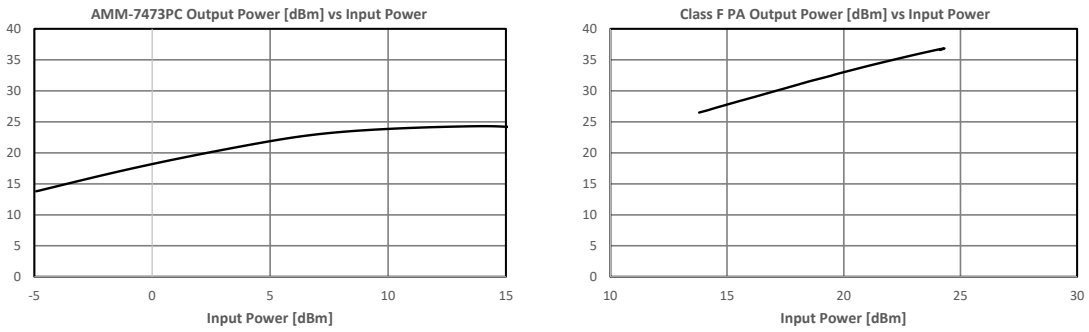


Figure 7.3: Photograph of VNA Output Power Sweep Test Circuit.

The PNA-X ports output a maximum of 14dBm up to 10GHz which is insufficient to saturate the Class F PA, therefore a pre-amplifier (Marki AMM-7473PC) was used to amplify the input power. A low-loss coupler (Marki C13-0150) was used to monitor the power output by the pre-amplifier input to the DUT – this is then set as the reference for DUT input power. Attenuators are placed after the DUT to prevent the output power from exceeding the PNA-X's maximum input power (27dBm). Additional s-parameter measurements taken on the attenuators and couplers are used to calibrate out thru-line losses. Figure 7.4 shows the AMM-7473PC and Class F Pout vs Pin sweep generated from this test configuration:



(a) (b)

Figure 7.4: AMM-7473PC Pre-amplifier (a) and Class F PA (b) Output Power Sweep.

As seen in Figure 6.4 (a), the AMM-7473PC saturates at 24dBm output (which is the maximum single-tone input allowed by HEPA-SDC rules) and drives the Class F PA output to 36.8dBm (4.7W) which confirms the designed Class F PA the minimum output power specification. This test configuration allows rapid power sweep characterization at different frequencies; however, it cannot

monitor the DC current directly to calculate PAE, and the output power limit prevents further characterization of the device.

Alternatively, the power sweep curve can be generated manually by monitoring the DUT input and output with power meters at discrete input powers levels. This test bench switches the AMM-7473PC pre-amplifier for a 50W 500kHz-2.5GHz PA to further drive the DUT into saturation. The drain voltage and DC current are recorded at each input power from the DC power supply to calculate a single-tone PAE curve. Figures 7.5 and 7.6 show the schematic and photograph for the updated test bench:

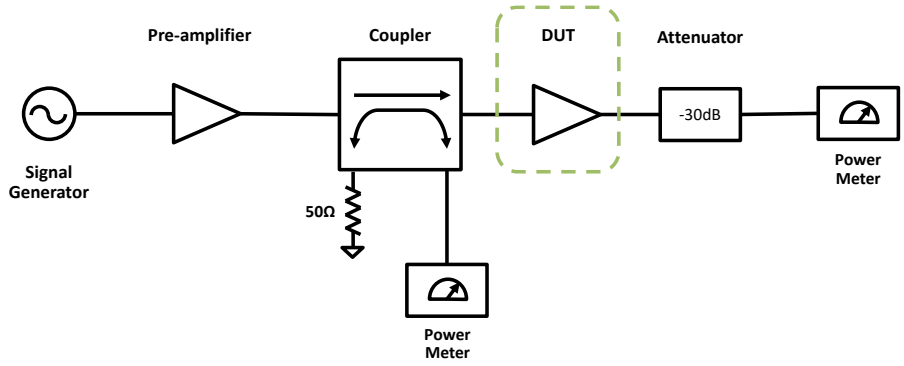


Figure 7.5: Single-Tone Power Sweep Test Bench Schematic.

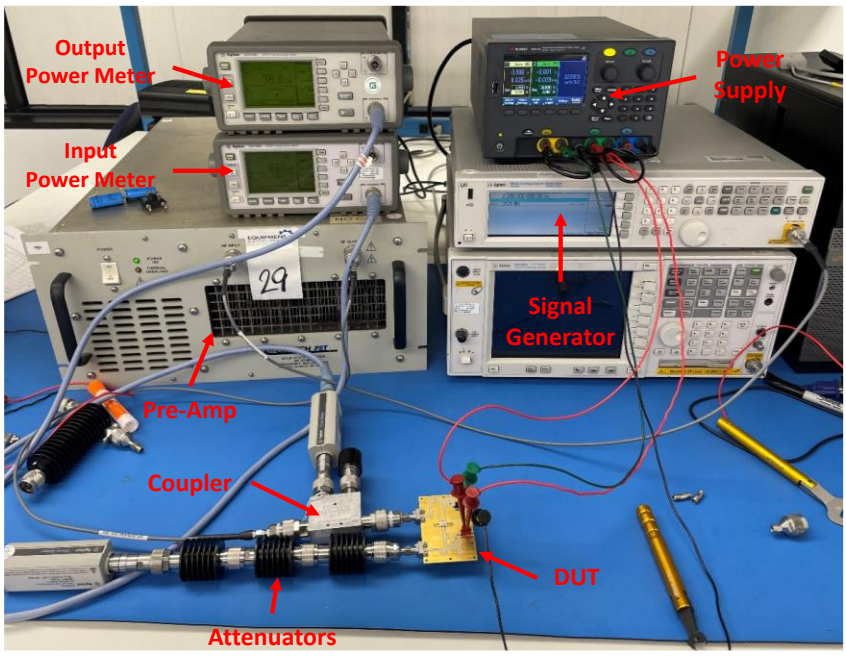


Figure 7.6: Photograph of Single-Tone Power Sweep Test Bench.

The test bench shown in Figure 6.6 is further modified by adding a power combiner and an additional signal generator to generate a two-tone input. The two-tone total input power is monitored on the power

meter through a coupler while the total output power is monitored similarly through a high-power, low-loss coupler. The DUT's output power is attenuated and monitored by a spectrum analyzer to determine IM3 over input power – the spectrum analyzer measurements are calibrated to account for the attenuators and cable losses. Figures 7.7 and 7.8 show a schematic and photograph of the test bench used to characterize two-tone measurements on the Class F PA and DPA:

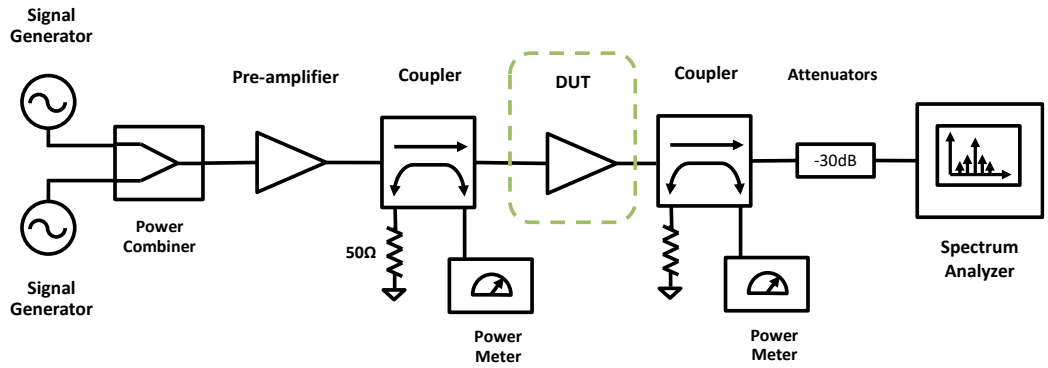


Figure 7.7: Two-Tone Power Sweep Test Bench Schematic.

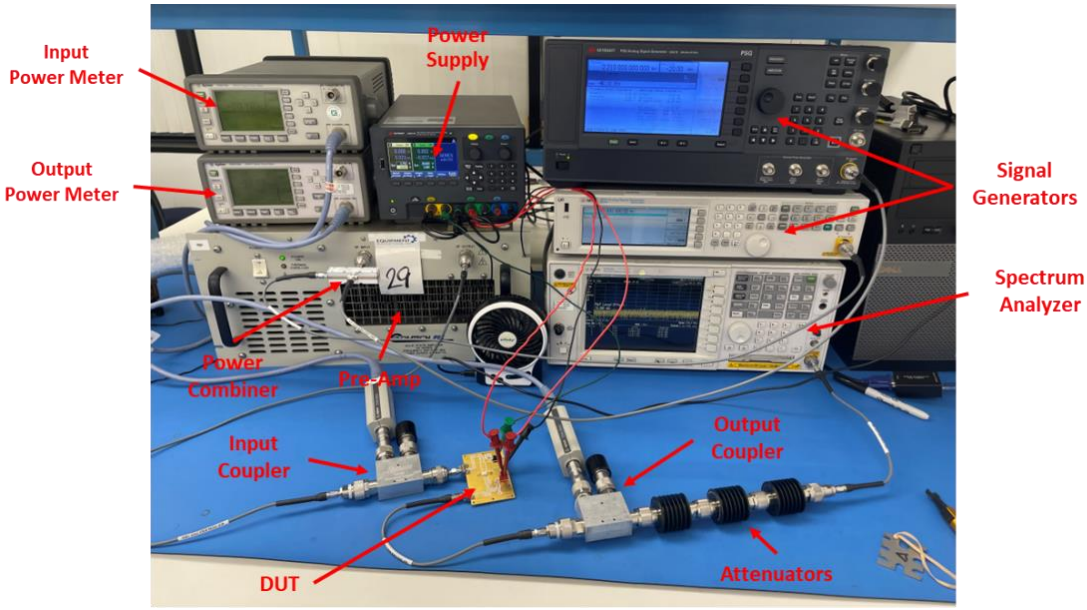


Figure 7.8: Photograph of Two-Tone Power Sweep Test Bench.

Prior to testing with the designed amplifiers, two input tones with 20MHz spacing and equal power are input to the combiner and pre-amplifier without the DUT to confirm the pre-amplifier is linear throughout the input power sweep. The DUT is then placed in line with the pre-amplifier to measure the output spectrum. Figure 7.9 shows the output spectrum of the designed DPA with a -10dBm per tone

input power, and Figure 7.10 shows the output spectrum when the DPA is subject to 21dBm per tone input power. As seen in Figures 7.9 and 7.10, the IM3 products are in the noise floor at low input powers, however these products become identifiable with increasing input power.

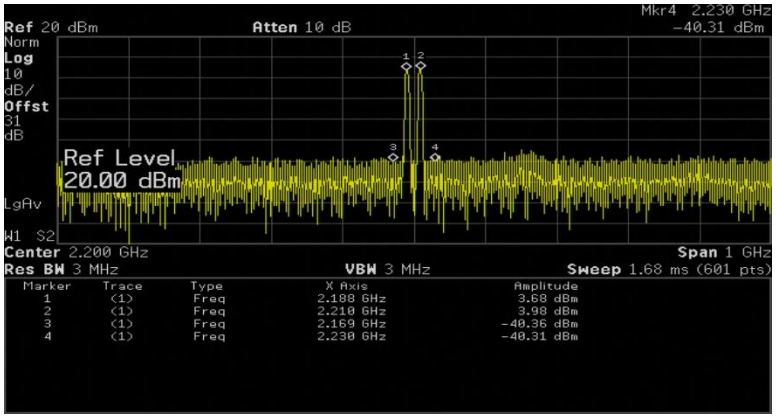


Figure 7.9: Output Spectrum of DPA with -10dBm per Tone Input Power, 20MHz spacing at 2.2GHz with IM3 Products in the Noise Floor.

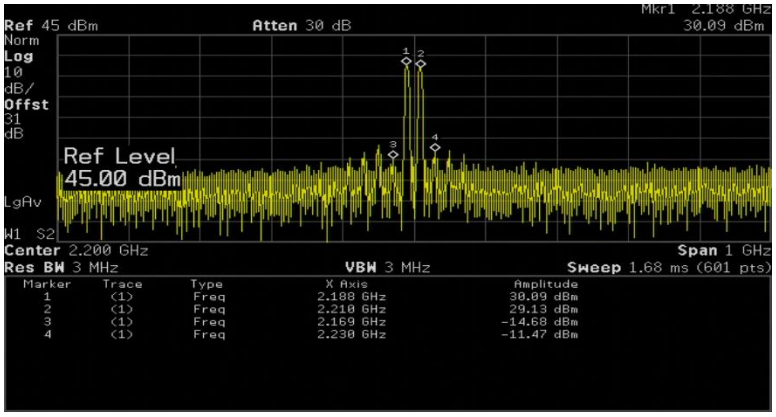


Figure 7.10: Output Spectrum of DPA with 21dBm per Tone Input Power, 20MHz spacing at 2.2GHz with over -40dBc IM3 Products.

7.2 Class F Amplifier Measurements

After setting up the test benches, the two fabricated PAs were characterized to generate the same plots created in simulation. Figure 7.11 shows the measured s-parameters at -15dBm input with V_d = 28V and V_g = -2.75V.

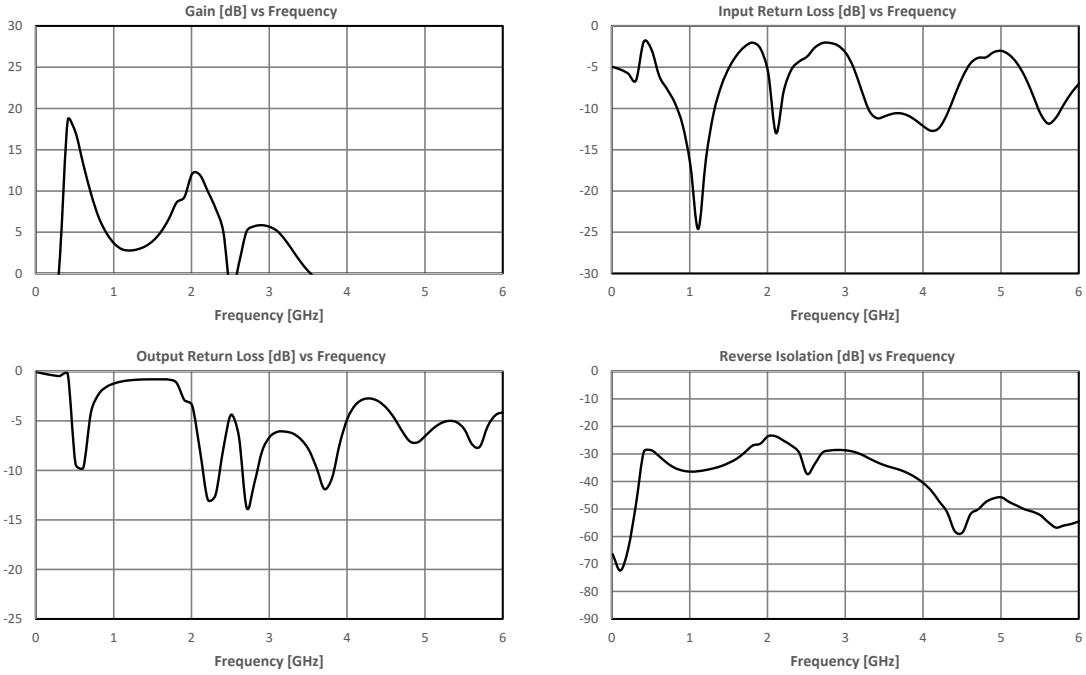


Figure 7.11: Class F Unit 1 PA Measured S-parameters, V_d = 28V, V_g = -2.75V.

The PA achieves ~12dB gain at 2.1GHz which is slightly shifted down from the simulated 19dB gain maximum at 2.2GHz. The discrepancy in gain is attributed to the poor return loss characteristic from input impedance matching. Additionally, the circuit losses were not accounted for in the simulation, however these effects are negligible compared to the impedance mismatch caused by the transistor lead transition. As shown in Figure 6.3, the transistor leads are not flush with the trace due to the brass plate missing a cutout for the transistor. As a result, there is increased parasitic inductance due to the transistor leads acting like wire bonds - this impedance mismatch is likely causing the -13dB return loss at 2.1GHz compared to the simulated -30dB return loss resulting in poor gain performance. In simulation, the amplifier showed optimal IM3 performance at 2.4GHz, however the measured gain at 2.4GHz drops off significantly resulting in poor single-tone and two-tone performance. In simulation, the operating frequency was set slightly above the maximum gain frequency to decrease the IM3 products and meet

the 30dB C/I linearity requirement. Therefore, the Class F PA power sweep and PAE are first characterized at 2.2GHz as shown in Figure 7.12:

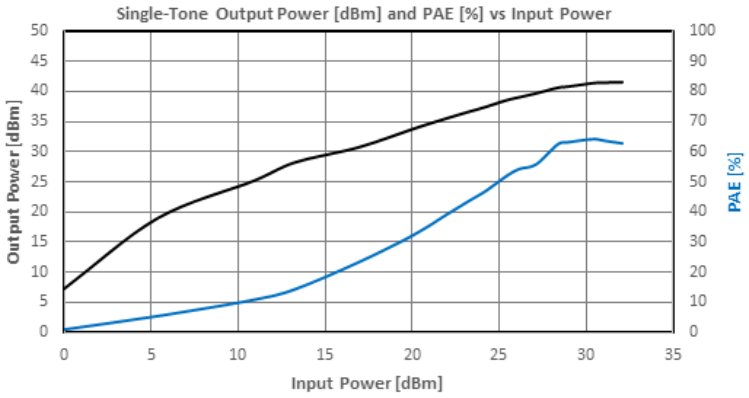


Figure 7.12: Class F Unit 1 PA Single-Tone P_{out} and PAE vs Input Power Sweep at 2.2GHz, V_d = 28V, V_g = -2.75V.

Compared to simulation results, the output power sweep shows output saturation at 41.5dBm with ~30dBm input – this is ~0.5dBm lower than simulation which can be attributed to previously unaccounted circuit losses. With a single-tone CW input at 24dBm, the Class F PA outputs ~37dBm which meets the minimum requirement for HEPA-SDC design rules. This input power also corresponds to a 45% PAE which is higher than the simulated 37%. The peak PAE is 64% when the amplifier is saturated with a 30dBm input as expected for a Class F amplifier.

Linearity measurements were completed next using two equal amplitude tones spaced at 20MHz about a 2.2GHz center frequency. The two-tone power sweep, PAE, and IM3 measurements are presented below, Figure 7.13:

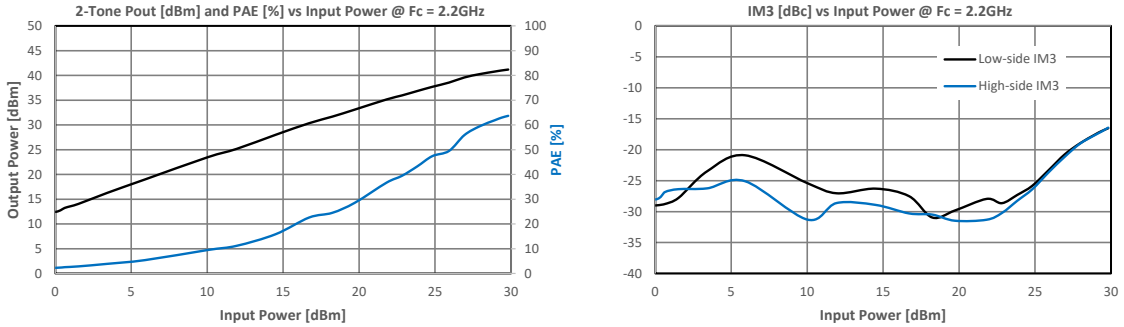


Figure 7.13: Class F Unit 1 PA Two-Tone P_{out}, PAE and IM3 vs Input Power Sweep at Fc = 2.2GHz, V_d = 28V, V_g = -2.75V.

Similar to the single-tone power sweep, the average two-tone output power begins to saturate at 41.2dBm with 30dBm input power. At 30dBm total input power, the amplifier achieves 63.8% PAE similar to the single-tone test, however the high-side and low-side IM3 are -16dBc. When swept from 0dBm to 24dBm total input power, the required 30dB C/I ratio is not maintained, however both IM3 are below -30dBc at 18.5dBm total input power which corresponds to a 28% PAE. It is also noted that the low-side IM3 is ~3-4dB higher than the high-side IM3 – this is attributed to the narrow bandwidth of the amplifier. When operating at 2.2GHz center frequency and 20MHz tone spacing, the low-side tone experiences higher gain relative to the high-side tone resulting in higher IM3 generation at the low-side tone.

Additional characterization was done at a 2.1GHz center frequency to balance the IM3 products – the gain at 2.09GHz and 2.11GHz are of equal amplitude as seen in Figure 7.11:

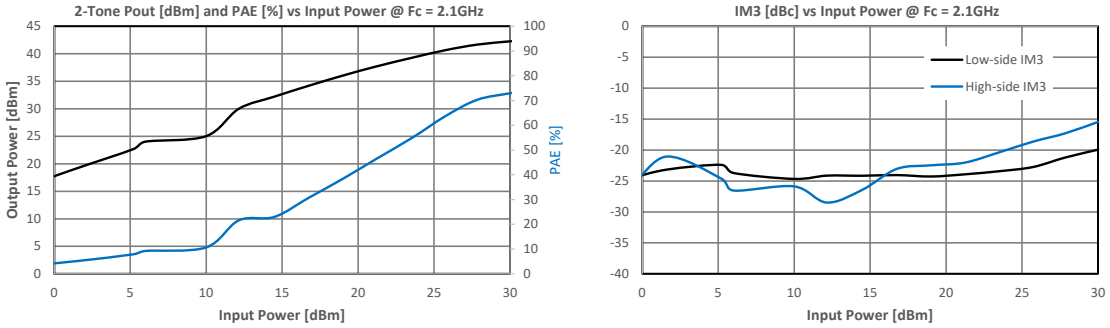


Figure 7.14: Class F Unit 1 PA Two-Tone P_{out}, PAE, and IM3 vs Input Power Sweep at Fc = 2.1GHz V_d = 28V, V_g = -2.75V.

Compared to the 2.2GHz center frequency, the Class F PA achieves a higher P_{sat} at 42.3dBm and PAE at 73% with 30dBm input. The low-side and high-side IM3 are consistent over input power due to the equal gain at each tone frequency, however the C/I ratio is typically 25dB.

The poor linearity and gain performance of the assembled Class F PA is likely due to the transistor assembly on to the PCB – the transistor is missing a cutout on the brass plate for the drain and gate to mount flush with the top traces. A second unit was built with shorter transistor leads to minimize any impedance mismatches caused by the non-planar lead-to-trace transition. The measured s-parameters are presented below, Figure 7.15:

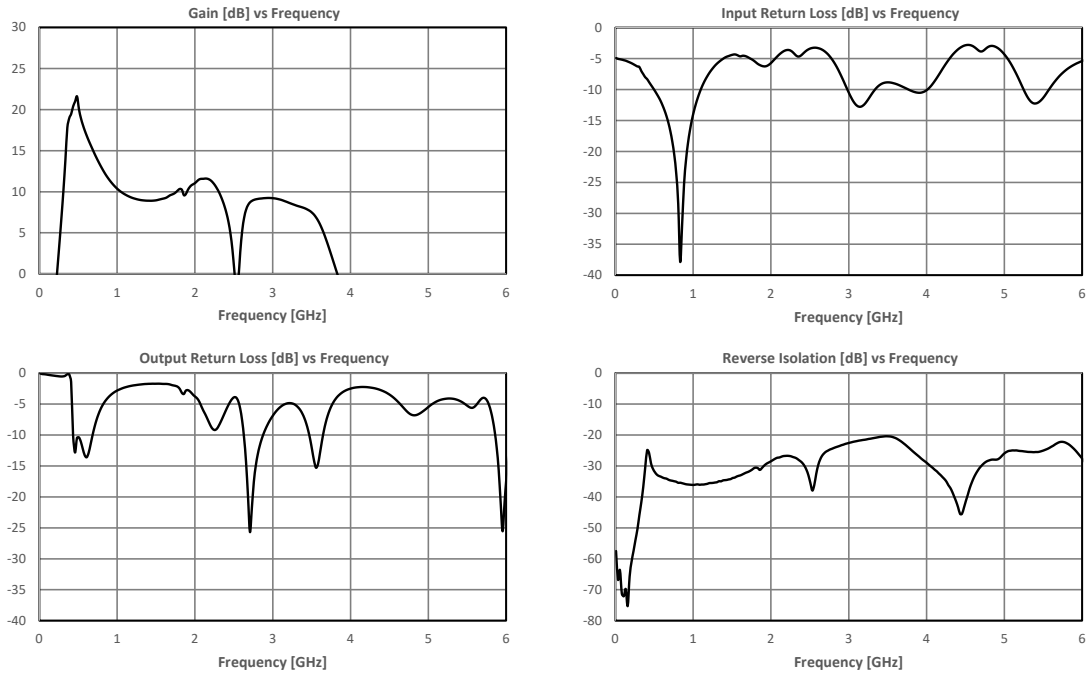


Figure 7.15: Class F Unit 2 PA Measured S-parameters, V_d = 28V, V_g = -2.75V.

Compared to the previously built Class F amp, the adjustment to the leads improved input matching as demonstrated by the 2dB return loss improvement. The amplifier's operating bandwidth about 2.2GHz increased and demonstrated improved gain flatness at 12.2dB. The two-tone measurements on the second Class F amplifier are presented below (Figure 7.16) with 20MHz tone spacing about 2.2GHz, Vd set to 28V, and Vg set to -2.75V:

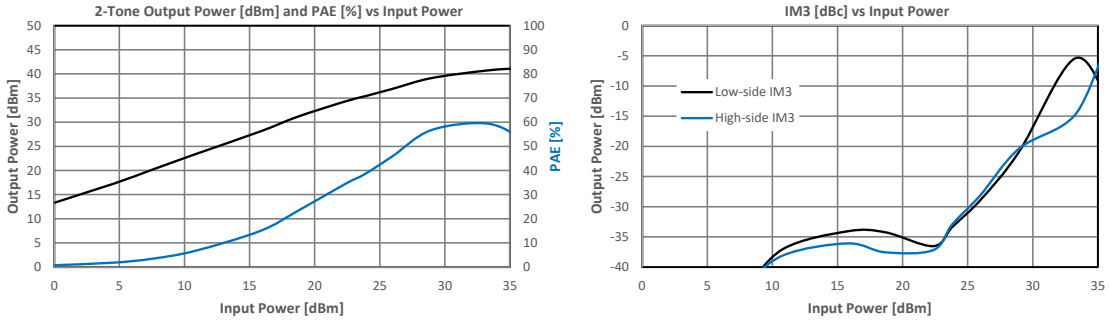


Figure 7.16: Class F Unit 2 PA Two-Tone P_{out}, PAE, and IM3 vs Input Power Sweep at Fc = 2.2GHz, V_d = 28V, V_g = -2.75V.

The modified Class F amplifier shows improved IM3 performance and maintains over 30dB C/I ratio through 24dBm total input power - this corresponds to a 30% PAE and 33.4dBm total output power. A quick test with 24dBm CW input at 2.2GHz confirms the amplifier outputs 36.25dBm - this meets 4W output minimum requirement.

To further tune the Class F PA Unit 2, additional tests with varying gate bias voltages were conducted. The following plots (Figure 7.17) show the output power, PAE, and IM3 performance over varying gate voltage:

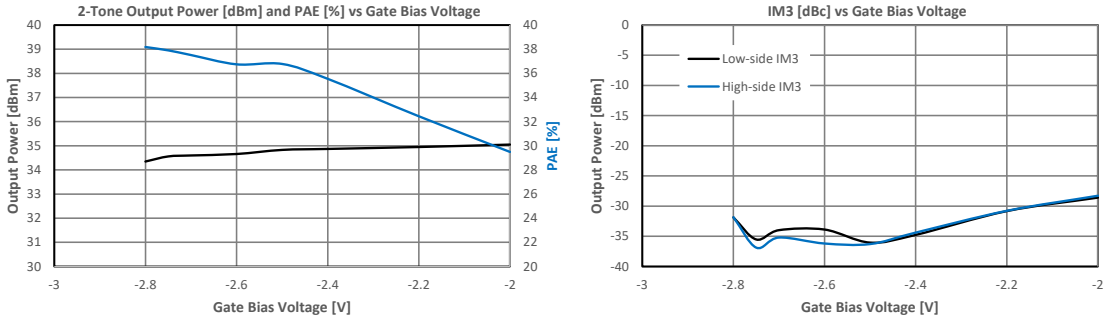


Figure 7.17: Class F Unit 2 Two-Tone P_{out}, PAE, and IM3 vs Gate Voltage at Fc = 2.2GHz, V_d = 28V, V_g = -2.75V.

When increasing gate bias voltage from -2.8V to -2V, total output power increases by less than 1dB while PAE decreases by nearly 10%. At -2V gate voltage, the C/I ratio falls below 30dB. Therefore, the fabricated Class F amp should be biased with at most -2.5V to maintain balance between high PAE and linearity. Table 7.1 provides key measurement values for the Class F amplifiers:

Table 7.1: Class F Measurement Summary.

Amplifier	**Center Frequency [GHz]**	**V_d [V]**	**V_g [V]**	**Pout @ 24dBm Input [dBm]**	**PAE @ 30dB C/I [%]**
Class F – Unit 1	2.2	28	-2.75	36.8	Does not meet
Class F – Unit 2	2.2	28	-2.75	36	40%

7.3 DPA Measurements

After characterizing two Class F PA units, the DPA is experimentally measured on the same test benches. Figure 7.18 shows the DPA's measured s-parameters with -15dBm input power and Vd set to 28V, the carrier amplifier gate set at -2.45V, and the peaking amplifier gate set at -5.75V.

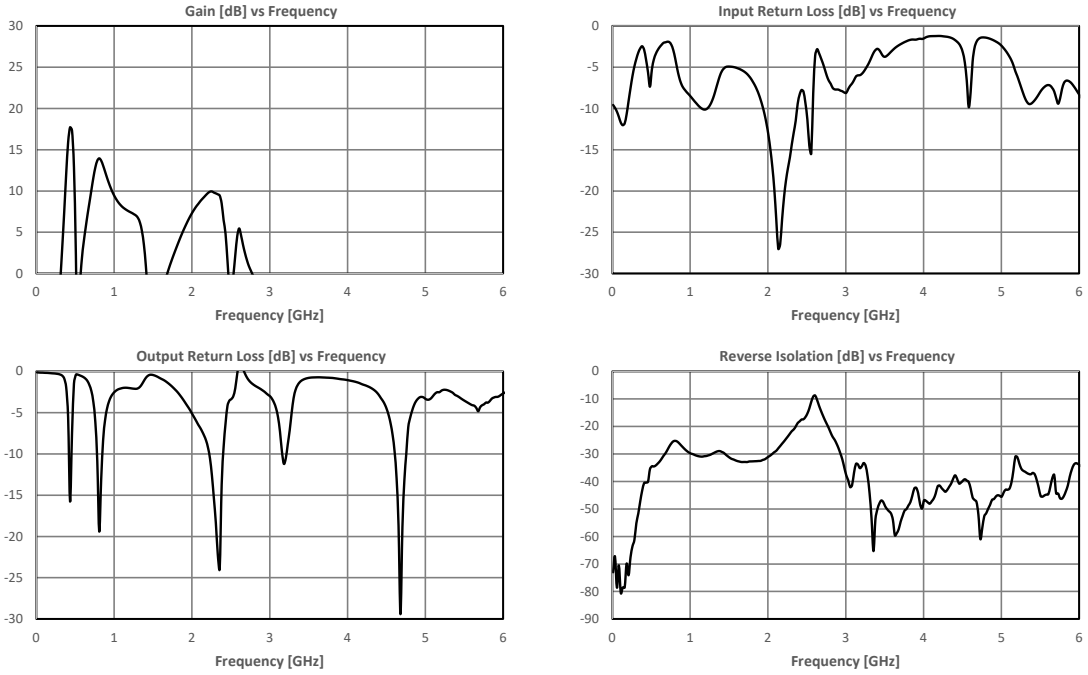
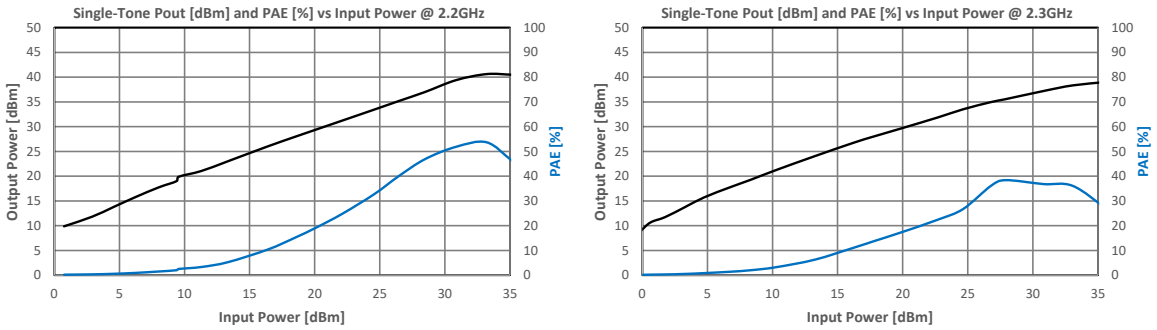


Figure 7.18: DPA Unit 1 Measured S-parameters, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

Compared to simulation results, the fabricated DPA has 3dB lower gain and a narrower bandwidth about 2.3GHz. The amplifier also shows >10dB gain from 0.5-1GHz which was expected to be <5dB from simulation. This error is likely caused by assembly issues with the DPA. Similar to the Class F PA, the transistor's leads on the DPA are slightly elevated causing a wirebond-like transition from the transistor to the top layer traces. At 2.3GHz, the amplifier exhibits excellent input and output return loss at -20dB and -15dB respectively.

The DPA is then characterized with a single-tone CW input shown in Figure 7.19:



(a) (b)

Figure 7.19: DPA Unit 1 Single-Tone P_{out} and PAE vs Input Power Sweep at 2.2GHz (a) and 2.3GHz (b), V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

The single-tone power sweep and PAE curves were generated at 2.2GHz and 2.3GHz. At both frequencies, the amplifier saturates near 39dBm with a 34dBm input power which is well below the simulated 44dBm. Additionally, the calculated PAE performance does not meet the expected >50% from simulated results. This is attributed to the poor gain performance on the fabricated amplifier – the gain rolls off steeply about 2.2GHz resulting in narrowband operation. Figure 7.20 shows DPA unit 1 two-tone measurement results:

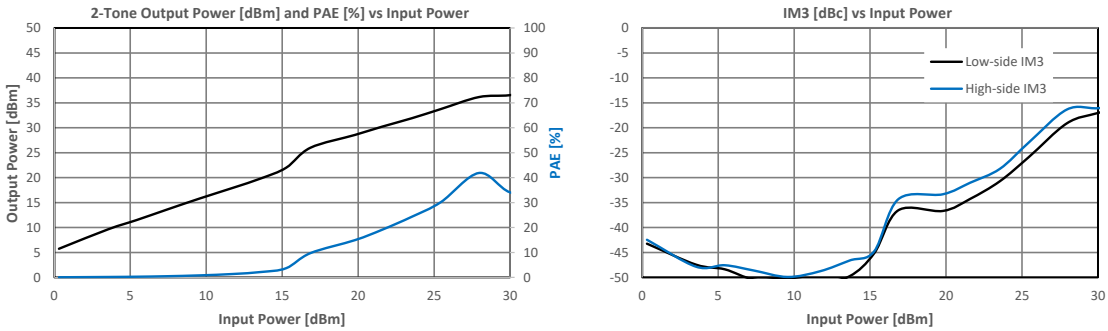
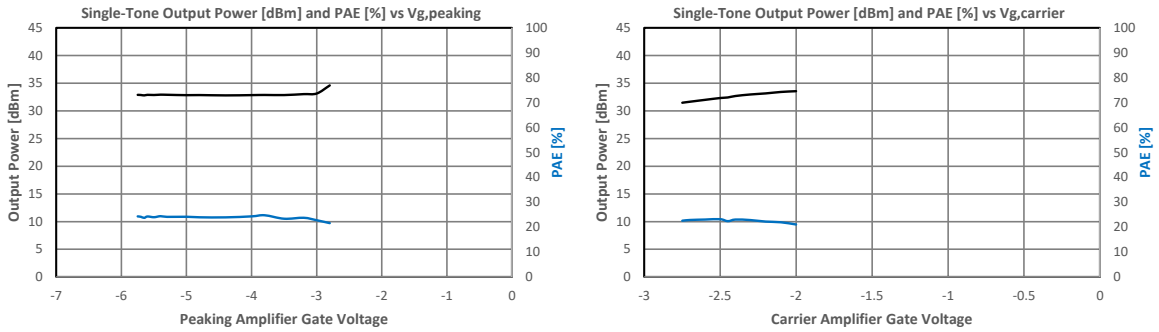


Figure 7.20: DPA Unit 1 Two-Tone Pout, PAE, and IM3 vs Input Power Sweep at Fc = 2.2GHz, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

When subject to a two-tone input centered about 2.2GHz, the amplifier exhibits excellent C/I ratio performance with over 30dB C/I when total input power is swept from 0 to 24dBm. The high-side IM3 falls below 30dB C/I at 24dBm total input power, therefore the total input power is backed off to 23dBm. This corresponds to a 30dBm total output power and 24% PAE. This deviation from simulation results is likely due to the excess current draw on the carrier amplifier.

Additional tuning to the peaking amplifier gate voltage and carrier amplifier gate voltage was used to improve output power and PAE. The DPA is subject to a constant 24dBm total input power at 2.2GHz CW input.



(a) (b)

Figure 7.21: DPA Unit 1 Single-Tone P_{out} and PAE vs Peaking Amplifier Bias (a) and Carrier Amplifier Bias (b), V_d = 28V, $V_{g,carrier}$ = -2.75V (or varies), $V_{g,peaking}$ = -5.75V (or varies).

Figure 7.21 (a) shows output power and PAE over peaking amplifier bias voltage ($V_{g,peaking}$) while the carrier amplifier bias voltage ($V_{g,carrier}$) is maintained at -2.45V. When the $V_{g,peaking}$ is increased towards 0V, the total output power increases at the cost of efficiency – this is expected from increasing the I_{dq} of the peaking amplifier. It is noted when the peaking amplifier is biased in "deep-AB" along with the carrier amplifier, the DPA maintains ~24% PAE. When $V_{g,carrier}$ is varied from -2.75V to -2V, as seen in (b), there is 3dB increase in output power with less than 2% change in PAE.

A second DPA unit is constructed to debug the poor PAE performance in the previously measured unit. Although the stackup uses an additional RT5880 layer as a common ground and a heatsink, the material does not provide enough rigidity for the PCB. This causes significant gain variance between units and lab benches. Additional screws were placed to bind the two PCB layers closer, and solder was used to adhere the two layers together. The following Figures 7.22 and 7.23 show the second unit constructed for testing, top-down and side-profile:

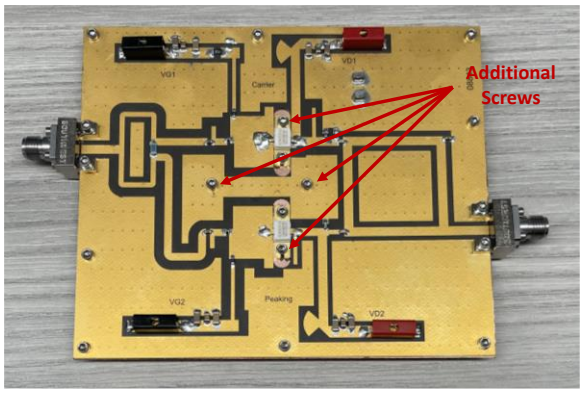


Figure 7.22: Photograph of DPA Assembly, Top-down - Unit 2.

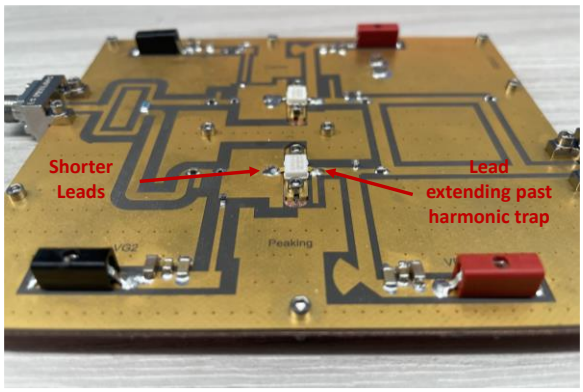


Figure 7.23: Photograph of DPA Assembly, Side-Profile – Unit 2.

The second DPA was constructed with more care to minimize the transistor lead lengths and the amount of solder used. DPA unit 2 shows some improved performance in the measured s-parameters below (Figure 7.24):

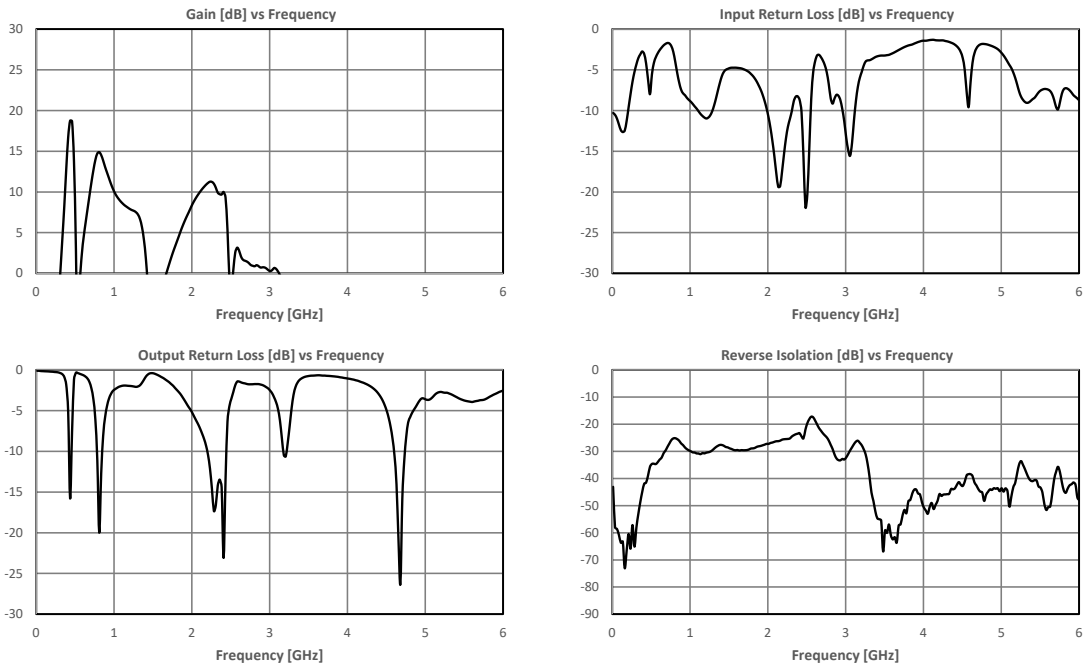


Figure 7.24: DPA Unit 2 Measured S-parameters, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

Compared to the previous manufactured DPA, the gain at 2.2GHz increased by 2dB and DPA demonstrates equal gain amplitude at 20MHz bandwidth about 2.2GHz. However, there is still significant gain from 0.5 to 1.5GHz. Similar to the Class F assembly, the transistor leads sit slightly above the top layer trace, resulting in a PCB launch similar to a wirebond. The drain lead extends beyond the first peaking amplifier harmonic trap resulting in an impedance mismatch which may be causing the low frequency gain and poor gain performance about 2.2GHz compared to simulation results.

The single-tone measurement results for DPA Unit 2 are presented in Figure 7.25:

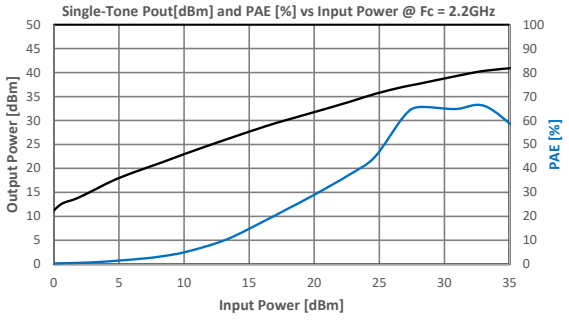


Figure 7.25: DPA Unit 2 Single-Tone Pout and PAE vs Input Power Sweep at Fc = 2.2GHz, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

The improved grounding increased the DPA's gain to 12dB, but the peak gain region is too narrowband for 20MHz bandwidth operation resulting in poor gain with a two-tone input. Two-tone

output power, PAE, and IM3 were swept at 2.2GHz and 2.3GHz center frequencies as shown in Figure 7.26 and 7.27 respectively:

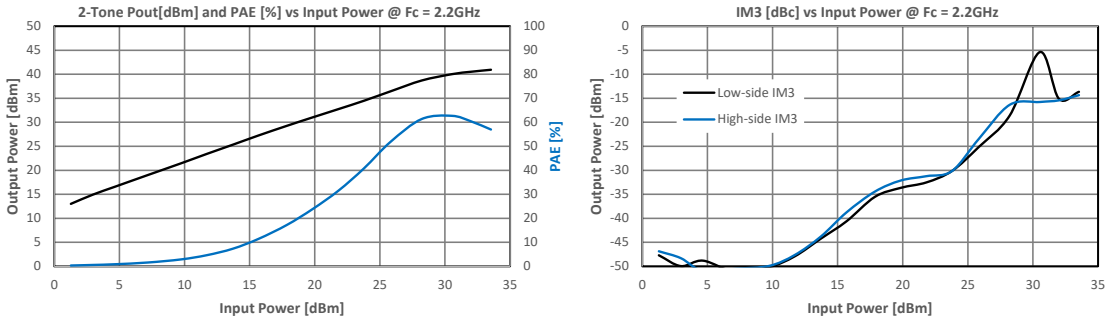


Figure 7.26: DPA Unit 2 Two-Tone Pout, PAE, and IM3 vs Input Power Sweep at Fc = 2.2GHz, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

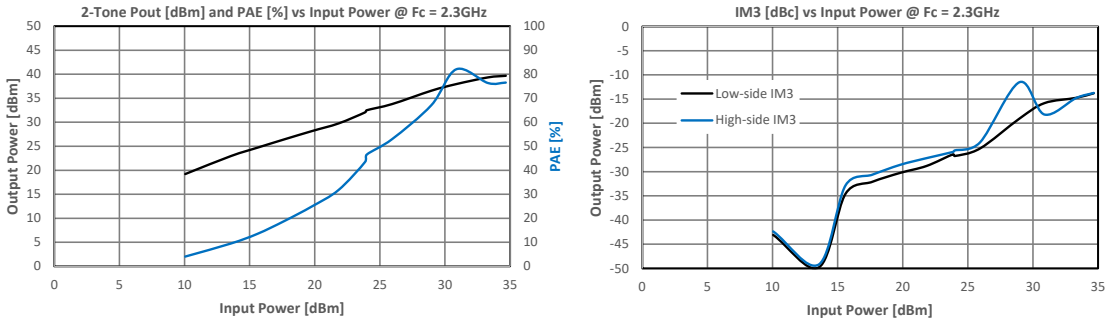


Figure 7.27: DPA Unit 2 Two-Tone Pout, PAE, and IM3 vs Input Power Sweep at Fc = 2.3GHz, V_d = 28V, $V_{g,carrier}$ = -2.75V, $V_{g,peaking}$ = -5.75V.

Compared to the previously built unit, the second DPA achieves higher output saturated power at 41dBm with a 2.2GHz center frequency. At 24dBm input, the DPA maintains the 30dB C/I ratio and has 45% PAE. From 0 to 15dBm input power, the DPA maintains over 40dB C/I ratio which is an improvement from the Class F PA IM3 performance. At 2.3GHz center frequency, the 30dB C/I ratio is not maintained beyond 17dBm total input power, however when driven towards saturation, the PAE reaches over 80% with 32dBm total input power. Table 7.2 summarizes key measured DPA parameters:

Table 7.2: DPA Measurement Summary.

Amplifier	**Center Frequency [GHz]**	**V_d [V]**	**$V_{g,carrier}$ [V]**	**$V_{g,peaking}$ [V]**	**Pout @ 24dBm Input [dBm]**	**PAE @ 30dB C/I [%]**
DPA – Unit 1	2.2	28.0	-2.75	-5.75	33.0	27.0
DPA – Unit 2	2.2	28.0	-2.75	-5.75	35.1	45.0

7.4 Summary of Results

As per HEPA-SDC competition rules, the designed PA must operate at a frequency between 1 to 10GHz. When excited by a single-tone carrier, the amplifier must output between 36 to 46dBm with no greater than 24dBm input power. An additional linearity test with two equal amplitude tones spaced 20MHz apart about a chosen center frequency characterizes the C/I ratio. With 0dBm input per tone, the C/I ratio must be greater than 30dB. The input tone powers are swept from 0dBm to 21dBm (corresponding to total input power of 3dBm up to 24dBm), and PAE is measured when the C/I ratio first falls below 30dB. If the 30dB C/I ratio is maintained, the PAE is measured at 21dBm per tone input power.

The following Tables 7.3 and 7.4 summarize key performance indicators for the designed, assembled, and tested Class F PAs and DPAs with single-tone and two-tone measurements compared to the design goals. The blue parameters indicate acceptable values while red indicates unacceptable performance:

Table 7.3: Comparison of Single-Tone Measurements to Design Goals.

Parameter	Design Goal	Class F Unit 1	Class F Unit 2	DPA Unit 1	DPA Unit 2
Center Frequency [GHz]	1 - 10	2.2	2.2	2.2	2.2
Gain [dB]	≥ 12	12	12	10	11
Output Power @ Single-Tone 24dBm Input [dBm]	36 - 46	37	36.25	33	35.1
PAE @ Single-Tone 24dBm Input [%]	--	32	45	24	41
Saturated Output Power [dBm]	--	41	41.5	40	41
Peak PAE [%]	--	60	64	40	65

Table 7.3 presents single-tone CW measurements. The key parameter is output power generated by a single 24dBm input tone – the minimum spec for the competition is 36dBm output power. In order to achieve this spec, the amplifier must have at least 12dB gain. The DPA's do not meet this spec and therefore are eliminated from participating in the HEPA-SDC. The Class F Unit 1 PA outputs 37dBm with a 24dBm input at 2.2GHz and achieves 45% PAE. Class F Unit 2 outputs 36.25dBm output power when subject to the 24dBm input tone and achieves 32% PAE. When driven into saturation, the Class F Unit 2 PA reaches 41dBm saturated output power and reaches a peak PAE of 60% which is slightly lower than the 41.5dBm saturated output power and 64% PAE obtained by Unit 1.

All four fabricated PAs are also tested with a two-tone input about the selected center frequencies – Table 7.5 presents the experimentally measured results:

Table 7.4: Comparison of 2-Tone Measurements to Design Goals.

Parameter	**Design Goal**	**Class F Unit 1**	**Class F Unit 2**	**DPA Unit 1**	**DPA Unit 2**
C/I Ratio @ 0dBm per Tone Input [dB]	>30	27	>40	43	45
Maximum Total Input Power for <30dB C/I Ratio [dBm]	--	--	>24	23	24
Total Output Power for <30dB C/I Ratio [dBm]	--	--	36	32	34
Peak PAE at <30dB C/I Ratio [%]	--	--	40	25	45
Saturated Output Power [dBm]	--	41	41	37	41
Peak PAE [%]	--	64	60	42	63

The presented two-tone CW measurements have 20MHz tone spacing with equal amplitude input tones about 2.2GHz. The two-tone design goal was to obtain over 30dB C/I ratio when the PA is subject

to 0dBm input tones. Class F Unit 1 does not meet 30dB C/I ratio when subject to 0dBm per tone input power, therefore it is eliminated from participating in the HEPA-SDC. The remaining Class F PA Unit 2 maintains 30dB C/I ratio up to 25dBm total input power and meets the competition requirements for >30dB C/I ratio with 0dBm input per tone. At the 24dbm maximum total input power (corresponding to 21dBm per tone input), the Class F PA presents 40% PAE. The PA scores 48.7 according to the HEPA-SDC FOM score which includes a multiplier based on center frequency. This score falls short of previous FOM records of 87.6 [27].

DPA Unit 1 and Unit 2 maintained over 30dB C/I ratio throughout the power sweep, however the PA suffered from poor gain performance preventing the amplifier from meeting the minimum output power specifications in the single-tone tests. DPA Unit 2 achieves 45% PAE with 21dBm per tone input, which is an improvement over the Class F Unit 2 PA at 40%. Both amplifiers output 41dBm saturated output and have a peak PAE over 60% when driven beyond the competition's maximum input power.

7.5 Competition Results

The 19th HEPA-SDC hosted at IMS 2023 saw a total of 6 PA designs submitted by competitors from around the world. Two PAs were withdrawn from competition due to missing the minimum output power requirement and therefore could not enter for the linearity test. The following Table 7.5 presents the measurement results from the competition with the Class F PA presented in this thesis highlighted in blue:

Table 7.5: IMS 2023 HEPA-SDC Competition Results.

Entry #	Team (Country)	PA Topology	Frequency [GHz]	PAE [%]	Score
1	Cal Poly (USA)	Class F (This Work)	2.2	40	48.71
2	Cal Poly (USA)	Class F	1.45	32.57	35.74
3	FAU (Germany)	DPA	3.80	58.25	81.32
4	FAU (Germany)	DPA	3.78	54.13	75.48
5	U. College Dublin (Ireland)	DPA	3.01	52.46	69.09
6	CINVESTAV-IPN (Mexico)	--	2.95	--	--

Unfortunately, the Class F amplifier designed in this thesis that was selected to compete at the HEPA-SDC did not meet the minimum output power requirement of 36dBm by 2dB. During testing at

the competition, the amplifier exhibited poor drain current stability when the gate was swept from -4V towards -2.7V to set the desired I_{dq}. The amplifier was likely damaged in transit to the competition location which prevented the amplifier from competing. Further testing post-competition concluded that the transistor source was not adhered to the brass plate fully resulting in an intermittent ground connection. Additional screws were placed in the Class F Unit 2 assembly as seen in Figure 7.28:

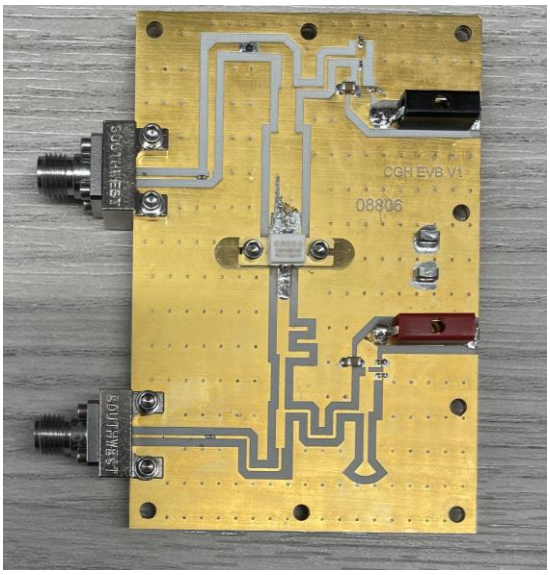


Figure 7.28: Photograph of Fixed Class F Unit 2 Amplifier.

The PA was characterized again for s-parameters (Figure 6.28), single-tone power sweep (Figure 6.29), and two-tone power sweeps (Figure 6.30):

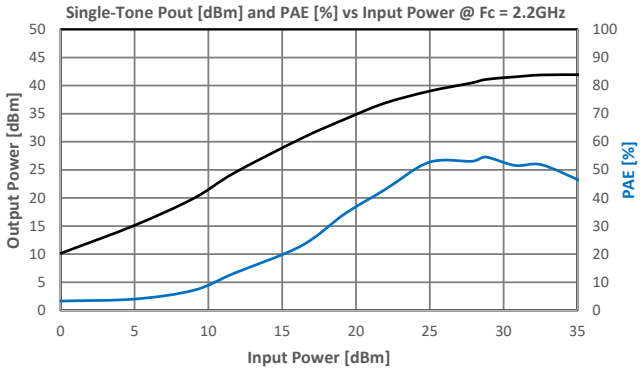


Figure 7.29: Measured Class F Unit 2 Single-Tone Power Sweep, F_c = 2.2GHz, V_d = 28V, V_g = -2.75V, Fixed Post-Competition.

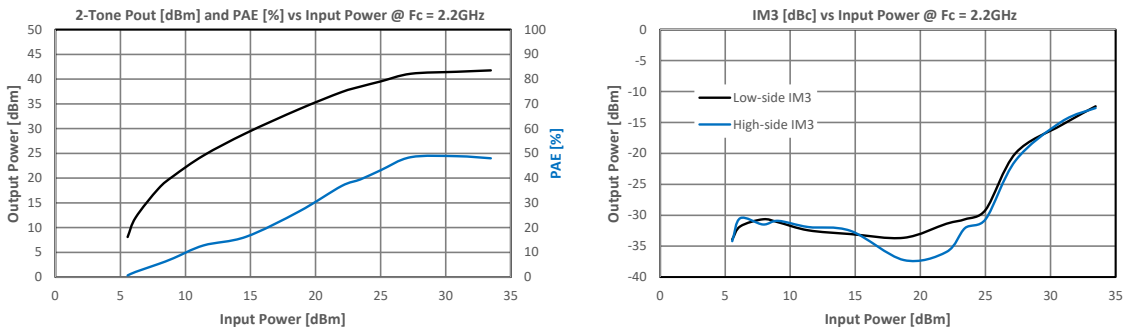


Figure 7.30: Measured Class F Unit 2 Two-Tone Power Sweep, Fc = 2.2GHz, Vd = 28V, Vg = -2.75V, Fixed Post-Competition.

The fixed Class F Unit 2 PA outputs 37dBm with a 24dBm input tone at 2.2GHz. When two tones spaced at 20MHz about 2.2GHz sweep from 0dBm to 21dBm per input tone, the Class F Unit 2 PA maintains over 30dB C/I throughout the power sweep. At 21dBm input per tone, the PA achieves 40% PAE – this corresponds to a FOM score of 48.71.

8. CONCLUSION

The work presented in this thesis provides the design, assembly, and test results for a high-linearity S-band Class F PA and Class F-based DPA. With careful gate bias and output matching network design, the Class F amplifier exceeded typical linearity performance expectations. The designed DPA expanded on the Class F topology and implemented harmonic trapping at the carrier and peaking amplifier output networks to improve efficiency. Additionally, a quadrature hybrid output network was implemented with a capacitive load to improve the DPA's linearity.

The presented Class F PA and DPA maintain at least 30dB C/I ratio up to 24dBm total input power while achieving 40% and 45% PAE respectively. The DPA saw 5% improvement in PAE and up to 15dB improvement in IM3 performance when the two tones are swept from 0dBm to 21dBm per tone when compared to the Class F PA. However, due to the impedance mismatch, the DPA saw decreased gain performance resulting in poor gain performance and narrow operating bandwidth. The designed Class F PA Unit 2 was selected to participate at IMS HEPA-SDC since it met the minimum 36dBm output power and minimum 30dB C/I ratio requirements. In competition, this PA theoretically scores 48.71, placing the Class F Unit 2 PA at 4^{th} overall against all competing amplifiers.

In future designs, care should be taken to improve the PA assembly. The non-planar lead-to-trace transitions caused impedance mismatches that were detrimental to the amplifier gain and input/output matching networks. Leads were soldered to the circuit beyond the correct launch location (Figure 6.22) which caused poor gain performance (~10dB), therefore the amplifier could not meet the 36dBm output requirement with the 24dBm input tone. The brass plate heat sink silver epoxied to the substrate should be retained as it provides a rigid structure and excellent thermal dissipation properties compared to the copper clad RT5880 sheet. This limitation was due to cost, however winning PA designs should spend the money to maximize PA performance.

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