

# DESIGN OF A RADIATION-HARDENED OPTICAL TRANSCEIVER

An Undergraduate Research Scholars Thesis

by

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# **ABSTRACT**

Design of a Radiation-Hardened Optical Transceiver

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Reliable and efficient communication links are vital in harsh environments where ionizing radiation is present. Optical links specifically are necessary to support the growing need for higher data rates and faster signal processing requirements of devices in these environments. For many years, radiation hardness in electronics has been achieved via specialized manufacturing processes in dedicated foundries. These techniques have failed to scale at the rate of commercial CMOS processes, disallowing for faster and more efficient circuits. One strategy to create radiation tolerant circuits while still retaining the benefits of commercial fabrication is a hard-by-design methodology. Techniques such as enclosed layout (EL) and triple modular redundancy (TMR) can be used to design circuitry tolerant to ionizing radiation.

This thesis demonstrates an optical transceiver in a 180nm CMOS process based on a transmit vertical-cavity surface-emitting laser (VCSEL) and a receive photo-detector (PD) with radiation-hardened circuitry. The transceiver has been characterized electrically and comparisons between the radiation-hardened and non radiation-hardened versions were performed in the Texas A&M Cyclotron Institute and Nuclear Engineering & Science Center (NESC).

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## Contributors

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All other work conducted for the thesis was completed by the student independently.

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# 1. INTRODUCTION

Radiation-hardened electronics have been a topic of interest for both analog and digital integrated circuit design for many years. The existence of energized particles in the form of ionizing radiation have the potential to disrupt circuit performance, especially in critical applications such as spacecraft inter-system communications or reactor electronics. Microelectronics in these environments must have the ability to withstand both the total ionizing dose (TID) effects from trapped charged particles and single event effects (SEEs) from high-energy particle strikes [1].

For many years, radiation-hardness in microelectronics has been achieved via specialized foundries and specific manufacturing processes. Due to the low demand for these types of devices, these processes have failed to scale at the same rate as commercial CMOS processes. Thus, the use of a hard-by-design methodology incorporating rad-hard techniques into commercial processes is necessary. Techniques such as enclosed layout (EL) and triple modular redundancy (TMR) can be used to achieve radiation-hardness in a traditional CMOS process. With this, the door is opened for the use of modern CMOS processes to achieve faster and more efficient circuits.

In addition to radiation-hardened electronics, optical links can be leveraged to achieve higher bandwidth, longer distance communications at lower losses than the equivalent electrical link. Since these channels typically display a strong low-pass characteristic, the losses become too large to maintain signal integrity at higher data rates. The losses of light through a fiber optic cable are dramatically lower than that of electrical cabling, and as such, light as a mode of transmission can generally support a much larger bandwidth. For this reason, the use of optical interconnects is highly attractive for critical applications requiring high-speed, low loss communications, such as spacecraft interconnects [2].

This thesis focuses on the development and testing of an optical transceiver intended to support inter-system wireline communications in an irradiated environment. An optical frontend consisting of a transmit vertical-cavity surface-emitting laser (VCSEL) and receive photodetector

(PD) operating over a multimode fiber is driven with rad-hard circuitry.

## **1.1 Organization**

In order to understand and support the conclusions drawn from the design of a radiation-hardened transceiver in this thesis, some theoretical background is necessary. Thus, Chapter 2 discusses the basics of high-speed optical links and the mechanisms and effects of ionizing radiation. The remaining chapters will present the design and testing of the radiation-hardened optical transceiver in a 180nm CMOS technology. The design process, challenges, and techniques used are discussed in Chapter 3 and experimental results are analyzed in Chapter 4. Finally, in Chapter 5, conclusions are drawn and experimental results are re-summarized.

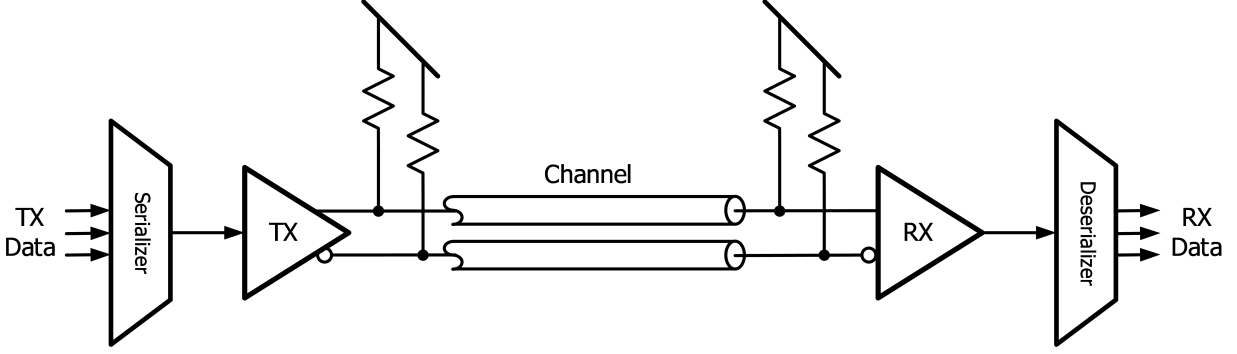
## 2. BACKGROUND

This chapter provides the necessary background to understand the radiation-hardened transceiver design. It begins with a description of the basic concept of high-speed links, continues with the application of optical links, and concludes with an overview of the effects and mechanisms of ionizing radiation.

### 2.1 High-Speed Links

High-speed links are used to transmit large amounts of data between two locations. A basic high-speed link is shown in Figure 1. In a typical system, many channels of data are serialized into a single high-speed stream. A transmitter (TX) takes this stream and drives a differential transmission line accordingly. Most often, a current-mode driver is used such that the TX driver steers some current swing through the terminations in the channel. The termination resistance values are typically equal to the characteristic impedance of the transmission line to reduce reflections as the signal reaches the front-ends. In the receiver (RX), the signal is amplified to output levels and equalization or compensation is applied as needed. The data stream is then deserialized into its original components. The most common type of data modulation used is non-return-to-zero (NRZ) signaling, which allows for one bit of data per symbol period. Other signaling types exist, but will not be covered in this thesis. Differential signaling is often used for its advantages in negating the common-mode noise present. In a standard differential data stream, one channel contains the complement of the nominal channel such that at any given time the sum of the two streams is equal to zero. The output signal is then obtained by subtracting one channel from the other. Thus, in the case where there is some noise present on the entire transmission line, or both channels, it is negated at the decision element when the single-ended signal is restored.





**Figure 1:** High-speed link system

### 2.1.1 Transmission Channels

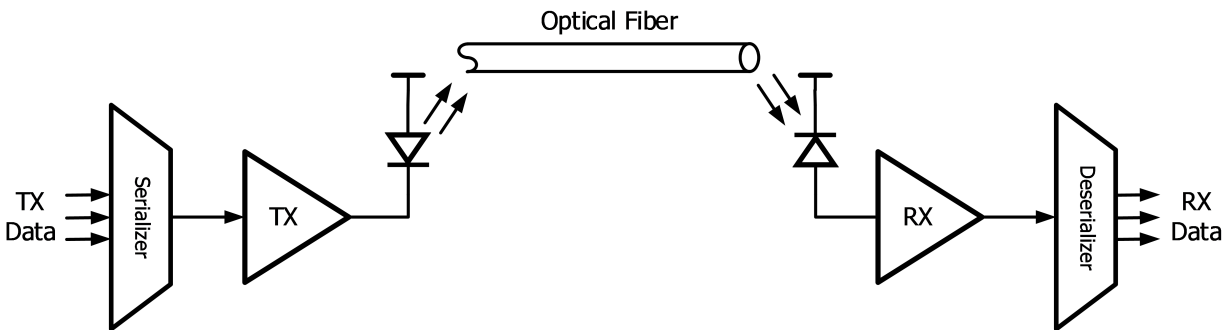
As important as the circuitry driving high-speed links is the transmission channels themselves. Links can be as short as a few centimeters, such as from chip-to-chip within a system, or as long as thousands of meters, such as between multiple systems in a server center. The material used for transmission varies based on distance to cover and speed of the data being transmitted. In general, materials supporting electromagnetic propagation experience a loss due to factors such as absorption, scattering, or dielectric losses. This loss can be expressed as below in Equation 1, where  $L$  is the distance of the transmission line and  $\alpha$  is the loss coefficient [3].

$$P_{out} = P_{in}e^{-\alpha L} \quad (1)$$

With electrical channels, the loss coefficient is directly proportional to the frequency of data propagating, thus creating a low pass characteristic. Fiber optic cables display a far lower frequency-dependent loss than electrical cabling and for this reason are far more advantageous for long distance transmission. For example, a standard single-mode fiber (SMF) such as SMF-28 displays losses as low as 0.32 dB/km at a wavelength of 1310nm [4], while supporting virtually limitless bandwidth. Because they are less prone to losses, fiber optic cables have the potential to transmit far more bandwidth than electrical transmission lines.

## 2.2 Optical Links

Optical links are slightly more complex than electrical links since the signal must be driven as an optical signal over a fiber. A typical optical link is shown below in Figure 2. The channel of transmission is a single-ended fiber which can be classified as "single-mode" or "multi-mode", referring to the behavior of the light waves as they travel down the fiber.



**Figure 2:** Typical optical link system

On the transmit side, the input electrical signal must be converted to light via some method of modulation. The TX circuitry typically consists of various stages of buffering and a current driver for the output optical device. Commonly used devices include lasers or light emitting diodes (LEDs). For transmission over a fiber, the use of a laser is most advantageous for its high focus and power. Particularly, the use a vertical-cavity surface-emitting laser (VCSEL) is attractive for its large availability and ease of manufacturing [5].

On the receive side, the optical signal from the fiber must be converted back to the electrical domain and amplified to the appropriate output voltage swing. To accomplish this, a transimpedance amplifier is employed to amplify the current swing into a voltage swing, followed by various stages of post-amplification and buffering. To receive the optical signal, devices such as a p-i-n photo-detector (PD) can be used. In general, the optical devices described require a single-ended current-mode signal in contrast to the typical low-voltage differential signaling (LVDS) that

is used in the electrical domain. For this reason, it is important to design transceiver circuitry specifically suited to these applications. Chapter 3 will describe in detail the design considerations needed for this type of system.

## 2.3 Radiation Effects

Operation of microelectronic devices in locations such as outer space has the potential to be disrupted by ionizing radiation. Particularly, the impacts of particles such as cosmic rays, heavy ions, and protons must be considered. The two primary radiation impacts on microelectronics are the total ionizing dose (TID) and single event effects (SEEs).

### 2.3.1 Total Ionizing Dose (TID)

TID is defined as the total radiation dose received over some length of time. In a CMOS process, large doses of radiation have the potential to disrupt circuit performance through a few different mechanisms. Particularly, particle strikes in the gate oxide of a transistor are most impactful. When a particle collides with a solid, such as the  $SiO_2$  in the gate, a number of electron-hole pairs are created as the particle passes through. After the charges recombine, a number of holes are left over. These holes drift to the interface between the gate and the silicon and become entrapped. Due to this increase of positive charge in the oxide, the threshold voltage is shifted according to Equation 2, where  $C_{ox}$  is the oxide capacitance,  $t_{ox}$  is the oxide thickness, and  $\rho(x)$  is the additional charge density. [6, 7]

$$\Delta V_T = \frac{-1}{C_{ox}t_{ox}} \int_0^{t_{ox}} x\rho(x)dx \quad (2)$$

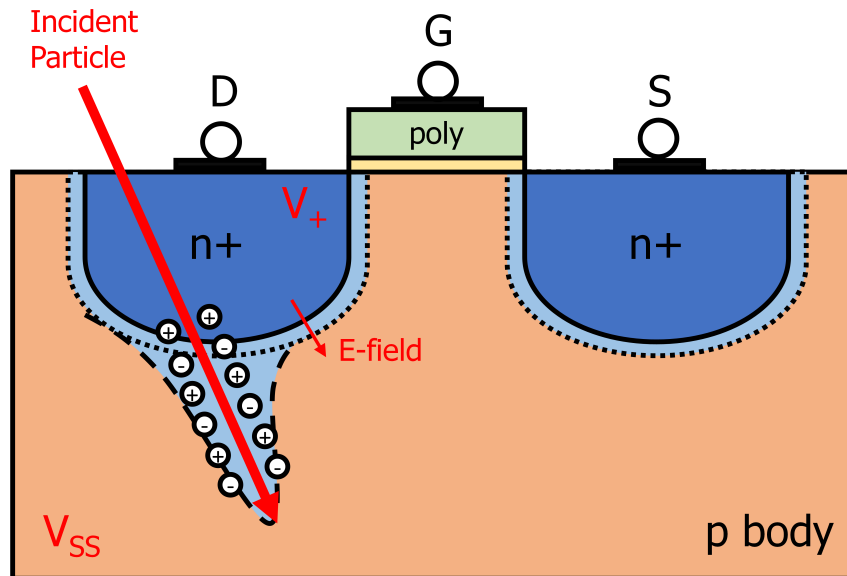
The shift in an intrinsic parameter such as the threshold voltage can easily become a problem in sensitive analog circuits where bias points are set precisely. As the oxide thickness decreases, such as in more modern processes, this effect is amplified due to the larger charge density.

Another impact of TID is radiation-induced edge leakage. Similar to the gate oxide, the field oxide, which is typically used to separate transistors, can accumulate trapped charges. These trapped charges in practice can form "edge transistors", which with enough trapped charges begin to conduct current through the channel of the device. This causes an unwanted leakage current

through the transistor that persists when there is no voltage applied to the gate and the device is off. Given a large enough dose of radiation, this leakage can reach into the range of nano-amperes, severely affecting device bias points and altering the I-V characteristics of the device.

### 2.3.2 Single Event Effects (SEEs)

In addition to the more analog impacts of the total ionizing dose, effects on digital elements also occur due to ionizing radiation. Single event upsets (SEUs) occur when a single highly energized particle strikes a digital storage element such as a flip-flop or latch, causing a bit switch. When the particle impacts the diffusion region, a trail of electron hole pairs are created as the particle passes through the silicon (Figure 3). With enough incident energy, the collection of charges on the end of the tail can cause a net flow of current between the depletion region and the substrate connection, creating a voltage transient with the potential to cause data corruption.

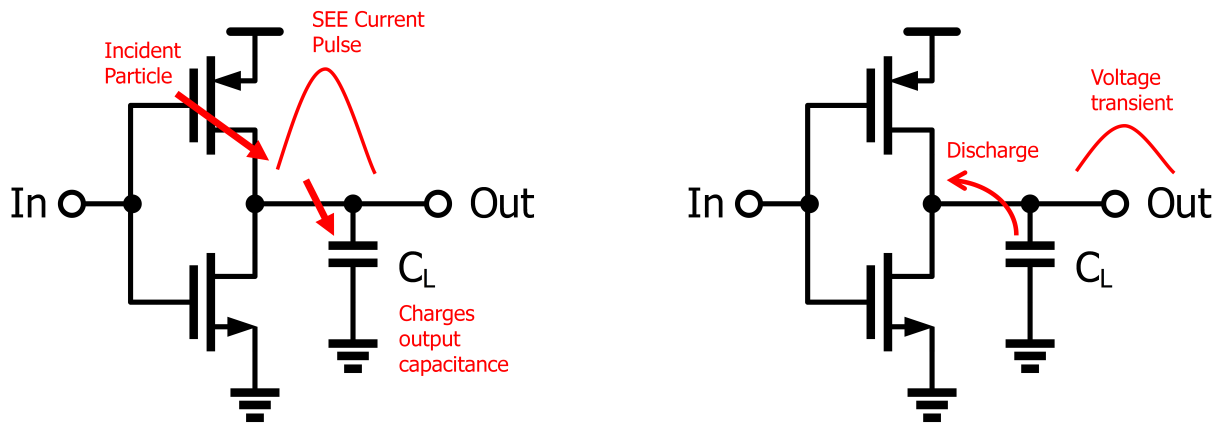


**Figure 3:** Single event upset (SEU) mechanism

To understand this effect further, let us consider its impact on a CMOS inverter (Figure 4). Suppose a particle strikes the drain node of the PMOS device with sufficient energy to induce a

current pulse from the n-well to the p+ diffusion of the transistor. This current pulse is passed to the output node, which charges the output capacitance (typically the gate capacitance of the next stage). When the inverter is switched and the NMOS device reaches saturation, the output capacitance discharges and creates a voltage transient. Clearly, this transient has the potential to cause corruption of the data, in the worst case causing a bit error as the voltage is sampled.

For latched devices such as an SRAM cell or flip-flop, when an SEU occurs and a voltage transient with enough energy is generated, this change can propagate to the complementary element, overwriting its value and causing a complete bit flip. In a typical environment, the particle strikes do not have enough energy to propagate across the cell, but in a harsh environment such as space, the energies are high enough to cause bit flips and must be mitigated.



**Figure 4:** CMOS inverter SEU effect

Similarly, if a particle strike occurs through the boundary between the n-well and p-substrate and a large enough transient is generated, single event latch-up (SEL) becomes possible by introducing a low-impedance path between the supply ties. In cases where latch-up occurs, a power cycle of the device is required, and in some cases the device can be permanently damaged.

### 3. OPTICAL TRANSCEIVER DESIGN

In this chapter, the design considerations for the radiation-hardened optical transceiver will be discussed. Important factors to support optical I/O will be weighed, particularly utilizing a p-i-n photodetector on the receive side and a vertical-cavity surface-emitting laser (VCSEL) on the transmit side. The design and requirements will be discussed for both a Gen 1 prototype chip which has been fabricated and tested, and a Gen 2 chip which is in development.

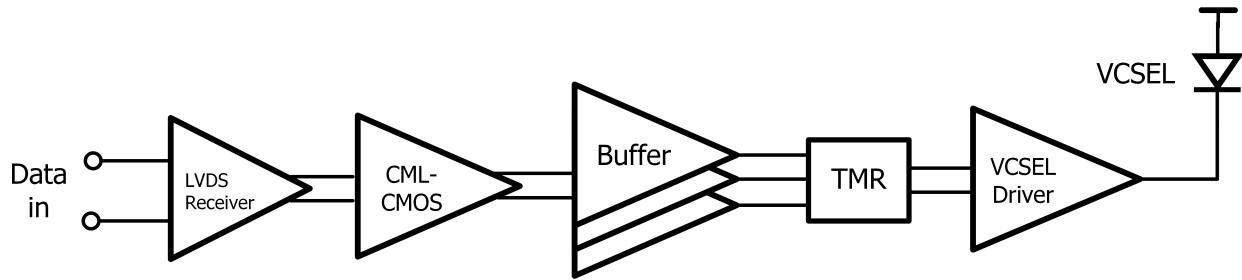
#### 3.1 Optical Transmitter Design

The optical transmitter must receive the voltage signal from the input LVDS interface, buffer the signal, and drive the VCSEL with a current-mode logic (CML) signal. The desired specifications for the transmitter are outlined in Table 1. The desired output current range is similar for both generations, but its center value will vary based on the VCSEL's LIV behavior. Additionally, a different topology will be used in the second generation transmitter to support more straightforward radiation testing.

**Table 1:** Optical transmitter specifications

<b>Specification</b>	<b>Gen 1</b>	<b>Gen 2</b>
Modulation Current	0-10 mA	0-10 mA
Bias Current	0-10 mA	0-10 mA

The topology of the second generation optical receiver is shown below in Figure 5. The input data is passed through an LVDS receiver, converted from current-mode logic to a full-swing CMOS signal to then be passed through a series of inverter-based buffers including TMR for radiation protection. Finally, the voltage signal is driven as a current through the VCSEL to be transmitted.



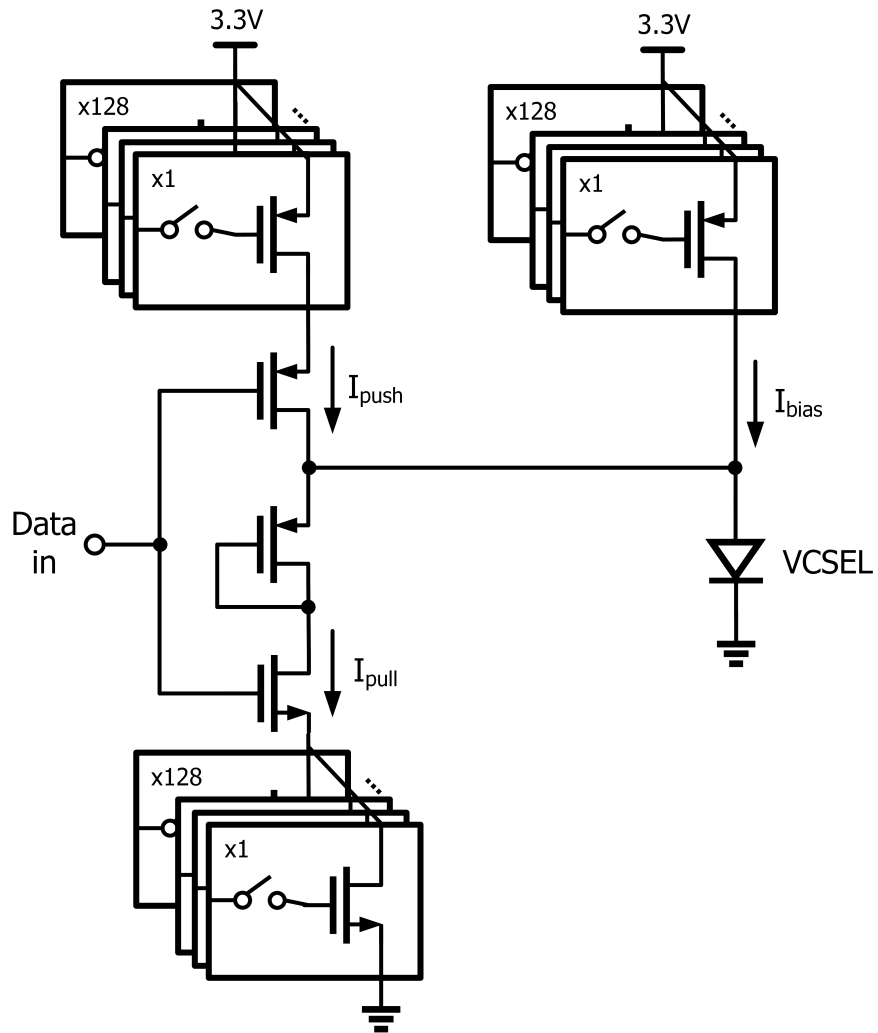
**Figure 5:** Optical transmitter block diagram

### 3.1.1 VCSEL Driver Design

Perhaps the most crucial block of the TX architecture is the VCSEL driver. This stage modulates the signal as an output current, and must do so within a swing that corresponds to a relatively linear optical current swing. This operating point is determined specifically by the behavior and characteristics of one specific VCSEL, and thus must be designed with a certain model in mind. Parasitics such as the series resistance, bond wire inductance, and pad capacitances must also be considered when designing this stage. Two common VCSEL driver designs are the push-pull driver [8, 9, 10] and the common-anode driver [11].

#### 3.1.1.1 Push-Pull Driver

In the push-pull driver topology (Figure 6), two complementary sets of modulation current mirrors provide a digitally-controlled "push" and "pull" current which is directed through the VCSEL load via a inverter structure, driven by the full CMOS-level swing signal. A diode-connected PMOS device in the driver protects against any back-flow of current. The bias current of the VCSEL is driven separately by another set of digitally-controlled current mirrors. This topology is advantageous for its ease of control and simplicity, but can suffer some nonidealities post tape-out such as mismatch between the push and pull current mirror sets. Imbalances like these can cause higher bit error rates and DC mismatches in the transmitter and overall system.

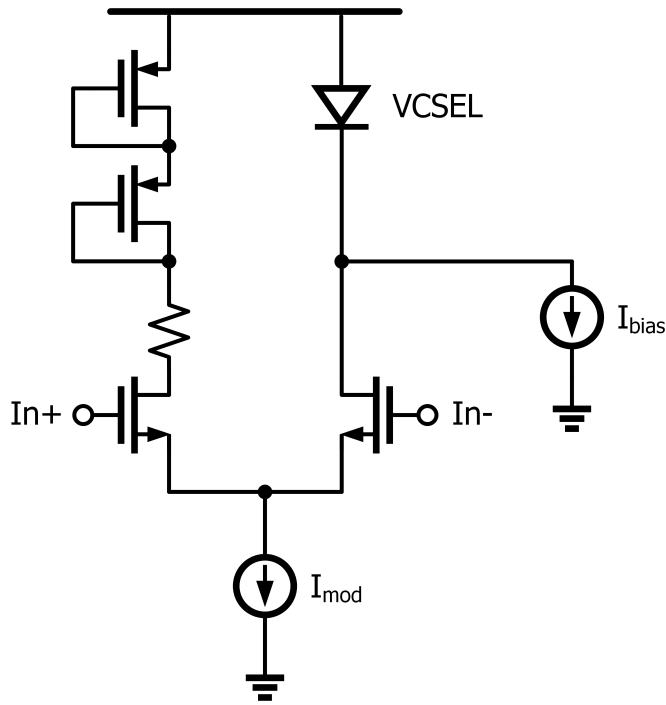


**Figure 6:** Push-pull VCSEL driver with digitally controlled current mirrors

### 3.1.1.2 Common-Anode Driver

In the common-anode VCSEL driver (Figure 7), the modulation current is implemented as a digitally-controlled tail current source that is steered through the left and right branches of the circuit. The left branch includes a dummy load consisting of diode-connected PMOS devices and a resistor to match the characteristics of the VCSEL. The right branch drives the output VCSEL, also including another digitally-controlled bias current mirror to allow for DC adjustments to support optimal operating conditions.





**Figure 7:** Common-anode VCSEL driver

### 3.2 Optical Receiver Design

The chip's optical receiver is tasked with receiving the input current from the PD, amplifying and equalizing the signal to the appropriate voltage swing, and driving an output LVDS line with the appropriate termination to eliminate reflections. The front-end must accomplish these tasks while remaining low-noise and sensitive to small input amplitudes. Additionally, the characterization of the optical receiver as burst-mode requires some additional design considerations.

Burst-mode refers to the receiver's ability to operate on "bursts" of data rather than a continuous stream, where the distance between data bursts can range from a few milliseconds to multiple years. The usage of this type of receiver means there cannot be low-frequency attenuation, that is, there cannot be a low-frequency zero in the front-end's frequency response. This effect limits the method of DC cancellation that can be used.

The desired specifications for the receiver are outlined in Table 2. For the first generation design, the bandwidth is relatively low, but as a result the receiver produces a larger gain and has

a greater noise tolerance. Additionally, due to the lower data rate, a higher PD capacitance can be tolerated. For the second generation receiver, higher bandwidth has been prioritized and thus other specifications have been relaxed. Most notably, the PD capacitance has been lowered to represent a chip-style device rather than connectorized. This change is necessary in order to meet the desired bandwidth specification.

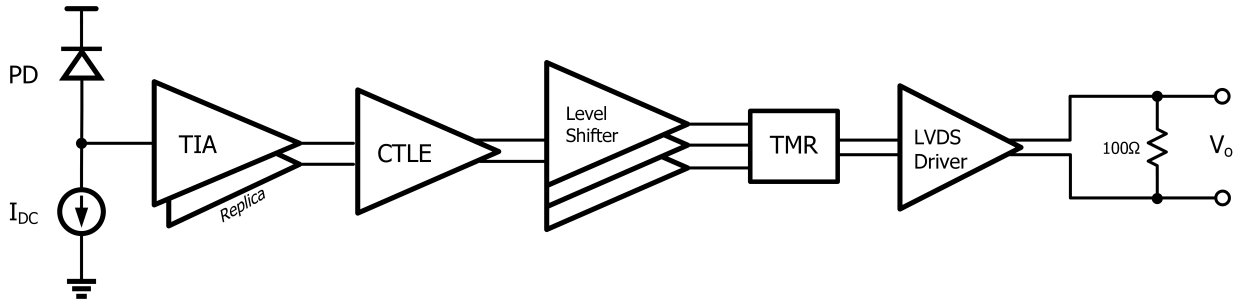
**Table 2:** Optical receiver specifications

<b>Specification</b>	<b>Gen 1</b>	<b>Gen 2</b>
Gain	70 dB	60 dB
Bandwidth	1 GHz	4 GHz
Noise Sensitivity	-16 dBm	-12 dBm
PD Capacitance	1.5 pF	0.12 pF

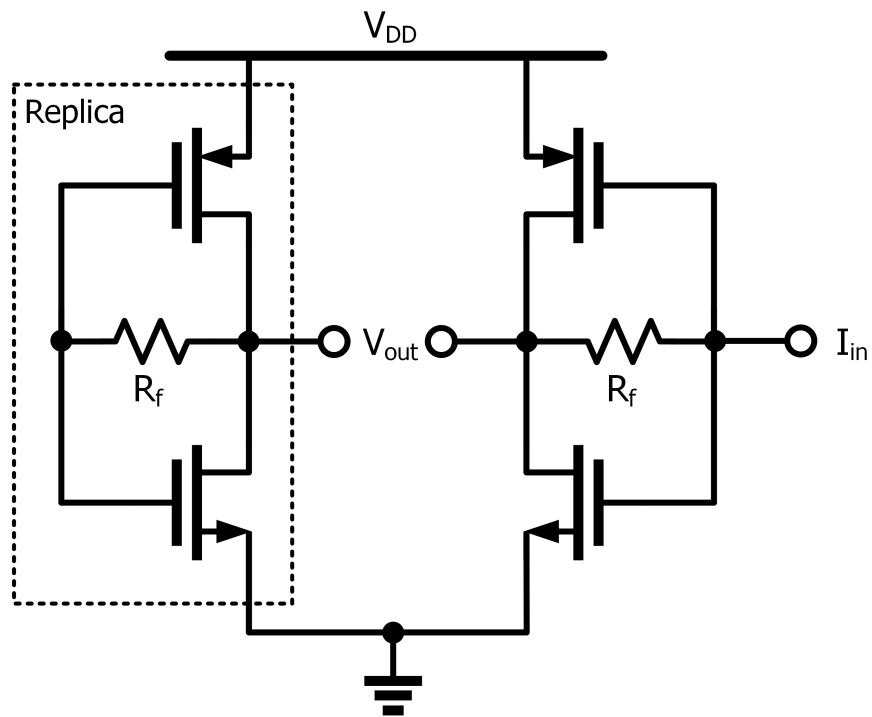
The topology of the second generation optical receiver is shown below in Figure 8. The input current from the PD is first passed through the TIA to be amplified and converted to a voltage swing. The DC component of the PD current is removed using digital compensation to ensure the proper common-mode voltage is present. Next, equalization and some post-amplification is performed using CTLE. The signal is then level shifted to the appropriate value, including TMR for radiation resiliency. Finally, the signal is driven as an LVDS signal over the appropriate  $100\Omega$  termination. In the below sections, the design of the RX frontend, consisting of the initial amplification and equalization, is discussed.

### *3.2.1 Transimpedance Amplifier Design*

The transimpedance amplifier is the most critical stage of the frontend, as it provides a majority of the gain and is often a limiting factor on the receiver's bandwidth. Several designs exist such as the shunt-feedback inverter TIA (Figure 9), which is attractive particularly for its low-noise performance. In this topology, the closed loop transimpedance gain can be found as



**Figure 8:** Optical receiver block diagram



**Figure 9:** Shunt-feedback inverter TIA

$$R_T = \frac{A}{A+1} * R_f \quad (3)$$

where  $A$  is the open loop gain of the inverter [12]. From this, it is clear that assuming  $A$  to be much larger than unity, the gain is approximately equal to the feedback resistor  $R_f$ . Similarly, the 3-dB bandwidth can be found as

$$BW_{TIA} = \frac{A + 1}{2\pi R_f C_T} \quad (4)$$

where  $C_T$  is the total input capacitance. Because of the  $A + 1$  factor present, the shunt-feedback topology has the advantage of higher bandwidth, while still retaining low-noise benefits from a larger feedback resistor. The input-referred noise current is approximately equal to its largest component, the thermal noise of the resistor:

$$I_{n,TIA}^2 = \frac{4kT}{R_f} \quad (5)$$

One final consideration placing an upper bound on  $R_f$  is known as the transimpedance limit [13, 14]. As bandwidth increases, a first-order model is no longer sufficient to characterize the TIA, as the cutoff frequency of the core amplifier must be considered. With this second-order behavior, the maximum value of  $R_f$  is limited to have adequate phase margin for stability according to

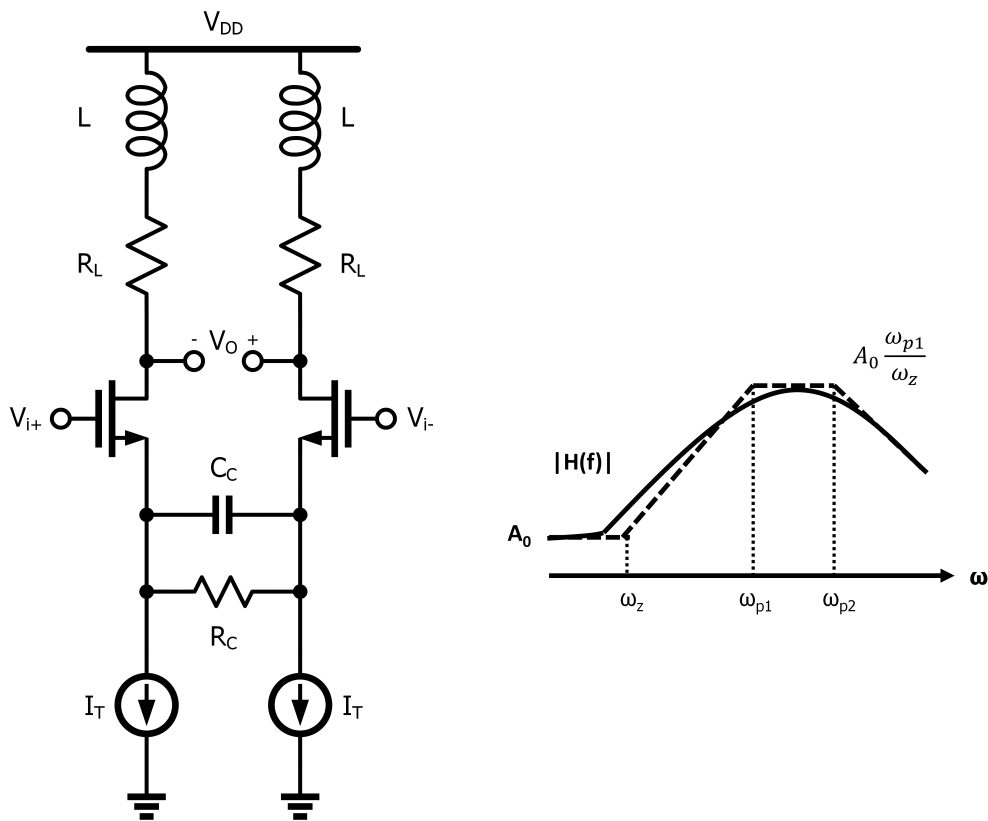
$$R_f \leq \frac{Af_0}{2\pi C_T BW^2} \quad (6)$$

where  $f_0$  is the bandwidth of the core amplifier. From this, it is clear that the transimpedance is limited by the gain-bandwidth of the core TIA and the input capacitance, which includes the photodetector, gate capacitances, and any chip pad parasitics. Further, since  $f_0$  is a process parameter, the maximum achievable transimpedance trades with the square of its bandwidth. To get around this limitation, especially when working close to the  $f_T$  of a process, it is necessary to employ equalization in order to achieve desirable gain and high bandwidth, while still retaining the low-noise characteristic of the shunt-feedback TIA [15].

### 3.2.2 Equalization

In general, equalization involves the modification of a system's frequency response by applying a filter to the signal. To extend the bandwidth and counteract a strong low-pass behavior, techniques such as continuous time linear equalization (CTLE) can be applied. CTLE extends a

system's bandwidth by reducing the DC gain and applying peaking at a selected point, typically the Nyquist frequency of the desired data rate. In order to retain as much DC gain as possible, an active topology can be utilized to apply positive boosting. The schematic and response of a typical active CTLE circuit is shown below in Figure 10. The degeneration resistor and capacitor can be controlled via a tunable resistor and capacitor DACs to allow for flexibility of compensation post tape-out [16].



**Figure 10:** Active CTLE circuit and frequency response

In this active topology, boosting is accomplished via a degenerated differential pair, implementing a real zero through  $C_S$  as

$$|\omega_z| = \frac{1}{R_S C_S} \quad (7)$$

and two poles

$$|\omega_{p1}| = \frac{1}{R_D C_P} \quad |\omega_{p2}| = \frac{1 + g_m R_S / 2}{R_S C_S} \quad (8)$$

Some key design parameters include the DC gain,  $A_0$ , the boost-factor  $\omega_{p1}/\omega_z$ , and the maximum bandwidth,  $\omega_{p2}$ . The product of the boost-factor and the maximum peaking represents how much compensation is applied and how quickly it is applied. For systems with a strong low pass characteristic the roll-off can be as high as 30-40dB/decade, creating a limitation on the total equalization that can reasonably be applied to the system.

As such, a process-dependent limitation can be derived using the product of the gain, boost-factor, and bandwidth [17]

$$A_0 \frac{\omega_{p1}}{\omega_z} \omega_{p2} \simeq \frac{g_m}{C_P} \quad (9)$$

where  $C_P$  represents the parasitic capacitance in the drain node, or most commonly, the gate capacitance of the next stage and  $g_m$  is the transconductance of the NMOS devices. In systems where post-amplification is applied after equalization, this causes the maximum bandwidth to become limited by the overall gain-bandwidth product of the front-end. Due to the  $f_T$  of a process, there is a maximum equalization that can be achieved while retaining sufficient gain.

One more consideration in the design of active CTLE arises when implementing the tail current sources. Though larger device currents are attractive for their resulting increased transconductance and decreased output resistance, the parasitics associated with large current mirroring devices becomes non-negligible, especially when sensitive tuning is applied to move  $\omega_z$  to a relatively high frequency. Because of this non-ideality, as the amount of peaking increases, the maximum achievable  $\omega_z$  decreases.

Additional peaking gain can be achieved at a reasonable power efficiency by including shunt-peaking inductors [18]. By placing inductors in series with a load, the output capacitance is "shunted" and a zero created in the frequency response. From a transient point of view, the inductor

delays the current flow to the resistive branch, allowing more current to initially charge the output capacitance, thus reducing the rise time. While this technique is extremely useful for extending system bandwidth, over-equalization is possible, causing group delay, ringing, and overshoot in the transient response that can cause errors and degrade the signal.

### 3.2.3 DC Cancellation

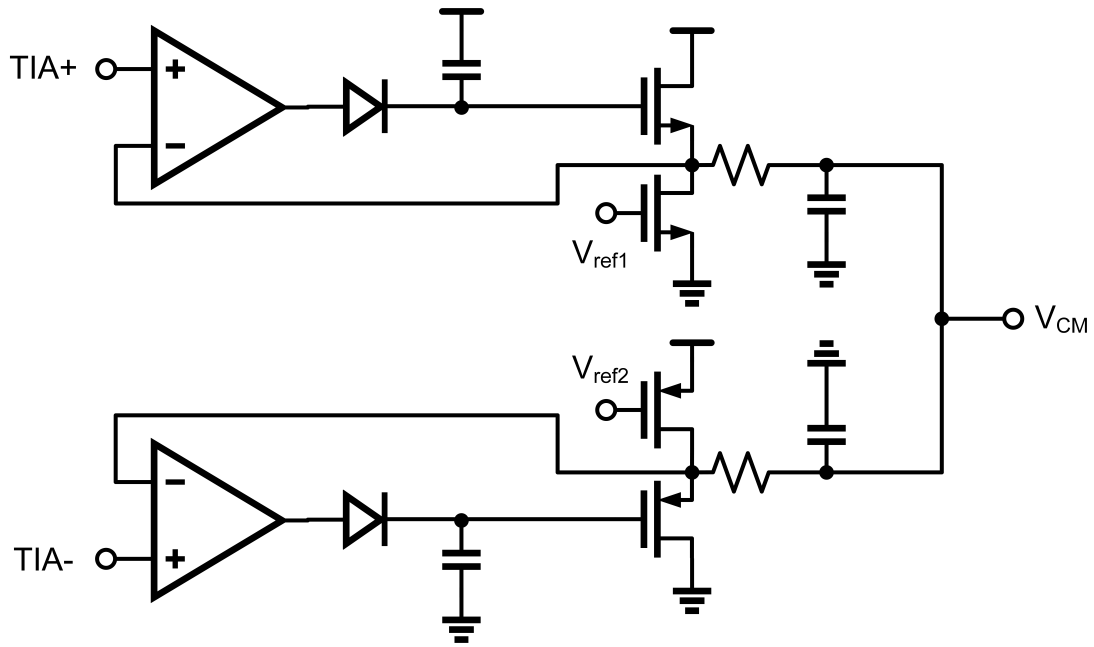
In optical receiver frontends, the variable DC current produced by the photodetector must be negated to properly set the common-mode of the amplifier stages. Specifically, for burst-mode devices, the typical feedback-controlled cancellation method [19, 20] is not acceptable as it would introduce low-frequency attenuation that would interfere with burst-mode behavior.

Previous burst-mode receivers have used a system based on automatic offset control (Figure 11), consisting of top and bottom hold circuits to detect the signal high and low levels, and averaging resistors to acquire the common-mode value [21, 22]. For lower data rates, this method is acceptable, however, when designed for higher frequency operation, the level-hold's RC time constant can introduce a large error in the common-mode signal according to

$$\Delta V_{CM} = e^{-T/\tau} \quad (10)$$

where  $T$  is the period of the signal and  $\tau = R_P C_h$  is the level-hold time constant, consisting of the diode resistance and hold capacitance. For high data rates, a small time constant is necessary to eliminate this error. If not considered, a large error in the common mode reference can cause reduced sensitivity and high bit error rates in the receiver.

A different approach to high data rate DC cancellation is that of a digital control scheme [23]. In this approach, the DC level of the signal is sampled, and using a binary-search algorithm, the optimal DC cancellation current is set through a variable-gain current mirror network at the input.



**Figure 11:** Auto offset control circuit

### 3.3 Radiation Hardening

To achieve radiation hardness to both the total ionizing dose (TID) and single event effects (SEEs) a few design techniques were adopted in the transceiver. A summary of the radiation hardening is included below in Table 3. Each technique is discussed in detail in the below section.

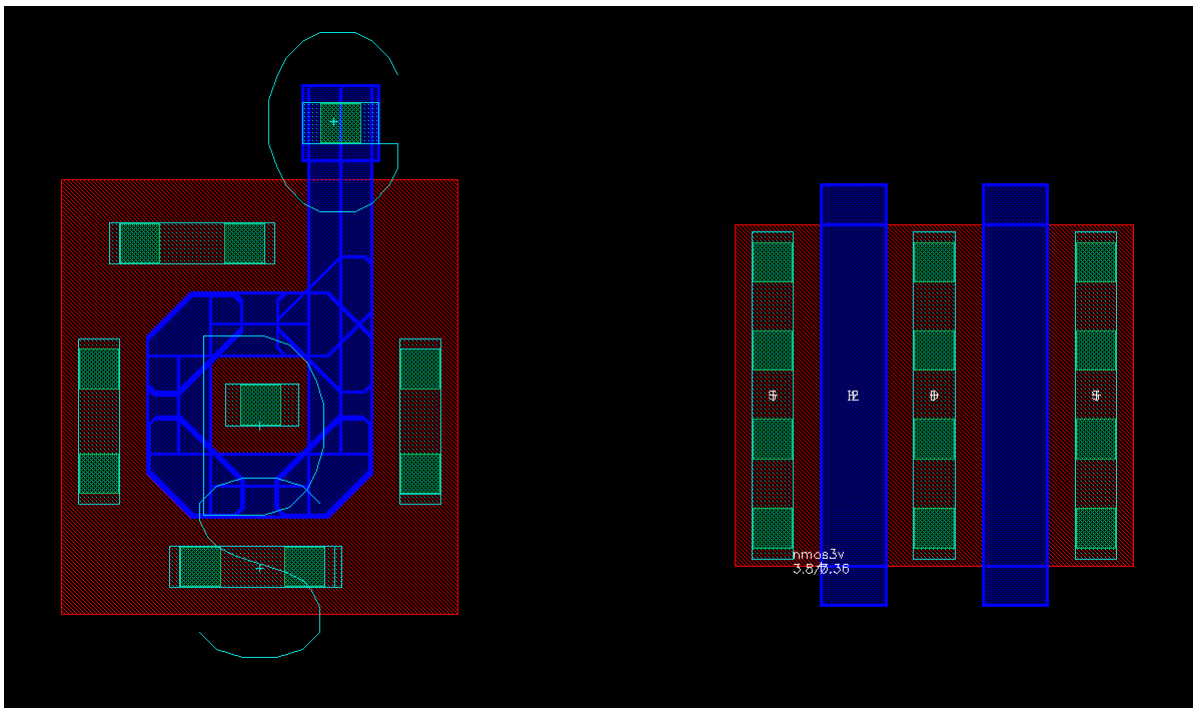
**Table 3:** Transceiver Radiation Hardening

Block	Rad-Hard	Non Rad-Hard
Scan Chain	TMR	None
RX/TX Data Path	TMR	None
Band Gap Reference	EL	None
VCSEL Driver	EL	None



### 3.3.1 Enclosed Layout

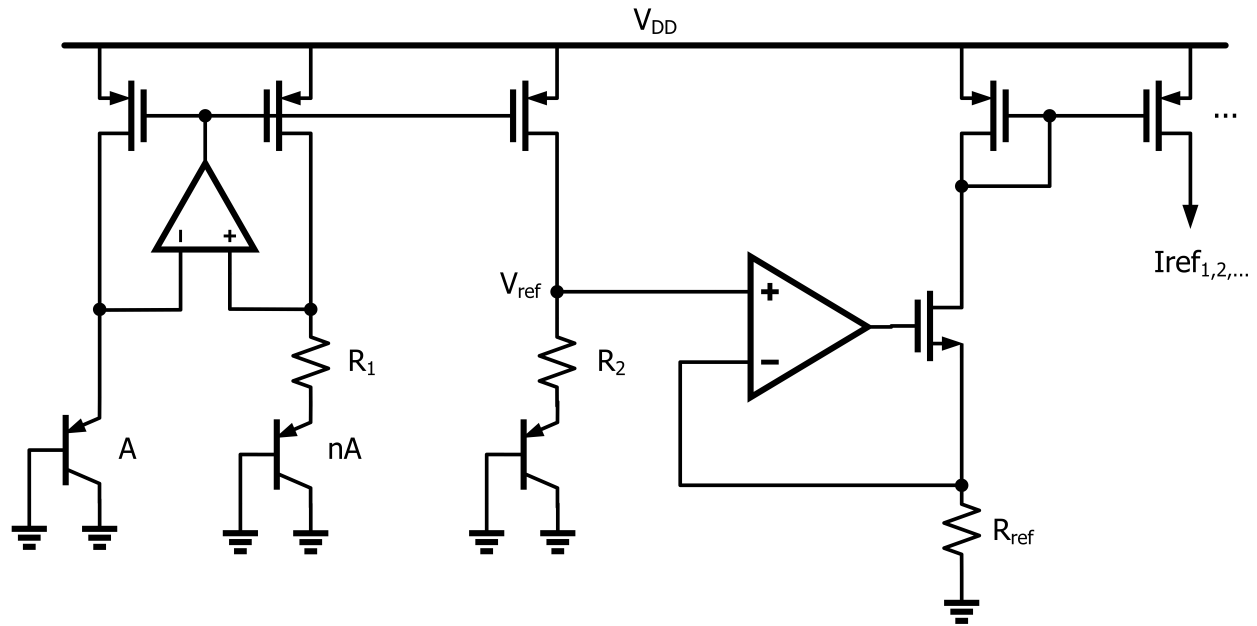
To control against TID effects and prevent both edge leakage and device isolation problems, an enclosed layout technique was used as shown in Figure 12. By surrounding the drain completely, the leakage path at the edge of the diffusion and substrate is eliminated. Particularly, this technique was implemented in the TX VCSEL driver. It is crucial to eliminate the potential for leakage current in this stage, as the driver relies on the ability to completely turn off a set of transistors to steer the current. Any leakage will cause modulation errors and variation in the set bias current. Additionally, due to the large area of the output driver transistors, the potential for greater leakage is possible.



**Figure 12:** Enclosed layout transistor (left) and equivalent standard transistor (right)

### 3.3.2 Band Gap Reference

Band gap references have been used for many years in the design of analog circuits to provide stable voltage and current references for use throughout a given design. The purpose of a band gap reference is to produce a voltage or current reference independent of any supply voltage or temperature variations. Typically, to produce a temperature-independent reference, the voltage difference between two p-n junctions of different sizing are used to generate a proportional to absolute temperature (PTAT) current. Next, A PTAT voltage is generated by passing this current through a fixed resistor and adding the base-emitter voltage of a third diode-connected device [24]. From here, a baseline reference current can be generated using an output stage and an external precision resistor (Figure 13).



**Figure 13:** Band gap reference circuit

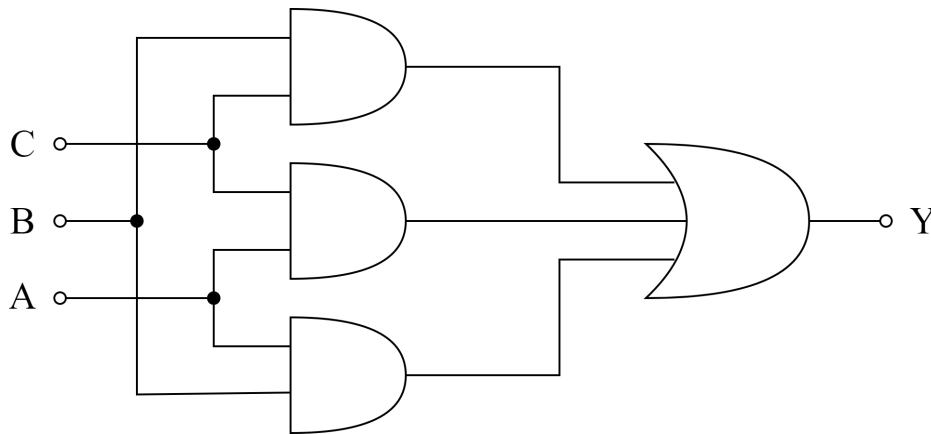
In this topology, the band gap reference voltage,  $V_{ref}$  can thus be found as

$$V_{ref} = |V_{BE}| \frac{R_2}{R_1} V_T \ln n \quad (11)$$

where  $V_{BE}$  is the voltage over the output p-n junction and  $V_T$  is the thermal voltage. From here, the reference voltage is used to drive an op-amp generating an output current via a precision resistor. The generated current can then be mirrored as needed to provide the desired references across the chip.

In an irradiated environment, this approach to reference generation is not successful due to the TID impacts on the p-n junctions used. Thus, the above circuit can be modified in order to create a radiation-hard band gap reference. By incorporating enclosed layout and surrounding the band gap diodes' p+ diffusion with thin oxide, rather than the traditional field oxide, the effects of the TID are avoided [25]. By using this approach, the current and voltage references for key circuit blocks are able to remain stable over radiation dose as well as temperature and process variation. This is imperative to ensure the accuracy of precise references, and thus correct biasing and successful transceiver operation.

### 3.3.3 Triple Modular Redundancy



**Figure 14:** Triple modular redundancy (TMR) logic implementation

Finally, to prevent SEUs in digital elements of the circuit such as inverter buffers and level shifters, triple modular redundancy (TMR) is adopted [26]. TMR involves creating three copies of the data path circuitry to be protected and implementing a majority voting system such that the

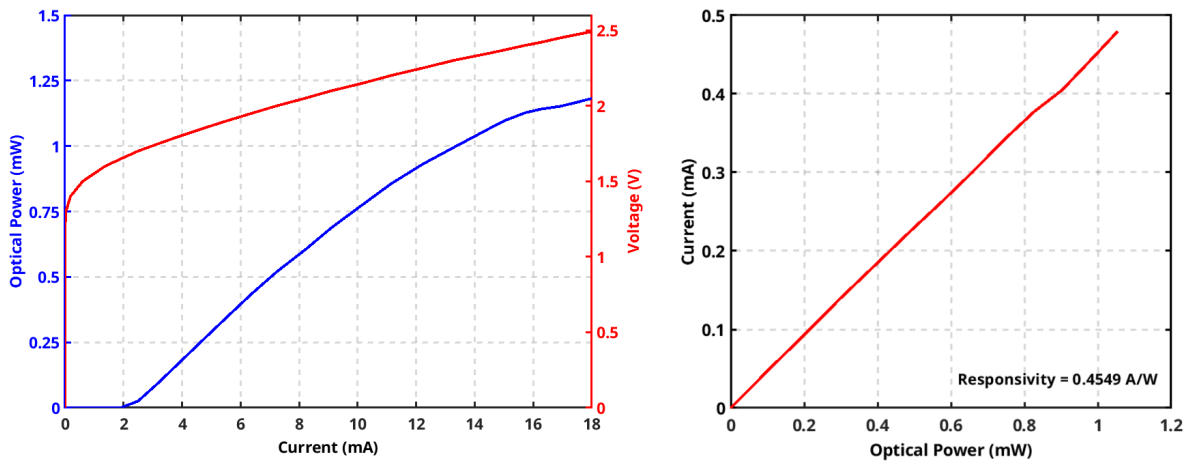
non-corrupted output is always selected when a single upset occurs. The technique is implemented on a gate level as shown below in Figure 14 where A, B, and C are the outputs from the duplicated circuitry and Y is the TMR protected output. The principle of TMR relies on the fact that for a given block, a SEU is extremely unlikely to occur on multiple copies of the circuit at exactly the same moment in time. For this reason, TMR is highly efficient at eliminating SEUs under a reasonable amount of radiation, such as what would be present in outer space.

## 4. RESULTS

In this chapter, the experimental results of the first generation transceiver are summarized. The transceiver was tested both electrically and under radiation to verify both baseline operation and its hardness to radiation. The simulated results for the second generation transceiver are also included. Post-layout parasitics are considered in the analysis.

### 4.1 Gen 1 Experimental Results

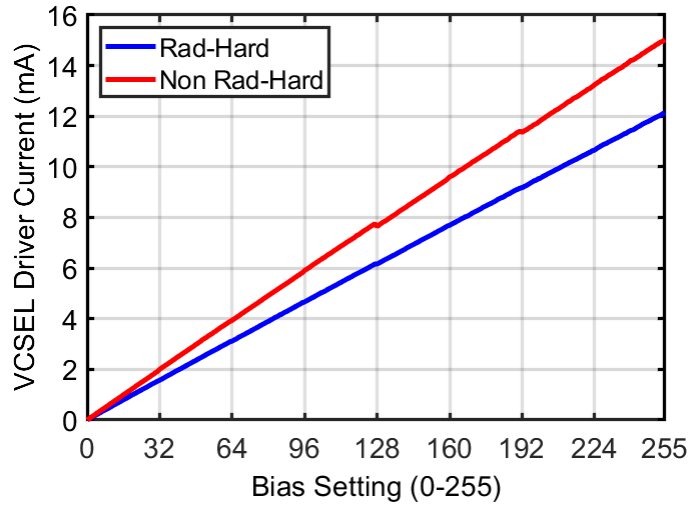
To begin, the connectorized VCSEL (Lasermate TLC-P85A4x6-4) and PD (Lasermate RLC-P85A306) were characterized for the operating conditions of transceiver (Figure 15).



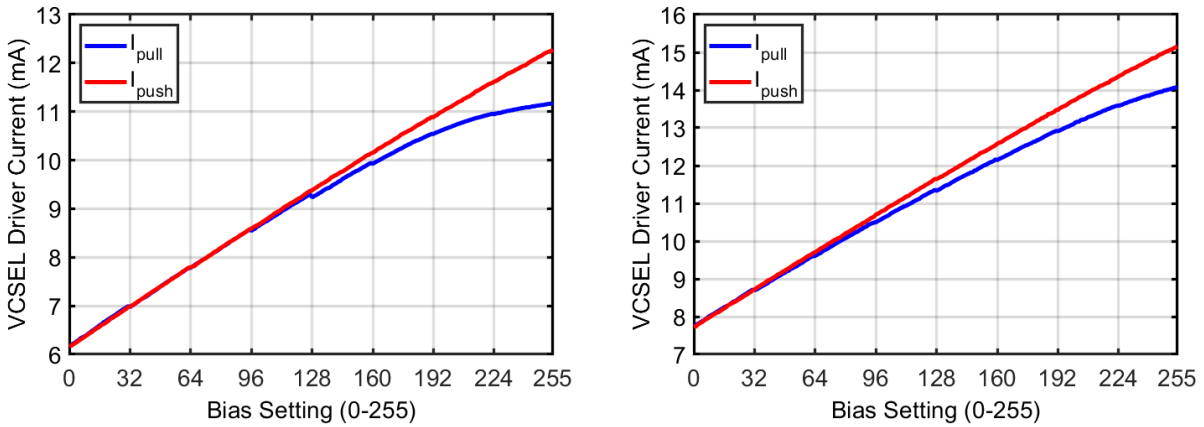
**Figure 15:** VCSEL L-I-V curve (left) and PD responsivity curve (right)

The TX VCSEL driver behavior was characterized over its digital control, for both the radiation-hard and non-hardened versions of the chip. Both the bias and modulation (push and pull) DACs were characterized (Figures 16, 17).

The transceiver measurement setup is shown in Figure 18. The optical transceiver operates over an 850nm multimode fiber. A FPGA is used to generate a 7-bit pseudo-random bit sequence



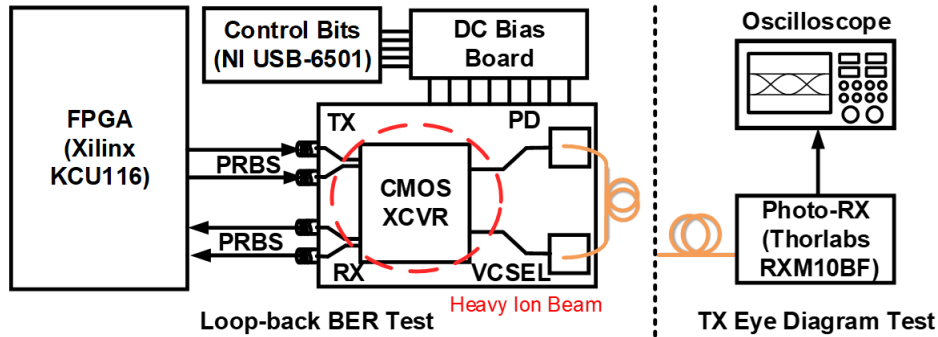
**Figure 16:** VCSEL driver bias current vs. digital control



**Figure 17:** VCSEL driver modulation current vs. digital control; rad-hard (left) and non rad-hard (right)

(PRBS7) to test the system bit-error rate (BER). Controlling bits and the chip DC bias are sent to the transceiver through a DC bias board. To perform a BER test, the optical transceiver is set in a loop-back configuration by connecting the optical fiber between the VCSEL and PD. The TX eye diagram is measured by connecting the output of the VCSEL to a commercial photo receiver (Thorlabs RXM10BF), which is then connected to the oscilloscope.

TID testing was performed at the Texas A&M NESC. To understand what impact TID had



**Figure 18:** Transceiver BER and eye diagram test setup

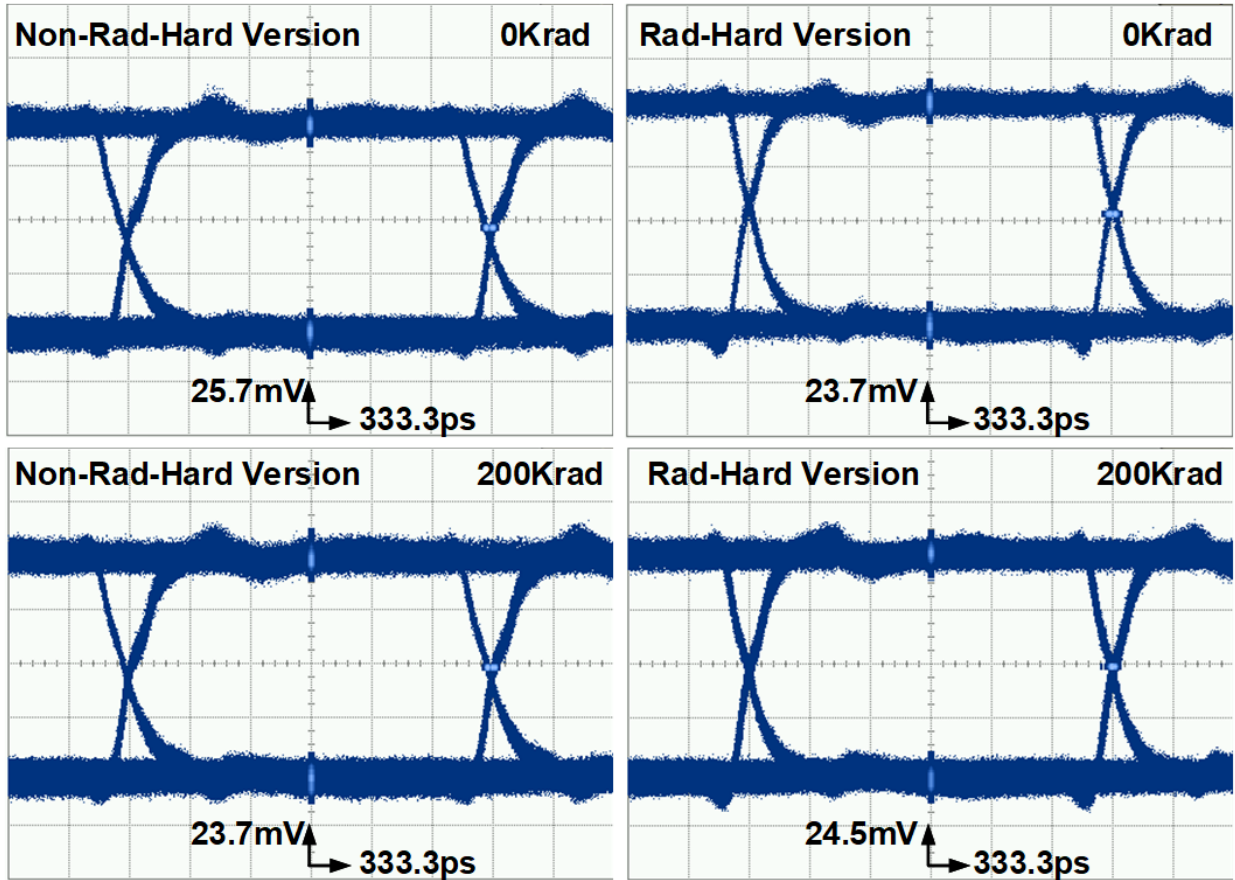
on the transceiver circuits, the chips were first characterized with a given PD and VCSEL. To avoid degradation that would interfere with the test results, these VCSELs and PDs were replaced with dummy loads during the TID irradiation. After irradiation, the original VCSEL and PD were placed back on the board to perform post-irradiation characterization. Both the radiation-hardened version and non radiation-hardened designs were irradiated with up to a dose of 200krad at a dose rate of 50krad/hour. During irradiation, the chips were powered up to a nominal operating condition, however, no electrical stimuli was provided at the inputs.

After irradiating both versions of the chip, eye diagrams at 0.5Gbps and 2Gbps (Figures 19, 20) were measured to quantify the TID induced degradation in the TX. At a data rate of 0.5Gbps, there was no significant difference between the rad-hard and non rad-hard TX versions, however, at a data rate of 2Gbps, the total jitter of the non rad-hard version increased 42% while the rad-hard version only increased 5.7%. A more detailed breakdown of the performance is summarized in Table 4. While the radiation hardening used in the TX does incur some initial penalty, after irradiation, the rad-hard version is far superior to the unhardened version, especially at higher data rates.

The sensitivity of the RX was also measured to characterize the TID's effect on it. As shown in Figure 21, the radiation-hardened RX sensitivity was -4.5 dBm and the non-radiation-hardened sensitivity was -5.8 dBm for at a BER of  $10^{-12}$ . This result is not conclusive, and more testing will need to be done to reach a reasonable conclusion. Factors such as board-to-board variation can

**Table 4: TX TID Performance Summary**

Irradiation (Rads)	Non Rad-Hard		Rad-Hard	
	0k	200k	0k	200k
TJ (ps) @ 0.5 Gbps	124.4	123	137.0	112.5
TJ (ps) @ 2 Gbps	168.6	239.8	191.6	202.5
Q-factor @ 0.5 Gbps	33	32	29	30
Q-factor @ 2 Gbps	32	30	28	30

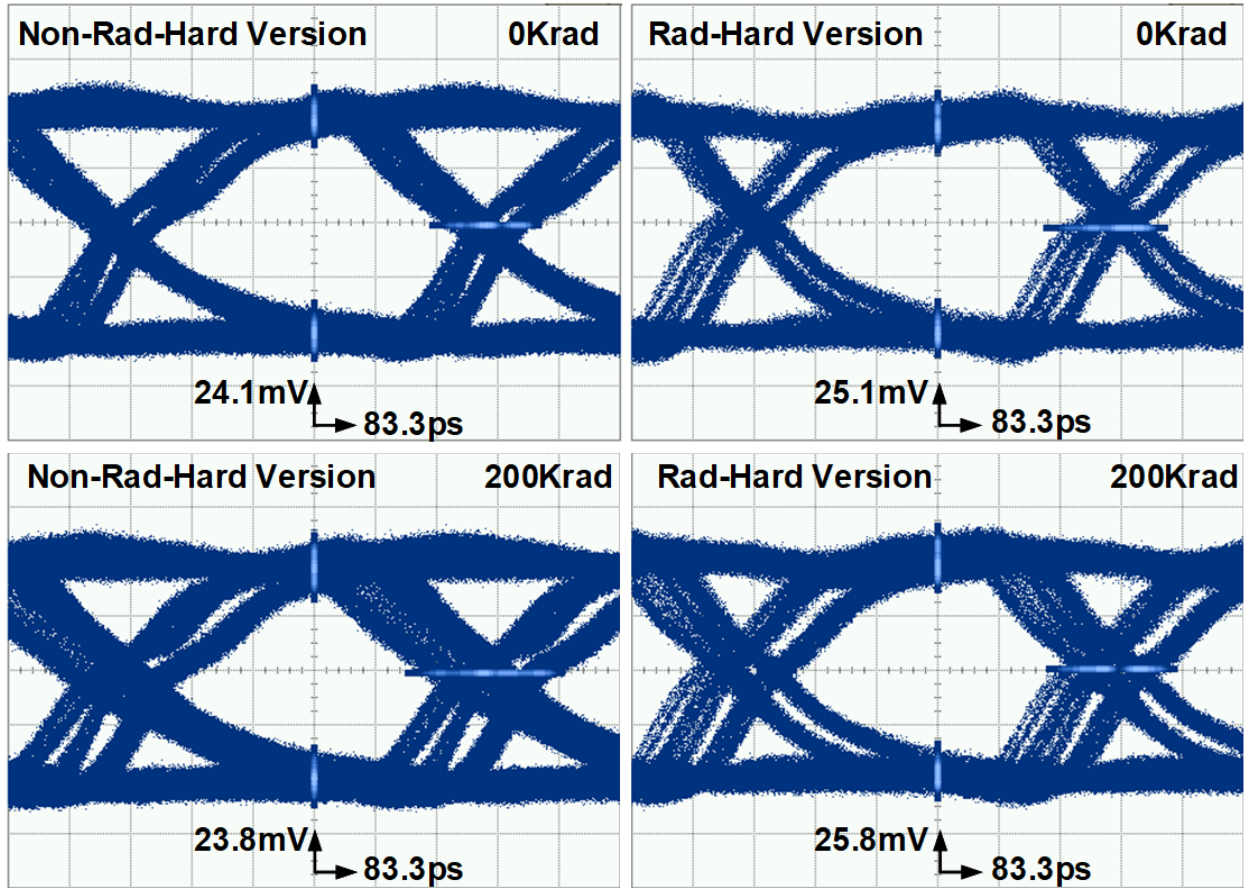


**Figure 19: 0.5 Gbps TX eye diagrams before and after irradiation**

cause inconsistencies in the measurement that are only reduced with a larger sample set.

The measurement setup for SEE testing shown in Fig. 9 was used to perform SEE testing at the Texas A&M Cyclotron Institute for LET levels of 1.3 and 2.5 MeV/(mg/cm<sup>2</sup>). During irradiation, the TX was driven with a 2Gbps PRBS-7 sequence and the BER was monitored during

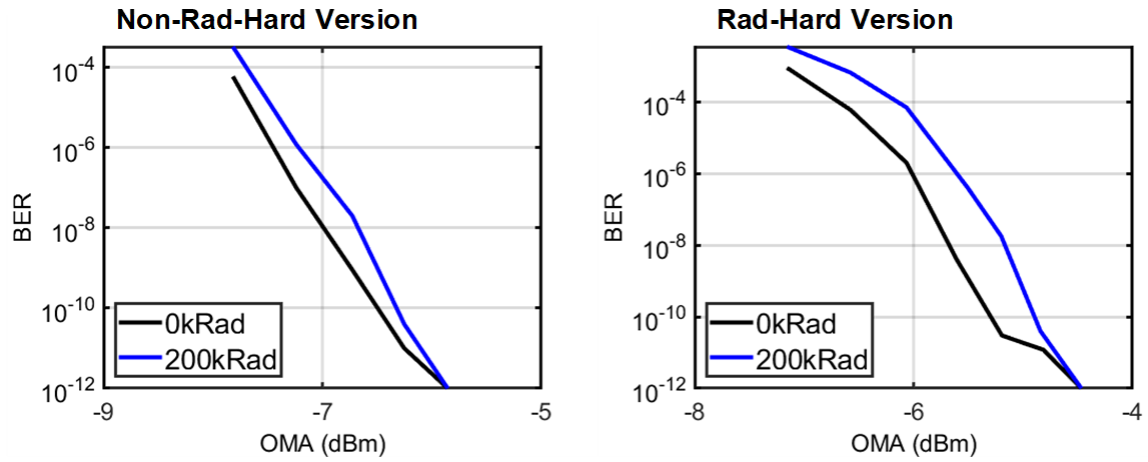




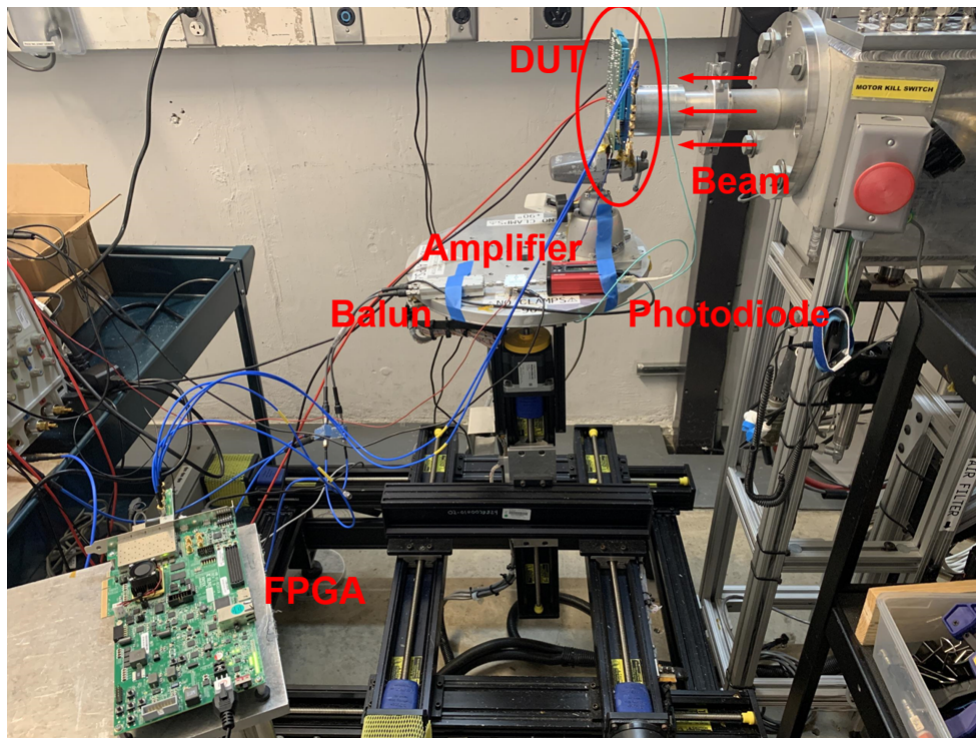
**Figure 20:** 2 Gbps TX eye diagrams before and after irradiation

irradiation to capture upsets. Several runs were carried out to check the BER performance and the overall link health. No errors were observed for both radiation-hardened and non-radiation-hardened version at an energy level of  $1.3 \text{ MeV}/(\text{mg}/\text{cm}^2)$ . However, both versions had recorded link failures at an LET of  $2.5 \text{ MeV}/(\text{mg}/\text{cm}^2)$ . TX link issues were observed in the radiation-hardened design on only 1 out of 8 runs while the unhardened design had link issues on 3 out of the 7 runs. While this result shows some success in the TMR protection in the scan chain and data path, more testing needs to be done to verify SEE impacts using measurements such as eye diagrams.

The summary of the first generation transceiver performance is shown below in Table 5. The RX operated at a slightly lower data rate than that of the TX due to limitations with the DC



**Figure 21:** RX sensitivity (loopback) before and after irradiation



**Figure 22:** SEE test setup at TAMU Cyclotron Institute

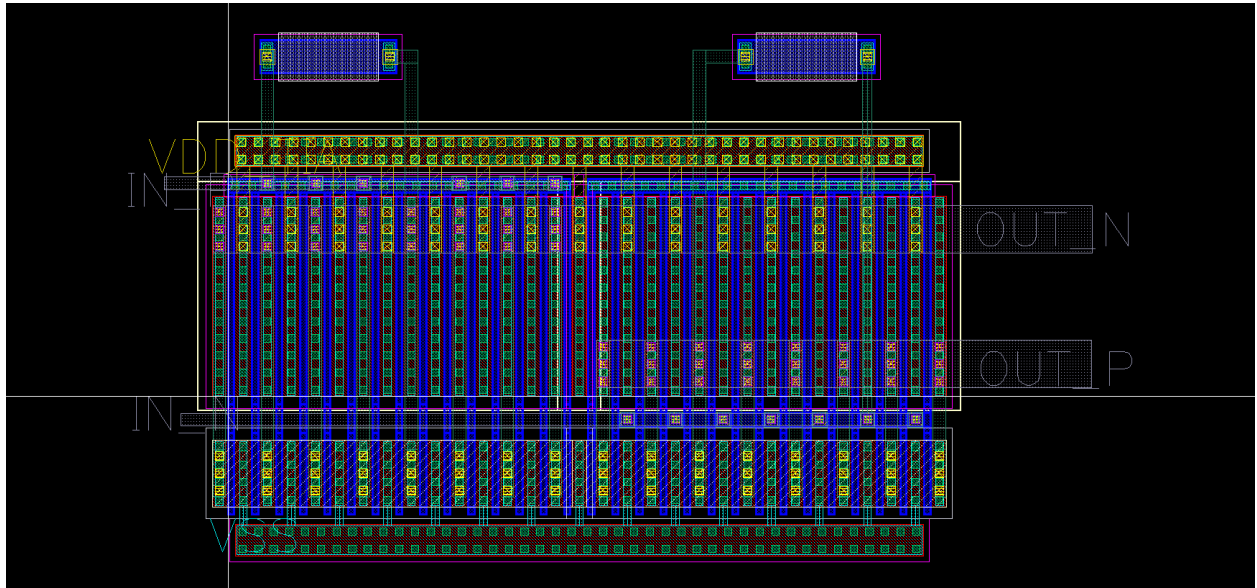
cancellation scheme as discussed. A result of this is lower than expected sensitivity at higher data rates.

**Table 5:** Gen 1 Performance Summary

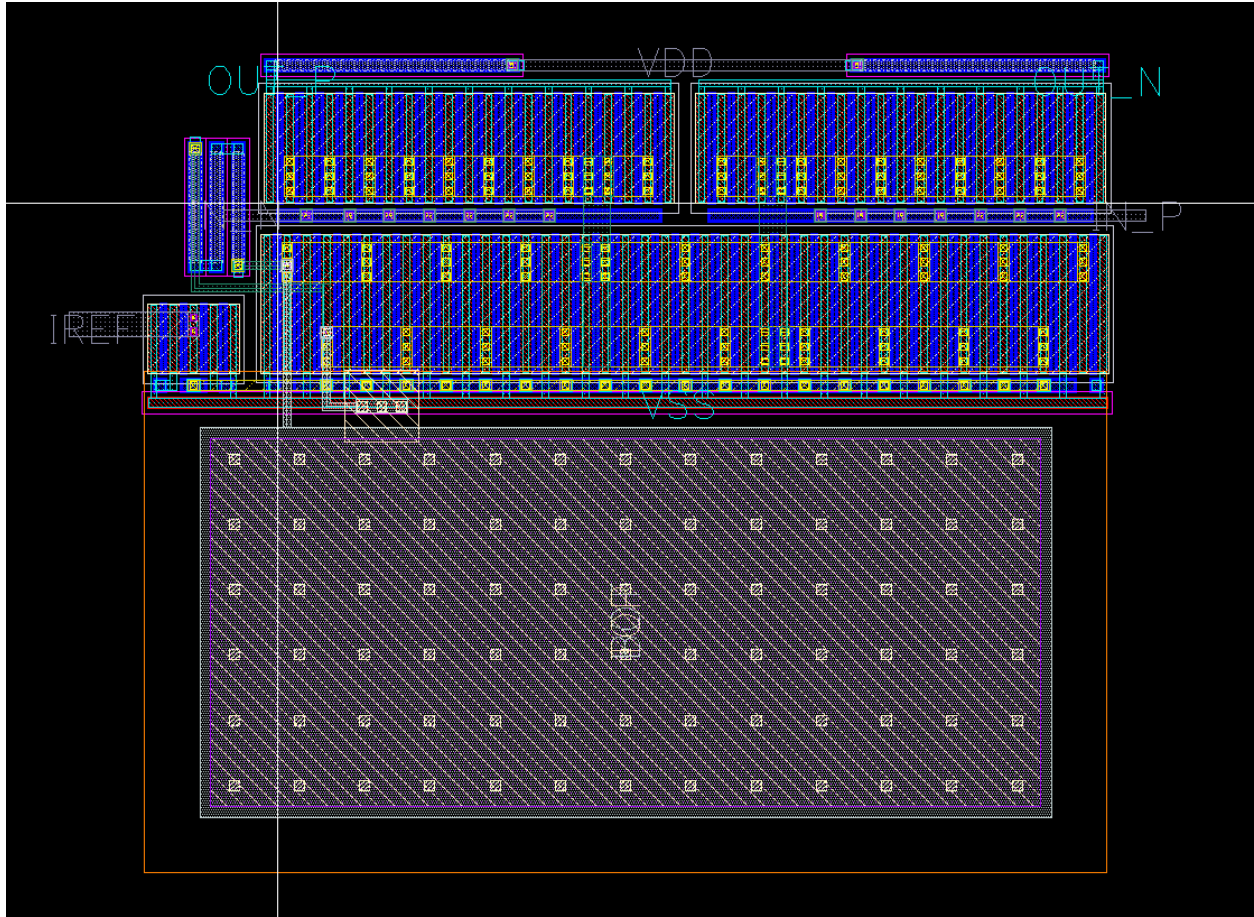
Technology	180nm CMOS
PD & VCSEL	Connectorized
Supply Voltage	1.8V/3.3V
TX Data Rate	0.01-2 Gbps
RX Data Rate	0.01-0.5 Gbps
TX Bias Current	0-11 mA
TX Modulation Current	0-7 mA
Loopback Sensitivity ( $10^{-12}$ BER)	-4.6 dBm
TX Power Consumption	117 mW
RX Power Consumption	128 mW
Radiation Hardening Techniques	TMR, ELT
TID Radiation Tolerance	200kRads

## 4.2 Gen 2 Simulated Results

In this section, the post-layout simulations for the second generation RX frontend are presented. Both the AC behavior and transient behavior at 6.25 Gbps was verified after layout was completed for the TIA and CTLE blocks. The layout for the TIA and CTLE was completed in the TSMC 180nm CMOS process and is included below (Figures 23 and 24)



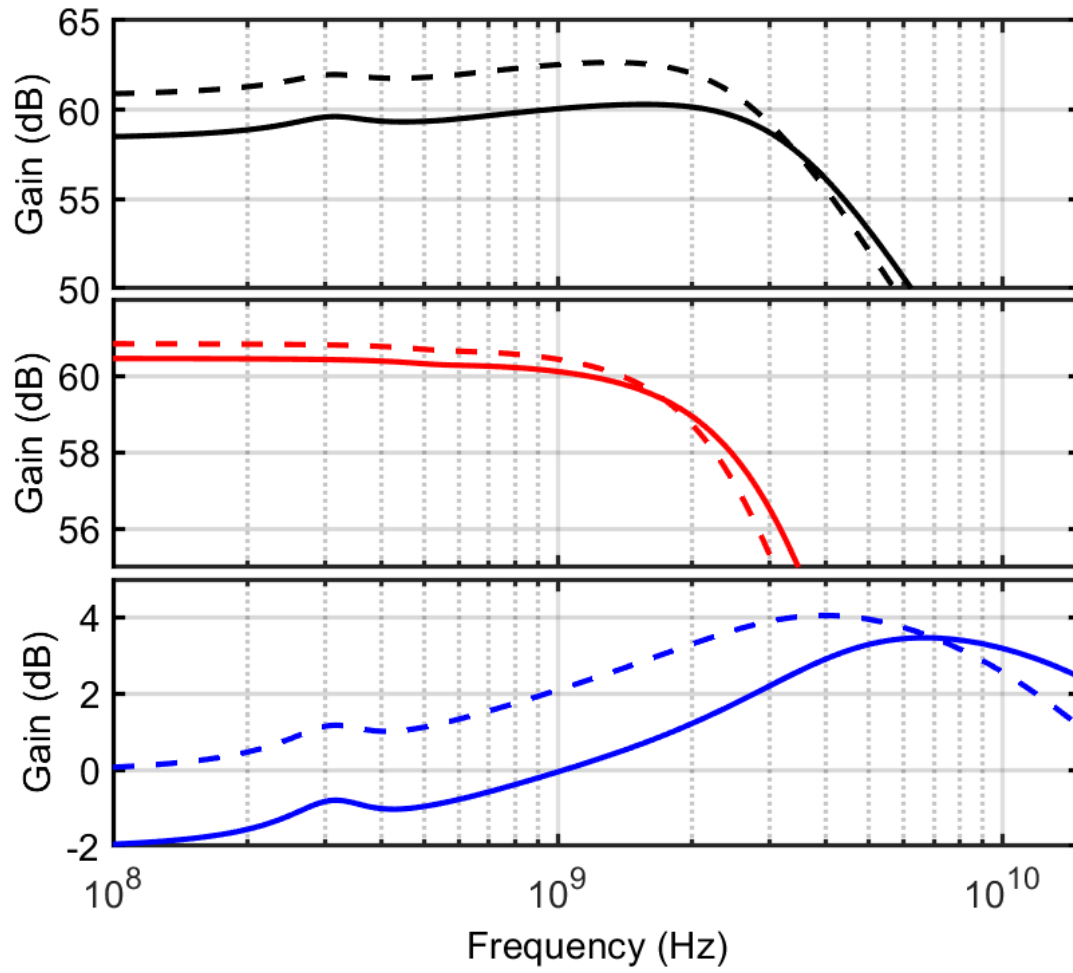
**Figure 23:** TIA layout



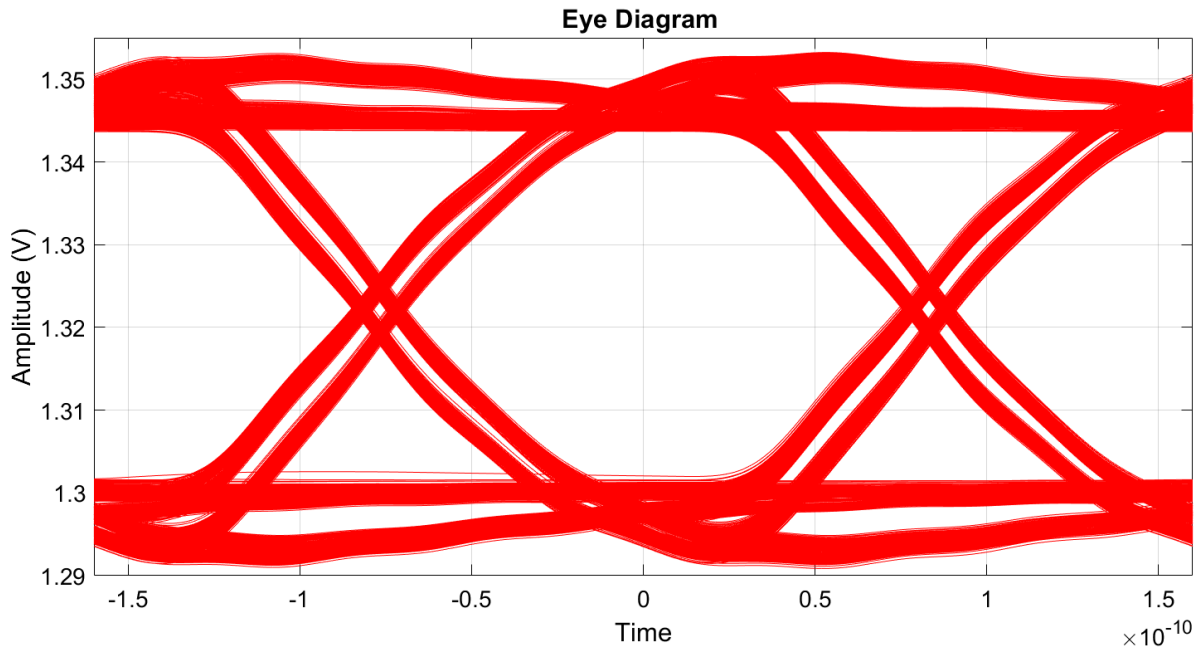
**Figure 24: CTLE layout**

The AC responses of the RX frontend pre and post layout are shown below in Figure 25. The bandwidth of the TIA stayed relatively the same after layout, decreasing only slightly with an increase in the block's gain. The CTLE suffered the most degradation, with peaking shifting to a lower frequency. The circuit's sensitivity to capacitance makes it susceptible to post-layout parasitics, and more tuning needs to be done to restore the behavior. As a result of this, the overall system's bandwidth decreased significantly with the loss in peaking.

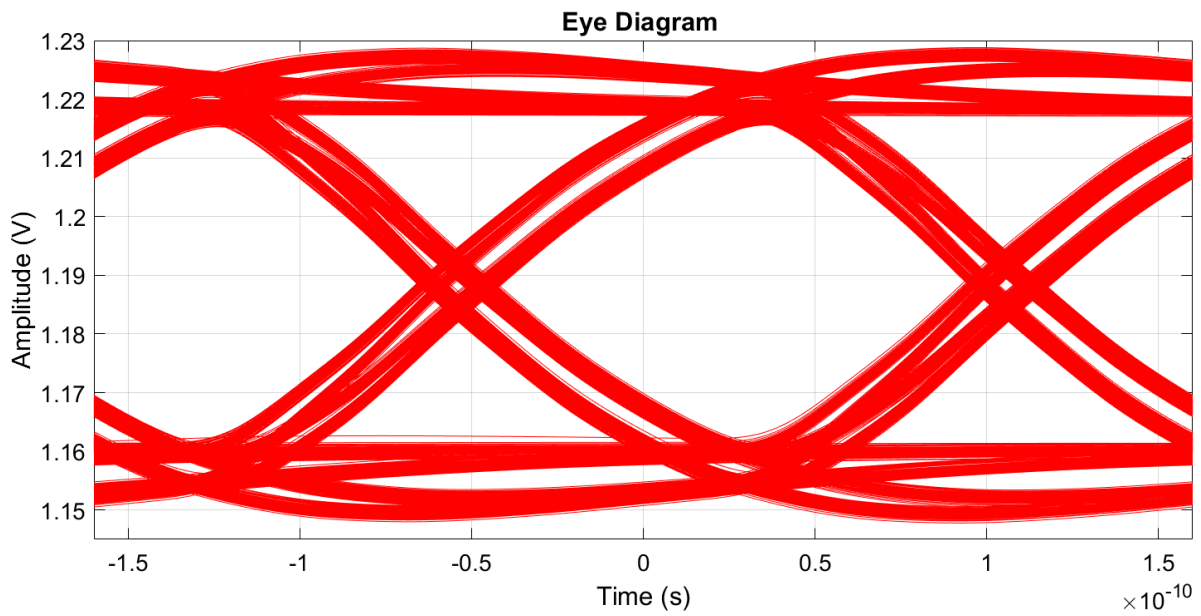
The transient response of the RX frontend was also characterized using eye diagrams at the target data rate of 6.25 Gbps. The pre-layout (Figure 26) eye diagram is significantly better than the post-layout (Figure 27) as expected, with the latter displaying some inter-symbol interference and group delay discrepancies due to the reduced bandwidth.



**Figure 25:** RX frontend AC responses - overall (top), TIA (middle), and CTLE (bottom) - pre-layout (solid), post-layout (dashed)



**Figure 26:** RX frontend pre-layout 6.25 Gbps eye diagram



**Figure 27:** RX frontend post-layout 6.25 Gbps eye diagram

## 5. CONCLUSION

The demand for radiation-hard circuitry, specifically for spacecraft interconnect applications is increasing at a rapid pace. In order to support the growing need for high data rate interconnects, commercial processes must be utilized for their increasing speeds and power efficiency. At the same time, circuits fabricated for spacecraft must be hard to the ionizing radiation and energized particles present.

This thesis has discussed the considerations and tradeoffs necessary for the design of a radiation-hardened transceiver supporting an optical link in a 180nm commercial CMOS process. A low data rate first generation chip was experimentally tested both electrically and under ionizing radiation. The design of a higher data rate second generation device was discussed, and post-layout simulations verifying its operation were presented.

The first generation chip served as a proof-of-concept for hard-by-design practices and their application to optical transmit and receive circuitry, utilizing connectorized optical devices to support ease of testing and modular operation. The second generation chip targets a more realistic integration, with chip-style optical devices and 3D-integration such as what would be present in an industrial solution [27].

Overall, the combination of traditional optical transceiver design practices, radiation hardening methods, and industrial-style integration creates a solution for resilient communication links in spacecraft that does not significantly trade-off efficiency or performance over robustness to radiation. By utilizing these hard-by-design practices, cutting-edge processes can be leveraged to provide improvements to spacecraft electronics that has previously been limited by specialized foundries providing radiation hardening.

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