THERMOELECTRIC POWER HARVESTING FOR BIOMEDICAL IMPLANTS

An Undergraduate Research Scholars Thesis

by

THOMAS JANES, SETH PETROSKY

Submitted to the LAUNCH: Undergraduate Research office at
Texas A&M University
in partial fulfillment of requirements for the designation as an

UNDERGRADUATE RESEARCH SCHOLAR

Approved by
Faculty Research Advisors: Aydin Karsilayan
José Silva-Martínez

May 2021

Major: Electrical Engineering

RESEARCH COMPLIANCE CERTIFICATION

Research activities involving the use of human subjects, vertebrate animals, and/or biohazards must be reviewed and approved by the appropriate Texas A&M University regulatory research committee (i.e., IRB, IACUC, IBC) before the activity can commence. This requirement applies to activities conducted at Texas A&M and to activities conducted at non-Texas A&M facilities or institutions. In both cases, students are responsible for working with the relevant Texas A&M research compliance program to ensure and document that all Texas A&M compliance obligations are met before the study begins.

We, Thomas Janes and Seth Petrosky, certify that all research compliance requirements related to this Undergraduate Research Scholars thesis have been addressed with my Research Faculty Advisors prior to the collection of any data used in this final thesis submission.

This project did not require approval from the Texas A&M University Research Compliance & Biosafety office.

TABLE OF CONTENTS

Page

ABSTRACT 1

DEDICATION 3

ACKNOWLEDGEMENTS 4

NOMENCLATURE 5

1. INTRODUCTION 6

    1.1 Research Description 6

2. SYSTEM OVERVIEW 12

    2.1 Project Specifications 12
    2.2 Oscillator 14
    2.3 DC-DC Boost Converter 25
    2.4 Scenarios 27

3. CONTROL SCHEME AND CIRCUIT BLOCKS 31

    3.1 Control System 31
    3.2 Circuit Blocks 37

4. PHYSICAL IMPLEMENTATION AND LAYOUT 62

    4.1 Full System Integrated Circuit Layout 62
    4.2 System Results & Performance 64

5. CONCLUSION 70

REFERENCES 71

APPENDIX: LAYOUTS 73

ABSTRACT

Thermoelectric Power Harvesting for Biomedical Implants

Thomas Janes and Seth Petrosky
Department of Electrical and Computer Engineering
Texas A&M University

Research Faculty Advisor: Aydin Karsilayan
Department of Electrical and Computer Engineering
Texas A&M University

Research Faculty Advisor: José Silva-Martínez
Department of Electrical and Computer Engineering
Texas A&M University

The modern healthcare industry relies on the use of implantable monitoring devices to obtain potentially life-saving data. This has led to the necessity for small, long-lasting batteries to be used in these devices. In order to replace a device's battery, patients often undergo invasive surgery. This surgery can be costly and physically strenuous for the patient; thus, there is a desire to minimize the frequency of battery replacement. The goal of this research is to develop an integrated circuit that can supply harvested energy to an implantable monitoring device so as to extend implant batteries' lifetime. These monitoring devices are often implanted just below the skin of a patient, where natural temperature gradients exist. Using the well-known physical principle called the Seebeck effect, these temperature gradients can be exploited to produce electrical power by using a specialized device called a thermoelectric generator. With some additional circuitry, this harvested energy can be used in place of the battery to supply power to

the implanted device. Such circuitry includes a switching regulator with a PWM controller, an oscillator, and digital logic. The thermoelectric generator can harvest enough energy to power the device, but the voltage produced is generally too low to be used. Thus, the voltage must be stepped up to a higher value. The switching regulator topology best suited for this purpose is the DC-DC boost converter due to its high efficiency. However, the amount of power harvested is small, so this paper has a major emphasis on power consumption optimization for each circuit block added. Also, the boost converter must use feedback in order to regulate the output to a constant voltage, so a controller was designed and implemented for this purpose. An additional feedforward path was added to perform an impedance match between the source resistance and the boost converter to reduce the charge time of the output capacitor. An oscillator was needed to switch transistors in the boost converter and provide the synchronicity needed in the digital logic blocks. Finally, the last circuitry developed was digital logic to control the startup procedure and choose to use either the harvested energy or the battery to power the implanted device. This paper will discuss the design procedure for each of the mentioned circuit blocks and provide the results of the research conducted.

DEDICATION

To our friends, families, instructors, and peers who supported us throughout the research process.

ACKNOWLEDGEMENTS

Contributors

We would like to thank our faculty advisors, Dr. Karsilayan and Dr. Silva-Martínez, and our industry mentors, David Genzer and Vighnesh Das, for their guidance and support throughout the course of this research.

Thanks also go to our friends and colleagues and the department faculty and staff for making our time at Texas A&M University a great experience.

Finally, thanks to Troy Buhr for his encouragement and guidance in helping us to complete this project.

All other work conducted for the thesis was completed by the students independently.

Funding Sources

There was no provided funding for this research.

NOMENCLATURE

TEG	Thermoelectric Generator
V	Volt
mV	Millivolt (10^{-3} V)
µW	Microwatt (10^{-6} W)
µA	Microamperes (10^{-6} A)
nA	Nanoamperes (10^{-9} A)
CMOS	Complementary metal-oxide semiconductor
IC	Integrated circuit
IBM	Intelligent Business Machines Corporation
°C	Degrees Celsius
µm	Micrometers (10^{-6} m)
nW	Nanowatt (10^{-9} W)
pF	Picofarad (10^{-12} F)
fF	Femtofarad (10^{-15} F)
kHz	Kilohertz (10^{3} Hz)
Ω	Ohm
kΩ	Kiloohm (10^{3} Ω)
MΩ	Megaohm (10^{6} Ω)

1. INTRODUCTION

1.1 Research Description

This project seeks to tackle the challenge of extending the lifetime of biomedical implant batteries with the addition of an integrated circuit and energy harvesting techniques. Currently, biomedical implants and implantable medical devices (IMDs) operate on batteries with a limited lifespan. Battery replacement for IMDs and other implants is an inherently invasive procedure, and taxing for the patient [1]. Decreasing implant power consumption and increasing the battery capacity are two ways to reduce the frequency of battery replacement. Since neither of these methods ensure continuous operation, the motivation to provide an alternative to the current process is clear.

This project will investigate power harvesting techniques to utilize natural temperature gradients in the human body to power the device in place of the battery. The addition of this feature can increase battery lifespan and reduce the frequency at which patients require replacement procedures. The overall architecture is similar between existing technology/research and the implementation of this project, with both using clock generation and DC-DC conversion circuitry [2]-[4]. The expected results of this project include a fully designed integrated circuit layout using an IBM 180nm CMOS process capable of providing the necessary amount of power and boosting an ultra-low input voltage to a usable level.

1.1.1 Input and Output Devices

Throughout the course of this research, the team focused on developing circuitry for specific input/output devices. This allowed for a tailored IC to be designed to work with these parts.

These devices were the TEG and IMD. The TEG targeted was the 1MC04-048-05_TEG from the company TEC Microsystems. Ten of these devices were purchased for the purpose of this research, despite a physical IC was not being manufactured. The IMD targeted was the Biomonitor from the company Biotronik. The researchers met weekly with two industry representatives who work as engineers at Biotronik. This allowed for the group to ensure the circuitry developed would be able to interface with the Biomonitor device.

The TEG datasheet along with the temperature gradient expected across the Biomonitor device sets a lower limit for the input voltage and power [5]. These values are 19.2mV and 29.8µW for a 1ºC temperature gradient. Furthermore, Figure 1.1 displays the data recorded when testing the TEGs selected for this work. The device was tested by applying ice, a human finger and hot plate to one side, in order to create a temperature gradient, and measuring the voltage produced by the gradient with a multimeter. The TEG itself was determined by the size available within the IMD, since the TEG had to be small enough to fit inside of implant. The size of the TEG is 8mm x 8mm x 1.6mm.

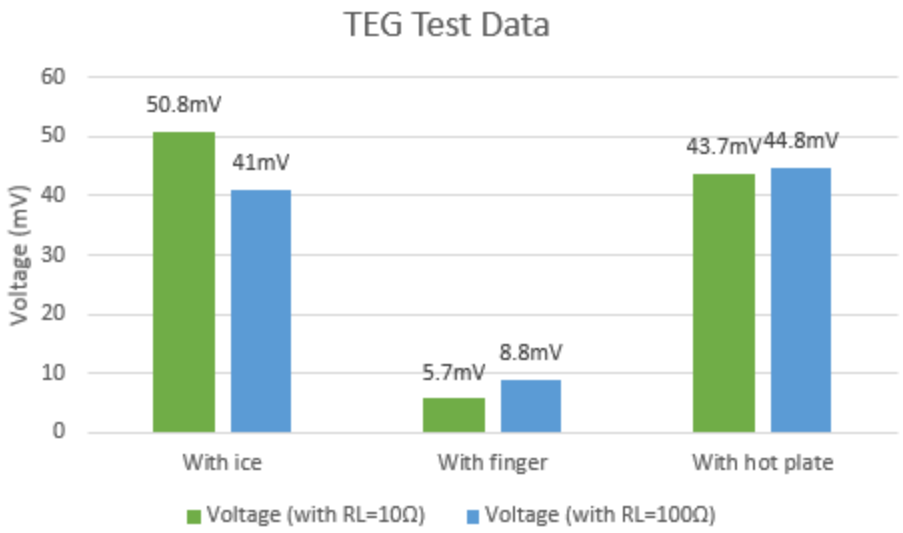

Figure 1.1: Recorded TEG Performance Data

The TEG was the input device for the IC, serving as the primary power supply. The load for the IC was the IMD itself, where the amount of power drawn at any time could be represented as a DC current source. With the insight of the Biotronik representatives, the baseline for this current draw was set to a nominal 10µA. This would cover most of the operations of the Biomonitor device besides some short periods of communication. If the IC did not have enough power to deliver to the IMD to cover these periods of communication, the digital logic on chip would switch the connection to the Biomonitor's fixed battery voltage instead of the IC's output. Furthermore, the Biomonitor has an internal power supply of 1V, so the voltage that was set as the target for the output of the IC was 1V.

1.1.2 System Design

The IC developed for this project had two primary objectives: boost the TEG voltage to a usable level and be able to deliver 10µA to the IMD. To do this, there were four main circuit structures that had to be designed and implemented. These circuits were a DC-DC boost converter, an

oscillator, a PWM controller, and a decision logic block as shown in Figure 1.2. This section will describe the purpose of each of these blocks.

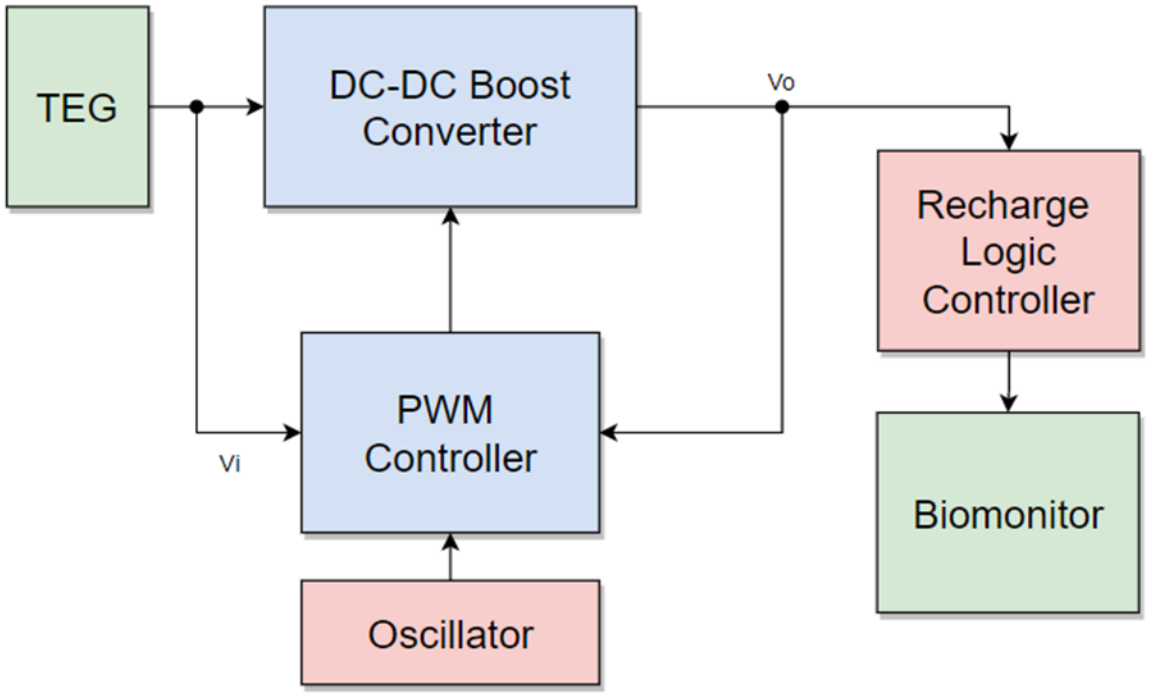

Figure 1.2: System Block Diagram

A DC-DC boost converter circuit was needed in this project because the voltage produced by the TEG was too small for the IMD to use. As the name implies, a DC-DC boost converter converts a DC voltage to a higher DC voltage. These circuits typically have higher power efficiency than other regulators that perform the same function. In this application, efficiency was crucial, so the boost converter was the only viable option.

An oscillator was required for the control scheme of the boost converter. By generating an input clock signal, the oscillator is used to develop non-overlapping clock signals that are pulse-width modulated by the PWM controller. Furthermore, the oscillator was used in conjunction with

other logic blocks throughout the control scheme (e.g. the sawtooth generator, an SR latch, and the maximum duty cycle logic).

The PWM controller was used alongside the DC-DC boost converter and the oscillator to regulate the circuit. The controller regulated two voltages in the circuit: the input and output voltage. This regulation would be performed in two separate modes of operation, which were the maximum current mode and the constant voltage mode. During the maximum current mode, the input voltage would be regulated to half of the open-circuit voltage of the TEG. This required the open-circuit voltage of the TEG to be sampled at different times, which was done with a dedicated circuit block. By regulating the input voltage of the boost converter to one half of the open-circuit voltage, the source resistance of the TEG and the boost converter itself are effectively impedance matched. Under this condition, the input current to the boost converter is maximized. This is because the power transfer to the boost converter is maximized in a DC circuit when the source and load resistance are equal [16]. This notion is part of the maximum power transfer theorem. Maximizing the current sent to the load charges the output capacitor at the maximum rate, which was the purpose of this mode of operation. The second mode of operation regulates the output voltage to a reference. This mode of operation is switched to when the output voltage exceeds a specific threshold. The specific values of the references and threshold voltages will be discussed in later sections.

Since there were times in which the boost converter's output voltage or power was too low to adequately provide power to the implant, a digital logic block was developed to select between the implant's internal power source or the boost converter's output. This allowed for normal

operation of the implant under conditions where the TEG was not seeing a temperature gradient or if the implant was demanding more power than the boost converter could provide.

The following sections of this paper will explore the design process of each of these respective blocks in more detail and discuss design challenges. Furthermore, simulation results and layout images are compiled in the final section of this paper.

2. SYSTEM OVERVIEW

2.1 Project Specifications

Since the internal V_{DD} for the Biomonitor is 1V, the boost converter needs to boost the input voltage coming from the TEG up to a constant 1V. Furthermore, the boost converter should be able to provide the current required by the Biomonitor up to 10µA. With this information, a simple power budget calculation can be performed for the worst-case scenario input with a 1ºC gradient:

$$P_{budget} = 29.8\ \mu W - \ 10\mu A * 1V = 19.8\mu W \qquad (2.1)$$

Since this research is designing for the worst-case scenario, the power dissipated from the control logic, PWM controller, oscillator, and boost converter itself must be less than 19.8µW. This is a small amount of power to work with and presents considerable design constraints. The amount of current used in each of the blocks had to be limited to the nano-amp range to keep the average power dissipation within the specifications.

The traditional approach to implement the switches in the boost converter is to use an n-type transistor for the low-side switch and a diode for the high-side switch. This requires less control and timing logic but consumes a nominal amount of voltage when forward-biased. Thus, since this application cannot afford extraneous voltage losses like some high-voltage applications can, the high-side switch was selected to be a p-type transistor. This required the development of a non-overlapping clock generator in order to ensure the two switches were never on simultaneously.

Since this research involved an IC design in a CMOS technology, the switches used were MOSFETs. When operating as switches, these devices mostly operate in the triode or linear region and ideally have zero drain-source resistance. This allows the transistor to look like a switch. However, these devices have a non-zero drain-source resistance when conducting. The parameters that affect the channel resistance of these devices include the transistor width, length, and finger number. As the length increases, the resistance increases proportionally. So, the minimum length in the process, 180nm, was used for both switches. Additionally, the resistance follows a 1/W behavior with the width W as shown in Equation 2.2.

$$r_{ds} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{tn})} \text{ [10]} \qquad (2.2)$$

However, the capacitance seen at the gate of the device increases linearly with width. Increased capacitance at the gate leads to increased switching losses. So, a balance with the width had to be satisfied in order to best reduce the amount of power consumed in the switches. Higher finger numbers also reduce the channel resistance for triode devices. So, the maximum number of fingers the process would allow, 200, were used for both switches. The final devices were sized such that the r_{ds} value was less than 1Ω for both switches. The final sizes of the devices were 1µm/180nm with 6000 fingers for the NMOS and 2µm/180nm with 12000 fingers for the PMOS. The tradeoff of sizing the devices this big was the added capacitance to the gate of each transistor. This will increase the switching losses that occur on each clock cycle according to Equation 2.3 shown below.

$$P_{sw} = C_{gate} V_{clk}^2 f_{clk} \qquad (2.3)$$

In addition to incurring power losses, having larger switches requires a driver circuit to be developed to reduce the delay of the clocks. The design of this circuit will be discussed in a later section.

2.2 Oscillator

The oscillator subsystem is the most critical component in the control circuitry required to operate the DC-DC boost converter for power harvesting. DC-DC boost converters and power harvesting circuits typically operate at frequencies of 10s to 100s of kHz, so designs that could generate signals in this frequency range were explored. The circuit is powered by a 1 V supply that will be selected by an on-chip logic circuit. First, this supply will be the primary battery attached to the Biomonitor, for cold-startup. Once the boost converter charged the local supercapacitor to the selected minimum supply voltage of 700 mV, the oscillator will operate with it as the supply. In order to ensure sufficient power is supplied to the biomedical implant, power consumption must be minimized. With these considerations in mind, schematic level Cadence simulations were run on the oscillator to confirm ultra-low power consumption and validate performance.

2.2.1 Design Iterations

2.2.1.1 Design 1 - LC Oscillator

The design process for this subsystem was centered around three main characterizations: the power consumption, minimum frequency and minimum startup voltage. Initially, research began with a survey of various low power LC oscillator designs. A Colpitts oscillator was designed and tested with few initial simulations, however, this topology proved undesirable given the size of inductors and capacitors needed to generate oscillations in the target frequency range. Capacitors and inductors implemented through an IC process are typically very unreliable and consume more space than would be available on the final IC. As a result, off-chip components would have needed to be used which would be undesirable since off-chip inductors and capacitors were already needed for the operation of the DC-DC boost converter.

2.2.1.2 Design 2 - Ring Oscillator

After evaluating the Colpitts, research moved to the exploration of ring oscillators. The ring oscillator is the simplest oscillator available and consists of an odd number of inverters in series to provide an oscillating output signal. For this iteration, 7 inverters were used in series with a delay capacitor located at the output of each inverter to lower the frequency to the kHz range. In addition, a single stage frequency divider was required at the output of the oscillator to meet the 100 kHz target. Though the power consumption for this design was very low at approximately 5.5 µW, it still consumed more of our system's power budget than desired. This leaves less room for power consumption in additional feedback circuit blocks required by the system. Furthermore, the delay capacitors of the ring oscillator have an undesirable chip footprint. Given these findings, I expanded my research to more complex oscillator designs specifically meant for ultra-low power consumption.

2.2.1.3 Design 3 - Relaxation Oscillator

The next design tested was a relaxation oscillator. Figure 2.1 presents the schematic of a relaxation oscillator designed and adapted from [6]. The oscillation of signals Q and QB are based on the alternating charging and discharging of equally sized capacitors by comparing the voltages of these capacitors with a reference and sending the result to an SR latch. A bias current generation block delivers charge to the capacitors to generate a voltage which is then compared against the reference voltage created by the bias resistor included in the current source. This bias current block includes a Wilson current mirror connected to a cold start block. Furthermore, the bias current is the key to low power consumption in the oscillator.

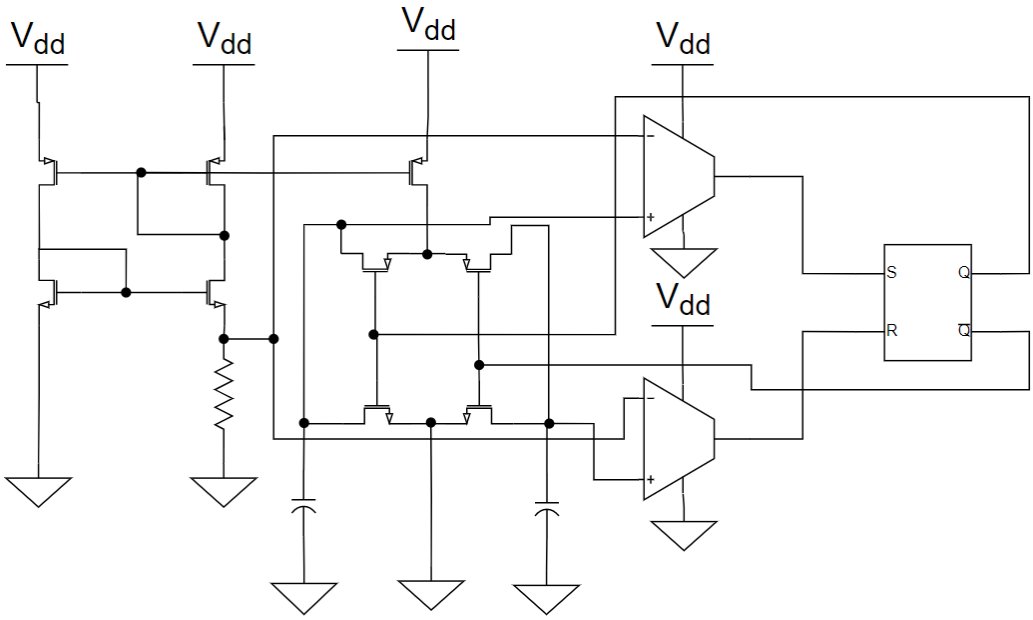

Figure 2.1: Relaxation Oscillator Schematic

Although this design demonstrated dramatic power consumption improvements from previous designs, the minimum startup voltage required for the oscillator was 826 mV. The minimum supply voltage we expected to see in the system was 700 mV, so a more robust relaxation oscillator was needed.

2.2.1.4 Design 4 – Relaxation Oscillator 2.0

Figure 2.2 highlights the improved relaxation oscillator schematic. This design exhibits a number of similarities to the previous design. Though the startup circuitry has a slightly different topology, the new cell includes a bias current generation block implemented using another Wilson current mirror biased with a 1 MΩ on-chip resistor. Moreover, the new oscillator is realized with significantly less complexity than the original relaxation oscillator. First, the need for multiple current mode comparators, which were designed as operational transconductance amplifiers, and SR latches was eliminated. Furthermore, a single current comparator using two

NMOS transistors, one in series with an on-chip resistor and the other in series with an on-chip capacitor, was used in conjunction with a series of digital output buffers in order to send the output voltage node high. The output voltage node is fed back into the gate of an NMOS transistor connected in parallel with the bias capacitor such that the transistor operates as a "relaxation" switch to discharge the capacitor and trigger periodic oscillations. The frequency of these oscillations is determined by the size of the bias resistor (R), capacitor (C) and buffer delay (τ). See Equations 2.4 and 2.5 from [8] for the calculation procedure used to determine the oscillator's period. Note that in Equation 2.5 C_{INV} refers to the capacitance of a single buffer (inverter) stage and is approximated as 10 fF which is the set value for a single delay capacitor in output buffer chain. Equations 2.6 and 2.7 demonstrate the applications of Equations 2.4 and 2.5 used for this design. Notice that Equation 2.7 approximates the period as 12.862 µs, however, the actual period of the design is estimated as 17.334 µs using the frequency ($f = {}^{1}/_{T}$) in Table 2.1 for the 1 V supply case. These differences are likely a product of the gate capacitances and parasitics seen within the output buffer at the schematic level.

$$T = R \cdot C + \tau \tag{2.4}$$

$$\tau \propto \frac{V_{DD} \cdot C_{INV}}{I_{BIAS}} \tag{2.5}$$

$$\tau \cong \frac{1 \cdot (5 \cdot 10f)}{10n} = 5\ \mu s \tag{2.6}$$

$$T \cong 224k \cdot 35.1p + 5 = 7.862 + 5 = 12.862\ \mu s \tag{2.7}$$

In addition, the transistors used in this circuit are less numerous with some sized significantly smaller, helping to further reduce the complexity of the design.

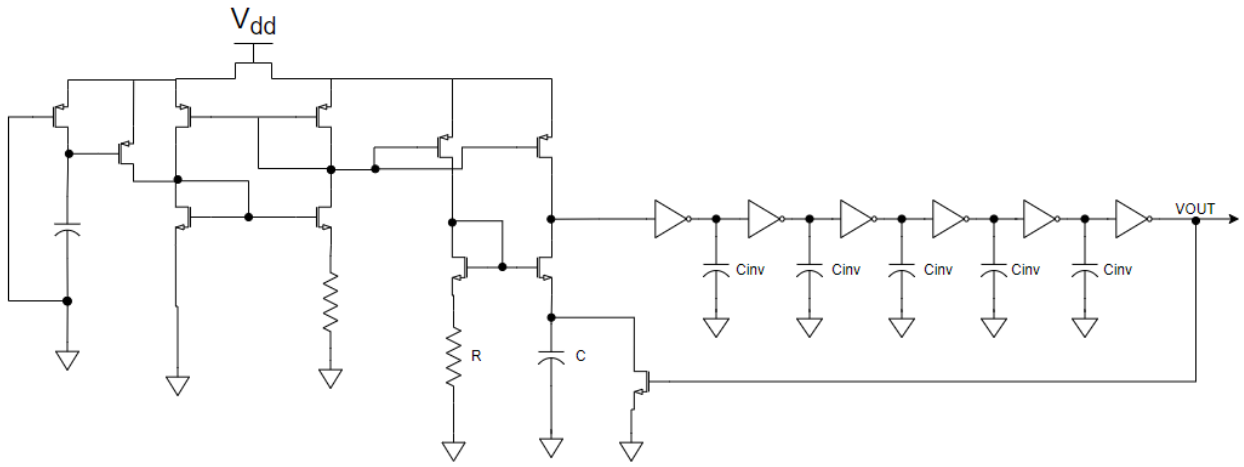

Figure 2.2: Final Relaxation Oscillator Schematic

Another significant benefit of the new design is the low duty cycle of the output waveforms. Since our system requires a "one-shot" oscillation signal with a duty cycle less than or equal to 1%, the optimized oscillator was able to remove the need for a one-shot logic block we originally planned to have in the full system design. The optimization of this design's duty cycle was accomplished by manipulating the size of the relaxation switch and reducing the size of delay capacitors located in the output buffer chain. The validation steps and test results for this design will be discussed in the next section.

2.2.2 Validation & Schematic Level Tests

The first step in validation of the oscillator was to characterize the output waveforms using a transient analysis. Table 2.1 highlights the frequency, power consumption and duty cycle observed at different expected supply voltage levels. Notice the worst case power consumption, seen at the maximum expected power supply of 1 V, is merely 707.2 nW. Figure 2.3 displays an example transient output signal of the oscillator.

Table 2.1: Oscillator characterization at 37 ℃

VDD (supply)	Frequency	Power	Duty Cycle
1 V	57.69 kHz	707.2 nW	0.27 %
700 mV	46.18 kHz	64.57 nW	1.02 %

Note: Duty cycle of the oscillator needs to be approximately ≤ 1%.

Figure 2.3: Oscillator Transient Output Waveform

Since frequency is directly proportional to the supply voltage, a frequency drop from 57.69 to 46.18 kHz is observed at our minimum expected supply. However, the duty cycle, which is our primary validation metric, is still measured to be within the acceptable range at a 700 mV supply. Furthermore, a large drop in power consumption is observed which is a result of the proportional relationship the power consumption shares with both the voltage supply value and the frequency of oscillations.

The second validation step was to evaluate whether the oscillator correctly triggered the blocks it's directly connected to. Figures 2.4 and 2.5 demonstrate the oscillator interfacing with the SR latch and sawtooth generator, respectively.

Figure 2.4: Oscillator Triggering Transistor Level SR Latch

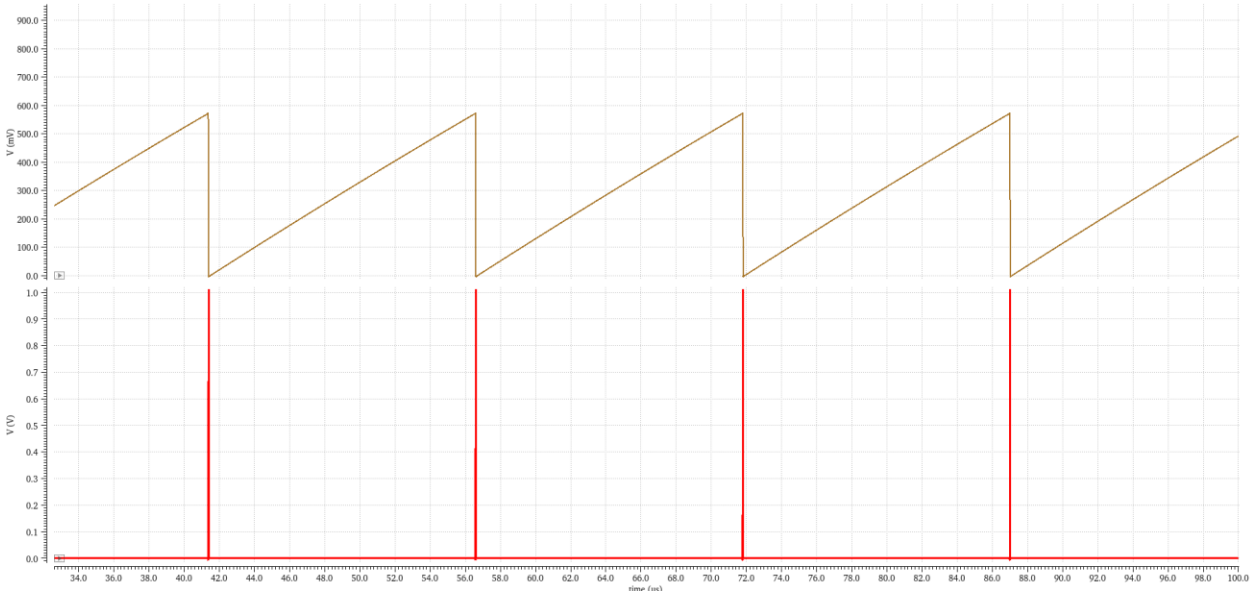

Figure 2.5: Oscillator Feeding Sawtooth Waveform Generator

The final verification step was to run corner simulations. Corner simulations allow the evaluation of extreme cases where process variations cause slow or fast transistors. Cadence provides a way to set NMOS and PMOS transistors to ‘s’ for slow, ‘f’ for fast, or ‘t’ for typical. 5 corners were set up to evaluate ‘ff’, ‘fs’, ‘sf’, ‘ss’ and ‘tt’ cases where the first letter corresponds to NMOS and the second to PMOS. All corner simulations provided expected swing values, so the main

concern when analyzing these simulation results is to ensure that the frequency does not drop below the minimum switching frequency required to operate in continuous conduction mode. The slowest case observed is the ‘ss’ corner at a 700 mV supply, however, the frequency is still above the minimum specified by our inductor size (500 µH) indicating that physical implementation of the design could commence. Figure 2.6 highlights the corner results at 700 mV supply, where 37.3 kHz is the slowest frequency observed due to process variation.

	Parameter	Nominal						C0	C1	C2	C3	C4
	allModels.scs	tt						ff	fs	sf	ss	tt
	design.scs							<unspecified section>	<unspecified section>	<unspecified section>	<unspecified section>	<unspecified section>
	temperature	37						37	37	37	37	37
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4
ThermoBioimplant_SP:RelaxOscV2Test:1	/V0/PLUS											
ThermoBioimplant_SP:RelaxOscV2Test:1	Out freq	46.18K				35.47K	65.46K	65.46K	45.63K	47.16K	35.47K	46.18K
ThermoBioimplant_SP:RelaxOscV2Test:1	Avg. Power	-64.57n				-102.6n	-43.82n	-102.6n	-65.3n	-62.88n	-43.82n	-64.57n
ThermoBioimplant_SP:RelaxOscV2Test:1	Swing	700.4m				700.4m	700.4m	700.4m	700.4m	700.4m	700.4m	700.4m

Figure 2.6: Lowest Frequency Case Corner Simulation Results (VDD = 700 mV)

In addition, Figure 2.7 displays the corner results collected at 1 V supply, where the highest potential frequency and power consumption, seen in the ‘ff’ case, are characterized as 84.11 kHz and 1.258 µW.

	Parameter	Nominal						C0	C1	C2	C3	C4
	allModels.scs	tt						ff	fs	sf	ss	tt
	design.scs							<unspecified section>	<unspecified section>	<unspecified section>	<unspecified section>	<unspecified section>
	temperature	37						37	37	37	37	37
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4
ThermoBioimplant_SP:RelaxOscV2Test:1	/V0/PLUS											
ThermoBioimplant_SP:RelaxOscV2Test:1	Out freq	57.69K				40.68K	84.11K	84.11K	56.36K	58.94K	40.68K	57.69K
ThermoBioimplant_SP:RelaxOscV2Test:1	Avg. Power	-707.2n				-1.258u	-367.7n	-1.258u	-718.2n	-669.8n	-367.7n	-707.2n
ThermoBioimplant_SP:RelaxOscV2Test:1	Swing	999.1m				995.3m	1	995.3m	997.2m	1	1	999.1m

Figure 2.7: Highest Frequency Case Corner Simulation Results (VDD = 1 V)

2.2.3 Layout

The next step in oscillator development was the physical implementation and layout at the silicon level. Figure 2.8 displays the final layout cell view of the oscillator subsystem. Parasitic extraction was performed on the layout such that they are included and considered in the post-layout simulations discussed in Section 2.4.

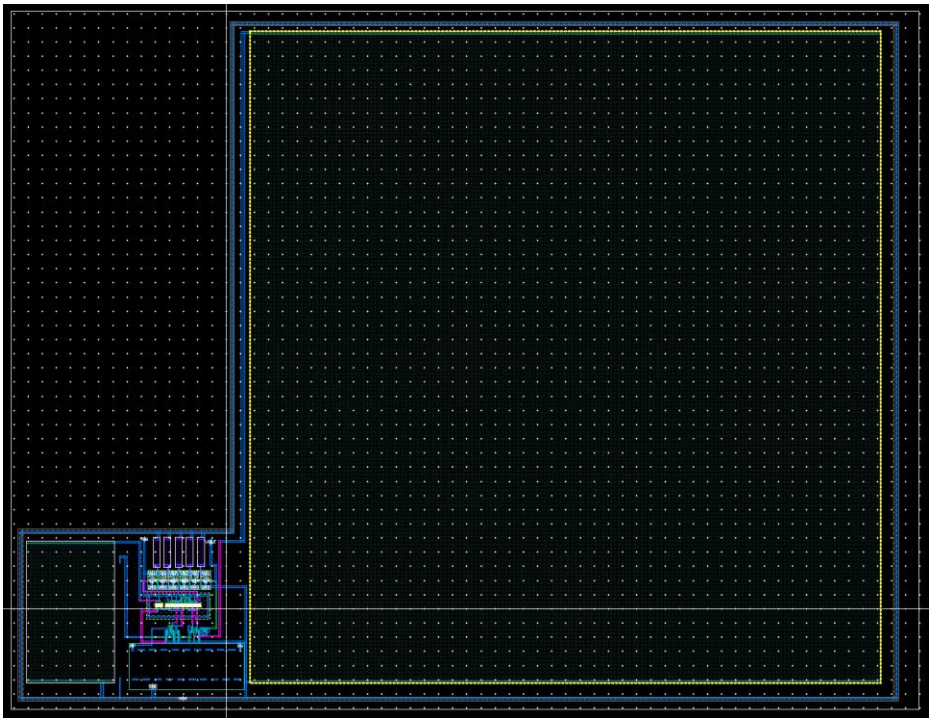

Figure 2.8: Oscillator Layout (x = 320.58 µm, y =246.41 µm)

2.2.4 Post-layout Performance

Once parasitic extraction had been completed, certain simulations performed in section 2.2.2 needed to be recompleted to verify that the physical implementation performed as expected. Figure 2.9 is a transient demonstration of the oscillator output signal, which tracks closely with the expected shape seen in Figure 2.3 from the schematic level. Furthermore, Table 2.2 characterizes the frequency, power and duty cycle at the maximum and minimum supply voltages.

Table 2.2: Post-layout Oscillator Characterization at 37 ℃

VDD (supply)	Frequency	Power	Duty Cycle
1 V	27.36 kHz	529.7 nW	0.15 %
700 mV	16.79 kHz	33.17 nW	0.49 %

Note: Duty cycle of the oscillator needs to be approximately ≤ 1%.

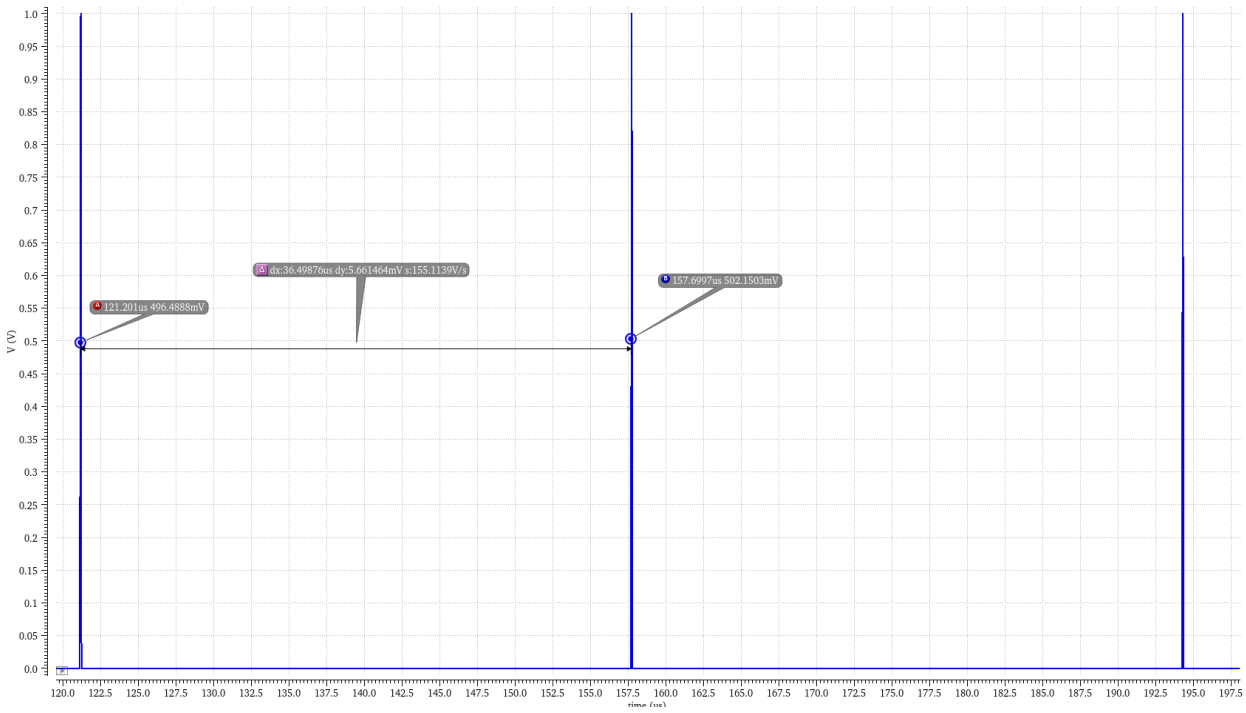

Figure 2.9: Post-layout Transient Output Waveform

Some very clear differences are observed between the characterization of the oscillator at the schematic and chip level in Table 2.1 and 2.2. The minimum frequency is dropped from 46.18 to 16.79 kHz and maximum duty cycle is reduced from 1.02 to 0.49 %. Figure 2.10 displays the post-layout capacitance table and highlights critical capacitances of nodes that play a vital role in determining the frequency of the oscillator. The first highlighted nodes are the positive and negative nodes of the bias on-chip capacitor listed in Equation 2.4, which illustrates that the capacitor is resolved as approximately 35.397 pF compared to the schematic's 35.1 pF. In addition, the parasitic capacitances introduced between the inverters in the output buffer stage are circled in Figure 2.10. To clarify, this is not the value of the delay capacitors included at these nodes in the schematic, but a capacitance introduced by the metal traces added on top of the on-chip delay capacitor. The parasitic capacitances of these traces are each resolved to approximately 5 fF, thus, the delay capacitors are realistically 150% larger than the original 10

fF included in the schematic. With 6 buffers and 5 delay capacitors included in the output chain, the combination of the delay capacitor parasitics and bias capacitor value increase likely play significant roles in introducing the oscillator performance variations. Additional trace parasitics seen at nodes on the current-mode comparator can contribute as well.

Capacitance Table

From	To	Variable	Fixed	Total
I4.CC10.1	I4.CC10.1	0.0	1e-17	1e-17
I4.CC1.4	I4.CC1.4	0.0	2e-17	2e-17
I4.CC1.3	I4.CC1.3	0.0	3.539673e-11	3.539673e-11
I4.CC1.2	I4.CC1.2	0.0	3.539672e-11	3.539672e-11
I4.CC1.1	I4.CC1.1	0.0	1e-17	1e-17
/net1	/net1	1.282094e-13	1.742812e-14	1.456375e-13
/net03	/net03	1.446039e-15	1.00749e-12	1.008936e-12
/I4/noxref_8	/I4/noxref_8	0.0	2.172162e-16	2.172162e-16
/I4/net38	/I4/net38	7.655127e-16	6.780567e-15	7.54608e-15
/I4/net37	/I4/net37	7.703591e-16	2.937086e-15	3.707446e-15
/I4/net30	/I4/net30	3.502407e-15	4.417616e-15	7.920023e-15
/I4/net24	/I4/net24	2.877784e-15	6.177948e-15	9.055732e-15
/I4/net23	/I4/net23	2.312565e-15	9.824362e-13	9.847488e-13
/I4/net20	/I4/net20	2.138451e-15	2.715417e-15	4.853868e-15
/I4/net19	/I4/net19	3.618986e-15	7.27189e-15	1.089088e-14
/I4/net12	/I4/net12	1.131114e-15	3.98449e-14	4.097602e-14
/I4/net057	/I4/net057	1.474703e-15	3.708739e-15	5.183442e-15
/I4/net049	/I4/net049	1.474705e-15	3.825739e-15	5.300443e-15
/I4/net048	/I4/net048	1.474659e-15	3.700702e-15	5.175361e-15
/I4/net046	/I4/net046	1.475866e-15	3.512171e-15	4.988037e-15
/I4/net030	/I4/net030	1.474703e-15	3.707823e-15	5.182526e-15
/I4/X9_noxref_26	/I4/X9_noxref_26	0.0	2.139178e-16	2.139178e-16

Figure 2.10: Post-layout Capacitance Table

Despite the differences seen between schematic and layout cell views, corner simulations seen in Figure 2.11 indicate the minimum frequency seen at the ‘ss’ corner is 11.45 kHz, which is above the minimum required to maintain continuous conduction mode in a DC-DC boost converter system with a 500 µH inductor. For reference, a 165 µH inductor yields a minimum switching frequency of 10 kHz. Also, the duty cycle characterized in Table 2.2 is a much safer distance from the maximum 1 % required by the feedback system.

For informational purposes, Figure 2.12 is included and characterizes the maximum possible frequency, at the ‘ff’ corner with a 1 V supply, as 41.3 kHz with 955.8 nW of power consumption.

	Parameter	Nominal						C0	C1	C2	C3	C4
	allModels.scs	tt						ff <unspecified section>	fs <unspecified section>	sf <unspecified section>	ss <unspecified section>	tt <unspecified section>
	design.scs											
	temperature	37						37	37	37	37	37
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4
ThermoBioimplant_SP:RelaxOscV2Test:1	/V0/PLUS											
ThermoBioimplant_SP:RelaxOscV2Test:1	Out freq	16.79K				11.45K	25.75K	25.75K	16.91K	16.73K	11.45K	16.79K
ThermoBioimplant_SP:RelaxOscV2Test:1	Avg. Power	-33.17n				-57.97n	-20.09n	-57.97n	-34.7n	-31.33n	-20.09n	-33.17n
ThermoBioimplant_SP:RelaxOscV2Test:1	Swing	700.6m				700.6m	700.7m	700.7m	700.6m	700.7m	700.7m	700.6m

Figure 2.11: Corner Simulation Results at V_{DD} = 700 mV

	Parameter	Nominal						C0	C1	C2	C3	C4
	allModels.scs	tt						ff <unspecified section>	fs <unspecified section>	sf <unspecified section>	ss <unspecified section>	tt <unspecified section>
	design.scs											
	temperature	37						37	37	37	37	37
Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4
ThermoBioimplant_SP:RelaxOscV2Test:1	/V0/PLUS											
ThermoBioimplant_SP:RelaxOscV2Test:1	Out freq	27.36K				18.3K	41.3K	41.3K	26.82K	27.79K	18.3K	27.36K
ThermoBioimplant_SP:RelaxOscV2Test:1	Avg. Power	-529.7n				-955.8n	-266n	-955.8n	-533.6n	-494.2n	-266n	-529.7n
ThermoBioimplant_SP:RelaxOscV2Test:1	Swing	1				999.1m	1.001	999.1m	999.8m	1.001	1.001	1

Figure 2.12: Corner Simulation Results at V_{DD} = 1 V

2.3 DC-DC Boost Converter

A boost converter is a circuit topology used to boost input voltage values while maintaining power efficiency. It is referred to as a DC-DC converter because the input signal and output signal are both DC. This is done by switching between charging an inductor and charging a capacitor on different cycles. The basic schematic for a boost converter is shown in Figure 2.13.

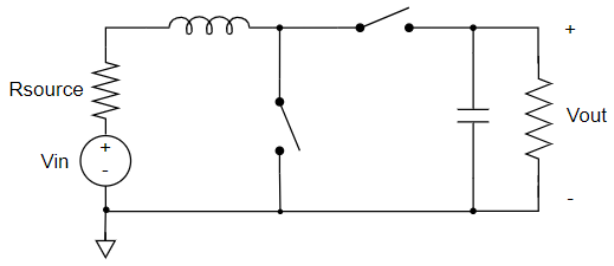

Figure 2.13: Boost Converter Schematic

The switch connecting the inductor to ground is referred to as the low-side switch, and the switch connecting the inductor to the output node is referred to as the high-side switch. The resistor in shunt with the output capacitor represents the load that the boost converter is driving.

The boost converter was the topology chosen among the various topologies capable of stepping up a voltage (e.g., charge pump, linear regulator, etc.) due to its good power conversion efficiency. The only notable power losses for an unloaded boost converter are through the switch resistances, the inductor's equivalent series resistance, switching losses at the gates of the transistors, and the capacitor's equivalent series resistance.

The boost converter operates in two modes in order to transition between charging the inductor and charging the capacitor. The equivalent circuits of the two modes of operation are shown in Figure 2.14. These modes are:

1. The low-side switch is on, and the high-side switch is off, charging the inductor by increasing its stored magnetic energy.
2. The low-side switch is off, and the high-side switch is on, charging the capacitor by increasing the voltage across its plates.

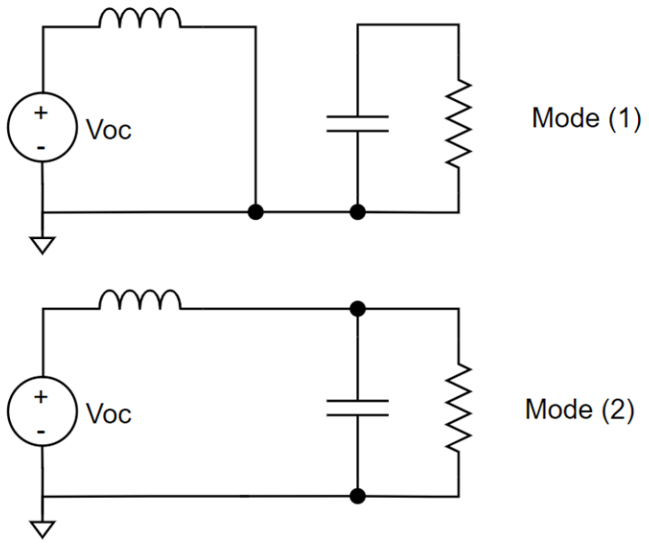

Figure 2.14: Boost Converter Modes of Operation

These switches are controlled by periodic clock signals that have variable pulse-widths. The ratio of the amount of time the clock is high to the total period of the clock is known as the duty cycle. The higher the duty cycle, the longer the low-side switch is on and the more energy is stored in the inductor. Thus, this increases the amount of current that can be sent to charge the capacitor when the high-side switch is on. This behavior can be modeled below in Equation 2.8, where *D* represents the duty cycle ratio:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \text{ [9]} \qquad (2.8)$$

Thus, a higher duty cycle yields a higher voltage gain. The PWM controller that will be discussed in later sections in more depth is the circuit responsible for controlling the value of the duty cycle sent to the boost converter and therefore its overall voltage gain.

2.4 Scenarios

To demonstrate how the IC responds to various conditions, a few plots are shown in this section detailing different expected scenarios. These simulations were performed with semi-ideal

components (e.g. analogLib switches with non-zero switch resistance). This was to decrease simulation time while still capturing the circuit's behavior.

The first scenario to discuss is the case in which the load is demanding more power than can be supplied by the boost converter. This was simulated by attaching a current source of value 1mA to the output once the circuit transitions into the constant voltage mode. Then, after some time, the current is decreased to a manageable 10µA. When the current drops to a manageable level, the circuit should be able to boost back up to 1V and sustain operation. Figure 2.15 below shows the results of this simulation.

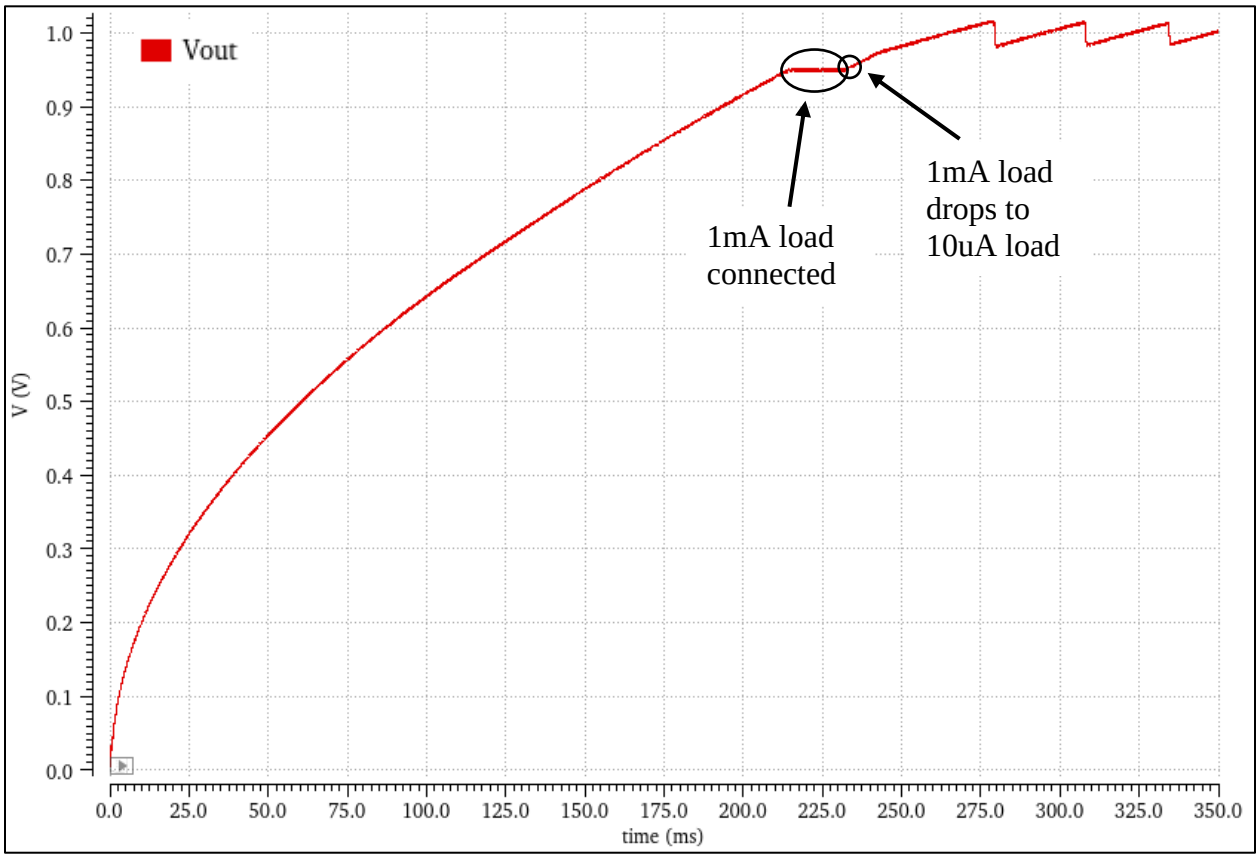

Figure 2.15: Scenario 1 – Load Demanding Too Much Power

Figure 2.15 shows the stalled response of the IC as it struggled to deliver the demanded power. Once the load is reduced to a manageable 10µA, the system quickly recovers and begins to deliver power to the Biomonitor.

The second scenario tested was the response of the IC to a negligible temperature gradient. If the temperature seen across the TEG is close to zero, the voltage will drop to around 0V. To simulate this condition, the TEG voltage was set initially to 19.2mV, which corresponds to a 1ºC gradient. Then, the voltage is dropped to 0V and, after some time, is reset to 19.2mV. The response of the circuit is shown in Figure 2.16.

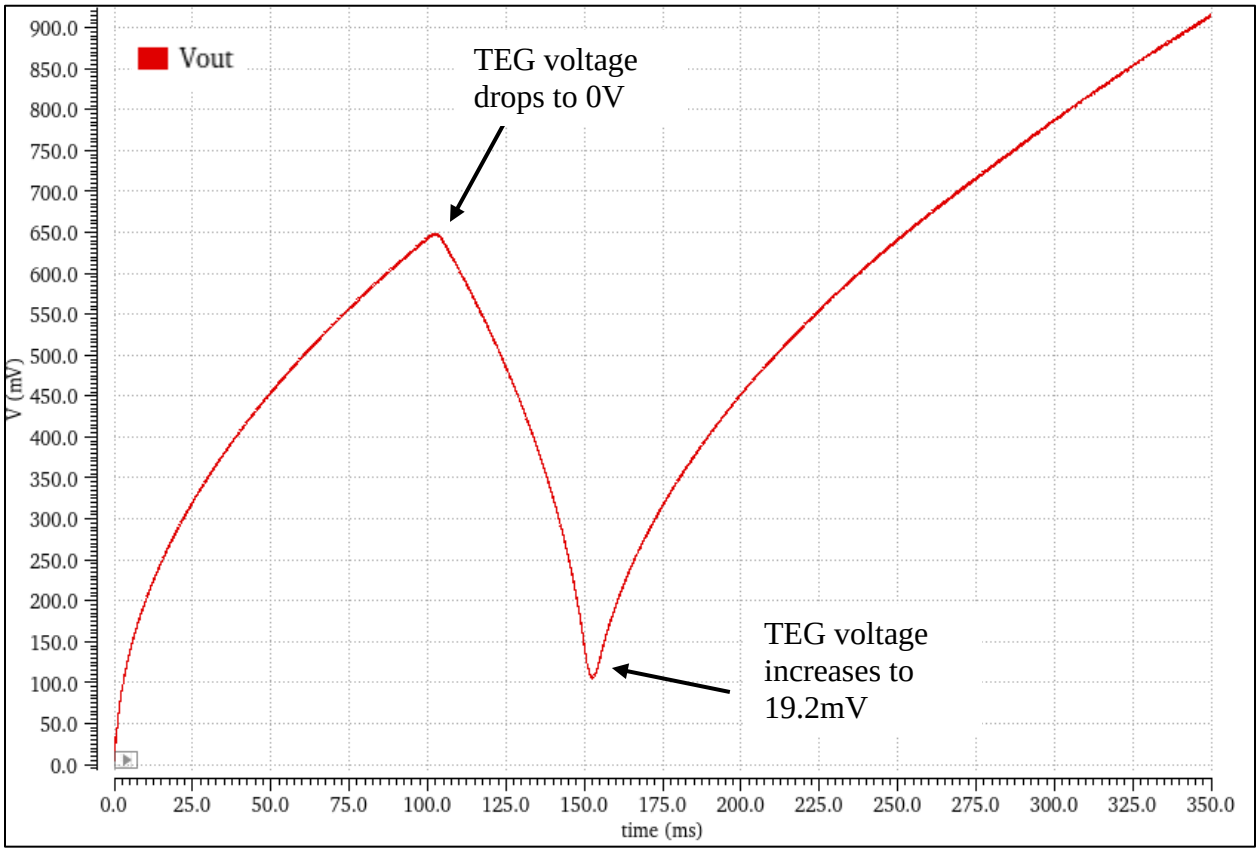

Figure 2.16: Scenario 2 – Loss of Temperature Gradient

The output voltage begins to drop as soon as the TEG voltage drops to 0V. The Biomonitor is supported by its own V_{DD} during this period. Once the TEG voltage increases back to 19.2mV, the voltage at the output steadily rises and begins to function properly again. Thus, the system was able to recover in this case.

3. CONTROL SCHEME AND CIRCUIT BLOCKS

3.1 Control System

3.1.1 System Overview

One of the requirements of this research is to maintain a constant output voltage of 1V. Since the input voltage changes with the temperature gradient seen across the TEG, a hard-coded duty cycle could not be used. If a set duty cycle is used, the voltage at the output will not be maintained as a constant. Thus, a feedback network needed to be applied to keep the voltage constant. Furthermore, since the capacitor at the output is large, the steady-state voltage would take a long time to reach. To speed up the output capacitor's charge time, a second mode of operation in addition to keeping the voltage at a constant value was designed. This method is called the maximum current mode, since it maximizes the current going to the capacitor. Both modes use the same circuitry but require different reference voltages. Figure 3.1 shows how the full system operates with the feedback and impedance matching circuitry.

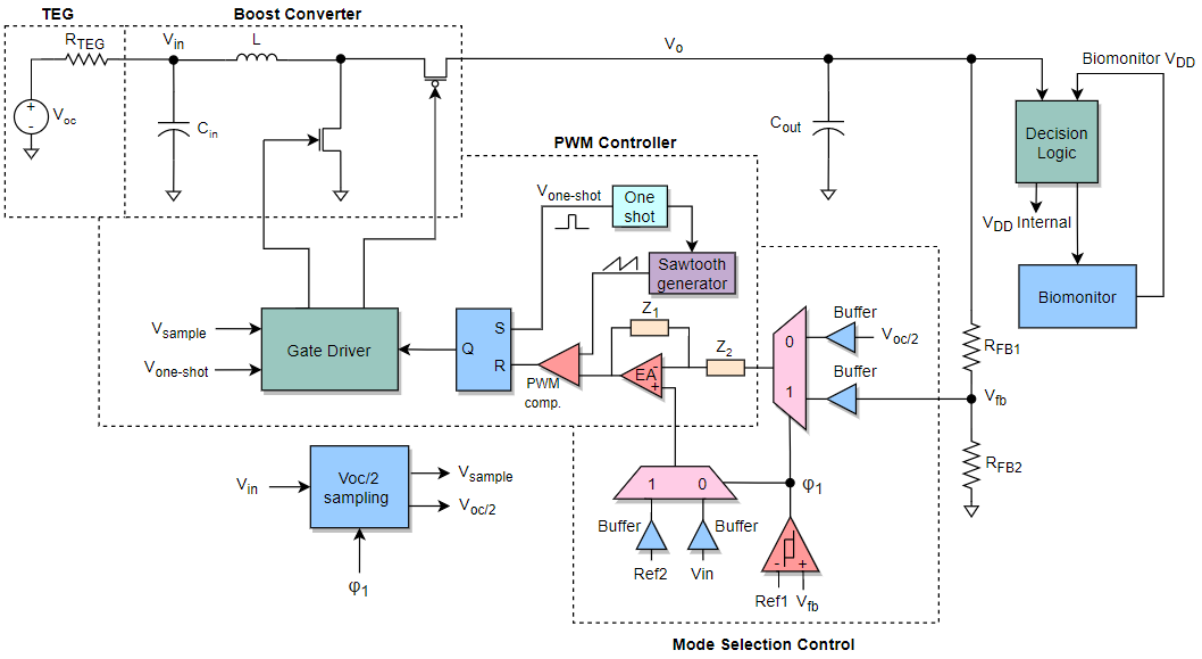

Figure 3.1: Full system with feedback and impedance matching

This system can be segmented into two major components: the PWM controller and mode selection control. The PWM control sets the duty cycle of the input clock signals to either maintain the output voltage at 1V or maximize the current through the circuit. The multiplexors controlled by the output of a hysteretic comparator determine which mode of operation is currently being performed. The multiplexors are composed of transmission gates instead of logic gates so that an analog signal can be passed. If the divided feedback value V_{fb} is greater than Ref1+ $V_{hysteresis}$, then the circuit will be in constant voltage mode. Otherwise, the mode will be maximum current mode. A hysteretic comparator was used to control this state instead of a normal comparator so that the state does not oscillate around the transition point. The buffers seen before the multiplexors are used for two reasons:

1. Remove the loading effect of the feedback resistors R_{FB1} and R_{FB2} from the compensation network of Z_1 and Z_2

2. Prevent leakage from the capacitor storing the value of $V_{OC/2}$ through the multiplexors at the V_{in} input

The decision logic block is responsible for controlling both the circuit's V_{DD} value and the Biomonitor's V_{DD} value. While the value of V_o is less than a given reference, the internal value of V_{DD} would be supplied by the Biomonitor. When this value is exceeded, the output voltage will begin to power all the circuitry in the IC. Thus, each design had to work with a range of V_{DD} values. This range was set from 700mV to 1V. The reason for the choice of 700mV as the low voltage value was due to simulation results run on the oscillator: at 700mV, the frequency was within the range to keep the boost converter in continuous-conduction mode.

The feedback path from the output to the inputs of the error amplifier first pass through a resistor divider with R_{FB1} and R_{FB2}. These two resistors provide divided feedback so that all comparison through the loop can be done at lower voltages. This allows for the common mode inputs of all amplifiers and comparators to be within a set range and, therefore, more easily designed. The references must also be divided by the same factor to appropriately regulate the circuit. The feedback factor is given in Equation 3.1 below.

$$\beta = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \qquad (3.1)$$

The feedback factor for this application was chosen to be 1/10 such that all output voltages would be divided by 10 before being feed into the rest of the loop. The values of the feedback resistors were set to 9MΩ and 1MΩ for R_{FB1} and R_{FB2}, respectively. These large resistances allowed for low quiescent current consumption, which helped improve the overall efficiency of the circuit. Thus, whenever discussing reference values for the comparators and amplifiers, each reference will be regulating the signal input to 10 times its value. For instance, a 100mV input

into the non-inverting input of the error amplifier would regulate the output of the circuit to 1V rather than to 100mV.

3.1.1.1 Constant Voltage Mode

The constant voltage mode of operation regulates the output to a constant value. The voltage-mode control scheme outlined in [11] was used. This method uses an error amplifier that compares the output with a reference value and produces an error signal representing the difference between the two voltages as an analog value between V_{DD} and V_{SS}. This voltage is then compared to a sawtooth signal in an analog comparator. Since the output of the comparator is either V_{DD} or V_{SS}, the voltage sent to the SR latch appears to be a duty-cycle modulated clock signal. The one-shot clock will set the SR latch output to V_{DD} when high and the signal coming from the PWM comparator will reset the output to V_{SS} when high. This orientation effectively inverts the PWM signal, so the terminals of the comparator must be oriented accordingly. The output of the latch is then fed into a gate driver circuit that will produce non-overlapping clocks, implement maximum duty cycle logic, drive the transistors' gates with minimal delay, and turn off the boost converter when sampling the open-circuit voltage. The clocks need to be non-overlapping to ensure the boost converter switches are never on simultaneously, which can drain the output capacitor's voltage and cause other undesirable behavior. This mode of operation is active when the output voltage exceeds 900mV + 10*$V_{hysteresis}$, where $V_{hysteresis}$ is the amount of hysteresis developed in the hysteretic comparator. For this application, this value in total is 925mV because the hysteresis value is 2.5mV. To exit this mode of operation, the voltage at the output must be below 900mV - $V_{hysteresis}$ = 875mV.

3.1.1.2 Maximum Current Mode

This mode of operation is the mode that takes over when the voltage at the output is below a reference voltage. This is because the capacitor in this condition needs to be charged by the boost converter. In this scenario, the load is disconnected by the decision logic block connecting the load to the boost converter and the capacitor consumes all the available current (except for leakage current and quiescent current consumed by the feedback resistors). Equation 3.2 shows the relationship between the capacitor's voltage and the current provided by the boost converter. This equation indicates that the voltage across the capacitor increases linearly with time assuming a constant current. It also shows that, for higher currents, the capacitor will reach a constant voltage more quickly than for lower current cases. Thus, the motivation to maximize current provided to the capacitor when the capacitor needs charging is clear.

$$V_{cap} = \frac{I \cdot t}{C} \qquad (3.2)$$

This method could easily be implemented alongside the constant voltage method because the same circuit blocks were required. Thus, the only change required to switch between the two modes was to select different reference values sent to the error amplifier. Multiplexors controlled by the output of a hysteretic comparator comparing the output with the 925mV reference were used for this purpose.

The way in which this method performs the impedance matching that results in maximum current being sent to the output is by regulating the input voltage to half of the open-circuit TEG voltage. Thus, the open-circuit voltage must be sampled, and the input voltage is monitored. When the input is equal to half of the open-circuit voltage, the boost converter is impedance matched to the series resistance of the TEG. This ensures the maximum current is flowing to the

capacitor. Shown below in Figure 3.2 is a plot created with semi-ideal components comparing the use of only constant voltage mode to using both modes. The addition of the maximum current mode clearly decreases the amount of time the circuit takes to charge the capacitor.

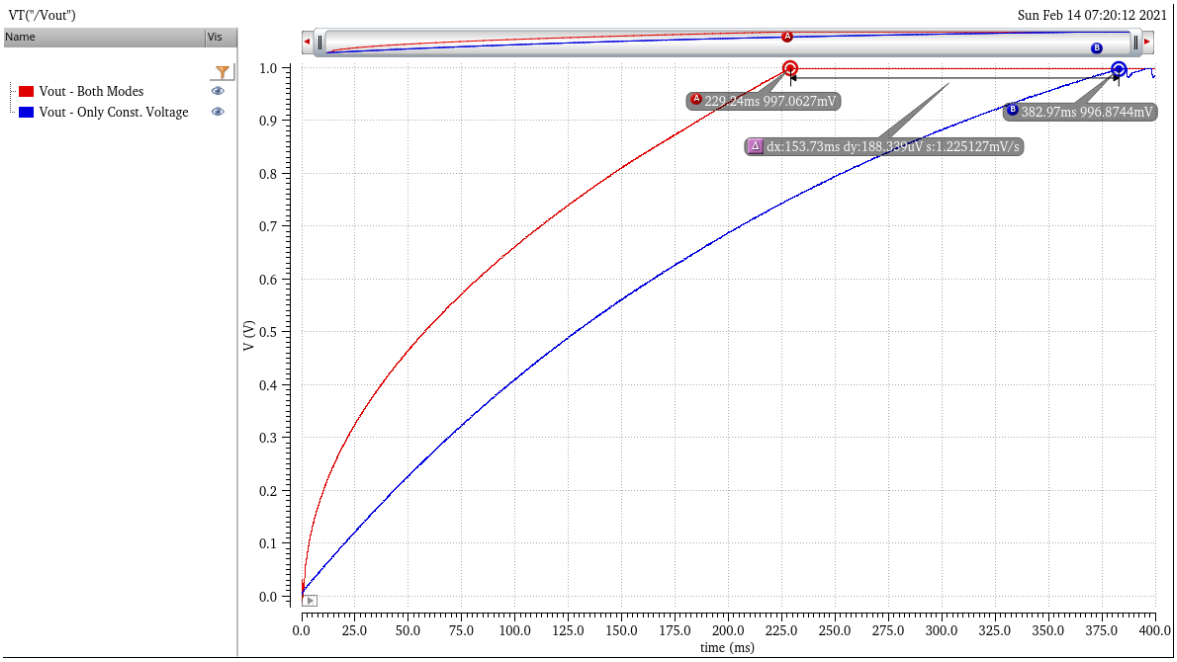

Figure 3.2: Speed Demonstration for Maximum Current Mode

The modes of operation can be expressed in the form of a flow chart. Figure 3.3 shown below displays the modes of operation with the values needed at the output to change between each mode.

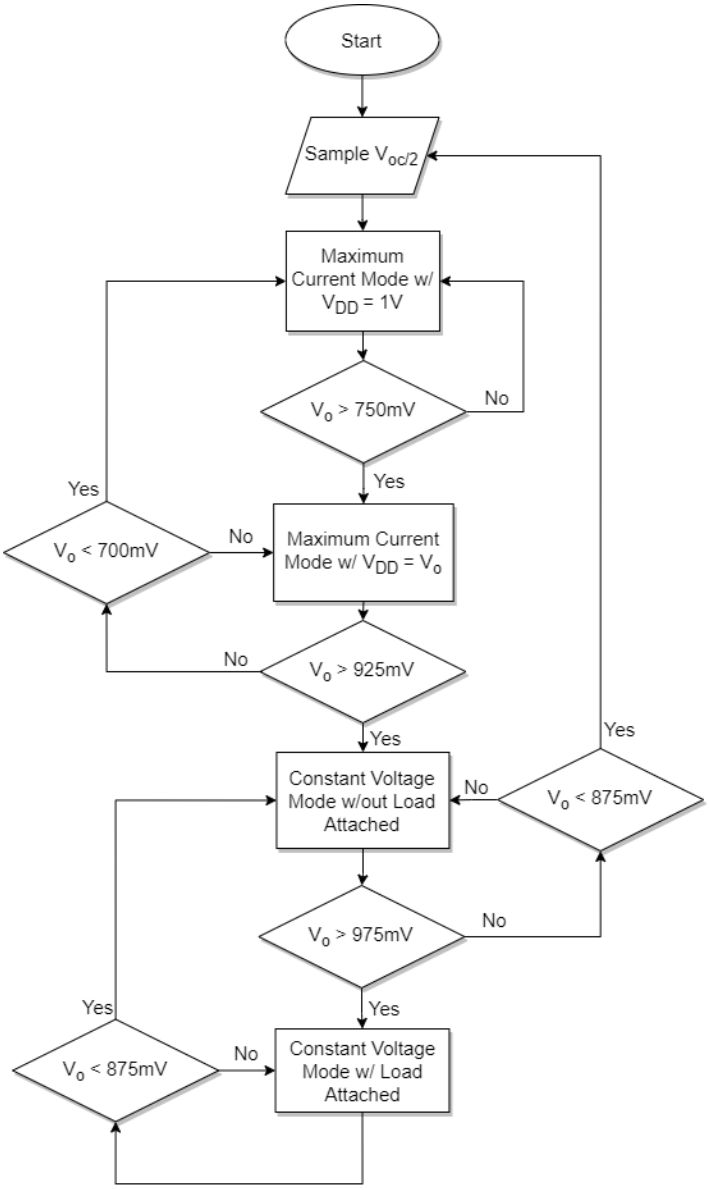

Figure 3.3: Mode Selection Flow Chart

3.2 Circuit Blocks

3.2.1 Open-Circuit Voltage Sampling Circuit

Since the maximum current mode requires a reference equal to half of the open-circuit voltage in order to perform the impedance match, the open-circuit voltage needs to be regularly sampled. This required the development of a dedicated one-shot circuit that would fire every time the

circuit switched from constant voltage to maximum current mode and upon startup. The one shot turns on a switch connected to a storage capacitor so that the sampled voltage is stored in the capacitor. The sampling only occurred in these cases because only the maximum current mode requires this reference. Furthermore, the duration for which the reference will be needed is on the order of a few hundred milliseconds, which is not very long. The time for which the reference I needed is determined by the length of time in which the capacitor will be charged. Therefore, the size of the capacitor is the factor that will determine how long the reference will be needed. Because the capacitor is expected to be able to be charged within 1 second, it was determined that the voltage only needed to be sampled once for adequate performance. An improvement to this research would be the addition of circuitry that sampled more often to ensure the leakage from the storage capacitor is negligible. This could potentially be realized using a digital up-counter in place of the one-shot. This could be done by using the oscillator as the clock for the up-counter of *n* bits. The output of the counter could be compared with a reference set to *n* 1's in a digital comparator. For all cases where the output of the counter is less than the reference, the output should be low. For the equal to case, the output should be high. This effectively creates a duty-cycle modulated pulse that can function as a one-shot. The number of bits will determine the width and frequency of the one-shot. This will need to be fine-tuned to be greater than 4 or 5 time constants for the $V_{oc/2}$ storage capacitor and voltage divider combination. This will ensure the capacitor will be nearly fully charged each sample cycle.

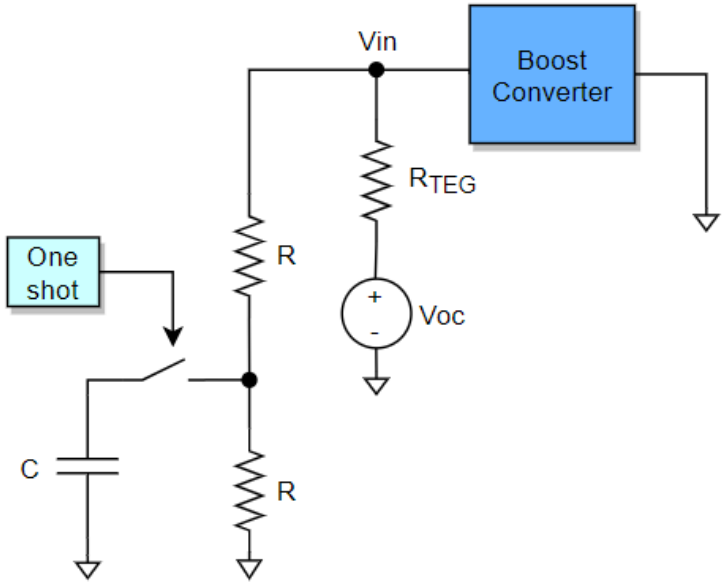

Figure 3.4: Open-circuit Voltage Sampling

The dedicated one-shot circuit opens the boost converter's switches and closes a switch connected as shown in Figure 3.4. This allows for current to flow from the resistor divider holding the $V_{oc/2}$ value onto the storage capacitor. Note that the resistors in Figure 3.4 must be sized equally in order to get a division of ½. Furthermore, these resistors will consume quiescent current, so they should be large. For this application, these resistors were selected to be 1MΩ each.

The truth table shown in Table 3.1 was used to model the behavior of the one shot circuit. Note that φ_1 here is the signal that controls which mode of operation the circuit is in as shown in Figure 3.1.

Table 3.1: One-shot truth table

Φ_1	Φ_1 + Delay	Clock Out
0	0	0
0	1	0
1	0	1
1	1	0

This circuit will set V_{sample} to V_{DD} when:

1. φ_1 either changes from a digital "1" (V_{DD}) to a digital "0" (ground voltage), or
2. When the circuit starts up (output voltage = 0V)

The truth table above can be implemented using a single NOR gate with an inverter to supply the delay. This is shown in Figure 3.5. To increase the delay such that the output pulse was wide enough to charge the capacitor in Figure 3.4, a string of inverters was used in the final application along with grounded capacitors at each inverter's output node.

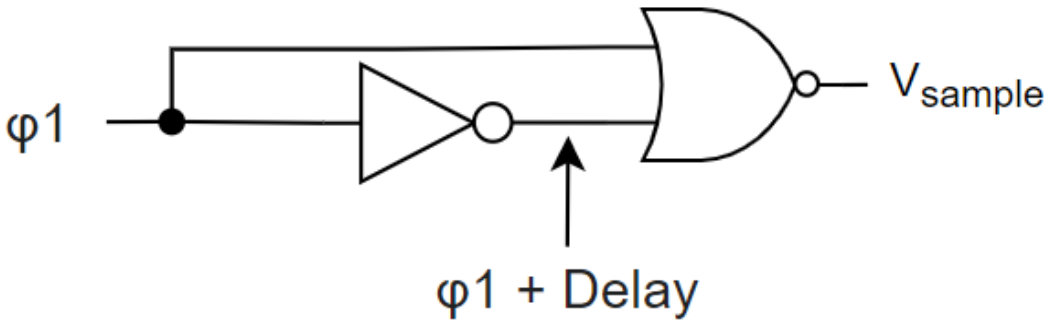

Figure 3.5: One-shot Circuit for Voc/2 Sampling

The circuit will fire when φ_1 changes from 1 to 0 because the delay through the inverter will exceed the delay through the wire. This means that the first input of the NOR gate will be 0

before the second input the NOR gate, which is connected to the output of the inverter, changes to a 1. This will allow for a brief window of time where the inputs to the NOR gate are both 0, making V_{sample} a 1 for the duration of the inverter delay. For startup, both inputs of the NOR gate are initially 0 since the gates will have just turned on. This will again allow for a brief window of time for the output to be a 1.

One consideration for the design of this block is the drive capability of φ_1. To ensure the one-shot does not fire when the mode changes from maximum current mode to constant voltage mode, the delay along the inverters must be higher than the delay to turn on the NOR gate's other input. To ensure this is the case, a chain of 4 inverters was designed to drive the circuit as discussed in section 3.3.2.2.

The delay block itself is comprised of an odd number of inverters. Figure 3.4 shows one inverter, but, in order to increase the delay, multiple inverters were stringed together. After finetuning the delay to be able to sample for at least 5 time constants (R_{switch}*$C_{storage}$), the number of inverters used was 5. This maintained the same logic as with using one inverter while simply adding delay between each stage. The storage capacitance was set to 10pF to maintain the sampled voltage for the appropriate amount of time. Additionally, a capacitor was added to the output node of each stage. These capacitors were set to around 780fF. This again came from finetuning the amount of delay needed to appropriately sample the open-circuit voltage. Future work may be able to reduce the amount of capacitance needed both with the storage capacitor and with each inverter delay stage. One potential way in which this could be done is to sample more often, as was expressed earlier. If sampling occurs more frequently, the size of the storage capacitor could be

reduced by multiple orders of magnitude. With a smaller storage capacitor, a smaller delay within the one-shot circuit would be needed to adequately charge the capacitor since the time constant would decrease proportionally to the decrease in the capacitor's size. Thus, by sampling more often, both the delay capacitors and the storage capacitor could be dramatically reduced in size.

3.2.2 Clock Logic and Gate Driver

3.2.2.1 Non-overlapping Clock Generator

The non-overlapping clock generator is the foundation of the gate driver. Figure 3.6 provides a look at the design of the block. The oscillator's output signal is fed in as an input and produces two unique clock signals for the PMOS and NMOS switches. Figure 3.7 displays the transient waveforms of these output signals ("Qn" and "Qp") and their inverses. Notice the dead time between the "Qn" and "Qp" signals, ensuring that the PMOS and NMOS switches are not on active at the same time.

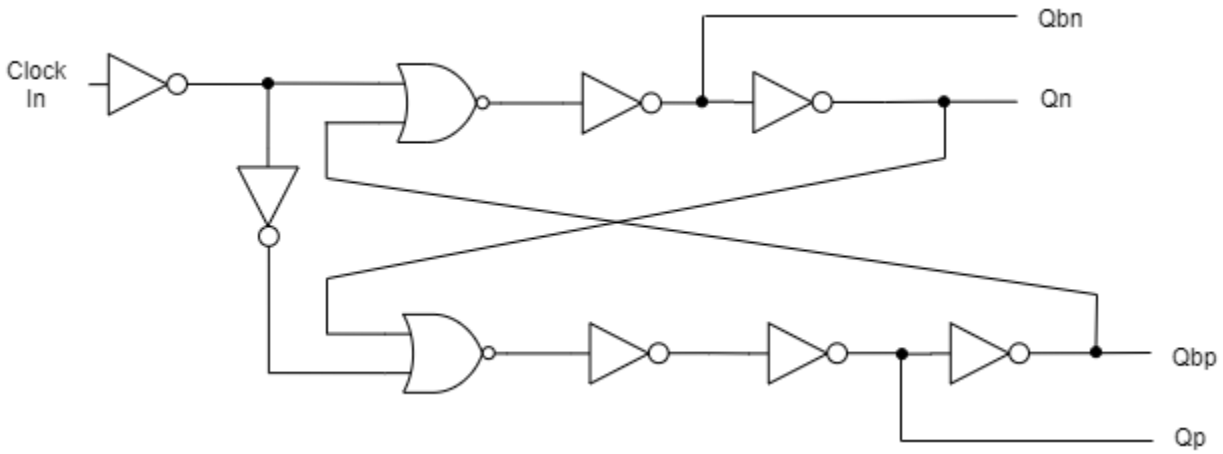

Figure 3.6: Non-overlapping Clock Generator Cadence Schematic

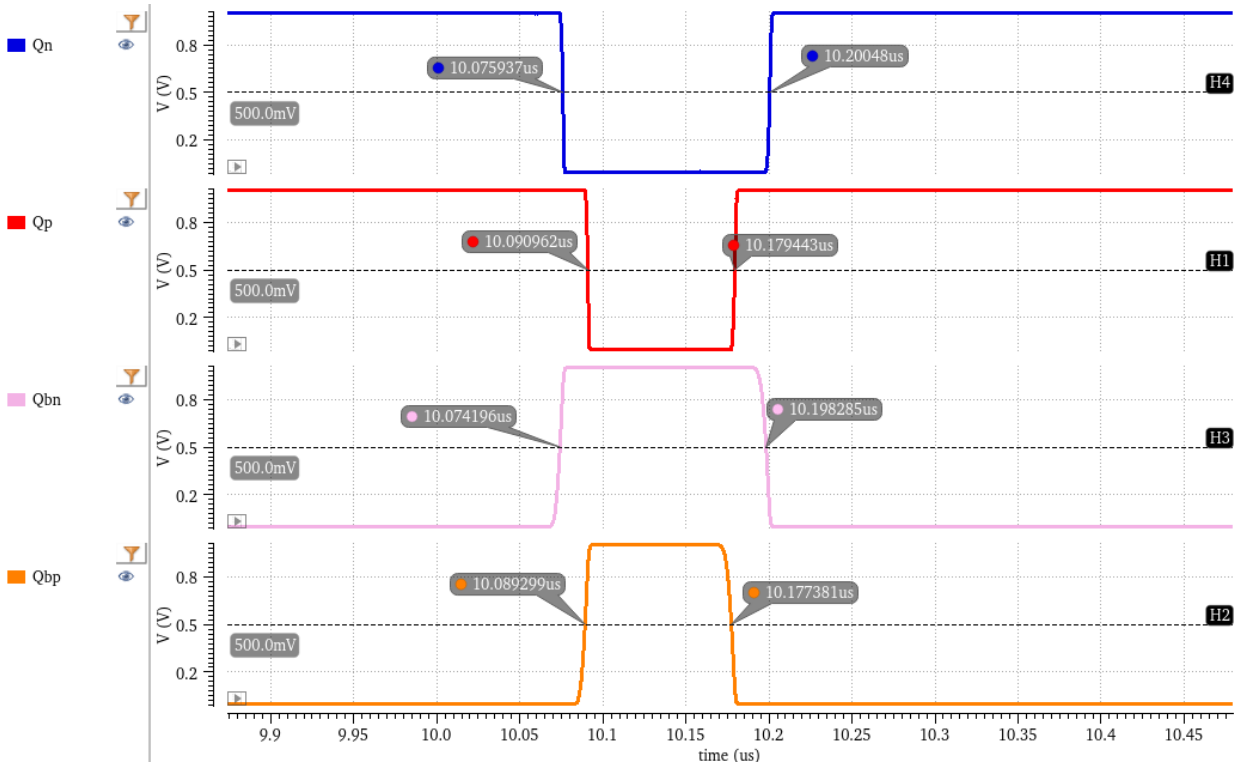

Figure 3.7: Non-overlapping Clock Transient Output Waveforms

3.2.2.2 Gate Driver

The gate driver circuit is responsible for minimizing the delay in turning the switches on and off. This is done by using an even number of inverters sized by a factor n, such that each stage is sized as n^{i-1}, where *i* is the current stage number. This was necessary because the switches had to be large to reduce the switching resistance, resulting in a large gate capacitance. The equation used to design the number of stages and the stage ratio *n* is shown in Equation 3.3 below.

$$n = \left(\frac{C_{out}}{C_{in}}\right)^{\frac{1}{x}} \text{ [3]} \qquad (3.3)$$

The C_{out} term refers to the gate capacitance of both the NMOS and PMOS devices. Since these values were different for both NMOS and PMOS, the stages had to be designed separately. The C_{in} term refers to the input capacitance of a buffer sized at 1. This means this is the standard inverter size for the process used where the NMOS and PMOS are sized such that their resistance

is approximately equal when conducting. To design the driver, a nominal number of stages was chosen, and the ratio was calculated to the nearest integer. For the CMOS process used in this application, a stage ratio of 4 for NMOS and 5 for PMOS was used with 4 stages in both cases. This ensured the minimal delay in driving the large capacitances seen at the gate of both switching devices.

3.2.2.3 Maximum Duty Cycle Logic

The maximum duty cycle logic was necessary to prevent a signal with 100% duty cycle, effectively a DC signal, from being sent to the switches in the boost converter. This allows for the boost converter to operate when the amplified error voltage is above the sawtooth wave's peak value. The logic here is simple in implementation: an inverter and NOR gate. This configuration is shown in Figure 3.8 below.

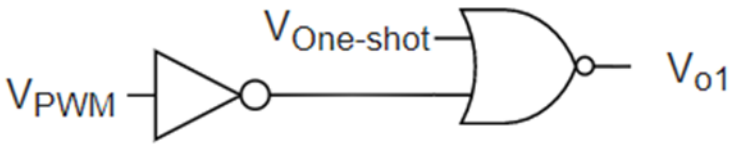

Figure 3.8: Maximum Duty Cycle Logic Circuit

The circuit accepts the input V_{PWM} directly from the output of the SR latch. Whenever the one-shot signal is high, the output V_{o1} will be low regardless of the value of V_{PWM}. This is because the circuit implements the below logical expression shown in Equation 3.4:

$$V_{o1} = \overline{\overline{V_{PWM}} + V_{One-shot}} \tag{3.4}$$

An improvement to this project could be the addition of minimum duty cycle logic such that the operation of the circuit is protected from both ends of the spectrum of the duty cycle.

3.2.3 Sawtooth Generator

The sawtooth waveform generator is a block used as an input to the PWM comparator. The output of the comparator is the duty-cycle modulated pulse that can be used to control the boost converter's gain. The reason a sawtooth signal was used is due to its linear waveform. The ramping voltage of the sawtooth allows for a comparison with the error voltage such that the comparator will output a pulse that is high or low for the time in which the output voltage of the error amplifier is higher than the ramp depending on which input the sawtooth is connected to. This is what physically produces the duty cycle of the output clock signal that is processed and sent to the boost converter's switches.

The circuit topology used for this block was simply a current source, capacitor, and n-type transistor used as a switch. This is shown in Figure 3.9. The current source charges the capacitor's voltage linearly while the switch connected to ground is off. When the switch is turned on, the voltage across the capacitor drops to around zero. When the one-shot clock is used as the gate controller for the switch, the output waveform appears as a sawtooth ramp signal. Note that the one-shot clock here is not the same one-shot that was used for the $V_{oc/2}$ sampling. This signal was produced by the oscillator block described in other sections of this paper.

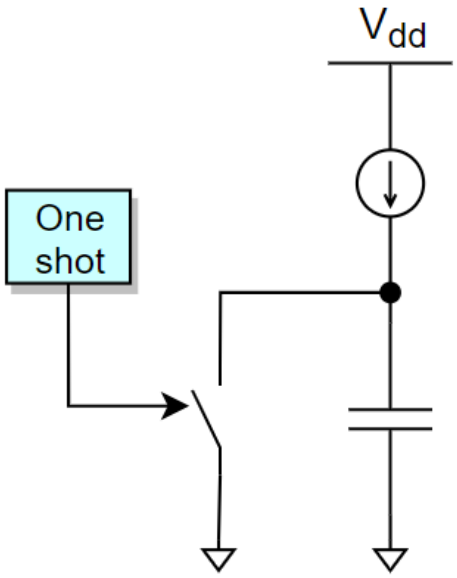

Figure 3.9: Sawtooth Generator Circuit

To maintain low power consumption, the current source had to use a small amount of current. The relationship between the voltage on the capacitor with the value of the current source is relayed in Equation 3.2. The voltage is a linear function of time assuming a constant current source, which is the desired behavior of this circuit.

One design consideration to mention for this block is the peak value of the sawtooth signal. If the sawtooth has the possibility to saturate to V_{DD} given process variation or other fluctuations, the boost converter may not be able to regulate itself appropriately. This is because the output voltage of the error amplifier can range from V_{SS} to V_{DD} to represent the necessary value of the duty cycle to regulate itself appropriately. However, if the sawtooth also ranges from V_{SS} to V_{DD}, the maximum duty cycle will be limited to a value that may be too low for the boost converter to properly regulate itself. Thus, keeping the sawtooth wave below V_{DD} is preferable. This, however, incurs the issue of being able to send a DC signal to the boost converter rather than a

clock with a duty cycle. This occurs when the amplified error voltage is above the sawtooth. To avoid this, maximum duty cycle logic was built and is discussed elsewhere in this document. By limiting the duty cycle, the case in which a DC signal is sent to the switches in the boost converter never occurs if the DC signal was V_{DD}. The case in which the DC signal is V_{SS} was not designed for since this boost converter typically never operates with a low duty cycle.

3.2.4 Error Amplifier & Loop Compensation

The error amplifier is a block along the feedback path used to amplify the error between a reference signal and a given input signal. Along with the PWM generator, this circuit helps regulate the value of one input signal to a given reference. This can take the form of regulating currents to reference values or, in the case of this research, regulating voltages to reference values. Thus, the error amplifier is the block that will control the loop when implemented properly. In practice, an error amplifier is a high-gain amplifier with differential inputs and a single-ended output. Thus, the amplifier can be implemented as an operational amplifier (op amp) or an operational transconductance amplifier (OTA). In this application, an OTA was implemented. An OTA is

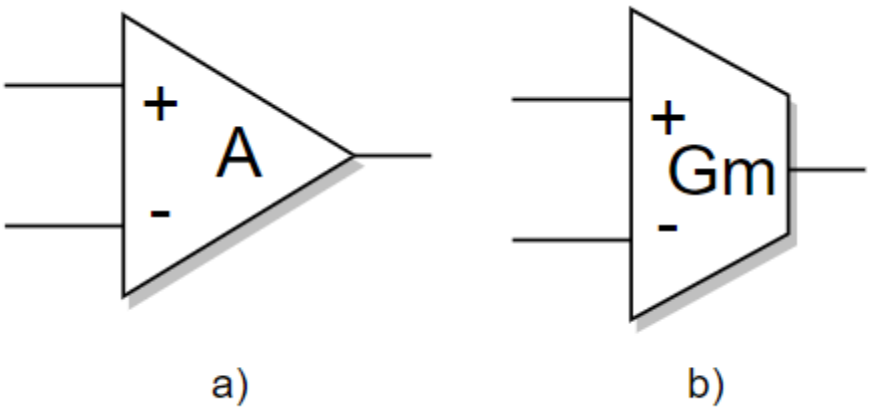

Figure 3.10: Op amp (a) and OTA (b) Block Diagram Symbols

typically seen as an op amp without an output stage. Thus, OTAs have much higher output impedance and can be thought of as producing an output current instead of a voltage. Figure 3.10 shows the symbols for an op amp with voltage gain A in a) and an OTA with transconductance Gm in b). In this application, the load is purely capacitive at DC, so the OTA will perform much like an op amp. Thus, the term op amp will be loosely used to refer to the amplifier designed in this section.

The topology chosen for this application was the 2-stage Miller amplifier with NMOS inputs. This is one of the simplest topologies that can be designed for high gain, which is an important feature of the error amplifier in order to have a fast, responsive loop. The Miller op amp schematic is shown in Figure 3.11. The Miller op amp gets its name from the type of internal compensation it uses to stabilize the amplifier: a capacitance across M5's gate and drain. This splits the two primary poles of the op amp by moving the dominant pole ω_{p1} to a lower frequency. This increases the phase seen at the loop gain's gain bandwidth product (GBW), thus increasing its overall phase margin. More advanced techniques, such as RC compensation or feedforward compensation, can be used in this amplifier as well, but it was determined to be unnecessary for this application.

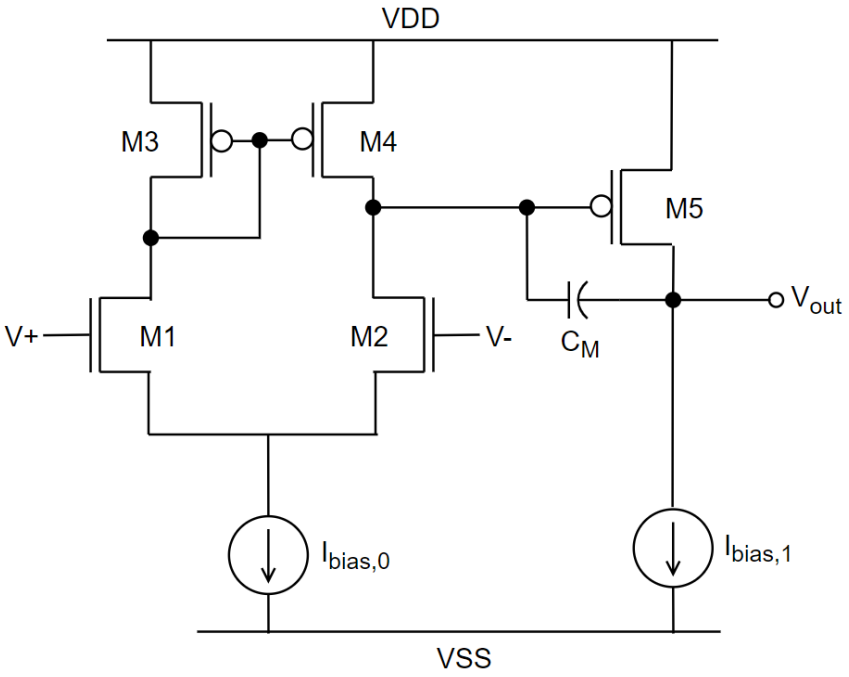

Figure 3.11: Miller Op Amp Schematic

To design the error amplifier, certain specifications were attained by first performing loop simulations with different values for parameters such as open-loop gain. These parameters were simulated by modifying the gain parameter of a voltage-controlled voltage source block from Cadence's analogLib in place of the error amplifier. The most critical parameters for the amplifier were gain and phase margin since these would determine the amplifier's ability to regulate the loop and remain stable under varying conditions. The minimum value that was determined for the amplifier's gain was 54 dB, or approximately 500 V/V. However, higher gain in this block is typically desired to increase the speed of regulation. The phase margin was challenging to set a direct target for, since the loop gain is not trivial to characterize or measure for a switching regulator. Furthermore, the amplifier had local compensation (Miller compensation) and loop compensation, which is shown in Figure 3.12. The targeted specification, therefore, was to ensure the amplifier's open-loop response showed phase margin

greater than 0º since this would ensure that the amplifier, isolated from the loop compensation, would remain stable for all passive feedback configurations where the feedback factor, β, is less than 1.

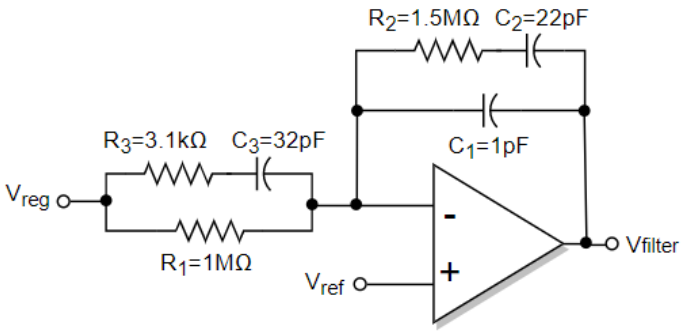

Figure 3.12: Error Amplifier with Loop Compensation

The amplifier's gain is defined by Equation 3.5 below.

$$A_{v0} = g_{m1,2}g_{m5}(r_{ds2}||r_{ds4})R_x \tag{3.5}$$

Where R_x is the resistance of the current source supplying I_{bias1}. The amplifier's phase margin and is defined by Equation 3.6.

$$PM \approx 90° - tan^{-1}\left(\frac{GBW}{p_2}\right) - tan^{-1}\left(\frac{GBW}{z}\right) \tag{3.6}$$

The equations defining the location of the second pole and zero are given in Equations 3.7 and 3.8 below.

$$\omega_{p2} = \frac{-g_{m5}}{C_L+C_1} \tag{3.7}$$

$$\omega_z = \frac{g_{m5}}{C_c} \tag{3.8}$$

In Equation 3.7, the value of C_1 is the capacitance at the output node of the first stage. Using these equations and the specifications set earlier, the error amplifier was designed. The resulting open-loop simulation for the upper and lower supply levels is shown in Figure 3.13.

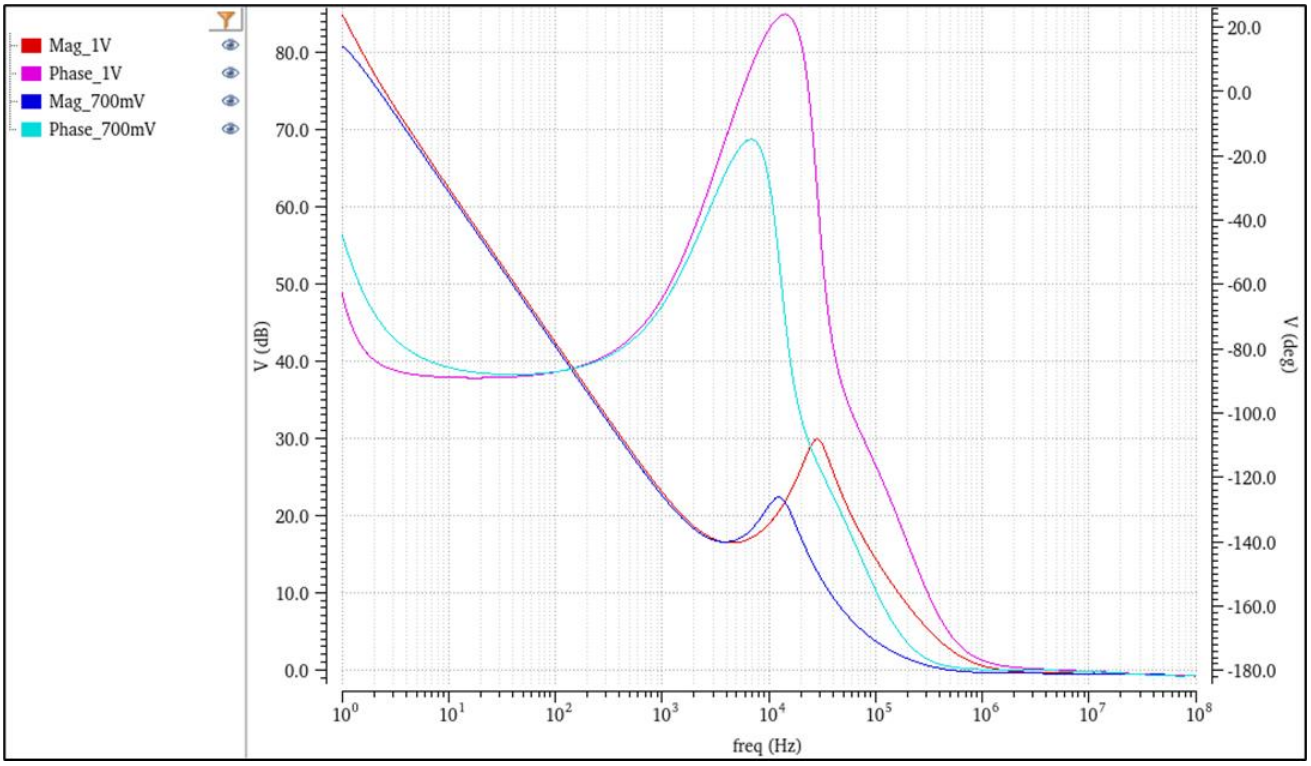

Figure 3.13: Error Amplifier Open-Loop Response

The phase margin at the unity gain frequency is 20º at V_{DD} = 1V and 15.8º at V_{DD} = 700mV. Thus, for all passive feedback applied, the amplifier will be stable. Furthermore, this will be the lowest phase margin that can be seen for this amplifier and will only increase as passive components are added to the feedback path. This is because the amplifier's open-loop response is equal to the loop gain for the unity gain configuration. The gain of the amplifier at DC is over 80dB in both cases, which exceeds the minimal spec of 500V/V.

To design the loop compensation components, the equations from [12] were utilized. These equations are shown below in Equations 3.9 to 3.13.

$$\omega_{p1} \cong \frac{1}{R_1 C_1} \tag{3.9}$$

$$\omega_{p2} \cong \frac{1}{R_3 C_2} \quad (3.10)$$

$$\omega_{p3} \cong \frac{1}{R_2 C_3} \quad (3.11)$$

$$\omega_{z1} \cong \frac{1}{(R_1+R_3)C_2} \quad (3.12)$$

$$\omega_{z2} \cong \frac{1}{R_2 C_1} \quad (3.13)$$

The desired transfer function for the closed-loop magnitude response is shown in Figure 3.14.

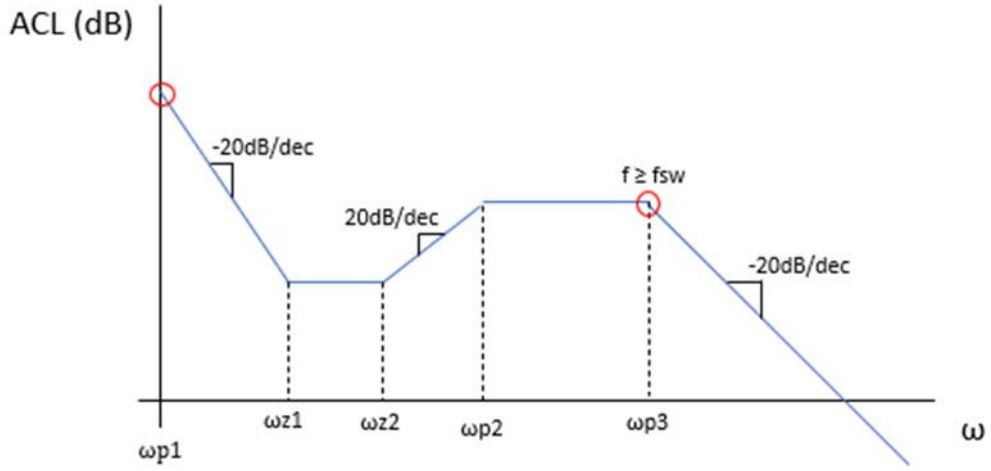

Figure 3.14: Desired Closed-Loop Response

Thus, using the equations and desired transfer function shown above, the values of the compensation capacitors and resistors were calculated. This transfer function has a DC pole, two zeros that reverse the slope to +20dB/dec, and two more poles around the LC pole. This provides higher phase margin at the unity gain configuration and allows for good rejection of higher frequency components that may be present due to noise.

3.2.5 Comparator

The comparator in this application was used to create the PWM signal from the amplified error voltage. This was done by comparing the amplified error with a sawtooth signal. The result

would be a duty cycle modulated signal that was used to turn the switches in the boost converter on and off. The circuit topology used in this application was inspired by [14] but was modified to better suit this application. The topology of the comparator is shown below in Figure 3.15.

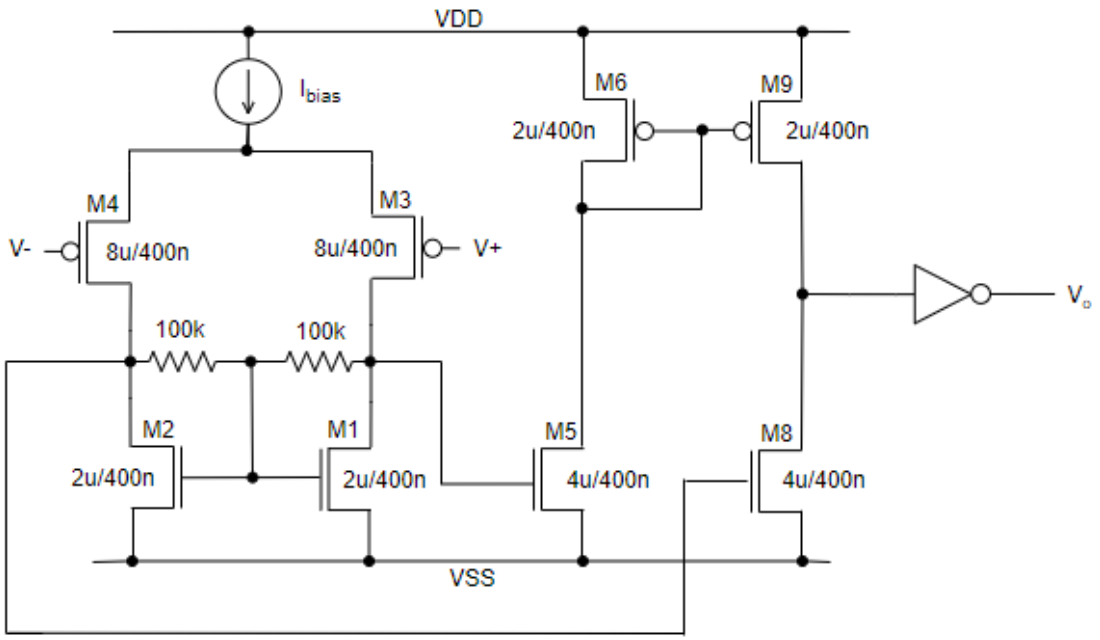

Figure 3.15: Comparator Schematic

The first stage of the comparator is a fully-differential differential pair. Instead of diode-connecting the load transistors M1 and M2, a semi-large resistor is placed between the drain and gate of each device. This provides higher gain because the resistance R is much larger than the $1/g_m$ value that would normally be seen as the load impedance. By increasing the gain of the first stage, the comparator's speed increases. Since this application deals with high duty cycles, the responsiveness and speed of the comparator is necessarily high. An inverter was placed at the output to restore rail-to-rail operation. The second stage is a class AB amplifier that is loaded by a current mirror. This adds more gain, which increases the speed of the comparator.

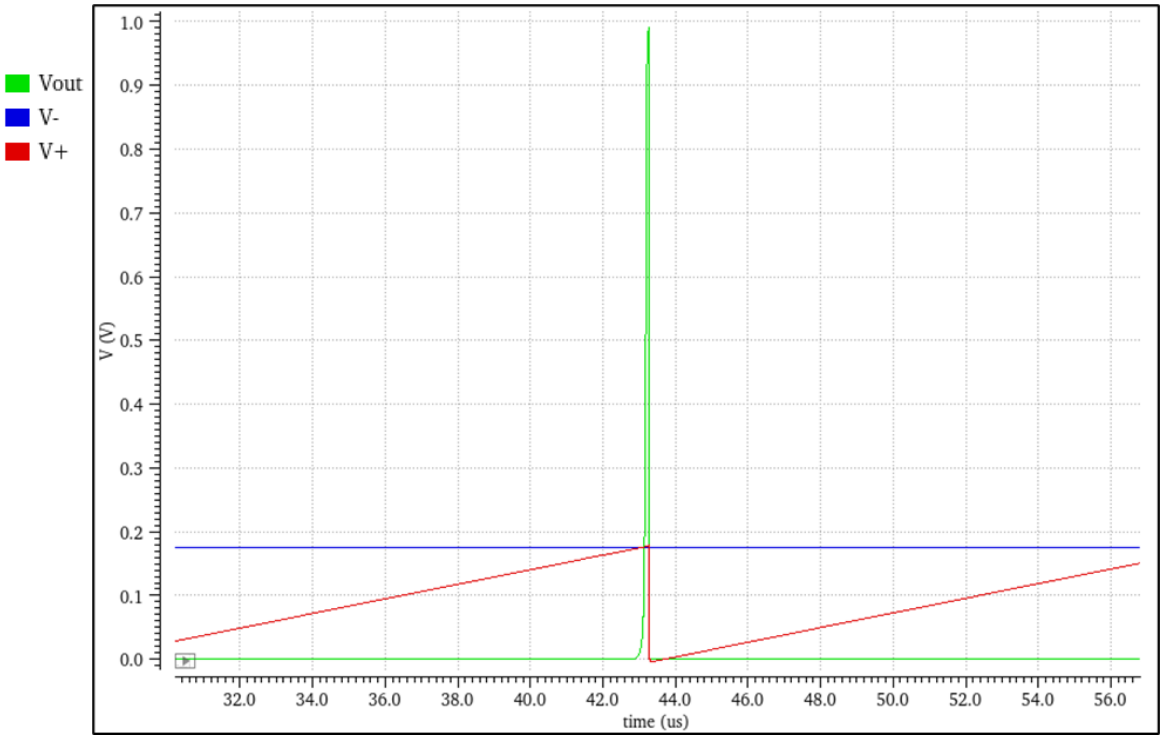

Figure 3.16: Comparator Transient Response

The performance of the comparator designed worsens as the common-mode levels increase past the threshold voltage. This is because the inputs are PMOS, which turn on with input voltages lower than the threshold voltage value (approximately 450mV for this process). Thus, since the sawtooth signal varies from 0V to its peak, the inputs need to be PMOS so that the input devices are always operating. So, the sawtooth signal should be designed to peak below the threshold voltage. An example simulation showing the reaction of the comparator to a sawtooth input is shown in Figure 3.16 above.

3.2.6 Hysteretic Comparator

The hysteretic comparator is a block that compares two input voltages but adds hysteresis to the comparison. What this means is that the current state of the output factors into the value in which the state will change. If the voltage at the output is originally a digital 0, the non-inverting input

will have to exceed the inverting input by an amount equal to the hysteresis value. The reverse is also true for a symmetric hysteretic comparator. The hysteretic comparator for this application was designed to have symmetric hysteresis of 2.5mV. The reason this voltage was this low was due to the nature of the divided feedback in the circuit. Since the hysteretic comparators would be handling voltages that were divided by 10 from the value they represented, the value of hysteresis must also be small. Thus, since the division factor is 10, the 2.5mV hysteresis represents 25mV of hysteresis with the signals it regulates.

The hysteretic comparator built for this application was comparator with PMOS inputs with added positive feedback in the form of cross-coupled NMOS devices. This schematic was derived from the research presented in [15]. These devices served to provide the hysteresis to the comparator. The schematic for the circuit is shown in Figure 3.17 below.

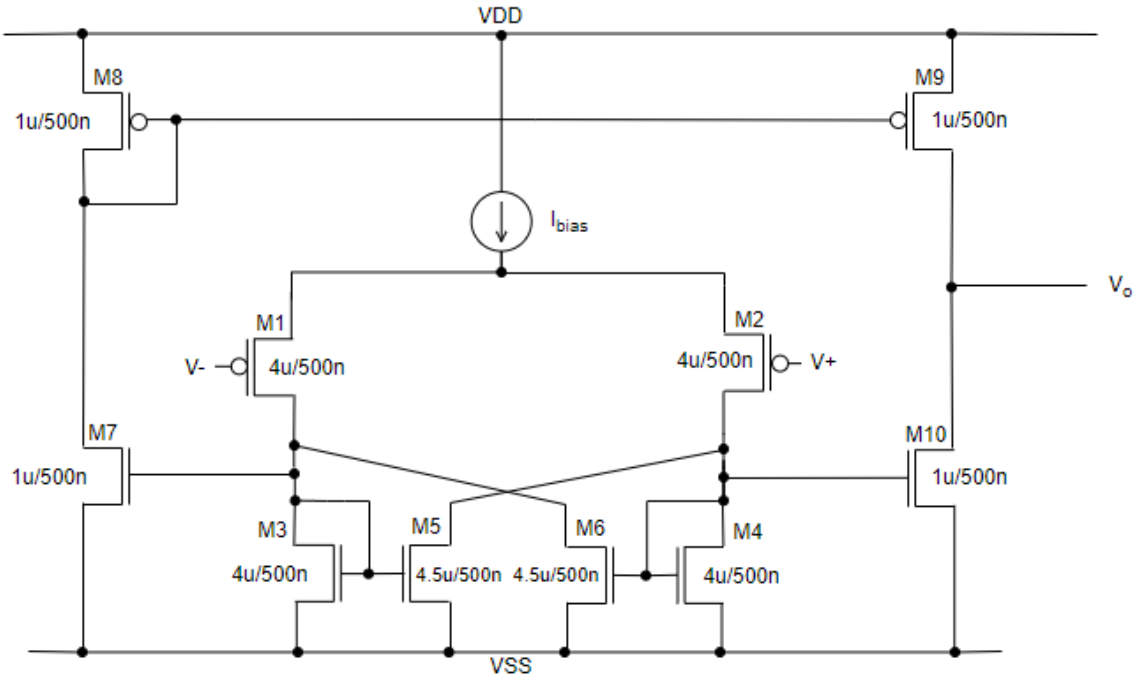

Figure 3.17: Hysteretic Comparator Schematic

The value of the hysteresis is controlled by the ratio of widths between M5:M3 and M6:M4. If the ratio is the same, the hysteresis is symmetric. As the ratio of M5:M3 or M6:M4 increases, the hysteresis value also increases. Thus, by modifying the aspect ratio of the NMOS devices, the amount of hysteresis can be easily tailored. Figure 3.18 below shows a DC hysteresis curve of the above comparator with V_{DD}=1V.

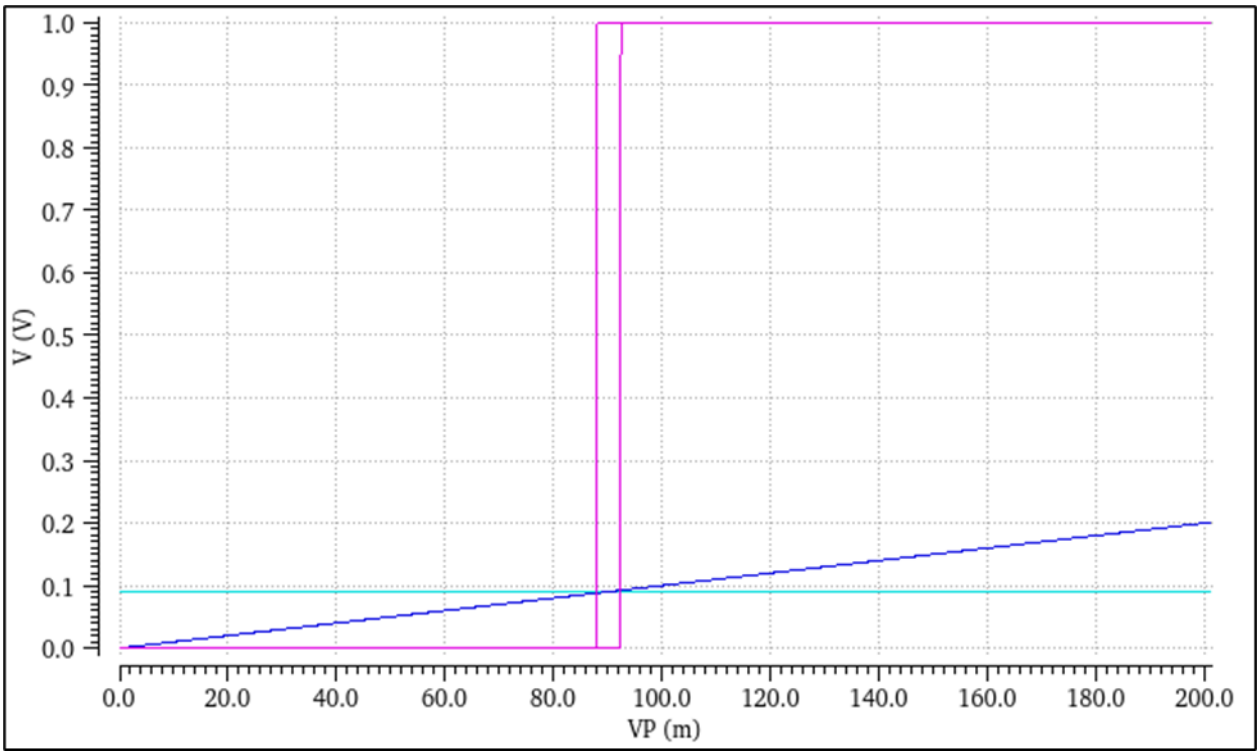

Figure 3.18: Hysteresis Curve

3.2.7 Buffers

In this application, buffers were used to fix two major issues: the loading effect on the compensation components and the leakage from the capacitor holding the voltage output of the open-circuit voltage sampling block. For the first case, it became apparent that the impedance of the feedback division resistors was negatively impacting the applied compensation. The location of the feedback resistors and compensation are shown in Figure 3.1 earlier in this document. In many applications, the feedback resistor contributing the feedback division (this is R_{FB1} in Figure 3.1) is typically incorporated as a component in the compensation. However, since this application uses multiplexors to choose which inputs to regulate, the compensation had to be placed after the multiplexor output to have the same compensation for both modes of operation. Thus, the buffer was needed to remove the loading effect of the feedback resistors from the compensation scheme.

The design of each buffer was the same: a PMOS source-follower stage loaded by a PMOS current source. This allowed for device operation within the saturation region at low input common-mode levels, which was what was expected due to the feedback factor being equal to 1/10. For most cases, the inputs of the buffers would never rise above 100mV. Thus, since the supply voltage minimum is 700mV, and the threshold voltage is approximately 450mV, there is no risk of saturating the buffers with this input common-mode level. The schematic for the buffer is shown in Figure 3.19. Each buffer was designed in this configuration.

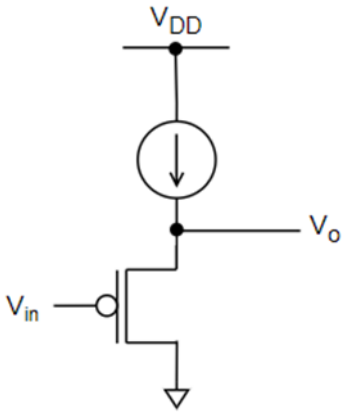

Figure 3.19: Buffer Schematic

3.2.8 Current and Voltage References

The references in this circuit were crucial to the operation of the boost converter. Four voltage references and one current reference were necessary to operate every block. The biasing for the circuit was completed by assuming two pad inputs: one current and one voltage. The current reference was mirrored through both PMOS and NMOS devices to bias the amplifier and comparators and other blocks. The voltage references were developed by using a voltage divider on the input voltage. This ensured the voltages produced depend only on the ratio of resistance

values rather than the value of the resistors. This is more robust than relying on any component value that can change with process variation or temperature. However, future work stemming from this research would benefit from having a bandgap reference for both the current and voltage references. This will remove the necessity to have external references. Also, the references developed by the bandgap circuits will be reliable and more immune to process variation and temperature.

The circuit used to generate the references is shown below in Figure 3.20.

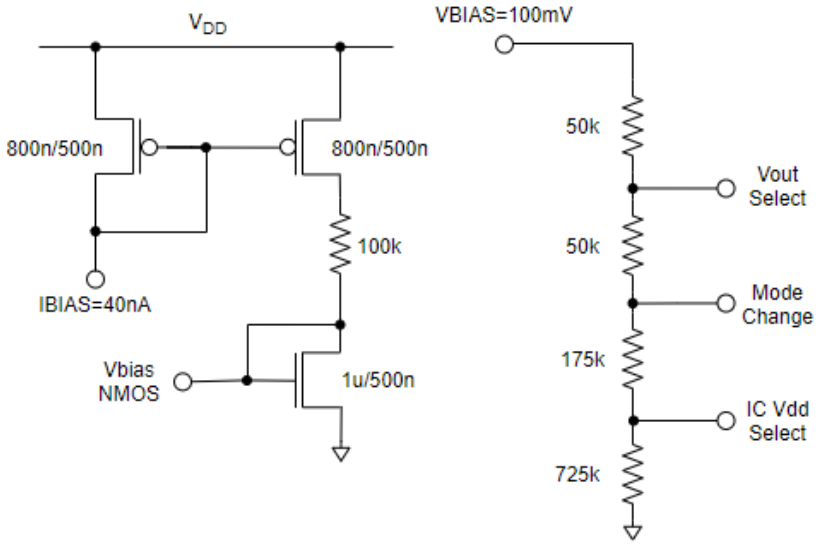

Figure 3.20: Reference Generation Circuit

3.2.9 Voltage Supply Decision Logic

The decision logic block deciphers whether the voltage on the super capacitor is at a high enough level to supply power to the control circuitry and/or the Biomonitor. Two different decisions are made using two pairs consisting of a multiplexor and hysteretic comparator. One pair evaluates whether the feedback voltage (“VFB”) indicates that the super capacitor voltage is above the minimum required supply voltage of 700 mV. If so, the output of the comparator triggers the

multiplexor to switch its output from the Biomonitor's fixed battery to the boost converter output, which is sent to the feedback system as the supply voltage for all blocks. At this point, the system is self-sustaining and will not consume any additional power from the fixed battery. The other decision pair makes the same evaluation with a higher reference and will switch the Biomonitor's supply from the fixed battery to the boost converter output. The decision logic will maintain this state unless the super capacitor voltage drops too low, in which case the power supply will revert to the fixed battery. Figure 3.21 illustrates the schematic design of the decision logic block.

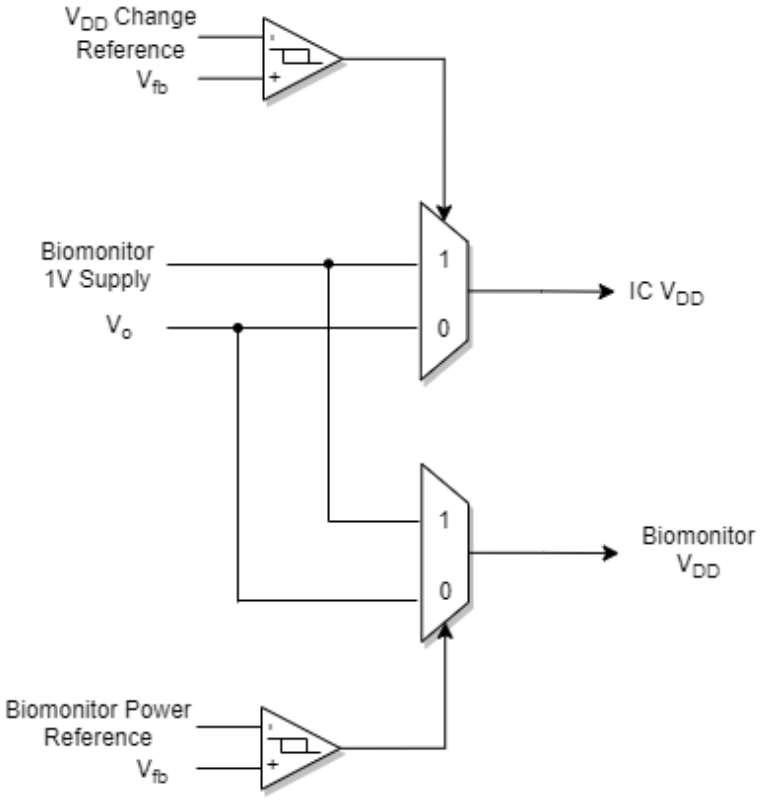

Figure 3.21: Decision Logic Schematic

It's worth noting that the multiplexor used to select the IC's V_{DD} value within this block was designed differently than the other multiplexors in this application. The transmission gates inside of this multiplexor were sized much larger than the other multiplexors' transmission gates. This

was done to reduce the series resistance of the transmission gates. Prior to resizing the devices, the V_{DD} voltage had large spikes that were the result of current being drawn more heavily at the rising edge of the oscillator. Thus, by reducing the drain-source resistance of the transmission gates, the spiking of the V_{DD} voltage was minimized. The switch sizes used were 1µm/180nm with 500 fingers for the NMOS and 2µm/180nm with 500 fingers for the PMOS.

4. PHYSICAL IMPLEMENTATION AND LAYOUT

4.1 Full System Integrated Circuit Layout

Figure 4.1 is an image of the full system layout including pads for input and output signals. Notice that the Cadence rulers define the IC area as a square 1.6 µm. Furthermore, Figure 4.2 displays the LVS check results of the layout confirming that the nets and device properties of the layout match those listed in the schematic.

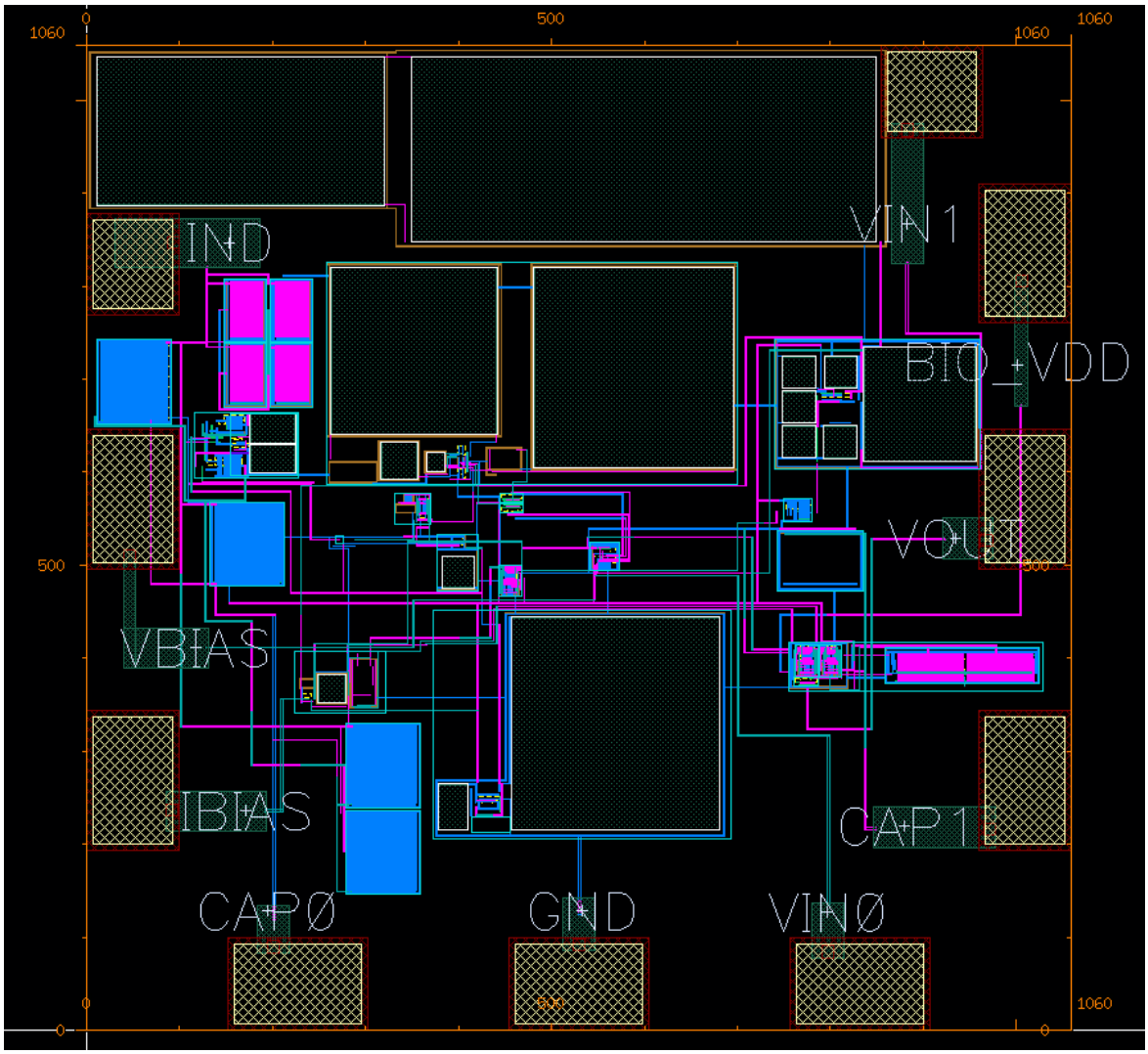

Figure 4.1: Final IC Layout

```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################


REPORT FILE NAME:         Master.lvs.report
LAYOUT NAME:              /home/ugrads/t/thomas99/CAL/Master.sp ('Master')
SOURCE NAME:              /home/ugrads/t/thomas99/LVS/Master.netlist.lvs ('Master')
RULE FILE:                /home/ugrads/t/thomas99/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Tue Apr 20 14:47:07 2021
CURRENT DIRECTORY:        /home/ugrads/t/thomas99/CAL
USER NAME:                thomas99
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                      OVERALL COMPARISON RESULTS


                        ##################
                        #                #
                        #    CORRECT     #
                        #                #
                        ##################


  Warning:  Unbalanced smashed mosfets were matched.
  Warning:  Ambiguity points were found and resolved arbitrarily.

*****************************************************************************************************
                                      CELL  SUMMARY
*****************************************************************************************************

  Result          Layout                      Source
  -----------     -----------                 --------------
  CORRECT         Master                      Master
```

Figure 4.2: LVS Report for the Master Cell

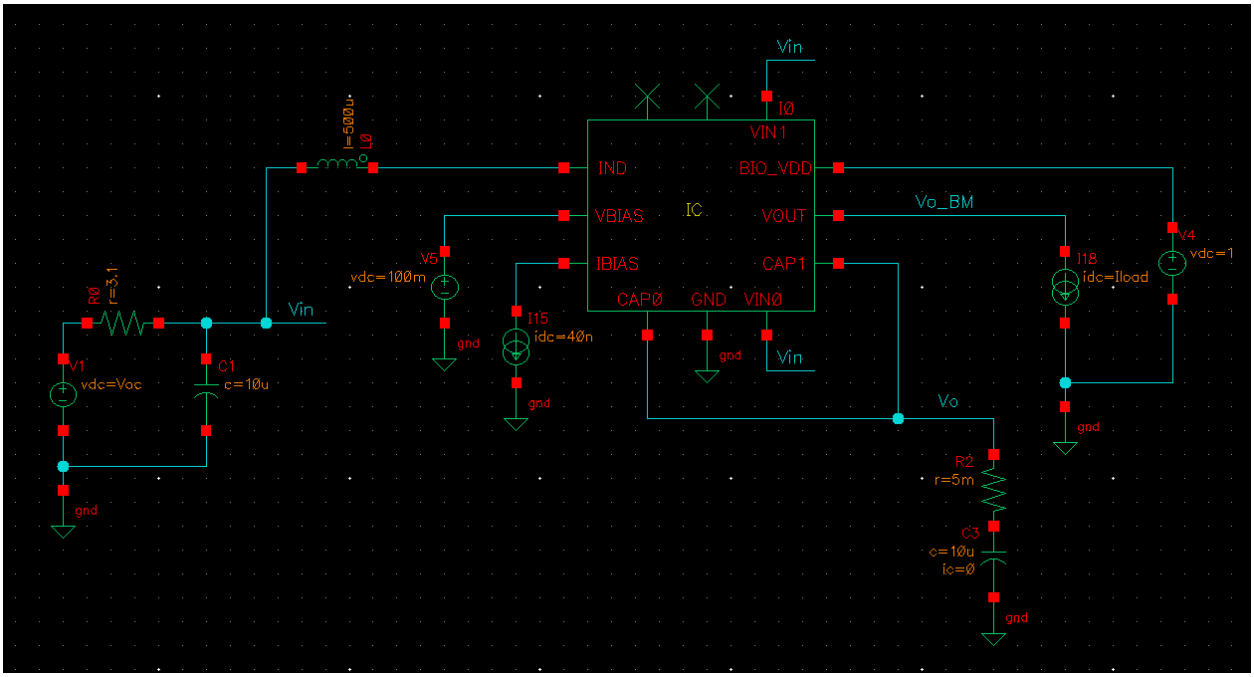

Figure 4.3: IC Component Setup and Connections

4.2 System Results & Performance

4.2.1 Transient Waveforms

This section characterizes the performance of the full system. First, transient waveforms were evaluated at a 1 ℃ temperature gradient, which was used as a worst-case scenario to design the circuit. Figure 4.4 defines the output voltage and shows that the signal regulates to 969.72 mV and drops about 5.17 mV over the course of the steady-state regulation. Though the system is not delivering enough power to reach the target 1 V, it is clear that the voltage is high enough to maintain the state of the decision logic circuit and continue supplying power to the Biomonitor. Thus, the Biomonitor is still able to be powered by the IC for much of the time, with only occasionally needing to supply power to the IC to boost the circuit's output voltage back to the viable region.

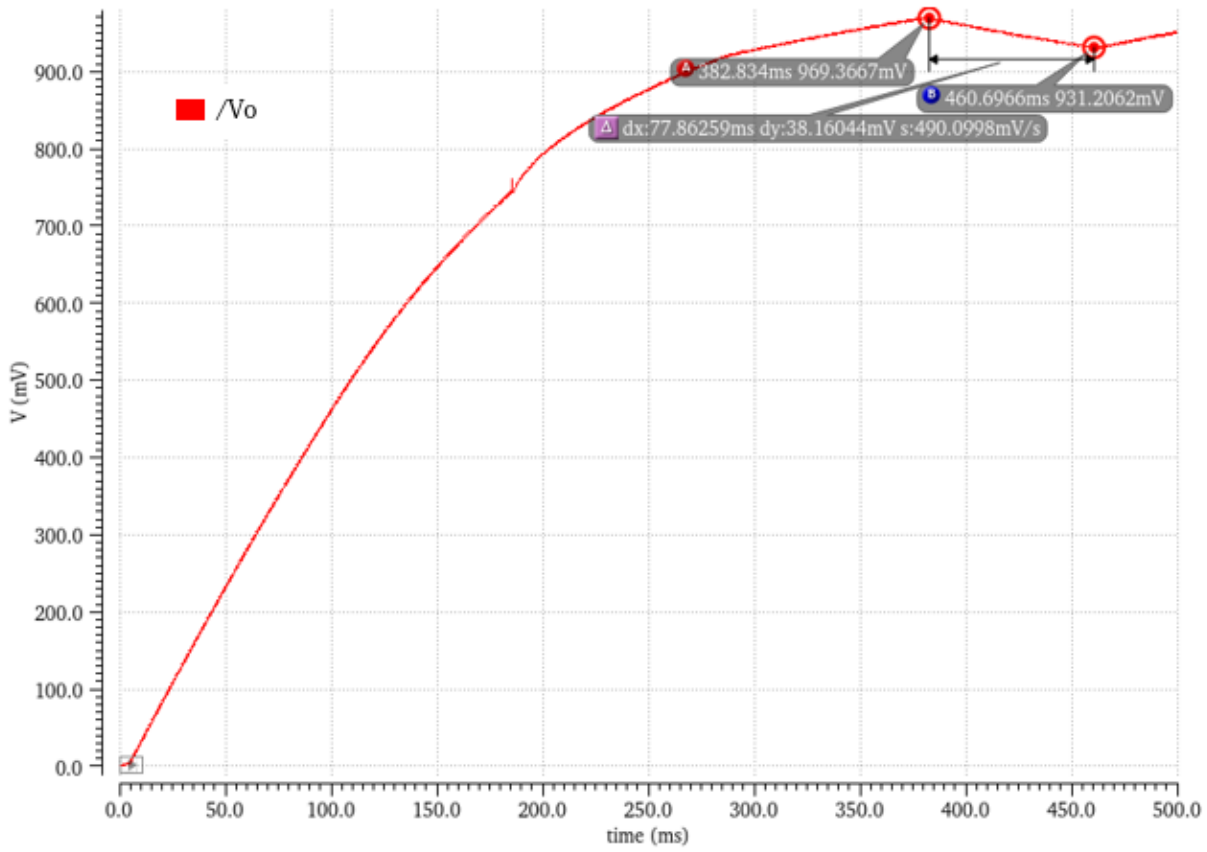

Figure 4.4: Transient Waveform of Output Voltage at 1 ℃ Gradient

In addition, Figure 4.5 offers a look at the effective impedance match seen within the maximum current mode. Note that the impedance matching target for the input voltage is approximately 10 mV in the 1 ℃ gradient case. The initial impedance match is close to 10 mV and continues to oscillate around this value. Until the V_{DD} voltage switches over to the output of the boost converter, the circuit is self-regulating and attempts to impedance match. The reason the input voltage drops is because the reference $V_{oc/2}$ drops over time due to leakage. The reason the change in V_{DD} causes a disruption in the impedance matching is because it causes the error voltage to rise, which then exceeds the peak value of the sawtooth signal.

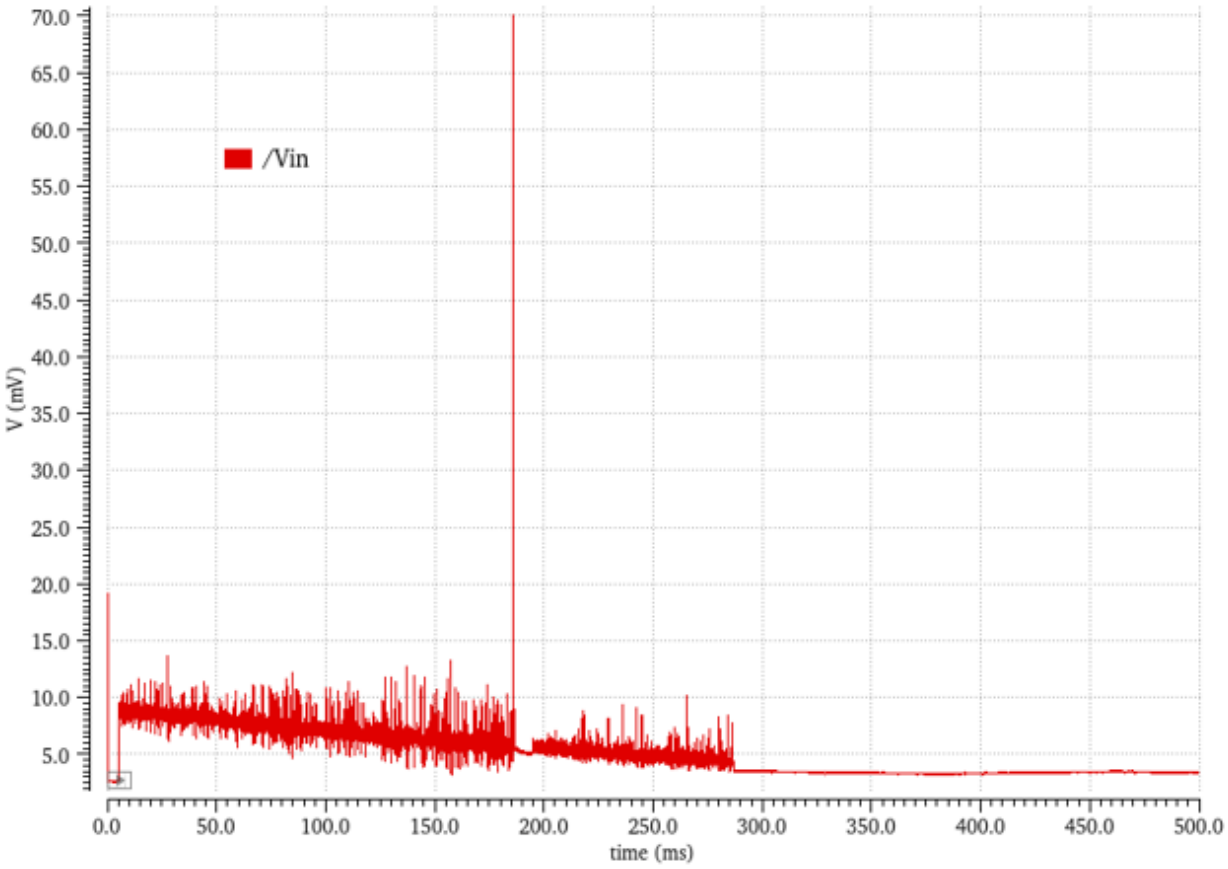

Figure 4.5: Transient Waveform of Input Voltage at 1 ℃ Gradient

The amplified error voltage rises due to the spike in the input voltage. The compensation slows down the response of the system, so the error takes some time to drop back down.

4.2.2 Power Analysis

Table 4.1 defines the total power consumption of each high-level block in the system at both 1 and 2 ℃ temperature gradients. Although the switches in the IC already quite large, improvements on the power dissipation of the circuit would likely begin with manipulation of the CMOS switches to reduce dissipation across the switch resistances. Figures 4.6 and 4.7 show the percentage of the total dissipated power consumed by each of the blocks listed in Table 4.1 at 1

and 2 ℃, respectively, with all feedback components abstracted away under the umbrella of "Control Circuitry".

Table 4.1: Power Dissipation of Major Components

Block	Power at 1 °C (W)	Power at 2 °C (W)
Decision logic	104.1n	112n
Voc sampling	456p	533.6p
Switch driver	1.644u	1.803u
SR latch	773.1p	837.5p
References	78.35n	79.72n
Comparator	2.087u	2.157u
Sawtooth	7.652n	7.771n
Error Amplifer	63.79n	65.32n
Muxes	48.99p	8.712p
Buffer	218n	221.6n
Hysteretic comparator	51.8n	55.39n
Driver	1.138n	1.341n
P switch	2.888u	12.57u
N switch	6.191u	23.14u

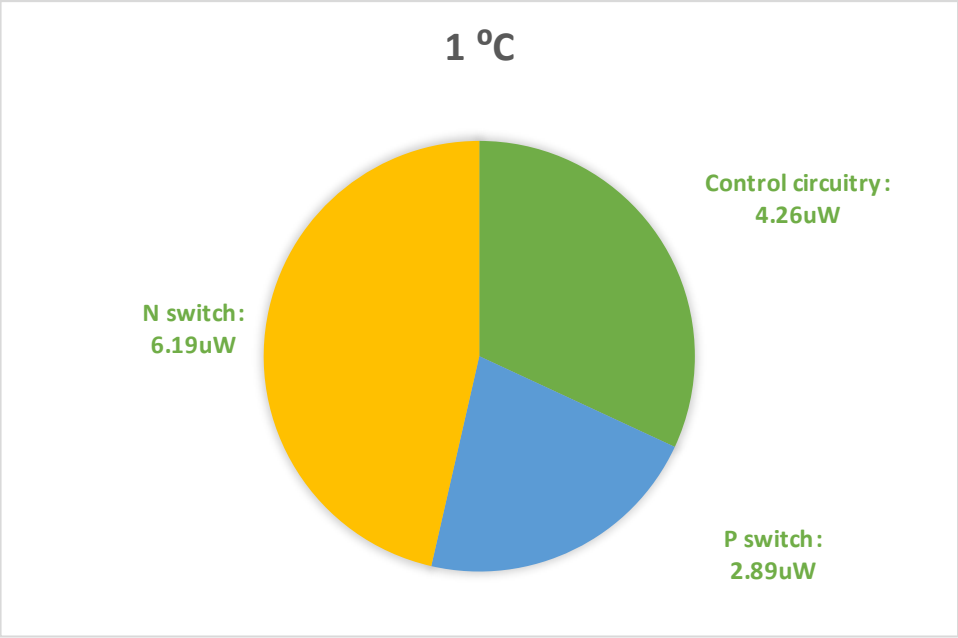

Figure 4.6: Power Dissipation Split at 1 ℃ Temperature Gradient

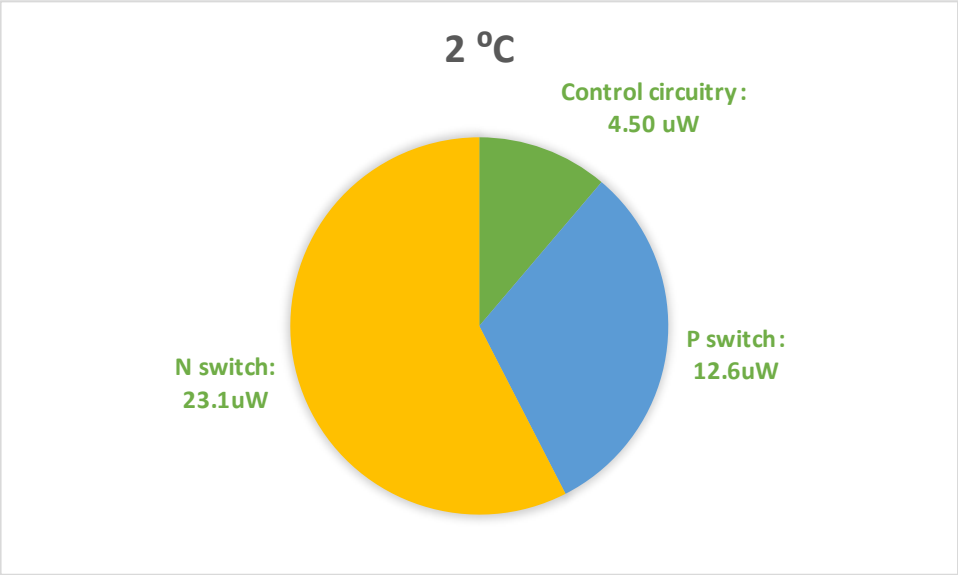

Figure 4.7: Power Dissipation Split at 2 ℃ Temperature Gradient

A primary performance indicator for the boost converter is the power conversion efficiency metric. This metric is the ratio of the maximum power that can be delivered to the load to the input power to the boost converter, whose measurement locations are illustrated in Figure 4.8. To get to the condition where maximum power was delivered, the load impedance had to be adjusted until simulation results showed a static output voltage when steady-state was reached with the load attached. The testbench for this circuit used the schematic-level switches and switch driver, but used ideal controller components to speed up simulation times. To include the power dissipation of the controller components, the power consumption of the controller components was subtracted from the output power value obtained from these simulations. The load impedance that was the minimum value the boost converter could support was found to be 41kΩ. This resulted in a power conversion efficiency of 40.9%. This may seem low, when compared to the typical 80-90% efficiency expected for a boost converter used in high power applications, but was reasonable for the application of this work due to the low power the system

worked with. This is mainly due to the control system consuming proportionally higher power in this design than would be expected for a higher power application. This is because the amount of power the control system would dissipate would most likely not scale linearly with input power. Thus, the amount of power subtracted due to the control system would be mostly negligible in high power applications, whereas it contributes a significant amount of loss for this application.

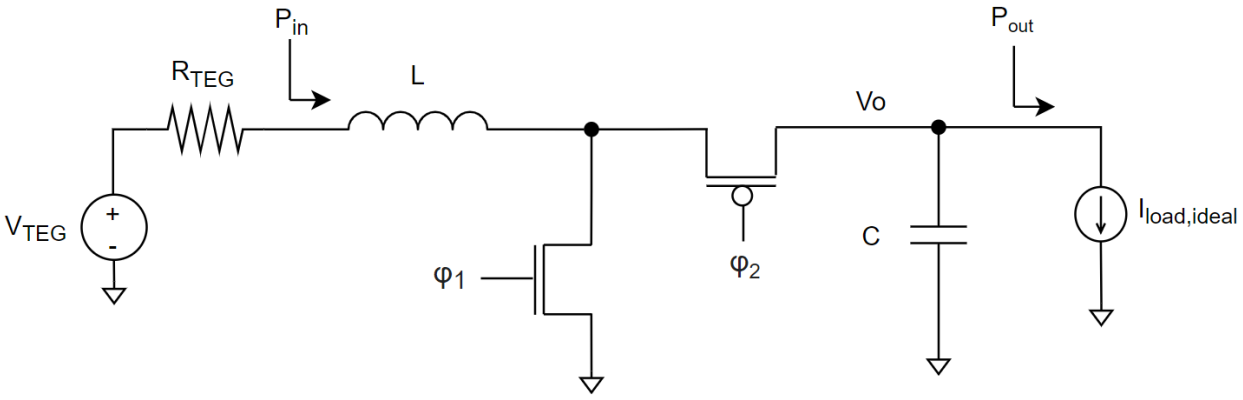

Figure 4.8: PCE Measurement Schematic

5. CONCLUSION

The research discussed in this document involved the design and implementation of a power harvesting system intended to harvest power from temperature differences in the human body using a TEG, switching converter and associated control circuitry. The primary contributions of this work include the unique feedback system designed that makes use of 2 modes of operation: impedance matching and regulation of the output voltage to a constant. This demonstrated a decrease in charge time of the output capacitor, thus, allowing the system to reach steady-state quicker than typical power harvesting solutions. It is important to emphasize that this work provides a practical power harvesting solution given the industry guidance received during the design process of the IC. Furthermore, the chip design experience gained by the students while completing this work was invaluable. This work presents a prototype and proof of concept for a biomedical implant power harvesting system. Future work and circuit design in this area could benefit from the developments discussed in this paper.

REFERENCES

[1] “Implantable Device Replacement Procedure,” Johns Hopkins Medicine. [Online]. Available: https://www.hopkinsmedicine.org/health/conditions-and-diseases/implantable-device-replacement-procedure. [Accessed: 24-Jan-2021].

[2] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, “A 1.1 nW Energy-Harvesting System with 544 pW Quiescent Power for Next-Generation Implants,” IEEE Journal of Solid-State Circuits, vol. 49, no. 12, pp. 2812–2824, 2014.

[3] E. J. Carlson, K. Strunz, and B. P. Otis, “A 20 mV Input Boost Converter With Efficient Digital Control for Thermoelectric Energy Harvesting,” IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 741–750, 2010.

[4] S. Bose, B. Shen, and M. L. Johnston, “A Batteryless Motion-Adaptive Heartbeat Detection System-on-Chip Powered by Human Body Heat,” IEEE Journal of Solid-State Circuits, vol. 55, no. 11, pp. 2902–2913, 2020.

[5] C. L. Thompson, C. Scheidel, K. E. Glander, S. H. Williams, and C. J. Vinyard, “An assessment of skin temperature gradients in a tropical primate using infrared thermography and subcutaneous implants,” *Journal of Thermal Biology*, vol. 63, pp. 49–57, 2017.

[6] Y. Zheng, L. Zhou, F. Tian, M. He, and H. Liao, “A 51-nW 32.7-kHz CMOS relaxation oscillator with half-period pre-charge compensation scheme for ultra-low power systems,” *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016.

[7] U. Denier, “Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1973–1982, 2010.

[8] Y.-H. Chiang and S.-I. Liu, “A Submicrowatt 1.1-MHz CMOS Relaxation Oscillator With Temperature Compensation,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 12, pp. 837–841, 2013.

[9] E. Rogers, “Understanding Boost Power Stages in Switchmode Power Supplies.” [Online]. Available: https://www.ti.com/lit/an/slva061/slva061.pdf. [Accessed: 28-Feb-2021].

[10] A.I. Karsilayan, Class Lecture, Topic: "IC devices and modeling" College of Engineering, Texas A&M University, College Station, TX, Feb., 28, 2021

[11] R. A. Mammano, Fundamentals of power supply design technology from Unitrode/Texas Instruments Power Supply Design Seminars. Dallas, TX: Texas Instruments Incorporated, 2017

[12] S. W. Lee, "Practical Feedback Loop Analysis for Voltage-Mode Boost Converter," Jan-2014. [Online]. Available: https://www.ti.com/lit/an/slva633/slva633.pdf. [Accessed: 06-Apr-2021].

[13] W. N. H. E. and D. M. Harris, CMOS VLSI design: a circuits and systems perspective, 4th ed. Boston, MA: Pearson, 2011.

[14] T. Saito and S. Komatsu, "A low — Voltage hysteresis comparator for low power applications," 2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2017.

[15] H.-W. Huang, C.-H. Lin, and K.-H. Chen, "A programmable dual hysteretic window comparator," 2008 IEEE International Symposium on Circuits and Systems, 2008.

[16] C. S. Kong, "A General Maximum Power Transfer Theorem," *IEEE Transactions on Education*, vol. 38, no. 3, pp. 296–298, Aug. 1995.

APPENDIX: LAYOUTS

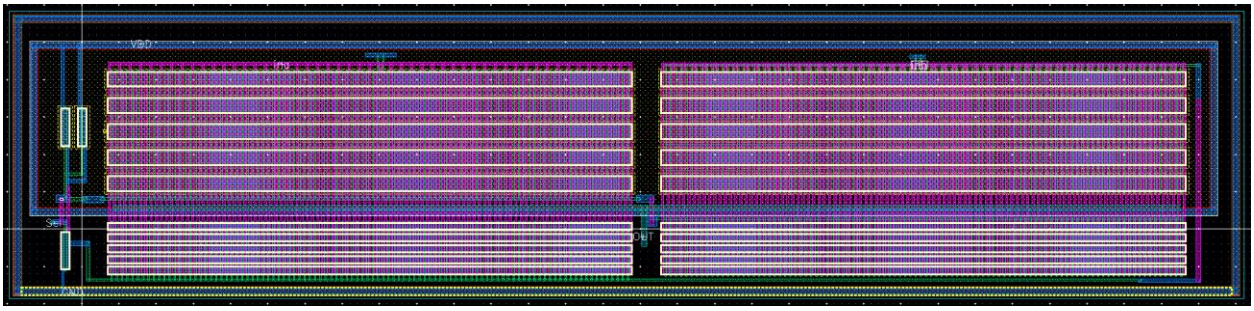

Figure 1: Large MUX Layout (x=165.88µm y=38.53µm)

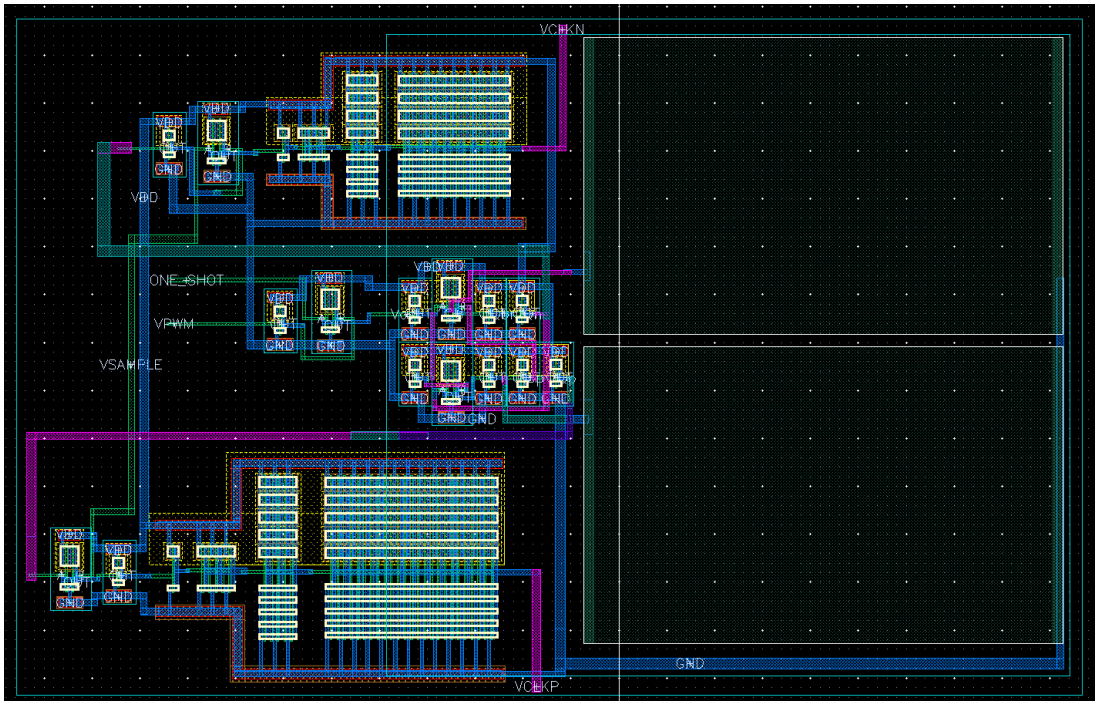

Figure 2: Switch Driver layout (x=111.27µm y=70.6µm)

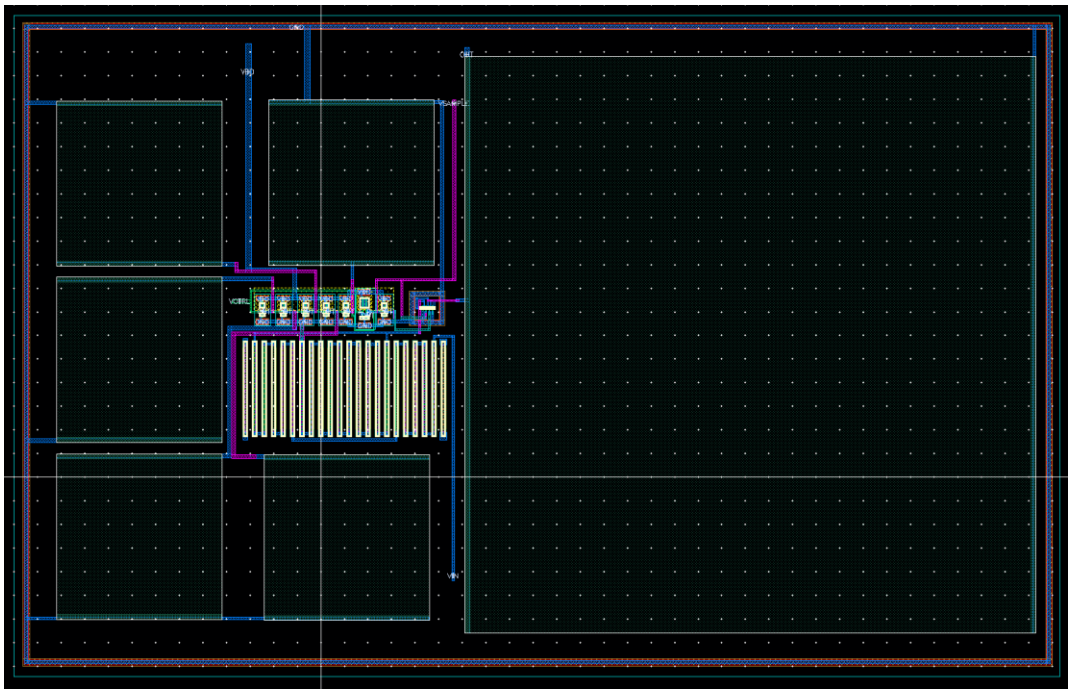

Figure 3: Voc Sampling Circuit layout (x=221.72µm y=139.87µm)

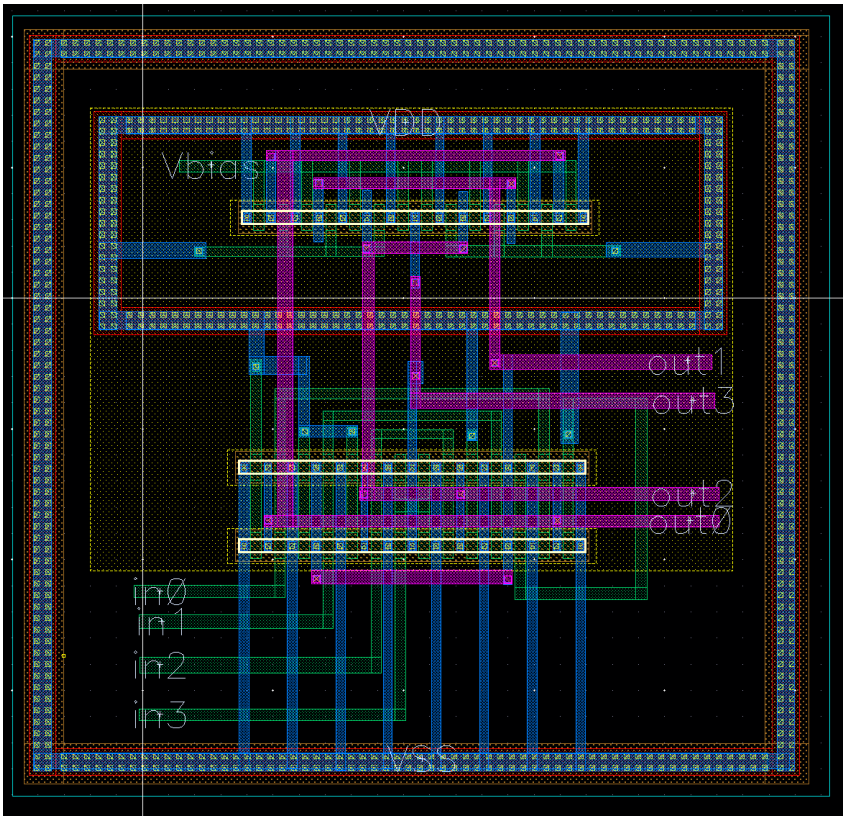

Figure 4: 4-Input Buffer layout (x=31.31µm y=29.83µm)

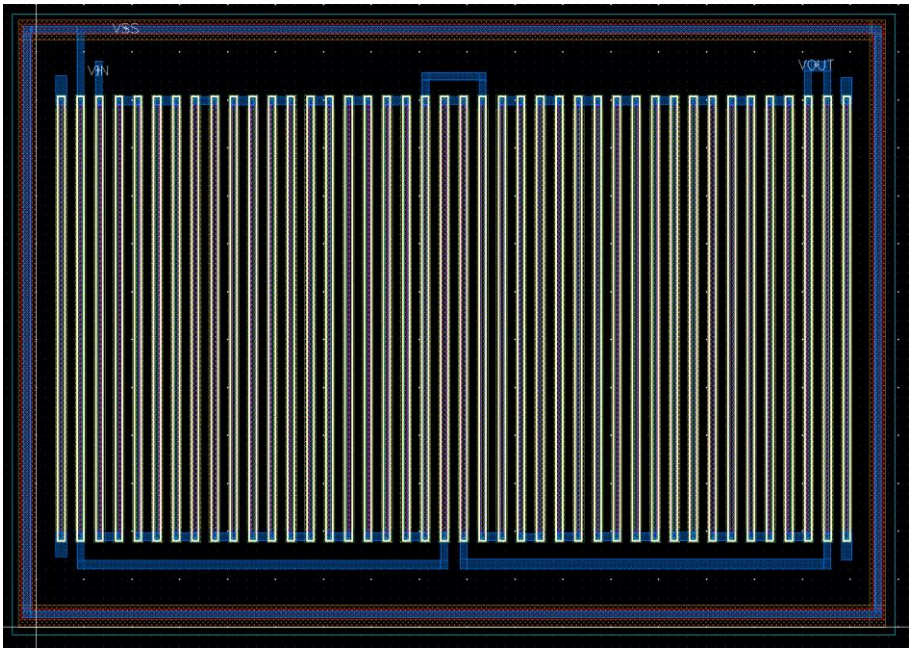

Figure 5: Feedback resistor layout (x=92.16µm y=64.72µm)

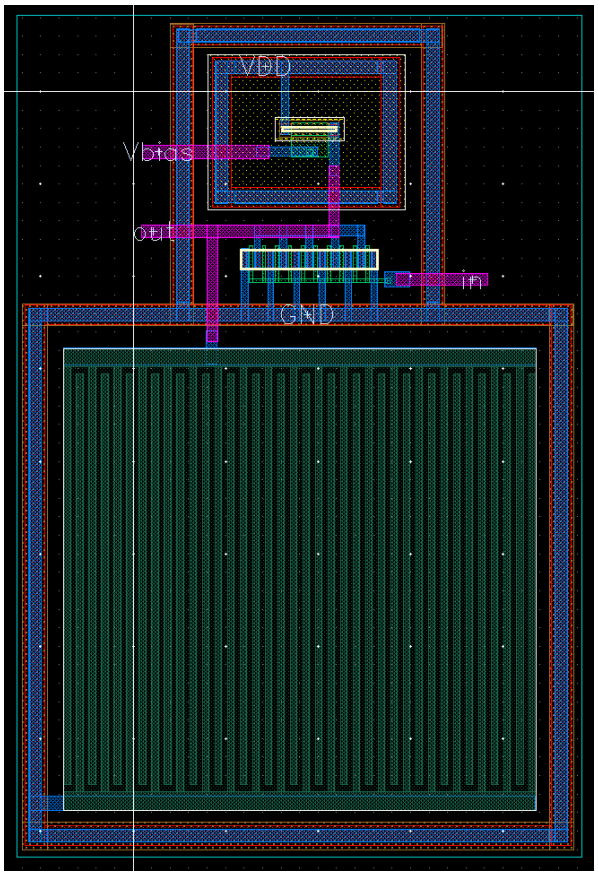

Figure 6: Sawtooth generator layout (x=45.04µm y=60.72µm)

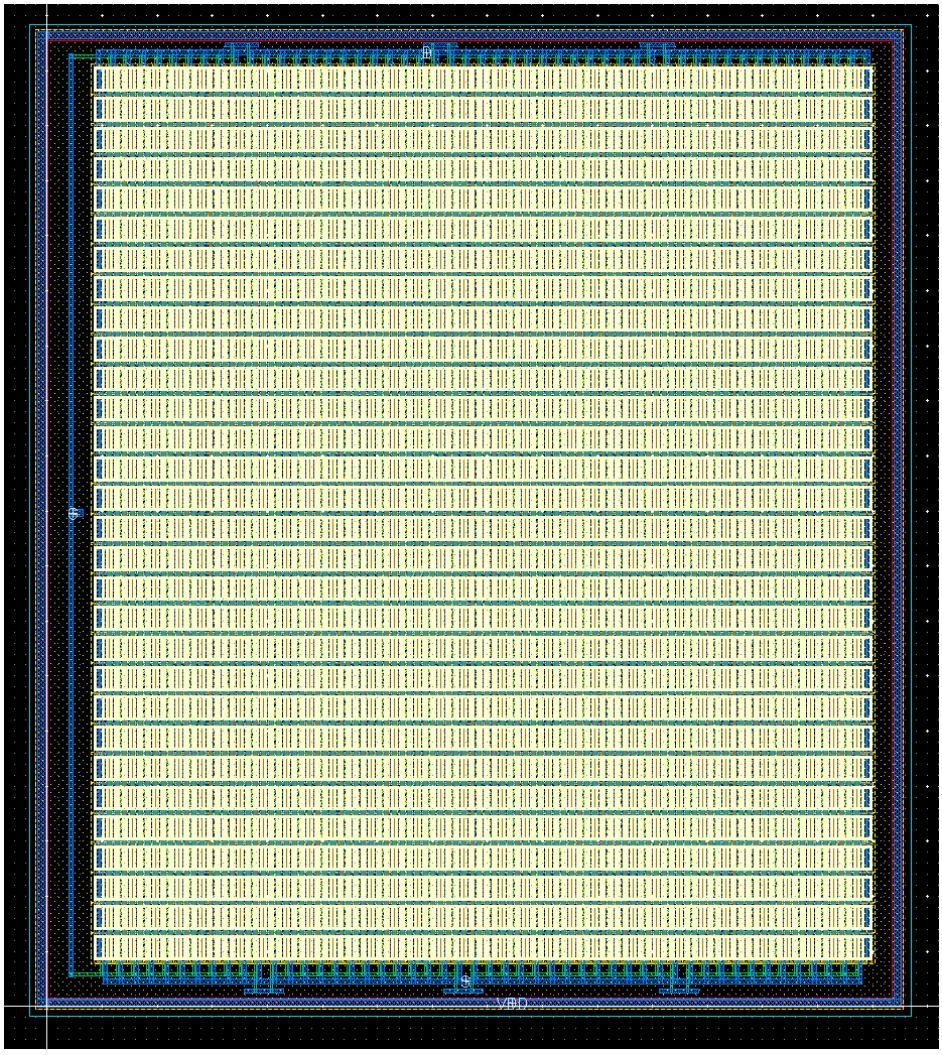

Figure 7: PMOS switch layout (x=80.01µm y=90.13µm)

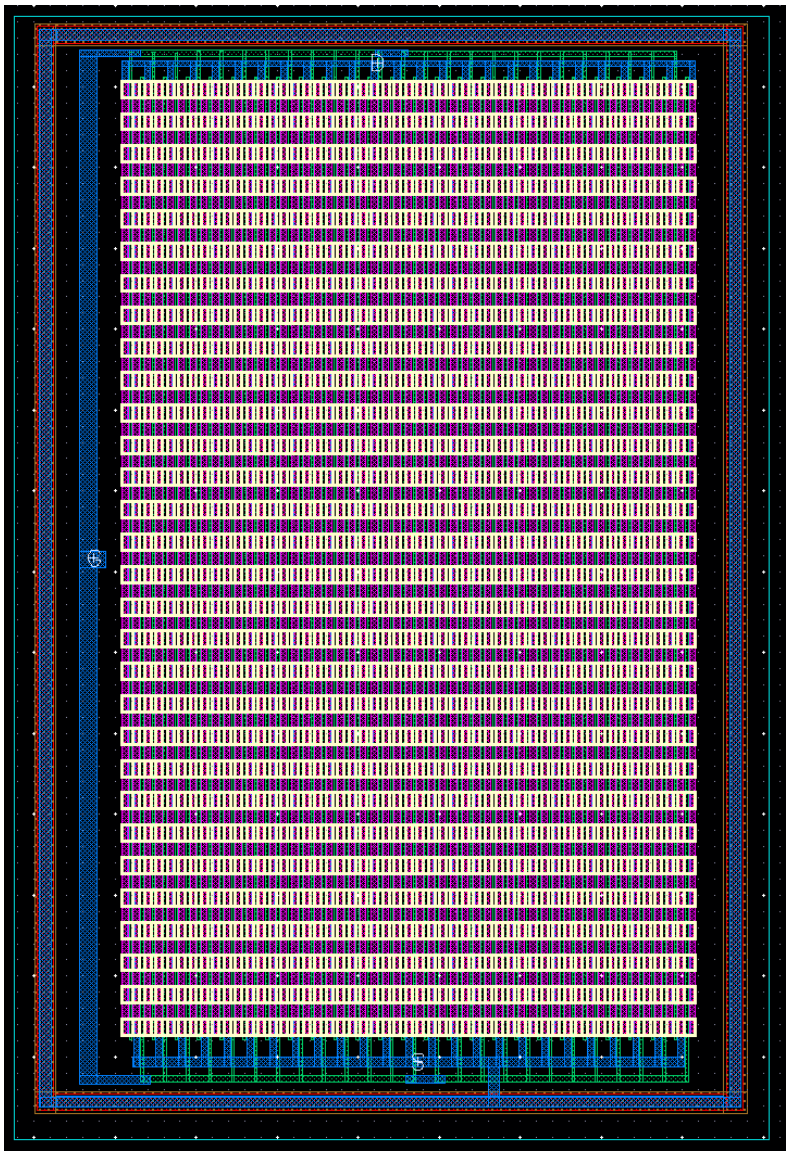

Figure 8: NMOS switch layout (x=46.55µm y=69.39µm)

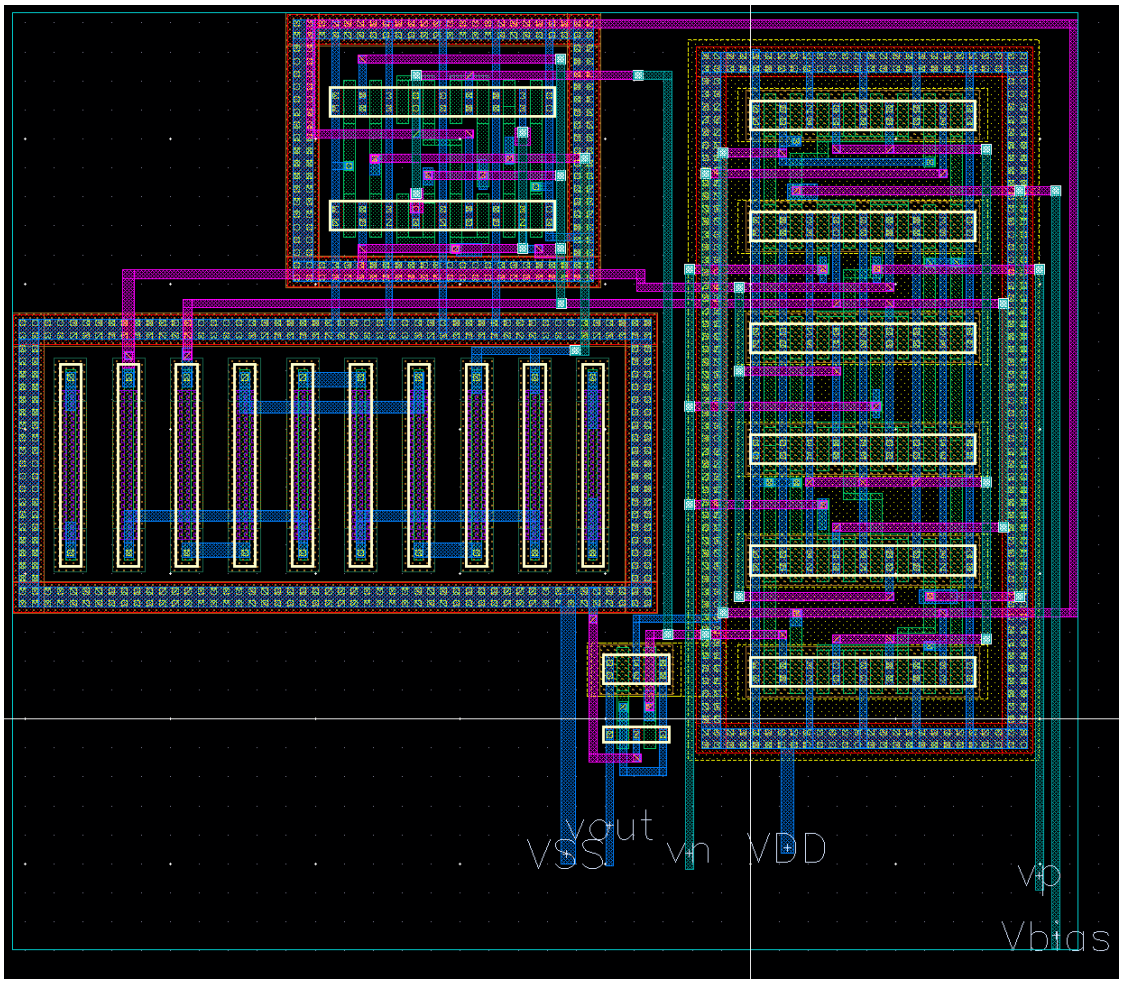

Figure 9: Comparator layout (x=36.37µm y=32.31µm)

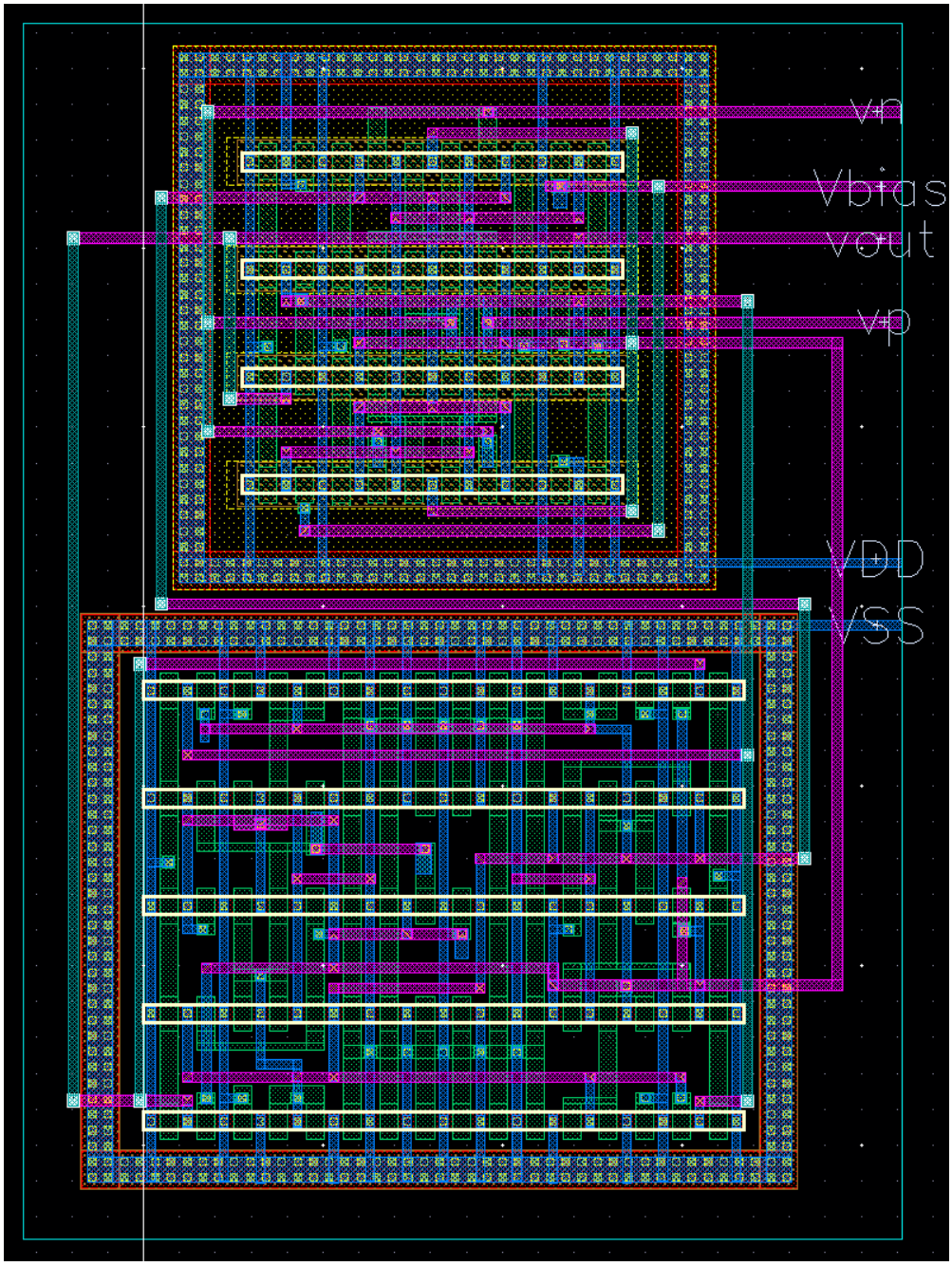

Figure 10: Hysteretic Comparator layout (x=24.47µm y=33.89µm)

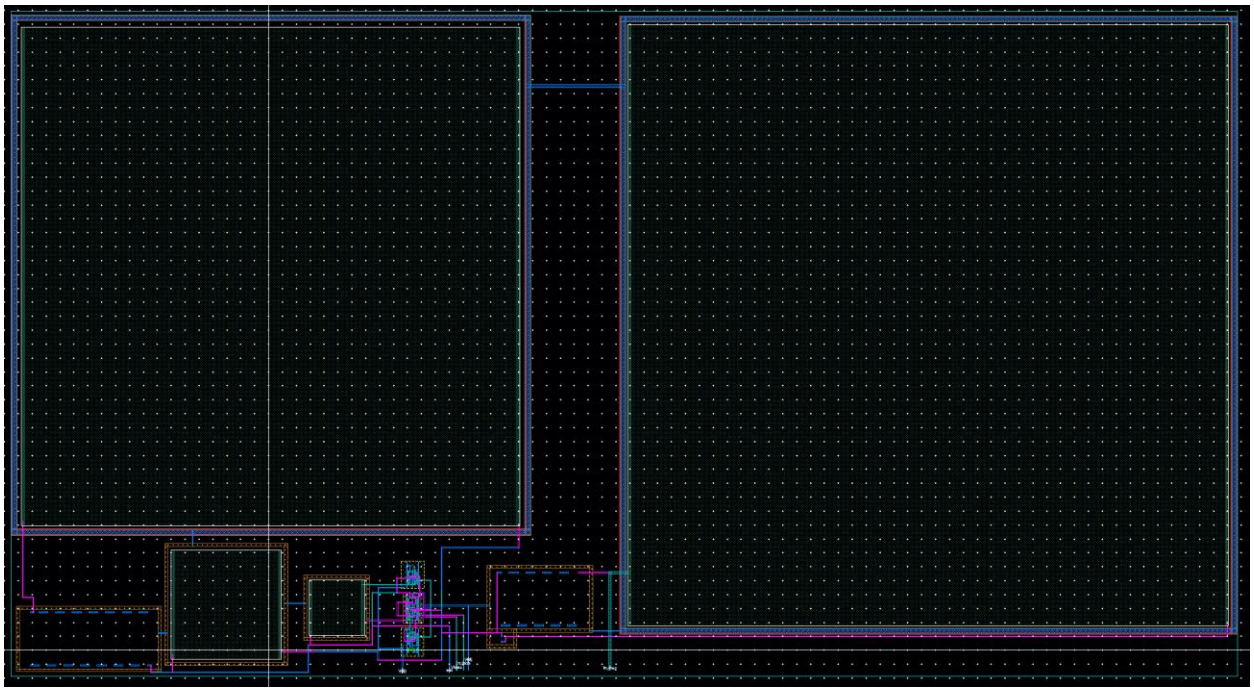

Figure 11: Error Amplifier layout (x=441.26µm y=239.07µm)

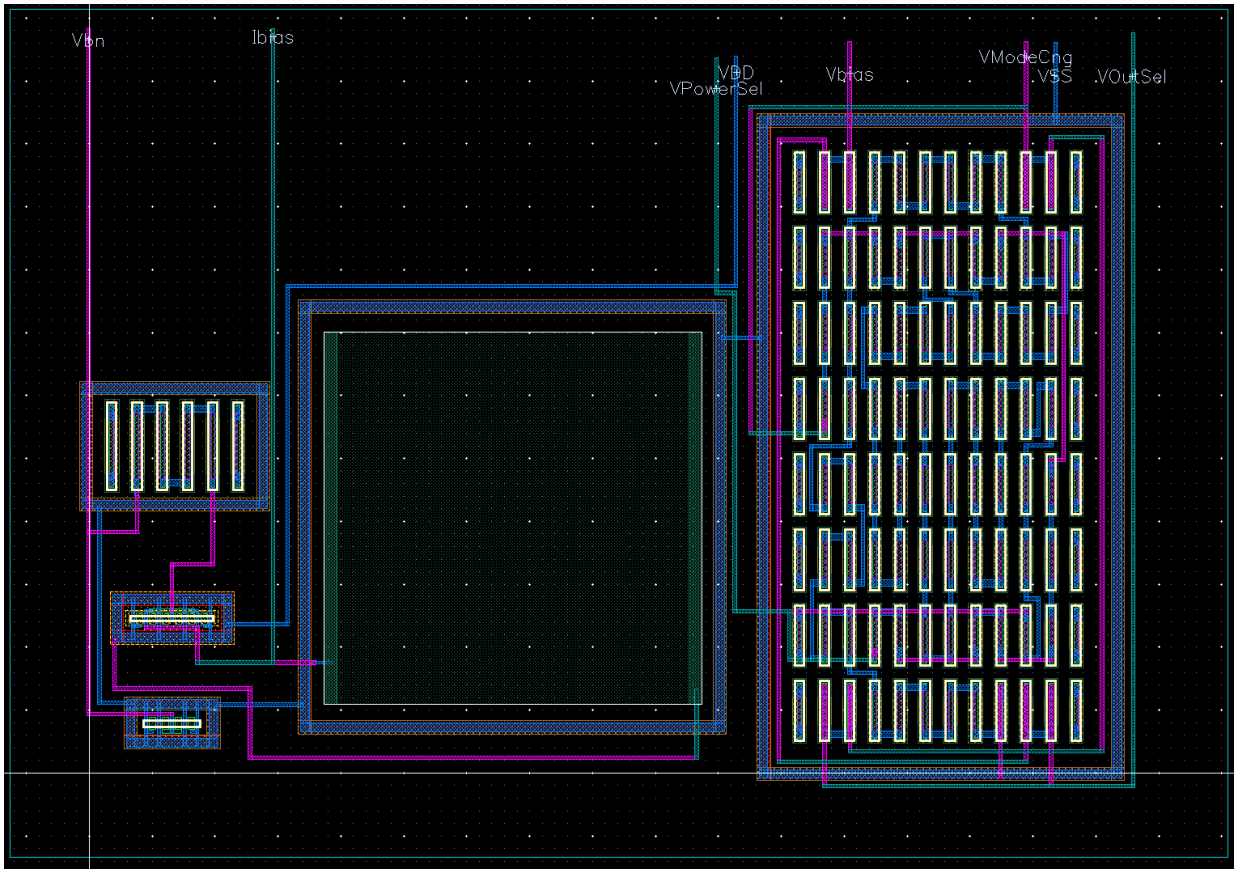

Figure 12: References layout (x=96.84µm y=67.37µm)

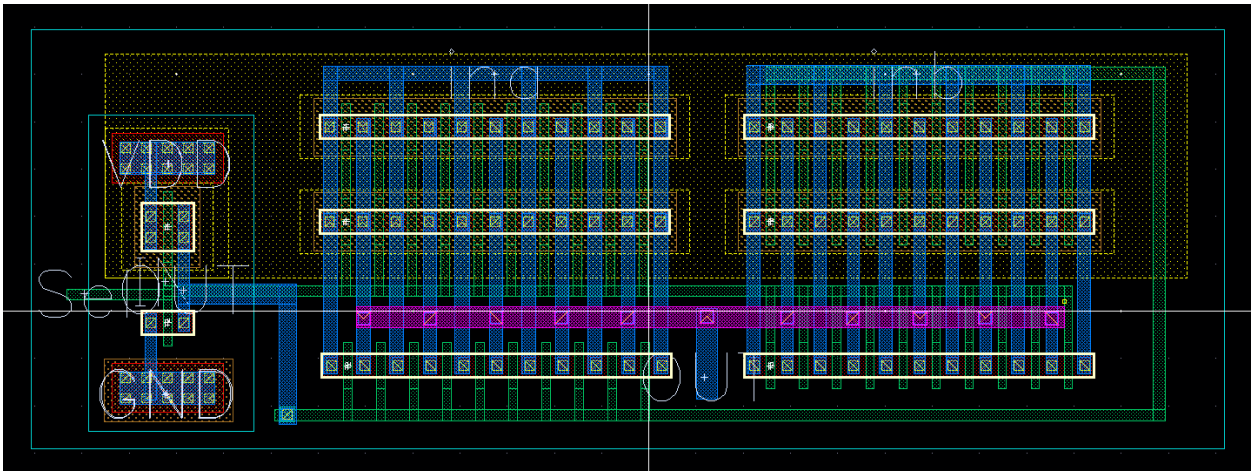

Figure 13: MUX layout (x=25.55µm y=8.86µm)

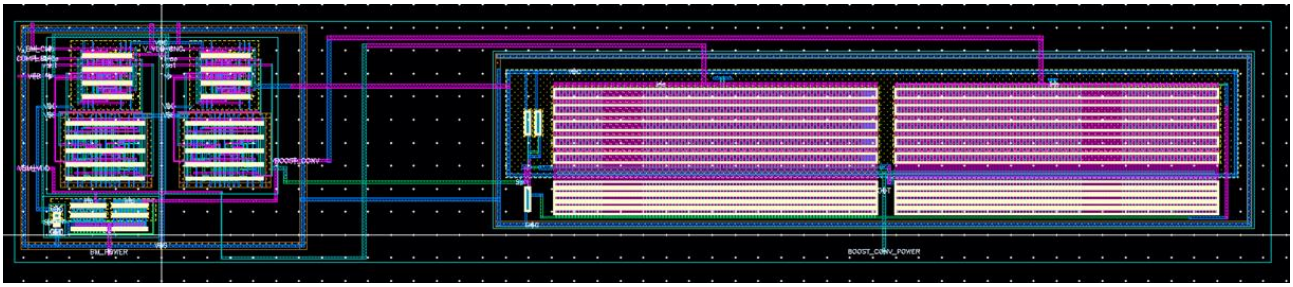

Figure 14: Decision Logic layout (x=273.72µm y=52.3µm)