EXPLORATION OF MUTLI-THRESHOLD FERRO-ELECTRIC FET BASED DESIGNS

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The supervisory committee certifies that this thesis complies with North Dakota State University's regulations and meets the accepted standards for the degree of

MASTER OF SCIENCE

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ABSTRACT

The surge in data intensive applications has given rise to demand for high density storage devices and their efficient implementations. Consequently, Multi-level-cell(MLC) memories are getting explored for their promising aspects of higher storage density and lower unit storage cost. However, the multi-bit data stored in these memories need to be converted to processor compatible forms (typically binary) for processing. In this work, we have proposed an adaptable multi-level voltage to binary converter using Ferro-electric Field Effect Transistors(FeFET) capable of translating input voltage to bits. The use of FeFETs as voltage comparators simplifies the circuit and offers adaptable voltage quantization, flexible output bit-width(1/2 bits) and security feature. The circuit also employs incremental output encoding, which limits error margin to the least significant bits(LSB). The proposed 4-level to 2-bit converter circuit is demonstrated in simulation to have an input voltage range of [0 – 3.75V] / [0 – 2.7V] for FeFETs with 20/2000-domains respectively.

ACKNOWLEDGEMENTS

This accomplishment for completing my dissertation would not have been possible without help and guidance from many kind-hearted people.

First of all, I would like to thank my advisor, Dr. Sumitha George, for helping and guiding me in every step of the way in my academic journey at NDSU. When I first came to this country, I found it hard to get accustomed to the new way of life. She was always there to help and advise me whenever I got stuck in my ideas, lab-experiments or any outside issue I faced, for which I am really grateful to Dr. George.

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I will be forever indebted for your kindness,
Thank you.

DEDICATION

I dedicate my thesis to my beloved Family.

Especially my father Sanatan Das, my mother Kabita Das and my brother Sujoy Das.

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LIST OF ABBREVIATIONS

FeFET . . . . . Ferro-electric Field Effect Transistor

MLC . . . . . Multi-Level Cell

PCM . . . . . Phase Change Memory

ReRAM . . . . . Resistive Random Access Memory

CAM . . . . . Content Addressable Memory

TCAM . . . . . Ternary Content Addressable Memory

Vpwlf . . . . . Voltage Piece-wise Linear File

NVM . . . . . Non-Volatile Memory

TVD . . . . . Threshold Voltage Defined

PDN . . . . . Pull Down Network

VTC . . . . . Voltage to Time Delay Converter

TDC . . . . . Time to Digital Converter

AGB . . . . . Adaptive Gate Biasing

LIST OF SYMBOLS

V ..... Voltage(Volts)

μC ..... Micro Coulomb(Unit of Charge)

V_D, V_S ..... Drain and Source Voltage(Volts) of FeFET

A ..... Ampere(Measure of Current)

λ ..... Smallest Dimension(Half of Gate Length) for Layout Design

τ_i ..... Switching Time Constant for i'th Domain in Ferro-electric Material

$E_{a,i}$ ..... Activation Field

F(t') ..... Applied Field

LIST OF APPENDIX FIGURES

CHAPTER 1: INTRODUCTION

Applications associated with surging amount of data such as artificial intelligence, data science, Internet of Things(IoT) etc. demand highly efficient systems for data storage and processing. Massive amounts of data need to be communicated between the memory and the processor in conventional von-Neumann systems and it severely impacts performance speed and energy consumption(referred to as *Memory Wall*[61]). This leads to exploration of novel architectures like in-memory and near memory computing which aims at processing data in or near to the memory respectively. In in-memory compute architectures, certain tasks are delegated to be performed in the memory itself by exploiting unique physical attributes of the memory device[49]. Resistance-based and charge-based memory devices have been explored for this novel computing process.

Memory hierarchies in today's systems consist of multiple levels of cache, main memory and storage, where the data is transferred from memory or lower level cache to higher cache levels for performing computational tasks. However, near-memory computing refers to processing nearer to where the memory resides[52]. This approach inspires tightly coupled design of memory and logic units for reducing memory access latency, power consumption and improves energy efficiency. An efficient and dense storage is crucial to execute data intense applications effectively in both conventional systems and near memory compute systems[33]. The capability to store multiple bits in a single cell results in higher data density with lower unit storage cost and provides phenomenal advantage for applications with high storage requirement[33]. Multi-level cell(MLC) storage devices offer a promising pathway towards high density storage of data. In MLC memories, each

cell is capable of storing multiple bits by exploiting a particular device property, such as charge [10], conductance[64], polarization[4] etc. For example, phase change memory(PCM) stores data by modifying the structure of the device between crystalline(less resistance) and amorphous(more resistance) states. A large signal margin between these states offer opportunity for MLC capability realization[44][18]. Another memory device technology, which has attracted considerable interest for MLC capability is Resistive RAM or ReRAM. In ReRAM, data is stored as resistance(or conductance) in the cell, and modulating the resistance switching by applying appropriate current or voltage signals, intermediate resistance states are observed allowing MLC applicability[58][64]. Spin transfer torque magneto-resistive random-access memory(STT-MRAM) has also been demonstrated for area efficient and fast MLC capability[7].

Recently, ferro-electric devices are attracting considerable attention and getting explored for their MLC capability along with multi-level logic functionality. Ferro-electric field effect transistor(FeFET) is a type of FET which consist of a ferro-electric layer in its gate stack to exploit the spontaneous electric polarization capability of ferro-electric materials. The device FeFET is capable of functioning as a logic device due to its three terminal FET nature along with its programmable threshold voltage capability. Additionally, as it can retain polarization from previously applied electric field to program the polarization, it can be exploited for achieving memory functionality. With the advent of hafnium-oxide(HfO_2)-based FeFET, research into efficient logic and memory designs with FeFET has increased. This is due to the excellent CMOS compatibility[14], scalability, retention performance, and energy-efficiency during electric-field driven polarization switching in HfO_2 FeFET[13][68]etc. These unique characteristics of the device can also open path for new

type of logic-in-memory designs for various applications[65]. In multi-level compute, the possibilities of storing more data and employing potentially less complex circuits attracts research efforts in an industrial manner[53]. Leveraging the partial polarization switching of the ferro-electric thin film, multiple threshold voltage (V_{t}) states can be realized, which opens up exciting opportunities for realizing Multi-bit memories and Multi-level logic systems based on FeFETs[3][35]. Moreover, FeFET based non-volatile content addressable memory(NV-CAM, NV-TCAM) designs for superior area and energy efficiency over existing CAM technologies and their application in associative processors has been a research hotspot for recent years[67].

The peripheral circuitry typically accounts for approximately $\sim 30\%$ of the area in a memory chip[56] . As compute and transmission logic typically process data in binary, data read and transfer operation demands for efficient data conversion mechanism be it traditional or near memory computation in MLC memories. Thus there exists a need to convert the data stored in MLC memories to binary bits. Peripheral circuits are employed to sense and convert the stored data into bits. These peripheral circuits in MLC memories are complex and bulky as they contain multiple signal reference comparison and encoding circuits for conversion. For instance, Cong Xu et al.[64] present two conversion schemes for stored data in ReRAM MLC viz, sequential sensing and parallel sensing. The sequential sensing scheme employs a sense amplifier, multiple latches, and a multi-bit encoder and utilizes time based latching and encoding to get the binary output. Parallel sensing scheme has multiple sense amplifiers with different reference voltage levels along with an encoding scheme to generate binary outputs(Fig. 5.6). Hossam et al. propose a time based reading mechanism for multi-bit memristor memories[32].

Figure 1.1. Multi-bit memristor memory reading operation[32]

In this mechanism the read signal is first interpreted to voltage signal. Then the voltage signal is converted to proportional pulse delay (voltage to time delay conversion or VTC), and the pulse delay gets converted to digital code using a time-to-digital(TDC) converter(Fig. 1.1)[32].

In PCM-MLCs N-comparisons with cell-resistances are performed in current, voltage or time signals to determine the N-bit data stored in the cell [18][8][62]. Latency to read data in PCM-MLCs can be reduced, if efficient sensing scheme with reduced comparison steps is implemented, for example, Some PCM-MLCs incorporate ADCs for the same[18]. In this work, we propose an ultra compact discrete multi-level voltage to binary converter using FeFETs.

In this work, the multiple threshold voltage(V_t) programming capability of FeFETs is utilized and exploited to discern or compare the level of a voltage to the FeFET threshold voltages and a compact multi-level voltage to binary converter is designed.

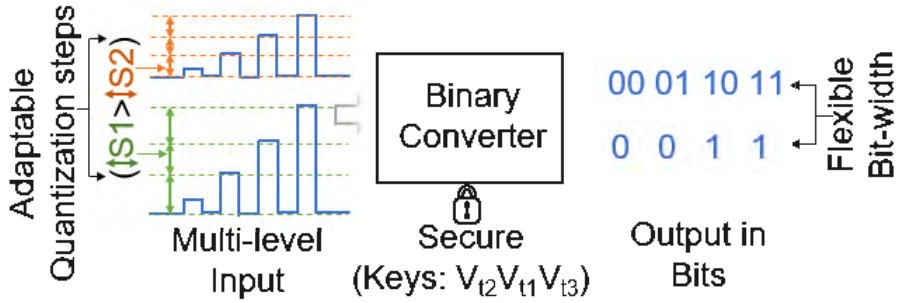

Figure 1.2. Overview of the proposed multi-level voltage to binary converter featuring adaptable quantization step, flexible output bit-width, security capability. Here S1 and S2 are the quantization steps for conversion[20](© 2022 IEEE).

It is demonstrated the following chapters that the converter design is flexible depending on the number of V_t states and the re-configurability of the FeFET device. Adaptable quantization provides the ability to vary the input voltage quantization step(Fig. 1.2). The circuit has the capability to function as 2-bit as well as 1-bit converter without any physical changes to the circuit, which is especially beneficial for MLCs to trade-off density or bit resolution with conversion accuracy.

As security has become more relevant with outsourcing of Integrated Chip(IC) fabrication to various foundries and with the necessity of data transmission through unreliable medium, the need for secure design for data handling has been ever increasing[46]. Our design is capable of incorporating an innate security feature in the output bit conversion. We utilize design specific features such as FeFET placement order and the programming of V_{t} states as keys to facilitate inherent encryption of binary data conversion. The scope of the design is not limited to main memory, but can also be explored for dense last level cache (STT-MRAM LLC, FeFET LLC) implementations. The design is also scalable.

The rest of the document is organized as follows. Chapter 2 describes the background. Chapter 3 elaborates on the device characteristics. Then in chapter 4, the proposed design and its unique features are discussed in detail. Chapter 5 discusses the simulation results. Chapter 6 presents conclusion and future works.

CHAPTER 2: BACKGROUND

2.1. Ferro-electricity

Ferro-electricity is a property exhibited by certain materials demonstrating spontaneous electric polarization without external field similar to ferro-magnetism characterized by spontaneous magnetic field[19]. Ferro-electric materials are a subclass of piezoelectric and pyroelectric materials. They consist of non-centrosymmetric crystals, which means some atoms in the unit cells of these materials are misplaced generating permanent electric dipole due to the unbalanced distribution of electric charges. However above certain temperature the ions arrange themselves to an equilibrium resulting in losing this property of ferro-electricity and the material starts behaving like paramagnetic or diamagnetic materials[36]. This temperature is called “Curie Temperature”. The polarization of ferro-electrics can be switched and reversed by applying appropriate external electric field. With applied field, the polarization starts increasing rapidly to reach a state where the behaviour is linear, then if an reversed electric field is applied, the polarization linearly decreases initially, and after it starts to fall rapidly to negative or opposite polarization with increase in the applied field[27].

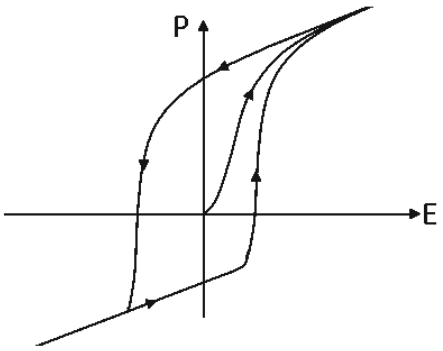

Figure 2.1. Hysteresis in Ferro-electrics[19] .

This behaviour creates a loop, which can be repeated countless times(Fig. 2.1). The capability of these materials to retain the polarization after removal of external electric field and the ability to reconfigure their polarization makes them a good choice for memory designs. The polarization depends not only on direction and amplitude of the applied electric field but also the history of polarization[5].

In a ferro-electric material the region with the same polarization direction is called a domain and the interfaces separating the domains are called domain-walls[26]. The size and number of domains formed, depend on the shape, size, orientation, local defect structure of the crystal and the energy costs associated with generating and inserting the domain-walls. Thus, depending upon the above variables a ferro-electric thin film can either break into multiple nano-domains or achieve a single domain state.

2.2. FeFET

Experimental study into Ferro-electric Field Effect Transistors(FeFET)for storing and switching information in a non-volatile manner dates back to 1960s[39]. Ferro-electric Field Effect Transistor(FeFET) is a type of Field-Effect-Transistor which consist of a ferro-electric layer in its gate stack(Fig. 2.7(a))[29]. Metal-ferroelectric semeconductor was first demonstrated and fabricated in 1974 using bismuth titanate[60]. Then in 2004 Sekai et al. demonstrated a strontium bismuth tantalate(SBT) based FeFET with high endurance and wide memory window, which was later expanded upon to design non-volatile logic as well[48][55]. Then the discovery of ferro-electricity in halfnium dioxide(HfO_2) opened up vast opportunities of FeFET research due to its full CMOS compatibility, lower parasitic leakage through gate stack compared to other ferroelectrics, stable data retention, a

reasonable memory window etc[39]. These properties sped up the advancement in HfO_2 based FeFET technology.

Xudong Wang et al. have demonstrated a low energy 2D-NCFET designed by replacing oxide layer of FET by ferro-electric polymer(P(VDF-TrFE))[57]. Their design achieved very low sub-threshold swing(24.2mV/dec) with four orders of drain current at V_{DD} of 0.1 volts at room temperature, which opens up the opportunity for this device to be implemented in future-nano-electronic fast switching and low power applications.

Proper ferroelectric film thickness ensures that the ratio of the capacitances of the ferro-electric layer and the MOSFET (C_{FE}/C_{MOS}) to be sufficiently low for polarization retention, achieving non-volatility[67][35]. Appropriate voltage at gate terminal of the device(write pulse) helps in setting the polarization(P), which controls channel carrier concentration causing shift in threshold voltage(V_t) of the device[6].

2.3. FeFET Multi-Threshold Characteristics

The capability of accessing intermediate polarization states through partial polarization switching in a multi-domain ferro-electric thin film using write pulses of different amplitudes or pulse widths lead researchers to explore FeFETs for non-volatile multi-bit storage[25]. Fig. 2.7(c) shows a typical $I_d - V_g$ curve of the device, demonstrating multi-V_t capability[63]. S. Dutta et al[24] have demonstrated multi-bit programming capability in FeFET with Tungsten(W) doped amorphous In_2O_3(IWO) channel integrated with ferro-electric $Hf_{0.5}Zr_{0.5}O_2$(HZO), which demonstrate distinct conductance states realizing a 2-bits/cell storage. With HZO and HSO laminated layers and appropriate inter-layers, multi-bit operation (1-3 bits/cell) in a FeFET is reliably demonstrated in [4]. Thus constant study into multi-V_{t} characteristics of FeFETs are being carried out to exploit these unique

features for application in denser memory, neural-network synaptic weights etc[4]. So, partial polarization of multi-domain ferro-electric film by applying differing write pulse in width and amplitude, results in multiple V_t states[43] and having multiple V_t states and their dynamic re-programmability provides opportunity for designing compact logic circuits for multi-valued systems using FeFETs. CMOS compatibility, non-volatility, steep switching, dynamic programmability, voltage-driven nature etc. make the FeFET device an attractive candidate as an adaptable and energy efficient solution for modern memory and compute device[13]. The different polarization values enable in configuring the FeFET to a high V_t state or a low V_t state as desired, making the device capable of being implemented as a programmable logic. Various FeFET-based memory and logic designs are discussed in the following sections.

2.4. FeFET-based Memory Designs

FeFET has been utilized to design single-sell and multi-level-cell memories exploiting the reliable hysteresis phenomenon observed in the ferro-electric layer polarization under the influence of external electric field. For example, Sumitha George et al.[29] have demonstrated FeFET 2T memory with high logic distinguishability between logic '1'and '0', low read-or-write energy and read-disturb free operation. The authors also propose an array design for organizing the memory cell efficiently in regards to area penalty in comparison to FeRAM[51].

Fig. 2.2 illustrates the read and write operation of the FeFET 2T memory cell[29]. In write operation, the access transistor is turned on by write access signal and appropriate write pulse is applied to the FeFET gate terminal to program it to a polarization corresponding to "High" or "Low" polarization state of the device.

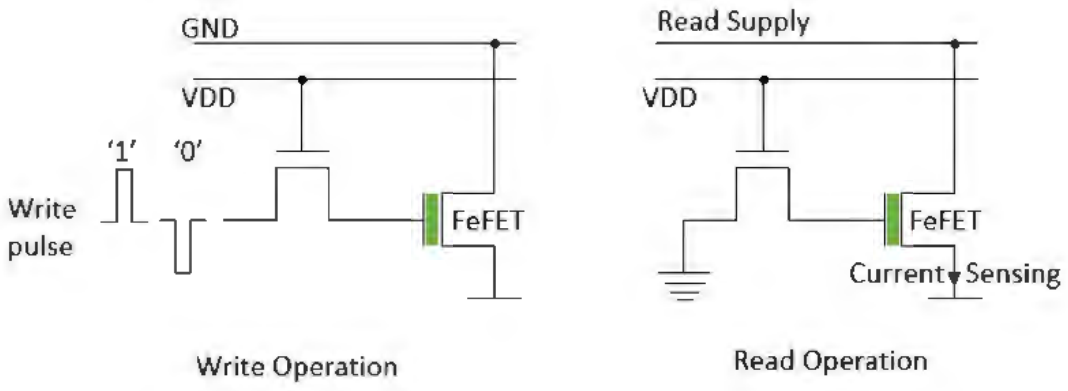

Figure 2.2. FeFET 2T single cell memory read and write operation[29]

In read operation, current sensing is implemented. In read, FeFET gate is kept at "GND" and a read supply is applied at the drain terminal. Depending on the written state of the FeFET, a "Low" or "High" current will pass through and will be sensed for discerning logic '0'or logic '1'respectively.

FeFET is also used for designing MLC memories by exploiting partial polarization of ferro-electric layer stacked in the gate stack. For example, Juejian Wu et al. have proposed a low power FeFET MLC design using adaptive design approach[59]. To maximize sensing margin and minimize sensing cost adaptive state mapping referring to automatic mapping of non-volatile-memory states depending on differing applications.

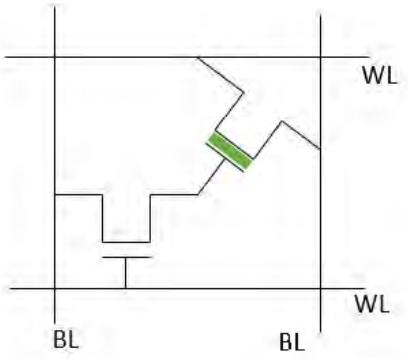

Figure 2.3. Typical FeFET-MLC cell in the memory array proposed in [59]

For example, in compute-in-memory applications, the states are mapped as currents (I_{DS}) to linearly represent the data for ease of processing MAC operations, whereas for traditional memory functionality, states are mapped in such a way that, the drain to source current(I_{DS}) gets converted to corresponding voltages(I-V conversion) with similar absolute difference[59]. Adaptive prediction-based direct(APD) write method is used for writing data into cells. In this writing method, the memory state of the cell is checked first. Then a control signal generates an according write pulse if necessary. The authors have also proposed an adaptive gate biasing(AGB) read mechanism for dynamically increasing the sensing range. In read operation, a gate bias(V1) is applied for sensing the read current. If the sensed read current is more than a minimum value then the data can be read, or else, a higher gate bias voltage(V2, such that V2$>$V1) is applied for increasing the sensing current over the minimum value.

Another application of FeFET is designing content addressable memories(CAMs) and ternary content addressable memories (TCAMs). CAM is a type of computer memory used in high speed search applications. In CAM an input search data is compared against a set of stored data, and the address of the matching rows is returned[45]. TCAMs are an extension of CAM notion, where another dimension("Don't care") is considered other than two bit-wise outcomes("Match" and "Mismatch")[9]. In [28], Sumitha George et al. propose an FeFET based 4T(2T-2Fe) TCAM design with features of search and read functionality. They also demonstrate topological variations of their design for NAND and NOR RAM functionality.

FeFET based binary and multi-bit associative search engine was proposed by Xunzhao Yin et al.[66], which uses series resistor current limiter for making the ON current

constant for ’0’ or ’1’ and a 2-step search operation for sufficient sensing margin. The content addressable memory design for the proposed engine consists of 1FeFET and 1R. The resistor is used for making the “ON” current independent of FeFET threshold voltages.

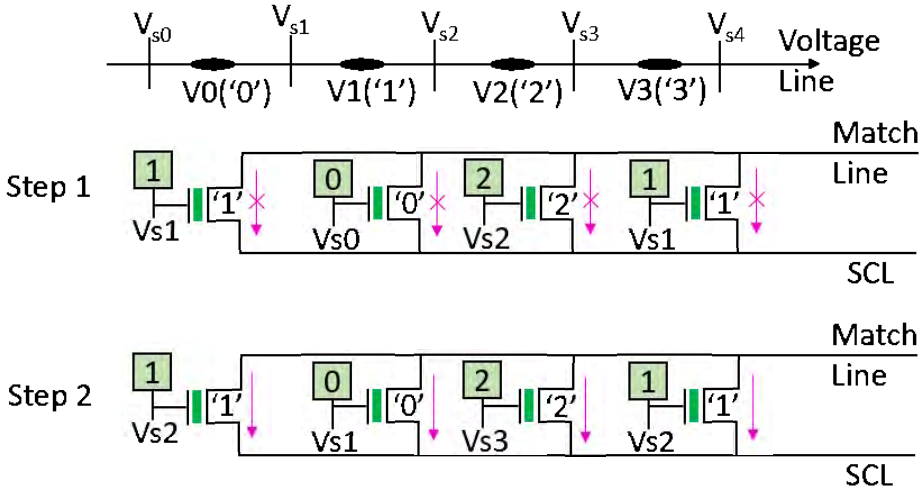

Figure 2.4. FeFET Multi-bit CAM design for Associative Search Engine discussed in [66].

As shown in Fig. 2.4, for searching a data (“1021” corresponding to threshold voltage “V1,V0,V2,V1”) searching voltage applied to the gate terminals, is less than search data threshold voltages respectively but more than the immediate lesser threshold (“Vs1,Vs0,Vs2 ,Vs1”) in the first step. In the second step voltages applied to the gates are more than the search threshold but less than next immediate higher threshold (“Vs2,Vs1,Vs3,Vs2”). As illustrated in the Voltage line, the applied gate voltages for search is in between the cell thresholds for correct operation. Any conduction in the first step and any open circuit in the second signifies a data “Mismatch”, otherwise it is a “Match”. The subsequent section discusses some re-configurable logic designs based on FeFET.

2.5. Re-configurable Logic using FeFET

In [15], E. T. Breyer et al. have proposed a single FeFET-based re-configurable NAND/NOR logic gate. The FeFET consists hafnium oxide as the ferro-electric material and the circuit have a pull-up device in series connection. The logic functionality is achieved by considering internal polarization state of the FeFET as one input and the applied gate signal to the FeFET as the other input for the logic operation. The logic is also re-configurable between NAND and NOR functionality, which is achieved by choosing the specific source bias or the back bias voltage of the FeFET(operation point tuning). Thus, the relative shift in Id-Vg curve of the FeFET by applying suitable source or back bias voltage is exploited to achieve the re-configurable FeFET logic, where the gate pulse(V_g) remains same for both NAND and NOR operation realizations.

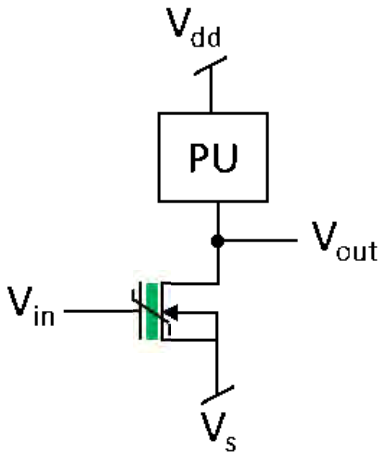

Figure 2.5. Structure of the re-configurable logic NAND/NOR gate consisting of an n-type FeFET and a pull-up device[15].

Similarly, the reconfigurability feature of FeFETs has been explored for security applications. Sourav Dutta et al. have experimentally demonstrated gate-level logic camouflaging and run-time re-configurability using FeFET for hardware security[22].

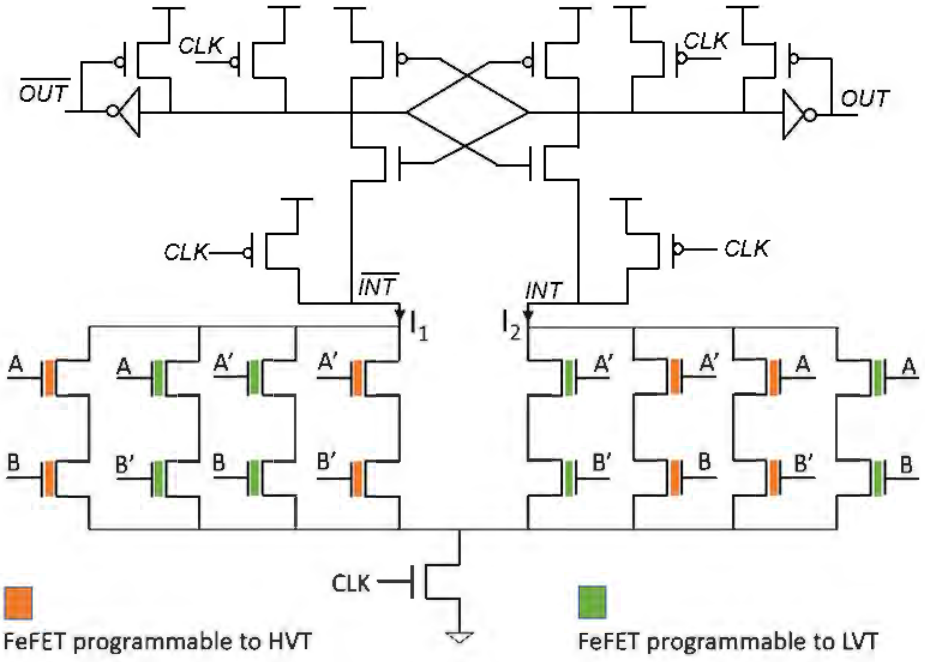

Figure 2.6. FeFET Re-configurable Pull Down Network(PDN) circuit[22]

Voltage dependent switching of FeFETs is primarily exploited for the proposed threshold voltage defined(TVD) camouflaging logic. The circuit consists of a pull-up network with a differential structure of cross-coupled inverters and a Pull Down Network. Fig. 2.6 shows an example of the FeFET-based TVD camouflaged logic. The Pull Down Network(PDN) consists of two differential branches, each consisting of 8-FeFETs[22]. This PDN block of 16-FeFETs are appropriately programmed to “HVT” and “LVT” combinations for realizing different gate operations(NAND, NOR, XNOR etc.) while still being highly secure from layout based reverse-engineering attacks.

2.6. FeFET Model

An FeFET device is designed by integrating a ferroelectric layer in the gate stack of a MOSFET (Fig. 2.7(a))[29]. An equivalent circuit of the device is shown in Fig. 2.7(b).

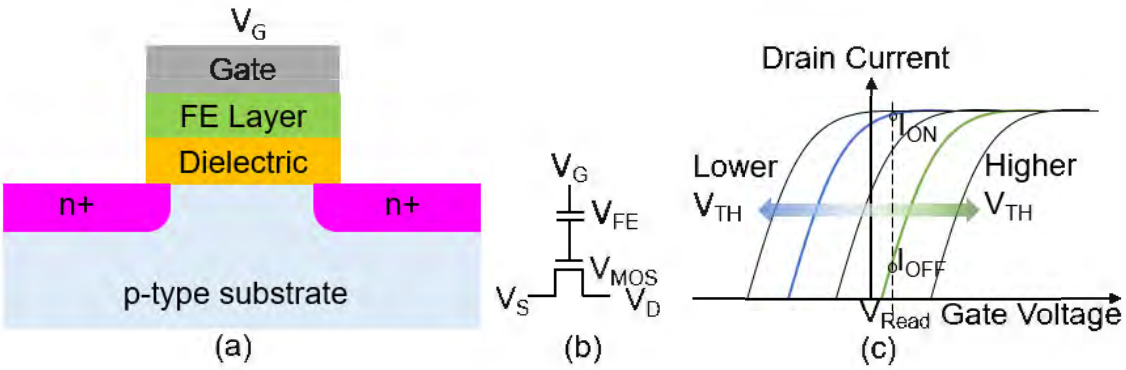

Figure 2.7. (a) FeFET Device structure, (b)FeFET model[21], (c)$I_d - V_g$ Characteristics [63](© 2022 IEEE).

The circuit equations followed by the model[21] is shown, where Q, C and V represents electric charge, capacitance and voltage potential respectively.

$$Q_{MOS} = Q_{FE}$$
$$Q_{FE} = P_{FE} + C_{FE}.V_{FE}$$
$$V_G = V_{FE} + V_{MOS}$$

The HfO_2 based FeFET model used in this work is based on distributed monte-carlo framework[2], where the ferro-electric flim is composed of several independent domains [21]. This model is capable of handling geometry scaling(20 domains to 2000 domains) and predicting stochastic switching in the scaled devices. This model also captures polarization accumulation phenomenon causing V_t shift and accordingly drain current variance. These capabilities are possible by following the change in "h" parameter value. This parameter keeps track of the ferro-electric history, thus capable of capturing the accumulation behavior. The "h" parameter value gradually increases till the flipping of the domain and the domain flips eventually after accumulation of switching probabilities because of

increase in "h" parameter, and this results in shift in the threshold voltage(V_t).

$$h = \int_{r_0}^{t} t'/\tau_i(E_{a,i}, F(t'))dt'$$

In the above "h" parameter equation, τ_i refers to switching time constant for i'th domain, $E_{a,i}$ and F(t') refers to activation field and applied field respectively[21]. We have used this FeFET model[21] for our simulation experiments.

2.7. FeFET for Peripheral Sensing

As introduced previously, most works so far leverage FeFETs for memory core or the compute kernel for in-memory computing, whereas few works have explored the possibility of using FeFETs for the peripheral sensing purposes. Banerjee. et al [11] discuss a ferroelectric-FinFET based neural network ADC implementation, where Fe-FINFET is employed in a diode connection fashion and requires precise conductance tuning for accurate operation. The ADC employs differential amplifier based neuron circuitry as decision elements(n-decision elements for n-bit ADC) for preserving polarization of the Fe-FinFETs while sensing for data conversion. In their design[11] the Fe-FinFETs are first pre-programmed to evaluated and desired polarization states for containing tuned conductance values for optimal performance.

In contrast, our implementation is very compact, as we directly utilize threshold voltage(V_t) of FeFETs for inherent voltage comparison and encode the generated thermometer codes to binary results using a single PFET encoding circuit for a 4-level to 2-bit converter. Moreover we propose a lot more features such as adaptability, flexible output bit-width and security capability in the design. Leveraging FeFET's programability and the

multi-V_t characteristics to implement quantized voltage comparison is the prime idea in the proposed adaptable voltage to bit converter circuit.

The circuit is simulated using a multi-domain FeFET model[21] for verification. The model is studied for capturing and analyzing device characteristics in chapter 3 before the design can be verified using this model.

CHAPTER 3: FEFET DEVICE STUDY

We have studied the characteristics of the FeFET device using a multi-domain Model [21] for its programming and behaviour after being programmed for 20-domains and 2000-domains respectively. We analyze the simulation results and decide on the V_t values(with distinct polarizations), programming voltages, pulse-width, read upset(which can affect the programmed polarization) etc. carefully for designing the proposed binary converter. Please note that, for demonstration purpose in this work, we define V_t as the voltage applied at the gate, which causes the source voltage to rise more than 80% of the drain supply voltage, unless stated otherwise.

3.1. FeFET with 20-Domains

Table 3.1. FeFET Characteristics with 20 Domains

Write Voltage(V) (Write time 1μs)	Polarization($\mu C/cm^2$)	Threshold voltage(V)(partial($V_S > 0.8V_D$) to full on($V_S \approx V_D$))
$>$3.9	5, 7.5, 10	—NA—
-1.5 to 3.85	2.5	0.8(403mV) – 1.1(494mV)
-2.4 to -1.5	0	1.6(405mV) – 1.8(487mV)
-3.2 to -2.45	-2.5	2.42(407mV) – 2.66(491mV)
-4.1 to -3.3	-5	3.22(410mV) –3.51(493mV) (read pulse 5ns)
$<$-4.3	-7.5, -10	—NA—

Table 3.1 illustrates the programming characteristics of FeFET with 20-domains. A write pulse of 1 μs is used to program the FeFETs to corresponding polarization(P) values respective to distinct V_t behaviour. For this study a 1 μs write pulse is applied to the gate terminal of the FeFET after an initial rest time of 1 μs. Then the device is rested for 6 μs, after which a read pulse of width 1 μs is applied. In this way, read pulses of a range

of magnitudes is swept through the device to determine the switching characteristics for distinct polarizations. When applying read pulses it is carefully considered that the pulse does not impact the programmed polarization. That is why for the polarization state -5 $\mu C/cm^2$ the read pulse-width is taken as 5ns(1 μs in all other cases).

Table 3.2. Re-programming of 20-domain FeFET

Programming pulse(V)	Polarization ($\mu C/cm^2$)	New Programming Pulse(V)	New Polarization ($\mu C/cm^2$)	Threshold Voltage(V)
1.5	2.5	> 4.2	5,7.5,10 etc.	–
1.5	2.5	-1.5 to 3.85	2.5	0.8
1.5	2.5	-2.2 to -1.6	0	1.6
1.5	2.5	-3.15 to -2.4	-2.5	2.45
1.5	2.5	-3.75 to -3.2	-5	3.25
1.5	2.5	< -3.8	-7.5,-10 etc.	–
-2.5	-2.5	> 4.2	5,7.5,10 etc.	–
-2.5	-2.5	3.2 to 4.15	2.5	0.8
-2.5	-2.5	2.65 to 3.15	0	1.6
-2.5	-2.5	-3.25 to 2.6	-2.5	2.45
-2.5	-2.5	-4.21 to -3.3	-5	3.25
-2.5	-2.5	< -4.23	-7.5,-10 etc.	–

Table 3.2 captures how an FeFET device can be re-programmed to a different polarization from its current polarization state by applying a suitable write pulse of appropriate width and amplitude. We first program the device to a specific polarization according to Table 3.1. Then we apply a sweeping of a range of pulses of width 1 μs and different magnitudes to the gate terminal to capture the transition characteristics. When a distinct polarization state transition occurs, the threshold voltage characteristics of the new polarization is checked in simulation. Both of these experiments were carried out using Virtuoso(version 6.1.8-64b) ADE-XL simulator using FeFET model[21] and we encoun-

tered many simulation glitches in the process. However, we have tried our best to capture a level of consistency according to the simulation results.

3.2. FeFET with 2000-Domains

The programming characteristics of FeFET with 2000-domains was studied by modifying the number of domains("ndom" parameter) in the model while keeping everything else unchanged. A 1 μs write pulse is applied to the gate terminal of the FeFET after an initial rest time of 1 μs. The resultant polarizations are checked after the write pulse has been removed. It is observed that there are a many more polarizations for FeFET with 2000-domains than FeFET with-20 domains.

Table 3.3. FeFET Characteristics with 2000-Domains[20](© 2022 IEEE)

Write Voltage(V)	Polarization($\mu C/cm^2$)	V_t(V)(Fully turned on($V_S > 0.9V_D$))
3.61	2.2	1
3.58	2.1	1
3.52	1.95	1.05
3.46	1.8	1.1
3.2	1.475	1.2
2.9	1.225	1.3
-1.5	0.825	1.45
-1.75	0.45	1.55
-2	-0.175	1.75
-2.2	-0.725	1.95
-2.4	-1.225	2.1
-2.5	-1.425	2.15
-2.75	-2.075	2.35

After programming, the device is rested for 6 μs, after which read pulses of width 1 μs and different amplitudes are applied. The 6 μs rest time is arbitrarily chosen for checking behaviour of the written polarization after the removal of the programming pulse. The sweeping of read pulses of 1 μs and different amplitudes(keeping in mind that the read pulse does not affect the written polarization) is applied for finding out the switching char-

acteristics of the device with 2000-domains. In Table. 3.3 we capture the characteristics for some of the various polarizations for FeFET with 2000-domains.

For designing a converter with this device, we choose certain polarizations with their corresponding V_ts, which have maximum absolute difference amongst each other, so that input voltage range for multi-bit to binary conversion is efficiently used. The circuit design and the converter operation is discussed in detail in chapter 4.

CHAPTER 4: PROPOSED DESIGN

[1] Data intensive Applications demand high storage and processing capability[33]. As Multi-level cell(MLC) storage devices offer high density storage of data, they have been getting explored for addressing this demand. However, as compute and transmission logic process data predominantly in binary, efficient data conversion mechanisms are required. There are various conversion schemes for various MLC technologies[17]. This work shows a design of an adaptable multilevel voltage to binary converter.

The designs also demonstrate various features - adaptability, flexible output bit-width, and secure binary output encryption.

4.1. 4-level Voltage to 2-bit Converter

We propose a converter design for converting one 4-level voltage signal to 2 voltage signals, which can be interpreted as a 2-bit output. For example, if we have a voltage signal which ranges from 0 to 2.7 Volts, and the circuit converts 0 – 0.6V to two signals both being less than 100mV, 1.05 – 1.25V to ($<$100mV, $>$450 mV) signals, 1.75 – 1.95V to ($>$450mV, $<$100mV) signals, 2.35 – 2.7V to ($>$450mV, $>$450mV) signals. We can interpret output signals greater than 450mV as "Logic 1" and less than 100mV as "Logic 0"(Fig. 4.1).

Fig.4.2 shows the proposed circuit to convert 4-discrete level voltages to $2 - bit$ outputs. The circuit consists of three FeFETs(F1, F2, F3), three NFETs(M1, M2, M3), and one PFET(M4). FeFETs function as voltage comparator due to their polarization retention and threshold voltage programming capability as inherent referencing and generate

[1]The material in this chapter is based on an article[20](© 2022 IEEE) authored by the author of this thesis, Sanjay Das, along with Arun Govindankutty, Shan Deng, Dr. Kai Ni and Dr. Sumitha George. The team collaboratively worked on the article, while Sanjay Das performed the research, drew conclusions and wrote majority of the paper. Proofread and revisions of the paper was done by the whole team. Sanjay Das also have drafted and revised all versions of this chapter in the thesis.

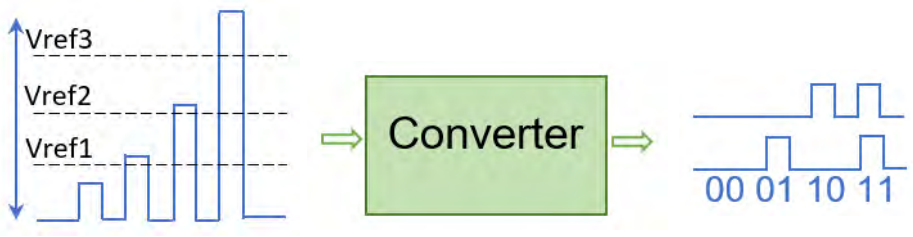

Figure 4.1. 4-level to 2-bit conversion overview

thermometer codes as output. Thermometer coding is an entropy encoding scheme which represents non-negative numbers in binary format($0 = 000, 1 = 001, 2 = 011, 3 = 111$ and so on)[1]. The generated thermometer codes are applied to the next encoding phase for generating the binary or bit outputs. NFETs are used to provide a discharge path for residual charges or voltage at the FeFET source terminals before the input is applied to cause a change source terminals ensuring reliable conversion of input voltage. The PFET works as an encoder to encode the thermometer codes to generate the output bits. The V_ts of FeFETs, F1, F2 and F3 are programmed to V_{t1}, V_{t2} and V_{t3} respectively by applying appropriate write pulse at their gate terminals. The relationship between the different V_ts is $V_{t1} < V_{t2} < V_{t3}$. When an input voltage V_{in} is applied, all the FeFETs having $V_t < V_{in}$ gets turned ON and passes drain voltage V_{DD} to their source terminals. For example if V_{in} is applied to all the FeFET gate terminals such that $V_{t1} < V_{in} < V_{t2} < V_{t3}$, only F1 will get turned ON and F2, F3 will remain in OFF state, which will generate the thermometer code "010" according to the Fig.4.2 and the encoded output will be "01".

Given that the polarization states have already been set, they remain unchanged during the conversion, which is ensured by limiting amplitude and pulse width for V_{in} signal. The selective turning ON of FeFETs provides distinct thermometer codes for the corresponding input voltages. We apply discharge enable signal at gate terminals of M1,

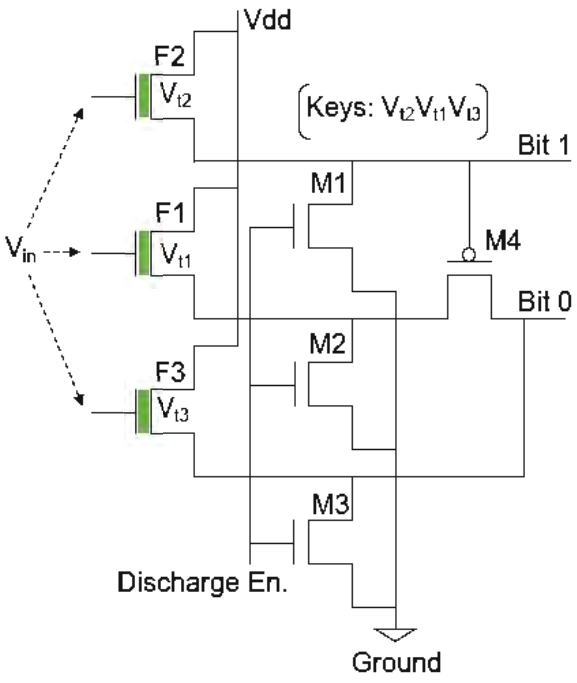

Figure 4.2. Multilevel voltage to binary converter circuit. FeFETs F1, F2, F3 are programmed to V_{t1},V_{t2}, V_{t3}. The placement order and programming of the FeFETs is used as keys for demonstrating security capability[20](© 2022 IEEE).

M2, and M3 before applying V_{in} to the circuit and ensure no residual voltage(or charge) is present at the source terminals of FeFETs. This eliminates false triggering of the outputs. M4 at the output stage converts the thermometer code to corresponding binary outputs. The source of F2 is the MSB of the output as well as the gate input for the PFET M4. When F2 is ON, M4 is OFF and source of F3 is observed as LSB of output. When F2 is OFF, M4 is turned ON and passes source terminal voltage signal of F1 as LSB to the output. Note that, the design is scalable for further quantized input voltage levels and more output bits by minimal modifications−having more V_t states in FeFET and adding more FeFETs(to increase the number of voltage comparison states) and modifying output encoding circuit.

4.2. Adaptability

One of the unique features of FeFET device is the ability to re-program its threshold voltage dynamically[25]. By applying an appropriate write pulse at the gate terminal we can re-program the FeFET to obtain a different threshold voltage and thus a different switching characteristic(section 3, Table 3.2). We utilize this dynamic re-programmability to achieve different V_ts in the device. As multiple domains in Fe-layer influences the number of polarization states and threshold voltages in an FeFET, choosing different threshold voltages for the FeFETs, offer different quantization steps and input range for the conversion operation. The device is programmable to different V_ts (default to V_{t1}, V_{t2} to V_{t1}, V_{t3} to V_{t2} etc) by choosing a different set of voltages to apply to the FeFET gate terminals, thus providing adaptability in the circuit. Our analysis shows lower number of domains in FeFET provide fewer polarization states than FeFET with more number of domains. In section 4.4 we discuss and expand upon the inherent potential security capability of the converter design depending on the threshold voltage programming order of the FeFETs. The adaptability of the design due to FeFET reprogrammablity is the necessary feature for the security capability.

4.3. Flexible Output Bit-width

Our proposed design offers the flexibility to change the output bit width(2-bit output to 1-bit output) without any explicit changes to the circuit. The design in Fig. 4.2, can be reconfigured to function for 2-level input voltage to 1-bit conversion by only utilizing F2 FeFET with appropriate V_t, in which case, the F2 source terminal will be considered as the output bit(Bit 1 in Fig. 4.2). Keeping F1 and F3 programmed to the highest possible V_t or disconnecting them, will reduce the energy consumption by preventing switching of

the successive logic. Flexible output bit-width conversion is a valuable feature for flexible precision computing applications with MLC memories. Bit density is often traded for reliability(larger gap between successive stored states) in Multi-level-cell memories[50] and due to the design flexibility, the proposed circuit is amenable to trade density for conversion accuracy.

4.4. Secure Binary Output Encryption

Hardware security and secure data transmission are critical with outsourcing of chip fabrication and transfer of data over an unreliable medium[54]. Threshold voltage re-configurability in FeFETs has been explored for logic security in [23][40]. In this work, we incorporate data encryption by exploiting dynamic multi-threshold voltage programmability and the programming order of FeFETs in the circuit. The order in which the FeFETs in the design are programmed with different V_ts influences the output and results in inherent data encryption. This is due to the fact that the programming order affects the thermometer code generation, which then gets encoded to output. For instance, if FeFETs F1, F2 and F3 in the circuit(Fig. 4.2) are programmed to V_{t1}, V_{t2}, V_{t3}(where $V_{t1} < V_{t2} < V_{t3}$) instead of V_{t2}, V_{t1}, V_{t3}(as used in the converter circuit) in top-down order, the output will be different for certain V_{in} values (i.e. an input voltage V_{in} between V_{t1} and V_{t2} would generate “10” and “01” for the two combinations, respectively).

Table. 4.1 illustrates some of the unique combinations of programming order of FeFETs in the converter circuit(Fig. 4.2) and their impact on the corresponding outputs for various inputs. For example, 1.3V input voltage $V_{t1}(1V) < V_{in} < V_{t2}(2.5V)$ according to Table 4.1 would generate “10” and “01” respectively for programming orders V_{t1},V_{t2},V_{t3} and V_{t2},V_{t1},V_{t3}. So, different programming orders of the FeFETs in the converter design

Table 4.1. Programming Order and Corresponding Outputs[20](© 2022 IEEE)

Combinations	Output Bits for Corresponding Inputs			
	$V_{in}<V_{t1}$	$V_{t1}<V_{in}<V_{t2}$	$V_{t2}<V_{in}<V_{t3}$	$V_{t3}<V_{in}$
V_{t3}, V_{t3}, V_{t3}	00	00	00	11
V_{t3}, V_{t3}, V_{t2}	00	00	01	11
V_{t2}, V_{t3}, V_{t3}	00	00	10	11
V_{t2}, V_{t3}, V_{t2}	00	00	11	11
V_{t3}, V_{t1}, V_{t2}	00	01	01	11
V_{t2}, V_{t1}, V_{t3}	00	01	10	11
V_{t2}, V_{t1}, V_{t2}	00	01	11	11
V_{t1}, V_{t2}, V_{t3}	00	10	10	11
V_{t1}, V_{t3}, V_{t2}	00	10	11	11
V_{t1}, V_{t3}, V_{t1}	00	11	11	11

varies the switching of the FeFETs, thus controlling the output for various ranges of inputs. This facilitates the use of threshold voltage programming order to be used as $keys$ for encryption.

CHAPTER 5: RESULTS ANALYSIS

[1] We use Virtuoso(version 6.1.8-64b) ADE-XL simulator environment with open-source NCSU 45nm Basekit[41] and a multi-domain FeFET model[42][21] for our simulation and analysis. We verify the functionality of the proposed design and explain in detail in this section.

5.1. Proposed Binary Converter

Fig. 5.1 shows simulation verification of the proposed 4-level input voltage to 2-bit output converter circuit shown in Fig. 4.2. As explained in Chapter 4, first the FeFETs are programmed to chosen V_ts. Second, the input voltages are converted to binary by applying them to the FeFET gate terminals. We explain both the operations below. For simulations, the ferro-electric layer thickness is set to 8nm and the number of ferro-electric domains in FeFET is set to 20 unless mentioned otherwise.

5.1.1. Programming(Write)

The FeFETs F1, F2, and F3 are programmed to polarization states 2.5, -2.5 and -5 $\mu C/cm^2$ respectively by applying write pulse of amplitudes 0.5V, -2.6V and -3.5V and $1\mu s$ width. The corresponding V_t values for those polarizations obtained are 1V (V_{t1}), 2.5V (V_{t2}) and 3.35V (V_{t3}). Fig. 5.1(a) captures the application of gate voltages and respective polarization change(programming) of FeFETs in the converter circuit. As shown in the figure the write pulses program the FeFETs to their intended polarizations and in turn to have distinct threshold voltages as shown in Table 5.1.

[1]The material in this chapter is based on an article[20](© 2022 IEEE) authored by Sanjay Das et al. The team collaboratively worked on the article, while Sanjay Das performed the research and wrote majority of the paper. Proofread and revisions of the paper was done by the whole team. Sanjay Das also drafted and revised all versions of this chapter in the thesis.

Table 5.1. Threshold Voltage Programming(20-domain FeFET)

Applied Gate Voltage(V)	Resultant polarization(P)($\mu C/cm^2$)	Threshold Voltage(V)
0.5	2.5	1 (V_{t1})
-2.6	-2.5	2.5 (V_{t2})
-3.5	-5	3.35 (V_{t3})

Table 5.2. Input Voltage to Bit Conversion(20 domains, pulse width: 5ns)

Input Voltage(V)	Output 1(V)	Output 0(V)	Logic State
3.4	0.498	0.472	11
2.6	0.485	0.001	10
1.4	0.02	0.48	01
0.5	0.001	0.001	00

5.1.2. Conversion(Read)

Table 5.2 illustrates the simulations parameter values and Fig. 5.1(b) shows the simulation waveform of the binary conversion for 4 discrete input voltages V_{in} in the range 0V to 3.75V. V_{in} gets translated to corresponding binary values depending on the programmed V_t values [$V_{t1} = 1V, V_{t2} = 2.5V, V_{t3} = 3.35V$]. In this example, V_{in} values $\{0.5V, 1.4V, 2.6V, 3.4V\}$ get converted to {"00", "01", "10", "11"} respectively. The drain bias voltage V_{DD} of the FeFETs is set to $500mV$ and for logic discernment, we consider any voltage greater than 450 mV at the output as Logic '1', and less than 100 mV as Logic '0'. The input voltage range is set between 0V and a voltage greater than V_{t3}. The upward limit of the input voltage range depends on the read upset voltage, which is not a safe operating region as it can disturb the programmed polarization state of the FeFETs. Our simulations indicate that $5ns$ pulse-width does not disturb programmed V_ts. Our simulations also show a worst case delay of $\sim 550ps$ for the conversion.

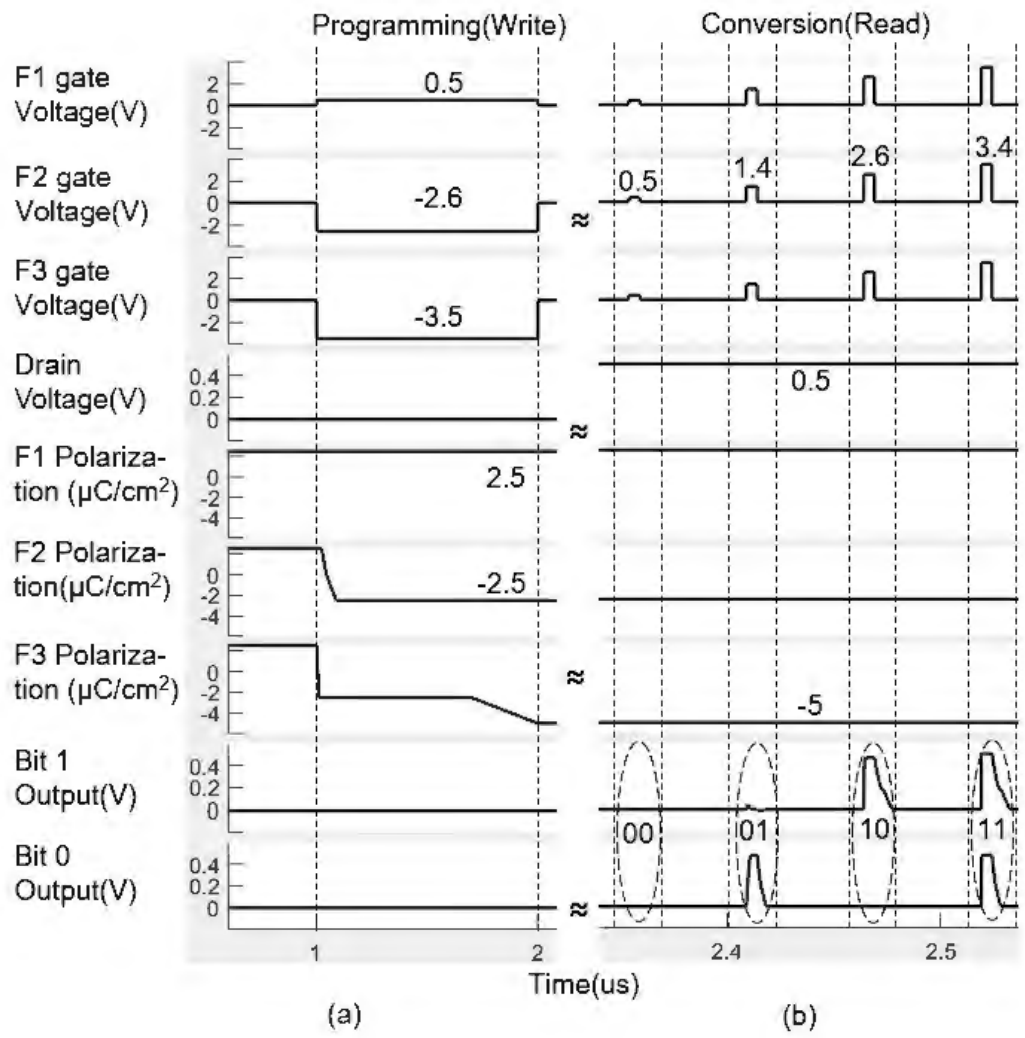

Figure 5.1. Simulation of converter with 20-domains FeFET. (a)Threshold voltage programming of FeFETs and (b)Input voltage(V_{in}) to output bit conversion is shown. V_{in} values {0.5V, 1.4V, 2.6V, 3.4V} get converted to {00, 01, 10, 11} [20](© 2022 IEEE).

5.2. Input Quantization Noise Margin

Ideally we expect 0V for logic '0'and V_{DD} for logic '1'at the output. However, absence of ideal switching in FeFET $I_d - V_g$ characteristics leads to partial conduction of FeFETs generating ambiguity in output bit conversion for certain range of input voltages. We denote these ambiguous regions of input voltage range as input quantization noise margin. In our design, we consider the input to be ambiguous, if the corresponding output

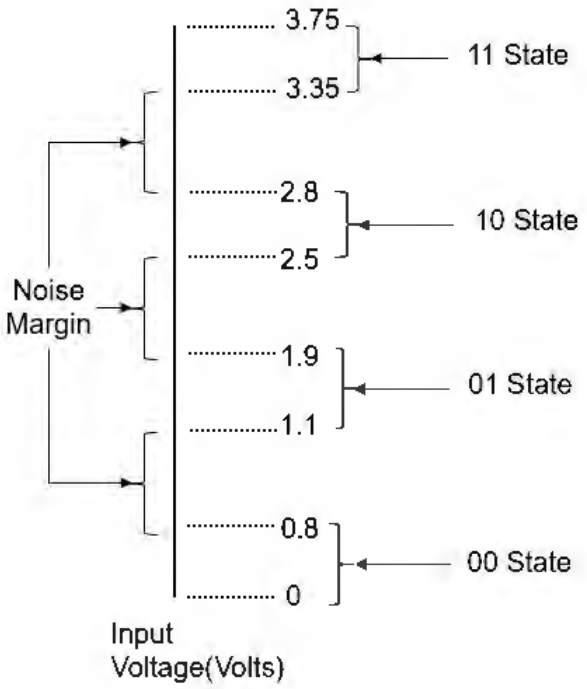

Figure 5.2. Quantization Noise Margins of the binary converter(with 20-domains FeFET) with thresholds set to 1V, 2.5V, 3.35V in input range of $\{0 – 3.75\}$ Volts[20](© 2022 IEEE).

bit voltage falls between $100mV$ and $450mV$. Fig. 5.2 illustrates quantized input voltage range and the noise margin for the circuit with 20-domains FeFET with input range $0V < V_{in} < 3.75V$, for which the V_t values are $V_{t1} = 1V, V_{t2} = 2.5V, V_{t3} = 3.35V$.

For example, $1.1V < V_{in} < 1.9V$ gets converted to "01"(output = $Bit0 < 100mV$, $Bit_1 > 450mV$), whereas an input voltage $V_{in} = 3V$ drives the $Bit0$ output to $\sim 200mV$ which is neither $logic0$ nor $logic1$ and considered an error or noise. The noise regions can be reduced or increased depending on the reliability demand from applications.

5.3. Adaptable Quantization Step and Input Range

The number of domains is directly correlated with the FeFET size, i.e., the smaller the FeFET, the less the number of domains. A larger number of domains implies more distinct polarizations and corresponding V_ts, leading to flexible quantization steps. Choos-

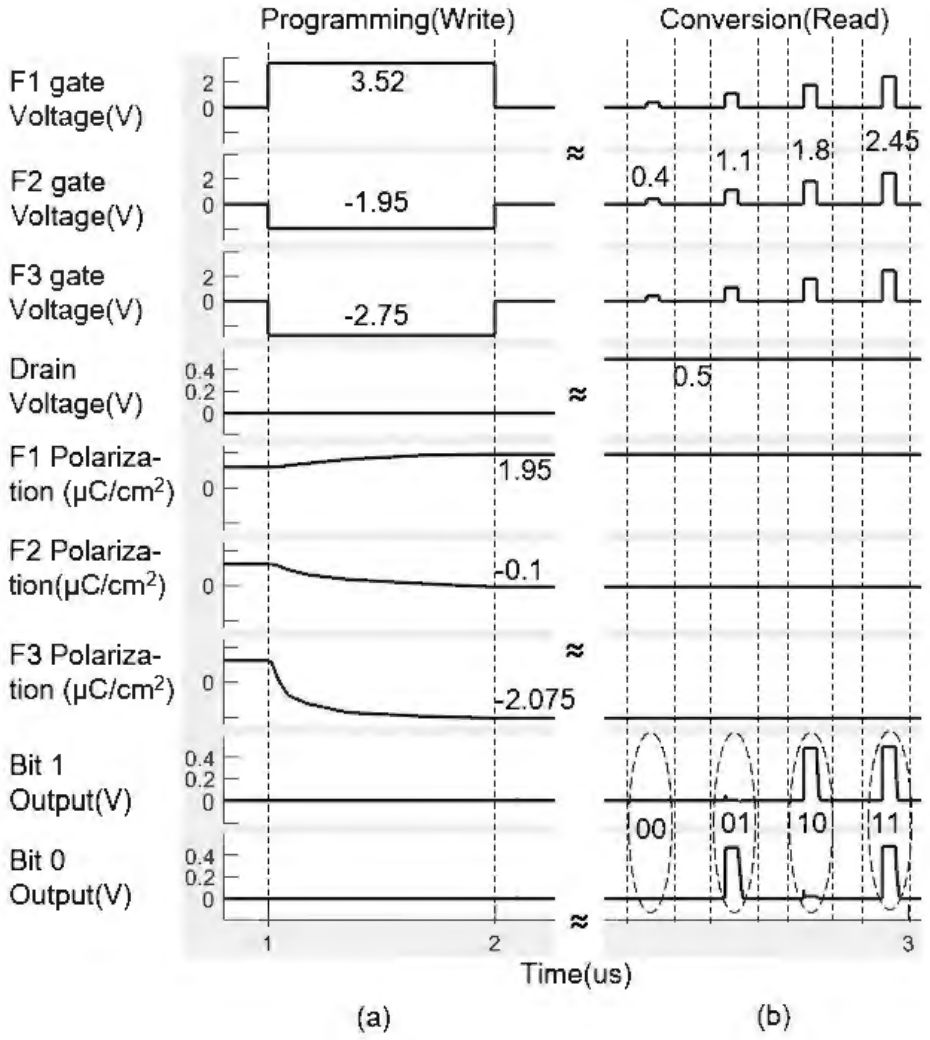

Figure 5.3. Simulation of converter with 2000-domains FeFET. (a)Threshold voltage programming of FeFETs and (b)Input voltage(V_{in}) to bit conversion is shown. V_{in} values {0.4V, 1.1V, 1.8V, 2.45V} get converted to {00, 01, 10, 11}[20](© 2022 IEEE).

ing neighboring V_ts for FeFET programming leads to smaller quantization steps and input range making the circuit suitable for memory technologies requiring low operating voltage. The simulation with 2000-domains is done to get different profile for the conversion operation. However note that smaller quantization step is more error prone due to smaller input quantization noise window. Table 3.3 demonstrates various polarization with distinct threshold voltages (V_t) for FeFET with 2000-domains.

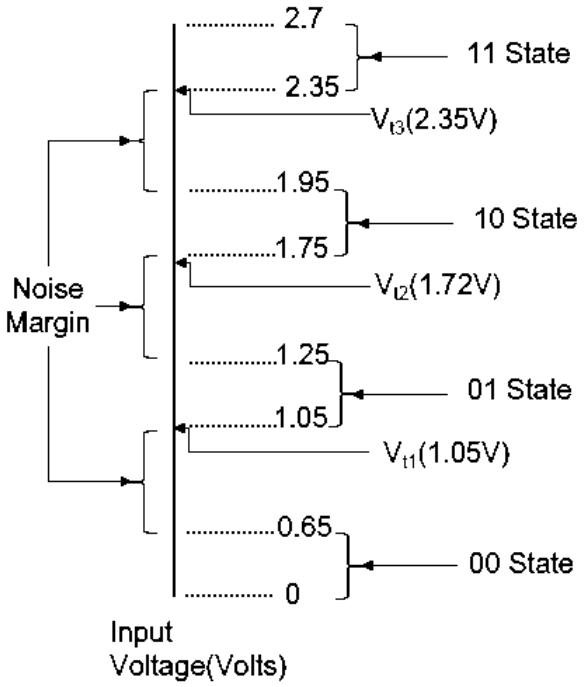

Figure 5.4. Quantization Noise Margins of the binary converter(with 2000-domains FeFET) with thresholds set to 1.05V, 1.72V and 2.35V in the input range of {0 – 2.7} Volts.

Fig. 5.3 illustrates a 4-level to 2-bit conversion using FeFET with 2000-domains, where F1, F2 and F3 are programmed to V_ts of 1.05V, 1.72V and 2.35V with write voltages 3.52V, -1.95V and -2.75V(pulse width: $1\mu s$) respectively, which is captured in Fig. 5.3(a). The input range for conversion is evaluated to be [0, 2.7V]. As shown in Fig. 5.3(b), Input voltages {0.4V, 1.1V, 1.8V, 2.45V} gets converted to {"00", "01", "10", "11"} respectively and the simulation parameters have been captured in Table 5.3.

Table 5.3. Threshold Voltage Programming(2000-domain FeFET, write pulse width: $1\mu s$)

Applied Gate Voltage(V)	Resultant polarization(P)($\mu C/cm^2$)	Threshold Voltage(V)
3.52	1.95	1.05 (V_{t1})
-1.95	-0.1	1.72 (V_{t2})
-2.75	-2.075	2.35 (V_{t3})

The Input Quantization Noise Margin of the converter with 2000-domains FeFET is demonstrated in Fig. 5.4. Thus, it is demonstrated that quantization step and input range is adaptable depending on the choice of different threshold voltage characteristics for the FeFETs.

5.4. Secure Encryption Verification

The programming order of the FeFETs and their corresponding V_t states is considered as $keys$ for encrypting the input voltage to binary output as discussed in section 4.4. The programmed threshold voltage determines if the device turn ON or remain OFF for the applied gate input. Changing the programming order from [V_{t2}, V_{t1}, V_{t3}] to [V_{t1}, V_{t2}, V_{t3}] generates different bit outcomes according to Table 4.1 i.e. input Voltages {0.35V, 1.2V, 2.6V, 3.4V} get converted to {“00”, “10”, “10”, “11”} instead of {“00”, “01”, “10”, “11”}, which is captured in Fig. 5.5 and Fig. 5.1 respectively. This change in output is due to the fact that the change in the V_t programming order generates “010” and “100” thermometer codes respectively for the input voltage $V_{t1} < V_{in} < V_{t2} < V_{t3}$. The thermometer codes then get converted to output bits by the encoder(PFET) accordingly.

5.5. Area Complexity Discussion

Multi-level to binary converters are an integral part of MLC memory peripheral circuitry. These data converters are based on various sensing mechanisms. One such mechanism is the use of Sense Amplifiers(SA) for reference signal comparison to generate thermometer codes. A proper encoding circuit then encodes the thermometer code to corresponding binary output. Our circuit uses just three FeFETs for voltage reference comparison and 3 NFETs for pre-discharge circuitry for thermometer code generation for a 4-level input voltage.

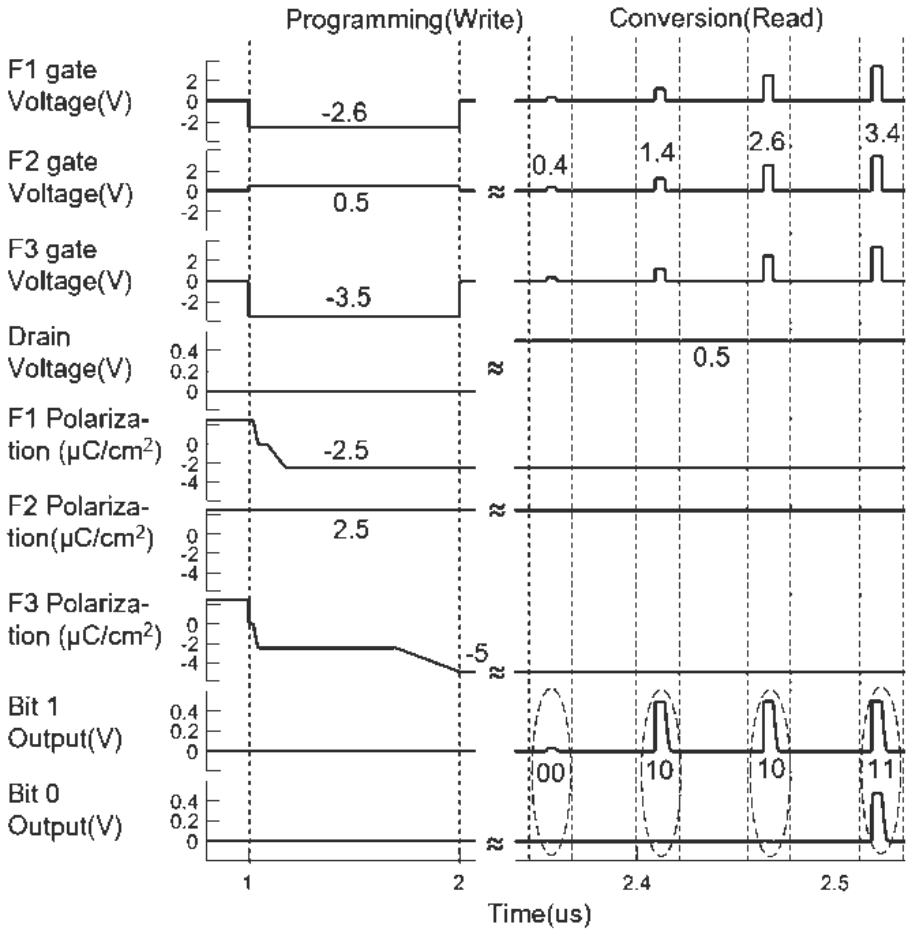

Figure 5.5. Simulation demonstration of security capability. (a)Threshold voltage programming of FeFETs with 20 domains and (b) Input voltage(V_{in}) to output bit conversion is shown. V_{in} values {0.4V, 1.4V, 2.6V, 3.4V} get converted to {00, 10, 10, 11} for key, $V_{t1}V_{t2}V_{t3}$ and {00, 01, 10, 11} for key $V_{t2}V_{t1}V_{t3}$(Fig. 4.1) respectively.

The encoding circuit consists of only a single PFET controlled by one of the signals generated in the previous stage. This simple compact encoder circuit is even simpler than a 2:1 multiplexer, which is faster and more power efficient than other encoders like Wallace, Fat-tree encoders[30][47][16]. Decode scheme explained in [37] uses resistor tree and voltage comparators for V_{in} conversion in Multi-Level RRAM Cells.

The number of transistors in the discharge circuitry can also be reduced based on the subsequent stage of the system. Fig. 5.6 shows the design of a ReRAM MLC multi-

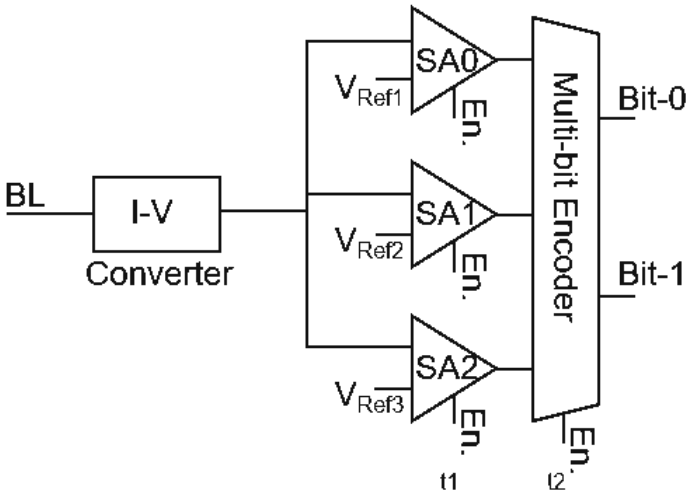

Figure 5.6. ReRAM Parallel sensing of 2Bits/cell read operation[64].

bit converter consisting of I-V converter, reference Sense Amplifiers(SA) and a multi-bit encoder[64]. Sense amplifiers are complex and contain multiple transistors(typically 5 or more[31][38]). In our design a single FeFET replaces the voltage sense amplifier, making the design ultra compact. FeFET act as a voltage reference comparator by exploiting its capability to hold multiple V_t states[25]. Complexity of the circuit is also less compared to the alternate timing based MLC multi-bit converter involving latches used in [64].

5.6. Layout Exercise

A layout exercise for the 4-level to 2-bit converter circuit is drawn using gpdk045 design rules in 45nm technology and shown in the Fig. 5.7. The layout is checked for DRC and LVS. Note that, in this design we assume same layout design and rules for FeFET and NMOS. More compact layout designs for the converter circuit need to be explored for optimization as future work.

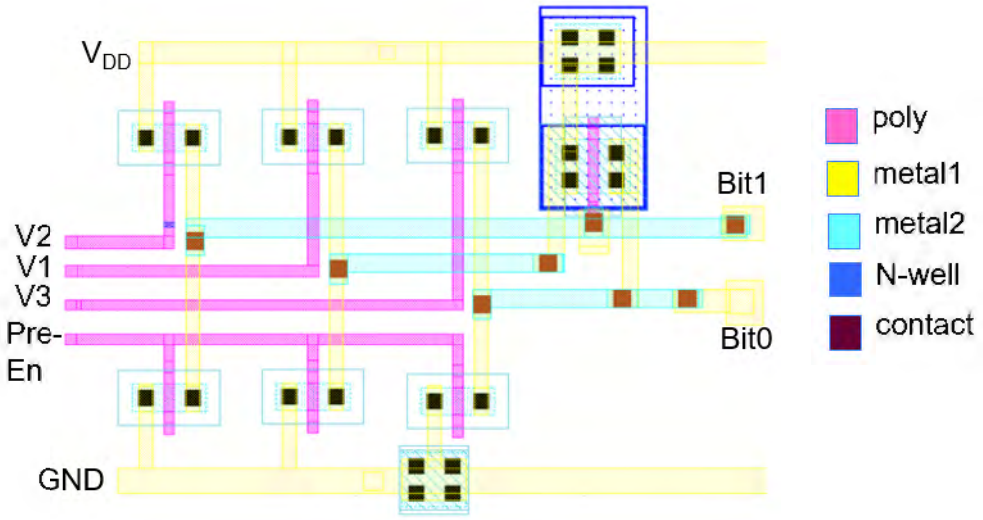

Figure 5.7. Layout drawn for the proposed 4-level to 2-bit converter design.

CHAPTER 6: FUTURE WORKS

An ultra compact multi-level voltage to binary converter is proposed and designed using FeFETs. FeFET multi-threshold voltage(V_t) capability is exploited for reference voltage comparison. A 4-level voltage to 2-bit converter is designed and verified using simulations. The circuit has adaptable input voltage quantization, flexible output bit-width and an inherent security capability making the design versatile. All of these features are possible due to re-configurabilty of the FeFET device. The circuit also encodes the output in incremental manner, which limits the error to the least significant bits(LSB). In comparison with existing voltage to binary conversion schemes, this design is very compact. Analysis on our binary converter design with 20 and 2000-domains FeFET demonstrated an input voltage conversion range of [0V – 3.75V] and [0V – 2.7V] respectively.

In literature it has been demonstrated that the FeFET device is CMOS compatible and has been fabricated in 28nm HKMG technology[12]. However, our work is purely based on circuit design and its functional verification using an FeFET model and simulations. So, in this work we have not examined the fabrication scenario of the design, which is open for future exploration.

As the proposed design is verified using simulations, the next step would be increasing the number of bits at the output by increasing number of FeFETs with distinct V_t states along with re-designing the encoding mechanism accordingly. Fabrication of the design and analyzing its behavior should also be explored. This would provide the information regarding actual performance and efficacy of the design, which then can be used for exploring its physical implementation in multi-bit memory peripheral sensing circuits.

The unique characteristics of FeFET warrants interesting circuit designs while being compatible with CMOS technology. Various multi threshold logic and memory designs can be explored for future work. Due to heavy parallelism in search operation, content addressable memory designs and associative processors are being explored industrially. An FeFET-based CAM engine capable of operating on single and multi-bit data is proposed by Xunzhao Yin et al.[66]. It takes two steps for searching a data in this CAM design. Chao Li et al.[34] have also proposed an FeFET-based multi-bit CAM design, where one CAM cell consists of two FeFETs and a transistor. A simplified version of the CAM design[34] is shown in Fig. 6.1. In this circuit both the first-half and the second-half of the row stores the same data(threshold V1 for '1', V2 for '2'and so on). For search operation, below-threshold and above-threshold search voltages are applied to first-half and second-half of the row respectively. Not-discharged Match Line-1 and discharged Match Line-2 signifies a data "Match", otherwise a "Mismatch". Thus, the design can search a pattern in the CAM array in one step. So, the design may potentially be faster, while it doubles the area with respect to the design in [66]. Similarly memory/CAM array designs needs to be further investigated and explored for designing optimized compute logics like in-memory sorter, comparator etc. for efficient algorithmic implementations.

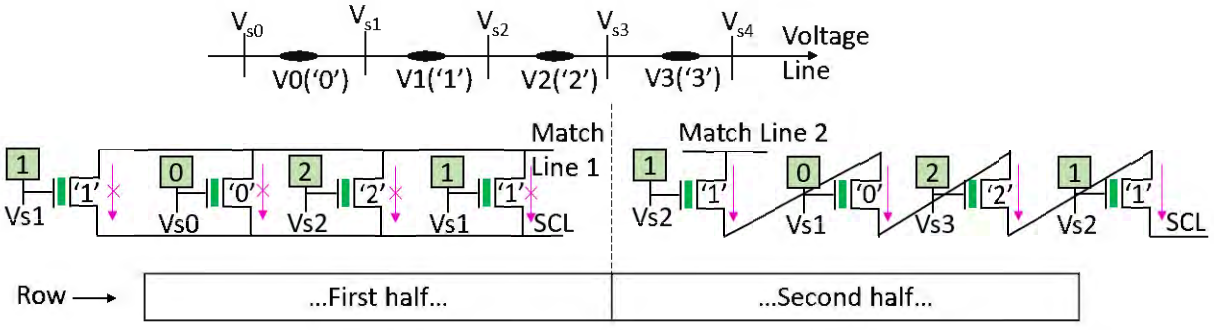

Figure 6.1. FeFET-based Multi-Bit CAM design discussed in [34].

6.1. Remarks

The revolution in computing technology in last couple of decades has seen a constant rate of improvement. The application demands has also been rising parallely. Although the Moore's law had been guiding the industry for a long time in this revolution, in the last decade that has not been case. Many even concluded that Moore's Law has ended. Consequently, the industry started looking into emerging devices for designing novel architectures for storage and processing units. FeFET-based CAM, ReRAM-based crossbar for in-memory compute, FeFET-based multi-bit memory etc. are some of the examples of these new compute designs. The increasing demand for more efficient designs will keep pushing us to look for innovative computing solutions.

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APPENDIX A. SIMULATION PROCESS

The proposed converter design was verified using simulations in Virtuoso(version 6.1.8-64b) ADE-XL simulator environment by using NCSU 45nm Basekit[41] and a multi-domain FeFET model[21]. We first draw the schematic of the design as shown in Fig. A1 in the Virtuoso editor.

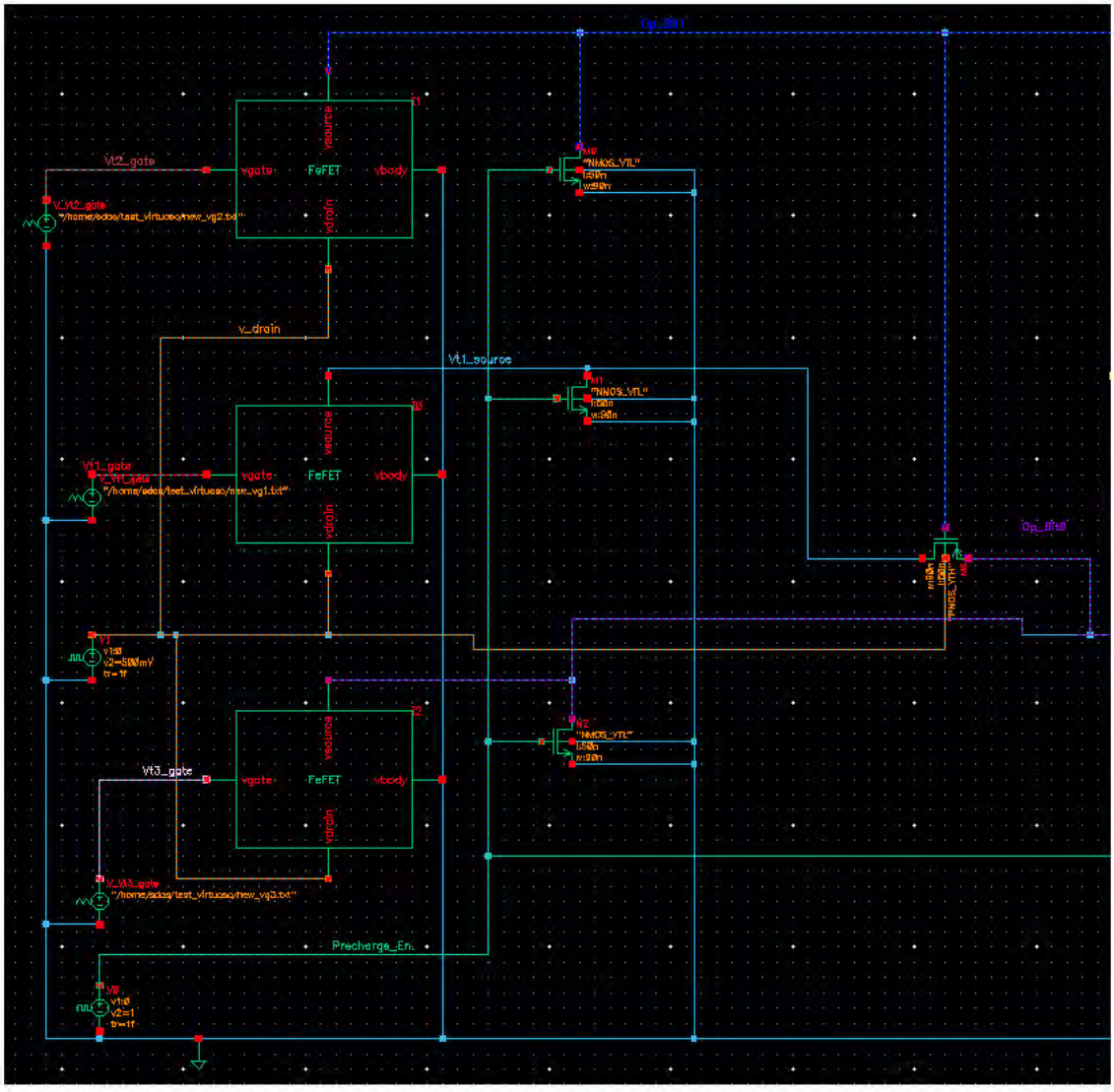

Figure A1. Circuit Schematic designed in Virtuoso ADE-Xl simulator.

In the Fig. A1 the square blocks are the FeFETs(F1, F2, F3) followed with three NFETs(NCSU Basekit NMOS_VTL) used for discharge path and a PFET (NCSU Basekit PMOS_VTL) used as encoder. Each FeFET gate terminal is connected to a Voltage Piece-wise Linear File(vpwlf) voltage source, through which the FeFETs are provided with write and read pulses for the conversion operation. The pre-discharge enable is connected to a pulsating voltage source and provided with pulses for enabling the discharge path before an input is applied for conversion.

A.1. Voltage Piece-wise Linear File Script

The voltage piece-wise linear files(vpwlf) are written as the following.

```
t_rise 0

t_rise+t_rest 0

t_rise+t_rest+t_rise  0

t_rise+t_rest+t_rise+t_set 0

t_rise+t_rest+t_rise+t_set+t_rise 0

t_rise+t_rest+t_rise+t_set+t_rise+t_rest  0

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise v_write1

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set v_write1

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise 0

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest 0

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
0

t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1 0
```

```
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise   v_read1
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read v_read1
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise  v_read2
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read v_read2
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise
0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
```

```
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise v_read3
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read v_read3
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read+t_rise 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read+t_rise+t_rest1 0
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read+t_rise+t_rest1+t_rise v_read4
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read+t_rise+t_rest1+t_rise+t_read v_read4
t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise+t_set+t_rise+t_rest+t_rise
+t_set1+t_rise+t_rest2+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise+
t_rest1+t_rise+t_read+t_rise+t_rest1+t_rise+t_read+t_rise 0
```

The variables used in the piece-wise linear script are given values in the Simulation setup window as shown in Fig. A2, otherwise the console will throw error when we run the simulation.

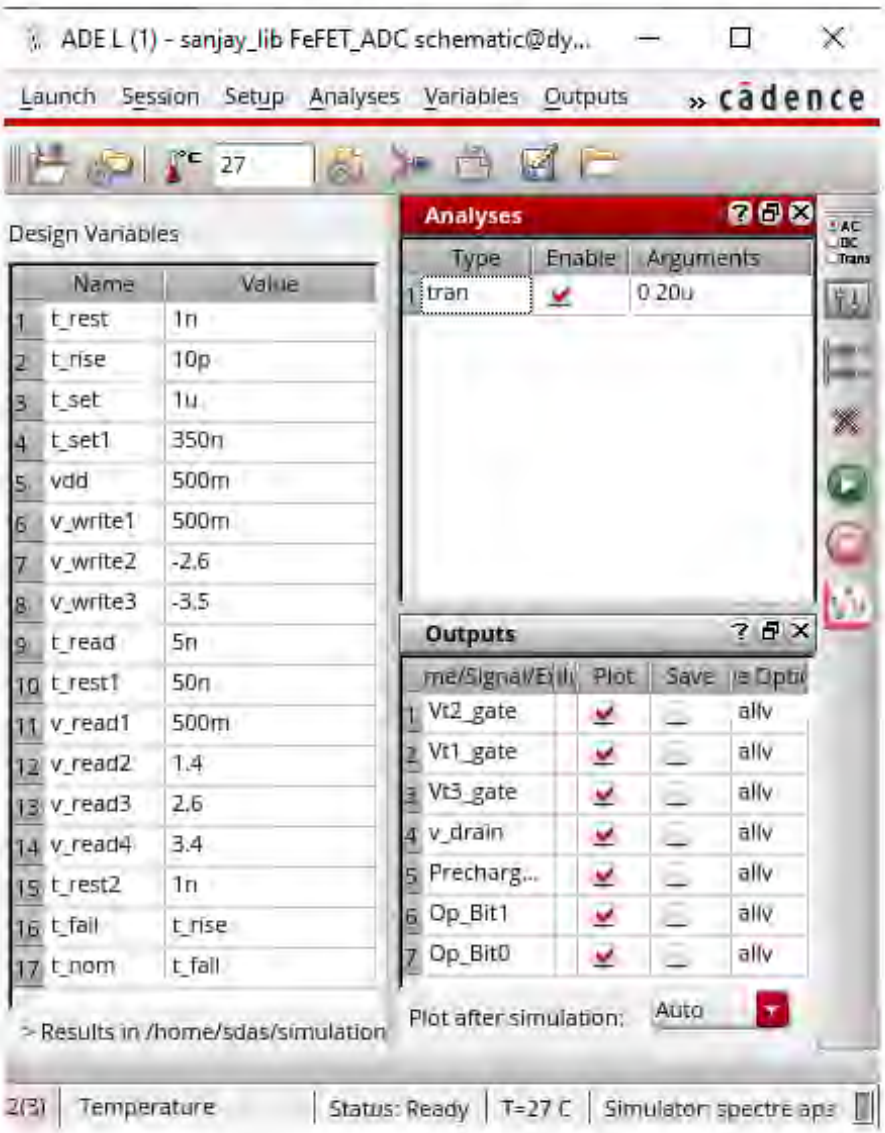

Figure A2. Simulation setup for the proposed converter design.

We vary the variable values in the console for testing and verifying functionality of the design. There is a parameter named “ndom” in FeFET model , by varying the value of which we vary the number of domains for the FeFETs in simulation. We study the FeFET behaviour and verify the proposed binary converter design using simulations.

Virtuoso Simulation of the 4-level to 2-bit converter designed with FeFET with 20-domains is shown in Fig. A3. We simulated the FeFET device and the converter circuit

countless times by varying various parameters to capture the conversion characteristics. These simulation data are exported for plotting the wave-forms in MATLAB.

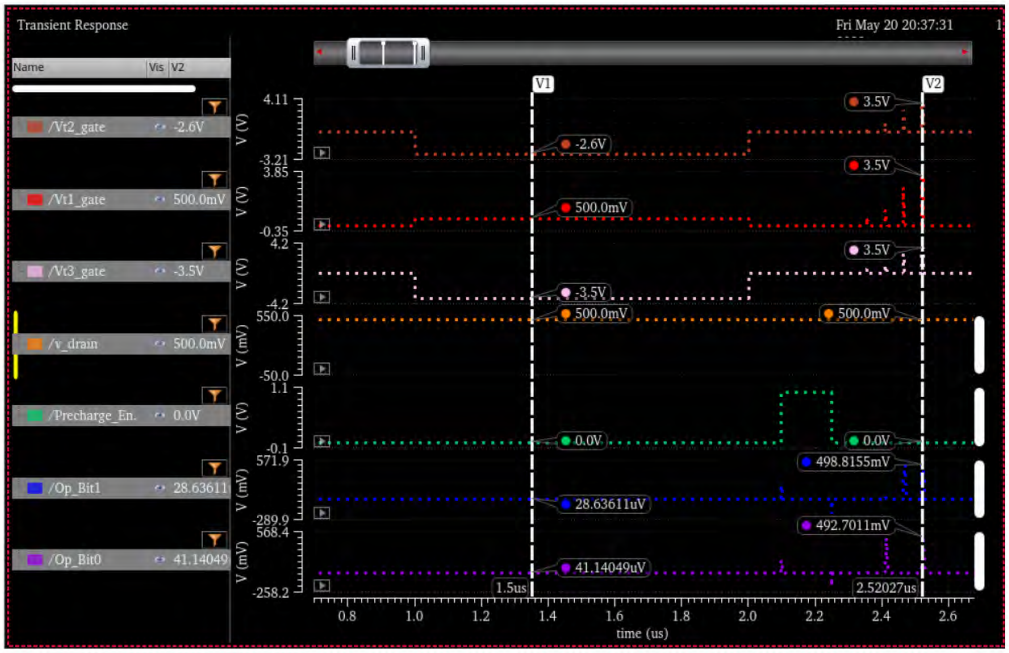

Figure A3. Virtuoso Simulation of the 4-level to binary converter designed with FeFET with 20-domains.

A.2. Sample of Exported Data

The data captured and exported for plotting wave-forms looks like the following.

```
Vt1_gate X Vt1_gate Y Vt2_gate X Vt2_gate Y Vt3_gate X Vt3_gate Y v_drain X
v_drain Y I0:sumq X I0:sumq Y I1:sumq X I1:sumq Y I2:sumq X I2:sumq Y
Op_Bit1 X Op_Bit1 Y Op_Bit0 X Op_Bit0 Y
0 0 0 0 0 0 0 0 0 12.5 0 12.5 0 12.5 0 3.09E-07 0 1.54E-07/
3.50E-08 0 3.50E-08 0 3.50E-08 0 3.50E-08 0 3.50E-08 5 3.50E-08 5
3.50E-08 5 3.50E-08 2.23E-06 3.50E-08 1.08E-06/
1.05E-07 0 1.05E-07 0 1.05E-07 0 1.05E-07 0 1.05E-07 5 1.05E-07 2.5
```

```
1.05E-07    5 1.05E-07 7.35E-06 1.05E-07 3.27E-06/
2.45E-07 0 2.45E-07 0 2.45E-07 0 2.45E-07 0 2.45E-07 5 2.45E-07 2.5
2.45E-07    5 2.45E-07 5.87E-05 2.45E-07 1.17E-06/
5.25E-07 0 5.25E-07 0 5.25E-07 0 5.25E-07 0 5.25E-07 2.5 5.25E-07 2.5
5.25E-07 2.5 5.25E-07 5.86E-05 5.25E-07 1.47E-05/
1.00E-06 0 1.00E-06 0 1.00E-06 0 1.00E-06 0 1.00E-06 2.5 1.00E-06 2.5
1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.004167857 1.00E-06 -0.021672857 1.00E-06 -0.029175 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.012503571 1.00E-06 -0.065018572 1.00E-06 -0.087525 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.029175 1.00E-06 -0.15171 1.00E-06 -0.204225 1.00E-06  0 1.00E-06
2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.062517857 1.00E-06 -0.325092858 1.00E-06 -0.437625001 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.129203572 1.00E-06 -0.671858572 1.00E-06 -0.904425001 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.262575 1.00E-06 -1.365390002 1.00E-06 -1.838025002 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.395946429 1.00E-06 -2.058921431 1.00E-06 -2.771625003 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.447973215 1.00E-06 -2.329460715 1.00E-06 -3.135812502 1.00E-06 0
1.00E-06 2.5 1.00E-06 2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
```

```
1.00E-06 0.5 1.00E-06 -2.6 1.00E-06 -3.5 1.00E-06 0 1.00E-06 2.5 1.00E-06
2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
1.00E-06 0.5 1.00E-06 -2.6 1.00E-06 -3.5 1.00E-06 0 1.00E-06 2.5 1.00E-06
2.5 1.00E-06 2.5 1.00E-06 5.78E-05 1.00E-06 1.48E-05/
```

The exported data files are plotted using MATLAB scripts for clear and concentrated focus on the important regions of the simulations. An example of the MATLAB scripts used for plotting conversion operation is shown in the following.

A.3. MATLAB Script for Plotting

```
T = readtable('C:\Users\sanjay.das\Desktop\Main\Research\ADC\domain20_without
Inv.csv');
T.Time = (T.Vt1_gateX).*1000000;
newYlabels={'Vg1  ','Vg2  ','Vg3  ','Vdd  ','P1  ','P2  ', 'p3  ','Out1  ',
'Out0  '};
s = stackedplot(T,{'Vt1_gateY','Vt2_gateY', 'Vt3_gateY', 'v_drainY','I0_sumqY',
'I1_sumqY','I2_sumqY','Op_Bit1Y','Op_Bit0Y'},'XVariable','Time','Title',
'FeFETs Programming and data conversion','DisplayLabels',newYlabels,Color='k',
LineWidth=2,XLimits=[2.33 3.1]);
s.AxesProperties(1).YLimits = [-4 4];
s.AxesProperties(2).YLimits = [-4 4];
s.AxesProperties(3).YLimits = [-4 4];
s.AxesProperties(4).YLimits = [-0.2 0.6];
s.AxesProperties(5).YLimits = [-6 2.5];
s.AxesProperties(6).YLimits = [-6 2.5];
```

```
s.AxesProperties(7).YLimits = [-6 2.5];
s.AxesProperties(8).YLimits = [-0.2 0.6];
s.AxesProperties(9).YLimits = [-0.2 0.6];
s.FontSize = 15;
```

MATLAB plotting properties has been used to plot the wave-forms clearly signifying the important regions of the plot such as programming and conversion operation. Figs 5.1, 5.3 and 5.5 captures the MATLAB plotted wave-forms.