CHALLENGE TO NEXT-GENERATION VLSI WITH VFET USING OXIDE SEMICONDUCTOR AND 3D STRUCTURE

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We have been committed to research and development of an oxide semiconductor (OS), and published a book on OSLSI by John Wiley & Sons, Inc., in 2017 [1]. OS has attracted such attention that almost 10% of the accepted papers was related to the field at the IEEE International Electron Devices Meeting (IEDM), the world's largest international conference on semiconductor manufacturing, held in December 2022. In the tutorial taught by IBM on the first day of IEEE IEDM 2022, the necessity of vertical field-effect transistors (VFETs) and stacked FETs was anticipated for beyond-1-nm-node semiconductors that are next to the 2- to 3-nm-node semiconductors [2]. A gate-all-around (GAA) structure has been proposed as the new structure in the Si VLSI field. However, we propose a VFET structure that goes a step ahead of the GAA structure and are convinced that a VFET using OS and a 3D structure (stack structure) in which the VFETs are stacked vertically will be the next mainstream. While a variety of scaling techniques has been considered, we proposed the VFET more than a decade ago, in 2012 and have been granted patents for the VFET technologies [3-5]. In addition, I had an opportunity to give a plenary lecture on the 3D structure [Figure 1] in which FETs having a gate last (GL) structure are stacked at an international conference, CIMTEC2022, held in Perugia, Italy, in June 2022 [6-7]. The presented technology has been further enhanced to this day.

We have prototyped a 5.72-inch smartphone display including VFETs using OS for the backplane for the first time in the world [Figure 2]. This display includes 67×10^6 OSFETs. In addition, we have been considering displays for AR/VR devices, which have been rapidly widespread in recent years, as the first product employing OSLSI in which OSFETs having the GL structure are stacked over SiFETs, and have prototyped a 1.5-inch AR/VR display [Figure 3]. The AR/VR display includes 232×10^6 OSFETs and 27×10^6 SiFETs and has a 3D structure in which the OSFETs are stacked over the SiFETs. The OSFET having the GL structure and the OSFET having the VFET structure are expected to be indispensable for the future display backplane. In this presentation, I will introduce the OSFET having the GL structure, the OSFET having the VFET structure, and their characteristics in detail.

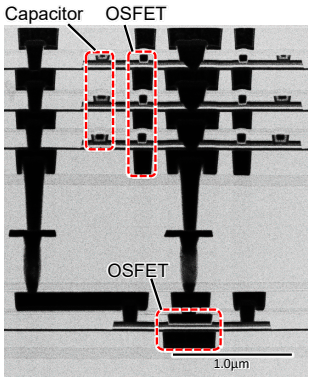
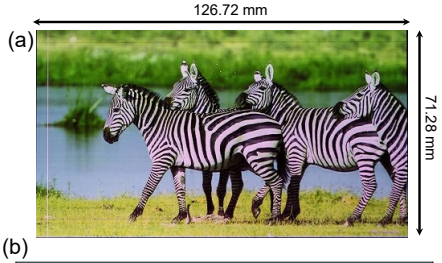
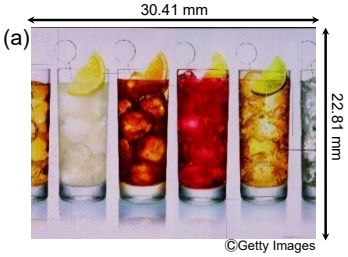


Figure 1 – Cross-sectional image of stack structure (3D structure) using OS



Specifications	
Panel size	5.72 inch diagonal 71.28 mm(H)×126.72 mm(V)
OSFET	66,600,000 FETs
Pixel count	1440 × RGB(H)× 2560(V)
Pixel density	513 ppi
Sub-pixel size	16.5 μm(H) × 49.5 μm(V)
Coloring method	RGB Side by Side

Figure 2 – Smartphone display (a) photograph of panel (b) specifications



Specifications	
Panel size	1.50 inch diagonal 30.41 mm (H) × 22.81 mm (V)
OSFET / SiFET	232,243,200 FETs / 26,800,000 FETs
Brightness	5k cd/m² ～
Pixel count	3840 (H) × 2880 (V)
Pixel density	3207 ppi
Sub-pixel size	2.64 μm (H) × 7.92 μm (V)

Figure 3 – AR/VR display (a) photograph of panel (b) specifications

References

[1] “Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI”, John Wiley & Sons, 2017. [2] T. Yamashita: presented at IEDM Tutorials 2022. [3] Japanese Patent 6,745,924. [4] US Patent 10,038,011. [5] Korean Patent 2,407,627. [6] S. Yamazaki, Plenary Lecture at 15th International Ceramics Congress, CIMTEC 2022, Italy. [7] S. Yamazaki *et al.*, “C-axis aligned crystalline indium–gallium–zinc oxide ceramics and oxide semiconductor LSI as countermeasures against global warming”, Ceramics International (To be published).