## WHAT CAN WE DO WITH FERROELECTRIC GATE?

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Thin film transistors (TFTs) are one of the key devices in flat panel displays and oxide channel TFTs are currently employed in such applications. Adding functionality to TFTs is an interesting topic for exploring new applications and ferroelectric materials are promising candidates to add functionality to TFTs. When the ferroelectric material is used as a gate insulator, the device has nonvolatile memory function. In addition, we pointed out that the ferroelectric gate can induce much larger charge density than the conventional paraelectric gate insulator [1]. As a result, conductive oxide such as indium-tin oxide (ITO) can be used as a channel, if the thickness is sufficiently thin. Figure 1 show transfer curve of a ferroelectric-gate TFT using Y-doped Hf-Zr-O (Y-HZO) as the gate insulator and 13-nm-thick ITO as the channel [2]. Both layers were fabricated by chemical solution deposition (CSD). Normal n-channel transistor operation was obtained even though a conductive oxide is used for the channel. A large on/off ratio, large on current, with a clear hysteresis loop due to the ferroelectric nature of Y-HZO gate insulator are observed.

For ITO channel ferroelectric-gate TFTs, thick ITO can be also used as source/drain electrodes. Therefore, as shown in Figure 2, the same material, ITO, can be used for both channel and source/drain, and the thickness determines its role. Such structures can be fabricated by one step of the direct nanoimprint process [3]. The use of conductive channel also makes it possible to easily fabricate NAND structures, series connections of the memory transistors, since both transistor channels and local connections can be fabricated simultaneously. Figure 3 shows an example of a NAND structure using ITO-channel ferroelectric-gate TFTs. By simply depositing the ITO channel regions across the bottom gate electrodes, we can fabricate NAND matrix without any metallization process. We demonstrated a NAND structure using ITO channel ferroelectric gate TFTs and investigated the memory operation, in which the memory cell consists of one memory transistor and one pass transistor [4]. Note that the conductive oxide channel ferroelectric gate TFT is applicable to 3D NAND structure, too. In the present 3D NAND flash memory, poly-silicon is used as a channel, which has large resistivity. Replacing the channel material and the gate stack with the conductive oxide and ferroelectric gate insulator, respectively, is expected to significantly reduce the series resistance along with the high-speed operation of the memory transistors.



Figure 2. Transfer curve of ITO channel ferroelectric-gate TFT with Y-HZO gate insulator [1].





Figure 2. Ferroelectric gate TFT with thin ITO channel and thick ITO source /drain regions.

Figure 3. Example of NAND structure using ITO channel ferroelectric-gate TFTs.

[1] T. Miyasako, M Senoo, and E. Tokumitsu, Appl. Phys. Lett., 86, 162902 (2005).

[2] Mohit, T. Miyasako, and E. Tokumitsu, Jpn J. Appl. Phys., 60, SBBM02 (2021).

[3] K. Haga, Y. Kamiya, and E. Tokumitsu, Jpn J. Appl. Phys., 57, 02CB14 (2018).

[4] B. N. Q. Trinh, T. Miyasako, T. Kaneda, P. V. Thanh, P. T. Tue, E. Tokumitsu, and T. Shimoda, Ext. Abst. 2011 Intern. Conf. Solid State Devices and Materials (SSDM), Nagoya (2011) pp.967-968.