LATCH-UP ISSUE BETWEEN HIGH-VOLTAGE CIRCUIT DOMIAN AND LOW-VOLTAGE CIRCUIT DOMAIN IN TFT LCD DRIVER IC FABRICATED WITH BCD PROCESS

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Key Words: Latch-up, bipolar-CMOS-DMOS (BCD) technology, N-buried layer (NBL), TFT LCD driver.

To drive the TFT LCD display panel, the driver ICs must be equipped with the low-voltage (LV) circuits and high-voltage (HV) together in a single chip to achieve the necessary circuit functions. The LV circuits are used to receive and decode the input signals from computers, as well as the HV circuits are used to send the output signals to the TFT LCD panel for display. With mixed-voltage circuits integrated in a single chip, the parasitic lateral latch-up path wouldl be formed between the neighboring HV-to-LV circuit blocks. When such a parasitic latch-up path was triggered on by external overshooting/undershooting transient noises, it would cause serious burned-out failure located between the HV-to-LV circuit blocks in the chip.

The TFT LCD driver ICs are often fabricated by the bipolar-CMOS-DMOS (BCD) technology with the N-buried layer (NBL) to isolate the LV circuit blocks from the common p-type substrate. In this work, the parasitic latch-up path between HV PNP ESD device and the LV circuit block was investigated in a 0.18-μm BCD technology. Fig.1(a) showed the test structure to investigate the latch-up issue between the HV PNP ESD device (provided by the foundry) to the LV circuit block isolated by a NBL layer from the common p-substrate. The NBL layer was biased to VDDE of 5V, typically. There is a parasitic latch-up path existing from the VCC-connected P+ diffusion (inside the PNP ESD device) to the VDDE-connected NBL/NVNW/N+ region (isolating the LV circuit block from the common p-substrate). If the holding voltage of this parasitic latch-up path was lower than the voltage difference between VCC and VDDE, the latch-up issue between power domains (VCC to VDDE) would be initiated to cause the circuit malfunction or even burned out. To overcome this latch-up issue, the NBL/NVNW/N+ region is biased to VDDE via a Schottky junction, as shown in Fig. 1(b). The Schottky junction diode was provided by the foundry for some HV applications. By replacing the contact by the Schottky junction to connect the NBL/NVNW/N+ region to VDDE, the holding voltage of this parasitic latch-up path will be expected higher than the voltage difference between VCC and VDDE. Therefore, the latch-up issue will not happen between VCC and VDDE in the HV and LV mixed circuit blocks in the TFT LCD driver ICs.

A test chip drawn with the test structures had been fabricated in a 0.18-μm BCD technology. The measured DC I-V characteristics of latch-up paths from VCC to VDDE are showed in Fig.2(a) and 2(b). In Fig. 2(a), the holding voltage of the parasitic latch-up path (with the test structure in Fig. 1(a) is 6.72V, measured by the curve tracer (Tek370B) at room temperature (25 °C). In Fig. 2(b), the holding voltage of the parasitic latch-up path (with the test structure in Fig. 1(b) is 40V. With a holding voltage of up to 40V, the latch-up immunity between HV and LV circuit blocks in the mixed-voltage TFT LCD driver ICs can be significantly improved. The latch-up test results with the corresponding voltage/current waveforms in time domain will be demonstrated in the presentation.

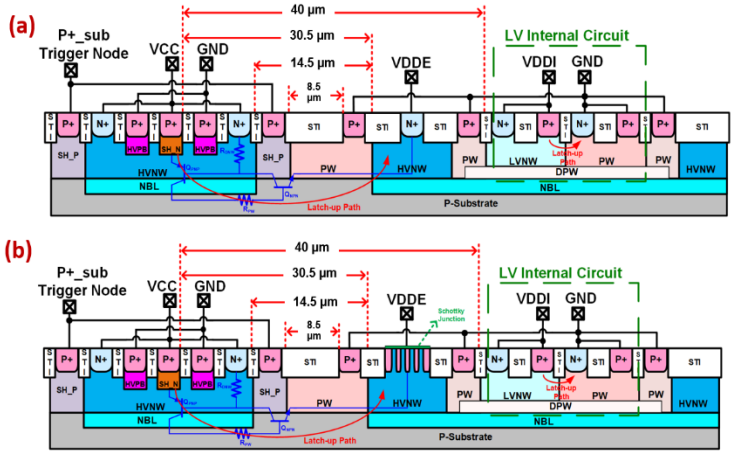

Figure 3 – The latch-up paths from the HV PNP device to the LV circuit block. (a) the LV circuit is isolated by a NBL layer that biased at VDDE, and (b) the LV circuit is isolated by a NBL layer that biased at VDDE through a Schottky junction.

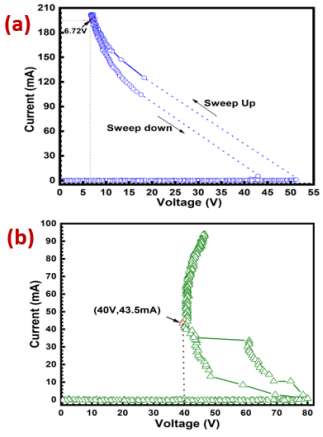

Figure 2 – The measured DC I-V characteristics of latch-up paths from VCC to VDDE with (a) the test structure of Fig.1(a), and (b) the test structure of Fig.1(b).