VERTICAL CHANNEL-ALL-AROUND IGZO FET FOR LOW LATENCY, HIGH-DENSITY 2T0C 3D DRAM APPLICATION

Di Geng, Institute of Microelectronics of the Chinese Academy of Sciences
digeng@ime.ac.cn
Chuanke Chen, Institute of Microelectronics of the Chinese Academy of Sciences
Xinlv Duan, Institute of Microelectronics of the Chinese Academy of Sciences
Ling Li, Institute of Microelectronics of the Chinese Academy of Sciences

Key Words: Vertica FET, channel-all-around, IGZO, 3D Dram.

DRAM devices are an essential component of most digital devices and they play a crucial role in the development of cloud computing, edge computing, Internet-of-Things and Artificial Intelligence. Currently, DRAM scaling is now facing challenges largely due to the mismatch of the reduced storage capacitance and increasing off-current. IGZO based field-effect transistors (IGZO FETs) are very well known for their very low I_{OFF} (<10^{-22}A/μm), representing a solution for reducing the DRAM cell leakage. The demonstration of BEOL-compatible long-retention 2T0C DRAM cell based on the IGZO-FETs shows a very promising approach to overcome the mismatch challenge of the traditional 1T1C DRAM cell. We demonstrated vertical channel-all-around IGZO FETs for ultra-high-density DRAM with $4F^2$ bit-cell area and long retention time of over 300 seconds. And the scaling capability and reliability of vertical CAA IGZO FET has been investigated and valuated with process critical dimension (CD) down to 50nm. The high driving current of 32.8 μA/μm, small subthreshold swing of 92 mV/decade, good thermal reliability and stability shows that the vertical IGZO FET is a promising candidate for the ultra-high density 3D DRAM/SoC applications in the future.

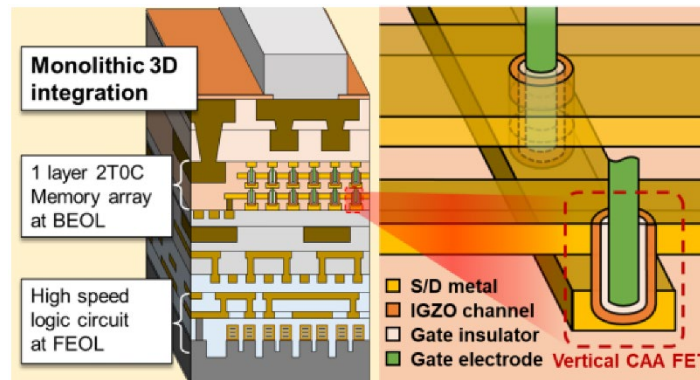

Figure 1 – The schematic of 3D memory chip with IGZO memory array in the BEOL and logic circuit in the FEOL, and the zoom in for details of a vertical CAA FET.

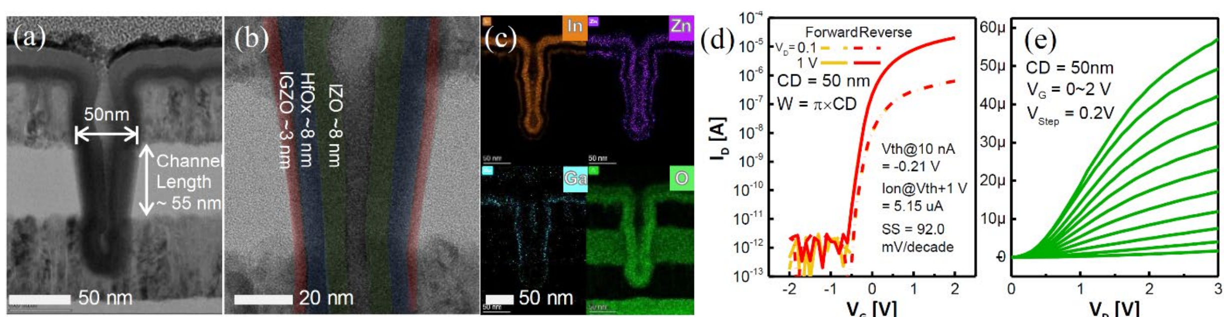

Figure 2 – (a) TEM cross-section of a IGZOFET with about 50 nm CD. (b) Zoom-in TEM image of the channel region with IGZO, HfOx and IZO film layers denoted. (c) Element mapping of the CAA FET by EDS. (d). Transfer curves and (e) Output curves of the CAA FET with 50 nm CD.