AN OVERVIEW OF THE THREE-DIMENSIONALLY STACKED DYNAMIC RANDOM ACCESS MEMORY

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As the DRAM scaling proceeds, challenges related to device integration are becoming overwhelming. The challenges include securing the cell transistor performance, cell capacitance, and low wire resistance. The current two-dimensional integration will meet a significant barrier for further device integration near the design rule of ~ 10nm, which will happen within the next ten years. The die-stacking technology, making the high-bandwidth memory, is an alternative approach but lacks cost-competitiveness. Therefore, cell-stacking technology will be needed for the higher-density DRAM fabrication up to tera-bit, which has been implemented in the vertical-NAND flash. However, DRAM requires a much higher cell transistor performance than the NAND flash, where the polycrystalline Si could meet cell transistor requirements. Such a requirement renders the integration process far more complicated and costs much more than NAND flash. Besides, due to its inherently lower bit line capacitance, the three-dimensional DRAM may have a lower need for cell capacitance than the current DRAMs. Even capacitance-less cell technology is possible when adopting separate writing and reading transistors. Therefore, it has pros and cons in various aspects. This talk will give an overview of the current DRAM technology, stressing its limitations and reviewing the existing ideas on integrating the DRAM cells in three-dimension.