VERTICAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTOR WITH EXTREMELY LOW OFF-STATE CURRENT

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Oxide semiconductor field-effect transistors (OSFETs) are actively developed for display applications. An OSFET exhibits a lower off-state current than a silicon FET and enables low-frequency driving. We developed the measurement method and revealed the OSFET exhibits an extremely low off-state current [1]. In addition, we discovered a c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) which was unique crystal morphology [2]. A display with a backplane formed using CAAC-IGZO FETs achieves low power consumption owing to idling-stop driving that allows an extremely low refresh rate [3].

A reason for the extremely low off-state current of the OSFET is that the OS has a wide band gap. Because of the wide band gap of the OS, electron injection from the source to the channel due to thermal excitation is less likely to occur in a low Vg state, and hole injection from the drain to the channel is less likely to occur because the electron affinity of the OS is close to the work function of source/drain electrodes. There is concern that hole tunneling from the drain to the channel may occur when a drain voltage is applied; however it is suggested that the probability of hole tunneling is low because the effective mass of a hole in the OS is large [4].
In general, a factor causing an off-state current in a transistor is a defect in the channel. In OS, the existence of deep defect states in the band gap is widely known. Although the deep defect states in the band gap might cause the generation of an electron-hole pair, the possibility of the generation is probably low owing to the wide band gap of the OS [5, 6]. The device simulation results of OSFET suggested that the off-state current was increased when deep defect states were introduced in the bandgap [6]. However, the relationship between a deep state and an off-state current is not clear, and thus further research on the mechanism of off-state current in an OSFET is necessary.
We are developing a vertical field-effect transistor (VFET) using OS for the purpose of achieving an FET having a smaller layout area on a glass substrate than that of a conventional planar FET [7]. The layout area of the VFET can be reduced to be approximately one third of that of a planar FET, and its size can be the same as that of a contact hole.
We fabricated an OS VFET on a glass substrate and measured the off-state leakage of the OS VFET. As for the device size of the fabricated OS VFET, the channel length was 0.5 μm and the channel width was 6.3 μm. The channel was formed by sputtering with the use of an IGZO target (In:Ga:Zn = 1:1:1). Although the channel length was on the order of submicron, which is shorter than that of an usual FET used for a display backplane, the OS VFET was found to exhibit good Id-Vg characteristics. The measurement of the off-state current was conducted by the method shown in Reference [1] and showed that the off-state current of the OS VFET was lower than 1 zA/μm at 85 °C (lower than 1 yA/μm at room temperature when extrapolated).

In this presentation, we will show data on the off-state current of VFETs whose channels are formed with OS of different compositions and also discuss the mechanism of the extremely low off-state current of the OSFET.

References
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