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(54) **TAPERED MULTIPATH INDUCTORS**

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CPC **H01F 27/2804** (2013.01); **H01F 17/0006** (2013.01); **H01F 27/29** (2013.01); **H01L 28/10** (2013.01); **H03B 5/12** (2013.01); **H01F 2017/0046** (2013.01); **H01F 2017/0073** (2013.01)

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See application file for complete search history.

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(57) **ABSTRACT**

In an embodiment, an integrated circuit die includes a semiconductor substrate, patterned metal layers compiled over the semiconductor substrate, and a tapered multipath inductor formed in the patterned metal layers. The tapered multipath inductor includes, in turn, an inductor input terminal, an inductor output terminal, and N number of parallel inductor tracks electrically coupled between the inductor input terminal and the inductor output terminal. The parallel inductor tracks wind or wrap around an inductor centerline to define a plurality of multipath inductor windings including an innermost winding and an outermost winding. The parallel inductor tracks further vary in track width when progressing from the outermost winding to the innermost winding of the plurality of multipath inductor windings.

18 Claims, 6 Drawing Sheets

