Voltage Balance for Five-Level DCC Based on Mixed-Integer Linear Programming

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ABSTRACT

In power converters, the modulation stage commands the switching devices to drive the converter outputs to the voltage required by the inner controllers in order to achieve their objectives. However, in multilevel converters, the modulation may be in charge of an additional goal since it also has to tackle with the capacitor voltage balancing issue. This paper formulates the modulation of multilevel three-phase power converters, specifically a five-level diode-clamped converter (DCC), as a mixed-integer linear optimization problem. In this paper, it is shown that the presented optimization problem can deal with the capacitor voltage balance at the same time that the number of commutations is minimized. The problem is solved offline and its solution is stored in a lookup table to be used during normal operation. Then, an online procedure to obtain the levels that modulate each phase from the lookup table is given. Comparisons with model predictive control, space-vector-based algorithms and other modulation approaches are presented in simulations. Several experimental results are presented showing the feasibility of this approach with changes in the operating conditions.

1. Introduction

Multilevel converter technology has been available in the power electronics field for decades [1, 2]. However, as the number of levels increases so does the number of switches and therefore the control complexity. Despite this, multilevel converters present numerous benefits that, with an appropriate control approach, can easily overcome them. The use of several levels instead of two entails a smoother behaviour of the controlled current, which implies a reduced current distortion, in addition to a reduction of the voltage stress of each switching device. Therefore, multilevel converters are a perfect candidate topology for medium-voltage and grid-connected applications where fulfillment of tight grid codes are required [3, 4].

Among the topologies of multilevel converters, the diode-clamped converter (DCC) is still under study and it is the most widely used in all types of industrial applications [5]. However, five-level DCC still finds some reluctance in its implementation due to the control complexity and the unresolved issues it has in comparison with the well-accepted three-level version. These issues are mainly related to how the switches are commanded—i.e the modulation stage—in which some additional constrains and several objectives have to be taken into account in comparison with the two-level version. Consequently, a proper design of the modulation stage is then required to make the five-level DCC a suitable option.

Many modulation techniques for multilevel converters have already been presented [1] which generally can be classified into three categories: 1) Space-vector based modulation (SVM) techniques [6, 7], 2) voltage-level based algorithms [8–10] and 3) techniques that directly compute the switching states at each sampling time such as [11–13]. SVM techniques modulate a voltage vector in the $\alpha\beta$ frame, computed by a previous control stage, by switching among a linear combination of the nearest discrete switching states. Voltage-level based algorithms focus on emulating the same vector in the abc frame but individually for each phase using independent carriers and PWM signals, allowing it to integrate the voltage balance control in the control stage. As a result, a staircase of different voltage levels is generated.

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In the third category, one can include finite control-set model predictive control (FCS-MPC) [11, 12] where knowledge about the system is used to select the more appropriate discrete state according to a model-based prediction. In the same line, there are other techniques that optimize a certain performance index, as in [13] where genetic algorithms are used to eliminate specific harmonics from the output voltage; or in [14] where hybrid dynamical systems theory is used to obtain a new control law for three-level converters with stability guarantee.

Space-vector-based algorithms (SVBA) are well-known and considered to be more flexible than other approaches as they select specific switching states that cover the three phases simultaneously, which grants the user with overall control of the commutations, output voltage, common voltage, etc. Nevertheless, the switching states to consider greatly increases as the number of levels does, and new objectives, such as voltage balance, have to be tackled. Alternatively, the second category is easier to implement as it modulates the phases individually without evaluating combined switching states. However, considering the five-level switched inputs individually—being them continuous—makes it difficult to come up with an algorithm that tackles the power and capacitor voltage balancing issues simultaneously. Nevertheless, PWM-based approaches, used by categories 1) and 2), take advantage of its fast-commutation capability to consider an averaged continuous model of the switchings without requiring small sampling times. On the other hand, the third category usually selects the optimum switching state according to a weighted cost function that takes into account some performance indicators and the system model. In this way, these performance indicators—namely, power tracking, number of commutations and capacitor voltage balancing—can be prioritized over others by changing these weights. In contrast to the other categories, the approaches inside this category allow commutations only at the sampling time instants and, thus, they lack the ability of allowing commutations at any time instant inside the sampling period. As a consequence, they usually need larger sampling frequencies to emulate the same switching frequency than PWM-based approaches, in addition to higher computational effort.

This paper, which is an extension of [15], includes different features of categories 2) and 3). Similar to category 2), it uses averaged models, which allows commuting at any time instant with the same sampling frequencies than PWM-based approaches, whereas the switching commands computation is carried out by solving an optimization problem—in this case a mixed-integer linear programming [16] problem—similar to those approaches included in category 3). In contrast to category 3), instead of computing the switching state directly, the resolution of the optimization problem determines which levels per phase are used in the current switching period. For this, the modulation problem is presented analytically with an explicit consideration of the inherent degrees of freedom and constraints and, from this perspective, an optimization problem is formulated. The optimization considers as constrains the fulfillment of the desired output voltage and the capacitor voltage balance, whereas the minimisation of the number of commutations is included in the cost function. This problem is too involved to be solved online and, thus, the modulation criteria is obtained offline and stored as a lookup table (LUT) using normalized system variables as input variables. The online use of the LUT is not trivial since 1) linear interpolation may lead to non-fulfillment of critical objectives and 2) as the optimization problem is solved numerically for given converter parameters, the resultant LUT is, in principle, only valid for that situation. In [15] an algorithm for interpolating the LUT taking into account these considerations was proposed and the approach was validated by simulation.

In comparison with the original proposal [15], this paper proposes an enhancement in the algorithm such that the steady-state behaviour is improved, namely the output current distortion and the number of commutations. Some comparisons are also shown for the overall controller (either the base and the enhanced ones) in simulation with respect to FCS-MPC, SVBA and integrated control modulations (ICM) to highlight their benefits. Additionally, their experimental implementation yielded some issues that were not covered in [15] and, therefore, are addressed in this paper. Finally, an experimental validation is carried out using a grid-connected five-level DCC of 12 kVA.

The outline of the paper is as follows: In Sect. 2 a description of the five-level DCC as a grid-connected rectifier along with its mathematical model is presented. Next, in Sect. 3 the strategy for controlling the currents and powers of the converter is presented. After that, in Sect. 4 the optimization problem is presented and discussed, whereas its implementation into the modulation stage and a modification for steady-state improvement is presented in Sect. 5. Simulation and comparisons with other approaches with Matlab-Simulink® and experimental results are depicted in Sections 6 and 7 respectively. Finally, some conclusions are drawn in Sect. 8.

2. Circuit description and model

This paper considers the converter in rectifier mode with resistive load as it is illustrated in Fig. 1. The ac-side of the converter is connected to the grid through inductances L and to a pure resistive load R at the dc-side. Point i in

Table 1
Switching signal and switching device correspondance.

switching signal	S_1^i	S_2^i	S_3^i	S_4^i
$f_{i1}=1$	0	0	0	0
$f_{i2}=1$	0	0	0	1
$f_{i3}=1$	0	0	1	1
$f_{i4}=1$	0	1	1	1
$f_{i5}=1$	1	1	1	1

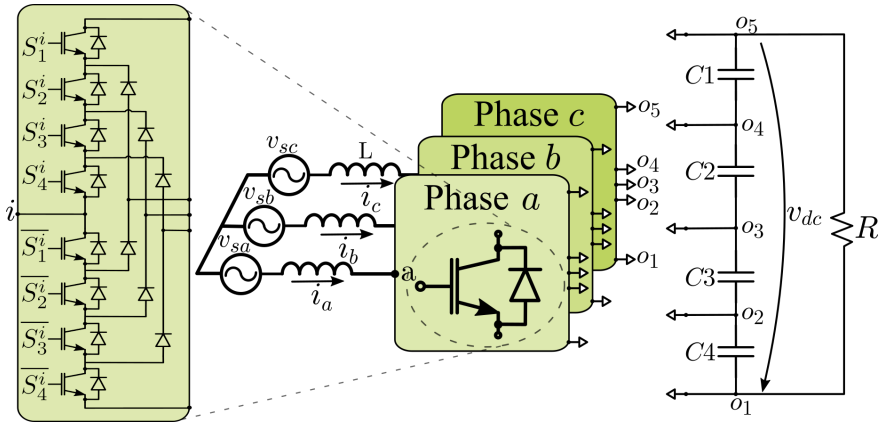

Figure 1: Circuit of a three-phase five-level diode-clamped converter.

Fig. 1 refers to the converter output point of branch i for $i = a, b, c$. The dc-link is composed of capacitors C_1, C_2, C_3 and C_4, with the same capacitance C. Their voltages are represented by v_{c_1}, v_{c_2}, v_{c_3} and v_{c_4}. Besides, the grid phase currents are denoted by i_a, i_b and i_c, while the grid phase voltages are defined by v_{sa}, v_{sb} and v_{sc}.

The output voltages generated in points a, b and c, with respect to the dc-link midpoint o_3, are denoted by v_a, v_b and v_c, respectively. These generated voltages depend on the switching states of the converter, which are determined by the switching functions $f_{ij} \in \{0, 1\}$, for $i = a, b, c$ and $j = 1, 2, 3, 4, 5$, considering that $\sum_{j=1}^{5} f_{ij} = 1$. Each switching signal f_{ij} represents whether the terminal i of the converter is connected to the dc-link point o_j through the corresponding switching devices S_n^i according to Table 1. Notice that $\overline{S_n^i}$ is commanded oppositely to S_n^i. Regarding the voltage balancing issue, the relations between the capacitor voltages are expressed through the balancing error signals denoted as $v_{d_1}, v_{d_2}, v_{d_3}$ and the total dc-link voltage (v_{dc})

$$v_{d_1} = v_{c_1} - v_{c_2} \tag{1}$$
$$v_{d_2} = v_{c_4} - v_{c_1} \tag{2}$$
$$v_{d_3} = v_{c_3} - v_{c_4} \tag{3}$$
$$v_{dc} = v_{c_1} + v_{c_2} + v_{c_3} + v_{c_4}. \tag{4}$$

The dynamic model of the five-level DCC presented in [17] is considered in this paper. According to Kirchhoff's laws, Fig. 1 and the previous definition of the switching functions f_{ij}

$$v_{si} = L\frac{di_i}{dt} + v_i + v_{o_3 n} \quad i = \{a, b, c\} \tag{5}$$
$$v_i = (v_{c1} + v_{c2})f_{i5} + v_{c2}f_{i_4} - v_{c3}f_{i_2} - (v_{c3} + v_{c4})f_{i_1}$$

where $v_{o_3 n}$ is the voltage drop between point o_3 and the neutral point of the grid. Considering a small switching period, the switching functions f_{ij} can be replaced by their respective averaged values denoted as duty ratios d_{ij}, for $i = a, b, c$ and $j = 1, 2, 3, 4, 5$. These duty ratios reflect the part of a switching period in which point i is connected to level j, consequently $d_{i1} + d_{i2} + d_{i3} + d_{i4} + d_{i5} = 1$ and $d_{ij} \in [0, 1]$ have to be fulfilled for $i = a, b, c$ and every j.

Transforming the dynamics (5) from the abc frame to the orthogonal $\alpha\beta\gamma$ frame using the power-invariant Clarke transformation [18] and assuming a balanced three-phase system, the term v_{o_3n} is suppressed.

$$v_{sk} = L\frac{di_k}{dt} + v_k \quad k = \{\alpha, \beta\} \tag{6}$$
$$v_k = (v_{c1} + v_{c2})d_{k5} + v_{c2}d_{k_4} - v_{c3}d_{k_2} - (v_{c3} + v_{c4})d_{k_1},$$

where the homopolar component γ does not appear due to the nature of three-wire system, therefore it has no effect on the current dynamics. Notice that in (6), variable v_k is the average value of the output voltage expressed in $\alpha\beta$. Using the ideas of [19], the degree of freedom associated with γ can be freely exploited.

On the other hand, the time derivative of the current can be controlled by defining the proper value of v_k. In order to do so, it is assumed that the voltage balance has been accomplished and therefore the capacitor voltage unbalances are close to zero, i.e. from (4), $v_{c1} = v_{c2} = v_{c3} = v_{c4} = \frac{v_{dc}}{4}$. In this way, v_k can be normalized dividing it by $v_{dc}/4$. By doing so, it retrieves an expression that does not depend on the capacitor voltages and relates the duty ratios with the generated voltage v_k. Defining normalized variables u_k as

$$u_k \doteq \frac{v_k}{\left(\frac{v_{dc}}{4}\right)} = 2d_{k5} + d_{k4} - d_{k2} - 2d_{k1}; \quad k = \{\alpha, \beta\}. \tag{7}$$

For this, consider that a current (or power) control stage defines at every sampling instant the desired value for u_k. The corresponding values in abc coordinates can be expressed as

$$u_a = \sqrt{\frac{2}{3}}u_\alpha + x = \eta_a + x \tag{8}$$
$$u_b = -\frac{1}{\sqrt{6}}u_\alpha + \frac{1}{\sqrt{2}}u_\beta + x = \eta_b + x \tag{9}$$
$$u_c = -\frac{1}{\sqrt{6}}u_\alpha - \frac{1}{\sqrt{2}}u_\beta + x = \eta_c + x, \tag{10}$$

where $\{\eta_a, \eta_b, \eta_c\}$ have been defined for ease of reading and $x = u_\gamma/\sqrt{3}$ can take any value such that u_i lies in the interval $[-2, 2]$ according to the previous restrictions of d_{ij}. In this way, x must be in the interval $[x_{\min}, x_{\max}]$ with

$$x_{\min} = -2 - \min(\eta_a, \eta_b, \eta_c) \;\; ; \quad x_{\max} = 2 - \max(\eta_a, \eta_b, \eta_c).$$

Regarding the capacitor voltage balance issue, the dynamics of (1)–(3) are obtained by differentiating them with respect to time and applying $i_{o_j} = \sum_{i=a,b,c} d_{ij}i_i$ where i_{o_j} is the current that enters into point o_j

$$C\frac{dv_{d_1}}{dt} = \sum_{i=a,b,c}(-d_{i4}i_i) \tag{11}$$
$$C\frac{dv_{d_2}}{dt} = \sum_{i=a,b,c}(-(d_{i1} + d_{i5})i_i) \tag{12}$$
$$C\frac{dv_{d_3}}{dt} = \sum_{i=a,b,c}(-d_{i2}i_i)\,. \tag{13}$$

Similarly, the dc-link voltage dynamic is retrieved from (4)

$$C\frac{dv_{dc}}{dt} = u_a i_a + u_b i_b + u_c i_c - 4\frac{v_{dc}}{R}, \tag{14}$$

according to (7)–(10).

3. Control strategy

Usually, several control loops are designed in order to achieve the different control objectives that define the proper operation of the converter, namely, desired dc-link voltage, desired behavior for currents and powers and capacitor voltage balance.

The dynamics of the phase currents i_α, i_β are much faster than the capacitor voltages ones [20, 21]. This feature permits the use of a cascaded control with an outer loop that regulates the total dc-link voltage by setting the reference for the inner controller. The inner control itself regulates the fast variables, which are controlled by using u_α and u_β as control inputs. Therefore, the cascaded controller can be summarized in a dc-link regulation loop (v_{dc} tracks its reference v_{dc}^r)—slow dynamics—whose controller output is the power reference (p^r) that has to be tracked by a current/power regulation loop—fast dynamics.

At this point, any of the numerous current/power controllers can be applied [22–27]. In this paper, the control adopted is taken from [27], where p and q are controlled to track their respective references p^r and q^r. Variable q^r, is considered equal to zero to achieve unity power factor. In this way, the chosen controller is a PI

$$\begin{aligned} u_\alpha(t) = {} & u_\alpha^z + k_p v_{s\alpha}\,(p - p^r) + k_i v_{s\alpha} \int_0^t (p - p^r)\,d\tau \\ & - k_p v_{s\beta}\,(q - q^r) - k_i v_{s\beta} \int_0^t (q - q^r)\,d\tau \end{aligned} \tag{15}$$

$$\begin{aligned} u_\beta(t) = {} & u_\beta^z + k_p v_{s\beta}\,(p - p^r) + k_i v_{s\beta} \int_0^t (p - p^r)\,d\tau \\ & + k_p v_{s\alpha}\,(q - q^r) + k_i v_{s\alpha} \int_0^t (q - q^r)\,d\tau, \end{aligned} \tag{16}$$

with the cancellation terms

$$\begin{aligned} u_\alpha^z = & \frac{4}{v_{dc}} \left(\left(1 + \frac{2\pi f L q}{v_{s\alpha}^2 + v_{s\beta}^2} \right) v_{s\alpha} + \frac{2\pi f L p}{v_{s\alpha}^2 + v_{s\beta}^2}\, v_{s\beta} \right) \\ u_\beta^z = & \frac{4}{v_{dc}} \left(\left(1 + \frac{2\pi f L q}{v_{s\alpha}^2 + v_{s\beta}^2} \right) v_{s\beta} - \frac{2\pi f L p}{v_{s\alpha}^2 + v_{s\beta}^2}\, v_{s\alpha} \right), \end{aligned}$$

and k_p, k_i are the proportional and integral controller gains and f is the grid frequency.

The dc-link voltage controller is also chosen as a PI with the error $({v_{dc}^r}^2 - {v_{dc}}^2)$ as the input, p^r as the output and k_p^{dc} and k_i^{dc} as the tuning parameters.

$$p^r = k_p^{dc}({v_{dc}^r}^2 - {v_{dc}}^2) + k_i^{dc} \int_0^t ({v_{dc}^r}^2 - {v_{dc}}^2) d\tau$$

The cascaded controllers end with a modulation stage that should achieve the value of u_α and u_β at the same time that it should equalize the capacitor voltages. Notice that, so far, the duty cycles for the switching devices in abc coordinates are not defined uniquely, since there is still a remaining degree of freedom related to the homopolar component—variable x in (8)-(10). This fact can be exploited for balancing the capacitor voltages but the problem is not trivial and there are several approaches in the literature for this purpose [28, 29]. In the next section, computation of the duty cycles is formulated as a linear mixed-integer optimization problem. Once the duty cycles are computed the output levels can be implemented with an usual PWM procedure.

4. Modulation as an optimization problem

As it was said previously, the modulation stage is in charge of commanding the switching devices in such a way that the power control is properly carried out in the converter. Additionally, because of the nature of multilevel converters, the capacitor voltage balancing issue has to be addressed in this stage as well. Therefore, considering the scheme of the five-level DCC, the modulation stage should decide, at each sampling time, which and for how long phase i is connected to each level j, i.e. the switching signals f_{ij} for $i = \{a, b, c\}$ and $j = \{1, \ldots, 5\}$. Thus, the optimization problem is formulated to compute the duty ratios d_{ij} of every phase i and level j every sampling time. This section shows that a linear mixed-integer optimization problem can be formulated to compute these duty cycles. Due to the computational burden of such optimization, the problem is solved off-line and stored in lookup tables to allow an affordable implementation.

Table 2
Eight possible combinations of signs of v_{d1}, v_{d2} and v_{d3}.

index	1	2	3	4	5	6	7	8
v_{d1}	+	-	+	-	+	-	+	-
v_{d2}	+	+	-	-	+	+	-	-
v_{d3}	+	+	+	+	-	-	-	-

4.1. Input Data

The input data for the optimization problem are the normalized values obtained from simulation of the currents i_a, i_b, i_c—or i_α, i_β as they can be directly transformed to abc—, the output of the power controller u_α and u_β, and the signs of the balancing error signals $v_{d_1}, v_{d_2}, v_{d_3}$. Variables i_a, i_b, i_c, u_α and u_β are assumed to have reached their sinusoidal steady state with unity power factor. As the problem has to be considered at every sampling time, a grid period is considered and discretized over N points. Thus, the optimization problem is solved offline for each point eight times—one for each combination of the balancing error signals sign. For this, eight lookup tables are generated, one for each combination of signs of the three v_{d_p} for $p = 1, 2, 3$ (see Table 2).

4.2. Constraints

The constraints considered are:

- The sum of the duty cycles for each phase has to be 1 (equality constraints)
$$\sum_{j=1}^{5} d_{ij} = 1;\ i = a, b, c. \tag{17}$$
- The outputs of the power controller (u_α, u_β) transformed to abc (η_a, η_b, η_c) have to be attained (equality constraints). According to Eqs. (7)–(10):
$$-2d_{i1} - d_{i2} + d_{i4} + 2d_{i5} = \eta_i + x = u_i. \tag{18}$$
- Through (11)-(13), the balancing error signals v_{d1}, v_{d2}, v_{d3} are imposed to go to zero monotonically, i.e. making $|dv_{d_p}/dt| < 0$ (inequality constraint) for each error signal $p = \{1, 2, 3\}$. Since the sign of each v_{d_p} is unknown from the input data, the eight cases, corresponding to the eight combinations of signs, have to be considered.

4.3. Cost Function

The cost function to be minimized will include the number of duties d_{ij} that are different from zero in order to reduce the switching losses as much as possible. In this way, as the sum for each phase of d_{ij} must be equal to one, the optimization procedure will try to find a feasible solution with only one d_{ij} active in each phase. Were this infeasible, the next combination to consider would be that two d_{ij} are nonzero for one phase and so on. It is clear that the more nonzero d_{ij} appear in the solution, the more switches are necessary. Thus, the optimization algorithm will look for the feasible solution with the least number of commutations.

Consequently, the optimization problem must handle the variables d_{ij} and, at the same time, the number of nonzero d_{ij}. This can be expressed in terms of linear mixed-integer constraints as follows. A new set of integer variables $s_{ij} \geq 0$, $i = \{a, b, c\}$; $j = 1, \ldots, 5$ is defined in such a way that s_{ij} must be equal to one if $d_{ij} \neq 0$. This can be achieved imposing that variables s_{ij} are integer and with the constraints

$$s_{ij} - d_{ij} \geq 0\,; \quad s_{ij} \geq 0.$$

In this way, if $d_{ij} > 0$—note that $d_{ij} \in [0, 1]$—the inequality implies that $s_{ij} \geq 1$. Thus, a cost function (f_{cost_1}) that minimizes the number of nonzero d_{ij} is

$$f_{\text{cost}_1} = \sum_{i=a,b,c} \sum_{j=1}^{5} s_{ij}.$$

Additionally, a penalty for some transitions should be considered. These transitions are those that jump between two non-consecutive levels—i.e. $\exists k_1, k_2 \neq 0 \in \mathbb{N}$ s.t. $d_{i(j-k_1)} \neq 0$, $d_{ij} = 0$, $d_{i(j+k_2)} \neq 0$—(in the following, they

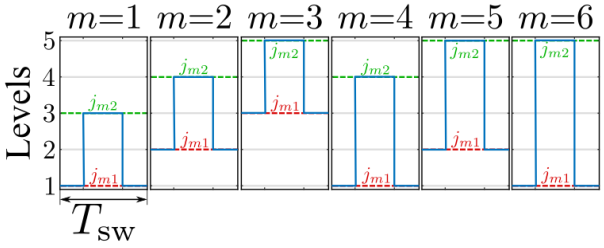

Figure 2
Large jumps index sample.

Table 3
Large jump notation

Index m	Levels involved (j_{m1}, j_{m2})	Index m	Levels involved (j_{m1}, j_{m2})
1	1, 3	4	1, 4
2	2, 4	5	2, 5
3	3, 5	6	1, 5

will be called “large jumps"), and it is desired to avoid them as they introduce larger output voltage transitions and more voltage stress on the switching devices. One possibility would be to include constraints such that those switches are forbidden, however this approach may lead to an unfeasible optimization problem. Thus, these large jumps are penalized for each phase in the cost function as follows. Firstly, the large jumps are classified using the index m: there are six possibilities (depicted in Fig. 2) whose notation and levels involved are shown in Table 3. Secondly, they have to be detected, and thirdly, penalized in the cost function. Using variables j_{m1} and j_{m2} for the outer levels in the considered jump, the detection stage for phase i must search for the occurrence of $d_{ij} \neq 0$ for $j = \{j_{m1}, j_{m2}\}$ and $d_{ij} = 0$ for $j_{m1} < j < j_{m2}$, which means that no level is active between the outer levels j_{m1} and j_{m2}. This can be accomplished by introducing two additional integer (in fact, binary) variables r_{im} and p_{im} (for $i = a, b, c$ and $m = 1, \ldots, 6$) and two additional constraints. Variables r_{im} are used to detect when the border levels (j_{m1}, j_{m2}) are both active, while variables p_{im} are used to detect if, additionally to $r_{im} = 1$, the intermediate levels are all inactive. In general terms, these two constraints are expressed as:

$$s_{ij_{m1}} + s_{ij_{m2}} - r_{im} \leq 1; \quad 0 \leq r_{im} \leq 1 \tag{19}$$

$$r_{im} - p_{im} - \sum_{j=j_{m1}+1}^{j_{m2}-1} s_{ij} \leq 0; \quad 0 \leq p_{im} \leq 1 \tag{20}$$

As an example, the following constraints correspond to jump $m = 4$ (which according to Table 3 corresponds to $j_{m1} = 1$ and $j_{m1} = 4$) for phase a:

$$\begin{aligned} s_{a1} + s_{a4} - r_{a4} &\leq 1 \\ -s_{a2} - s_{a3} + r_{a4} - p_{a4} &\leq 0, \end{aligned}$$

therefore, for phase a, if $r_{a4} = 1$ levels 1 and 4 are being used, whereas if $p_{a4} = 1$ only levels 1 and 4 are being used. In this way, the penalization for large jumps is included in the general cost function by penalising the existence of $p_{im} = 1$. Furthermore, an additional integer variable q_m is used to penalise larger jumps by making it equal to the number of additional switches this large jump implies, that is, q_m=1 for $m = \{1, 2, 3\}$; $q_m = 2$ for $m = \{4, 5\}$, and $q_m = 3$ for $m = 6$. Thus,

$$f_{\text{cost}} = f_{\text{cost}_1} + \sum_{i=a,b,c} \sum_{m=1}^{6} p_{im} q_m.$$

4.4. Optimization problem

The resulting problem has 67 unknowns: 15 variables d_{ij} and the 15 associated s_{ij}; 2×18 variables r_{im} and p_{im} associated with the large jumps and the degree of freedom x associated with the modulation. The number of equality constraints is 6 and there are 54 inequality constraints. Notice that all the constraints, as well as the cost function are linear. Therefore, the resulting optimization problem is linear and mixed-integer. There exist commercial software packages that solve this kind of problem in affordable time for off-line purposes, in any case, the software used in this paper is the MATLAB® Optimization Toolbox, function `intlinprog`. A simple flowchart is depicted in Fig. 3 to show how the results are obtained and stored in the lookup table for later use during online operation. There exist

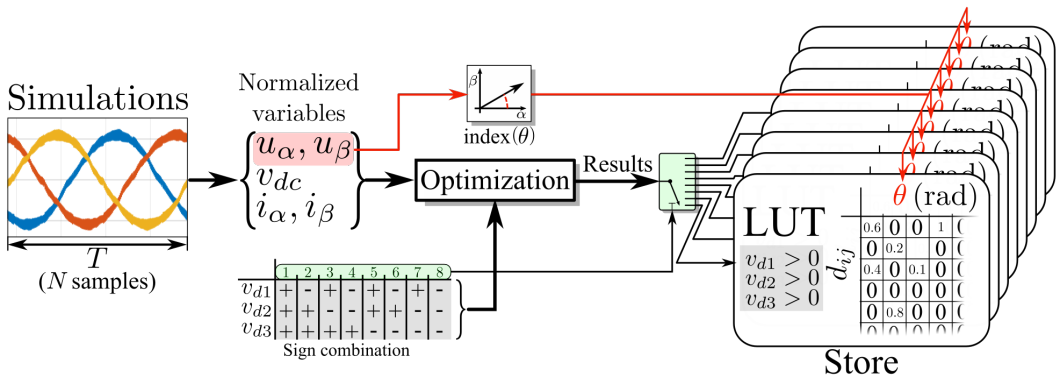

Figure 3: Flowchart of the optimization execution that store the results in the lookup table for later use in online operations.

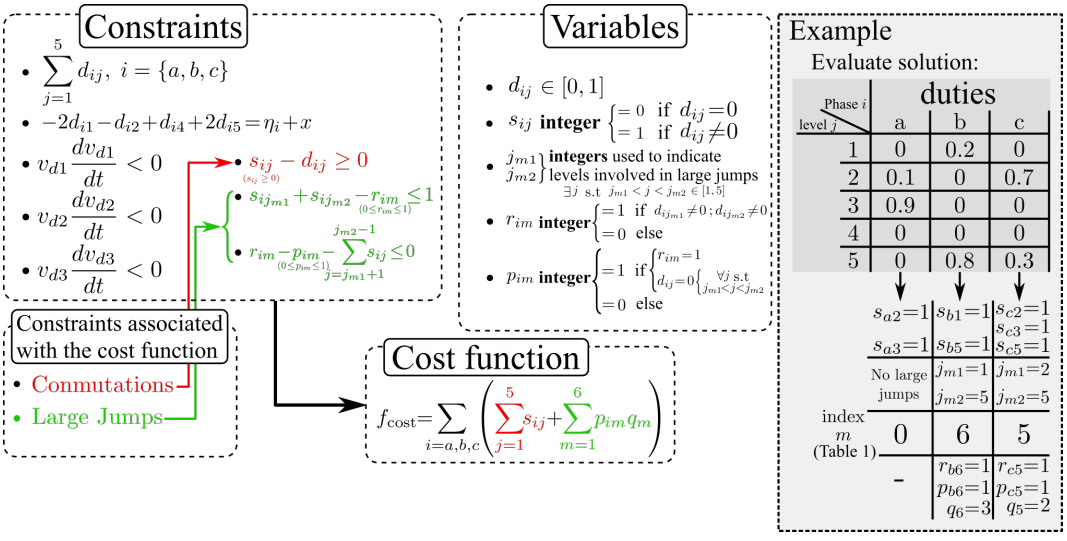

Figure 4: Summary of the optimization problem and example of codification for one point.

considerations that are not taken into account in the previous problem and they are left as future research. In particular, switching from one sampling interval to the following one, are not contemplated.

In summary, the optimization problem formulation and the involved variables are depicted in Fig. 4. Additionally, an example of the variables values associated with a particular case is given for the sake of clarity. In total, eight lookup tables are generated for the eight possible combinations of signs of v_{dp} (see Fig. 3). Each one of them will have N rows, which correspond to the optimization problem associated with N time instants over a grid period. Instead of indexing by the time along the sampling period, as the signals are sinusoidal and delayed 90º, the table can be indexed by the arguments of the sinusoids, $\theta = \arctan(u_\beta/u_\alpha)$. The stored values in each row are the corresponding d_{ij} obtained as the solution of the optimization problem. In fact, as it will be seen later, the only information that will be used is whether these duty cycles are equal to zero or not.

5. Control law implementation

Although there exist efficient algorithms for solving the previous optimization problem quite rapidly for off-line purposes, the problem would be too costly for online implementation in real applications. In this paper, the following method based on lookup tables is proposed. Considering that 8 different optimization problems can be formulated depending on the signs of v_{d_1}, v_{d_2}, v_{d_3}, 8 lookup tables have to be computed and stored. The problem is solved off-line assuming the nominal values of the converter in steady state over a grid period and a combination of signs

of v_{d_1}, v_{d_2}, v_{d_3}, then its solution is stored in a lookup table along with its data input, namely: normalized values of i_a, i_b, i_c and u_α, u_β. Therefore, each table contains the solution—values of d_{ij} and x—of the optimization problem based on the same inputs but for the signs of v_{d_1}, v_{d_2}, v_{d_3}. In the following, three aspects for the use of these lookup tables are explained: 1) row selection, 2) Lookup table interpolation and 3) steady-state improvement in order to reduce the number of commutations.

5.1. Row selection

As it was said above, there are 8 lookup tables, one assigned to each combination of the error signal signs. Thus, once the combination of sign(v_{d1}), sign(v_{d2}) and sign(v_{d3}) is known, the table can be selected accordingly. Then, it is necessary to locate the row corresponding to the stored information which is closer to the measured data. In order to do so, the angle of the vector composed by variables (u_α, u_β) is used as the index variable, hence the row with the closest angle value to this one will be chosen. Consequently, the row selection will depend only on the output of the current (or power) controller $u_{\alpha\beta}$.

5.2. Lookup table interpolation

Usually, the selected row will not correspond exactly to the measured data and, therefore, an interpolation algorithm must be used. A usual linear interpolation procedure could be applied but in this way some hard constraints could be violated. Consequently, a different interpolation approach must be considered. For this, the interpolation objectives are ordered in descending priority as follows:

1. The sums $\sum_{j=1}^{5} d_{ij}$ must be equal to 1 for $i = a, b, c$.
2. Variables d_{ij} must lay between 0 and 1.
3. Values u_α, u_β must be accomplished according to (7).
4. The voltage balance must be fulfilled.

In order to take into account these requirements and to avoid any interpolation issue the following procedure is used. The only information that will be used from the selected row of the lookup table is the duty ratios d_{ij} that are different from zero, namely, the levels j of those nonzero duties for each phase i. It has been observed that, as a result of the optimization, at every sampling instant there is a phase—referred as i_0—that is fixed at one level without switching while, in most of the cases, the other two—referred as i_1 and i_2—commute between two levels not necessarily consecutive. Therefore, the value of x can be determined using (18) by imposing that this characteristic is present in the result, i.e. detect the phase i_0 and level j whose $d_{i_0 j} = 1$ in the LUT, and then obtain the value of x in (18) that makes so for this phase considering the value of η_{i_0}. Once x is known, the values of u_i can be computed for the other two phases using (8)–(10). The fulfillment of u_{i_1} and u_{i_2} is made by applying (18) considering only the nonzero duty ratios obtained from the LUT. Generally, there is only two nonzero duties in the LUT for phase i_1 and i_2, thus the resultant duty cycles are unequivocal considering the objectives 1,2 and 3 listed. In the case there are more than two nonzero d_{ij}, one or more values of duty cycles are chosen from the lookup table. Finally, it may occur that the previous procedure yields some duty cycles outside the interval $[0, 1]$, which is infeasible because of the second objective considered. In such cases, the voltage-balance objective is not considered as it is the last priority listed above, and the corresponding u_i is achieved by distributing it between the two nearest levels—the closest integers to u_i. A simplified scheme of the proposed control and modulation approach is depicted in Fig. 5.

5.3. Steady state improvement

Despite the fact that this approach solves the unbalance issue as it will be shown in the simulation and experimental results, it may present an increased harmonic distortion in the grid current in steady state. This increment is due to the sudden change of balancing criterion from one sampling instant to the next one when the values of v_{d_p} are close to 0. A change of the sign of v_{d_p} would imply changing the lookup table among the eight entries, probably yielding to an abrupt change in the value of x and the levels used. This phenomenon is, by itself, acceptable. However when it occurs several times consecutively, it distorts the grid current as the common voltage component is increased along with the number of commutations. Another aspect to take into account is that it is not necessary that the balancing error signals tend to zero but to remain small enough. Thus, a modification in the algorithm described above—referred as base algorithm from now on—is proposed. The modification—referred as enhanced algorithm—tries to avoid, in steady state, frequent changes of balancing criterion and abrupt changes in x.

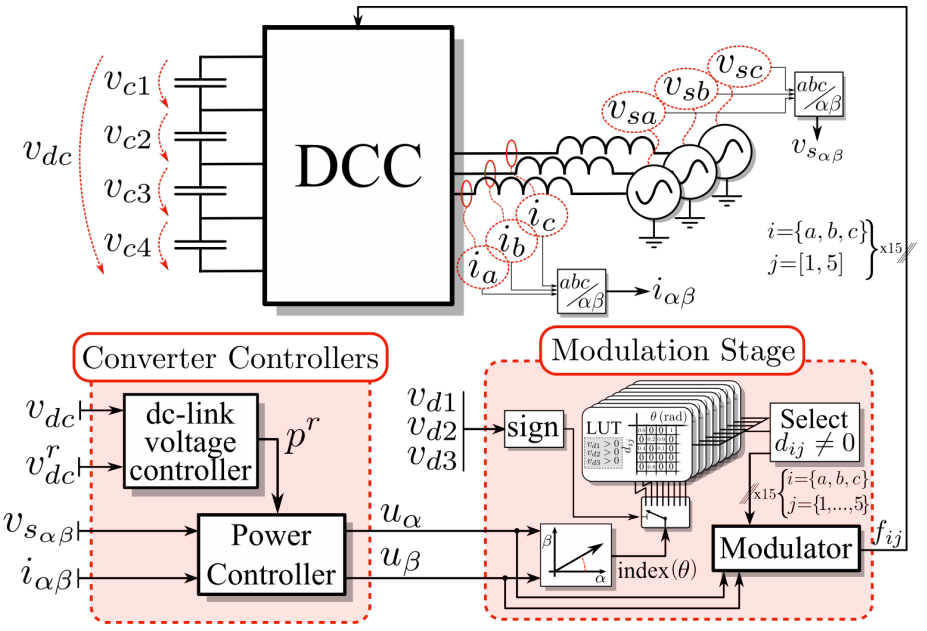

Figure 5: Implementation and control scheme of the proposed approach.

In the enhanced algorithm, the change of balancing criteria —change from one of the eight lookup tables to another— is limited to occur only when one of the error signals v_{dp} is large enough. Therefore, when the absolute value of the three v_{dp} is smaller than a threshold ν, the active lookup table is not changed. Only when one of them is larger than ν the lookup table is changed using the "normal" procedure exposed above. The larger the value of ν is, the lesser the times the change of criteria would occur, but larger values of v_{dp} would be allowed. As a result, the values of v_{dp} will be enclosed inside a band of width 2ν around 0 at the same time that the grid current will present a better harmonic distortion. In the next sections, both, the base algorithm and the one that includes the steady-state improvement, will be compared in simulations and experiments.

6. Simulation results

Before testing the system in a real environment, some simulations have been carried out in MATLAB-Simulink®. Table 4 shows the circuit and controller parameters that will be used both in simulations and experiments. The lookup tables were obtained under this nominal case fixing R and v_{dc} to 60 Ω and 700 V respectively. The time needed to solve 800 of such problems ($N = 100$ problems in an ac period times 8 combinations of signs of v_{d_p}) is around 20 secs.

In order to depict a comparison, two approaches from the literature are considered [7, 12] in addition to two published ones that have been tested in the same equipment [10]. Paper [7] uses the well-known space-vector modulation and will be referred as space-vector based algorithm (SVBA), paper [12] uses the finite-control-set model-predictive-control (FCS-MPC) to control a grid-connected NPC inverter, whereas [10] presents an approach and a modification of it where both use voltage-level-based PWM with the voltage balance control integrated in the control stage, and therefore they will be referred as original integrated control and modulation (OICM) and modified integrated control and modulation (MICM). Notice that despite the FCS-MPC presented in [12] is designed for three-level converters, the cost function is modified in this paper to be valid for five-level converters, similarly to [30]. Due to the nature of FCS-MPC, three different sampling rates (f_s) are considered in these simulations: 10, 25 and 50 kHz.

The phase currents obtained from simulation for these approaches are depicted in Fig. 6, and the switching states in Fig. 7, both with $v_{dc}^r = 800\,V$ and $R = 60\,\Omega$. Notice that the lookup tables were designed for $v_{dc}^r = 700\,V$. Thus, these results will show that this approach is valid not only for the operating point considered in the design. The resulting current THD values and number of commutations—the change from one level to a different one—in a grid period are shown in Table 5, where its variation in % with regard to the base algorithm presented in this paper are

Table 4
Converter Parameters

Parameter	Value	Parameter	Value
Grid frequency f	50 Hz	Sampling and switching frequency f_s, f_{sw}	10 kHz
Grid voltage v_{sabc}	230 V_{RMS}	Power factor	1
Filter Inductance L	2 mH	k_p (DPC)	$2e^{-7}$
dc-link capacitance C	3300 μF	k_i (DPC)	$2e^{-5}$
dc-link load R	120 $\rightarrow$ 60 Ω	k_p^{dc}	0.05
dc-link voltage reference v_{dc}^r	700 $\rightarrow$ 800 V	k_i^{dc}	1
Enhanced band ν	10 V	Points for LUT generation N	100

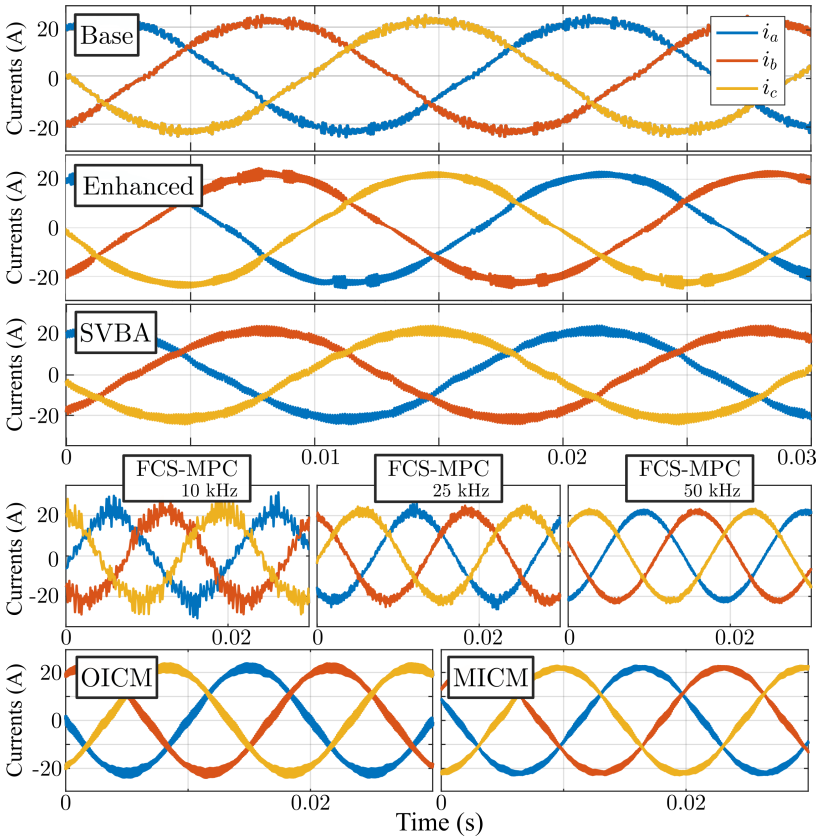

Figure 6: Three-phase currents in steady state when $R = 60\,\Omega$ and $v_{dc}^r = 800\,V$ for the base algorithm (top), the enhanced one (2nd), the SVBA (3rd), the FCS-MPC [12] (4th) considering three sampling rates (10, 25 and 50 kHz), and the OICM and MICM [10] (bottom). The THD values of these currents are shown in Table 5.

also highlighted. Notice how the proposed base and enhanced algorithms exhibit lower current distortion and lower number of commutations than SVBA and OICM. On the contrary, MICM achieves slightly better current distortion than the base algorithm at the cost of a large number of commutations. Regarding FCS-MPC, as the switches can only occur at the sampling instants unlike PWM approaches, three simulations are presented for different sampling frequencies: 10, 25 and 50 kHz. Note that higher frequencies usually result in less current distortion but larger number of commutations. Additionally, higher frequencies are more demanding in terms of computational burden. It can be seen that FCS-MPC with the same f_s than the base algorithm yields unacceptable current distortion (13.42 %). In order to achieve a more feasible current distortion, the sampling rate has to be increased from 10 kHz to 25 kHz, for which the currents reach a distortion of 5.1 % that is closer to the value of the base algorithm (4.63 %). At the same time, the number of commutations is increased proportionally to the sampling rate—again, this is true as long

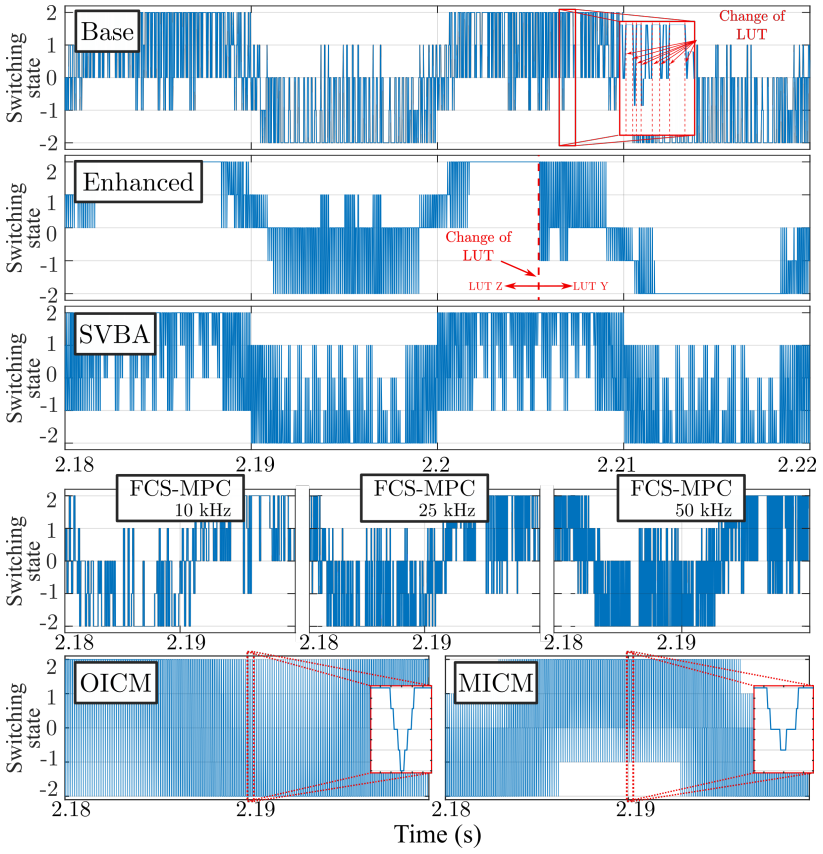

Figure 7: Switching state of phase a of the converter output with $v_{dc}^r = 800\,V$ and $R = 60\,\Omega$, for the base algorithm (1st), the enhanced one (2nd), the SVBA [7] (3rd), the FCS-MPC [12] (4th) considering three sampling rates (10, 25 and 50 kHz), and the OICM and MICM [10] (bottom). The number of commutations for each approach is shown in Table 5.

as the weights in the cost function are not changed—, reaching for 25kHz a similar number of commutations than the enhanced algorithm (540 vs 550). Larger sampling rates (50 kHz) further reduce the current distortion (2.54 %) and increase the commutations (1100). In summary, in terms of current distortion and number of commutations, the base and enhanced algorithms exhibit a better behaviour than SVBA [7] and OICM [10] with $f_s = 10$ kHz, while FCS-MPC [12] has to appeal smaller sampling rates to achieve similar performance. It is worth to mention that FCS-MPC uses a cost function whose weights can be modified as a trade-off between current distortion, capacitor voltage balance and number of commutations. These simulations were carried out using the weights that achieve the capacitor voltage differences to be less than ν in steady state. Alternatively, MICM improves the current distortion when compared with the base algorithm (4.2 % vs 4.63 %) at the cost of yielding twice the number of commutations. Nonetheless, the proposed enhanced algorithm further improves the base algorithm performance achieving lower distortion and commutations than MICM.

As it has been commented, the improvement in the current distortion and number of commutations for the enhanced algorithm is due to the relaxation in steady state, of the capacitor voltage balance criterion as they are not forced to go to zero but to keep around a band of value ν. In this way, the change of balancing criterion—the selected lookup table (LUT) among the available 8— is done much less frequently as it can be seen in Fig. 7.

Regarding voltage balancing capabilities, a simulation starting from an unbalanced situation is depicted in Fig. 8 ($v_{d1} = -40$, $v_{d2} = 60$, $v_{d3} = -5$). At $t = 1\,s$, the balancing strategy for each approach is enabled showing the behaviour of the capacitor voltages. Firstly, the FCS-MPC algorithm shows the fastest balancing but, because of the large values of $\{v_{d1}, v_{d2}, v_{d3}\}$, the current tracking is not prioritized in the cost function until these values are low enough. Therefore, there exists a transient where the current tracking is affected. Besides, the larger the sampling frequency, the faster the balancing. On the contrary, the SVBA algorithm shows a slower balancing (around 500 ms

Table 5
THD value and number of commutations (variation in % respect to base algorithm)

Algorithm	THD		Number of commutations	
Base	4.63		645	
Enhanced	4.05	(-12%)	550	(-15 %)
SVBA [7]	7.01	(+51%)	935	(+45 %)
FCS-MPC [12] (10 kHz)	13.42	(+190%)	210	(-68 %)
FCS-MPC [12] (25 kHz)	5.10	(+10%)	540	(-16 %)
FCS-MPC [12] (50 kHz)	2.54	(-45%)	1100	(+70 %)
OICM[10]	5.40	(+16 %)	1600	(+148%)
MICM[10]	4.20	(-9 %)	1333	(+106%)

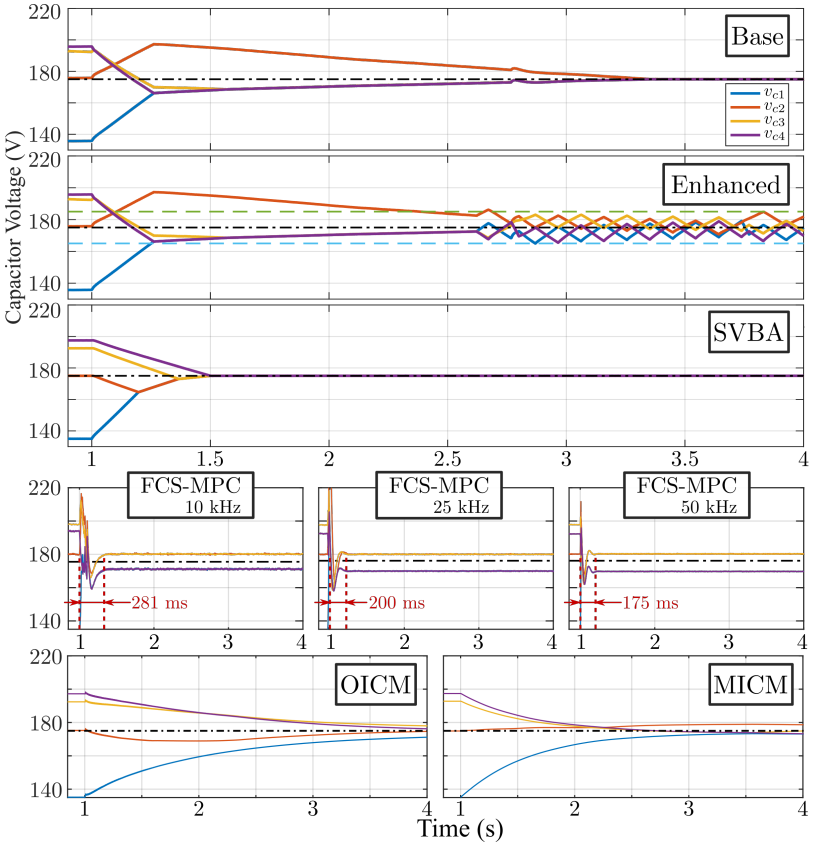

Figure 8: Capacitor voltages starting from an unbalanced condition ($v_{d1} = -40$, $v_{d2} = 60$ and $v_{d3} = -5$) for the base algorithm (1st), the enhanced one (2nd), the SVBA [7] (3rd), the FCS-MPC [12] (4th) under three different sampling ratios, and the OICM and MICM [10] (bottom). The voltage balancing algorithms are switched on at $t = 1$. Band and equalized value depicted with dashed and semi-dotted lines respectively. $v_{dc}^{r} = 700\,V$ and $R = 120\Omega$.

to reach steady state) but reaching zero steady-state error. OICM and MICM approaches, however, have a capacitor voltage balancing control parameter that determines the speed of the balancing. A higher value would yield a faster balancing and lower steady-state error at the cost of a worse power tracking transient. Nevertheless, these simulations used the same parameter value than the one used in the experiments in [10] yielding the slowest balancing speed and non-zero steady-state error in the simulations carried out. With regard to the proposed algorithms, the base and enhanced approaches present a voltage balancing that takes around 3 seconds to reach steady state (faster than OICM or

Figure 9: Five-level DCC used for the experiments.

MICM, but slower than SVBA or FCS-MPC). Comparing the base and the enhanced approaches, they result in similar balancing capabilities—indeed, its behaviour is the same whenever any capacitor voltage error signal is outside the band ν. The difference between them, however, lies in their behaviour in steady state. Because of the relaxation of the balancing objective, the enhanced algorithm avoids unnecessary changes in the evolution of the capacitor voltages (by avoiding selecting another lookup table) provided that the voltage balance signal errors are inside the band—depicted in dashed lines in Fig. 8—, while the base one tries to keep them as close to zero as possible.

In summary, regarding capacitor voltage balance, the proposed approaches are slower than FCS-MPC and SVBA but faster than OICM and MICM. Besides, the base algorithm reaches zero-steady state error similar to SVBA. On the contrary, the enhanced algorithm keeps the errors moving inside a band (whose amplitude is a design parameter), while FCS-MPC, OICM and MICM yield some fixed error in steady state. Nevertheless, the voltage balance is a secondary problem, while low current distortion and low losses (proportional to the number of commutations) are more important. In numerous applications this slowness is a reasonable price to pay in order to obtain the good results shown in Table 5.

7. Experimental results

This section is devoted to confirm the validity of the proposed approaches. For this, experimental results are obtained using the equipment shown in Fig. 9 with the same parameters than the previous section (Table 4). In order to test the behaviour of the system under different conditions, for which the lookup tables were not designed, an abrupt change in the load from 120 to $60\,\Omega$ at $t = 0.7$ s, a smooth change in v_{dc}^r from $700\,V$ to $800\,V$ starting at $t = 2.6$, and the load returning to $120\,\Omega$ from $60\,\Omega$ at $t = 4.6$ s are considered. The smooth change in v_{dc}^r consists of a linear ramp with a duration of $0.7\,s$.

Figure 10 depicts the behaviour of the phase currents in the experiment in steady-state ($v_{dc} = 800\,V$ and $R = 60\,\Omega$) for the base and the enhanced algorithm. Accordingly, the harmonic spectrum and the THD value of these currents is also depicted in Fig. 11, validating the improvement for the enhanced algorithm in terms of distortion in steady state.

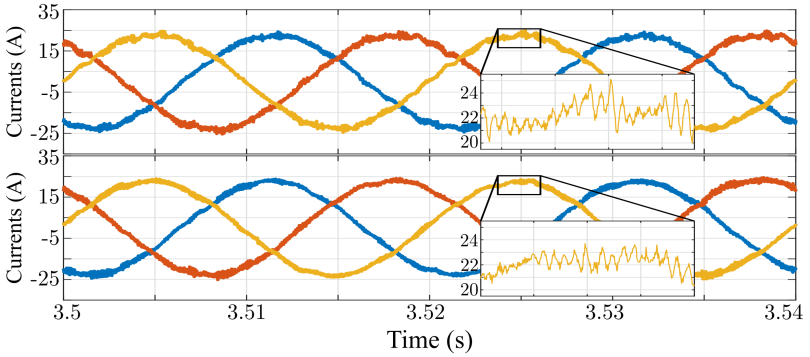

Figure 10: Experimental result: Three-phase currents in steady state for the base (top) and the enhanced (bottom) algorithms.

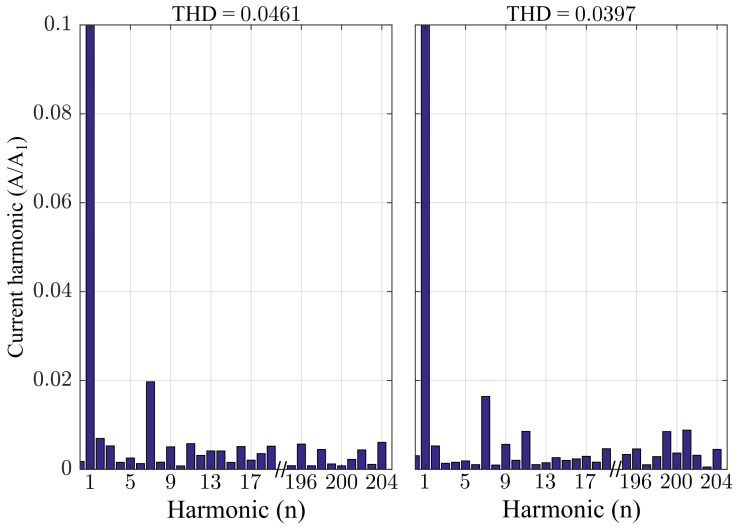

Figure 11: Experimental result: Harmonic spectrum of phase currents (Fig. 10) for the base (left) and the enhanced (right) algorithms.

Figure 12 shows the evolution of the active power over time with the changes considered. Notice the reduction in the ripple with the enhanced algorithm. Evolution of the dc-link capacitor voltages $(v_{c1}, v_{c2}, v_{c3}, v_{c4})$ and their reference signal $v_c^r = v_{dc}^r/4$ are depicted in Fig. 13. Finally, the capacitor voltages starting from an unbalanced situation (same than the one considered in simulations) are shown in Fig. 14 for the base and the enhanced algorithm, where the band in which the signals move in steady state can be seen. Despite the fact they do not tend to zero for the enhanced algorithm, the resultant values are perfectly assumable as they are quite small compared to the magnitude of the capacitor voltages. All these figures corroborate the simulation results and the good performance of the proposed method. Regarding the current distortion, the proposed approaches fulfill the Standard IEEE 519-2014 [4] as their THD value is below 5%. Therefore, these approaches can be used for real, grid-connected applications. Besides, the appearance of low-order harmonics (namely, 5th, 7th and 11th) can be explained by the presence of dead-times between commutations [31], and therefore it can be compensated using active harmonic elimination algorithms.

8. Conclusions

This paper has presented a new procedure for balancing the capacitor voltages in five-level DCC converters. The modulation stage is formulated as a linear, mixed-integer optimization problem with constraints. In this way, the balancing problem is solved at the same time that the number of commutations is minimized exploiting the degrees of

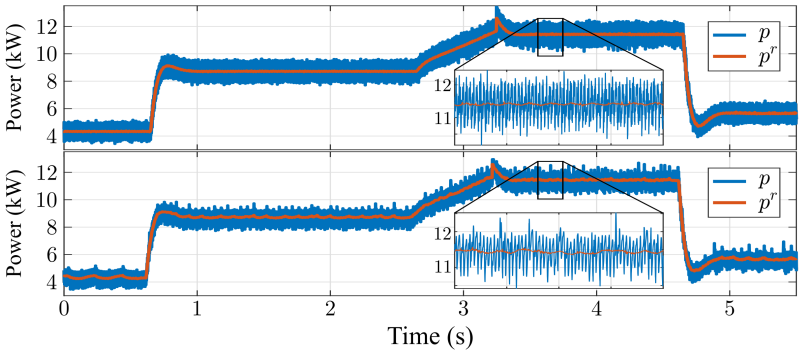

Figure 12: Experimental result: Power behaviour during the experiment for the base (top) and the enhanced (bottom) algorithms.

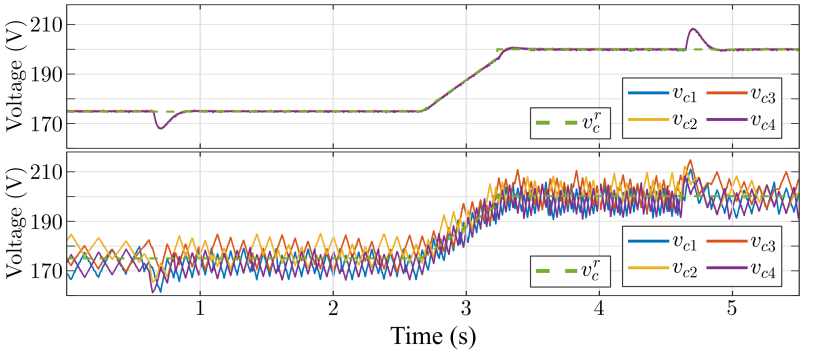

Figure 13: Experimental result: Evolution of the capacitor voltages in addition to their reference $v_c^r = v_{dc}^r/4$ during the experiment for the base (top) and the enhanced (bottom) algorithms.

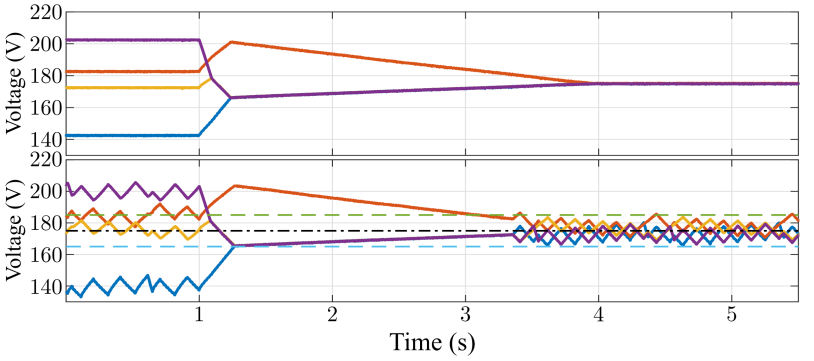

Figure 14: Experimental result: Evolution of the capacitor voltages starting from an unbalanced condition for the base (top) and the enhanced (bottom) algorithms. Band and equalized value depicted with dashed and semi-dotted lines respectively. $v_{dc}^r = 700\,V$ and $R = 60\,\Omega$

freedom remaining after the voltage and power control. The optimization problem is costly to be solved online and, thus, several lookup tables are used. Additionally, a procedure for adequately use the lookup tables is given including a relaxation of the algorithm in steady state in order to improve the harmonic distortion. The resulting approach is tested in both simulations and experiments showing the good behaviour of the proposed method under some changes in the load and the desired dc-link voltage, showing some flexibility in the operation point and robustness to load variations. Nonetheless, it is left as a future line of research the extension of this approach to those cases where larger variations

of the operating conditions are present.

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