ACS APPLIED ELECTRONIC MATERIALS

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Article

Controlling Volatility and Nonvolatility of Memristive Devices by Sn Alloying

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Cite This: ACS Appl. Electron. Mater. 2023, 5, 6842−6849

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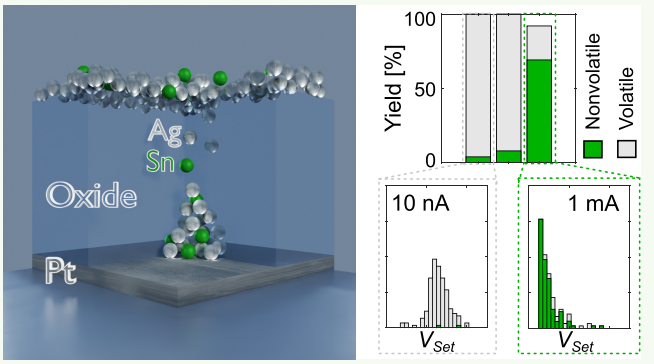
ABSTRACT: Memristive devices have attracted significant attention due to their downscaling potential, low power operation, and fast switching performance. Their inherent properties make them suitable for emerging applications such as neuromorphic computing, in-memory computing, and reservoir computing. However, the different applications demand either volatile or nonvolatile operation. In this study, we demonstrate how compliance current and specific material choices can be used to control the volatility and nonvolatility of memristive devices. Especially, by mixing different materials in the active electrode, we gain additional design parameters that allow us to tune the devices for different applications. We found that alloying Ag with Sn stabilizes the nonvolatile retention regime in a reproducible manner. Additionally, our alloying approach improves the reliability, endurance, and uniformity of the devices. We attribute these advances to stabilization of the filament inside the switching medium by the inclusion of Sn in the filament structure. These advantageous properties of alloying were found by investigating a choice of six electrode materials (Ag, Cu, AgCu-1, AgCu-2, AgSn-1, AgSn-2) and three switching layers (SiO_2, Al_2O_3, HfO_2).



KEYWORDS: *memristor, memristive switching, resistive switching, alloy, volatility, electrochemical metallization cells*

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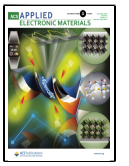
INTRODUCTION

In need of more computational power, the scientific community is searching for new beyond classical von Neumann computing architectures. Neuromorphic computing, in-memory computing, reservoir computing, and spiking neural networks are promising solutions addressing this challenge.[1] In these architectures, specialized devices are necessary that can mimic the adaptability of their biological counterpart. Memristive devices are an attractive option as they offer intrinsic device dynamics similar to those of a synapse or neuron.[2−4] Important fundamental building blocks toward the implementation of these architectures are volatile and nonvolatile memristive devices.

Memristive devices have already been applied in neuromorphic computing,[2,3,5−9] in-memory computing,[10,11] and reservoir computing.[12,13] They offer high scaling potential,[14,15] fast switching times,[16] high endurance,[17] and good retention.[18] However, they generally suffer from high variability between devices due to the stochastic nature of the switching process.[19,20] To address this and to enable the ability to tailor device functionalities, proposed solutions aim at either controlling the operation parameters or engineering the material composition of the memristive device. In this context, electrode alloying has been introduced to further tailor the design parameters and functionalities. For instance, alloying has been shown to improve weight control for neuromorphic computing[21] and improve uniformity.[22] Alternatively, the oxide thickness can be used to control volatility and nonvolatility.[23] Doping the switching layer is also a possible approach to achieve different device functionalities such as those of a memory or a selector.[24] Additionally, transitioning between threshold and nonvolatile switching by controlling compliance current has been demonstrated.[25,26] Compliance current can also be used to control bipolar or unipolar switching.[25,27] Voltage control has also been shown to be able to change volatility and nonvolatility of memristive devices.[28]

However, the state-of-the-art mentioned above is based on technologies optimized for operation in one of the regimes. A

Received: September 13, 2023
Revised: November 9, 2023
Accepted: November 9, 2023
Published: December 4, 2023



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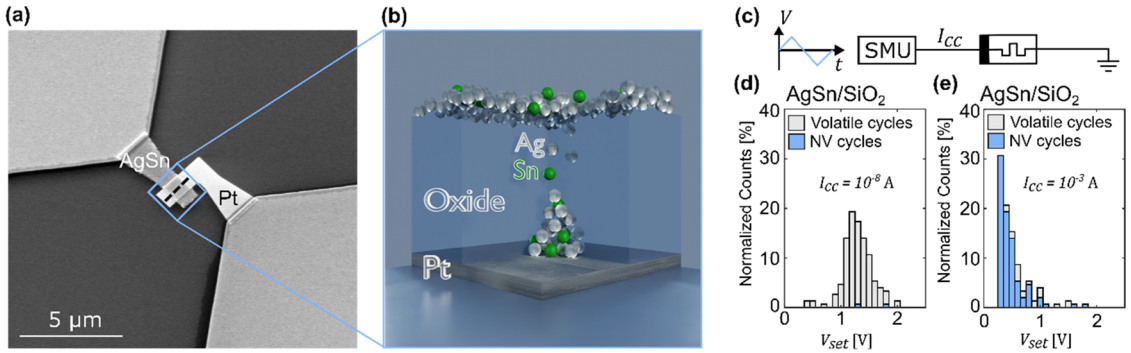

Figure 1. (Non)volatile conductive bridging random access memory (CBRAM) achieving high reproducibility by filament alloying. (a) Device structure illustrated by an SEM image of the memristive device with a passive Pt electrode (bottom) and an active AgSn metal electrode (top). The scale bar is 5 μm. (b) Artistic visualization of the filamentary switching mechanism. Silver (Ag) and tin (Sn) alloyed in the active metal electrode form a stable conductive filament. (c) Electrical measurement setup. A triangular voltage signal is applied with a source measurement unit (SMU) to switch the memristive device between its resistance states limited by a compliance current (I_{cc}). (d, e) V_{set} distribution of five devices over 30 cycles each with volatile cycles shaded in gray and the nonvolatile (NV) ratio in light blue. (d) For a low I_{cc} = 10^{-8} A, one finds mostly volatile switching. (e) For a high I_{cc} = 10^{-3} A, one finds mostly nonvolatile switching.

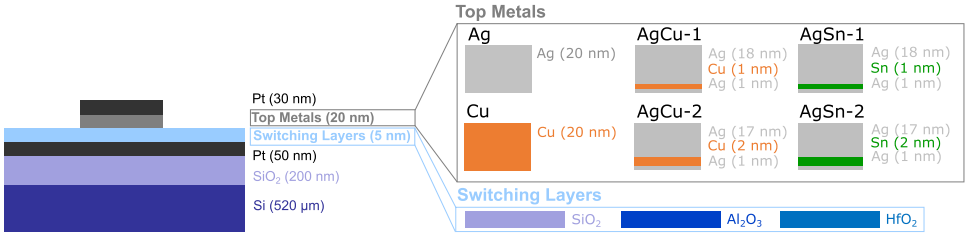

Figure 2. Vertical cross section along the dashed line in Figure 1a of the tested devices. The CBRAM is fabricated on top of silicon dioxide (SiO_2) on a Si substrate. The bottom electrode consisted of 50 nm platinum (Pt) covered by 5 nm of switching layer. SiO_2, Al_2O_3, and HfO_2 are investigated as candidates for the switching layer. As active top metals, two pure metals (Ag, Cu) and four alternate metal layers combining either Ag with 1 and 2 nm of Cu (AgCu-1, AgCu-2) or Ag with 1 and 2 nm of Sn (AgSn-1, AgSn-2), are used, respectively.

dedicated technology for controllable and reliable operation in both retention regimes is missing. Finding material compositions and operation parameters for new or combined applications is difficult due to the complex chemical and electrical interactions of the mobile species and the switching medium.[20,29] Hence, a large uncertainty about choosing the best technology remains. A study, which allows for flexible and reliable tailoring of volatility and nonvolatility, could fill this gap.

In this work, we demonstrate how to tailor the volatility and nonvolatility of a memristor specifically a conductive bridging random access memory (CBRAM). We exploit both material engineering and operation parameters by investigating various metal alloys for active electrodes and oxides for the switching layer while varying the compliance current. Compliance current investigations of a standard Ag/SiO_2/Pt CBRAM show a clear trend to nonvolatility with higher currents (1 mA) at the price of increased device breakdowns. This challenge is solved by engineering the active metal electrode materials (Ag, Cu, and Sn and their alloys) in combination with different switching layers (SiO_2, HfO_2, Al_2O_3). Our results show that mixing Ag with Sn significantly stabilized the filament for nonvolatile operation. We demonstrate a high yield >90% in the nonvolatile switching regime (1 mA). In the nonvolatile regime, we find a low median set voltage of 0.4 V with a standard deviation of 0.27 V and a reset voltage of −0.43 V with a standard deviation of 0.24 V. Likewise, volatile switching is observed for much lower currents (10 nA) with set voltages in the order of 1.3 V, standard deviation of 0.26 V and a 100% yield. We attribute these improvements to the inclusion of Sn in the filament formation based on scanning transmission electron microscopy energy-dispersive X-ray spectroscopy (STEM-EDX) analyses of pristine and cycled devices. Our findings show that incorporating small fractions of a second metal in the electrode composition in combination with precise electrical operation can be an effective strategy to fabricate tailorable and stable filamentary CBRAM. This approach is extendable to other material systems and may serve as a guideline for further optimizing the device performance.

EXPERIMENTAL SECTION

Concept. To find a flexible volatile and nonvolatile CBRAM, we fabricate different Ag- and Cu-CBRAMs and then assess their electrical characteristics and reliability. In a further step, the most promising combinations are examined in more detail.

In this investigation, single crossbars are selected as test structures to evaluate layered electrodes in combination with different oxides; see Figure 1. These structures were fabricated in-house using a three-step lithography process. The scanning electron microscope (SEM) picture in Figure 1a illustrates the crossbar consisting of two electrodes, an active top metal one (AgSn) and a passive bottom one (Pt). These two electrodes encapsulate the switching layer (oxide), forming the CBRAM. Figure 1b illustrates the filamentary switching behavior, which has been shown for Ag-based CBRAM[4,30,31] and is explored here for alloyed filaments. The material stacks are evaluated electrically by using voltammetry $I(V)$-sweeps. The measurement setup is shown in Figure 1c. The source measurement unit (SMU) applies a triangular voltage signal and limits the current to protect the device from damage. The alloying

https://doi.org/10.1021/acsaelm.3c01275
ACS Appl. Electron. Mater. 2023, 5, 6842−6849

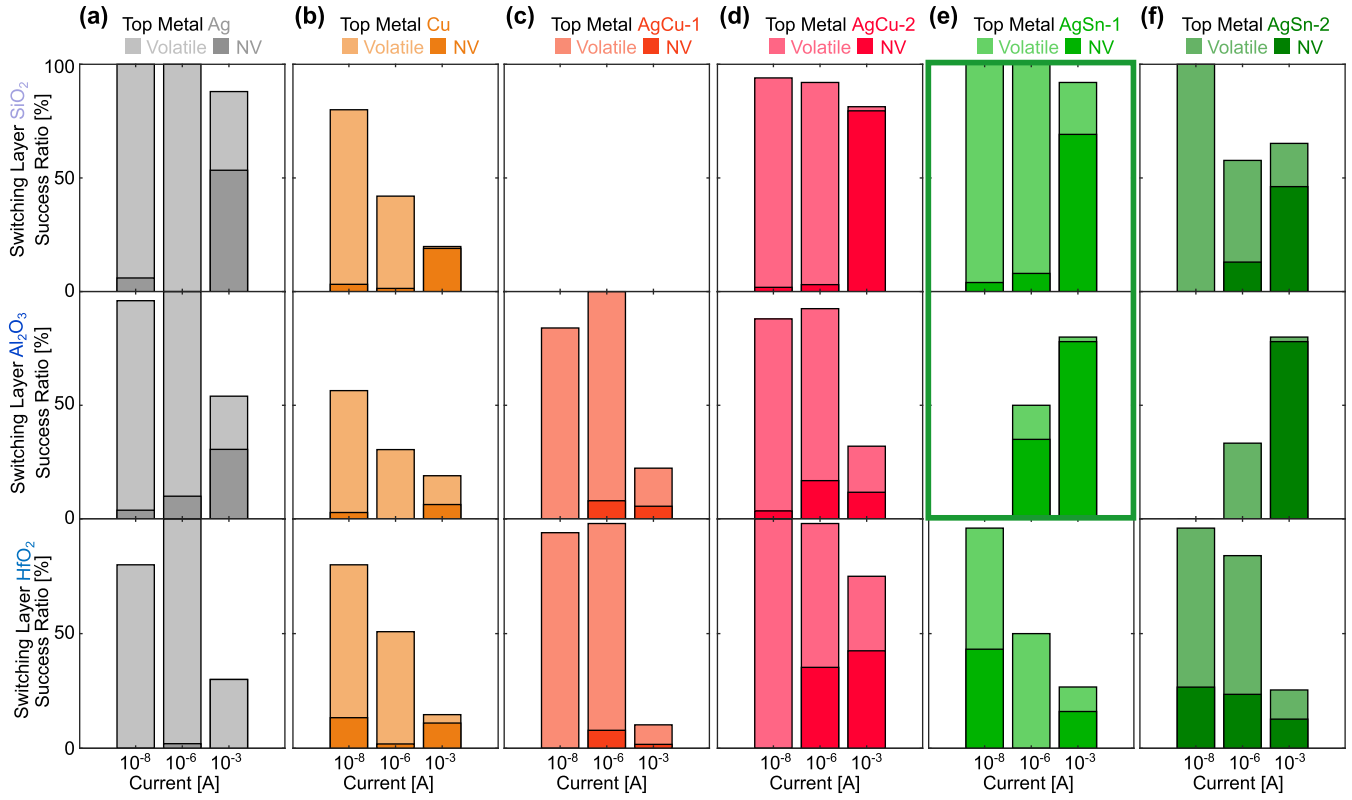

Figure 3. Comparison of success for volatile and nonvolatile switching as a function of the top metal, the switching layer, and the compliance currents. Five devices were measured per material stack. The (lighter) darker colorized part of the bar indicates the ratio of (volatile) nonvolatile cycles, respectively. Of interest are top metals in matrix layers with a high volatile and nonvolatile success ratio. It can be seen that increasing the current also increases the likelihood for nonvolatile operation. Most promising results are found for the material compositions encircled in green. In more detail, the figure shows the top electrode and switching matrix combinations. (a) Ag/(SiO_2, Al_2O_3, HfO_2). (b) Cu/(SiO_2, Al_2O_3, HfO_2). (c) AgCu-1/(Al_2O_3, HfO_2). AgCu-1/SiO_2 could not be measured due to fabrication issues. (d) AgCu-2/(SiO_2, Al_2O_3, HfO_2). (e) AgSn-1/(SiO_2, Al_2O_3, HfO_2). AgSn-1/SiO_2 and AgSn-1/Al_2O_3 (marked by the green box) have the best performance in the high current nonvolatile regime. (f) AgSn-2/(SiO_2, Al_2O_3, HfO_2). AgSn-1/Al_2O_3 and AgSn-2/Al_2O_3 start in the on-state and need high currents to reset.

approach enables the tuning of the devices for volatile or nonvolatile operation using compliance current (Figure 1d,e).

Device Fabrication. The material stacks selected for investigation are depicted in Figure 2. All devices have in common a thermally oxidized Si substrate (200 nm SiO_2) and a 50 nm Pt bottom electrode. These Pt bottom electrodes are deposited by standard electron beam evaporation at a pressure of 1×10^{-6} mbar. They consist of 3 nm Ti adhesion layer with 47 nm Pt on top. This electrode is then polished under a low incident angle with argon milling to remove imperfections from the lift-off. Three different CMOS-compatible amorphous oxides (SiO_2, HfO_2, and Al_2O_3) are chosen for the switching medium on top of the bottom electrode. The switching layer with a thickness of 5 nm is deposited as follows: SiO_2 with plasma-enhanced atomic layer deposition, HfO_2 and Al_2O_3 with thermal atomic layer deposition. The top electrode consists of either pure metals or mixed layered metals. In the case of pure Ag and Cu, the electrode is deposited with electron beam evaporation, which is followed by a 30 nm thick capping layer of Pt to reduce oxidation. The mixed metal electrode is sputtered by introducing nominal layers of 1 or 2 nm of the alloying material (Cu and Sn) in-between the primary metal. A 30 nm thick Pt capping layer is also used to cover these alloys to reduce oxidation. Finally, contact pads for electrical probing consisting of Au are deposited with electron beam evaporation. To access the bottom Pt electrode for electrical probing, reactive ion etching was used for SiO_2 and HfO_2 and wet etching for Al_2O_3. The two electrodes form crossbars with an overlap area of 1 μm^2. Cross-sectional images showing the layer heights of the AgSn-1/SiO_2 devices can be found in Figure S1.

Electrical Measurement and Data Analysis. For the $I(V)$ measurement, a voltage is applied over the device with a source measurement unit (SMU) (Keysight B2912a). The SMU also limits the current to the different levels to protect the devices from destruction. The devices are connected with a 50 μm pitch probe.

The initial forming of the devices is done with a triangular voltage sweep from 0 to 5 V to −0.5 V back to 0 V. During this forming step, the current is limited to 10 nA and the step size is 0.1 V with an integration time of 20 ms. The measurement data in this paper are acquired after this initial forming step. Triangular voltage signals with a smaller amplitude (−0.5 to 3 V) are then applied for the next 20−40 cycles with the same step and integration time as used during the forming. The measurement is paused for 1 s between the end of each cycle and the start of the next. During this pause, no voltages are applied to the device. The $I(V)$ measurement cycles were then repeated with increasing compliance currents (100 nA, 1 μA, 10 μA, 100 μA, and 1 mA).

Once a significant reset is necessary, the negative voltage amplitude was increased and the sweep direction was reversed (0 to −2 to 2 to 0 V). Therefore, the sweep cycle ended with the device in the on-state. This made it possible to analyze the volatility of the devices in the 1 s pause between each cycle. If the on-state resistance significantly increases (>10×) after the pause, the cycle was labeled as volatile. If the device kept a similar on-resistance state (<10×), the cycle was labeled nonvolatile. Retention measurements were performed with nonvolatile cycles, and they showed no visible degradation of the on-state resistance in 24 h (Figure S2a). Additionally, the step size for reversed sweeps was decreased to 0.05 V for a higher resolution.

For the data analysis, we extract the set point of the device upon reaching 90% of the compliance current. At the same point, the on-state resistance (R_{on}) is taken. The reset point in case of nonvolatile switching is defined as the device resistance reaching 10-times the on-

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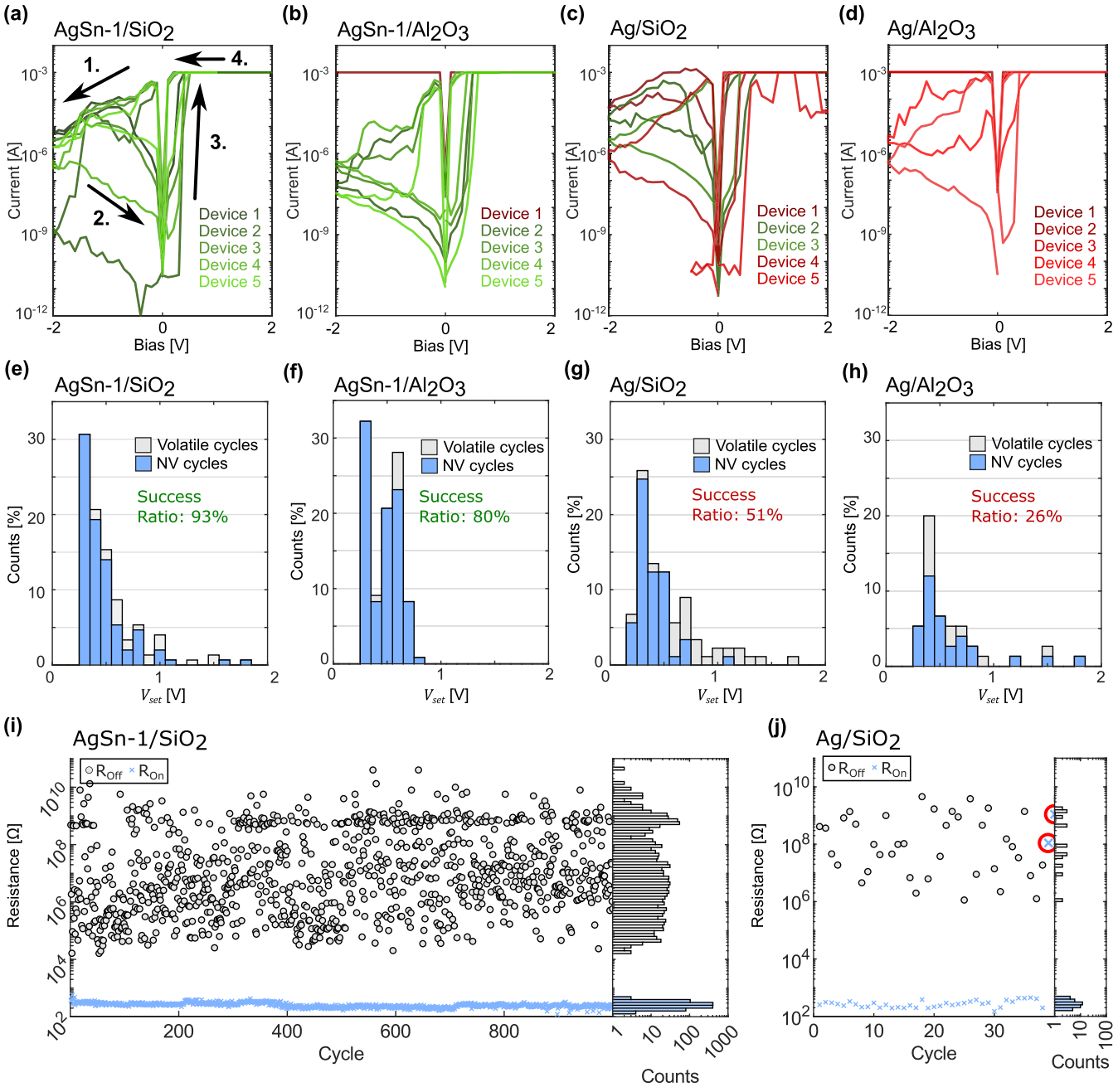

Figure 4. Comparison of five AgSn-1 devices against five pure Ag devices in the nonvolatile regime. (a–d) Median $I(V)$-switching cycles taken from the first 30 cycles measured on each device with indicated cycling direction. The green-colored devices successfully complete these 30 cycles, while red-marked ones fail before completing them. (a) AgSn-1/SiO_2. (b) AgSn-1/Al_2O_3. (c) Ag/SiO_2. (d) Ag/Al_2O_3. (e–h) Histograms of the extracted set voltages. The number of volatile cycles is shaded in gray, while the number of nonvolatile (NV) cycles is colored in blue. The success ratio is the percentage of successfully completed cycles (independent of volatility). (e) AgSn-1/SiO_2. (f) AgSn-1/Al_2O_3. (g) Ag/SiO_2. (h) Ag/Al_2O_3. Endurance comparison between AgSn-1 and Ag. (i) AgSn-1/SiO_2 device showing an endurance of 1000 $I(V)$ cycles without errors. The off-state (gray circles) shows no overlap with the on-state (blue crosses) as can be seen in the histogram inset. (j) Ag/SiO_2 device failing before completing 40 cycles due to unsuccessful switching from the high to low (red circles), remaining in the off-state.

state resistance. The off-state resistance is taken to be the median of the last five points before the end of a cycle.

RESULTS AND DISCUSSION

Control of Volatile/Nonvolatile Operation Point by Current. In this section, we discuss how the volatile or nonvolatile operation of a memristive device can be tailored by properly setting the compliance current. However, the operation in the nonvolatile regime is usually affected by a trade-off with reliability due to the high currents. This will be investigated in the following section.

CBRAMs have two interesting operation modes: volatile and nonvolatile. We observed that these operation regimes could be accessed by varying the compliance currents. If the compliance current is low, then one typically finds volatile threshold switching. If the compliance current is high, nonvolatile resistive switching dominates. In fact, one can transition from one operation mode to another by increasing

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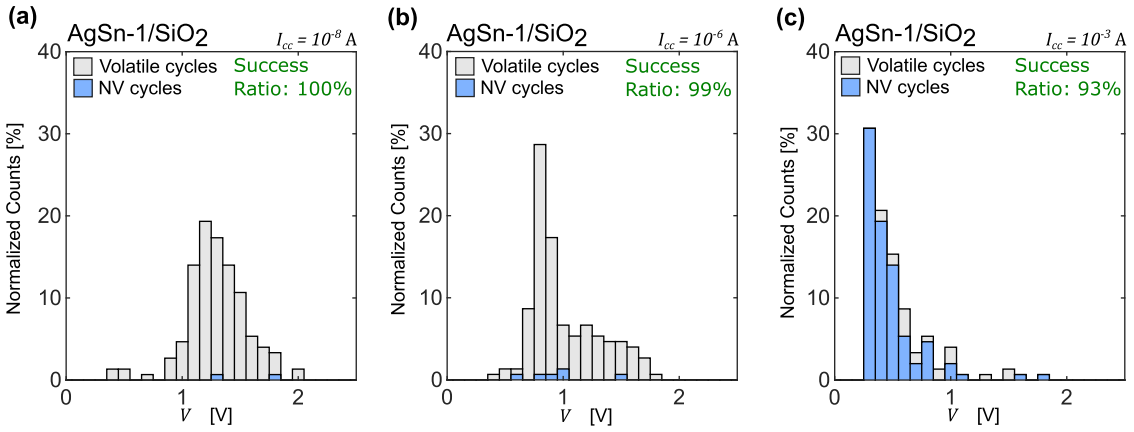

Figure 5. Histograms showing the operation change of AgSn-1/SiO_2 CBRAMs from volatile to nonvolatile with increasing compliance current (I_{cc}). Each plot contains 30 cycles of five CBRAMs each totaling 150 cycles. The compliance currents are (a) 10^{-8} A, (b) 10^{-6} A, (c) 10^{-3} A. The V_{set} distribution changes with higher currents to a lower mean and smaller spread. Success ratios are consistently high in both operation modes.

the compliance current. Devices then change from volatile threshold switching to nonvolatile switching. Similar observations have been reported for other CBRAMs.[14,26,32] This behavior is most likely the result of the different filament diameters: Lower compliance currents lead to thinner filaments compared with the larger filaments at higher compliance currents. The larger filaments are more stable due to the smaller surface to volume ratio and, thus, are less effected by Rayleigh instability.[33]

While tailoring the operation mode is one thing, the success ratio for obtaining either operation mode is still a bigger challenge. Figure 3 shows the success ratio, defined as the ratio between successful and attempted cycles in relation to the compliance current. Additionally, the ratio of nonvolatile cycles is indicated by the darker part of the bar. It can be seen that the nonvolatile regime at high currents in general has the disadvantage of a low success ratio. This behavior can be observed in nearly all the tested materials, as demonstrated in Figure 3 at a compliance of 1 mA.

To determine the influence of the current on success ratio and nonvolatility as shown in Figure 3, cyclic voltammetry measurements are employed. Toward this goal, the device under test (DUT) is directly connected to a source measurement unit (SMU) as shown in the setup in Figure 1c. A triangular voltage sweep from −2 V up to 5 V is then applied and the current through the DUT was measured. The current through the DUTs is limited to different levels in order to investigate its influence on the device characteristics and to prevent the devices from destruction. Details regarding the measurement scheme and analysis of the data can be found in the Experimental Section.

In conclusion, nonvolatility can be controlled by the current through the DUT, but at the price of a lower reliability. The higher currents lead to the formation of a stable and thicker filament, which is also indicated by the drastic reduction of the on-state resistance (Figure S5), at the risk of possible damage to the devices.

Tailoring the Yield by Alloying. In this section, we show that a choice of silver (Ag) with tin (Sn) improves the reliability performance in the nonvolatile regime. Toward this goal, six top electrode materials together with the three oxides (SiO_2, Al_2O_3, HfO_2) were characterized electrically to find the optimum nonvolatility vs success ratio. All combinations, with the exception of AgCu-1/SiO_2, were measured. AgCu-1/SiO_2 could not be measured due to issues during the fabrication process.

In the previous section, we stated that increasing the compliance current leads to an increase of nonvolatile operation but comes at the expense of successful switching. Nonetheless, there are two material combinations, which are to a lesser extent impacted by this general behavior, as can be seen in Figure 3e: AgSn-1/SiO_2 and AgSn-1/Al_2O_3. They have a high success ratio at 1 mA (92 and 80%) while also exhibiting high nonvolatility (>80%). The experiments with these material systems warrant further characterization and analysis. Interestingly, both of the AgSn/Al_2O_3 devices start in the on-state and require a higher current for resetting, explaining the low yield at low currents. Further insight into the device behavior will be gained by the STEM-EDX analysis in a later section.

More detailed distributions of the set voltages (V_{set}), reset voltages (V_{reset}), on-state resistances (R_{on}), and off-state resistances (R_{off}) across all measurements can be found in the Figures S3−S6.

These supporting data show the potential of AgSn-1/SiO_2 as a memristive device arrays. They show high device uniformity (Figure S3), tunability of the on-state resistance (Figure S5), and high off-state resistance (Figure S6). High-density memristive arrays pose a challenge due to the downscaling of the metal lines, which leads to an increase of the series resistance. Therefore, the remaining voltage drop over the device itself might be limited. Our devices offer a large on-state resistance window within which the resistances can be tuned (10^8−10^2 Ω). Therefore, we can adapt the on resistance to the line series resistance. Additionally, the high-off resistance (10^{11}−10^7 Ω) ensures that enough voltage can drop over the device to turn it on.

Performance Improvement by Sn Alloying. Additional $I(V)$ and endurance measurements in this section show the improvements of reliability and variability of V_{set} in the nonvolatile regime gained by alloying Ag with Sn. Figure 4 shows these improvements with two different material complexes: AgSn-1/SiO_2 and AgSn-1/Al_2O_3 by comparing them with Ag/SiO2 and Ag/Al_2O_3, respectively.

Figure 4 illustrates the median set $I(V)$ traces for AgSn-1 in SiO_2 and Al_2O_3. The results showed that 5 out of 5 devices successfully completed 30 cycles in the SiO_2 switching layer, and 4 out of 5 devices successfully completed 30 cycles in the

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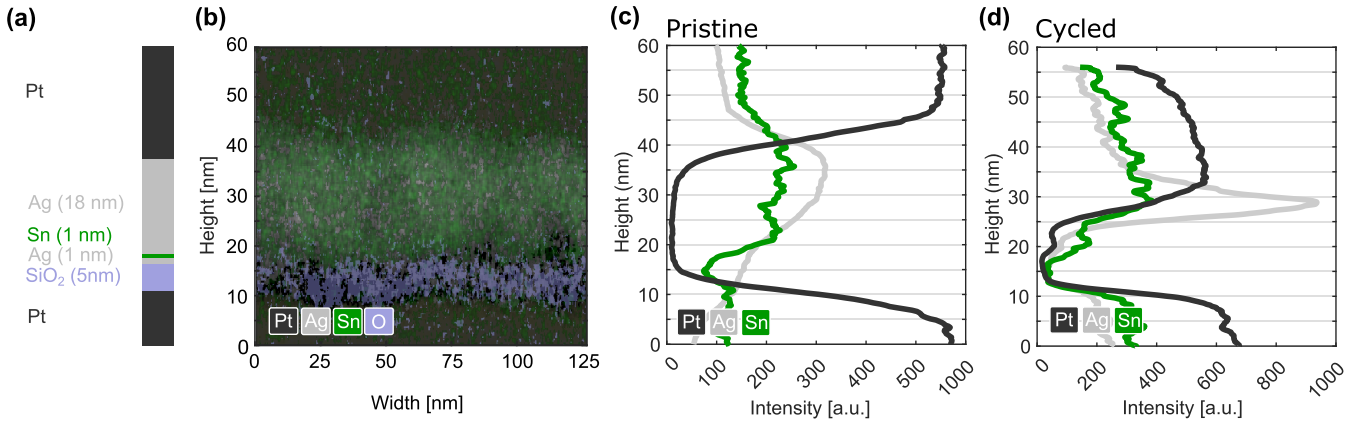

Figure 6. AgSn-1 material analysis using SiO_2 as the switching layer. (a) Layer stack as deposited during fabrication. (b) STEM-EDX analysis of a pristine uncycled device showing Pt (dark gray), Ag (light gray), Sn (green), and O (light blue). (c) Concentration curves of a pristine device demonstrating the intermixing of Ag and Sn. (d) Concentration curves of a cycled device. Cycling the device results in an accumulation of Ag and Sn at the bottom electrode, showing the involvement of both metals during the switching as an active mobile species. Note that the intensities of (c) and (d) are quantitatively not comparable.

Al_2O_3 switching layer. The single device failure was due to a reset error, and the device ended up stuck in the on-state. In comparison, the Ag devices exhibit worse performance for both switching media. In SiO_2, only two measured devices were able to perform these 30 cycles without failing to set or reset (Figure 4c). In Al_2O_3, none of the randomly selected ones were able to complete 30 cycles. All five ended up stuck in the on-state and not being able to be reset (Figure 4d).

Figure 4 shows the V_{set} distributions for AgSn-1 and Ag in both SiO_2 and Al_2O_3. The difference in performance can be clearly seen by the success ratio of AgSn-1 (93 and 80%) compared to Ag (51 and 26%). Also the nonvolatile ratio increased by alloying Sn (85 and 97%) compared to single top metal Ag (58 and 86%). Overall, the switching improved as can be seen by the lower and narrower distribution of the median switching voltages; see Figure 4a–h.

Additionally, endurance measurements were conducted as seen in Figure 4i,j. Randomly selected devices of both material complexes were cycled. AgSn-1/SiO_2 performed 1000 cycles with a narrow R_{on} distribution and without a failure as seen in Figure 4i. Ag/SiO_2 failed before 40 cycles due to a switching error. The device ended up stuck, as marked by the red circles, in the off-state of Figure 4j. These results clearly demonstrate the superior performance of the AgSn-1 alloy at high currents compared to the standard Ag electrode. A comparison between two different AgSn-1/SiO_2 fabrication batches can be found in Figure S7.

Controlling of AgSn-1/SiO_2 Volatility by Current. In this section, we show that AgSn-1/SiO_2 CBRAMs can be controlled for volatile or nonvolatile operation by current control with high yield. Figure 5 illustrates the controlling for volatile and nonvolatile operation of AgSn-1/SiO_2 by plotting the V_{set} characteristics of five devices at three different compliance currents (10 nA, 100 μA, 1 mA). At low compliance currents, almost all cycles exhibit a volatile operation (Figure 5a). They do so with a 100% yield. When increasing the compliance to 1 μA, increasingly more devices show a nonvolatile switching behavior, see Figure 5b. The figure also shows that the V_{set} distribution changes to a lower value. Finally, at high compliance currents of 1 mA, the device behavior changes predominantly to a nonvolatile operation. The V_{set} distribution moved further down and narrowed (Figure 5c). A high yield of 93% is found. This high yield is found only for the AgSn-1/SiO_2 material stack.

These results show that it is possible to control the volatility and nonvolatility of a CBRAM with only the compliance current. However, it is necessary to alloy the material stack (e.g., to add Sn) such that the devices retain a high yield when higher currents are applied (Figure 4e,g).

Structural Role of Sn. In this section, we show that the improved reliability for the nonvolatile operation of the alloyed memristor is most likely the result of Sn inclusion inside of the Ag filament structure. This conclusion is supported by STEM-EDX analysis. Additionally, the performance of AgSn-2 devices is discussed.

It can be shown by scanning transmission microscopy energy-dispersive X-ray (STEM-EDX) analysis that Sn is participating in the filament formation during cycling operation. We compare pristine and cycled device. Toward this end, devices with a layer stack as depicted in Figure 6a were used. An analysis of the pristine sample shows the diffusion and intermixing of Sn with Ag, as shown in Figure 6b. Integrating the atomic traces in the EDX image along the device width allows one to plot the material distributions across the device; see Figure 6c. The black, gray, and green solid lines show the distribution of Pt, Ag, and Sn in the pristine device. We find two high Pt plateaus at the top and bottom, indicating the Pt capping layer and the Pt bottom electrode. There is uniform distribution of Ag and Sn in the top electrode above the oxide indicating the fast diffusion of Sn into the Ag. Sn is mostly absent within the SiO_2 gap between the electrodes, and only small traces are found at the bottom electrode. The EDX data show initial Ag diffusion into the oxide of the pristine device as can be seen by the presence of Ag in the switching medium and at the bottom electrode. For the AgSn-1/SiO_2 devices, this concentration was not high enough to lead to an initial on-state. In fact, all memristive switches with the exception of AgSn/Al_2O_3 started in the off-state and needed a forming cycle. Figure 6 shows the EDX analysis on a cycled device. Going from the top metal toward the oxide, we can first observe an accumulation of Ag and Sn and then a depletion of both when approaching the SiO_2 interface. Inside the SiO_2, we do not detect any metals, which is to be expected due to the filamentary nature of the devices.

https://doi.org/10.1021/acsaelm.3c01275
ACS Appl. Electron. Mater. 2023, 5, 6842−6849

Yet, on the counter Pt electrode, there are now strong Ag and Sn signals, indicating the movement of both species through the SiO_2 during the cycling of the device. This leads us to believe that Sn acts as a mobile species and fulfills a critical role in stabilizing the filament, thus leading to the observed increase in reliability and device performance.

A binary phase diagram of Ag and Sn is needed (see ref 34 and Figure 1 therein) to discuss the difference in performance between AgSn-1 and AgSn-2. Due to the nominal thicknesses of the layers, we can only estimate the ratio of compounds. From the phase diagram, we can identify a Ag-rich f.c.c. phase where Sn is soluble until 11.5%. Alloy AgSn-1 is situated in the middle of this section with an estimated Sn ratio of 4%. AgSn-2 with an estimated tin ratio of 8.5% is close to the border of the disordered ζ phase. Thus, it is highly likely that this recipe consists of a mixture of f.c.c. and c.p. hexagonal lattices, and an inhomogeneous mixture of different phases may be the reason for the very different behavior and performance of the AgSn-2 alloy.

CONCLUSIONS

In conclusion, we show that AgSn-1/SiO_2 memristors can be tailored for volatile or nonvolatile operation by material engineering and current control with high yield. Our initial investigation confirms the possibility to control the volatility or nonvolatility of a memristor using compliance current. However, it is noted that the nonvolatile regime typically results in a compromised yield due to the high operating currents. We addressed the aforementioned trade-off by investigating secondary metallic species (Cu and Sn) to be included in the active electrode (Ag and Cu) and utilizing different switching media (SiO_2, HfO_2, Al_2O_3). We identified an alloy of Ag and Sn in combination with SiO_2 as a preferred material stack for (non)volatility tailoring.

Our approach improved the targeted parameters of yield (51−93%), nonvolatility (59−85%), and endurance (<40 cycles to >1000) in the nonvolatile regime compared to the standard Ag/SiO_2 device. The set (reset) voltage distribution is low and narrow in the nonvolatile regime with a median of 0.4 V (−0.43 V) and a standard deviation of 0.27 V (0.24 V). In the volatile operation point, the set voltage is 1.3 V with a standard deviation of 0.26 V. Energy-dispersive X-ray (EDX) analysis revealed that Ag and Sn both act as mobile species during the switching process, strongly indicating a stabilization of the filament structure due to the inclusion of Sn.

This work shows the ability to reliably tune the (non)-volatility of CBRAMs by current control and material engineering. We achieved a high yield by alloying the active metal and selecting the optimal switching layer. The tunable (non)volatility makes our devices highly suitable for next-generation computing and memory architectures such as neuromorphic computing where a simultaneous implementation of different functionalities is necessary. Additionally, our approach can be extended to other material systems and may serve as a guide on the path toward new architectures.

ASSOCIATED CONTENT

Data Availability Statement

Data from this work are available upon reasonable request. Code from this work is available upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.3c01275.

SEM and TEM cross section of AgSn-1/SiO_2, retention, V_{set}, V_{reset}, R_{on} and R_{off} distributions, and batch comparison (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work has been funded by the Werner Siemens Foundation. We thank the Cleanroom and Operations team of the Binning and Rohrer Nanotechnology Center (BRNC)

for their support. We thank Dr. Peng Zeng from ScopeM for the support during STEM-EDX.

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