On-die CMOS temperature sensors

Master's Thesis
University of Turku
Department of Computing
LG Electronics Finland Lab Oy
2023
Antti Auranen

UNIVERSITY OF TURKU
Department of Computing

Antti Auranen: On-die CMOS temperature sensors

Master's Thesis, 53 p.
LG Electronics Finland Lab Oy
November 2023

Temperature changes can have an impact on the reliability and functioning of sensitive integrated circuits. In this thesis an analog DTMOS transistor temperature was designed and laid out in 22 nm CMOS fabrication process using Cadence Virtuoso electrical design automation suite. The design was verified and validated using Cadence Spectre electrical simulation software and the simulation results were analyzed and compared to previous sensor designs. The new design was found to be less power hungry but slightly less accurate than the original design. The new design also showed a significant improvement in operating voltage resilience compared to a previous design used at LG Electronics Finland Lab Oy. Over all the design goals were met and the sensor is ready to be added to be a part of a future integrated circuit.

Keywords: CMOS, DTMOS, temperature sensor, dynamic threshold, integrated circuit, semiconductors

Contents

List of Figures

List of Tables

List of acronyms

I_D Drain-to-source current

I_S Saturation current of a BJT

V_{Dsat} Saturation voltage

V_{GS} Gate-to-source voltage

V_{TH} Threshold voltage

ADC Analog to Digital Converter

BJT Bipolar Junction Transistor

BOM Bill Of Materials

CMOS Complementary MOSFET

CTAT Complementary-To-Absolute Temperature

D Thermal diffusivity

DTMOS Dynamic Threshold Metal-Oxide Semiconductor

EDA Electrical Design Automation

ETF Electro-thermal filter

FET Field-Effect Transistor

FF CMOS process corner: Fast NMOS, Fast PMOS

FS CMOS process corner: Fast NMOS, Slow PMOS

HDL Hardware Description Language

IC Integrated Circuit

IP Intellectual Property

k Boltzmann constant, $1.38 * 10^{-23} J/K$

LOCOS local oxidation of the silicon

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor

MOS Metal-Oxide Semiconductor

NMOS n-channel MOSFET

PCB Printed Circuit Board

PDK Process Design Kit

PMOS p-channel MOSFET

PTAT Proportional-To-Absolute Temperature

q $1.6 * 10^{-19} C$

RTD Resistance temperature detector

SF CMOS process corner: Slow NMOS, Fast PMOS

SS CMOS process corner: Slow NMOS, Slow PMOS

STI shallow-trench isolation

TSMC Taiwan Semiconductor Manufacturing Company

T Temperature in Kelvin

TT CMOS process corner: Typical

VDD Voltage at the drain terminal of a semiconductor

1 Introduction

Out of all the environmental quantities, temperature is the most often-measured. [1] Temperature measurement is so important because nearly every physical, chemical, biological and mechanical system is in some way temperature dependent.

Integrated circuits are not an exception in this regard: semiconductors electrical characteristics change according to temperature and this can have a significant impact on the reliability of sensitive analog and digital circuits built using these technologies.

As technology progresses, companies are able to integrate more and more functionalities into semiconductor chips. Many of these functionalities benefit from maintaining certain operating temperatures and/or adjusting device characteristics according to temperature. For example the refresh rate of certain digital memory cell structures needs to be adjusted according to temperature to reduce and prevent data-loss caused by leakage currents. [2] Thus it is often beneficial to be able to measure the internal temperature of a complex integrated circuit. A sensor device integrated within a microchip could be not only cost-effective as no external analog-to-digital converters and sensors would be required, but as it can be positioned within micrometers of the power intensive areas there would be minimal latency between temperature fluctuations and the measured temperature. [3]

1.1 Stakeholders

This thesis and the temperature sensor design and layout proposed in this thesis is made for LG Electronics Finland Lab Oy. LG Electronics Inc. is a South Korean electronics company that produces home entertainment products, home appliances and vehicle components among others. LG Electronics is the second largest television manufacturer in the world and employs 74 000 people globally [4].

LG Electronics Finland Lab Oy is a research and development laboratory located in Turku, Finland and is a daughter company of LG Electronics. LG Electronics Finland Lab Oy is specialized in the development of radio frequency and millimeter wave integrated circuits.

1.2 Scope and goal

This thesis describes the schematic and layout design process of a temperature sensitive microelectronic circuit to be utilized as a temperature sensor integrated into the silicon die of a microchip.

The goal of the described sensor design is to overcome the sensitivity to operating voltage the design previously used at LG Electronics Finland Lab Oy suffers from. An additional goal is lowered power consumption.

1.3 Thesis outline

In chapter 2 I will introduce what semiconductors and typical semiconductor devices are and how they operate. In chapter 3 I will explain how temperature affects the electrical properties of a metal-oxide semiconductor (MOS) devices. In chapter 4 a review into different common temperature sensing technologies is conducted. Chapter 5 explains the tools and methods used as well as my position in the project

team. In chapter 5 I also go through the common steps of designing an electrical schematic as well as laying out the physical design of the integrated circuit. In chapters 6 and 7 I explain the design and layout of the 22nm on-die temperature sensor I designed. Chapter 8 gives an overview of the results and implications of this thesis and finally in chapter 9 we draw conclusions from the results.

2 Semiconductor Technology

2.1 Semiconductors

A semiconductor is a type of material that has properties that are between those of conductors and insulators. This is due to the semiconductor having a crystal lattice structure with free electrons or so called holes. Holes are available space on the outmost electron shell of an atom and they act as positive charge carriers while electrons moving from atom to another in the crystal lattice act as negative charge carriers. [5]

Semiconductors are typically made of silicon (Si) as it is abundant in nature but other suitable materials, such as germanium (Ge), are used as well. Regular sand typically contains high amounts of silicon in the form of silicon oxide commonly known as quartz. [5]

Fabricating integrated circuits requires the addition of certain atoms into the semiconductor fabric. These impurities, often referred to as dopants, either donate electrons to the silicon atoms or accept electrons from the silicon atoms increasing the conductivity of the material. The added impurities, or dopants, create regions of excess positive or negative charge carriers in the semiconductor material, which can be used to control the flow of electrical current. [5]

Introducing acceptor atoms, such as aluminum (Al), boron (B), gallium (Ga) or indium (In) to the silicon lattice creates regions of excess positive charge car-

riers (holes) in the semiconductor material due to the dopant atoms having one valence electron less than the semiconductor material and we end up with p-type semiconductor. On the other hand the introduction of donor type dopants such as antimony (Sb), arsenic (As) or phosphorus (P) creates regions of excess negative charge carriers (electrons) due to the dopants having one valence electron more than the semiconductor material. This gives us n-type semiconductor. Creating adjacent regions of n and p doped silicon makes it possible to fabricate complex microelectronic devices depending on the order and choice of dopants. [5], [6]

The most common semiconductor devices include diodes, transistors, and integrated circuits. Diodes are semiconductor devices that allow current to flow in only one direction, while transistors are semiconductor devices that can be used as switches or amplifiers. Integrated circuits, or ICs, are complex semiconductor devices that contain multiple transistors and other electronic components integrated on a single chip. [5]

Semiconductor technology has revolutionized modern electronics and technology, enabling the development of smaller, faster, and more powerful devices. Semiconductor devices are used in a wide range of applications, including computers, mobile phones, televisions, and medical devices. The semiconductor industry is a highly competitive and constantly evolving field, with new materials and technologies being developed regularly. [7]

2.2 Diode

A pn junction, more commonly referred to as a diode, is realized by doping one part of a semiconductor n-type and another part adjacent to it p-type as presented in Fig. 2.1. The diode forms between the p^+ and the n regions. The metal (aluminum in this example) contacts to the diode must be connected to heavily doped regions or the realized device will be a Schottky diode. [5]

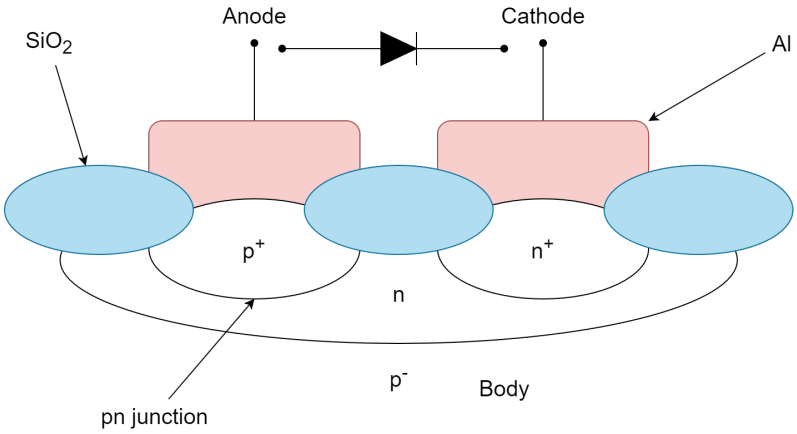

Figure 2.1: A cross-section of a pn diode. The superscripts denote relative doping levels. [5]

Due to the p^+ zone having a large quantity of free positive charge carriers and similarly the n side having a large quantity of free negative charge carriers these carriers have a tendency to diffuse into each other in a random manner. Due to this diffusion, the concentration of free carriers becomes lower in the junction area between both sides. Each electron that diffuses into the p side from the n side leaves a bound electron behind and likewise each hole that diffuses into the n side from the p side leaves behind a bound positive charge. Due to this diffusion a so called depletion region is formed as shown in Fig. 2.2. The p^+ side has a net negative charge and the n side has a net positive charge. In this junction no free charge carriers exist. The total charge must be neutral and thus the depletion region extends deeper into the more lightly doped side. [5]

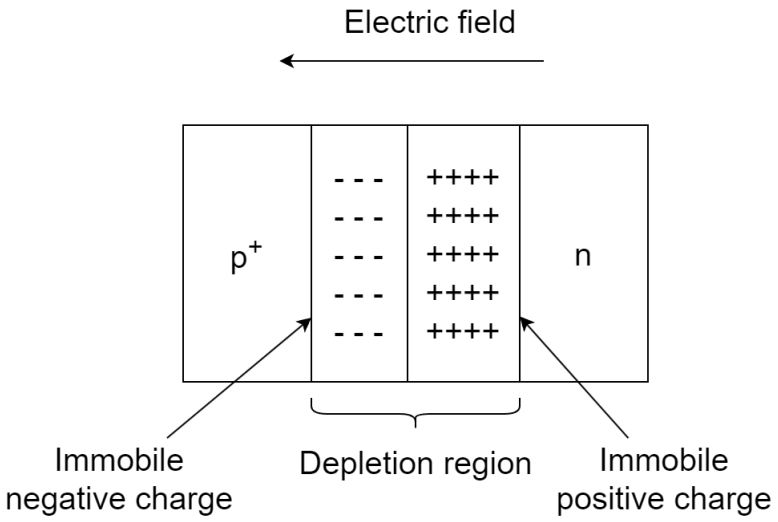

Figure 2.2: A simplified model of a pn junction diode [5]

These bound charges create an electric field from the n side to the p^+ side and a potential difference between the sides forms. This potential difference is referred to as the built-in voltage of the junction. The built-in voltage acts as an opposing force against diffusion of the free carriers. Assuming steady-state and open-circuit conditions, eventually the net movement of the charge reaches zero. The built-in voltage of an open-circuit pn diode can be expressed as

$$\Phi_0 = V_T ln \left(\frac{N_A N_D}{n_i^2} \right) \tag{2.1}$$

where

$$V_T = \frac{k_T}{q} \tag{2.2}$$

T is the absolute temperature in Kelvin, k is Boltzmann's constant and q is the charge of an electron. [8]

A silicon diode with a voltage of less than 0.4 V from the anode over to the cathode will not conduct excluding a tiny leakage current and is said to be reverse-biased. Current flow in reverse-biased state is mainly caused by thermally generated carriers within the depletion region. [8]

When a positive voltage from the anode to the cathode is applied the realized electric field reduces the electric field that opposes free carrier diffusion across the depletion region. In addition it reduces the width of the depletion region and when this voltage is large enough the charge carriers will be able to diffuse across the junction. This causes a current flow from the anode to the cathode. The required voltage to allow this current to flow depends on semiconductor material. For silicon it is roughly 0.5 V. [5]

2.3 Transistor

A transistor is a semiconductor component which has the ability to adjust current flow through itself. This effect can be used to make a transistor act as an active amplifier or a switch in a circuit. [9]

Transistors are commonly used in electronic circuits as amplifiers or switches. In amplification circuits, a small input signal is amplified by the transistor to produce a larger output signal. This is commonly used for example in audio and other signaling systems, where a weak signal from a microphone, antenna or other source is amplified to produce a stronger signal. [9]

In switching circuits, transistors are used to turn a signal on or off. This is commonly used in digital circuits, where a transistor can be used as a switch to represent a binary value of either 0 or 1. [9]

The development of transistors revolutionized electronics, enabling the development of smaller, more efficient, and more reliable electronic devices. Transistors are used in a wide range of applications, including computers, televisions, radios, medical devices, and many other electronic devices. The continued development of transistor technology has led to the development of smaller, faster, and more powerful electronic devices. [7]

A modern microchip can contain billions of transistors. For example the Apple

M1 Ultra central processing unit contains 114 billion transistors. [10], [11]

2.4 Bipolar Junction Transistor

A bipolar junction transistor (BJT) is historically the first transistor type that scientists managed to physically create. It was invented in 1947 at Bell Laboratories by the scientists John Bardeen, Walter Brattain, and William Shockley who were later awarded with the Nobel Prize in Physics in 1956 for the invention. [9], [12] It is called bipolar because both electrons and holes act as charge carriers in a bipolar device. [6]

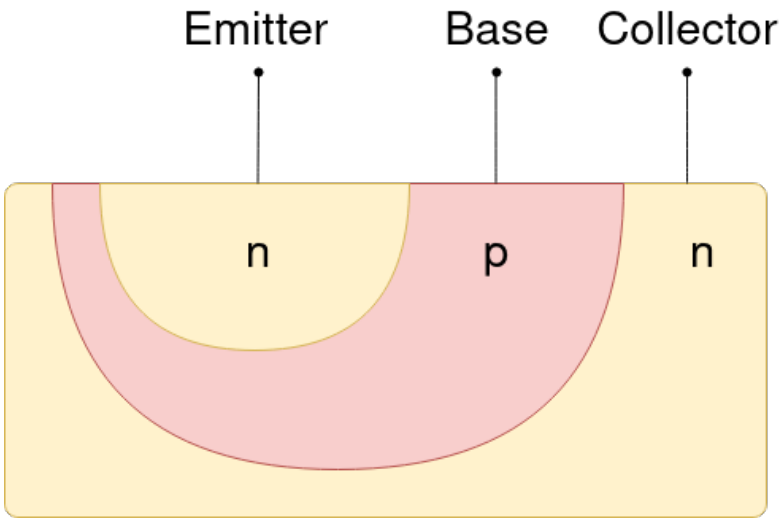

Figure 2.3: Cross-section of an NPN bipolar junction transistor

A BJT - pictured in figure 2.3 - has three terminals called emitter, base and collector. BJT's are separated into NPN and PNP types based on the arrangement of n-type and p-type semiconductor material. An NPN transistor is operated by driving a smaller control current from base to emitter causing a larger controlled current from collector to emitter. A PNP transistor is operated by driving a control current from emitter to base and this causes a larger controlled current to flow from emitter to collector. BJTs are in general more accurate and generate less noise than

field-effect transistors. [6], [9]

2.5 Field-Effect Transistor

A field-effect transistor (FET) is an active electronic component quite similar to the BJT but differs in that instead of a control current through the semiconductor a FET uses an electric field the to control the flow of current. A typical FET in an integrated circuit is made using a metal-oxide semiconductor (MOS) process which historically referred to the materials used to form the gate, insulator and channel regions respectively. This name is mostly historical however as most complementary MOS (CMOS) processes have replaced metal gates with polysilicon gates. Field-effect transistors realized in a MOS process are commonly referred to as MOSFET. [5], [9] The current carriers in a FET are either electrons or holes but not both simultaneously. Thus a FET is a unipolar device. [6]

A FET consists of three active terminals referred to as the source, the drain and the gate. Conductivity between the drain and the source is controlled by an electric field produced by creating a voltage difference between the gate and source terminals. FETs also have a fourth, passive terminal referred to as the bulk, the body or the substrate. [9]

The basic principle of field-effect transistor was first patented by Julius Edgar Lilienfeld in 1925 [13] but the first working prototype of such device took until 1960 after a series of innovations made it possible. Most notably Carl Frosch and L. Derick managed to accidentally grow an oxide layer on the silicon wafer in 1955. This silicon dioxide layer prevented the diffusion of dopants into the silicon wafer which was the main challenge preventing the fabrication of a FET. [14]

2.5.1 FET basics

MOSFETs are divided to two types by polarity: n-channel MOSFET also known as NMOS and p-channel MOSFET also known as PMOS. NMOS transistors use electrons as charge carriers while PMOS transistors use holes. [6]

Figure 2.4 shows a cross-section of two MOSFETs: NMOS and PMOS. On the bottom is a p-type silicon substrate. In the case of the NMOS the source and drain are doped as $n+$. The gate is created by growing an insulating silicon oxide layer on top of the substrate area between these two $n+$ areas and a polysilicon material is applied on top of this gate-oxide layer. This arrangement of materials creates two disjoint p-n junctions with a MOS capacitor bridge in the middle. When a positive voltage is applied to the gate, it creates a vertical electric field between the substrate and the gate. This field attracts electrons to the surface and when the concentration of electrons on the surface exceeds the hole concentration a conducting channel is formed between the drain and the source. In other words an inversion layer is formed. It is important to notice that the drain and source regions are physically identical. In an NMOS the $n+$ region with the lower potential is defined as the source and the other $n+$ region thus becomes the drain. As a conventional rule it is chosen to define all terminal voltages of a device respective to the source potential. [15] The minimum voltage from the gate to the source (V_{GS}) of a device required to form the channel is referred to as the threshold voltage V_{TH}. [15]

PMOS is a similar construction, but an n-type well has to be created in which two areas of $p+$ doped silicon are created to form the drain and the source. In a PMOS device V_{GS} and V_{TH} are inverted compared to an NMOS device. The n-well also has to be positively biased. [15]

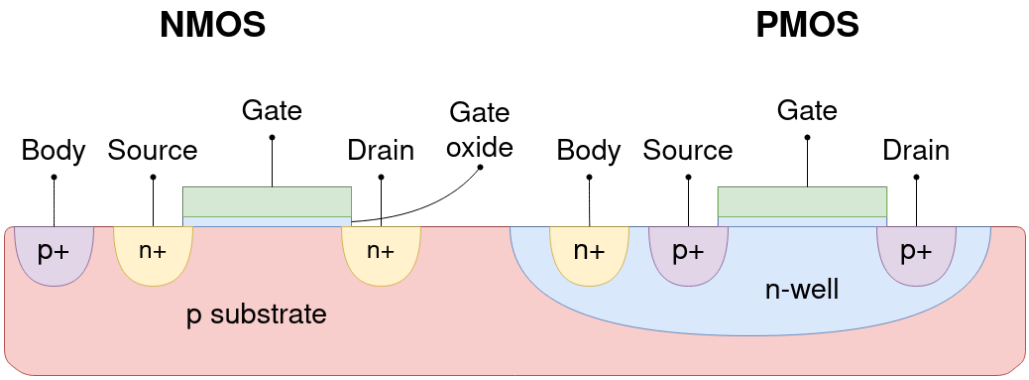

Figure 2.4: Cross-section of NMOS and PMOS transistors side by side [16]

2.5.2 FET operating modes

Before voltage is applied to the gate the transistor is said to be in the cutoff mode and the transistor is inactive.

When V_{GS} exceeds V_{TH} and a positive voltage is applied to the drain a current will begin to flow from the drain to the source. This current is called the drain current I_D and it is proportional to the drain voltage. The resistivity of the continuous inversion layer is dependent on V_{GS}. This is called the triode mode or linear mode and the transistor acts as a voltage-controlled resistor. [15] Triode mode drain current can be expressed as follows:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.3}$$

where μ_n is the charge-carrier mobility, W and L are the gate width and length respectively and C_{ox} is the gate oxide capacitance.

When we increase the drain voltage the channel depth at the drain end of the channel decreases and eventually we reach what is called the saturation voltage (V_{Dsat}). The drain current in this saturation mode can be expressed as follows:

$$I_{Dsat} = 1/2 \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{2.4}$$

2.5.3 Complementary Metal-Oxide Semiconductors

Historically the first MOSFET based integrated circuits used only n-channel transistors due to process limitations. However as the technology evolved and p-channel transistors became available and later possible to integrate on the same die together with NMOS transistors most of the semiconductor industry has moved to design and implement complementary metal-oxide semiconductors (CMOS) where both n-channel and p-channel devices are present on the same die. [5]

The advantage of CMOS technology can be easily visualized by looking at a CMOS inverter schematic diagram such as in the figure 2.5. When the input is high, the PMOS transistor at the top doesn't conduct, while the NMOS transistor at the bottom does and pulls the output potential to ground. On the other hand, when the input is low, the PMOS transistor lets current through from VDD to Out while the NMOS is off. Thus current only flows during switching of states. In addition as the gates are insulating, no passive currents aside from leakage are present. [6]

2.6 Semiconductor fabrication

Since the mid-1980s the majority of modern integrated circuits have been made in CMOS processes. [18]

Over the years there has been numerous different CMOS processes typically named after the minimum possible gate length as that was a conventional way for fabrication companies to market technological advancement over the competition. However due to competitive marketing, this naming convention over decades of semiconductor manufacturing processes eventually decoupled from the physical characteristic. In modern CMOS process nodes the label of the process has very little to do with the actual physical gate length. For example a 3nm node would

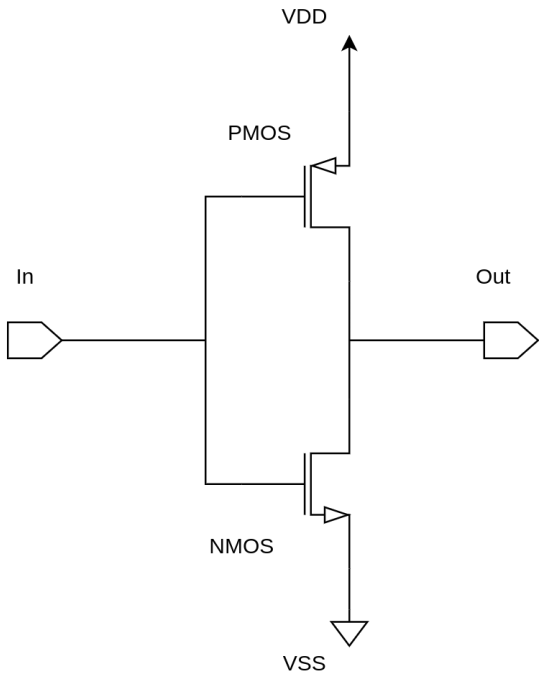

Figure 2.5: A simple CMOS inverter schematic [17]

imply a gate length of roughly 12 atoms. However it is important to understand this decoupling does not mean a lack of true improvements in the technology. [19]

2.6.1 Wafers

Semiconductors are fabricated on a circular disc of very highly pure monocrystalline silicon. These discs are typically called wafers and they are commonly made by a different company than the one that will fabricate integrated circuits into them. [5], [18]

To create silicon wafers a very highly pure silicon is first melted in a furnace. A shaft with a monocrystalline seed of silicon mounted on it is dipped into the molten silicon and then slowly rotated and raised at a precise speed to pull the molten silicon up via cohesion in a so-called Czochralski process. The ingots grown this way come in different sizes depending on the pull rate and speed of rotation and can weigh several hundred kilograms each. Typical ingots are more than 1 meter

long with diameter between 10 and 30 cm. Producing a single silicon ingot can take multiple days. [5], [18]

These cylindrical crystalline silicon bars are then cut into thin round discs using a diamond-coated saw. Theoretically these wafers could be as thin as a micrometer but in practice such silicon crystal would be too easy to break during handling. Thus most wafers are sawn to a thickness between $400\mu m$ and $1mm$. [18]

After the wafers are sawed from the ingot they are chemically and mechanically polished. [5]

As the top layer of the wafer is the substrate layer of the transistors, it needs to be doped. One method to achieving this background doping is to control the boron impurity levels in the ingot. Alternatively, it is possible to start with a very heavily doped p^{++} wafer and then grow a layer of p^{-} silicon on top of the wafer. All the devices would be realized in this top epitaxial layer. The benefit of having a heavier doped substrate underneath the epitaxial layer is to provide a higher level of control regarding dopant concentration while the p^{++} layer provides a low-resistivity ground plane. This ground plane underneath helps prevent latchup. [5]

2.6.2 Well definition

The actual transistors are realized inside so called well regions on the silicon substrate typically by using a photolitography process. These wells are areas that are either p or n type and contain either n-channel or p-channel transistors respectively. [5]

To be able to only realize these wells within specific areas of the wafer the silicon has to be selectively protected. This is done by creating a glass mask and covering it with photosensitive materials. The mask is then exposed to an electron beam that creates regions corresponding to the well areas turning these regions opaque. This mask acts as a negative for the first layer. Then a thin layer of silicon-dioxide

(SiO_2) is grown on the wafer to protect the surface. On top of the SiO_2 a light-sensitive photoresist is applied and an ultraviolet light is projected through the glass mask making the exposed areas insoluble to a solvent. Once the solvent is used, it removes the photoresist from the selected well areas and depending the process the uncovered SiO_2 may be removed using acid. After this the dopants are introduced either via diffusion or ion implantation resulting in a doped well. [5]

The wavelength of the light used imposes limits to the photolitography process. Any features smaller than the wavelength of light used will result in patterns on the photoresist not precisely matching the mask. However an optical proximity correction can be made to compensate against this by modifying the pattern on the mask to make the light create geometric patterns more closely matching what the designer intended. This correction is common practice in any feature sizes below 100nm. In addition techniques such as immersion to liquid causing a change in the path of the light are used to realize even smaller feature sizes. [5]

2.6.3 Well doping techniques

After removing the photoresist covering the well regions the dopants need to be introduced. It can either be done via diffusion or ion implantation. In diffusion implantation a quartz tube with the wafers inside is heated in a furnace and a gas containing the wanted dopant is introduced in the tube. The heat of the furnace causes the impurities to diffuse into the silicon through the areas exposed in the previous phase. [5]

In modern semiconductor fabrication ion implantation has become the more common method now as it allows a higher level of control over the concentration of dopants as well as the thickness of the doped region which in diffusion follows a Gaussian profile decreasing further in the silicon. Ion implantation uses ions that are generated by bombarding a gas with electrons. These ions are then accelerated

and passed through a slit purifying the ion beam from too heavy ions. This beam is then swept across the wafer using vertical and horizontal deflection plates. The acceleration potential of the beam is used to control how deep the implantation is and the dosage is limited by controlling the exposure time and beam current. [5]

2.6.4 Definition of the active regions

In this phase a new mask is used to define the transistor locations. First a thin layer of SiO_2 is again thermally grown to the surface of the silicon. Then a chemical vapor deposition technique is used to deposit Si_3N_4 everywhere. Then the photoresist is applied, exposed through the new mask, dissolved and hardened similarly to the technique discussed earlier. The photolitography process this time defines the active regions of the transistors. These areas are also known as oxide definition regions as they mark the areas where the very thin gate-oxide layer will be made. After a series of acid etching steps there are areas of Si_3N_4 left to act as a mask protecting the active regions during the realization of the isolation structures. [5]

2.6.5 Isolation structures

Whenever there's a conductor above and between the junction regions of different transistors a parasitic transistor is formed. This could cause issues such as unwanted leakage currents so to mitigate these issues it is common to perform extra processing such as local oxidation of the silicon (LOCOS) or shallow-trench isolation (STI). [5]

In LOCOS processing additional dopants are implanted between transistors. This increases the threshold voltage of the parasitic transistors which in turn reduces the current carrying capability of the parasitic transistor. In addition a very thick layer of SiO_2 is created on top of these areas. [5]

In an STI process trenches are etched into the substrate between the active regions and then filled with SiO_2. This process provides better isolation between

transistors and allows a tighter layout with less room between individual transistors. However it is more expensive due to requiring more steps than LOCOS. In addition the trench creation and filling causes strain on the silicon lattice affecting the electrical characteristics near the trench. [5]

2.6.6 Gate-oxide

In this phase the Si_3N_4 and SiO_2 are removed and using a dry process a thin gate-oxide is then grown everywhere on the wafer. After growing the gate-oxide layer, donors are implanted through the thin gate-oxide to adjust the threshold voltages of the transistors. [5]

2.6.7 Formation of polysilicon gates

In this phase the transistor gates are formed using a chemical deposition process. This can be achieved by heating the wafer and flowing silane gas over it causing the following reaction to occur

$$\mathrm{SiH_4} \longrightarrow \mathrm{Si} + 2\mathrm{H_2}$$

Using a lower temperature, approximately 650°C, when the original surface is SiO_2 the resulting silicon deposition will be amorphous or noncrystalline. This type of silicon is usually referred to as polysilicon. [5]

After this phase the whole wafer is covered in polysilicon. Again a new mask, photoresist and series of etching processes are used to remove the polysilicon elsewhere and leave just the gates in place. [5]

2.6.8 Junction implantation

Next, an ion implantation process is used to create the junctions. Using a mask, photoresist and etchingthe junction areas are revealed and dopants are introduced to the well creating the source and drain junctions. The channel side edge of these junctions is defined by the gate thus resulting in very little overlap. [5]

2.6.9 Metal layers

After the junctions have been formed the semiconductor routing must take place. This is done by depositing metal, for example aluminum or copper, on the wafer and patterning it using photolitography masks, photoresist and etching. There are typically up to ten metal layers with an insulating oxide in between. Finally a passivation is deposited using CVD SiO_2. [5]

3 Temperature effects on MOS transistors

Temperature affects silicon-based semiconductors by lowering both the mobility of charge carriers as well as lowering the threshold voltage of the transistor. [20]

3.1 Threshold voltage

It is commonly assumed [21] that the temperature dependence of the threshold voltage of a MOS transistor follows the equation

$$V_T(T) = V_T(T_0) + \alpha_{VT}(T - T_0) \tag{3.1}$$

and thus one can say that one of the primary effects of temperature on MOS transistors is the change in threshold voltage, which is the minimum voltage required to form a channel and thus activate the transistor. As the temperature increases, the threshold voltage decreases, which can result in increased leakage currents and decreased noise margins. This can cause errors in digital circuits and can also affect the power consumption of the device. [21]

3.2 Charge carrier mobility

The mobility of electrons and holes in the semiconductor material determines the speed of the transistor and its ability to switch on and off quickly. The mobility of

the transistor depends on temperature as [22]

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu} \tag{3.2}$$

As the temperature increases, the mobility of the charge carriers decreases, which can result in slower switching times and reduced performance. [23]

4 Temperature sensors in integrated circuits

In electronics temperature is traditionally measured using either resistance based temperature sensors or thermocouples. While these kinds of sensors achieve great precision and accuracy, they are relatively large and thus typically require a discrete component in an electronic device. [24] In the context of integrated circuits, using the temperature-dependent characteristics of the semiconductor makes it possible to integrate the sensor, or multiple sensors, directly on the silicon die of the microchip. [25]

Semiconductor sensors are typically fabricated as a part of a larger integrated circuit (IC). This is particularly useful in applications where the device temperature management is important as one could use this for example to throttle a processor core or to limit an amplifier output based on die temperature measured within micrometers from the high-power block. Fabricating the sensor in the IC is also beneficial in that it may lower the bill of materials (BOM) cost of the final product as the final product might not need a separate discrete temperature sensor along with any discrete components the sensor might have required in addition. [25]–[27]

4.1 Bipolar junction transistor temperature sensors

BJT devices can be realized as parasitic devices in CMOS technologies using the same diffusions that are typically used to realize MOSFETs. The Figure 4.1 shows a cross-section of a vertical PNP transistor. [3]

Use cases for parasitic vertical PNPs are somewhat limited due to how the collector is formed inside the P-substrate which causes the collector not being directly accessible. [3]

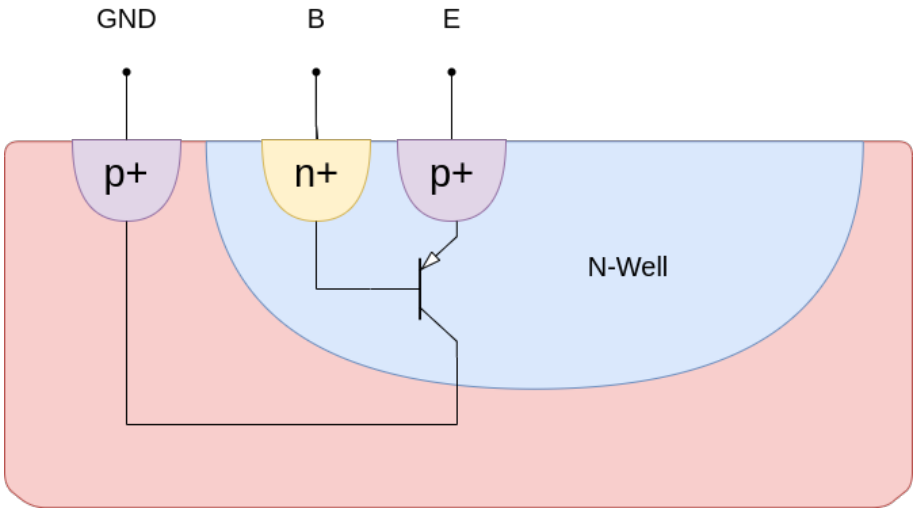

Figure 4.1: A cross-section of a vertical PNP transistor realized in a standard CMOS process [3]

The base-emitter voltage V_{BE} can be expressed as

$$V_{BE} \approx \frac{kT}{q} ln \left(\frac{I_C}{I_S} + 1 \right), \tag{4.1}$$

where k is the Boltzmann constant, T is the temperature in Kelvin and q is the electron charge. I_S represents the saturation current. [3] It has been shown that V_{BE} exhibits complementary-to-absolute temperature (CTAT) behavior [28]. When biased with different collector currents, the differences in two BJTs collector currents ΔV_{BE} will exhibit proportional-to-absolute temperature (PTAT) behavior.

Due to the well-defined temperature dependence of V_{BE} and ΔV_{BE} BJTs are often seen as an attractive choice to design CMOS temperature sensors with. [28] Due to the PTAT profile, inaccuracy caused by process spread can be corrected with a single-point offset correction. [3]

4.2 Resistance temperature detectors

Resistance temperature detectors (RTD) are temperature sensors utilizing the temperature dependence of certain resistor elements. RTDs are often implemented as discrete temperature-sensing components. [3]

Despite being relative accurate otherwise, resistors implemented in CMOS processes suffer from process spread in the range of 15-20 % between process corners. Due to this behavior RTDs typically require multiple calibrations in various temperatures to achieve reasonable accuracy. These additional calibration runs can increase the cost of the device as additional fabrication tests will have to be performed. [3]

4.3 Electro-thermal filters

For a highly pure silicon, such as the type of silicon used for IC fabrication the thermal diffusivity of the silicon is a well defined parameter. The definition of thermal diffusivity is the rate at which heat diffuses through a material. [29] D is also highly temperature dependent and this dependency can be approximated [30]. Due to the well-defined nature of the temperature dependency, this effect can be used in temperature sensor design. [3]

An electro-thermal filter generates heat pulses and a temperature sensor at a known distance s from the heater measures these pulses and converts them into a voltage signal. When examined in the thermal domain an ETF operates similarly to a low-pass filter and when driven at the right frequency the resulting signal will

have a temperature-dependent phase-shift. [31]

$$\phi_{ETF} \propto (s\sqrt{f_{ref})T^{n/2}} \tag{4.2}$$

where $n \approx 1.8$. As the true temperature readout is based on phase shift of the reference heater the temperature sensor needs to only know the relative temperature. [3]

A severe drawback of ETF is the relatively high power consumption of the heater and thus it is not well suited to low-power devices. However as the accuracy of an ETF relies on the litography processes accuracy in realizing the distance s, an ETF can reach decent accuracy with just a batch-calibration. No trimming of individual sensors required. [3], [31]

4.4 MOSFET temperature sensors

The drain current I_D of a sub-threshold biased MOSFET can be expressed as follows:

$$I_D^{bulk} \propto \frac{W}{L} exp\left[\frac{q}{mkT}\left(V_{GS} - V_T^{bulk}\right)\right], \tag{4.3}$$

where k is the Boltzmann constant, T is the temperature in Kelvin and q is the electron charge. W and L are respectively the width and length of the transistor. The body effect coefficient $m = 1 + C_D/C_{OX}$ where C_D is the depletion-layer capacitance and C_{OX} is the gate-oxide capacitance. [32] One can see similarities between the equations 4.1 and 4.3 and that suggests MOSFETS could be used to replace BJTs as temperature sensors in CMOS processes. The gate-oxide capacitance C_{OX} and threshold voltage V_T^{bulk} suffer from process spread. As there are two variables related to process spread, at least two temperature calibrations are required for the sensor to be usable in most applications. The benefit of a MOSFET compared to BJT is that the V_{GS} of a sub-threshold biased MOSFET can be considerably lower than

the operating voltage of a BJT. [3]

One possible CMOS temperature sensor principle is to measure the propagation delay of an inverter chain. Fig. 4.2 shows a block diagram of how a simple clock counter can be used to measure the time required for a trigger signal to pass through multiple CMOS inverters. The average propagation delay T_p of a balanced CMOS inverter [33]

$$T_p = \frac{(L/W)C_L}{\mu C_{OX}(V_{DD} - V_T)} \cdot ln\left[\frac{3V_{DD} - 4V_T}{V_{DD}}\right] \tag{4.4}$$

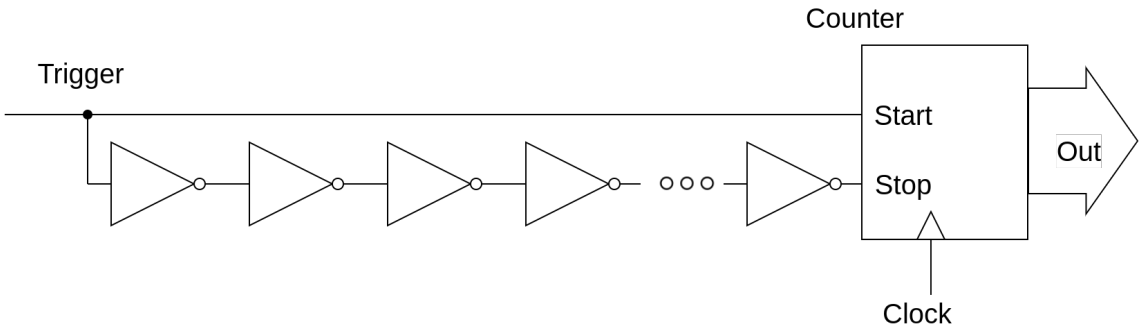

Figure 4.2: Block diagram of a CMOS inverter delay measurement [3]

4.5 Dynamic Threshold MOSFET

When a normal MOSFET is biased in the sub-threshold region, the drain current can be described as follows:

$$I_D^{body} \propto exp\left[\frac{q}{mkT}(V_{GS} - V_T^{body})\right] \tag{4.5}$$

where k is the Boltzmann's constant, T is the temperature in kelvin, q is the elementary charge, m is the body effect coefficient which equals $(1 + C_D/C_{OX})$. C_D is the capacitance of the depletion-layer and C_{OX} is the gate-oxide capacitance ie. the capacitance of the gate of the transistor. [32]

The depletion-layer capacitance C_D depends on surface potential and well doping, while process spread worsens the oxide capacitance C_{OX}. The threshold voltage V_T^{body} is affected by the body effect and thus $(V_{GS} - V_T^{body})$ is a function of I_D^{body}. What this means is V_{GS} and I_D^{body} relate approximately exponentially. [32]

A diode connected p-channel DTMOS transistor schematic is presented in figure 4.3.

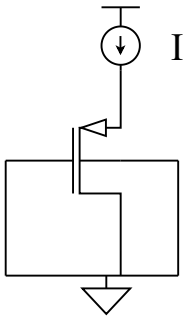

Figure 4.3: A schematic of a DTMOS transistor [25]

In practice, the device is a p-channel MOSFET or PMOS which can be found in most CMOS processes as a standard. In this PMOS the source, gate and body of the transistor are connected together. The width of the depletion layer under the channel becomes fixed due to the connection between the gate and body terminals. Thus when operated in the sub-threshold region the drain current I_D^{DT} of the DTMOS transistor can be expressed as follows:

$$I_D^{DT} \propto \frac{W}{L} exp\left[\frac{q}{kT}\left(V_{GS} - V_T^{DT}\right)\right] \tag{4.6}$$

We can observe that the threshold voltage V_T^{DT} is well-defined due to the connection between the gate and body of the DTMOS transistor. Resulting from this, the DTMOS diode has a nearly ideal relationship between V_{GS} and I_D^{DT}. [25]

5 Methods

The research was conducted at LG Electronics Finland Lab Oy which is a research and development laboratory focused on the design of radio frequency integrated circuits. During the research I worked as an intern in the analog design team and I was assigned a task to design a better temperature sensor as the previously used design had issues with reliability regarding operating voltage fluctuations.

The electrical schematic and layout were designed using Virtuoso electrical design automation (EDA) software and the simulations were performed using the Spectre simulation software. Both software belong to the analog IC EDA tool lineup of Cadence Design Systems

The project was organized as a waterfall and the deadline for the sensor was by the end of the year 2021.

5.1 Design process workflow

The figure 5.1 visualizes a possible overall flow of an analog or mixed-signal IC design project from conceptualization to IC fabrication according to Gielen and Rutenbar [34]. The project flow model presented by Gielen and Rutenbar is divided in multiple phases: System concept, System design, Architectual design, Cell design, Cell layout, System layout. After each design and layout phase the result of the phase is simulated and verified before moving on to the next phase. [34]

5.1.1 System Concept

In the System Concept phase the team gathers specifications and constraints and the general product concept, ie. what the actual device is designed to do, is developed. In this stage tools like Matlab and Simulink are typically used to create a mathematical model of the product. It is also important to set up project management goals during this phase. For example final product cost, time-to-market and general project planning. [34]

5.1.2 System Design

When the system is conceptualized, the first actual design phase takes place. In this phase the over all architecture of the system is partitioned and designed. Both hardware and software components are defined and behavioral level descriptions of hardware components are made using appropriate hardware description languages. Any interfaces have to be specified and decisions regarding implementation such as target technology process, packaging, and general strategy of testing have to be made in this phase. [34]

5.1.3 Architectural Design

In this phase the specified behavioral description is decomposed into a high-level architecture consisting of functional blocks. Analog and digital blocks are partitioned and the specifications regarding these blocks are defined. Hardware description languages (HDL) are used to describe these various blocks. [34]

5.1.4 Cell Design

The detailed implementation of the analog blocks in the form of a device-level schematic takes place in this phase. In this phase the designer will decide on a

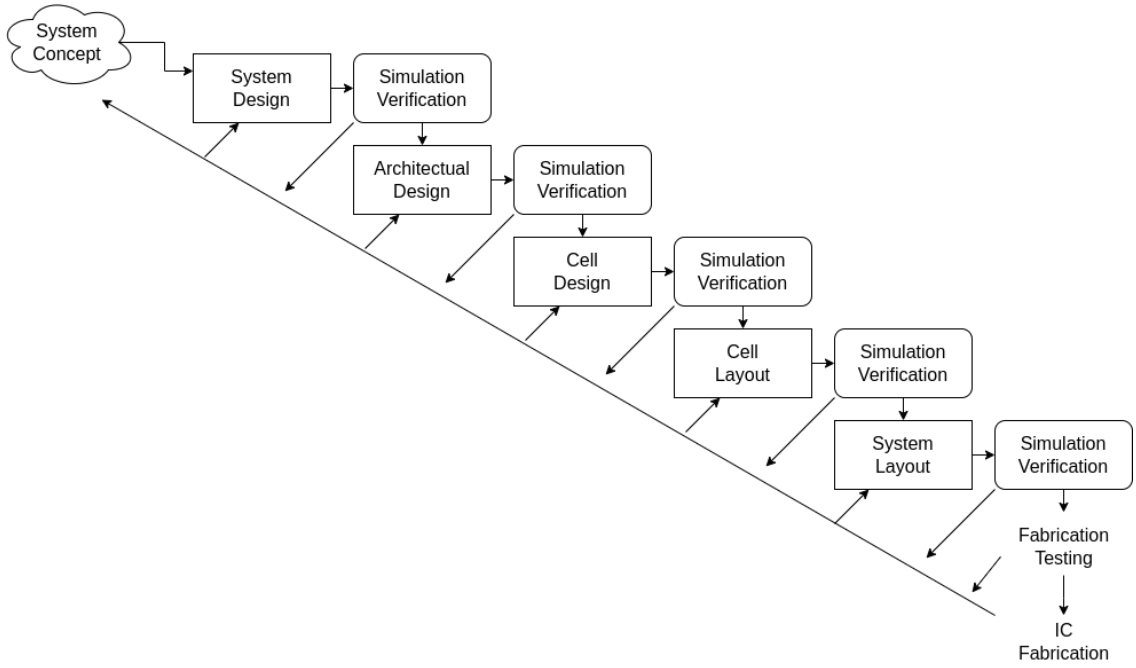

Figure 5.1: High level flow chart of an analog IC design process [34]

circuit topology as well as circuit parameter sizing. More complex blocks will be designed as a set of subblocks. The designer will take into account manufacturability such as mismatches and tolerances. [34]

5.1.5 Cell Layout

In this phase the electrical schematic is conveyed into a form of a multilayer layout that represents the actual physical layout of the circuit. In this phase the designer optimizes the block area and aims to reduce unwanted parasitic characteristics. [34]

5.1.6 System Layout

After a cell layout block is finished, it is added to the system level layout of the IC. In this phase the inter-block connections are designed together with power-grid routing. Test structures are added to ensure the finished physical IC can be tested

thoroughly. In this phase it is important to perform analysis regarding substrate coupling and trace crosstalk. [34]

5.1.7 Simulation and Verification

After each phase the relevant parts are simulated and compared against the higher level design. Any unwanted behavior is corrected by backtracking and redesigning the relevant parts of the design. [34]

5.1.8 Fabrication

After the system level layout is designed, simulated and verified, the complete design is transferred to fabrication. In this phase the IC is fabricated and tests are performed in various stages of fabrication as well as after the fabrication. [34]

5.1.9 Process corners

CMOS fabrication processes are never perfect. Slight variations in material properties and the precision of the manufacturing equipment cause physical inconsistencies within the semiconductor which causes inconsistencies in carrier mobility, threshold voltage and junction capacitances. High carrier mobility is referred to as fast and low carrier mobility is referred to as slow as carrier mobility directly affects the switching speed of the transistors. As there are both NMOS and PMOS transistors in a CMOS circuit two-letter acronyms are the common naming convention for the corners: FF, SS, FS, SF and TT. F stands for fast, S stands for slow and T stands for typical. The first letter corresponds to the speed of the NMOS transistors while the second letter corresponds to the speed of the PMOS transistors. In addition it is common to refer to the TT or typical case as a process corner even though it technically is not a corner case. Corners are used to simulate and verify that the

circuit works correctly in the extreme worst cases when it comes to manufacturing inconsistencies. [5]

5.1.10 Monte Carlo Simulation

Monte Carlo is a method of experimental calculation using random numbers to test various possibilities regarding a complex system. [35]

In the Monte Carlo simulation phase the same simulation is ran multiple times while randomly altering process parameters for each simulation run according to the process variation models provided by the fabricator. This provides understanding of the reliability of the design throughout the variations and imperfections of the semiconductor fabrication processes. [36]

5.1.11 Computer Aided Design Tools

Electrical Design Automation (EDA) software tools are used throughout the design process. EDA tools are software and hardware that are designed to assist companies and individual designers in performing the various steps required to design IC's, printed circuit boards (PCB) and other electrical systems. [37], [38]

5.1.12 Process Design Kit

Process design kit (PDK) is a package or library containing the available components, their simulation models and design rules for a specific IC fabrication process. PDK's are provided by the silicon foundry and they play a crucial part in helping the designers verify and validate their design. [39]

5.2 Layout design workflow

Once the conceptual design of the intended integrated circuit is designed as a schematic, the individual components and their relation to each other are imported into a layout design software. This list of components and their relations is referred to as a netlist. [40]

5.2.1 Transistor realization

Analog integrated circuits are typically composed of much wider individual transistors than digital circuits. To reduce process variation effects the transistor is typically laid out by either using multi-finger transistors or by dividing the transistor into identical copies of smaller transistors. It is also common to have multiple copies of multi-finger transistors. These smaller transistors are connected in parallel. Should one require precision matching between transistors, then the transistors should be laid out as single-sized units in a common-centroid pattern. The common-centroid pattern is discussed further in section 5.2.2. In addition the transistor fingers should be interdigitated with the fingers of the second transistor and so on. [5]

5.2.2 Common-centroid layout

In a common-centroid layout the transistor gate fingers are laid out such that the linear gradient in any device parameter, such as gate-oxide thickness, across the whole circuit has ideally a net-zero effect on device performance. [5]

As discussed earlier, a single transistor is divided into multiple mutually identical smaller units. These smaller transistors are spread so that the mean position of the individual transistors are the same as can be observed in figure 5.2. [5]

In figure 5.2 the rectangles marked by letters A-E represent transistor units. Units that form a single transistor in schematic are marked with the same letter.

Lines are drawn to represent that each transistor unit is laid out so that the mean distance from the center (marked with a red dot) is zero for each transistor A-E.

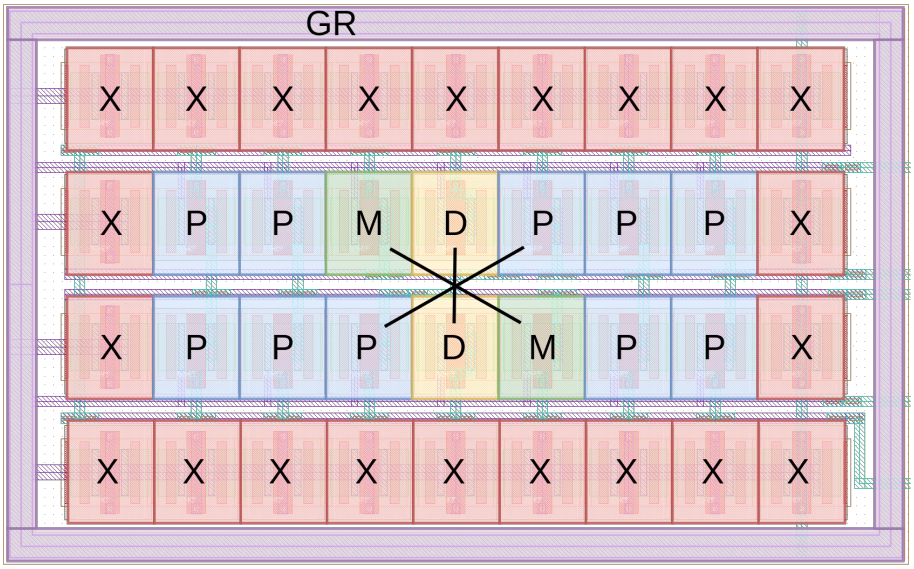

Figure 5.2: A common-centroid layout scheme.

5.2.3 Dummy devices

In integrated circuits (IC), dummy devices are structures that are added to a layout or design but do not perform any electrical function. Instead, their purpose is to ensure that the manufacturing process is consistent and that the finished ICs meet certain specifications. [41]

Dummy devices are often used to balance the stress and strain on a wafer during the manufacturing process. When a wafer is heated and cooled during the fabrication of an IC, it can warp or bend slightly. This can lead to variations in the dimensions of the devices on the wafer and affect their electrical properties. By adding dummy devices to the layout, the stress and strain on the wafer can be balanced, reducing variations and improving yield. [41]

Dummy devices can also be used to ensure that the metal layers in an IC are uniform. Metal layers are used to connect different devices on an IC, and variations

in the thickness or shape of these layers can affect the electrical properties of the IC. By adding dummy devices to the metal layers, the thickness and shape can be controlled more precisely. [41]

Overall, dummy devices play an important role in ensuring the consistency and reliability of ICs during the manufacturing process.

In the figure 5.3 is shown a current mirror layout. In the figure dummy devices are highlighted with red boxes and marked with "X". The dummy devices are laid out around the active transistors.

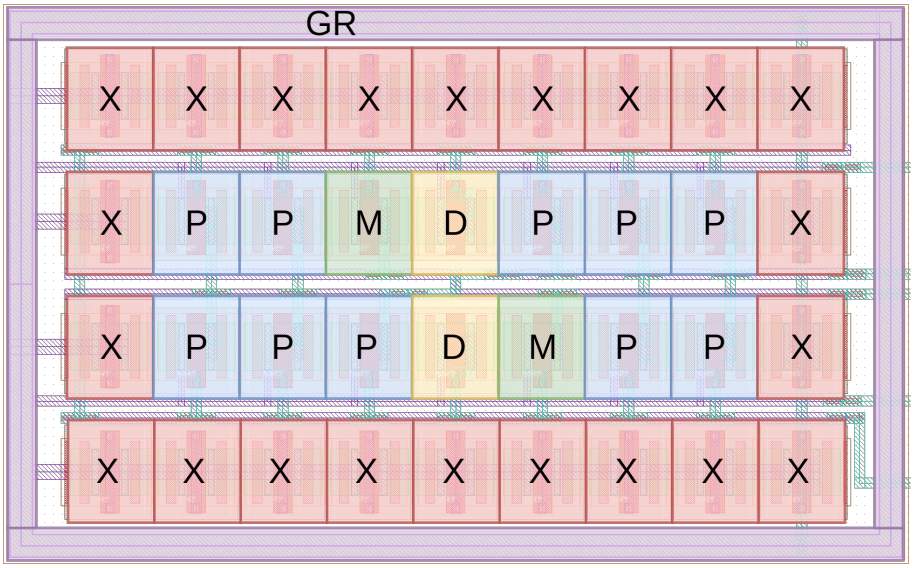

Figure 5.3: A common-centroid layout of the current mirror

5.2.4 Guard rings

Guard rings are structures that are commonly used in ICs to prevent unwanted electrical signals from interfering with the functioning of the IC. They are typically made of a metal or semiconductor material and are placed around the periphery of the IC. [42]

The primary purpose of a guard ring is to protect sensitive circuitry inside the IC from external noise or interference. This is especially important in analog and

mixed-signal ICs, where even small amounts of interference can cause significant errors or signal distortion. The guard ring acts as a shield, preventing electrical signals from leaking in or out of the IC block. [42]

Guard rings can also be used to reduce the impact of parasitic capacitance and leakage currents in the IC. Parasitic capacitance is an unwanted capacitance that arises from the layout of the IC and can cause delays or distortions in the signals. Leakage currents are unwanted electrical currents that can cause errors and unwanted in the functioning of the IC. By placing guard rings around sensitive areas of the IC, these effects can be minimized. [42]

Another use of guard rings is to control the electric field in the vicinity of the IC. The electric field can affect the functioning of the IC, and by carefully designing the shape and placement of the guard ring, the electric field can be controlled and minimized. [42]

In the figure 5.3 the guard ring surrounds the whole current mirror block and is highlighted in purple and marked with "GR".

5.2.5 Current mirror

A current mirror is a type of circuit that takes a current in its input terminal I_{in} and produces an equal output current I_{out} at its output terminal. Figure 5.4 represents a simple PMOS current mirror. Current mirrors are commonly used in integrated circuits to provide precise and stable current sources for various applications such as biasing transistors or driving other circuitry. [5]

In a PMOS current mirror, two PMOS transistors are connected in a common source configuration, with their gates connected together. A current is applied through the reference transistor pulling the gates down and activating both the reference and mirror transistor. Thus the current flowing through the reference transistor is mirrored by the other transistor. The mirrored current is determined

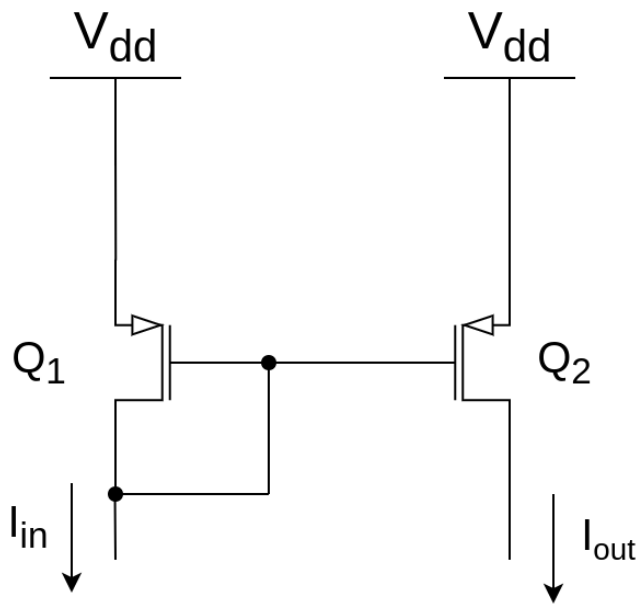

Figure 5.4: A PMOS current mirror

by the relative sizes of the transistors as well as the reference current. [5]

6 Dynamic threshold MOS transistor sensor design

6.1 Introduction

In this study a dynamic threshold MOS transistor temperature sensor schematic was designed, laid out and simulated in 22 nm CMOS process by Taiwan Semiconductor Manufacturing Company (TSMC). The implemented design is based on one proposed by Souri et al. [25] The original sensor design is implemented in a 160 nm CMOS process and has an inaccuracy of ± 0.4°C with a single offset trim at 30°C. As analog CMOS designs in general get worse when the process is scaled down it was expected that this sensor would not perform as well as the original in terms of measurement accuracy. [43]

6.2 Deciding the sensor type

While planning the sensor type there were many options to choose from. According to Souri et al. [3] the most precise on-die CMOS temperature sensors were typically designed using parasitic bipolar transistors implemented in a CMOS process. However it was quickly decided against using BJT devices in this project due to the difficulty of consistently implementing parasitic BJT devices in the current and future fabrication processes. In addition a BJT based approach can draw a rela-

tively large amount of power and is thus not well suited should the end product be battery powered. It is expected a design intellectual property (IP) is designed once and reused whenever possible across different projects as the designing process is slow and the designer time is relatively expensive.

Moving forward the choice was limited to either a diode-connected DTMOS transistor, ie. a DTMOS diode, sensor design proposed by Park et. al. [2] which periodically discharges a capacitor through a temperature sensing DTMOS diode or a dual DTMOS diode sensor design by Souri et. al. [25]. The latter design was chosen as it was a simpler design, the paper provided good estimates of the sensors capabilities on an older, 160 nm CMOS process and the design is not very susceptible to process spread and voltage supply fluctuation. The chosen design also doesn't require a digital controller or precise timing like the capacitor discharging model would and could just be measured using an analog to digital converter (ADC).

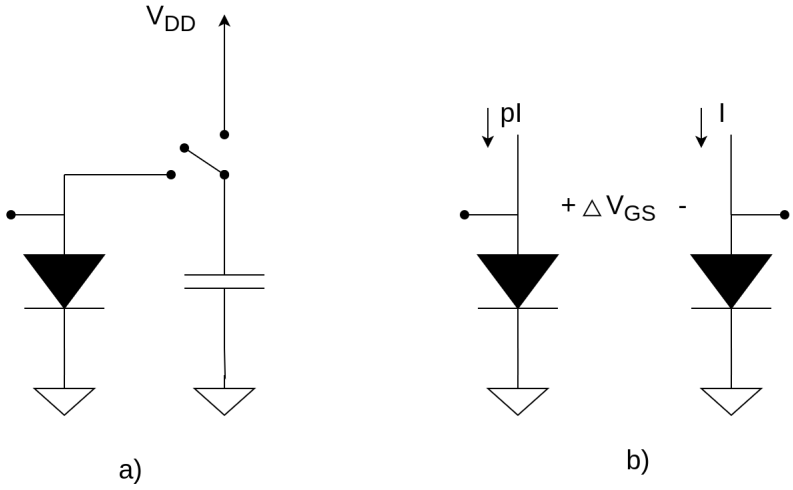

Figure 6.1: a) diode-capacitor switching sensor [2] b) continuous diode sensor [25]

6.3 Theory of operation

The sensor design is based on two identical PMOS transistors in a dynamic threshold configuration with the gate, body and source terminals of each transistor connected to the electrical ground. In this configuration both PMOS transistors act as diodes. In the DTMOS configuration the width of the depletion layer is fixed which results in the threshold voltage V_{TH} to change dynamically. [3]

The gate-source voltage (V_{GS}) of a DTMOS diode can be observed to follow complementary-to-absolute temperature (CTAT) behavior. On the other hand the gate-source voltage difference between two DTMOS diodes, ΔV_{GS} follows proportional-to-absolute temperature (PTAT) behavior:

$$\Delta V_{GS} = \left(\frac{kT}{q}\right) \cdot ln(p) \tag{6.1}$$

where $\frac{kT}{q}$ is the thermal voltage and p is the bias current ratio. [3]

6.4 Sensor design

In the schematic (figure 6.2) the PMOS diodes D_1 and D_2 are biased with biasing currents I and pI respectively and this creates a temperature dependent voltage difference ΔV_{GS}. The biasing currents I and pI are mirrored from Q_{bias} with a PMOS current mirror where the Q_{bias} and Q_2 are identical and $W_{Q1} = pW_{Q2}$. The V_D of the current mirror is connected to VDD through a PMOS transistor to allow enabling and disabling the sensor when required. [3]

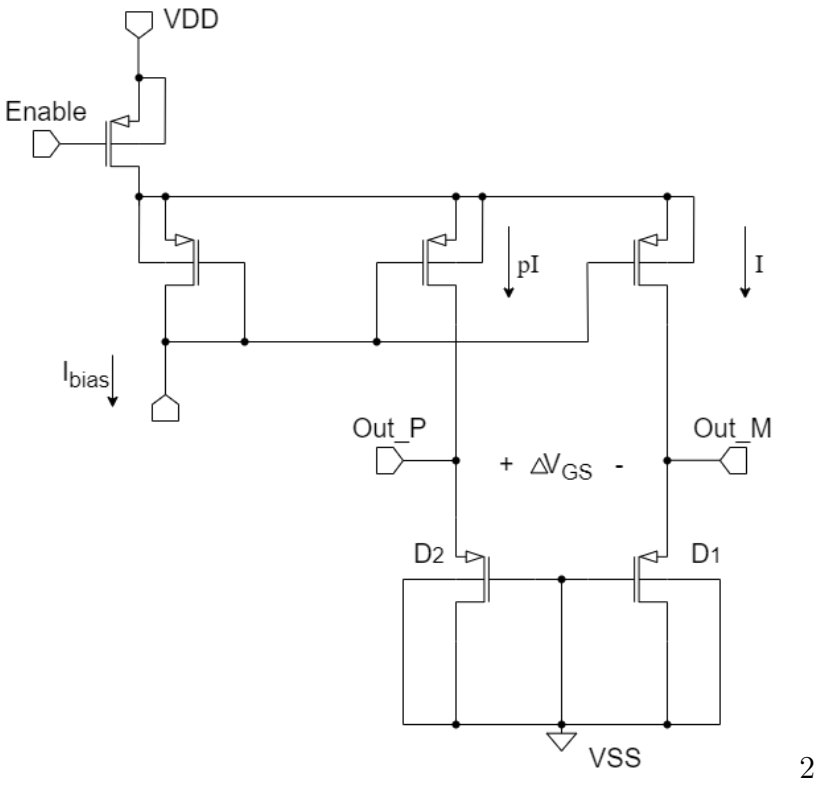

Figure 6.2: Temperature sensor schematic

The figure 6.3 shows how the gate-to-source voltages of the sensor transistors behave in a temperature sweep as well as the voltage difference $\Delta V_{GS} = V_{GS2} - V_{GS1}$

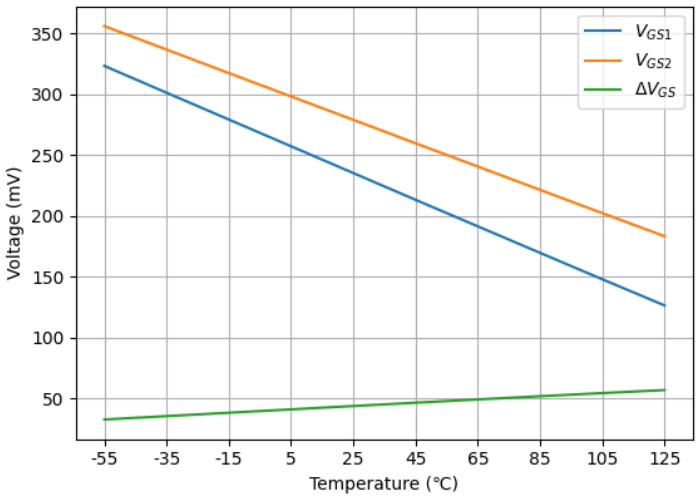

Figure 6.3: Temperature dependence of V_{GS1}, V_{GS2} and ΔV_{GS}

6.5 Simulation

The designed circuit was simulated using the Spectre simulation platform by Cadence Design Systems. The simulation results were post-processed and visualized with Python scripts written by the author.

The design was initially simulated using the typical corner model of the transistors to verify the design works as intended. After the typical simulation results were good enough, the design was simulated using process corners and finally using a 200 point Monte Carlo simulation. In each simulation a temperature sweep was performed to visualize how the measured voltages change in different temperatures.

6.5.1 Monte Carlo

A Monte Carlo statistical analysis was performed to visualize the effect of process spread for the design. Multiple iterations of the design were tested in this phase. The Figure 6.4 shows a temperature sweep Monte Carlo simulation of 200 points on the left together with the histogram of the values of ΔV_{GS} at 25°C. The histogram displays the effect of fabrication process spread on the sensor design.

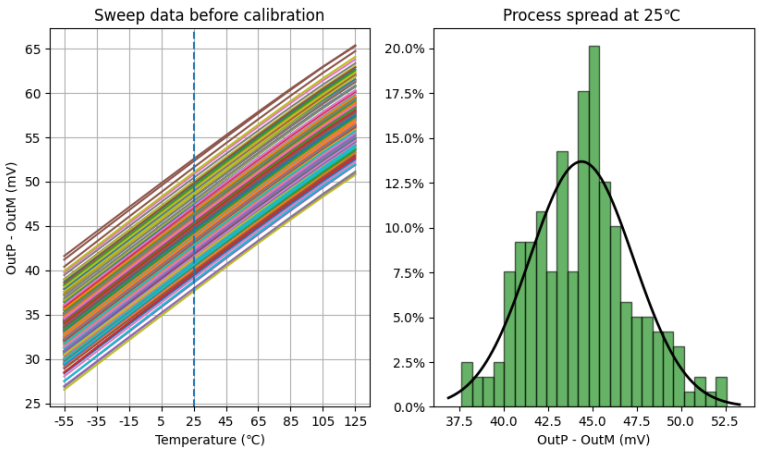

Figure 6.4: 200 sweep Monte Carlo simulation in a temperature range -55 to 125°C without calibration

In the final iteration of the design the temperature error was measured with a single offset calibration at 25°C as can be observed in the figure 6.5

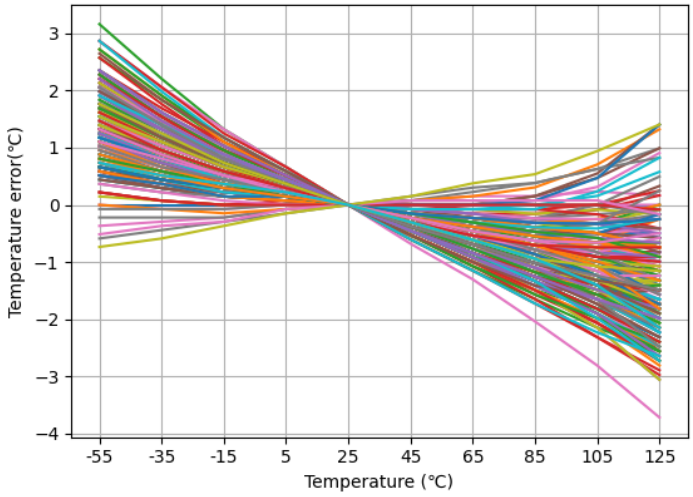

Figure 6.5: Temperature errors of 200 Monte Carlo simulation runs with a single point calibration at 25°C

This type of simulated post-calibration accuracy gives us understanding of the requirements regarding the sensors calibration before it can be utilized properly.

6.6 Voltage supply sensitivity

It is not uncommon to have up to 10 % mismatch in the supply voltages of an integrated circuit. Thus it is important to find out how a supply voltage above or below the expected voltage would affect the sensor readout.

To test the sensor sensitivity for supply voltage variations the sensor was simulated with three different supply voltage values along the military temperature range -55 to 125°C. The ΔV_{GS} voltage slope at the nominal 850 mV supply voltage was used as a reference to convert the ΔV_{GS} values into temperature. These values were compared with the nominal slope to find out the exact celcius value of temperature

offset.

As can be observed from the figure 6.6 the simulated sensor exhibits an error of roughly $\pm 0.08°C$ with a peak of $-0.14°C$.

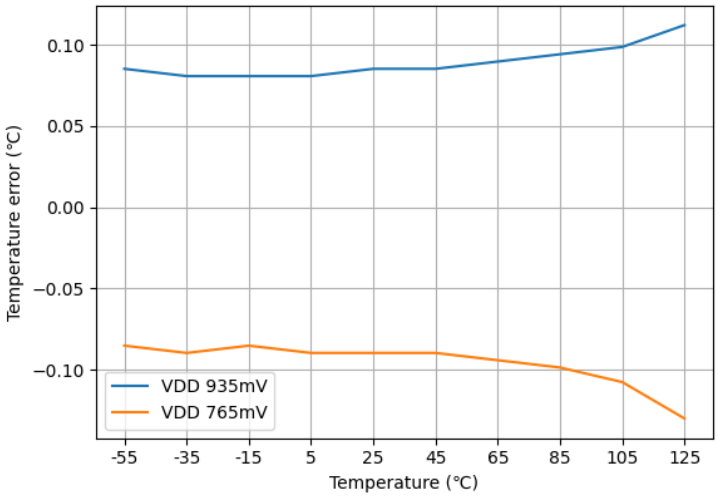

Figure 6.6: Supply voltage sensitivity of the sensor at $\pm 10\%$ supply voltage

7 Layout design of the sensor

An overview of the layout is shown in Figure 7.1. An enabling PMOS-transistor switch is located in the middle with the PMOS current mirror on the left and the sensing transistors on the right. Each sub block is shielded by using guard rings. Each sub block is arranged in a common-centroid pattern and the active transistors are surrounded with dummy transistors to minimize the effects of process variation.

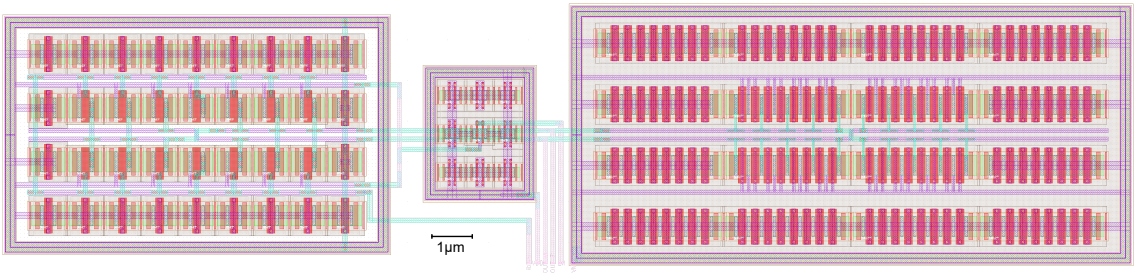

Figure 7.1: Temperature sensor layout

7.1 Current mirror

As the current mirror was designed with 1 to 1 and 1 to 5 ratio respective to the reference transistor it was decided to double the transistor number in order to achieve a common-centroid layout. In Figure 7.2 is shown a closer image of the current mirror layout with the arrangement of transistors highlighted.

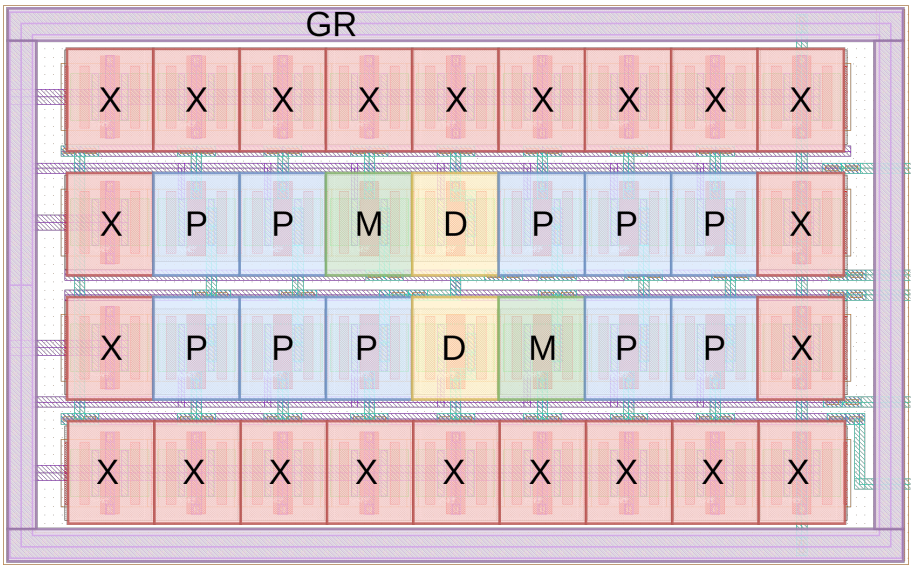

Figure 7.2: A common-centroid layout of the current mirror

7.2 DTMOS diode sensor

The dynamic threshold diode temperature sensor, shown in Figure 7.3, consists of two identical PMOS transistors in a diode configuration where the drain terminals are connected to the 1:1 and 1:5 outputs for the M and P bias currents respectively and the gate, source and body terminals are connected to ground. Due to the body terminals of the sensor transistors being connected to the ground the sensor block needs to be put inside a separate N-well and have a separate guard ring than the enable switch transistor and the current mirror.

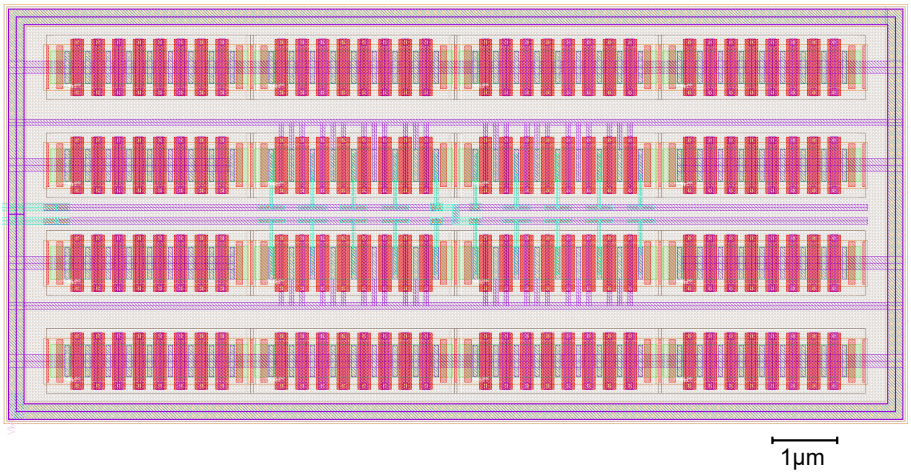

Figure 7.3: Layout of the sensor transistors

8 Discussion

8.1 Summary of contribution

There is little public research on temperature sensing in 22 nm analog CMOS processes. This thesis presents a small-footprint low-power temperature sensor suitable for the needs of modern integrated circuits.

8.2 Implications for practice

The temperature sensor presented in this thesis is small enough to integrate one close to every power intensive part of the chip such as amplifiers and CPU cores providing accurate temperature readouts and making possible dynamic temperature throttling of power-intensive parts.

As can be observed from the Figure 6.6 the error in temperature readout regarding operating voltage fluctuation of $\pm 10\%$ is under ± 0.10°C when the temperature is below 85°C. When we compare the output error to the original sensor design used at LG Electronics Finland Lab Oy in Figure 8.1 we can observe temperature readout fluctuation of ± 20 to ± 60°C.

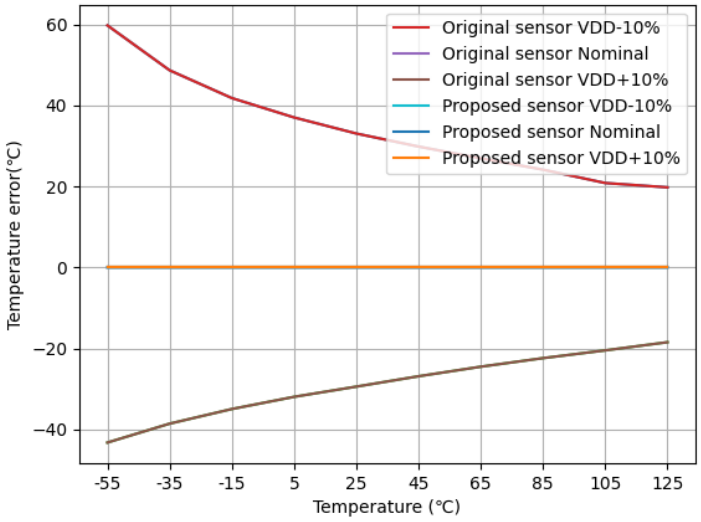

Figure 8.1: Supply voltage sensitivity of an old temperature sensor used in a previous project compared to the sensor design proposed in this paper

8.3 Implications for theory

The findings of this study provide strong empirical support for the temperature sensor model proposed by Souri et al. [25]. By demonstrating its applicability in 22 nm, this research validates the theory and provides understanding of how such sensors behave in smaller process nodes.

8.4 Limitations and future work

While this study has yielded valuable insights, it is important to acknowledge several limitations that may affect the interpretation and generalizability of the findings. In particular the performance of the sensor design was validated in Cadence Spectre simulation tool according to the PDK provided by TSMC. While Spectre is generally considered reliable it doesn't match the reliability of real world data of the sensors performance on a physical silicon die measured in a laboratory. IC samples with the

Table 8.1: Sensor performance comparison

Sensor	Process	V_{DD} (V)	Power (μW)	Inaccuracy (°C)
Original [3]	160 nm	1.8	8.6	0.4
This thesis	22 nm	0.850	0.39	1.5
Previous design	22 nm	0.800	32	

sensor design examined in this thesis did not arrive during the process of writing this thesis.

In the future the sensor will be tested as a part of a complete IC and the various applications where this type of sensor could be used for will be beneficial to study.

Future improvements of this sensor design could encompass lower process spread and higher accuracy.

8.5 Results

The original design proposed by Souri et al. [25] was designed in an older, 160 nm process and used a higher supply voltage of 1.8 V. The original design according to Souri consumes $8.6\mu W$ power in 30°C. In comparison the design proposed in this paper was designed in a 22 nm process and used a supply voltage of 850 mV with a power draw of $0.39\mu W$ in 30°C. With a smaller process and lower operating voltage we were able to reduce the power draw of the sensor by 95% while increasing the single-trim inaccuracy from ±0.4°C to ±1.5°C. The Table 8.1 shows a comparison between the original 160 nm design, my design and the previous temperature sensor design used at LG Electronics. The table shows operating voltage, power consumption during use and temperature reading inaccuracy caused by process variation with a single temperature offset trim. The previous designs inaccuracy data wasn't available.

From the Figure 6.4 one can observe the sensor is sufficiently linear but a single

point calibration is mandatory to perform before the sensor data can be considered practical. With multiple calibration points the error margin between different sensors could be pushed even smaller.

As the errors caused by process variations are closer to $\pm 1.5°C$ after a single point trim it can be stated that the error margin caused by the voltage supply variation is insignificant.

In a case of supply voltage fluctuation of $\pm 10\%$ the sensor exhibits an error of roughly $\pm 0.08°C$ with a peak of $-0.14°C$.

9 Conclusions

This thesis aimed to find and design a suitable temperature sensor for an integrated circuit. The goal was to find a better alternative to an older design suffering from supply voltage fluctuation.

Before looking into the sensor design itself, this thesis explained the basics of semiconductors, how temperature affects them and some example concepts for temperature sensing using integrated semiconductors. In addition the process of designing an integrated circuit from concept to fabrication is summarized.

Chapter one gives a brief introduction into the subject of the thesis and presents the stakeholders and goals to be reached with this study.

In chapter two a general look into semiconductor physics and CMOS electronics is presented.

In chapter three we looked into what effects temperature has on CMOS electronics and semiconductors in general.

Chapter four presented a review of some popular temperature sensing concepts that can be implemented in CMOS processes.

Chapter five explained the project structure, deadline and project organization regarding the sensor design project.

In chapter six an IC design process is described from system concept to IC fabrication. Design tools are also reviewed in this chapter.

Chapter seven gives us an overview of analog IC layout concepts and design

guidelines.

In chapter eight, the sensor design concept was chosen from literature review and the process of implementing it is explained. The sensor design was simulated and tested in various ways to verify and validate it works properly for the use case.

In chapter nine the layout design of the sensor is presented and discussed.

The sensor designed in this thesis achieved precision of $\pm 1.5°C$ which is somewhat worse than the original design proposed by Souri et al. [3] The lack in precision is compensated by low power consumption of $0.39\mu W$. This is 95% better than the original sensor.

As the main intended function of the design is to provide data on the internal temperature variations of a chip the achieved single-offset trim accuracy of $\pm 1.5°C$ is very good. Together with the low power consumption and low operating voltage sensitivity the result was deemed a success.

This sensor design plays an important role in gaining a better understanding of future integrated circuits designed at LG Electronics. The added ability to measure device temperature accurately without adding components to the product can generate savings but I think most importantly it allows better analysis of the products under development while still in the research and development laboratory.

Future improvements of this sensor design could encompass lower process spread and higher accuracy.

References

[1] National Semiconductor Corporation, "Temperature sensor handbook", 1978.

[2] S. Park, Y. Kim, W. Choi, *et al.*, "A dtmost-based temperature sensor with 3σ inaccuracy of ± 0.9°c for self-refresh control in 28nm mobile dram", in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4. DOI: 10.1109/CICC48029.2020.9075873.

[3] K. Souri, *Energy-efficient smart temperature sensors in CMOS technology* (Analog circuits and signal processing.), eng. Cham, Switzerland: Springer, 2018, ISBN: 9783319623078.

[4] LG Global. "Careers". (2023), [Online]. Available: https://globalcareers.lge.com/main (visited on 09/22/2023).

[5] T. C. Carusone, D. Johns, and K. Martin, *Analog integrated circuit design*, eng, 2nd ed. Hoboken, NJ: Wiley, 2012, ISBN: 0-470-77010-4.

[6] M. Rudan *et al.*, *Physics of semiconductor devices*. Springer, 2015.

[7] B. El-Kareh and L. N. Hutter, *Fundamentals of semiconductor processing technology*. Springer Science & Business Media, 2012.

[8] S. Sze, "Physics of semiconductor devices//(book)", *New York, Wiley-Interscience, 1981. 878 p*, 1981.

[9] P. Horowitz, W. Hill, and I. Robinson, *The art of electronics*. Cambridge university press Cambridge, 1989, vol. 2.

[10] Apple. “Apple unleashes m1”. (2020), [Online]. Available: https://www.apple.com/fi/newsroom/2020/11/apple-unleashes-m1/ (visited on 11/19/2022).

[11] Apple. “Apple unveils m1 ultra, the world’s most powerful chip for a personal computer”. (2022), [Online]. Available: https://www.apple.com/newsroom/2022/03/apple-unveils-m1-ultra-the-worlds-most-powerful-chip-for-a-personal-computer/ (visited on 11/19/2022).

[12] The Nobel Prize. “The nobel prize in physics 1956”. (2023), [Online]. Available: https://nobelprize.org/prizes/physics/1956/summary/ (visited on 10/06/2023).

[13] J. Lilienfeld, “Us 1745175a,"” *Method and apparatus for controlling electric current", filed October*, vol. 8, 1926.

[14] N. Holonyak, “The origins of diffused-silicon technology at bell labs, 1954-55”, *The Electrochemical Society Interface*, vol. 16, no. 3, p. 30, 2007.

[15] D. Leblebici and Y. Leblebici, *Fundamentals of high-frequency CMOS analog integrated circuits*. Springer, 2009, vol. 16.

[16] Samsung. “Semiconductor glossary cmos”. (2013), [Online]. Available: https://semiconductor.samsung.com/emea/support/tools-resources/dictionary/semiconductor-glossary-cmos/ (visited on 10/10/2023).

[17] W. Bae, “Cmos inverter as analog circuit: An overview”, *Journal of Low Power Electronics and Applications*, vol. 9, no. 3, p. 26, 2019.

[18] J. Jessing, “Cmos fabrication”, *The VLSI Handbook:*, 2016.

[19] H.-S. P. Wong, K. Akarvardar, D. Antoniadis, *et al.*, “A density metric for semiconductor technology [point of view]”, *Proceedings of the IEEE*, vol. 108, no. 4, pp. 478–482, 2020.

[20] I. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in cmos circuits", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876–884, 2001. DOI: 10.1109/81.933328.

[21] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. McGraw-Hill, Inc., 1987.

[22] K. R. Laker and W. M. Sansen, *Design of analog integrated circuits and systems*. McGraw-Hill New York, 1994, vol. 1.

[23] S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, and G. Baccarani, "An analytical, temperature-dependent model for majority-and minority-carrier mobility in silicon devices", *VLSI Design*, vol. 10, no. 4, pp. 467–483, 2000.

[24] T. W. Kerlin and M. Johnson, *Practical thermocouple thermometry, second edition*, eng, 2nd ed. International Society of Automation (ISA), 2012, ISBN: 9781937560270.

[25] K. Souri, Y. Chae, Y. Ponomarev, and K. A. Makinwa, "A precision dtmost-based temperature sensor", in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, IEEE, 2011, pp. 279–282.

[26] A. Bakker, *High-accuracy cmos smart temperature sensors*, eng, 2000.

[27] J. H. Huijsing, F. R. Riedijk, and G. van der Horn, "Developments in integrated smart sensors", *Sensors and Actuators A: Physical*, vol. 43, no. 1-3, pp. 276–288, 1994.

[28] M. A. Pertijs and J. Huijsing, *Precision temperature sensors in CMOS technology*. Springer Science & Business Media, 2006.

[29] T. Veijola, "Model for thermal spreading impedance in gaas mesfets", in *Proceedings of Third International Conference on Electronics, Circuits, and Systems*, IEEE, vol. 2, 1996, pp. 872–875.

[30] S. Kashmiri and K. Makinwa, "Measuring the thermal diffusivity of cmos chips", in *SENSORS, 2009 IEEE*, IEEE, 2009, pp. 45–48.

[31] K. A. Makinwa and M. F. Snoeij, "A cmos temperature-to-frequency converter with an inaccuracy of less than $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) from $-40\,^{\circ}\mathrm{C}$ to $105\,^{\circ}\mathrm{C}$", *IEEE journal of solid-state circuits*, vol. 41, no. 12, pp. 2992–2997, 2006.

[32] M. Terauchi, A. Hamasaki, and A. Suketa, "Selectable logarithmic/linear response active pixel sensor cell with reduced fixed-pattern-noise based on dynamic threshold mos operation", *Japanese journal of applied physics*, vol. 44, no. 4S, p. 2347, 2005.

[33] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, "A time-to-digital-converter-based cmos smart temperature sensor", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1642–1648, 2005.

[34] G. G. Gielen and R. A. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits", *Proceedings of the IEEE*, vol. 88, no. 12, pp. 1825–1854, 2000.

[35] A. Stevens, *Monte-Carlo simulation : an introduction for engineers and scientists*, eng. Boca Raton, Florida: CRC Press, 2023, ISBN: 1-00-329523-1.

[36] A. Asenov, "Advanced monte carlo techniques in the simulation of cmos devices and circuits", in *International Conference on Numerical Methods and Applications*, Springer, 2010, pp. 41–49.

[37] Synopsys. "What is electronic design automation". (2023), [Online]. Available: `https://www.synopsys.com/glossary/what-is-electronic-design-automation.htm` (visited on 11/05/2023).

[38] Siemens. "Electronic design automation". (2023), [Online]. Available: `https://www.plm.automation.siemens.com/global/en/our-story/glossary/electronic-design-automation-eda/95805` (visited on 11/05/2023).

[39] Synopsys. "Process design kit". (2023), [Online]. Available: `https://www.synopsys.com/glossary/what-is-a-process-design-kit.html` (visited on 11/05/2023).

[40] G. Dupenloup, *Method of accessing the generic netlist created by synopsys design compilier*, US Patent 6,263,483, 2001.

[41] G. Van der Plas, J. Vandenbussche, A. Van den Bosch, M. Steyaert, W. Sansen, and G. Gielen, "Mos transistor mismatch for high accuracy applications", in *Proceedings of the 10th ProRISC/IEEE Workshop*, 1999, pp. 529–534.

[42] M. Shen, J. H. Mikkelsen, K. Zhang, O. K. Jensen, T. Tian, and T. Larsen, "Modeling and design guidelines for guard rings in lightly doped cmos substrates", *IEEE transactions on electron devices*, vol. 60, no. 9, pp. 2854–2861, 2013.

[43] H. Mattausch, A. Yumisaki, N. Sadachika, *et al.*, "Variation analysis of cmos technologies using surface-potential mosfet model", *Journal of Telecommunications and Information Systems*, pp. 37–44, Oct. 2009.