UNIVERSITÀ DEGLI STUDI DI PADOVA

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Analysis and design of a Current-Fed Dual-Half-Bridge Converter

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Abstract

In this thesis the Current-Fed Dual-Half Bridge converter (CFDHB) has been presented and studied under three degrees of freedom. This is an isolated bidirectional converter useful in a lot of applications characterized by sources and/or loads that benefit from a smooth input/output current. A design methodology has been proposed which reduces the RMS current in all devices and guarantees the soft commutations of all switches in a wide range of operating points. Finally, simulations and experimental verifications complete the work.

Contents

Chapter 1

Introduction

Energy transition to a zero-carbon-emission-based economy is one of the most driving force toward transport electrification, and power electronics will be the leading technology in this energy transition. The electric vehicles (EVs) ecosystem has been improved in every aspect, from the reduction of the charging time, by increasing the power levels, to the evolution of the battery technologies, indeed they show performance enhancements and cost reductions [1], [2].

As often happen for any growing technology, new opportunities appear, which can make the adoption of EVs more interesting and cost-effective for the users. One interesting and growing aspect is the integration/interaction of EVs with the grid, different integration levels are possible, as represented in Fig.1.1. EVs will become able to exchange energy with the grid and so they will play new roles in the future, enabling technologies from the simplest vehicle-to-home (V2H), vehicle-to-vehicle (V2V) up to, the most complex, vehicle-to-grid (V2G). This kind of vehicles will be called gridable EVs (GEVs) [3]. This new technologies will create a lot of new opportunities, from which both the grid and the users can benefit, some examples for the V2H: acts as a home backup generator and sells excess energy back to the grid at high priced peak time. The V2G system can provides: energy sources for ancillary services, distributed storages as well as reactive power support [3]. Considering the simplest V2H technology, an house should handle with a single (or few) EV, the main objective is to sustain/cooperate with the house, and then provides other services, if necessary. For this reason, a relative small On-Board or Off-Board charger, sized for about the house rated power (3.3 kW in Italy), can be enough for this user. A possible network can be the one proposed in Fig.1.2, where the key elements, which enable this interaction, are the bidirectional converters, supervised by a Home Control system. As can be seen

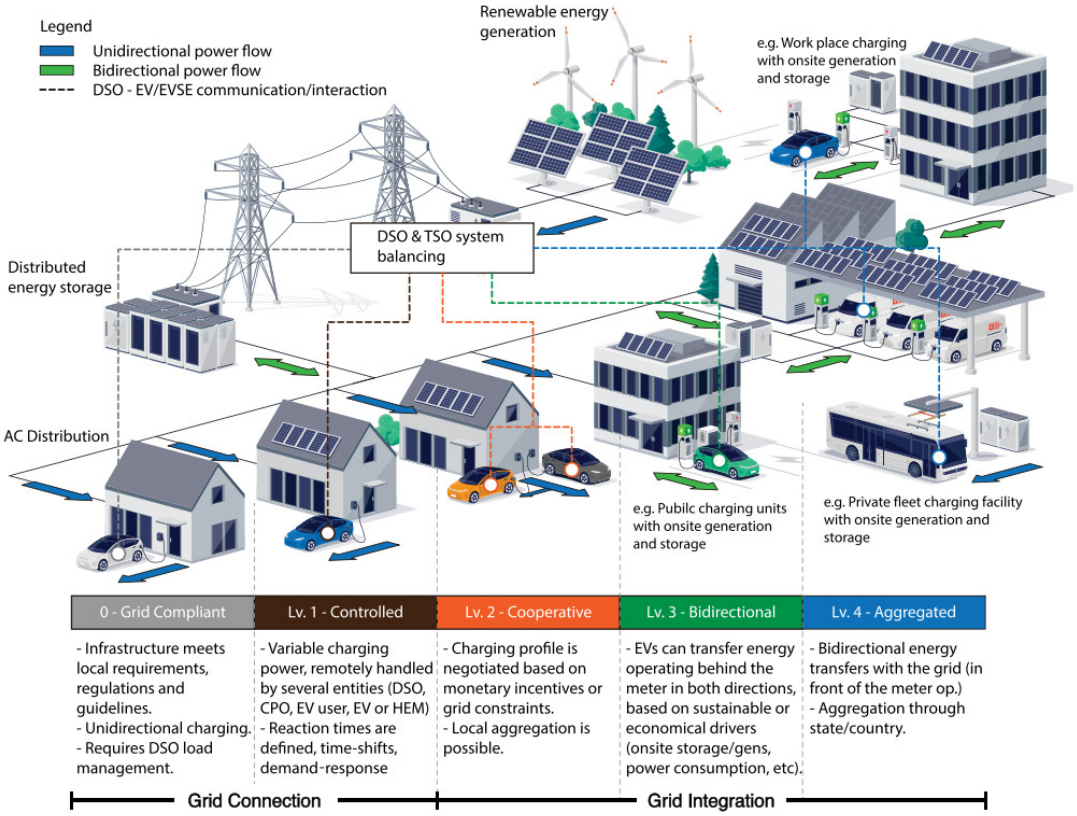


Figure 1.1: Different level for grid integration of EVs, from [1]. EVSE: EV Supply Equipment, DSO: Distributor System Operator, TSO: Transmission System Operator.

in Fig1.2, power electronics are at any level in order to exchange power between GEVs and home/community grid. In particular, develop and study bidirectional converters can help this new technology.

In a scenario in which batteries will be more and more used, their variable voltage levels require converters that work in a wide input range. One possible topology is the CFDHB in Fig.2.1, which has an intrinsic boost effect useful with variable voltage sources. Moreover, it offers bidirectional power flow and galvanic isolation. Several studies have been published on the topology, for example, the connection with batteries under 50% duty cycle on each switching leg, has been discussed in [4]. The connection with super capacitors, which have variable voltage levels and they require bidirectional power capability, has been discussed in [5] and [6]. On both cases the duty cycles have been assumed equal on the two switching legs, but different from 50%. Another interesting work is proposed in [7], which makes a lot of effort to control the current managed by the converter. So this topology seems a good candidate to work with variable voltage sources, and it can be integrated into the V2H network, as highlighted in Fig.1.2. One drawback

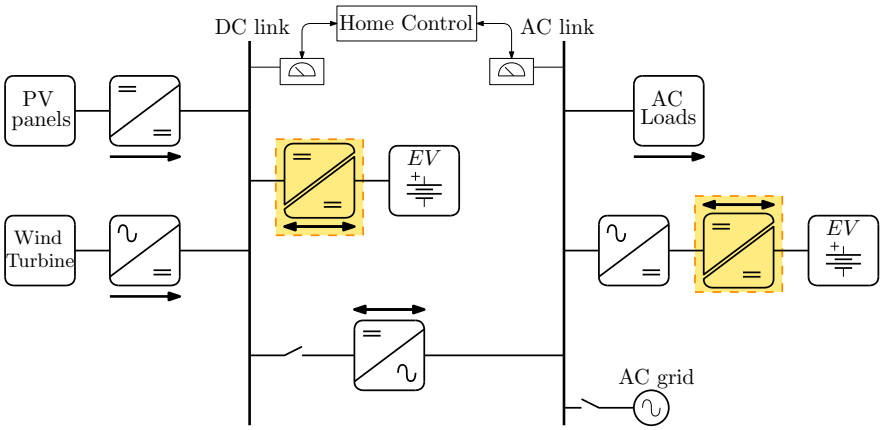


Figure 1.2: Possible network for V2H system, inspired by [3]. Arrows specify the power flow directions. The highlighted blocks represent the application of the converter herein.

is the presence of the capacitors of the half-bridge configuration. Indeed, all the current passes through the Equivalent-Series-Resistance (ESR) of that capacitors and this affects the efficiency. But this problem can be compensated using parallel converter connections, in a modular design, and/or using a considerable number of parallel capacitors to reduce the ESR.

This work wants to investigate deeper this topology studying the three available degrees of freedom in Ch.2, a design methodology will be proposed in Ch.3, the magnetic components will be designed in detail in Ch.4, simulations and experimental validations will be presented in Ch.5 and Ch.6 respectively, and finally a small improvement will be discussed in Ch.7.

Chapter 2

CFDHB analysis

In this chapter the Current-Fed Dual-Half-Bridge topology, represented in Fig.2.1, will be introduced and analyzed under steady-sate operation. At the end, the conditions for Zero-Voltage Switching (ZVS) will be discussed.

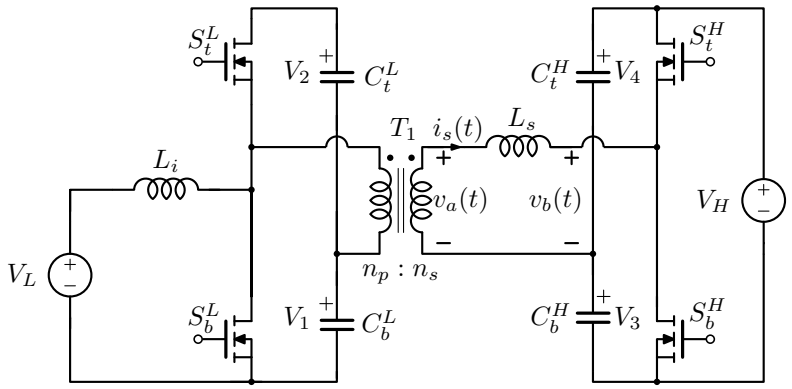


Figure 2.1: Current-Fed Dual-Half-Bridge converter scheme.

Current and voltage expressions will be reported in normalized form using the following base quantities:

- *Base time:* $T_N = T_s = 1/f_s$ (f_s is the switching frequency)
- *Base voltage:* $V_N = V_H$
- *Base impedance:* $X_N = 2\pi f_s L_s$
- *Base current:* $I_N = V_N/X_N$
- *Base power:* $P_N = V_N^2/X_N$
- *Normalized voltage:* $u_x = v_x/V_N$

- *Normalized current:* $j_x = i_x/I_N$
- *Normalized power:* $\Pi_x = P_x/P_N$

2.1 Steady-state analysis

This topology integrates a Boost cell into the left half bridge, which is driven by the duty-cycle D_b, corresponding to the low-side device. The sum of the voltages on the two capacitors, C_b^L and C_t^L, is related to the Boost voltage gain:

$$V_B = V_1 + V_2 = \frac{V_L}{1 - D_b} \tag{2.1}$$

From the volt-second balance of inductors L_i and L_μ, which is the magnetizing inductance of the transformer T_1, it's possible to obtain the voltages on the two capacitors on the current-fed side, which are reported in Tab.2.1.

The voltage-fed side is driven by the duty-cycle D_h, which corresponds to the low-side device, and using again the volt-second balance it's possible to obtain the voltages on the capacitors C_b^H and C_t^H, which are reported in Tab.2.1.

$\mathbf{V_1}$	$\mathbf{V_2}$	$\mathbf{V_3}$	$\mathbf{V_4}$
V_L	$V_L \frac{D_b}{1-D_b}$	$V_H(1 - D_h)$	$V_H D_h$

Table 2.1: Average capacitor voltages.

The analysis of this converter considers three degrees of freedom, namely:

1. Duty-cycle on the current-fed side (D_b);
2. Duty-cycle on the voltage-fed side (D_h);
3. Phase shift between the two control signals (D_ϕ).

The circuit can be analyzed under some simplifying hypothesis, which allow to understand the basic behaviour of the converter: the voltages on the capacitors will be considered constant during the switching period, this brings piece-wise linear current into L_s. In this way it's possible to simplify the analysis considering the equivalent circuit reported in Fig.2.2.

Due to the presence of the capacitors C_b^L, C_t^L, C_b^H and C_t^H the charge-balance imposes that the average current through L_s is equal to zero, namely $\bar{i_s}(t) = 0$.

This is one advantage of an Half-Bridge topology, indeed the absence of DC component of transformer magnetizing current reduces the losses and the possibility of core saturation.

In Fig.2.3 it's possible to see some generic waveforms including the switches' commands, which will be excluded hereafter. Further it's possible to see an example of the phase shift, which is defined as the distance between the midpoints of D_b and D_h. In particular, D_ϕ is positive if D_b leads D_h, and a positive phase-shift means a positive power-flow from V_L to V_H source. For this preliminary analysis the dead-time will be neglected.

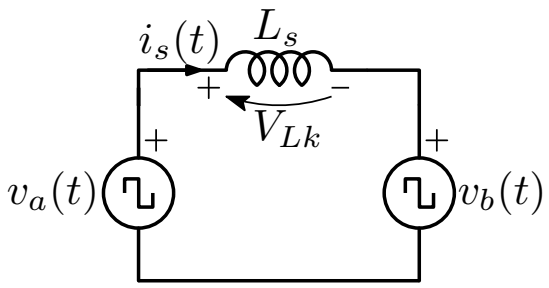


Figure 2.2: Equivalent circuit for the inductor current analysis, referred to the secondary side of the transformer.

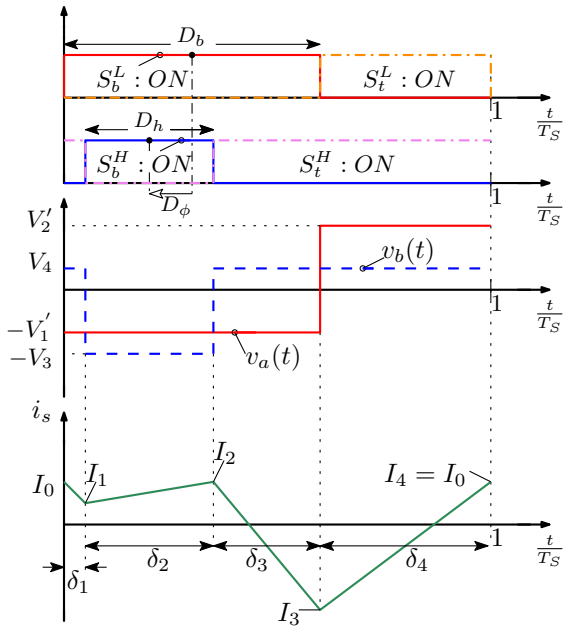
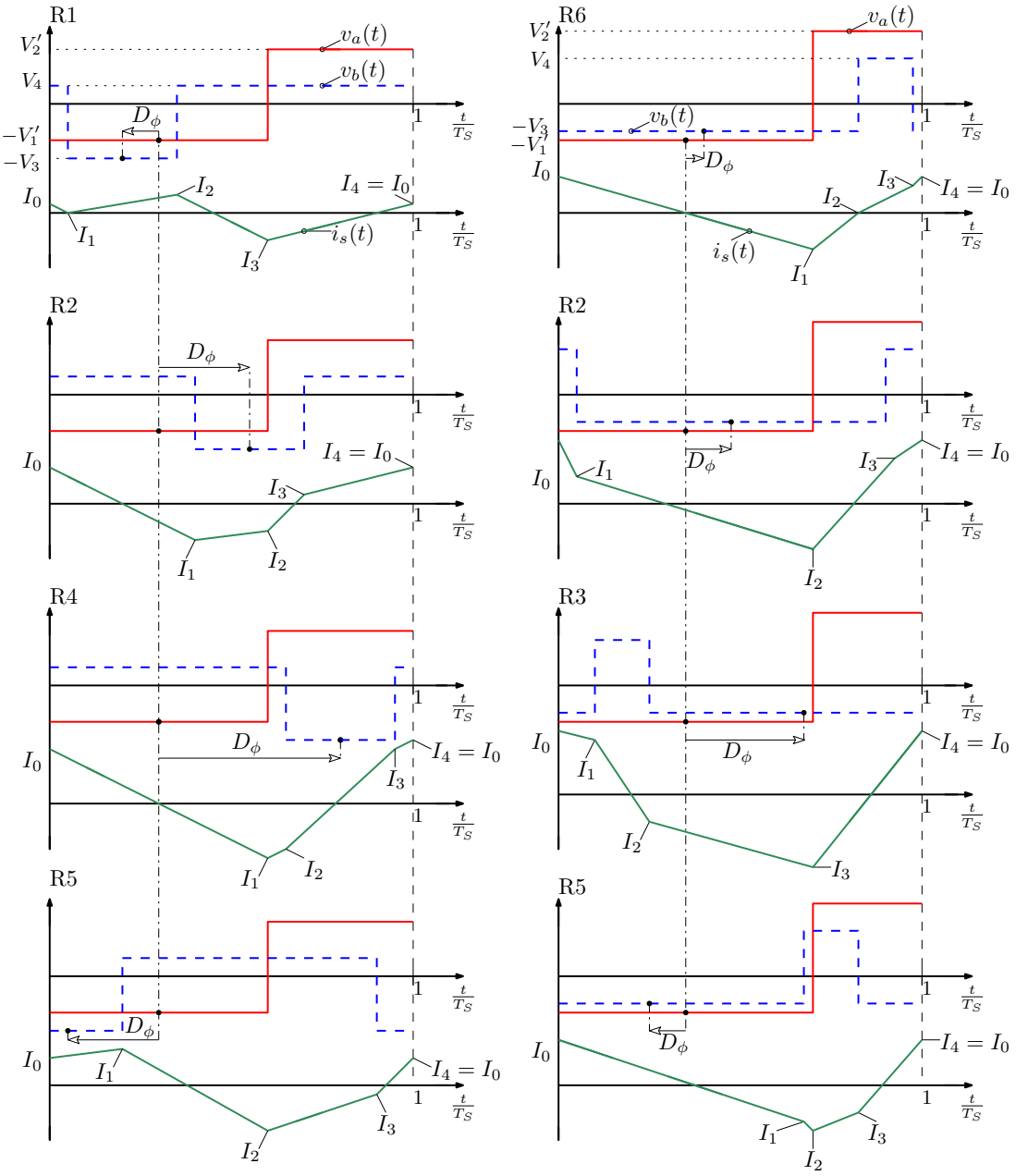


Figure 2.3: Generic waveforms including the switches' commands.

The converter can operate in six different regions and an example of waveforms in each region is depicted in Fig.2.4, while the boundary conditions are reported in Fig.2.5.



(a) $D_h < D_b = D_{b1}$

(b) $D_h > D_b = D_{b2}$

Figure 2.4: Main waveforms for different D_ϕ, D_b, D_h. R_i denotes the operating region.

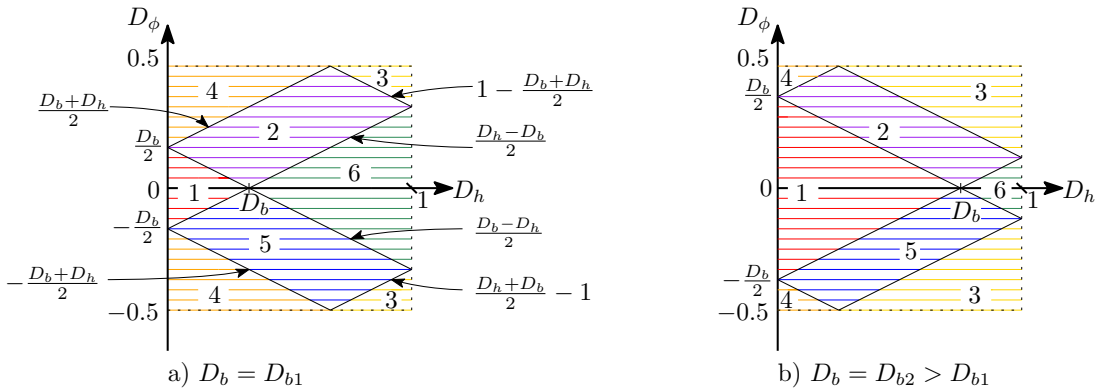


Figure 2.5: Operating regions boundaries for different values of D_b.

Region	**R1**	**R2**	**R3**
$\delta_1 = \frac{\Delta t_1}{T_s}$	$\frac{D_b-D_h}{2} + D_\phi$	$\frac{D_b-D_h}{2} + D_\phi$	$\frac{D_b+D_h}{2} + D_\phi - \frac{1+sgn(D_\phi)}{2}$
$\delta_2 = \frac{\Delta t_2}{T_s}$	D_h	$\frac{D_b+D_h}{2} - D_\phi$	$1 - D_h$
$\delta_3 = \frac{\Delta t_3}{T_s}$	$\frac{D_b-D_h}{2} - D_\phi$	$\frac{D_h-D_b}{2} + D_\phi$	$\frac{D_b+D_h}{2} - D_\phi + \frac{1-sgn(D_\phi)}{2}$

Table 2.2: Normalized sub-intervals duration for R1-R3 operating regions.

Each switching period can be divided into 4 sub-intervals: $\Delta t_k, k = 1, 2, 3, 4$, and the duration of each can be calculated using Tab.2.2 and Tab.2.3. The voltages applied to L_s in each sub-interval are reported in Tab.2.4.

At this point it's possible to calculate J_0, namely the current through L_s at the beginning of the switching period in normalized form. The derivation is explained in App.C.1, while the result is reported in the following expression:

$$J_0 = -\pi\big[U_{L1}\delta_1(1+\delta_2+\delta_3) + U_{L2}\delta_2(1-\delta_1+\delta_3) + U_{L3}\delta_3(1-\delta_1-\delta_2)\big], \quad (2.2)$$

where $J_4 = J_0$ and $\bar{j_s}(t) = 0$ have been used to obtain it.

Knowing J_0 it's possible to find the initial current, in normalized form, for

Region	**R4**	**R5**	**R6**
$\delta_1 = \frac{\Delta t_1}{T_s}$	D_b	$\frac{D_b+D_h}{2} + D_\phi - 1$	D_b
$\delta_2 = \frac{\Delta t_2}{T_s}$	$D_\phi + \frac{1-sgn(D_\phi)}{2} - \frac{D_b+D_h}{2}$	$1 - D_\phi + \frac{D_b-D_h}{2}$	$\frac{D_h-D_b}{2} + D_\phi$
$\delta_3 = \frac{\Delta t_3}{T_s}$	D_h	$D_\phi - \frac{D_b+D_h}{2}$	$1 - D_h$

Table 2.3: Normalized sub-intervals duration for R4-R6 operating regions.

Region	$V_{L1} = U_{L1}V_N$	$V_{L2} = U_{L2}V_N$	$V_{L3} = U_{L3}V_N$	$V_{L4} = U_{L4}V_N$
R1	$-V_1 n - V_4$	$-V_1 n + V_3$	$-V_1 n - V_4$	$V_2 n - V_4$
R2	$-V_1 n - V_4$	$-V_1 n + V_3$	$V_2 n + V_3$	$V_2 n - V_4$
R3	$-V_1 n + V_3$	$-V_1 n - V_4$	$-V_1 n + V_3$	$V_2 n + V_3$
R4	$-V_1 n - V_4$	$V_2 n - V_4$	$V_2 n + V_3$	$V_2 n - V_4$
R5	$-V_1 n + V_3$	$-V_1 n - V_4$	$V_2 n - V4$	$V_2 n + V_3$
R6	$-V_1 n + V_3$	$V_2 n + V_3$	$V_2 n - V_4$	$V_2 n + V_3$

Table 2.4: Voltage on L_s for each sub-interval, $n = n_s/n_p$, $V_{Lk} = V_{Ak} - V_{Bk}, k = 1, 2, 3, 4$.

each sub-interval easily:

$$J_k = J_{k-1} + 2\pi U_{Lk}\delta_k \quad k = 1, 2, 3, 4. \tag{2.3}$$

The normalized RMS current can be calculated using the following expression:

$$J_{RMS} = \sqrt{\sum_{k=1}^{4} \delta_k \Big[(J_{k-1})^2 + 2\pi J_{k-1} U_{Lk}\delta_k + \frac{4}{3}\pi^2 \delta_k^2 U_{Lk}^2 \Big]}. \tag{2.4}$$

The transferred active power can be calculated using (2.5) and the equivalent circuit in Fig.2.2, which will be considered positive if transferred from source A to source B.

$$P_A = f_s \int_0^{T_s} v_a(t) i_s(t) dt = f_s \sum_{k=1}^{4} V_{Ak} \frac{\Delta t_k}{2} (I_{k-1} + I_k) \tag{2.5}$$

The expressions for the active power in all the six operating regions have a common structure, namely: a constant factor times a function of D_b, D_h, D_ϕ. So the general expression, in normalized form, is reported here:

$$\Pi_{Ar} = n\pi U_L f_r(D_b, D_h, D_\phi) \;\; r = 1, 2, 3, 4, 5, 6, \tag{2.6}$$

where r denotes the corresponding operating region. The proper expressions of f_r are reported in Tab.2.5, they are general and cover all the cases. Indeed, they bring to the equations reported in [4] and [8], using the same hypothesis of the papers. At this point it's possible to plot the variation of the normalized power flow for different operating regions, depicted in Fig.2.6, where it's clear

Region	$f_r(D_b, D_h, D_\phi)$
R1	$2D_hD_\phi$
R2	$\frac{2D_\phi D_b(1-D_h)-(D_\phi+(D_b-D_h)/2)^2}{1-D_b}$
R3	$(1-D_h)(1-2D_\phi)$
R4	$\frac{D_bD_h(1-2D_\phi)}{1-D_b}$
R5	$\frac{(D_\phi+(D_b+D_h)/2)^2-D_bD_h(1+2D_\phi)}{1-D_b}$
R6	$\frac{2D_\phi D_b(1-D_h)}{1-D_b}$

Table 2.5: Expressions of f_r in all the six operating regions. R1 derivation in App.C.2.

that the power variation is symmetric with respect to D_ϕ, so its sign determines the direction of the power. The power flow together with the RMS current trends can be seen in Fig.2.7, for some specific operating points. From it can be seen that the derivative of the power with respect to D_Φ is positive, until a certain limit, after which it becomes negative. It's very important to known this limit, indeed, if the phase shift will be used as a control variable, the feedback loop can become unstable when the derivative changes sign. Each operating point has its limit, so Fig.2.8 reports the power peaks and the corresponding phase shifts considering two modulations: $D_b \neq D_h$ and $D_b = D_h$. An example can be useful to clarify this concept. Let's consider the following specific case: $D_b = 0.2$, $D_h = 0.5$; the power peak is reached with $D_\Phi = 0.25$, as can be seen in Fig.2.7 and Fig.2.8, going beyond that limit is not feasible since the controller will become unstable. From Fig.2.8 other considerations can be made:

- the power capability of the converter increases with D_b;
- a three degrees of freedom control allows to reach higher transferred power levels with respect to a simpler two degrees.

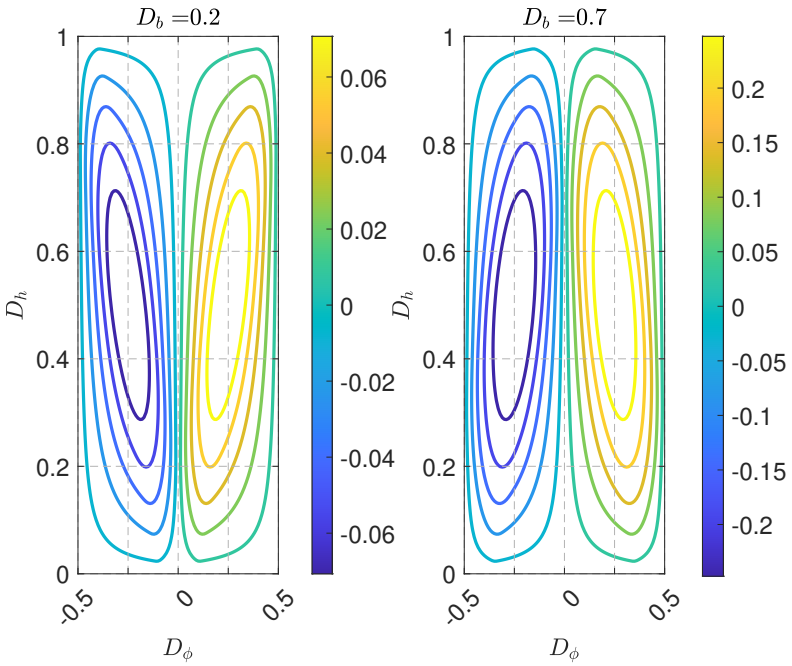


Figure 2.6: Normalized power flow for different D_b, D_h, D_ϕ. $U_L = 1$, $n = 0.55$. The color bar represents normalized power: Π_{Ar}.

2.2 ZVS analysis

In order to reduce the losses due to an hard-switching commutation, it's important to understand which are the operating points that can satisfy the ZVS conditions. In general, it's possible to achieve a zero voltage turn on if, during the dead time, an impressed current discharges the MOSFET output capacitances (C_{oss}), turning on the body diode of the correct switch. It's not easy to study the conditions to achieve this, in particular due to the strong non-linearity of the C_{oss}. There are a lot of articles on this topic, such as [6], [9], and one problem is to have a right estimation of the C_{oss} or better, the quantity of charge to be moved in order to discharge that capacitance.

In order to write some qualitative conditions to achieve ZVS, in this study a constant current will be considered during the dead time, which discharges linearly an equivalent capacitance (2.7), that stores the same amount of charge of the non linear one at V_{DC}. A threshold current (I_{ZVS}) will be considered as the limit between an hard and a soft commutation.

$$C_{Q,eq}(V_{DC}) = \frac{\int_0^{V_{DC}} C_{oss}(v)dv}{V_{DC}} \tag{2.7}$$

Let's start with the voltage-fed side. The simplified schematic of Fig.2.9

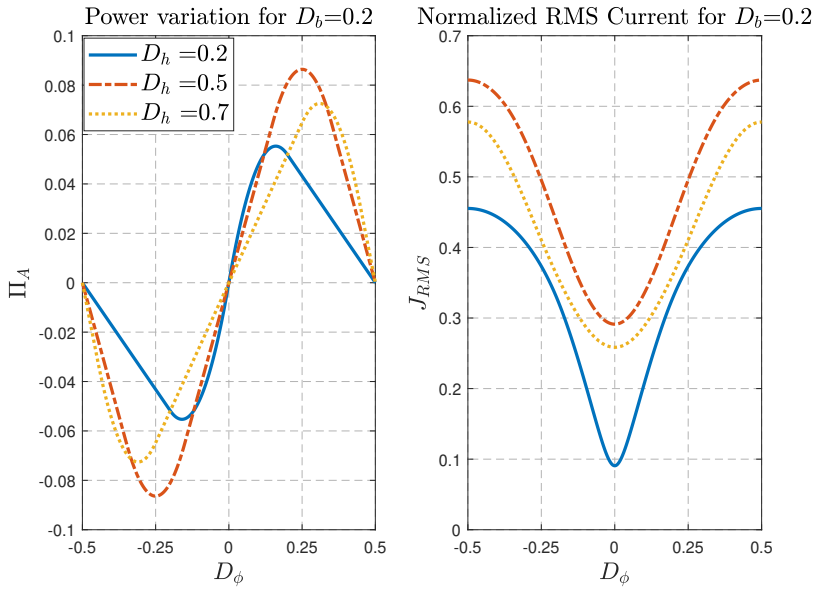


Figure 2.7: An example of normalized power flow and normalized RMS current for some specific values of D_b and D_h, $U_L = 1$, $n = 0.55$.

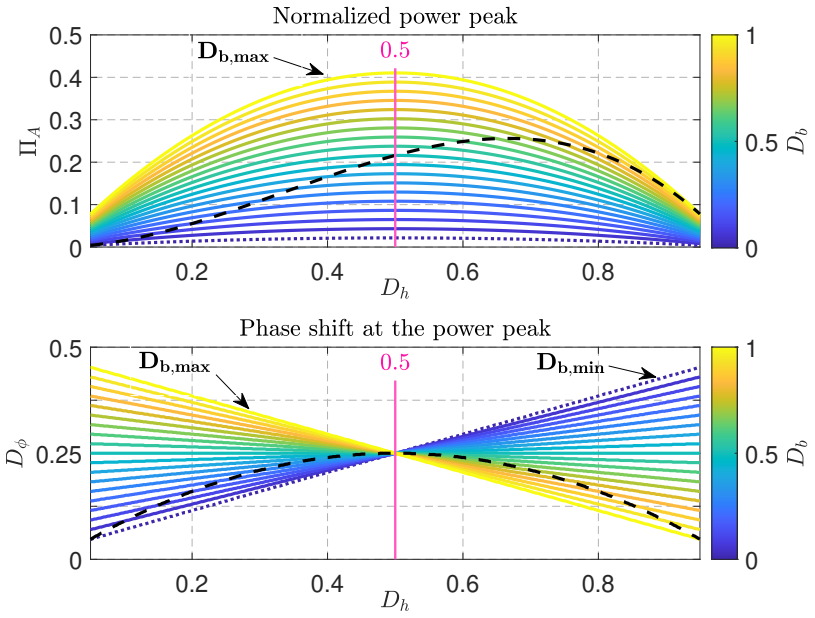


Figure 2.8: Power peaks behaviour and corresponding phase shifts with $U_L = 1$ and $n = 0.55$. The dashed line represents the power peaks for $D_b = D_h$.

represents the situation during the dead time. The two switches are off and an equivalent current generator, which represents the inductor L_s, injects a current into the node N_H. Depending on the operating region the current value involved in the transient is different and the specific values are reported in Tab.2.6.

The situation on the current-fed side is more complex since there are two

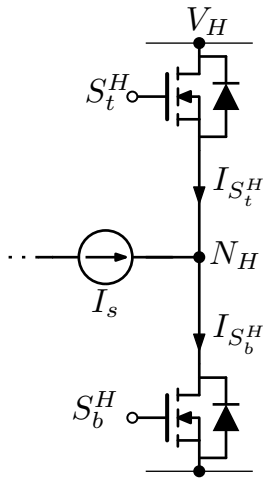


Figure 2.9: Simplified schematic of the voltage-fed leg during the dead time.

	R1	**R2**	**R3**	**R4**	**R5**	**R6**
$I_{S_t^H}$	$-I_2$	$-I_3$	$-I_1$	$-I_3$	$-I_1$	$-I_2$
$I_{S_b^H}$	I_1	I_1	I_2	I_2	I_3	I_3

Table 2.6: ZVS conditions for the voltage-fed leg for all operating regions, $I_{S_t^H} < -I_{ZVS}$ and $I_{S_b^H} < -I_{ZVS}$. By assuming that at t=0 s, S_b^L turns on, which corresponds to the current values I_0, as can be seen in Fig.2.4.

current generators involved. One represents the input inductance (L_i) and the other the current from the transformer (T_1). The situation is represented in Fig.2.10. Using the Kirchhoff current law on the N_L node, it's possible to write the conditions that allow the zero-voltage turn on of S_b^L (2.8) and S_t^L (2.9).

$$I_{S_b^L} = I_{IN} - I_{T1} < -I_{ZVS} \tag{2.8}$$

$$I_{S_t^L} = I_{T1} - I_{IN} < -I_{ZVS} \tag{2.9}$$

	R1	**R2**	**R3**
$I_{S_t^L}$	$I_3^{'} - I_{IN}(D_b T_s)$	$I_2^{'} - I_{IN}(D_b T_s)$	$I_3^{'} - I_{IN}(D_b T_s)$
$I_{S_b^L}$	$I_{IN}(0) - I_0^{'}$	$I_{IN}(0) - I_0^{'}$	$I_{IN}(0) - I_0^{'}$

Table 2.7: ZVS turn on conditions for the current-fed leg for R1-R3 regions, $I_{S_t^L} < -I_{ZVS}$ and $I_{S_b^L} < -I_{ZVS}$. Note that $I_k^{'} = nI_k$, $k = 0, 1, 2, 3$, is the initial current for each sub-interval at the primary side of T_1. By assuming that at t=0 s, S_b^L turns on, which corresponds to the current values I_0, as can be seen in Fig.2.4.

Also in this case, depending on the operating region, the current value in-

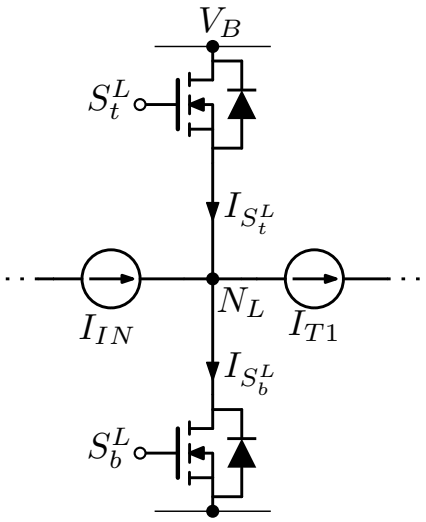


Figure 2.10: Simplified schematic of the current-fed leg during the dead time.

	R4	**R5**	**R6**
$I_{S_t^L}$	$I_1^{'} - I_{IN}(D_b T_s)$	$I_2^{'} - I_{IN}(D_b T_s)$	$I_1^{'} - I_{IN}(D_b T_s)$
$I_{S_b^L}$	$I_{IN}(0) - I_0^{'}$	$I_{IN}(0) - I_0^{'}$	$I_{IN}(0) - I_0^{'}$

Table 2.8: ZVS turn on conditions for the current-fed leg for R4-R6 regions, $I_{S_t^L} < -I_{ZVS}$ and $I_{S_b^L} < -I_{ZVS}$. Note that $I_k^{'} = nI_k$, $k = 0, 1, 2, 3$, is the initial current for each sub-interval at the primary side of T_1. By assuming that at t=0 s, S_b^L turns on, which corresponds to the current values I_0, as can be seen in Fig.2.4.

volved in the transient is different and the specific values are reported in Tab.2.7 and Tab.2.8.

Chapter 3

Design guidelines

In this chapter the CFDHB topology will be designed according to the specifications reported in the following table:

Parameter	Symbol	Value
Current-fed side voltage	V_L	$250 - 500\,V$
Voltage-fed side voltage	V_H	$400\,V$
Nominal output power	P_O	$2.5\,\mathrm{kW}$

Table 3.1: Converter specifications.

3.1 Design guidelines

A current-fed topology has the ability to boost the input voltage and this can be useful in a wide input range converter, like this. In order to use 1200 V devices the duty cycle on the Boost side has a maximum value, which depends on the input voltage. Including 25% of margin, it's possible to write (3.1), which brings the maximum values of D_b expressed in (3.2).

$$V_B = V_1 + V_2 = \frac{V_L}{1 - D_b} < 900\,\mathrm{V} \tag{3.1}$$

$$\begin{cases} D_b < 0.72 \text{ with } V_L = V_{Lmin} \\ D_b < 0.44 \text{ with } V_L = V_{Lmax} \end{cases} \tag{3.2}$$

In references it's reported that trapezoidal current ensures better performances since reduces the RMS current and increases the ZVS range [4], [6]–[8]. For these reasons this design will be done with the goal to achieve it. An

example of trapezoidal current can be seen in Fig.3.1, based on the conditions reported here:

$$\begin{cases} nV_1 = V_3 \\ nV_2 = V_4. \end{cases} \tag{3.3}$$

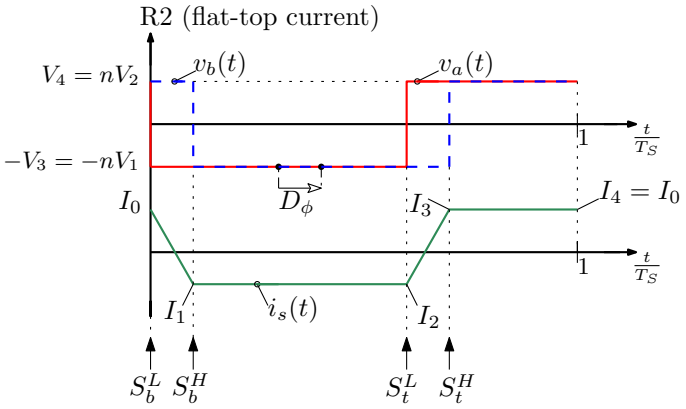


Figure 3.1: An example of trapezoidal current in region R2. Arrows specify the turn on instant of the corresponding switch.

Conditions (3.3) can be satisfied if:

$$D_b = D_h = D = 1 - \frac{nV_L}{V_H}, \tag{3.4}$$

which imposes the same duty-cycle on the two legs, thus only the phase shift will be used to control the transferred power.

Using the flat-top condition (3.4) into (3.2), a range of possible transformer turns ratio appears and in this case results: $0.45 < n < 0.8$.

Considering a positive transferred power, namely $D_\phi > 0$ and (3.4), the converter works in region R2 until a certain $D_\phi = \min\big[D, 1-D\big]$. Under these hypotheses, the normalized transferred power can be computed using the following expression:

$$\Pi_{A2} = n\pi U_L f_2(D_b, D_h, D_\phi) = n\pi U_L \frac{2D_\phi D(1-D) - D_\phi^2}{1-D}. \tag{3.5}$$

Now it's possible to plot the variation of the normalized power in region R2, which is reported in Fig.3.2. It shows that the power capability doesn't vary monotonically with a variation of input voltage, as reported in [6]. Studying the derivative of (3.5), it's possible to find the phase shift that brings the maximum

power point, as reported in the following:

$$\frac{\partial \Pi_{A2}}{\partial D_\phi} = \frac{2n\pi U_L}{1-D}(D(1-D) - D_\phi) = 0, \tag{3.6}$$

$D_\phi = D(1-D)$ is the solution, which is a maximum, as can be deduced looking at the sign of the derivative. Another important information is $U_{L_{peak}} = \frac{1}{2n}$, which brings the highest power transfer. It can create problems with the control requiring low phase shift, as will be discussed. A maximum exists since the power capability increases with U_L, and then decreases as can be seen in Fig.3.2. This can be found looking at the power peaks ($\hat{\Pi}_{A2}$) using (3.4) and the solution of (3.6) into (3.5), and searching the maximum, as reported in the following:

$$\frac{\partial \hat{\Pi}_{A2}}{\partial U_L} = 2\pi n^2(2n^2U_L^3 - 3nU_L^2 + U_L) = 0. \tag{3.7}$$

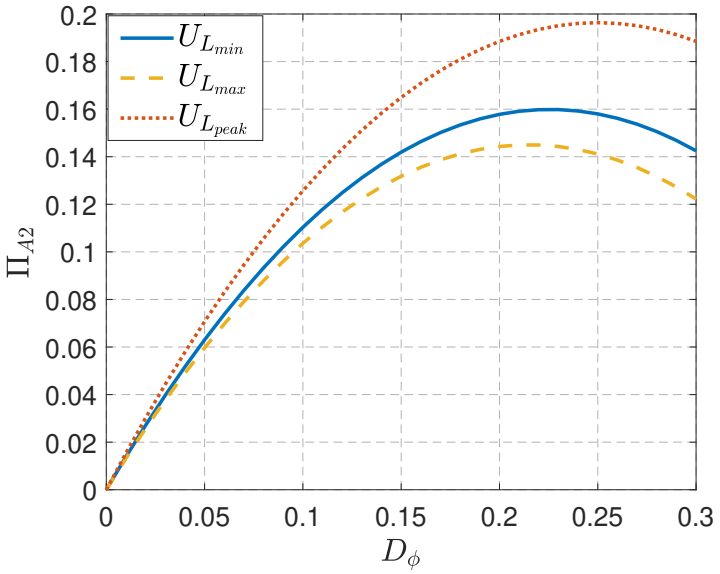


Figure 3.2: Normalized power in region R2 calculated using $n = 0.55$.

The transformer turns ratio influences the power capability and should be chosen carefully. A right value for n should guarantee a reasonable phase shift, not too small, to reach the nominal output power (P_O), in order to have better controllability of the converter. Fig.3.3 shows the variation of the power peaks as a function of the transformer turns ratio. A good value of n can be the one which guarantees similar peaks for any operating point. For this specific case, the condition is satisfied around the value $n = 0.533$, where there is the cross point between the curves. Let's select $n = 0.55$.

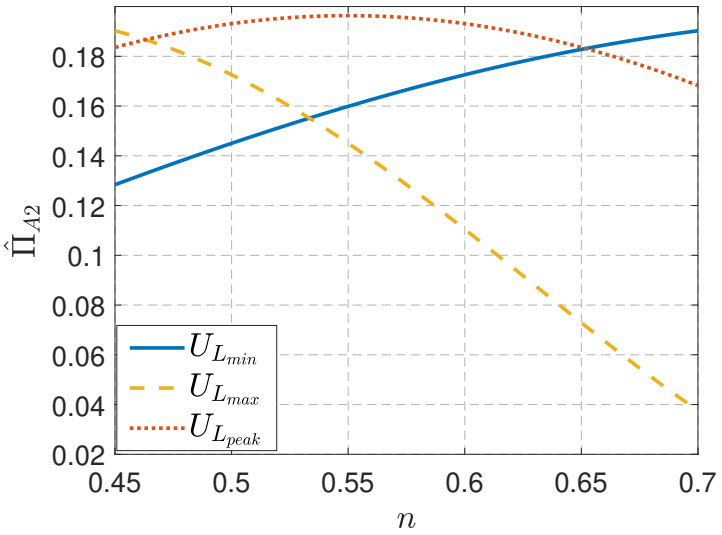


Figure 3.3: Normalized power peak for different transformer turns ratio, n. For each n the right value of D and then $\hat{D}_\Phi$ has been calculated.

In order to guarantee a good controllability it's necessary to impose a minimum phase shift ($D_{\Phi min}$) at nominal output power, for any operating point. If the transformer turns ratio has been selected such that the power peaks are close, it's easier to satisfy this constraint. The correct value for L_s can be found imposing the following conditions:

1. the power peak (Π_a), of the operating point which has the lowest one, must be greater than P_O, for this specific design $U_L = 1.25$ has the lowest power peak: Π_a=0.145 in normalized form;

2. the power value (Π_b), of the operating point which has the highest one at $D_{\Phi min}$, must be smaller than P_O, for this specific design and considering $D_{\Phi min} = 0.1$, $U_{L_{peak}} = 0.909$ has the highest power value: Π_b=0.126 in normalized form.

Using the values reported above it's possible to find a proper value for L_s, by solving the inequalities reported here:

$$\begin{cases} \Pi_a P_N > P_O \\ \Pi_b P_N < P_O. \end{cases} \tag{3.8}$$

For this design (3.8) can be satisfied with L_s in the following range:

$$6.42\,\mu\text{H} \leq L_s \leq 7.38\,\mu\text{H}, \tag{3.9}$$

considering $P_O = 2.5\,\text{kW}$. At this point it's possible to select the proper value looking at how the impedance X_{Ls} influences the RMS current, which is reported in Fig.3.4. It's possible to see that the RMS current increases with X_{Ls}, thus it's better to select a value near the lower side. For this reason, let's select $L_s = 6.5\,\mu\text{H}$.

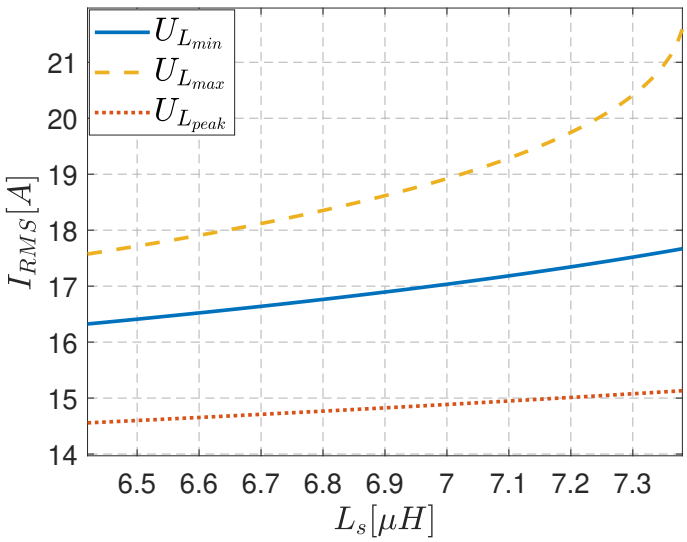


Figure 3.4: RMS Current vs L_s value at nominal output power: 2.5 kW. Note: For each value of L_s and U_L the correct value of D and D_Φ have been selected to reach the desired power.

Finally Fig.3.5 summarises the main converter behaviour for this specific design.

3.2 ZVS Operation

Considering the flat-top condition in region R2, it's possible to find the expressions for the currents at the switching instants at the secondary side:

$$I_0 = I_3 = \frac{V_H D_\phi D}{L_s f_s}, \tag{3.10}$$

$$I_1 = I_2 = -\frac{V_H D_\phi}{L_s f_s}(1 - D), \tag{3.11}$$

where $D = 1 - nU_L$.

In order to satisfy the ZVS conditions for S_t^H, I_3 should be positive and looking at (3.10) it's verified; for the S_b^H switch I_1 should be always negative, and looking to (3.11) it's verified. So the ZVS are always possible for the switches

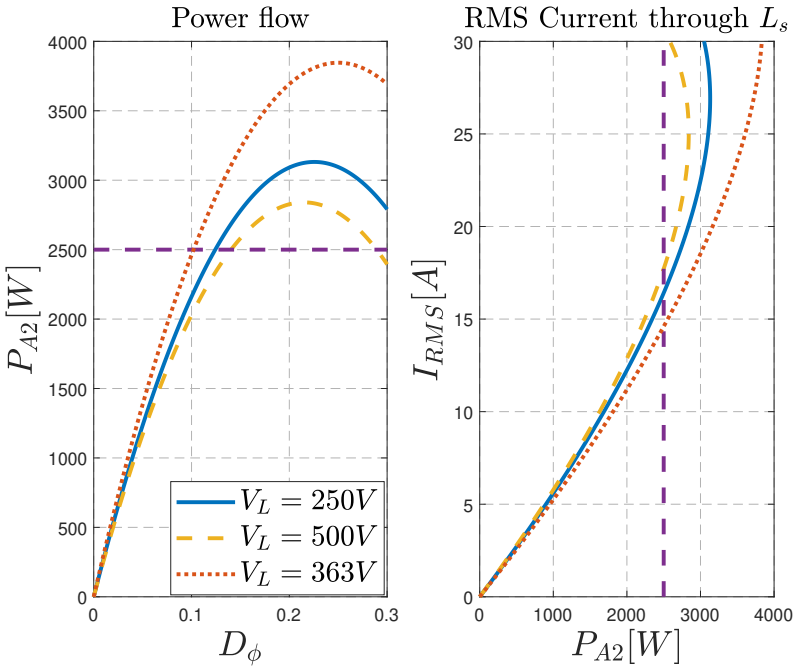


Figure 3.5: Converter power flow and RMS current through L_s vs D_ϕ for different V_L. Note that V_L = 363 V corresponds to the point which has the highest power transfer for this design.

on the voltage-fed side, considering a threshold current of 0A. But imposing a minimum current value, the ZVS cannot be always achieved, for example at light load.

The current-fed side can be analyzed considering the circuit reported in Fig.3.6. Since S_b^L turns on at t=0 s, the ZVS can be achieved if the current

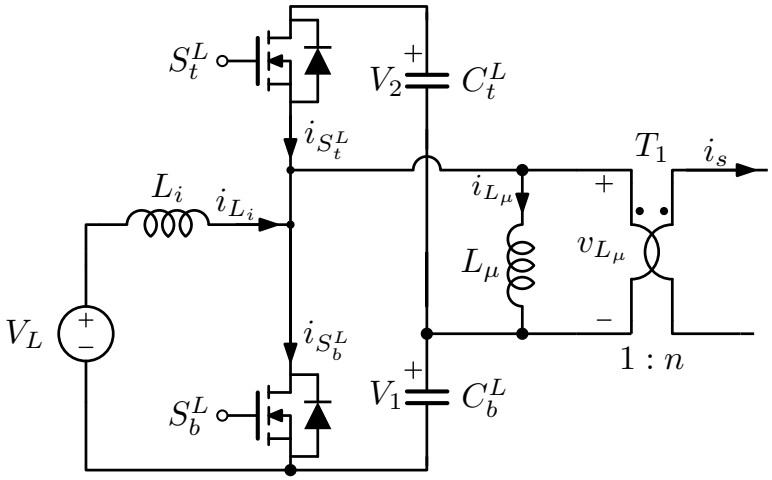


Figure 3.6: Circuit for ZVS analysis on the current-fed side.

$i_{S_b^L}(0)$ is negative during the dead time. Considering S_t^L OFF, the current into the bottom switch can be calculated using Kirchhoff current law:

$$i_{S_b^L}(t) = i_{L_i}(t) - ni_s(t) - i_{L_\mu}(t). \tag{3.12}$$

The current through L_i can be calculated considering $\eta = 1$ to obtain the average value, and then superimposing a linear variation. This method can be used also with L_μ but considering an average value of 0A. An example of current waveforms in region R2 can be seen in Fig.3.7. So at t=0 s, $i_{S_b^L}(t)$ should be negative, but a threshold of 0 A it's not sufficient to achieve a proper ZVS, so a minimum current has been introduced:

$$i_{L_i}(0) - ni_s(0) - i_{L_\mu}(0) < -I_{ZVS}. \tag{3.13}$$

The current through the input inductance at t=0 s is (3.14), while in the magnetizing inductance is (3.15).

$$i_{L_i}(0) = I_{L_i,min} = \frac{P_{A2}}{V_L} - \frac{V_L D}{2L_i f_s} \tag{3.14}$$

$$i_{L_\mu}(0) = \hat{I}_{L_\mu} = \frac{V_L D}{2L_\mu f_s} \tag{3.15}$$

Looking at (3.13) and Fig.3.7, it can be seen that $i_{L_\mu}(0)$ helps the ZVS turn on, so the magnetizing current will be neglected in order to compute L_i. At this point combining (3.4), (3.10) and (3.14), it's possible to find the maximum L_i value to achieve ZVS for S_b^L:

$$\frac{1}{L_i} > \frac{1}{D}\left(\frac{2I_{ZVS}f_s}{V_L} - \frac{D_\phi^2}{U_L^2 L_s}\right), \tag{3.16}$$

note that the effect of i_{L_μ} can be taken into account considering a lower value for the I_{ZVS}.

The ZVS turn on of S_t^L can be achieved if the current $i_{S_t^L}(DT_s)$ is negative during the dead time. Imposing a minimum value for that current, such as been done before, the condition for ZVS can be written in this way:

$$i_{S_t^L}(DT_s) = ni_s(DT_s) + i_{L_\mu}(DT_s) - i_{L_i}(DT_s) < -I_{ZVS}. \tag{3.17}$$

Looking at Fig.3.7 it's possible to see that $i_{L_\mu}(DT_s) < 0$, also in this case the magnetizing current helps the ZVS, so again its value will be neglected. Substituting the expressions of the currents into (3.17) and using straightforward

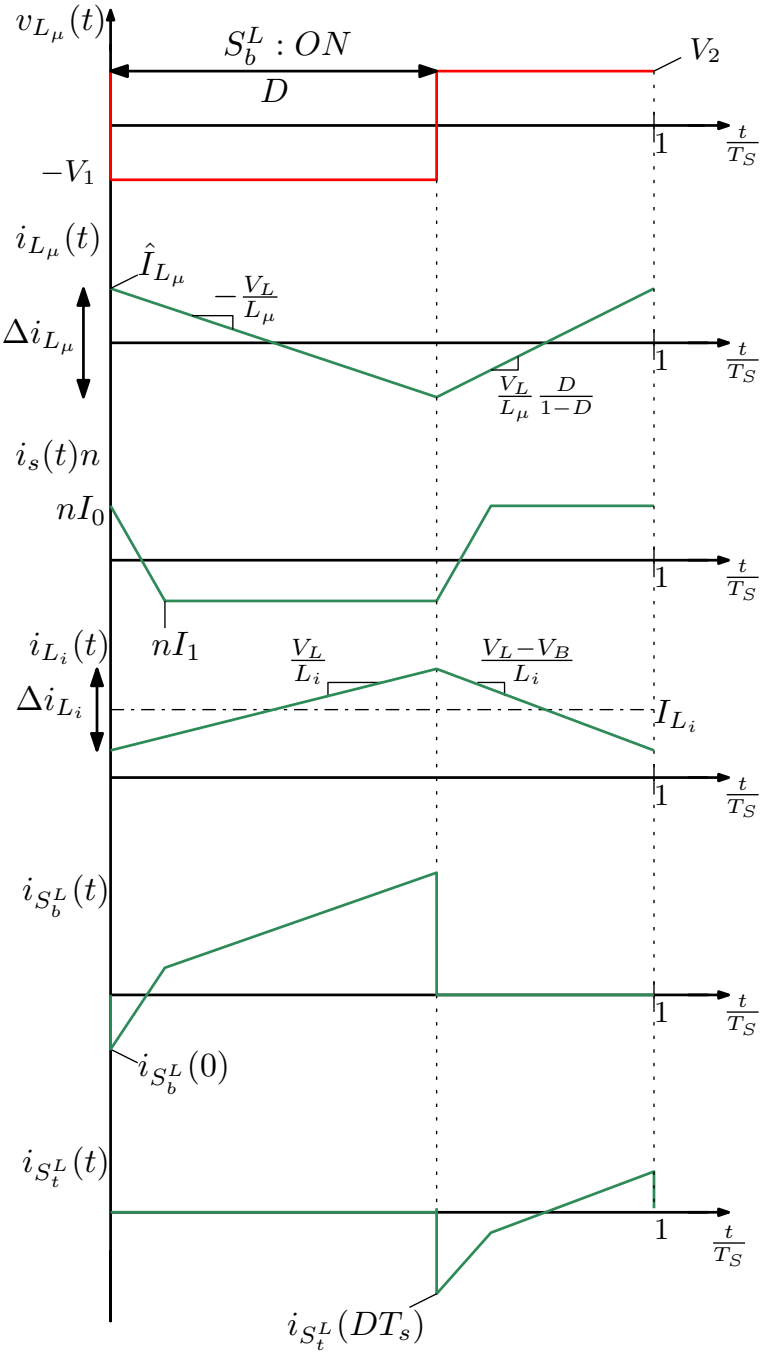


Figure 3.7: Current waveforms in region R2, current-fed side, $D_b = D_h = D$.

algebra it's possible to obtain:

$$\frac{1}{L_i} > \frac{1}{D}\left(\frac{2I_{ZVS}f_s}{V_L} - \frac{D_\phi(2-2D-D_\phi)}{U_L L_s}\right). \tag{3.18}$$

From these conditions some comments can be made:

- i_{L_μ} helps the ZVS on the current-fed side, in all the working regions;
- if $I_{ZVS} = 0$, the ZVS condition on S_b^L is always satisfied even with an infinite L_i, indeed nI_0 is always higher than the average current through L_i;
- if $I_{ZVS} = 0$, the S_t^L and S_b^L have soft-commutations for any value of L_i, as reported in [8].

3.2.1 Condition for ZVS

The minimum current necessary to achieve a ZVS commutation can be calculated using this approach: let's suppose to work at the nominal output power and let's assign a total maximum power loss (P_D), to the conduction of the body diode. A maximum dead time can be computed in order to not overcame this constraint and I_{ZVS} follows from (3.22).

A simplified behaviour during the dead time can be seen in Fig.3.8. In particular, during the discharge of the parasitic capacitors, the system recovers some energy then, due to the inverse conduction of the device, the system dissipates some energy. This approach is based on the assumption that during the dead time there is a constant current at the switching node, an approximation which simplifies the equations. The dissipated power can be estimated using the following expressions:

$$P_D \approx f_s |I| V_R (t_{dead} - t_1), \tag{3.19}$$

$$t_1 = \frac{(V_{OFF} + V_R) 2 C_{oss}}{|I|}, \tag{3.20}$$

where I is the current that goes into the switching node. So a lower boundary of the dead time is t_1, since it guarantees the discharge of the capacitances, while an upper boundary derives from the constraint on the dissipation of the body diode, as reported in the following:

$$t_1 < t_{dead} < \frac{P_D}{f_s |I| V_R} + t_1. \tag{3.21}$$

On the voltage-fed side, the current values involved in this process are I_0 and I_1, which are reported in Fig.3.9 for different input voltages. The worst case, for the choice of the dead time, corresponds at the highest value of I, since this result in a narrower interval (3.21).

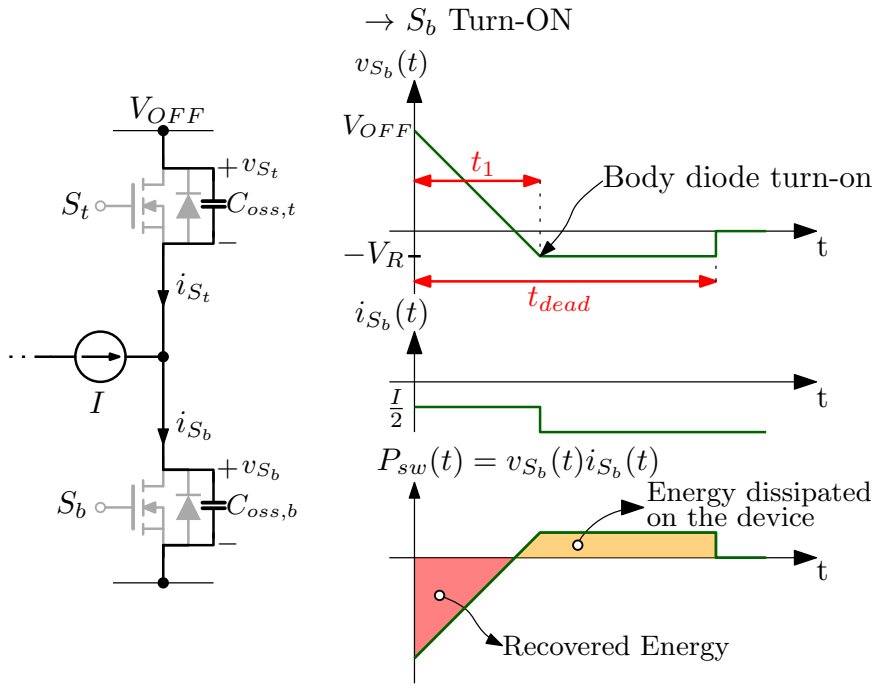


Figure 3.8: Approximated behaviour during a soft commutation of the bottom device, under the assumption of a constant current at the switching node and constant output capacitances C_{oss}. For $t \leq 0\,\text{s}$, S_t was ON.

The selected devices, for the voltage-fed side, are the UF3C065040K4S from UnitedSiC, which are 650 V Silicon Carbide MOSFETs with a reverse voltage around 1.5 V. In order to evaluate the dead time it's necessary to estimate the parasitic capacitance, using the method explained in section 2.2. Using the C_{oss} plot from the datasheet it's possible to evaluate (2.7), which results $C_{Q,eq}(400\,\text{V}) = 350\,\text{pF}$. At this point selecting $P_D = 1.25\,\text{W}$, $|I| = 30\,\text{A}$ which is the highest value from Fig.3.9.a, the dead time results: $9\,\text{ns} < t_{dead} < 148\,\text{ns}$, using (3.21). Imposing $t_{dead} = 120\,\text{ns}$ the corresponding minimum current to reach the ZVS condition is:

$$I_{ZVS} = \frac{(V_{OFF} + V_R)2C_{oss}}{t_{dead}} = 2.3\,\text{A}. \tag{3.22}$$

On the current-fed side the selected devices are the UF3C120040K4S, which are 1200 V switches with the same technology of the 650 V devices. Considering that V_B is equal to 727 V and $C_{Q,eq}(727\,\text{V}) = 285\,\text{pF}$, the minimum current necessary to completely discharge the parasitic capacitances should be around 3.5 A, using $t_{dead} = 120\,\text{ns}$ and (3.22). At this point it's possible to compute the input inductance. Let's consider the worst case which brings the lowest L_i, for this design at $V_L = 500\,V$ and $D_\phi = 0$, and results $L_i < 111\,\mu\text{H}$ using (3.16). Using

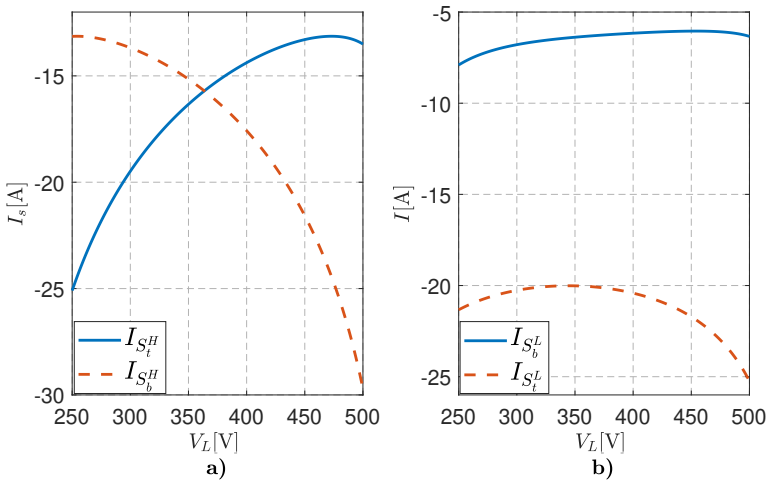


Figure 3.9: Current through the switches on the voltage-fed (a) and on the current-fed side (b), at the turn on, considering flat top current.

$L_i = 100\,\mu H$ and neglecting the current through the magnetizing inductance, the current values $i_{S_b^L}(0)$ and $i_{S_t^L}(DT_s)$, considering all the input voltage range, can be seen in Fig.3.9.b.

Summarizing this analysis reports that at low output power it's not possible to have ZVS for all the switches, as represented in Fig.3.10, since a minimum current of 2.3 A is mandatory on the voltage-fed side, to achieve the ZVS.

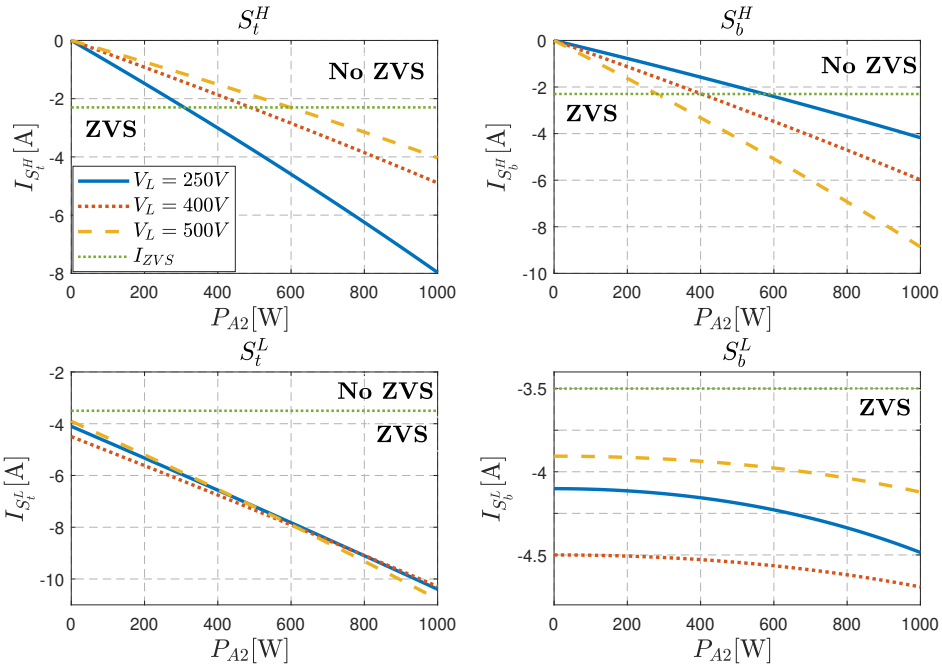


Figure 3.10: Current through the devices at the commutation instants at low output power and flat top current.

3.3 Final design

The last components to be designed are the capacitors of the half-bridge legs. Let's consider the voltage-fed side, imposing a maximum voltage ripple (ΔV_H), on each capacitor, it's possible to determine their values. The current waveforms in the capacitors' node is equal to i_s, as can be deduced from Fig.2.1. Assuming V_H constant, the voltage variations on the capacitors are equal and opposite. Using the Kirchhoff laws and imposing that $C_b^H = C_t^H = C_H$, it's possible to obtain the following relation:

$$i_{c_t}(t) = -i_{c_b}(t) = \frac{i_s(t)}{2}. \tag{3.23}$$

Fig.3.11 represents this behaviour under the hypothesis of flat top current. At this point it's possible to approximate the voltage variation using the following equation:

$$\Delta V_c \approx \frac{I_0(1 - D - D_\phi)}{2 f_s C_H}. \tag{3.24}$$

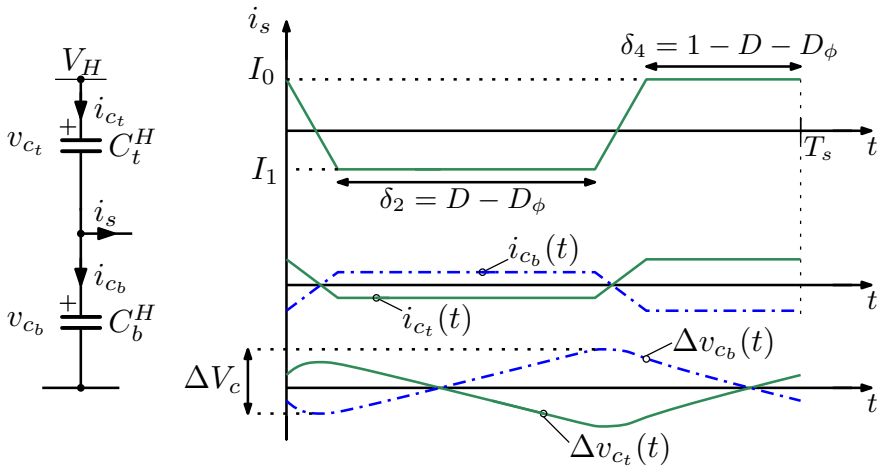


Figure 3.11: Voltage ripple on the voltage-fed side capacitors. Flat top current and $C_b^H = C_t^H$ have been assumed.

For this design, considering flat top current, the worst case, that brings the highest voltage variation, occurs at nominal output power and $V_L = 500\,\text{V}$. Selecting $\Delta V_H = 10\,\text{V}$ the capacitors result around $2\,\mu\text{F}$.

A similar procedure has been applied on the current-fed side, considering V_B constant and neglecting the magnetizing current. Imposing the same voltage ripple $\Delta V_H = 10\,\text{V}$ and under flat top current, the capacitors result close to $2\,\mu\text{F}$.

In conclusion the parameters selected for the converter are reported in the following table:

Parameter	**Symbol**	**Value**
Switching frequency	f_s	200 kHz
Transformer turns ratio	n	0.55
Transfer energy impedance	L_s	6.5 µH
Magnetizing inductance	L_μ	As big as possible
Input Inductor	L_i	100 µH
Capacitor	C_t^H, C_b^H, C_t^L, C_b^L	2 µF
S_b^L, S_t^L	UF3C120040K4S	SiC MOSFETs
S_b^H, S_t^H	UF3C065040K4S	SiC MOSFETs

Table 3.2: Prototype parameters.

Chapter 4

Magnetic components

In this chapter the magnetic components selected in chapter 3 will be designed according to the methodology presented in [10].

4.1 Input inductor design

Specifications for the input inductor:

Parameter	Symbol	Value
Inductance	L_i	100 µH
Switching frequency	f_s	200 kHz
Temperature	T	100°C

Table 4.1: Input inductor specifications.

Assuming to work at the nominal output power and an unitary efficiency, the maximum DC current is:

$$I_{DC} = \frac{P_O}{V_{Lmin}} = 10\,\text{A}. \tag{4.1}$$

The current ripple on the inductor can be calculated as reported in the following:

$$\Delta I_{Lpk-pk} = \frac{V_L D}{L f_s} = \frac{V_L(1 - n\frac{V_L}{VH})}{L f_s}, \tag{4.2}$$

where the flat-top condition (3.4) has been assumed. Using $V_L = V_{Lmin}$ the current ripple results: $\Delta I_{Lpk-pk} = 8.2\,A$. Since the shape of the current ripple is triangular, it's possible to find the RMS current easily:

$$I_{RMS} = I_{DC}\sqrt{1 + \frac{1}{3}\Big(\frac{\Delta I_{Lpk-pk}}{2I_{DC}}\Big)^2} = 10.3\,\text{A}. \tag{4.3}$$

In order to use the core geometrical constant (K_g) method [10], it's necessary to decide a certain amount of copper loss (P_{Cu}) and a maximum magnetic flux density (B_{max}). Moreover, the wires don't pack perfectly, thus the effective available area for the winding is smaller than the core window area (W_A). This effect can be taken into account using the window fill factor (K_u), a coefficient between zero and one which reduces the available space. Once these values have been selected, K_g can be calculated using (4.4). For this design, all the cores available are based on the N97 material, which has a saturation flux density around 400 mT at 100°C. After some iterations of the design, $B_{max} = 260\,\text{mT}$ and $P_{Cu} = 3\,\text{W}$ have been selected, which guarantee some margin from the saturation and an approximately equal amount of copper and core losses. At this point K_g results:

$$K_g = \frac{\rho I_{max}^2 I_{RMS}^2 L_i^2}{B_{max}^2 P_{Cu} K_u} = 0.51\,\text{cm}^5, \tag{4.4}$$

where ρ is the copper resistivity, $I_{max} = I_{DC} + \Delta I_{Lpk-pk}/2$ and $K_u = 0.5$. A suitable core is the **PQ40/40** which has the following parameters:

Parameter	**Symbol**	**Value**
Core geometrical constant	K_g	$1.20\,\text{cm}^5$
Cross section area	A_c	$189\,\text{mm}^2$
Volume	V_{ol}	$17\,580\,\text{mm}^3$
Mean length per turn	MLT	8.6 cm
Material		N97

Table 4.2: PQ40/40 core parameters. K_g has been taken from [10].

In order to estimate the core loss the Steinmetz equation (4.7) will be used. This method is based on an empirical equation, which models the core loss under sinusoidal excitation, at a given frequency and AC peak variation of the magnetic flux density (B_{pk}). The coefficients Cm, x and y of (4.7) can be extracted by fitting the manufacture's data on core loss. But this equation tries to model different contributions of losses, like Eddy current and Hysteresis loss, on a ferromagnetic material which is strongly non linear. For these reasons, this method is sensitive to the work temperature, frequency and applied waveform. In addition, manufactures report the core loss under sinusoidal excitation, which is non common in power electronics and also in this design. So there is a lot of uncertainty on this method and the coefficients fit only a small interval of operating points. In case of the N97 material the coefficients are reported in Tab.4.3.

Parameter	Value
Cm	1.26
x	1.47
y	2.40

Table 4.3: Steinmetz coefficients for N97 material at 200 kHz.

At this point is possible to calculate the number of turns and the AC variation of magnetic flux density as reported in the following:

$$N = \frac{I_{max} L_i}{B_{max} A_c} = 30, \tag{4.5}$$

$$B_{pk} = B_{max} \frac{\Delta I_{Lpk-pk}}{2 I_{max}} = 80\,\mathrm{mT}. \tag{4.6}$$

Thus the core losses can be calculated using the Steinmetz equation:

$$P_{Core} = C_m f^x B_{pk}^y V_{ol} = 3.2\,\mathrm{W}. \tag{4.7}$$

The wire selected is the Litz 1050x50 µm, which has a resistance per unit of length equal to $r_{DC} = 0.112\,\mathrm{m\Omega/cm}$ at 100 °C. The $F_R = R_{AC}/R_{DC}$ ratio can be calculated using the equations reported in App.A.2, which results $F_R = 2.5$. So the copper loss can be calculated using the following expressions:

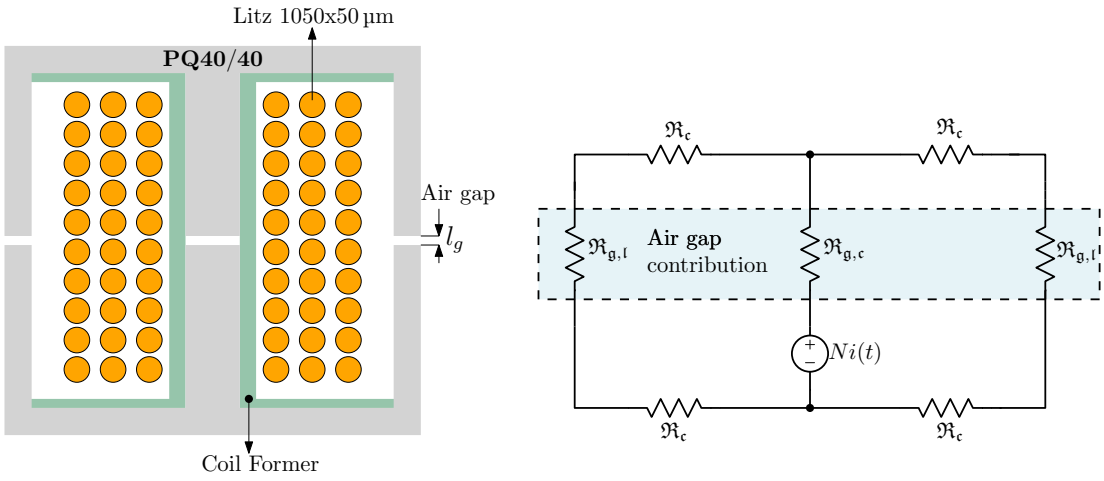
$$P_{Cu} = r_{DC}(MLT) N \left[I_{DC}^2 + F_R I_{AC}^2 \right] = 3.4\,\mathrm{W}, \tag{4.8}$$

$$I_{AC} = \sqrt{I_{RMS}^2 - I_{DC}^2} = 2.6\,\mathrm{A}, \tag{4.9}$$

where I_{AC} represents the AC component of the current.

Finally, the gap length can be calculated considering the equivalent reluctance scheme represented in Fig.4.1. Since the lateral legs have half cross section area of the central one and under an infinite relative permeability of the core material ($\mathfrak{R}_c \to 0$ [1/H]), it's possible to find an equivalent total reluctance (4.10), which models the structure. The gap length follows from (4.11) and (4.12).

$$\mathfrak{R}_{tot} = \mathfrak{R}_{g,c} + \frac{\mathfrak{R}_{g,l}}{2} = 2\mathfrak{R}_{g,c} = 2\frac{l_g}{\mu_0 A_c} \tag{4.10}$$



a) L_i realization

b) Equivalent reluctance scheme of L_i.

Figure 4.1: Representation of the inductor L_i (a) with the equivalent reluctance model (b). $\mathfrak{R}_c$ represents the core reluctance while $\mathfrak{R}_{g,c}$ and $\mathfrak{R}_{g,l}$ the central and lateral air gap reluctances.

$$L = \frac{N^2}{\mathfrak{R}_{tot}} \tag{4.11}$$

$$l_g = \frac{\mu_0 N^2 A_c}{2L} = 1.07\,mm \tag{4.12}$$

The inductor has been built in the laboratory and can be seen in Fig.4.2. It has been tuned using the impedance analyzer, adjusting the gap length to obtain the desired value. Some measurements on the prototype are reported in Tab.4.4. The final dimension of l_g is higher than expected due to the fringing effect, which increases the overall inductance.

Parameter	Measure
R_{DC}	34.3 mΩ
R_{AC}	172 mΩ
L_i	103.7 µH
l_g	2 mm

Table 4.4: Important measurements on L_i prototype, R_{AC} and L_i from the impedance analyzer at 200 kHz while R_{DC} from a volt-ampere measurement using a constat DC curent of 1 A.

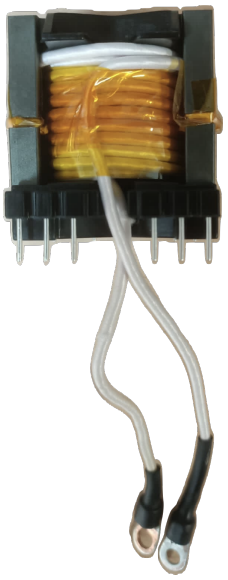


Figure 4.2: Physical inductor L_i.

4.2 Transformer design

High frequency transformers are characterized by a big and fast variations of the magnetic flux density, so core losses are a limiting factor. The peak amplitude of the AC magnetic flux density (B_{pk}) is related to the number of turns, the core cross section area and the volt-seconds applied, as reported in the following expression:

$$B_{pk} = \frac{\int_{t_1}^{t_2} |v_1(t)|dt}{2N_1A_c} = \frac{\lambda_1}{2N_1A_c}, \tag{4.13}$$

where $v_1(t)$ is the voltage applied at the primary side and the integral is defined as reported in Fig.4.3. Using the procedure explained in [10], an optimum value of B_{pk} can be found, which minimizes the core plus copper loss. In this design, a simplified and faster procedure has been followed in order to have a first prototype, the only constraint imposed was to not overcame a total power loss equal to P_T.

The selected core is the **PQ 35/35** and the operating point considered is the one with the highest volt-seconds value. Considering the flat top condition (3.4), the integral in (4.13) can be calculated as reported in the following:

$$\lambda_1 = \int_{t_1}^{t_2} |v_1(t)|dt = \frac{V_L(1 - n\frac{V_L}{V_H})}{f_s}. \tag{4.14}$$

The maximum point of (4.14) can be found by studying its derivative, as reported

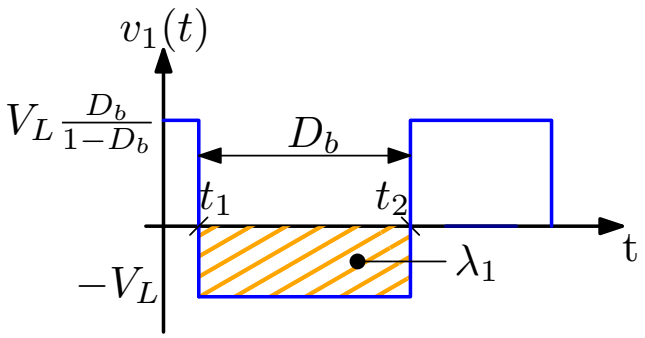


Figure 4.3: Voltage applied to the transformer primary side.

here:

$$\frac{\partial \lambda_1}{\partial V_L} = \frac{V_H - 2nV_L}{V_H f_s} = 0, \tag{4.15}$$

the solution is $V_L = \frac{V_H}{2n}$, which is a maximum as can be seen looking at the sign.

In this design $V_L = 363\,\mathrm{V}$ at nominal output power is the point with the highest volt-seconds value (λ_1), equal to $909\,\mathrm{V\mu s}$. The operating frequency is $200\,\mathrm{kHz}$, the desired turns ratio is $n = n_s/n_p = 0.55$, the secondary RMS current ($I_{RMS,2}$) is $14.6\,\mathrm{A}$, P_T has been fixed to $25\,\mathrm{W}$ and the core specifications are reported in Tab.4.5.

Parameter	Symbol	Value
Cross section area	A_c	$171\,\mathrm{mm}^2$
Volume	V_{ol}	$13\,650\,\mathrm{mm}^3$
Mean length per turn	MLT	$7.7\,\mathrm{cm}$
Material		N97

Table 4.5: PQ35/35 core parameters.

The Litz wire 1050x50 µm has been selected for the windings, since it has good performances for wire losses. After some design iterations, B_{pk} has been fixed to $170\,\mathrm{mT}$ in order to use all the available space. The number of turns result:

$$N_1 = \frac{\lambda_1}{2B_{pk}A_c} = 15, \tag{4.16}$$

$$N_2 = nN_1 = 8. \tag{4.17}$$

The effective B_{pk} can be computed using (4.13) which results around $177\,\mathrm{mT}$ and brings a core loss of $17\,\mathrm{W}$ using (4.7). The selected wire has a DC resistance per unit of length equal to $r_{DC} = 0.112\,\mathrm{m\Omega/cm}$ at 100°C and the

winding's structure can be seen in Fig.4.4. The AC resistances can be evaluated using the procedure explained in App.A.2, $F_{R1} = R_{AC1}/R_{DC1} = 1.5$ and $F_{R2} = R_{AC2}/R_{DC2} = 1.2$, which bring the following copper losses:

$$P_{Cu,1} = r_{DC} F_{R1} (MLT) N_1 I_{RMS,1}^2 = 1.2\,\mathrm{W}, \tag{4.18}$$

$$P_{Cu,2} = r_{DC} F_{R2} (MLT) N_2 I_{RMS,2}^2 = 1.8\,\mathrm{W}. \tag{4.19}$$

As can be seen from (4.18) and (4.19) the wire losses are much lower than the core loss. A different design approach aims to reach the same amount of core and copper losses, by iterating the process changing B_{pk} and the wires.

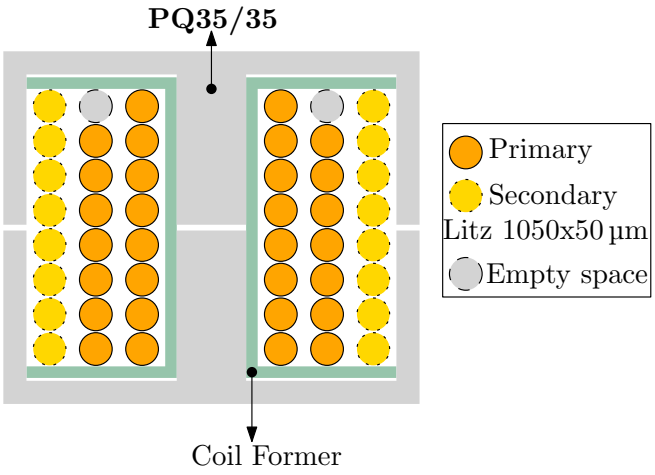


Figure 4.4: Transformer T_1 structure. Note that to obtain a big magnetizing inductance the air gap will be kept very small.

The prototype has been built in the laboratory and can be seen in Fig.4.5.

At this point it's necessary to characterize the transformer, in order to build an equivalent circuit. A generic model can be seen in Fig.4.6, where it's possible to see the leakage inductances at primary and secondary side, L_{l1} and L_{l2} respectively, and the magnetizing inductance, L_μ. The model is described by the following impedance matrix:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} s(L_{l1} + L_\mu) & snL_\mu \\ snL_\mu & s(L_{l2} + n^2 L_\mu) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{4.20}$$

The coefficients of the matrix (4.20) can be extracted by three measurements on the impedance analyzer:

- $L_1^{OL} = (L_{l1} + L_\mu)$: inductance at the primary with the secondary in open circuit,

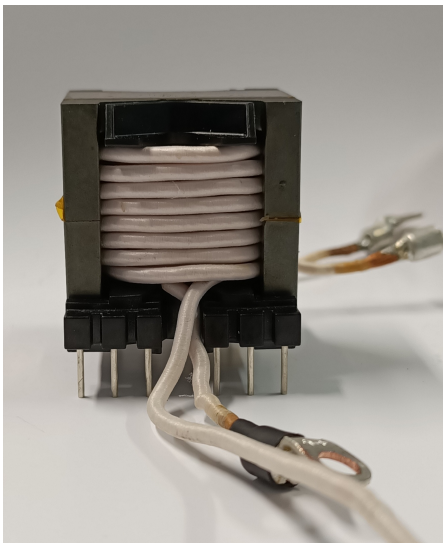


Figure 4.5: Physical realization of the transformer prototype.

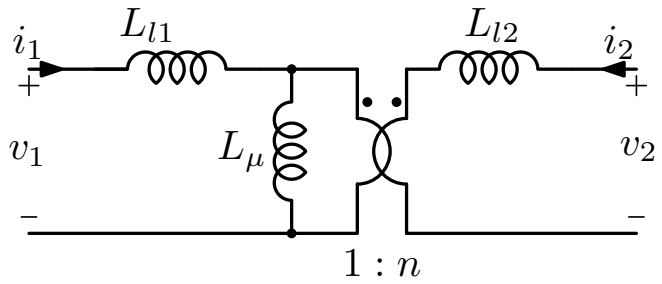


Figure 4.6: Generic transformer model with three inductances.

- $L_1^{SC} = L_{l1} + (L_\mu \parallel L_{l2}/n^2)$: inductance at the primary with the secondary short circuited,
- $L_2^{OL} = L_{l2} + L_\mu n^2$: inductance at the secondary with the primary in open circuit.

The measurements are reported in the following table:

Parameter	$\mathbf{R_s}$ [Ω]	$\mathbf{L_s}$ [µH]
Z_1^{OL}	1.136	275.78
Z_1^{SC}	0.064	3.04
Z_2^{OL}	0.376	79.05

Table 4.6: Measurements from the impedance analyzer at 200 kHz using the R_s, L_s function.

The number of turns can be fixed as reported in (4.21), neglecting the leakage inductances.

$$n \approx \sqrt{\frac{L_2^{OL}}{L_1^{OL}}} = 0.535 \tag{4.21}$$

The model's parameters can be found using the expressions reported here:

$$\begin{cases} L_\mu = \sqrt{(L_1^{OL} - L_1^{SC})L_2^{OL}/n^2} = 274.3\,\mu\text{H}, \\ L_{l1} = L_1^{OL} - L_\mu = 1.5\,\mu\text{H}, \\ L_{l2} = L_2^{OL} - n^2 L_\mu = 436.9\,\text{nH}. \end{cases} \tag{4.22}$$

Once the model in Fig.4.6 has been characterized, it's possible to extract the parameters for the one used during the steady-state analysis, reported in Fig.4.7 and described by the following impedance matrix:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} sL_{\mu,eq} & sL_{\mu,eq}n_{eq} \\ sL_{\mu,eq}n_{eq} & s(L_{l,eq} + n_{eq}^2 L_{\mu,eq}) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{4.23}$$

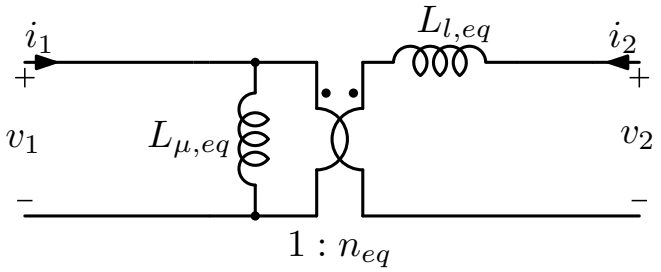


Figure 4.7: Transformer model with only two inductances.

Equating the elements of the two matrices, (4.20) and (4.23), it's possible to obtain all the parameters, reported in Tab.4.7, using the following expressions:

$$\begin{cases} L_{\mu,eq} = L_{l1} + L_\mu, \\ n_{eq} = n\frac{L_\mu}{L_{\mu,eq}}, \\ L_{l,eq} = L_{l2} + nn_{eq}L_{l1}. \end{cases} \tag{4.24}$$

Parameter	**Value**
$L_{\mu,eq}$	275.8 µH
n_{eq}	0.532
$L_{l,eq}$	871.4 nH

Table 4.7: Parameters for the equivalent model of Fig.4.7.

4.3 Energy transfer inductor design

The design of the inductor L_s should consider the transformer leakage inductance at the secondary side ($L_{l,eq}$), indeed the sum of these should be equal to 6.5 µH. Since $L_{l,eq}$ is too small, an external 5.6 µH inductance will be designed. First of all it's useful to understand the voltage waveform applied to L_s, which is reported in Fig.4.8 under the hypotheses to work in region R2 and with the same duty cycle (3.4) on the two switching legs. Starting from the Faraday's law, it's possible to

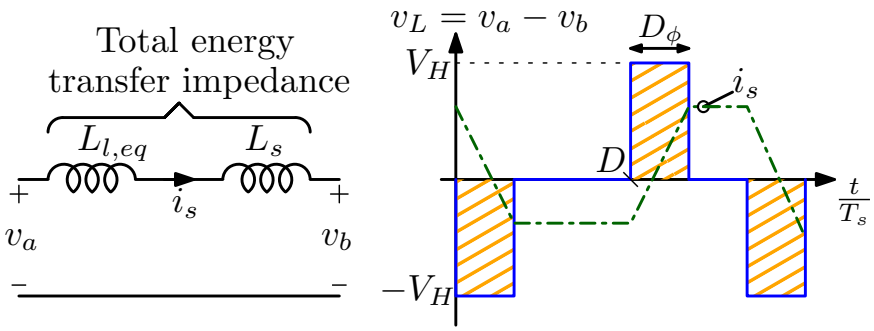


Figure 4.8: Voltage waveform applied to the energy transfer impedance.

find the AC peak value of the magnetic flux density:

$$B_{pk} = \frac{1}{2NA_c}\int_0^{D_\phi T_s} \alpha v_L(\tau)d\tau = \frac{\alpha V_H D_\phi}{2f_s N A_c}, \tag{4.25}$$

where N is the number of turns, A_c is the cross section area of the core and $\alpha = \frac{L_s}{L_s+L_{l,eq}}$. This inductor has an high magnetic flux density variation so the core loss cannot be neglected. For this reason it's necessary to find an optimum value for B_{pk}, which minimizes the core plus copper losses. An iterative process has been followed, starting from the selection of the core and selecting the number of turns in order to minimize the total losses. At the end of this process the core **PQ32/30** has been selected for its small size and low loss. The volt-second value (λ) applied to the inductor can be calculated using the following expression:

$$\lambda = \frac{\alpha V_H D_\phi}{f_s}. \tag{4.26}$$

The phase shift (D_ϕ) is a function of the output power (P_L) and can be calculated solving (3.5) for D_ϕ, as reported here:

$$D_\phi = D(1-D)\left[1 - \sqrt{1 - \frac{P_L/P_N}{\pi D^2(1-D)^2}}\right]. \tag{4.27}$$

where the minus sign has been selected, in the solution of the second order equation, to obtain a phase shift lower than the peak (3.6). For this design, the point with the highest λ has been selected, that corresponds to $V_L = 500\,\mathrm{V}$ with $D_\phi = 0.14$ at nominal output power and flat-top condition. This operating point brings $\lambda \approx 243\,\mathrm{V\mu s}$ and a RMS current equal to $I_{RMS} = 17.8\,\mathrm{A}$. The operating frequency is again 200 kHz and a temperature of 100°C will be be considered.

The core specifications are reported in Tab.4.8 while the parameters in Tab.4.3 can be used to estimate the core loss through the Steinmetz equation, reported in the following expression:

$$P_{Core} = C_m f^x B_{pk}^y V_{ol} = K_{Core} B_{pk}^y. \tag{4.28}$$

Parameter	Symbol	Value
Cross section area	A_c	$153.8\,\mathrm{mm}^2$
Volume	V_{ol}	$10\,440\,\mathrm{mm}^3$
Mean length per turn	MLT	6.82 cm
Window area	W_A	$107.3\,\mathrm{mm}^2$
Material		N97
Window fill factor	K_u	0.5

Table 4.8: PQ32/30 core parameters.

Tab.4.8 can be used to estimate the wire length and so the losses, which are divided into DC and AC. In this case the average current is 0 A, so only the AC losses will be considered. The coefficient $F_R = R_{AC}/R_{DC}$ is assumed equal to 2, since the winding's structure isn't known yet. At this point it's possible to express the wire loss as a function of B_{pk}:

$$P_{Cu} = \rho F_R \frac{(MLT)N}{A_w} I_{rms}^2 = \rho F_R \frac{(MLT) I_{RMS}^2 \lambda^2}{4 K_u W_A A_c^2} \frac{1}{B_{pk}^2} = \frac{K_{Cu}}{B_{pk}^2} \tag{4.29}$$

where (4.25) and $K_u W_A = A_w N$ have been used.

The total power loss can be expressed as the sum of wire and core loss:

$$P_{tot} = P_{Cu} + P_{Core} = \frac{K_{Cu}}{B_{pk}^2} + K_{Core} B_{pk}^y. \tag{4.30}$$

Looking on (4.28) and (4.29) can be seen that the wire loss decreases as B_{pk} increases, vice versa for the core loss, thus there is a point which minimizes the

sum of the two contributions. The point which minimizes (4.30) can be found using the following method:

$$\frac{\partial P_{tot}}{\partial B_{pk}} = \frac{\partial P_{Cu}}{\partial B_{pk}} + \frac{\partial P_{Core}}{\partial B_{pk}} = 0, \tag{4.31}$$

which brings an optimum AC peak flux density equal to:

$$B_{pk,opt} = \left(\frac{2K_{Cu}}{yK_{Core}}\right)^{\left(\frac{1}{y+2}\right)} = 75\,\mathrm{mT}, \tag{4.32}$$

this value can be seen on Fig.4.9.

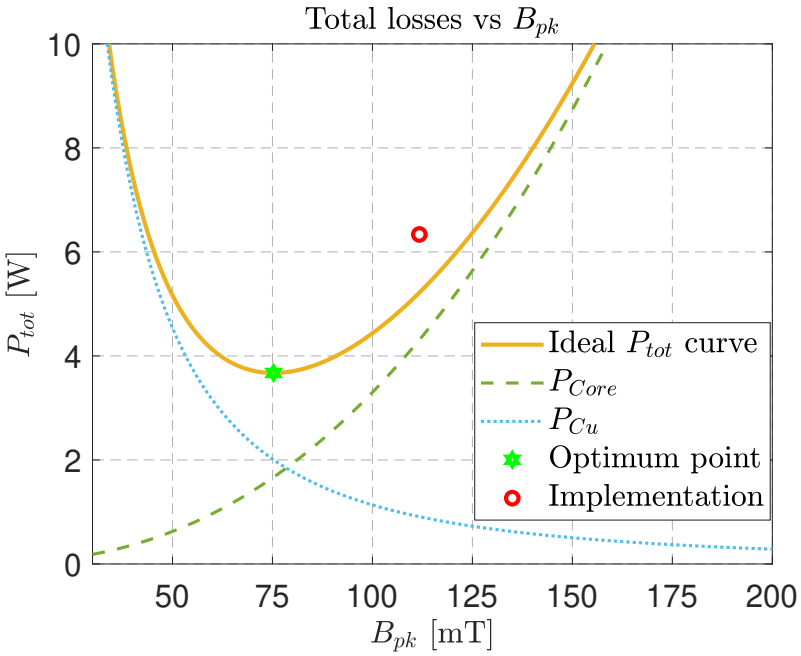


Figure 4.9: Inductor losses as a function of B_{pk}.

At this point it's possible to calculate the number of turns, which is equal to $N = 10$ using (4.25). The selected core has the same structure of the one used for L_i, so it's possible to find the air gap length using the following expression:

$$l_g = \frac{\mu_0 N^2 A_c}{2L_s} \approx 1.7\,\mathrm{mm}. \tag{4.33}$$

This gap size is quite high taking into account that the real implementation will use an higher value due to, for example, fringing flux. Further, fringing increases the wire losses. So the number of turns have been reduced to $N = 7$, in

order to decrease l_g to the one reported here:

$$l_g = \frac{\mu_0 N^2 A_c}{2L} \approx 845\,\mu\text{m}, \tag{4.34}$$

obviously this increases the core loss.

The wire selected for the winding is the Litz wire 1050x50 µm which has a DC resistance per unit of length equal to $r_{DC} = 0.112\,\text{m}\Omega/\text{cm}$ at 100°C. Its diameter allows only one layer of winding and this is the best condition for wire loss. The inductor has been wounded as represented in Fig.4.10, this structure brings $F_R = R_{AC}/R_{DC} = 1.2$, using the equations reported in App.A.2, and a copper loss equal to:

$$P_{Cu} = r_{DC}(MLT)NF_R I_{RMS}^2 = 2\,\text{W}. \tag{4.35}$$

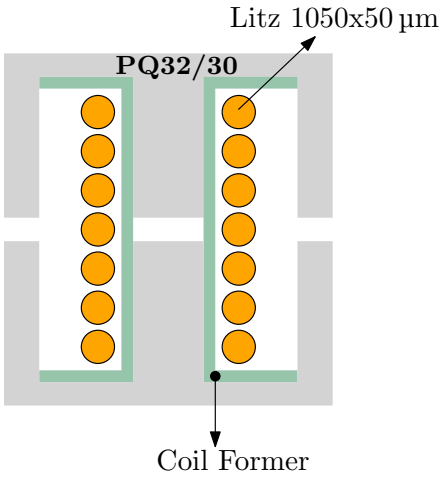


Figure 4.10: Inductor L_s winding structure.

Since the number of turns have been fixed to $N = 7$, the corresponding B_{pk} is equal to 111.7 mT using (4.25), while P_{Core} is 4.4 W using (4.28). At the end the total losses would be $P_{tot} \approx 6.4\,\text{W}$, this power point is represented also in Fig.4.9 with a circle.

The inductor has been made in the laboratory and it can be seen in Fig.4.11, the right inductance value has been tuned using an impedance analyzer and some measurements are reported in Tab.4.9.

Parameter	Value
R_{DC}	$5.1\,\mathrm{m\Omega}$
R_{AC}	$11.4\,\mathrm{m\Omega}$
L_s	$5.5\,\mu\mathrm{H}$
l_g	$1.7\,\mathrm{mm}$

Table 4.9: Measurements on L_s prototype. R_{AC} and L_s from the impedance analyzer at 200 kHz, while R_{DC} using a volt-ampere measurement using a constant DC current of 1 A.

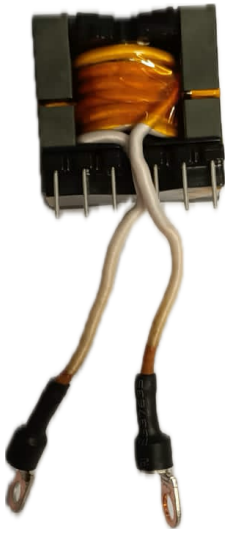


Figure 4.11: Physical inductor L_s.

Chapter 5

Simulation

In this chapter will be explained how the circuit has been simulated, in order to verify the theoretical behaviour of the topology. Simulations have been set up using the PLECS/Simulink environment and they consider the effective values of the components, in particular for the magnetic parts. Some measurements will be reported, together with the estimation of the converter efficiency. The adopted parameters are reported in the following table:

Parameter	**Symbol**	**Value**
Switching frequency	f_s	200 kHz
Input Inductor	L_i	103.7 µH
Series resistance	r_{L_i}	34.3 mΩ
Transformer turns ratio	$n = n_s/n_p$	0.535
Primary Magnetizing inductance	L_μ	274.3 µH
Primary Leakage inductance	L_{l1}	1.5 µH
Secondary Leakage inductance	L_{l2}	436.9 nH
Equivalent series resistance	r_T	64 mΩ
Transfer energy impedance	L_s	5.5 µH
Series resistance of L_s	r_{L_s}	11.4 mΩ
Capacitor	C_t^H, C_b^H, C_t^L, C_b^L	2 µF
Capacitor ESR	ESR_t^L, ESR_b^L	12.5 mΩ
	ESR_t^H, ESR_b^H	40 mΩ
1200 V Switch series resistance	$r_{s,L}$	35 mΩ
650 V Switch series resistance	$r_{s,H}$	42 mΩ

Table 5.1: Effective parameters used into the simulations. ESR values taken from the capacitors used on the physical prototype.

5.1 PLECS configuration

On the PLECS environment the implemented circuit is reported in Fig.5.1. Particular attentions should be given to the transformer component, which implements the following equations:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_1 & M_{1,2} \\ M_{2,1} & L_2 \end{bmatrix} \begin{bmatrix} \frac{d}{dt} i_1 \\ \frac{d}{dt} i_2 \end{bmatrix}, \tag{5.1}$$

this means that it can model general coupled inductors. It has been chosen to implement the model of Fig.4.6 using the coefficients of (4.20) in the time domain.

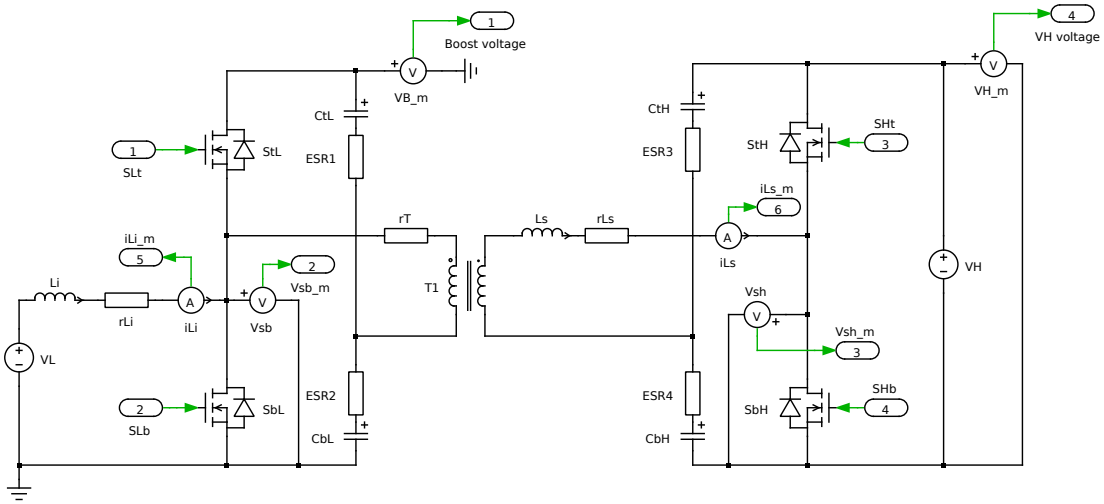


Figure 5.1: Circuit implemented on PLECS.

5.2 Simulink configuration

The Simulink environment has been configured as reported in Fig.5.2, where it's possible to see three different areas:

- *Control signal generation*: a three inputs block which generates the commands for the switching legs and the phase shift;
- *Current-Fed Dual-Half-Bridge Circuit*: the PLECS circuit of Fig.5.1 has been implemented herein;
- *Measurements*: where scopes visualized some important quantities.

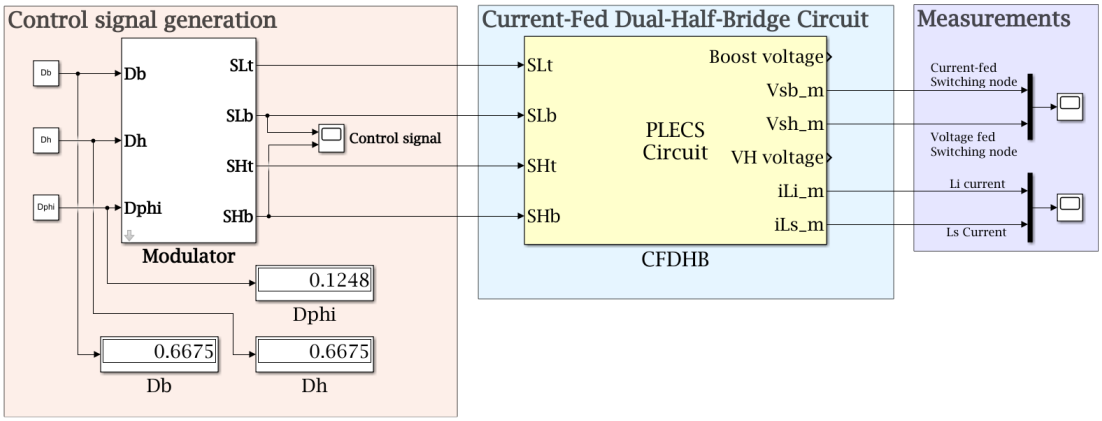


Figure 5.2: Simulink configuration used to test the PLECS circuit.

5.3 Simulation results

The circuit designed so far has been simulated and some important waveforms, at steady-state, are reported in Fig.5.4 and Fig.5.5. Furthermore, the current values at the beginning of each sub-interval has been measured and compared with the theoretical ones, obtained from (2.2) and (2.3). That values are summarized in Tab.5.2 and Tab.5.3, where it's possible to see good matches.

Parameter	Theory	Simulation
I_0 [A]	26.1 A	26.6 A
I_1 [A]	−13.0 A	−13.4 A
I_2 [A]	−13.0 A	−12.5 A
I_3 [A]	26.1 A	27.0 A
P_{out} [W]	2500 W	2557 W

Table 5.2: Comparison between theoretical and simulated values considering $V_L = 250\,\text{V}$, $D_b = D_h = 0.667$ using (3.4) and nominal output power. $D_\phi = 0.1248$ has been used, which is the theoretical value obtainable from (4.27) to reach the nominal output power considering the effective parameters in Tab.5.1. Simulated waveforms in Fig.5.4.

5.3.1 Efficiency evaluation

A simulation set-up has been carried out in order to estimate the efficiency of the converter. It has been evaluated for two different input voltages and different output powers. The measurements are reported in Fig.5.3. As can be seen the efficiency is always higher than 95% for a wide power range, with an estimated peak efficiency of 96.5% at $V_L = 400\,\text{V}$ and $P_O = 2\,\text{kW}$.

Parameter	Theory	Simulation
I_0 [A]	9.0 A	9.2 A
I_1 [A]	9.0 A	8.9 A
I_2 [A]	−7.9 A	−8.2 A
I_3 [A]	−7.9 A	−7.8 A
P_{out} [W]	−1500 W	−1548 W

Table 5.3: Comparison between theoretical and simulated values considering $V_L = 400\,\mathrm{V}$, $D_b = D_h = 0.468$ using (3.4) and $-1.5\,\mathrm{kW}$ as output power. $D_\phi = -0.0538$ has been used, which is the theoretical value obtainable from (4.27), considering the absolute value of the power and the effective parameters in Tab.5.1. Simulated waveforms in Fig.5.5.

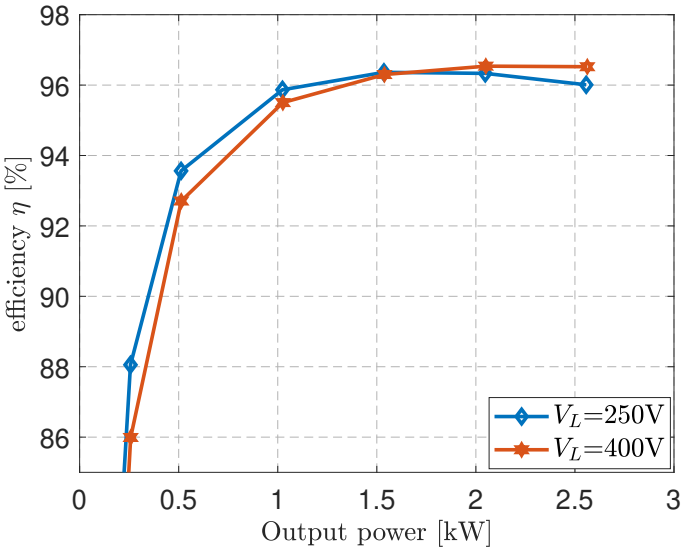
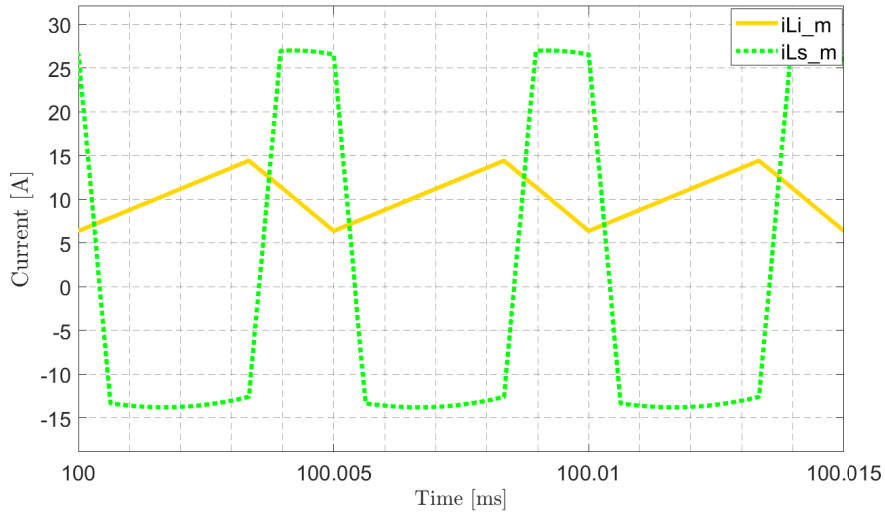
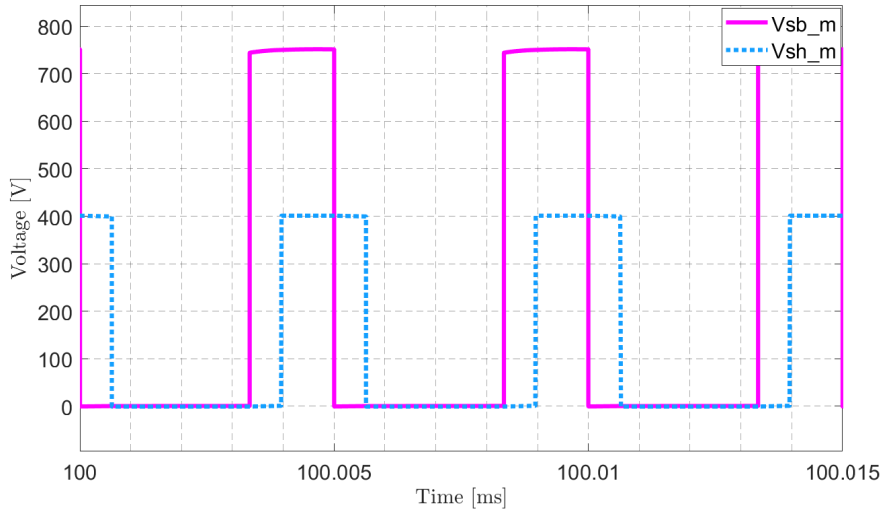


Figure 5.3: Estimated efficiency from simulation.

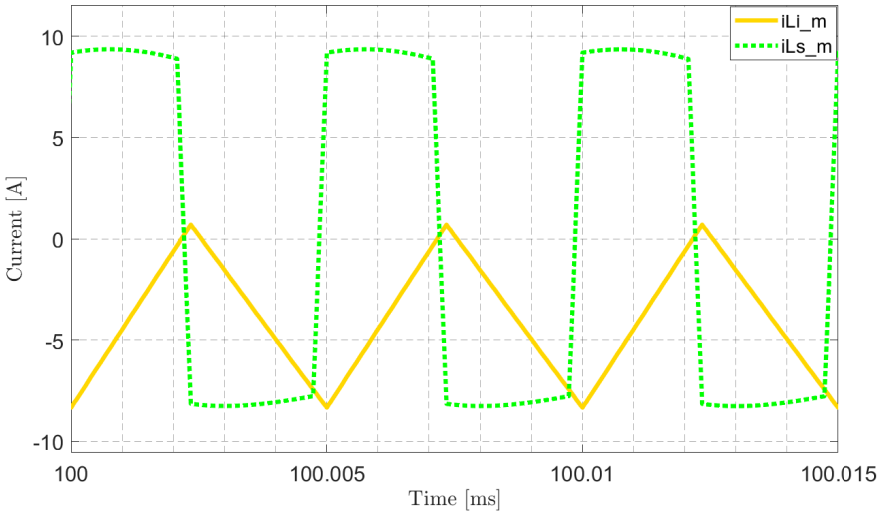


(a)

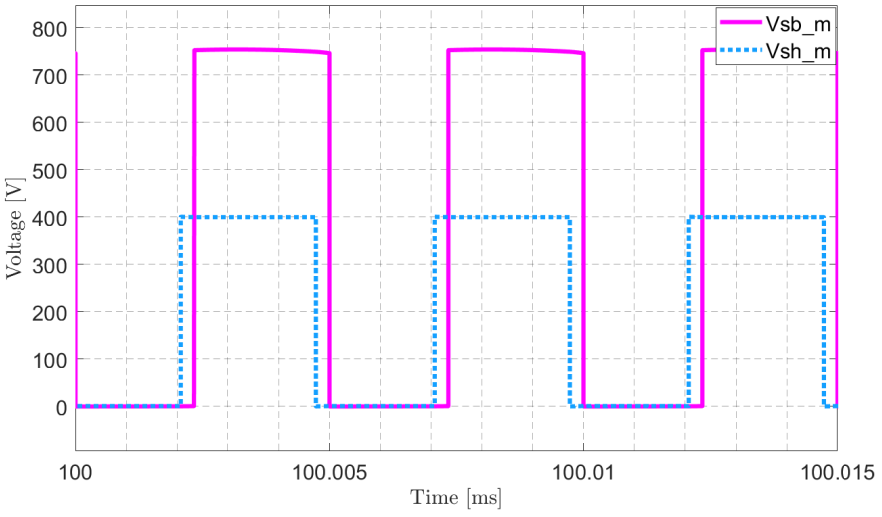


(b)

Figure 5.4: Simulation results for $V_L = 250\,\mathrm{V}$, $V_H = 400\,\mathrm{V}$ and $P_o = 2557\,\mathrm{W}$ (measured considering the average power at the V_H generator). Measurements have been taken following Fig.5.2 and Fig.5.1.



(a)



(b)

Figure 5.5: Simulation results for $V_L = 400\,\mathrm{V}$, $V_H = 400\,\mathrm{V}$ and $P_o = -1548\,\mathrm{W}$ (measured considering the average power at the V_H generator). Measurements have been taken following Fig.5.2 and Fig.5.1.

Chapter 6

Experimental validation

In this chapter will be reported the physical realization of the prototype. The magnetic components realized in Ch.4 will be used together with the switching legs realized in the following. The prototype will be controlled through a micro-controller with a strategy explained in App.B.

6.1 Prototype construction

The basic building block (BB) of this prototype is a switching leg connected to a capacitors leg, a representation of this BB can be seen in Fig.6.1. It's possible to see some circles which represent connection points, often based on screws.

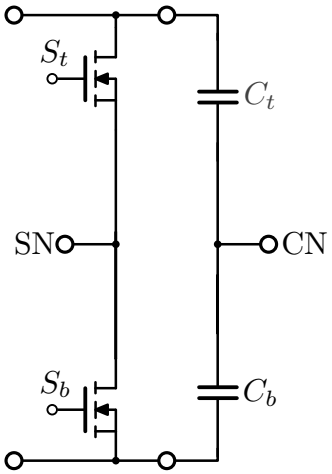


Figure 6.1: Basic building block, circles represent connection points. Switching Node (SN) and Capacitor Node (CN) represented.

Two BBs have been built in the laboratory and one of these can be seen in Fig.6.2. MOSFETs are on the bottom side of the board since they will be

connected to an heat sink. Each switch will be controlled, in an isolated way, through a pin on the Control Pin connector.

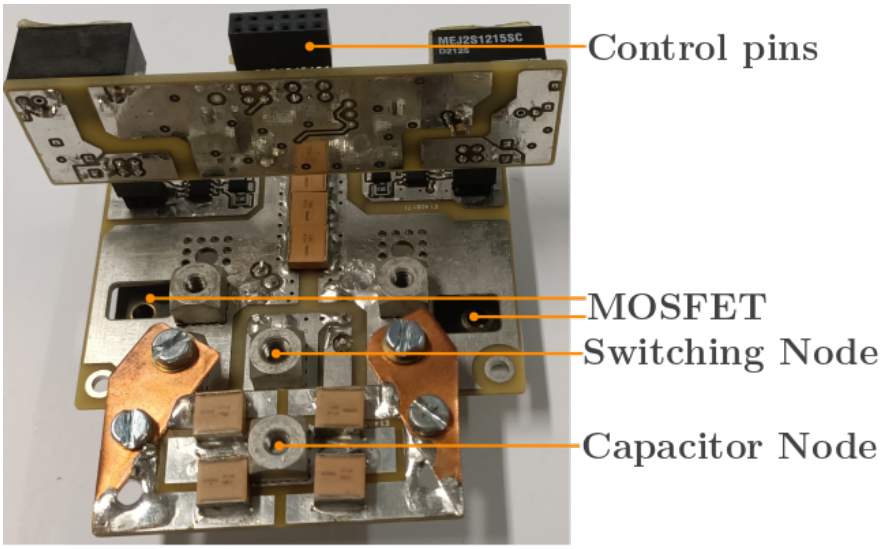


Figure 6.2: Physical realisation of one building block in Fig.6.1 with all the auxiliary components necessary for the control.

At this point, the two BBs have been attached on an heat sink and all the components have been added, according to the schematic of Fig.2.1. The realized prototype can be seen in Fig.6.3. A test bench has been set up connecting the Current-Fed side to a generator and the Voltage-Fed side to an active load. The converter has been controlled through a microcontroller, as explained in App.B, and a PC to control the duty-cycles and the phase shift. Some measurements have been taken following the probe connections of Fig.6.4.a. The test bench can be seen in Fig.6.4.b, note that the two generators mentioned aren't in the figure since they are too big.

6.2 Experimental results

A first test has been done at a reduced output power and voltage, to verify the converter behaviour. The voltage V_L has been increased until 200 V keeping flat-top current shape and ZVS commutations, thanks to the active load. As expected, the first thing noticed was that this converter is very sensitive to the phase shift, indeed, small variations brought high power variations. An output power of 1 kW has been reached and the measured waveforms are reported in Fig.6.5. With the voltage levels under test, the flat top condition can be reached using $D = 1 - nU_L = 0.516$, with $n = 0.532$, this theoretical duty cycle is very

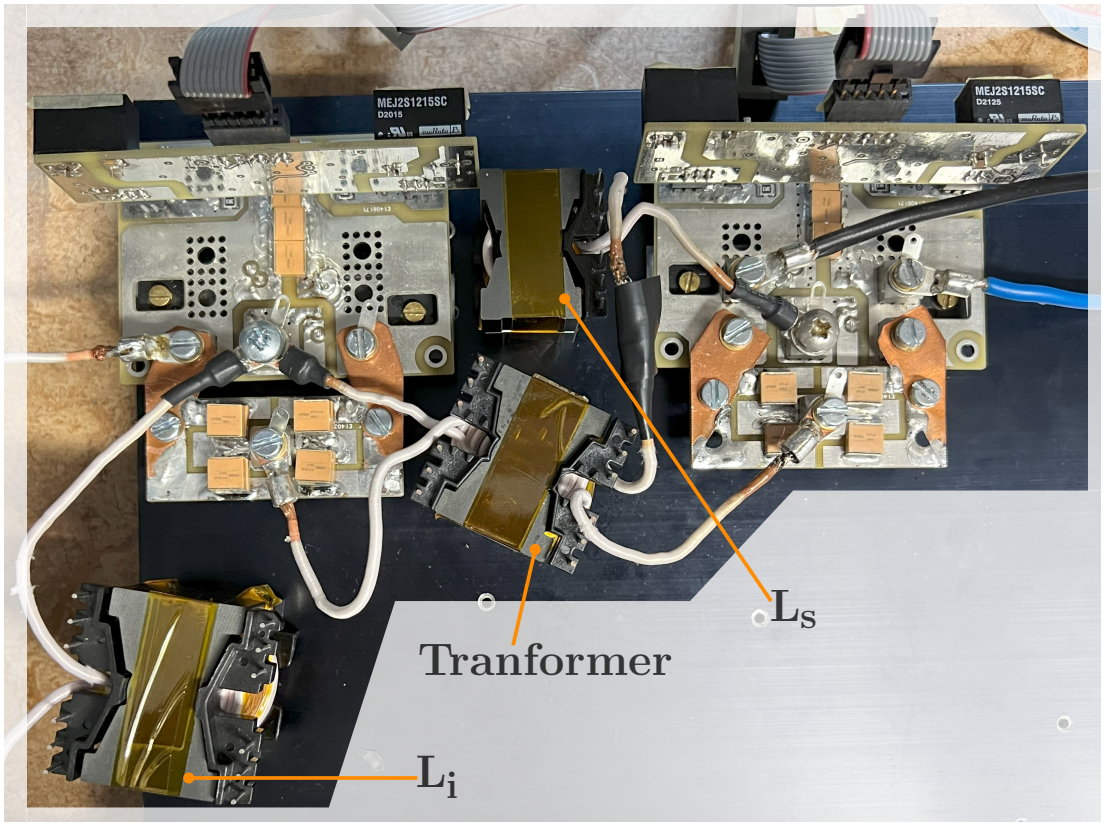


Figure 6.3: CFDHB prototype highlighting the input inductance (L_i), the transformer and the energy transfer impedance (L_s).

close to the experimental one, as can be seen in Fig.6.5.

At this point voltage V_L has been increased reaching around 2 kW of output power visible in Fig.6.6. So looking at the two tests, some considerations can be made:

- From the current variation of Fig.6.5.b, which is around 26 A, and the phase shift, it's possible to estimate the equivalent energy transfer impedance:

$$L_s = \frac{V_H D_\phi}{f_s \Delta I} \approx 6.1\,\mu\text{H}, \tag{6.1}$$

  slightly lower than designed. So an higher power transfer capability is expected.

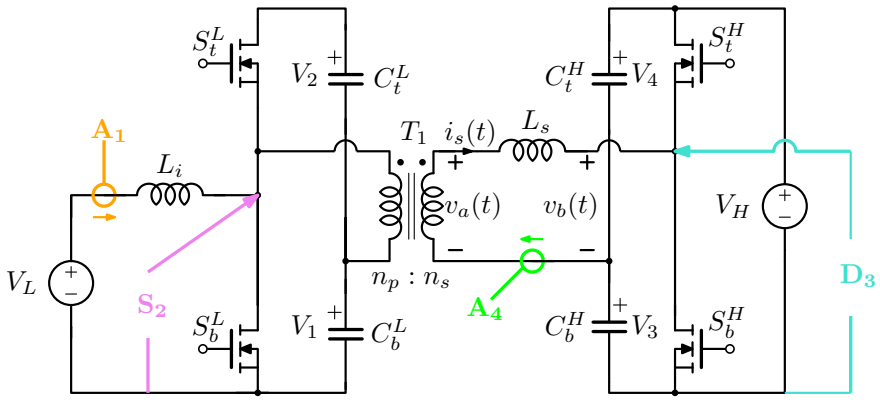
- In each figures, the ZVS commutations are verified for all the switches.

- In Fig.6.6 the current doesn't have a good flat-top shape, indeed the required duty cycle would have to be around 63%, an higher D_b increases the voltage V_B flattening the current.

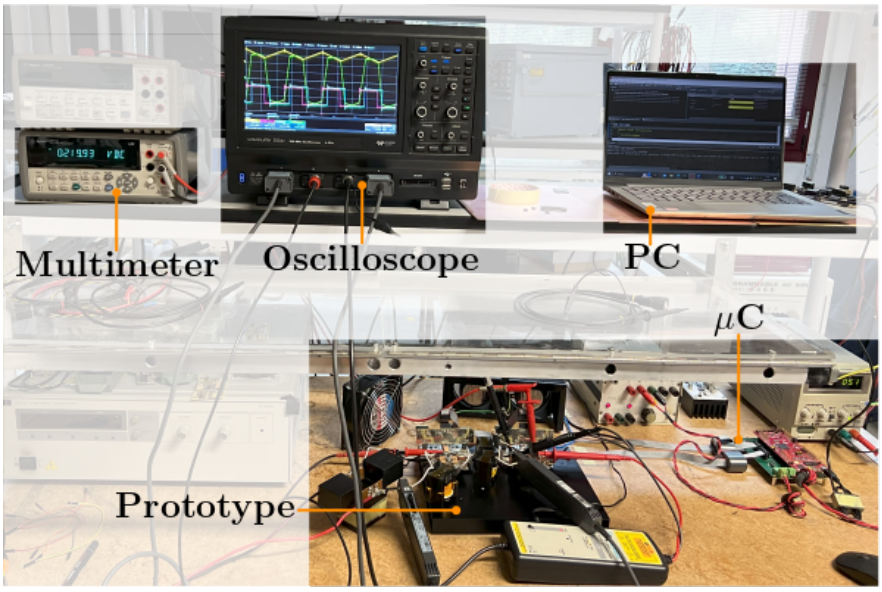
- Considering 6.1 µH as the energy transfer impedance there is a good match between the current values measured on the 1 kW test and the theoretical ones, as reported in Tab.6.1.

	Theory	**Measure**
I_0 [A]	13.8	13
I_1 [A]	-12.5	-13
I_2 [A]	-12.7	-12
I_3 [A]	-13.5	14
P_O [W]	1026	1092

Table 6.1: Theoretical and measured values at 1 kW. The same duty cycles on Fig.6.5 and $n = 0.532$ have been considered for the theoretical values.

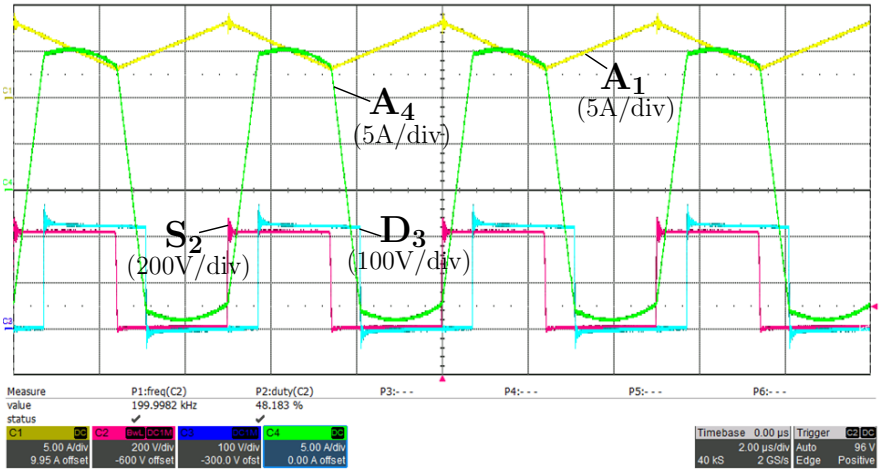


(a)

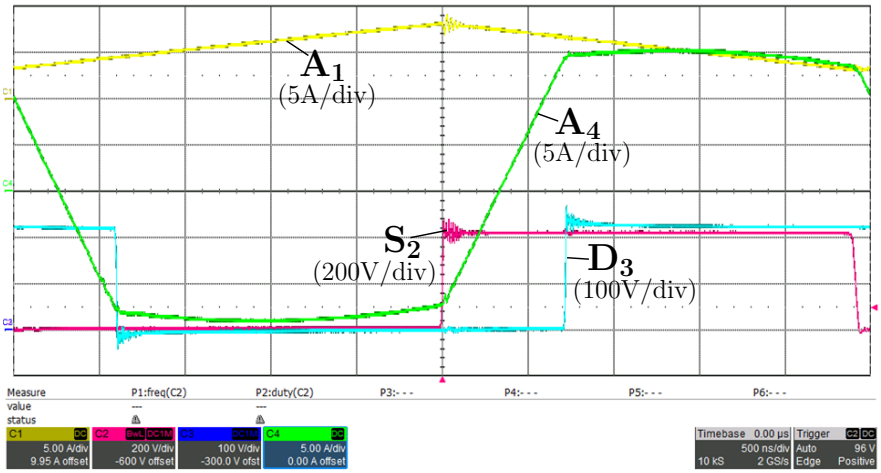


(b)

Figure 6.4: (a) Schematic representation of the probe connections. A: Current Probe; S: Simple voltage probe; D: Differential probe. (b) Test bench for the converter. The oscilloscope acquires the signals according to the above schematic while the multimeter measures the voltage on the V_H side.



(a)



(b)

Figure 6.5: Experimental waveforms at $V_L = 200\,\mathrm{V}$, $V_H = 220\,\mathrm{V}$ and $P_O = 1092\,\mathrm{W}$. $D_b = D_h = 52\,\%$, $D_\Phi = 0.145$. (a) waveforms on multi periods, (b) detail view on the phase shift. Measurements taken according to Fig.6.4.a. Note that the duty cycle measure on (a) corresponds to $1 - D_b$.

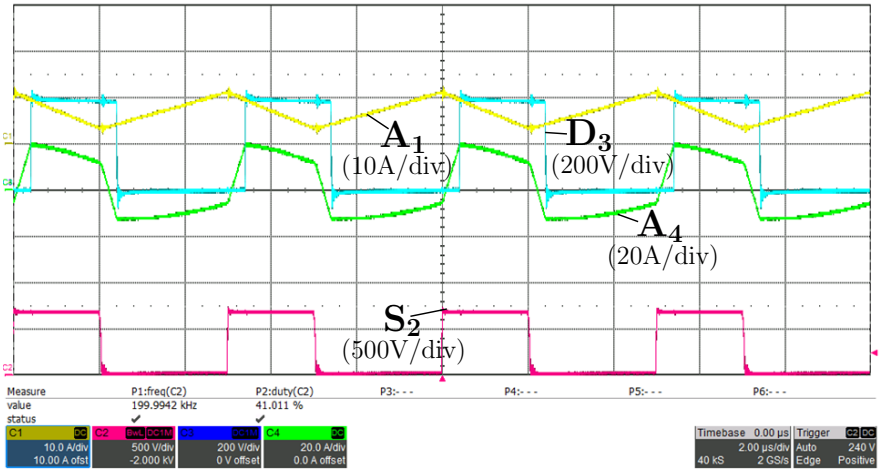


Figure 6.6: Experimental waveforms at $V_L = 277\,\mathrm{V}$, $V_H = 403\,\mathrm{V}$ and $P_O = 2005\,\mathrm{W}$. $D_b = D_h = 59\,\%$, $D_\Phi = 0.08$. Measurements taken according to Fig.6.4.a.

Chapter 7

Extension of ZVS range

In this section a simple modification of the topology will be discussed, in order to achieve soft switching commutations of all devices, in any operating point. Up to this point this cannot be achieved, as can be seen in Fig.3.10. Indeed, for low output power, the impressed current during the dead time is not enough to fully discharge the output capacitances.

7.1 Proposed solution

The proposed circuit modification can be seen in Fig.7.1, and uses an available degree of freedom from the previous design: the transformer magnetizing inductance, L_μ. In this way it's possible to introduce a current, at the switching node, which helps the ZVS.

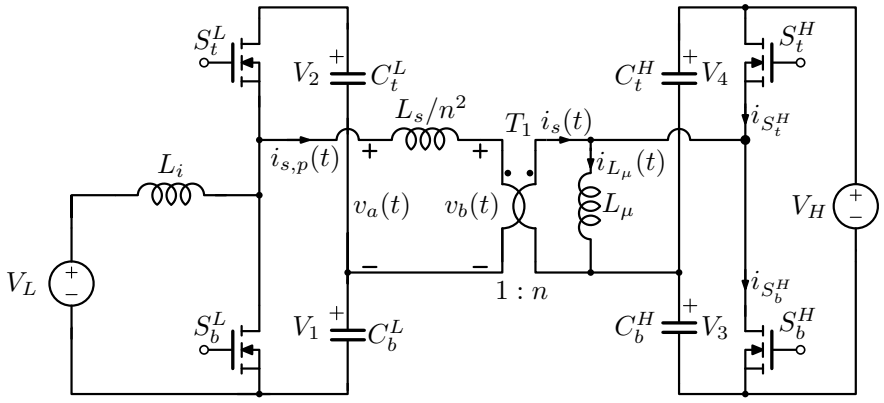


Figure 7.1: Proposed circuit to extend the ZVS range. The magnetizing inductance has been purposely shown and the energy transfer impedance has been only scaled by the number of turns squared. The MOSFET body diodes are implicitly considered.

The modified behaviour can be seen in Fig.7.2, where it's clear that, at the

commutation instants, the current i_{L_μ} has the right sign to help the discharge of the output capacitances. This means that, by selecting a proper magnetizing inductance, a minimum current can be guaranteed, at the commutations.

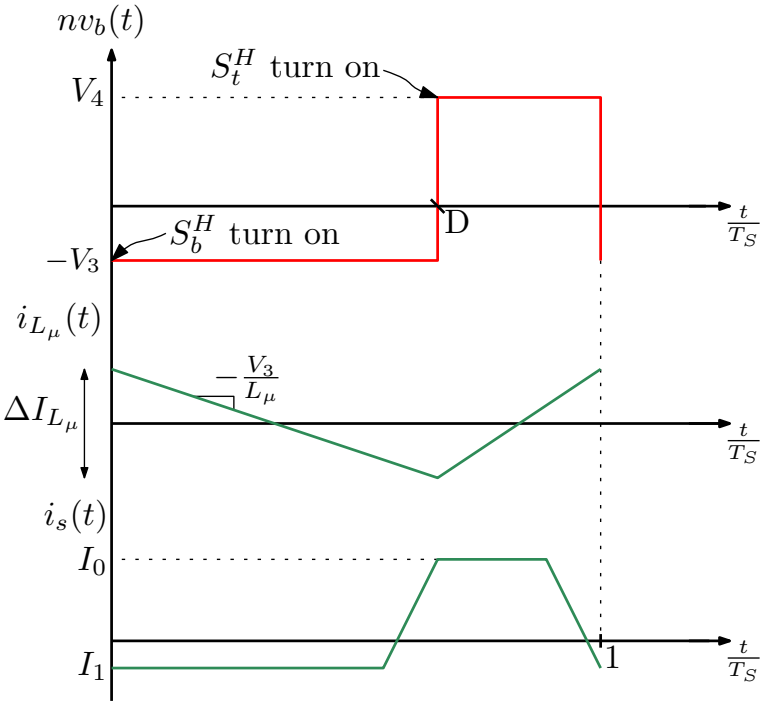


Figure 7.2: Main current and voltage waveforms.

The current ripple on L_μ can be calculated easily:

$$\Delta I_{L_\mu} = \frac{V_H(1-D)D}{L_\mu f_s}. \tag{7.1}$$

The magnetizing inductance can be sized following a similar procedure used in Ch.3 to design L_i. Let's start considering the S_b^H turn on, using the Kirchhoff current law it's possible to write:

$$I_{S_b^H} = i_s(0) - i_{L_\mu}(0) = I_1 - \frac{\Delta I_{L_\mu}}{2} < -I_{ZVS}, \tag{7.2}$$

that should be smaller than the threshold current calculated in Ch.3, namely $I_{ZVS} = 2.3\,\mathrm{A}$ for this design. Using (3.11) and (7.1) it's possible to obtain:

$$\frac{1}{L_\mu} > \frac{1}{D}\left[\frac{2f_s I_{ZVS}}{nV_L} - \frac{2D_\phi}{L_s}\right]. \tag{7.3}$$

Following a similar procedure for S_t^H, the same condition (7.3) has been found. Considering the worst case for this design at $D_\phi = 0$ and $V_L = 500\,\mathrm{V}$,

which brings the lowest L_μ, it's possible to write:

$$L_\mu < \frac{DnV_L}{2f_s I_{ZVS}} = 93\,\mu\text{H}, \tag{7.4}$$

where the flat top duty cycle (3.4) has been used. This limit value for L_μ can be verified on the transformer built in Ch.4.2, using a different model represented in Fig.7.3. Knowing the parameters of the model in Fig.4.6, it's possible to extract the ones for this, using the following expressions:

$$\begin{cases} L_{\mu,eq} = L_{l2} + n^2 L_\mu = 79.1\,\mu\text{H}, \\ n_{eq} = \frac{L_{\mu,eq}}{nL_\mu} = 0.538, \\ L_{l,eq} = L_{l1} + L_\mu(1 - \frac{n}{n_{eq}}) = 3.1\,\mu\text{H}. \end{cases} \tag{7.5}$$

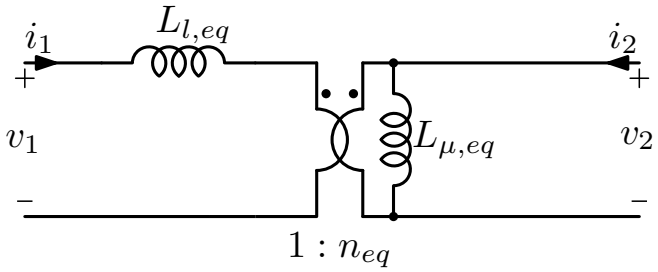


Figure 7.3: Transformer model.

As reported in (7.5) the magnetizing inductance is below the maximum value, so the transformer designed is suitable for this modification. Finally the new values for the currents at the commutation instants are reported in Fig.7.4 and a graphic expansion of the ZVS region can be seen in Fig.7.5.

7.2 Simulation verification

The circuit in Fig.7.1 has been implemented on the Simulink/PLECS environment. Fig.7.6 shows some waveforms at 250 W. As expected on the current $i_s - i_{L_\mu}$, which is the secondary side output current of the transformer, there is a triangular variation generated by L_μ, superimposed to the flat top current.

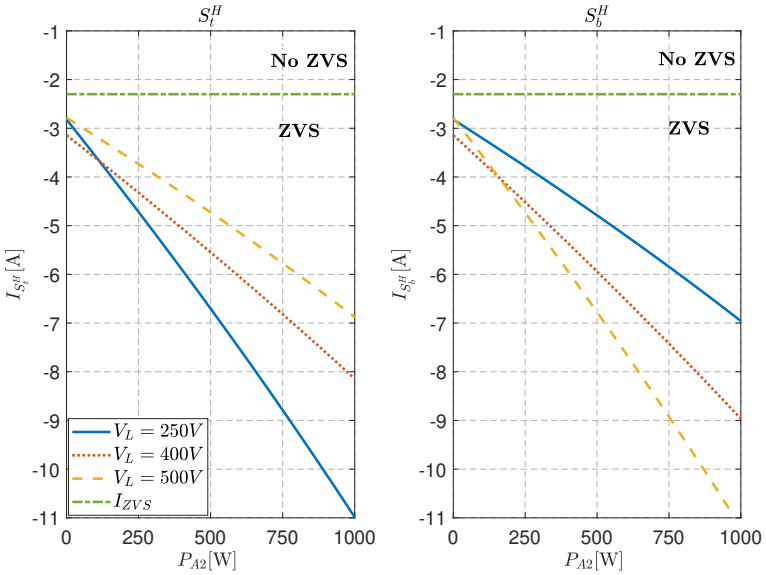


Figure 7.4: Currents through the switches at the commutation instants considering a magnetizing inductance of 79.1 µH at the secondary side and flat top operation.

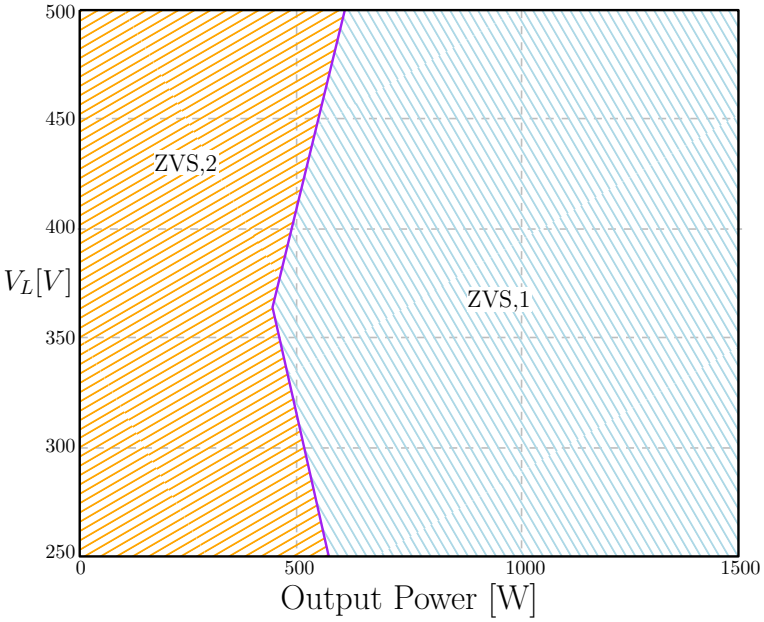


Figure 7.5: ZVS region for all switches. Original design: only ZVS,1 area; after the modification: ZVS,1 + ZVS,2 areas.

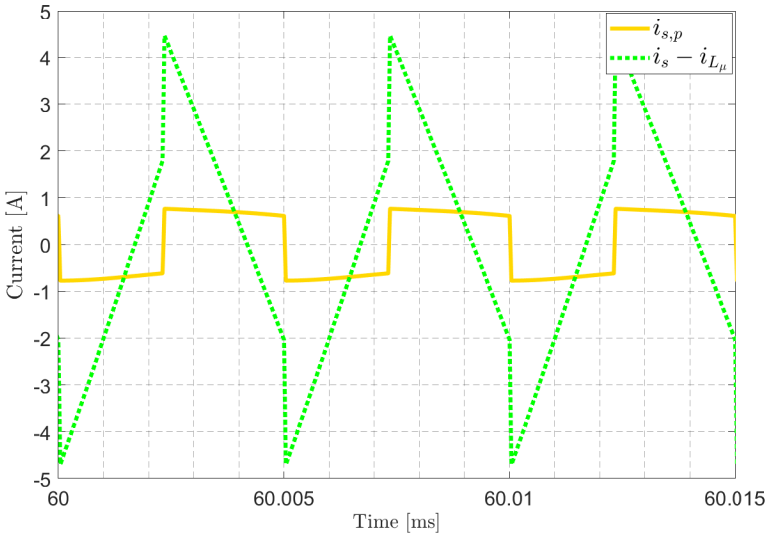


Figure 7.6: Simulation results at $V_L = V_H = 400\,\text{V}$ and $P_o = 250\,\text{W}$. Note that, with the modification, the flat top current is at the primary side ($i_{s,p}$).

Chapter 8

Conclusions and future developments

In conclusion the objective of this work was to analyze the CFDHB converter under three degrees of freedom. All the equations have been developed under a simplifying hypothesis of piece-wise linear current. Simulations and theoretical analysis coincide, if the voltage ripples on the capacitors are kept small. An experimental prototype, rated 2.5 kW, has been built for this experience. There are good matches between theoretical and experimental measurements, some differences are caused by voltage ripple on the capacitors, dead times and parasitic components, not considered in the analysis.

Future developments are possible, starting from the experimental verification of the proposed modification to extend the ZVS range. That was not done since the realization of the prototype has been very time consuming. A minimum current trajectory control can be studied, using all the three degrees of freedom. Further, a close loop control can be implemented, studying the small signal model of the converter. Fast tests are now possible on the prototype, and the code developed for the microcontroller can be used as a base to implement these controls.

Appendix A

Losses in an inductor/transformer winding employing Litz wire

A.1 Losses in a round conductor

Considering a round conductor, as represented in Fig.A.1, by solving the Maxwell equations it's possible to estimate the conductor losses due to skin and proximity effects.

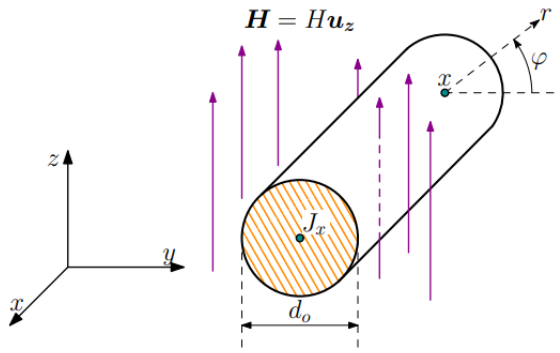


Figure A.1: Round conductor invested by an external magnetic field in z-direction. The conductor is infinitely long in x-direction.

A.1.1 Skin effect

The skin effect contribution has been calculated under the assumption of zero external magnetic field and sinusoidal quantities. The solution of the Maxwell equations brings to a differential equation as reported in (A.1).

$$\frac{d^2\dot{J}_x}{dr^2} + \frac{1}{r}\frac{d\dot{J}_x}{dr} = j\omega\mu\sigma\dot{J}_x \tag{A.1}$$

This is a standard form of a Bessel differential equation of order zero, which can be solved by looking at the generic solution of this kind, and imposing the right boundary conditions. Once the expression of $\dot{J}_x$ has been obtained, the conductor losses per unit length, due to the non uniform current distribution caused by the skin effect, can be calculated using the following expression:

$$P_C^{Skin} = \frac{1}{2\sigma}\int_0^{2\pi}\int_0^{r_0} \dot{J}_x\dot{J}_x^* r dr d\varphi = \frac{\left|\dot{I}_o\right|^2}{2\pi\sigma\delta d_o}\psi_1(\xi), \tag{A.2}$$

with

$$\xi = \frac{d_o}{\sqrt{2}\delta}, \tag{A.3}$$

$$\psi_1(\xi) = \frac{ber_0(\xi)bei_1(\xi) - ber_0(\xi)ber_1(\xi) - bei_0(\xi)bei_1(\xi) - bei_0(\xi)ber_1(\xi)}{ber_1^2(\xi) + bei_1^2(\xi)}. \tag{A.4}$$

Equation (A.2) can be rewritten taking into account the DC resistance per unit length, $r_{DC} = \frac{4}{\sigma\pi d_o^2}$, which results:

$$P_C^{Skin} = \frac{1}{2}r_{AC}\left|\dot{I}_o\right|^2 = \frac{1}{2}r_{DC}F_R\left|\dot{I}_o\right|^2, \tag{A.5}$$

where

$$F_R = \frac{\xi}{2\sqrt{2}}\psi_1(\xi). \tag{A.6}$$

In order to check the solution, at low frequency r_{AC} should be equal to r_{DC}, hence $F_R = 1$, from Fig.A.2 it's possible to see that.

The solution has been compared with the one proposed in [11] and reported in (A.7) for clarity ($F_{R,V}$: F_R coefficient obtained in [11]). Equation (A.7) seems differ from (A.5) by a $1/\sqrt{2}$ coefficient. But the two papers use two different definitions of $\psi_1(\xi)$. Indeed the one reported in [11] uses a definition of ber' and bei' which has been found in [12] and reported in (A.10) and (A.11). Using these definitions the two expressions bring the same F_R, as depicted in Fig.A.2.

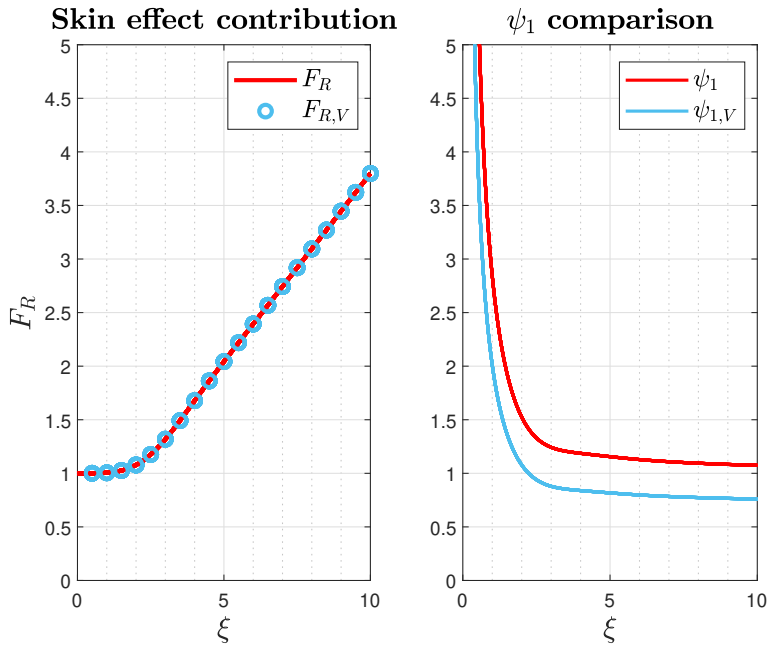


Figure A.2: Comparison between the solutions proposed in the two papers. Low ξ values means low frequency, considering constant the other quantities.

$$P_{C,V}^{Skin} = \frac{\left|\dot{I}_o\right|^2}{\sqrt{2}\pi\delta\sigma d_o}\psi_{1,V}(\xi) = \frac{1}{2}r_{DC}\frac{\xi}{2}\psi_{1,V}(\xi)\left|\dot{I}_o\right|^2 = \frac{1}{2}r_{DC}F_{R,V}\left|\dot{I}_o\right|^2 \tag{A.7}$$

$$\psi_{1,V}(\xi) = \frac{ber_0(\xi)bei_0'(\xi) - bei_0(\xi)ber_0'(\xi)}{ber_0'(\xi)^2 + bei_0'(\xi)^2} \tag{A.8}$$

$$F_{R,V} = \frac{\xi}{2}\psi_{1,V}(\xi) \tag{A.9}$$

$$ber_0'(x) = \frac{ber_1(x) + bei_1(x)}{\sqrt{2}} \tag{A.10}$$

$$bei_0'(x) = \frac{-ber_1(x) + bei_1(x)}{\sqrt{2}} \tag{A.11}$$

After some straightforward algebra it's possible to obtain the relation between the two $\psi_1(\xi)$:

$$\frac{\psi_1(\xi)}{\psi_{1,V}(\xi)} = \sqrt{2}. \tag{A.12}$$

A.1.2 Proximity effect

Considering again a round conductor invested by an uniform external magnetic field **H**, it's possible to obtain the power dissipation for unit length which is reported in the following expression:

$$P_C^{Proximity} = \frac{1}{2} r_{DC} G_R \left|\dot{H}\right|^2, \tag{A.13}$$

where

$$G_R = \frac{\xi \pi^2 d_o^2}{\sqrt{2}} \psi_2(\xi), \tag{A.14}$$

$$\psi_2(\xi) = \frac{ber_1(\xi)bei_2(\xi) - ber_1(\xi)ber_2(\xi) - bei_1(\xi)bei_2(\xi) - bei_1(\xi)ber_2(\xi)}{ber_0^2(\xi) + bei_0^2(\xi)}. \tag{A.15}$$

The result reported in (A.13) has been compared with the one reported in [11]. An error on the numerator of Eq.(30) of [11] has been found, indeed a term r_o has been omitted. After this correction and taking into account that $\psi_{2,V}(\xi)$ includes a factor $1/\sqrt{2}$, due to the use of (A.10) and (A.11), the two expressions are identical.

$$\frac{\psi_2(\xi)}{\psi_{2,V}(\xi)} = -\sqrt{2} \tag{A.16}$$

A.2 Losses in an inductor/transformer winding employing Litz wire

The estimation of the losses in windings which employ Litz wire follows the approach proposed in [11], which starts from the skin and proximity losses in round conductor, that have been calculated in (A.5) and (A.13).

The study has been done under some simplifying assumptions: the current will divide equally among the separate strands, the internal magnetic field created by the current has a component only along the φ direction, and the external magnetic field is supposed to have only a z-component. A graphic representation of the structure under analysis can be seen in Fig.A.3.

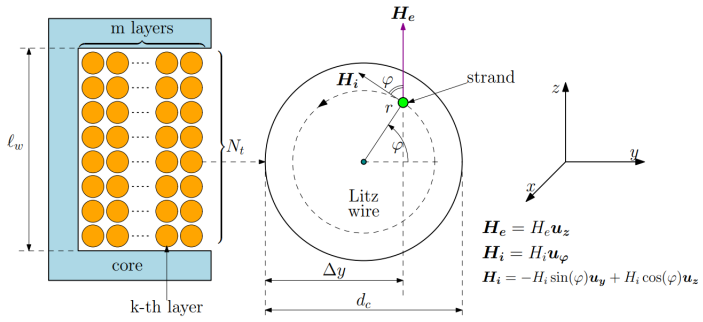


Figure A.3: Structure under analysis, one strand of the Litz wire highlighted. The conductor is infinitely long in x-direction.

Since in (1) of [11] has been found an error on the projection of the magnetic field on the reference axes, the procedure has been repeated step by step in order to check the final expression with the one reported in [13].

Let's start from the nomenclature used in the next expressions:

- N_t: Number of conductors in one layer
- N_s: Number of strands in a conductor
- m: Number of layers
- r_c: Ray of a conductor
- r_o: Ray of a strand
- l_w: Core window length
- $\delta = \frac{1}{\sqrt{\pi \sigma f \mu_0}}$

- $\xi = \frac{d_o}{\sqrt{2}\delta}$

The DC resistance per unit of length reported in (A.17) has been used as a normalization factor for the AC resistance.

$$r_{DC} = \frac{N_t m}{N_s \sigma \pi r_o^2} \tag{A.17}$$

Knowing all the parameters it's possible to calculate the ratio between the AC and DC resistance with the expression proposed in [13], and reported here:

$$F_R = \frac{\xi}{2\sqrt{2}}\Big\{\psi_1(\xi) + \Big[\frac{8N_s^2\pi^2 r_o^2 N_t^2 m^2}{3l_w^2} + N_s^2\frac{r_o^2}{r_c^2}\Big(1 - \frac{\pi^2 r_c^2 N_t^2}{6l_w^2} + \frac{\pi r_c N_t}{l_w}\Big)\Big]\psi_2(\xi)\Big\}, \tag{A.18}$$

where $\psi_1(\xi)$ and $\psi_2(\xi)$ are (A.4) and (A.15) respectively.

So the AC resistance is:

$$r_{AC} = r_{DC} F_R. \tag{A.19}$$

At this point (A.18) has been compared with the expression of F_R from [11] (which is identified by K_d in the paper, Eq.(23)) under the same hypothesis, namely:

- $\beta = N_s\big(\frac{r_o}{r_c}\big)^2$;
- $l_w = 2r_c N_t$.

After some straightforward algebra and taking into account (A.12) and (A.16) the two expressions are identical, except for a term $\frac{12}{\pi}$, which is not present in [11]. But, using the right projection of the magnetic field on the reference axes and repeating all the procedure, this term appears also in [11] and the final expression coincides with (A.18). So, under the above hypothesis the corrected expression in [11] is:

$$F_R = \frac{\xi}{2}\Big[\frac{\psi_1(\xi)}{\sqrt{2}} + \frac{\pi^2 N_s \beta}{24}\Big(16m^2 - 1 + \frac{24}{\pi^2} + \frac{12}{\pi}\Big)\frac{\psi_2(\xi)}{\sqrt{2}}\Big] \tag{A.20}$$

So the two expressions, after the corrections, are identical, but the one proposed in [13], (A.18), is more general, so this will be the reference equation for the estimation of the losses in a Litz wire.

Appendix B

Digital control implementation

The topology studied in this work has been controlled using the TMS320F28379D microcontroller (uC) from Texas Instruments (TI). It's very powerful and has some peripherals useful in the control of power electronic converters. A custom board has been designed, in order to rise the signal levels from the uC and have better cable managing, employing flat cables. This board can be seen in Fig.B.1, which hosts the development board from TI.

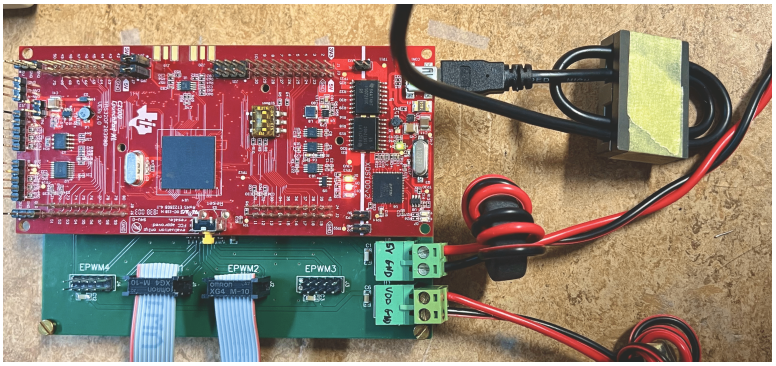


Figure B.1: uC board used during the experience. Note the presence of some ferrites against the uC disconnection during tests.

B.1 Control signals generation

The software implemented uses the enhanced Pulse Width Modulator peripheral (ePWM) to generate the control signals for each switch in Fig.2.1. The ePWM is organized in different sub-modules (ePWMx) capable to generate two signals each: ePWMxA and ePMWxB. Each ePWMx can be configured independently from the others, for frequency, duty cycles and dead times. A simplified structure can be seen in Fig.B.2, where the fundamental blocks and registers have been

reported, in order to understand the basic functionality. The operation is very

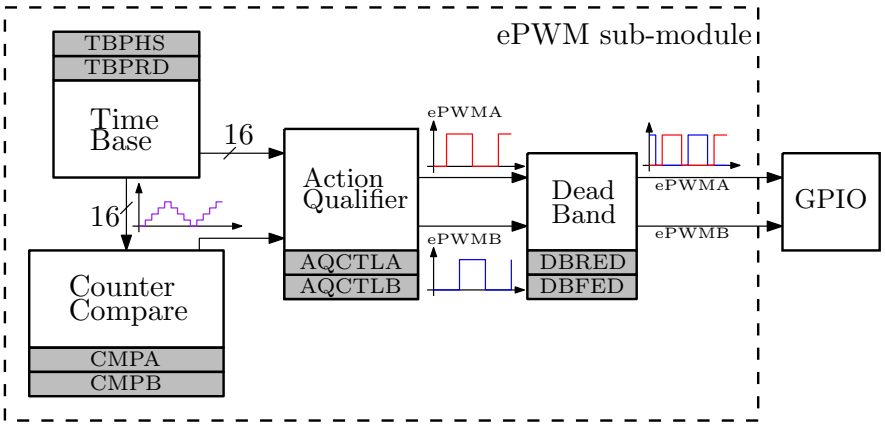


Figure B.2: Simplified block diagram of each ePWM sub-module. Some fundamental registers have been reported on the figure. The complete structure can be seen on [14]

simple and will be explained in the following. The Time Base (TB) implements a double ramp counter, which starts from zero to TBPRD. The counter value is compared with some thresholds, defined into the Counter Compare: CMPA and CMPB. When this thresholds have been reached, some impulses will be sent to the Action Qualifier, which pull up or down, in a configurable manner, the signals A and B. Finally, the Dead Band introduces the dead time selected by the programmer. For this specific case, ePWMxA control the low side devices of Fig.2.1. Signals A and B are complementary, namely one is the negative version of the other, this was implemented using CMPA=CMPB, and programming opposite actions from the Action Qualifier. The PWM period (T_{PWM}) and the duty cycles can be computed using the following expressions:

$$T_{PWM} = 2(\text{TBPRD})T_{TBCLK}, \tag{B.1}$$

$$D_b = \frac{t_b}{T_{PWM}} = 1 - \frac{\text{CMPA}}{\text{TBPRD}} - \frac{t_{dead}}{T_{PWM}}, \tag{B.2}$$

$$D_h = \frac{t_h}{T_{PWM}} = 1 - \frac{\text{CMPA}}{\text{TBPRD}} - \frac{t_{dead}}{T_{PWM}}, \tag{B.3}$$

where T_{TBCLK} is the clock provided to the TB. A representative behaviour can be seen in Fig.B.5.

The idea is to control each leg of Fig.2.1 with a sub-module, synchronizing the two to obtain the desired phase shift. This can be implemented through an hardware synchronization, available on the peripheral. Each sub-module has a synchronization input (SYNCI) and output (SYNCO), so a synchronization path can be configured from a master to a slave. In this specific case, ePWM1 is the

master, which generates an impulse when the counter reaches zero. This impulse is propagated to the SYNCI of ePWM2 which loads the counter with the value in the phase register (TBPHS). This behaviour is represented in Fig.B.3. The phase shift between the two counters is also the phase shift with respect the center points, as defined in Ch.2, and can be calculated using the following expression:

$$D_\Phi = \frac{t_\Phi}{T_{PWM}} = \frac{\text{TBPHS}}{2(\text{TBPRD})}. \tag{B.4}$$

Finally an example of waveforms taken from the uC can be seen in Fig.B.4.

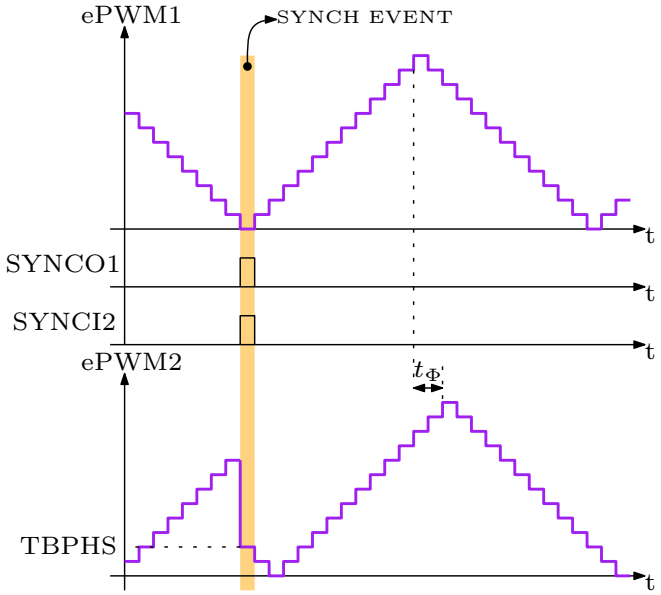


Figure B.3: Detailed representation on the synchronization event. Note that after the synch event the ePWM2 counter counts down, to implement a positive phase shift as defined in Ch.2. For a negative one it counts up.

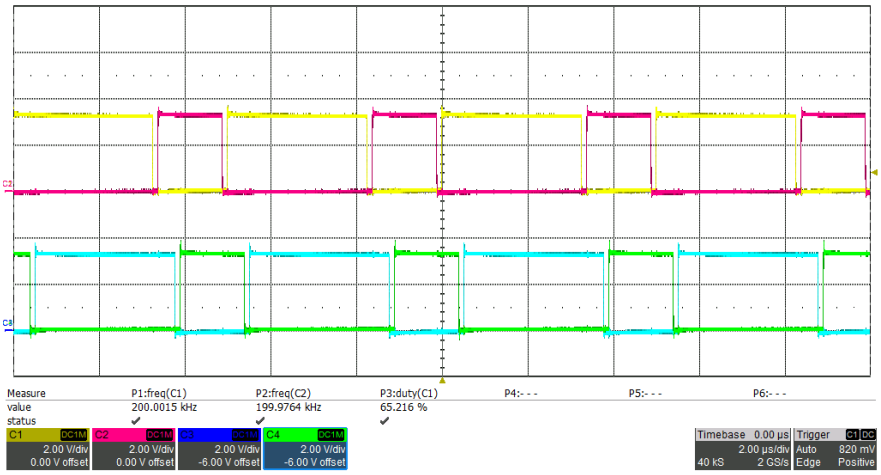


Figure B.4: Control signals generated from the uC considering CMPA/B=81, TBPHS=50, TBPRD=250, $T_{PWM} = 5\,\mu s$ and 120 ns of dead time.

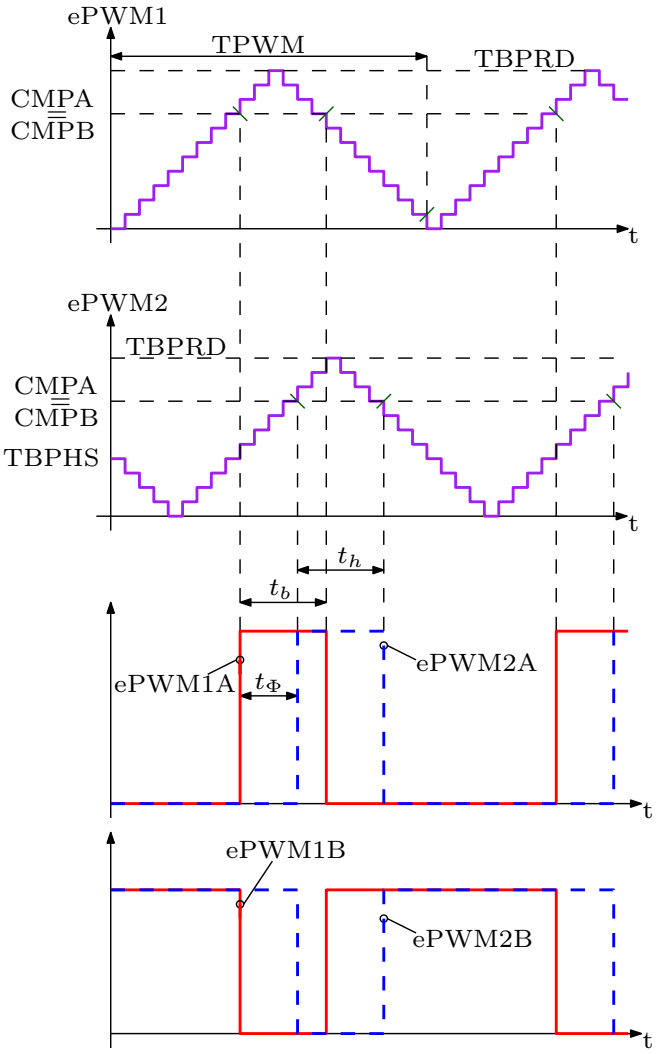


Figure B.5: Representative waveforms generated by the peripheral. Dead time has been omitted.

B.2 ePWM initialization

This section contains the code used to initialize the ePWM peripherals.

```
/*
 * EPWM_Init.h
 *
 *  Created on: Luglio 2023
 *  Author: Mirco Marcazzan
 */

#ifndef EPWM_INIT_H_
#define EPWM_INIT_H_

#include "F28x_Project.h"
#include "driverlib.h"
#include "device.h"

/*
 * Constant definition for ePWM
 * TBCLK=EPWMCLK=100MHz
 */
#define EPWM1_TIMER_TBPRD_200_KHZ 250//TBPRD to have 200kHz with
   up-down counter mode
#define DB_120_NS 12//120ns dead time
#define D_65 81//Value to implements 65% of duty-cycle

/*EPWM1 initialization*/
void initEPWM1();

/*EPWM2 initialization*/
void initEPWM2(void);

/*ePWM GPIO initialization*/
void initEPWMGPIO(void);

#endif /* EPWM_INIT_H_ */
```

Listing B.1: Header file for the ePWM initialization.

```
/*
 *  EPWM_Init.c
 *  Created on: July 2023
 *  Author: Mirco Marcazzan
 *  This file contains the initialization functions for the ePWM1
```

```
 *  the ePWM2, and for the GPIO pins.
 */

#include "F28x_Project.h"
#include "driverlib.h"
#include "device.h"
#include "EPWM_Init.h"

/*
 * ePWM1 initialization
 */
void initEPWM1(){
    /*Setup Time base Tpwm [s] =2*TBPRD*T_TBCLK [s]*/
    EPwm1Regs.TBPRD = EPWM1_TIMER_TBPRD_200_KHZ;//Timer period
   for 200kHz
    EPwm1Regs.TBPHS.bit.TBPHS = 0x0000;//Phase is 0
    EPwm1Regs.TBCTR = 0x0000;//Clear counter
    EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;//Count up and
   down
    EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;//Disable phase
   loading
    EPwm1Regs.TBCTL.bit.PHSDIR=TB_UP;//Count up on synch event
    EPwm1Regs.TBCTL.bit.PRDLD=TB_SHADOW;//Shadow mode enabled for
    period register

     /* Time base clock: TBCLK=EPWM_CLOCK/(HSPCLKDIV*CLKDIV)*/
    EPwm1Regs.TBCTL.bit.CLKDIV=TB_DIV1;// Division factor: 1
    EPwm1Regs.TBCTL.bit.SYNCOSEL=TB_CTR_ZERO;//Output sync signal
    on TBCTR=0
    EPwm1Regs.TBCTL.bit.HSPCLKDIV=TB_DIV1;// Division factor: 1

    /*Set Counter-Compare submodule*/
    EPwm1Regs.CMPA.bit.CMPA = EPWM1_TIMER_TBPRD_200_KHZ>>1;// Set
    compare A value
    EPwm1Regs.CMPB.bit.CMPB = EPWM1_TIMER_TBPRD_200_KHZ>>1;// Set
    Compare B value
    EPwm1Regs.CMPCTL.bit.SHDWAMODE=CC_SHADOW;//Shadow mode
   enabled for COMPA
    EPwm1Regs.CMPCTL.bit.LOADAMODE=CC_CTR_ZERO;//Load from shadow
    when CTR=Zero
    EPwm1Regs.CMPCTL.bit.SHDWBMODE=CC_SHADOW;//Shadow mode
   enabled for COMPB
    EPwm1Regs.CMPCTL.bit.LOADBMODE=CC_CTR_ZERO;//Load from shadow
    when CTR=Zero
```

```
39
40      /*Set Action Qualifier*/
41      EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;//Set PWM1A on event TBCTR
    ==COMPA, up count
42      EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;//Clear PWM1A on event
    TBCTR==COMPA, down count
43
44      EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;//Complementary signal
45      EPwm1Regs.AQCTLB.bit.CBD = AQ_SET;
46
47      /*Dead-band submodule*/
48      EPwm1Regs.DBCTL.bit.OUT_MODE=DBB_ALL;//Complete enabled
49      EPwm1Regs.DBCTL.bit.POLSEL=DB_ACTV_HIC;//Active High
    complementary
50      EPwm1Regs.DBCTL.bit.DEDB_MODE=0;//Active High complementary
51
52      /*Dead time configuration: Tdead= DBFED * T_TBCLK (Also for
    DBRED)*/
53      EPwm1Regs.DBRED.bit.DBRED=DB_120_NS;//Dead time duration 120
    ns on rising edge
54      EPwm1Regs.DBFED.bit.DBFED=DB_120_NS;//Dead time duration 120
    ns on falling edge
55
56      /*Bypass the chopper submodule*/
57      EPwm1Regs.PCCTL.bit.CHPEN=0;
58
59      /*Interrupt configuration*/
60      EPwm1Regs.ETSEL.bit.INTEN=1;//Enable Interrupt generation
61      EPwm1Regs.ETSEL.bit.INTSEL=0b010;//Interrupt generated when
    TBCTR=TBPRD
62      EPwm1Regs.ETPS.bit.INTPRD=0b01;//Interrupt generated at the
    first event
63      EPwm1Regs.ETCLR.bit.INT = 1;//Clear the interrupt flag
64
65      return;
66  }
67
68  /*
69   * ePWM2 initialization
70   */
71  void initEPWM2(void){
72
73      /*Setup Time base Tpwm [s] =2*TBPRD*T_TBCLK [s]*/
74      EPwm2Regs.TBPRD = EPWM1_TIMER_TBPRD_200_KHZ;//Timer period
```

```
   for 200kHz
75  EPwm2Regs.TBPHS.bit.TBPHS = 0x0000;//Phase is 0
76  EPwm2Regs.TBCTR = 0x0000;//Clear counter
77  EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;//Count up and
   down
78  EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;//Enable phase loading
79  EPwm2Regs.TBCTL.bit.PHSDIR=TB_DOWN;//Count down on synch
   event
80  EPwm2Regs.TBCTL.bit.PRDLD=TB_SHADOW;//Shadow mode enabled for
    period register
81
82  /* Time base clock: TBCLK=EPWM_CLOCK/(HSPCLKDIV*CLKDIV)*/
83  EPwm2Regs.TBCTL.bit.CLKDIV=TB_DIV1;//Division factor: 1
84  EPwm2Regs.TBCTL.bit.HSPCLKDIV=TB_DIV1;//Division factor: 1
85  EPwm2Regs.TBCTL.bit.SYNCOSEL=TB_SYNC_IN;//SYNCI as synch
   events
86
87  /*Set Counter-Compare submodule*/
88  EPwm2Regs.CMPA.bit.CMPA = EPWM1_TIMER_TBPRD_200_KHZ>>1;// Set
    compare A value
89  EPwm2Regs.CMPB.bit.CMPB = EPWM1_TIMER_TBPRD_200_KHZ>>1;// Set
    Compare B value
90  EPwm2Regs.CMPCTL.bit.SHDWAMODE=CC_SHADOW;//Shadow mode
   enabled for COMPA
91  EPwm2Regs.CMPCTL.bit.LOADAMODE=CC_CTR_ZERO;//Load from shadow
    when CTR=Zero
92  EPwm2Regs.CMPCTL.bit.SHDWBMODE=CC_SHADOW;//Shadow mode
   enabled for COMPB
93  EPwm2Regs.CMPCTL.bit.LOADBMODE=CC_CTR_ZERO;//Load from shadow
    when CTR=Zero
94
95  /*Set Action Qualifier*/
96  EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;//Set PWM1A on event TBCTR
   ==COMPA, up count
97  EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR;//Clear PWM1A on event
   TBCTR==COMPA, down count
98
99  EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;//Complementary signal
100 EPwm2Regs.AQCTLB.bit.CBD = AQ_SET;
101
102 /*Dead-band submodule*/
103 EPwm2Regs.DBCTL.bit.OUT_MODE=DBB_ALL;//Active High
   complementary dead band
104 EPwm2Regs.DBCTL.bit.POLSEL=DB_ACTV_HIC;//Active High
```

```
    complementary dead band
105     EPwm2Regs.DBCTL.bit.DEDB_MODE=0;//Active High complementary
    dead band
106
107     EPwm2Regs.DBRED.bit.DBRED=DB_120_NS;//Dead time duration 60ns
     on rising edge
108     EPwm2Regs.DBFED.bit.DBFED=DB_120_NS;//Dead time duration 60ns
     on falling edge
109
110     /*Bypass the chopper submodule*/
111     EPwm2Regs.PCCTL.bit.CHPEN=0;
112
113     return;
114 }
115
116 /*
117  * GPIO initialization
118  */
119 void initEPWMGPIO(void)
120 {
121     EALLOW;
122     /*GPIO0 -> EPWM1A configuration*/
123     GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;//Disable pull-up on GPIO0
124     GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;//Configure GPIO0 as
    EPWM1A
125     GpioCtrlRegs.GPADIR.bit.GPIO0 = GPIO_OUTPUT;//Configure GPIO0
     as OUTPUT
126
127     /*GPIO1 -> EPWM1B Configuration*/
128     GpioCtrlRegs.GPAPUD.bit.GPIO1=1;//Disable pull-up on GPIO1
129     GpioCtrlRegs.GPAMUX1.bit.GPIO1=1;//Configure GPIO1 as EPWM1B
130     GpioCtrlRegs.GPADIR.bit.GPIO1 = GPIO_OUTPUT;// Configure
    GPIO1 as OUTPUT
131
132
133     /*GPIO2 -> EPWM2A configuration*/
134     GpioCtrlRegs.GPAPUD.bit.GPIO2=1;//Disable pull-up on GPIO2
135     GpioCtrlRegs.GPAMUX1.bit.GPIO2=1;//Configure GPIO1 as EPWM2A
136     GpioCtrlRegs.GPADIR.bit.GPIO2= GPIO_OUTPUT;//Configure GPIO2
    as OUTPUT
137
138     /*GPIO3 -> EPWM2B configuration*/
139     GpioCtrlRegs.GPAPUD.bit.GPIO3=1;//Disable pull-up on GPIO2
140     GpioCtrlRegs.GPAMUX1.bit.GPIO3=1;//Configure GPIO3 as EPWM2B
```

```
141     GpioCtrlRegs.GPADIR.bit.GPIO3 = GPIO_OUTPUT;// Configure
        GPIO3 as OUTPUT
142
143     /*GPIO pin as output*/
144     GpioCtrlRegs.GPBMUX2.bit.GPIO61=0;//This ensure that this pin
        is a simple GPIO, not a peripheral GPIO
145     GpioCtrlRegs.GPBDIR.bit.GPIO61=1;//Pin as output (BLUE LED)
146
147     EDIS;
148     return;
149
150 }
```

Listing B.2: Implementation of the header.

Appendix C

C.1 Calculation of the initial currents

In this section the equation (2.2) and the expressions for the initial current in each sub-interval will be derived. The simplified circuit in Fig.2.2 will be considered, to have constant voltages applied to the energy transfer impedance (L_s) and thus piece-wise linear currents. Let's assume to work in steady state condition. The charge balance on the capacitor legs imposes an average current equal to zero. Under this hypothesis a generic current waveforms, in normalized form, can be seen in Fig.C.1, where $J_0 = J_4$ is imposed by the steady state condition.

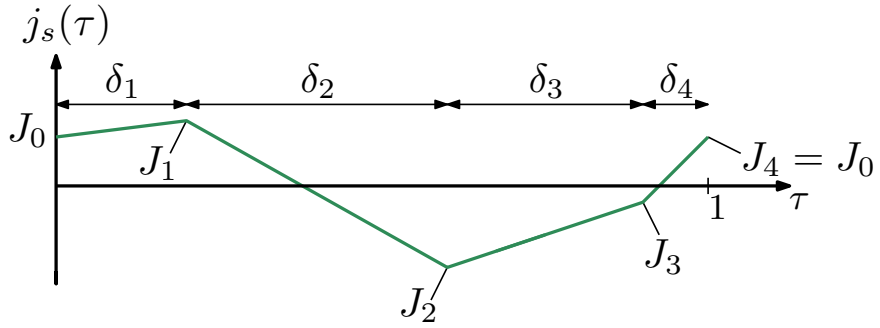


Figure C.1: Generic steady state normalized current waveforms, $\tau = t/T_N$. Each interval (δ_k) corresponds to a different state of the switches in Fig.2.1.

Let's calculate the mean value of j_s in a switching period:

$$\bar{j_s} = \int_0^1 j_s(\tau)d\tau = \frac{\delta_1(J_0 + J_1)}{2} + \frac{\delta_2(J_1 + J_2)}{2} + \frac{\delta_3(J_2 + J_3)}{2} + \frac{\delta_4(J_3 + J_4)}{2}. \quad \text{(C.1)}$$

Since $j_s(\tau)$ is piece-wise linear, the initial currents (J_k) can be calculated in this way:

$$J_k = J_{k-1} + m_k\delta_k \quad k = 1, 2, 3, \quad \text{(C.2)}$$

where m_k is the normalized current slope inside the interval δ_k. Substituting

(C.2) into (C.1), and applying straightforward algebra, it's possible to rewrite the expression of the mean value:

$$\bar{j_s} = J_0 + \frac{1}{2}\Big(m_1\delta_1(1+\delta_2+\delta_3) + m_2\delta_2(1-\delta_1+\delta_3) + m_3\delta_3(1-\delta_1-\delta_2)\Big). \quad \text{(C.3)}$$

The normalized current slope can be calculated in this way:

$$m_k = \frac{V_{Lk}}{L_s}\frac{T_s}{I_N} = 2\pi U_{Lk} \quad k = 1,2,3,4, \quad \text{(C.4)}$$

where U_{Lk} is the normalized voltage applied to L_s, inside the interval δ_k. At this point, imposing (C.3) equal to zero and using (C.4), it's possible to determine J_0:

$$J_0 = -\pi\big[U_{L1}\delta_1(1+\delta_2+\delta_3) + U_{L2}\delta_2(1-\delta_1+\delta_3) + U_{L3}\delta_3(1-\delta_1-\delta_2)\big]. \quad \text{(C.5)}$$

C.2 Calculation of the power expression

In this section the power expression of the operating region R1 will be derived in detail. The analysis herein uses the hypothesis of C.1, since the expression of J_0 will be used. The active power can be calculated using (2.5), in normalized form results:

$$\Pi_{A1} = \sum_{k=1}^{4} U_{Ak}\frac{\delta_k}{2}(J_{k-1} + J_k) \quad \text{(C.6)}$$

where U_{Ak} is the normalized voltage of the generator $v_a(t)$ (Fig.2.2) inside the interval δ_k. In particular, in region R1, $U_{Ak} = -nU_L$ for k=1,2,3 and $U_{Ak} = nU_L\frac{D_b}{1-D_b}$ for k=4.

Let's compute J_0 using (2.2), Tab.2.2 and Tab.2.4, which results:

$$J_0 = \pi[nU_L D_b + D_b D_h + 2D_\phi D_h - D_h]. \quad \text{(C.7)}$$

Since the current is assumed piece-wise linear the normalized current values J_k, for k=1,2,3,4, can be calculated using (2.3) and result:

$$J_1 = \pi[nU_L D_h - D_h - 2nU_L D_\phi + D_h^2] \quad \text{(C.8)}$$

$$J_2 = \pi[D_h - nU_L D_h - 2nU_L D_\phi - D_h^2] \quad \text{(C.9)}$$

$$J_3 = \pi[D_h - nU_L D_b - D_b D_h + 2D_\phi D_h] \quad \text{(C.10)}$$

At this point can be useful to calculate J_4 using again (2.3). The result should

be $J_4 = J_0$, imposed by the steady state condition, otherwise there is an error somewhere.

At this point using (C.8), (C.9), (C.10), Tab.2.2 and some straightforward algebra, it's possible to evaluate (C.6), which results:

$$\Pi_{A1} = n\pi U_L 2 D_h D_\phi. \tag{C.11}$$

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