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A Novel Approach for Single-Source 3-Phase 7-level Boost Inverter

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Abstract—In this article, a 3-phase inverter with a voltage gain of three demonstrated via the toggle capacitor concept.*It synthesizes a line voltage waveform with seven levels. The most salient feature of this topology is that a single input DC locate is* necessaryfor *the 3-phase implementation.Each branch of the proposed topology requires eight power electronics switches and 2condenser. The opposite of the current reach their highest across the energyoutlet is equal to the value of the input DC voltage. The capacitors are all self-balanced at all modulation indices. The proposed approach minimizes the cost function to 5.429, as the proposed topology exhibits better topological characteristics mainlythe boosting-factor, overall-voltage and component..Topology with similar features, however, has a const function of 7.333. In addition, the suggested topology is highly modular, so the amount of pole energyscalescould be increased by further adding switched capacitors, and the same arm structures can be used for all phases. However, an important limitation is that the pole voltage is unipolar, and therefore redundant states in phase are not available, although they are readily available in line voltage. The 7-level topology and modulation procedure are verified by result discussion, which represents that with a DC energy of 100 V, a 3-phase voltage with about 300 V could be obtained in equal steps of 100 V, while the pole voltage is a unipolar 4-level peak value 300V in equal steps of 100V.*

Keywords-Multilevel convertor, switched-condenser, energy boosting, self-balancing**.**

I. INTRODUCTION

Multilevel convertorare employed innumerous applications [1-2] as theyoffersuperior features such as: low peak-inverse-voltage stress on the power switches, reduced total harmonic distortion(THD) and better harmonic profile, low dv/dt stresses on the power switches and the load, reduced filtering requirement, high modularity, possibility of programming fault tolerant operation, easy integration of multiple energy sources and so on [3]. Many tradional sources, like arrays, air turbines, and cells, are now being employed for the generation of electrical power. However, the amount of electricity accessible from these sources is restricted [4] and they may fail to fulfill the power quality requirements of several applications. With such sources as photovoltaic panels and fuel cells, a voltage boost is also required. To achieve a desirable boosting, a dc-dc converter with a normal MLI or a load-end transformer are common solutions [5-6]. These solutions, however, cause increased losses and add to the volume of the system.

The three basic MLI structures, which are considered to be conventional topologies are:clamped multilevel converters, cascaded H-bridge multilevel device and the flying capacitors multilevel converters. These topologisare characterized by their respective pros and cons for various applications. As an example, the modular cascaded H-bridge requires several dc energy which is essential to be galvanically isolated.The capacitors used in the diode-clampted and flying capacitors multilevel structures are difficult to balance.

This work focuses on a new class of MLIs, known as 'switched capacitors based MLIs (SCMLIs)'. The SCMLIs can boost the voltage, offer self-balancing of capacitors' voltage, and effectively extend the number of levels due to their flexibility. The topologies discussed in [6-7] are based on the switched-capacitors principle and offer high modularity. However, the high peak-inverse-voltage on the semiconductor power switches limits the application of these topologies. The topology proposed in [8] shows utilizes a basic cell which creates a waveform with seven levelsof output voltage. While the structure manifests modularity, it is more costly and less attractive due to the presence of multiple input dc sources and polarity reversal with the application of H-bridge power electronics device with inverse energy at highest. The SCMLIs presented in [12-14] offer low voltage gain even though they require high module count (mainly of powerdevices).

Another approach to obtain a seven-level waveformis discussed in [16], though the voltage-gain is less than one and requirement of power semiconductor devices is indeed high. Topology presented in [17] generates seven the amount using a three-volt acquire, although the structure places the switches under high voltage stress. In the multilevel inverters discussed in [9-11],[15], the voltage-gain is low. Hence, based on this discussion, most topologies have several drawbacks, including morenumber of switching devices, more peak-inverse-voltage on the power switches and low value of overall voltage-gain.

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Therefore, The purpose of this investigation is to advance a new topology that has the following characteristics:

a) It generates a seven-level waveform.
b) It offers an overall voltage-gain equal to three.
c) It offers self-balancing of the voltages of the topology's employed switched-condenser.
d) It requires less number of devices.
e) It requires just one power source to synthesize three-phase voltages.

II. PROPOSED TOPOLOGY

A. Proposed Structure:

Figure.1 shows the suggested tripartite structure based on the switched-capacitors principle. Each phase of the proposed inverter comprises eight number of semiconductorpower switches S_{Xi} (i = 1, 2...,8) and two switched capacitors ($C_{X1}$and C_{X2}), where X ∈(a, b, c). The three-phase inverter requires a single dc voltage source.

For each of the phase, the pole voltage is shown as$V_{Xo}(t)$, wherein X = a,b,c, and the proposed topology can synthesize four levels as the pole voltage viz. 0, $+V_{DC}, +2V_{DC}, +3V_{DC}$. As a result, the line voltage waveform would have seven levels viz. 0, $\pm V_{DC}, \pm 2V_{DC}, \pm 3V_{DC}$. Table I summarises the valid switching states for one of the legs (say leg 'a'). The switching states for the leg 'a' are discussed here, and it follows that the other legs operate in a similar fashion.

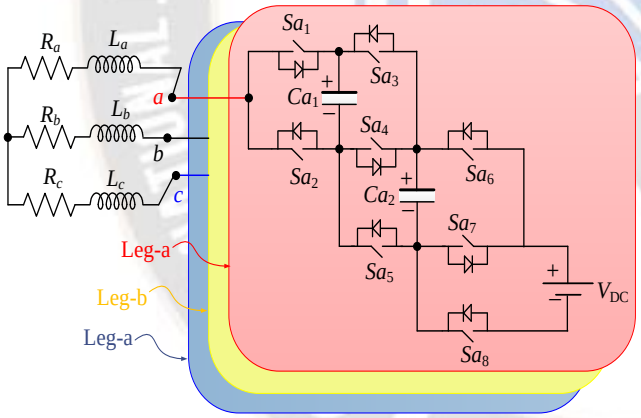


Fig.1 circuitof the 3-phase multilevel topology proposed inthis work based on switched capacitors

B. Switching states for the leg 'a'

Table 1: Switching statesfortheleg 'a'

State	State of the Semiconductor Power Switches (1=ON, 0=OFF)								$V_{ao}(t)$
	Xa1	*Xa2*	*Xa3*	*Xa4*	*Xa5*	*Xa6*	*Xa7*	*Xa8*	
1	0	1	1	0	1	1	0	1	0
2	1	0	1	0	1	1	0	1	V_{DC}
3	1	0	0	1	0	1	0	0	$2V_{DC}$
4	1	0	0	1	0	0	1	0	$3V_{DC}$

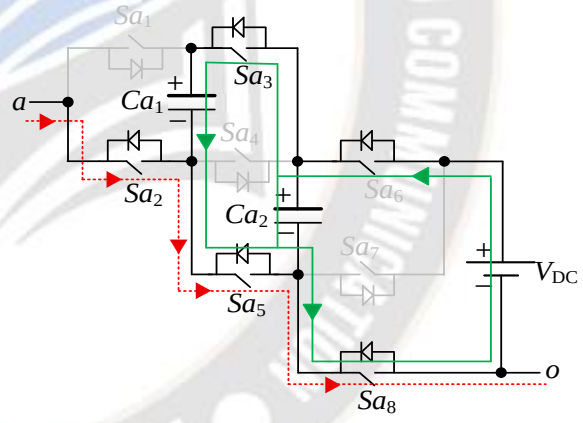
In this description, the capacitor charging path is shown by 'green' and current path by 'red' dotted line in Figure.2. The following outlines the switched-phase:

State 1: $\mathbf{V_{ao}(t) = 0}$ the pole voltage is equal to zeroby turning ON powerswitches S_{2a}, S_{3a}, S_{5a}, S_{6a}, and S_{8a}simultaneously and turning OFF S_{1a}, S_{4a}, and S_{7a}. As a result, the capacitors C_{1a}, and C_{2a}comeidentical to the DC power origin input, and hence C_{1a} and C_{2a} get charged to voltage V_{DC}. The outputpolevoltage ($V_{ao}(t)$) is 0.

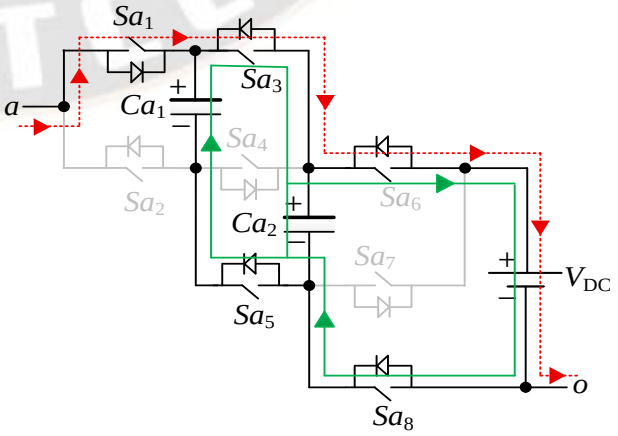
State 2: $\boldsymbol{V_{ao}(t) = V_{DC}}$ This state comes to force when the power switches S_{1a}, S_{3a}, S_{5a}, S_{6a}, and $S_{8a}$are turned ON simultaneously and the power switches S_{2a}, S_{4a}, and $S_{7a}$are turned OFF As a result, the capacitors C_{1a}, and C_{2a}come in parallel with the input dc voltage source, and hence C_{1a} and C_{2a} get charged to voltage V_{DC}. The resultantpole energy ($V_{ao}(t)$) is V_{DC}.

State 3: $\boldsymbol{V_{ao}(t) = 2V_{DC}}$ This state comes to force when the power switches S_{1a}, S_{4a},and $S_{6a}$are turned ON simultaneously and the power switches S_{2a}, S_{3a}, S_{5a}, S_{7a}, and $S_{8a}$are turned OFF. As a result, the capacitors C_{1a} get discharged. During this state, the output pole voltage ($V_{ao}(t)$) is $2V_{DC}$.

State 4: $\boldsymbol{V_{ao}(t) = 3V_{DC}}$ This state comes to force when the power switches S_{1a}, S_{4a},and $S_{7a}$are turned ON simultaneously and the power switches S_{2a}, S_{3a}, S_{5a}, S_{6a}, and $S_{8a}$are turned OFF (as depicted in Fig.2d). As a result, the capacitors C_{1a} and C_{2a} get discharged. During this state, the output pole voltage ($V_{ao}(t)$) is $3V_{DC}$.



(a)



(b)

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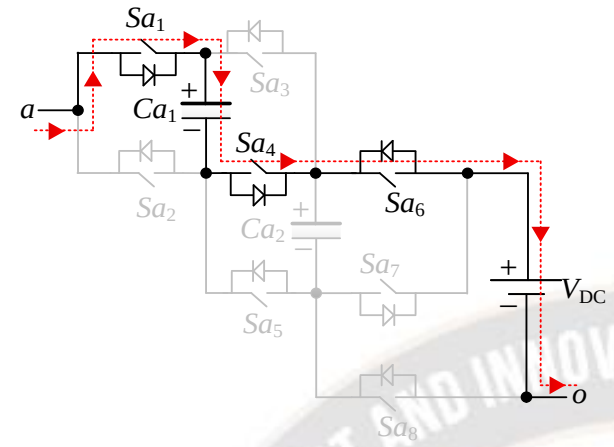

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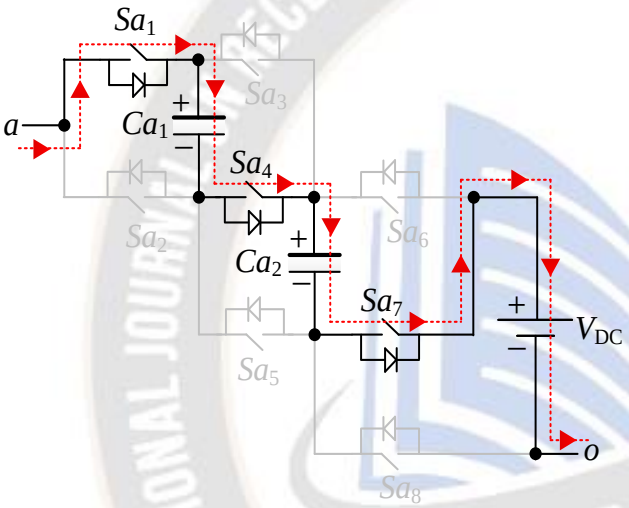

(d)

Fig. 2 Conductingand charging paths forvarious switching states of one leg of the proposed inverter

It is worth mentioning at this point that the SCMLIs is beingexamined on the basis ofcost function [12,14] described as:

$$CF = \left(\frac{N_{IS}}{N_L}\right) * \left\{N_S + N_D + N_{AD} + N_{GD} + N_C + \left(\frac{\alpha * TSV}{\beta}\right)\right\} \quad (1)$$

Where, CF is the cost function, N_s, N_D, N_{AD}, N_{GD} and N_C are number of sources, The amount of gate drivers, the amount of condensers, the amount of diodes, and the amount of additional diodes respectively, while TSV is the total standing voltage. Thus, based on these parameters, the CF of the proposed topology is 5.429, whereas with similar topological features (such as the topology proposed in [21]), CF of that topology is 7.333. The proposed topology, therefore, manifests better topological features.

III. SCHEME OF MODULATION

Gate pulses for multilevel converters have been created using a variety of transmission techniques. The following are

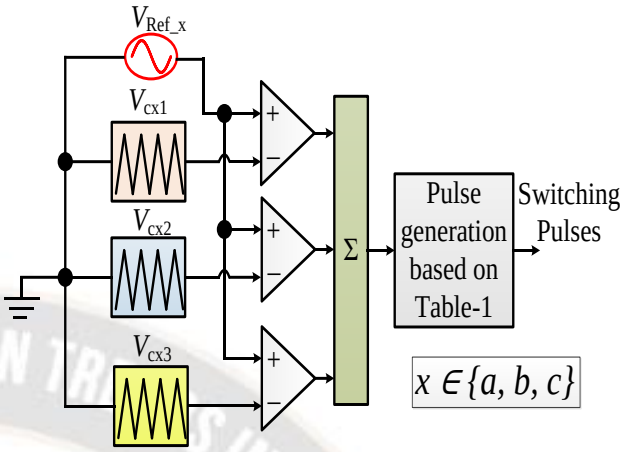

Fig.3 Level-shifted carriers based modulation procedure for the phase 'x' of the proposed inverter

some of the commonly used techniques within these processes: (1) multi-carrier pulse width modulation (PWM); (2) spatial vector PWM; (3) space vector control; and (4) selective harmonic elimination (SHE). The final two techniques are low switching frequency techniques, while the initial two are high-switching frequency techniques [18–20]. This work uses a carrier level shifted pulse width modulation (LS-PWM) approach to generate gate signals for the proposed SCMLI.

Modulation procedure for the suggested three-phase 7 stagesconvertor is depicted in Figure. 3. In this procedure, three bearer signals with the identical amplitude and switching are continuously analogousto modulation oscillation of the appropriate frequency equal to the desired power frequency.The comparators will output as "1" and when the signal that modulates,VREF_xis is greater than the triangular bearer signals or else the result will be "0". The output signals obtained from these comparators are summed to obtain the so-called 'aggregated signal'. This aggregated signal is further used to obtain gate pulses by comparing it with the corresponding levels. The lookup table for obtaining the gate pulses for each switch is based on the states shown in Table 1. The pole voltages only have positive levels, but the line voltages that areapplied to the load are both positive. and negative levels. The three voltages in the networkhas been seen as energy given below:

$$V_{ab} = V_{ao} - V_{bo} \ (1)$$
$$V_{bc} = V_{bo} - V_{co} (2)$$
$$V_{ca} = V_{co} - V_{ao} (3)$$

VI. EXPERIMENTALSTUDY

The demonstration is realized in the lab is used to investigate the topology based on three-phase switched capacitors proposed in this work as discussed in the previous sections. Table 2 summarizes the parameters used for experimentation. The results for a star-connected three-phase symmetrical inductive load is depicted in Figure. 4. The resultant pole energyis depicted in Figure. 4(a), the pole energyinclude four stages viz. 0, +100V, +200V and +300V.

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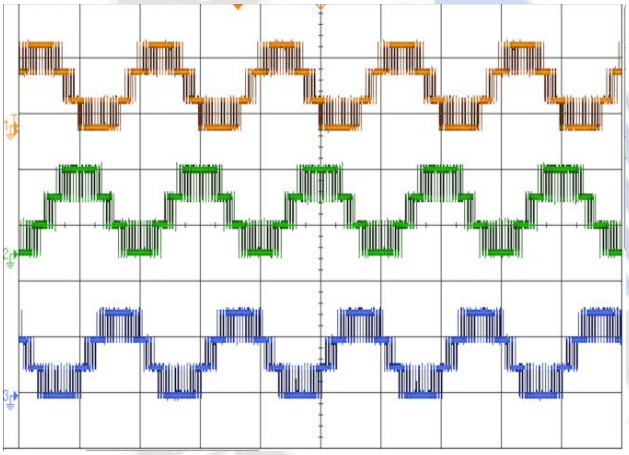
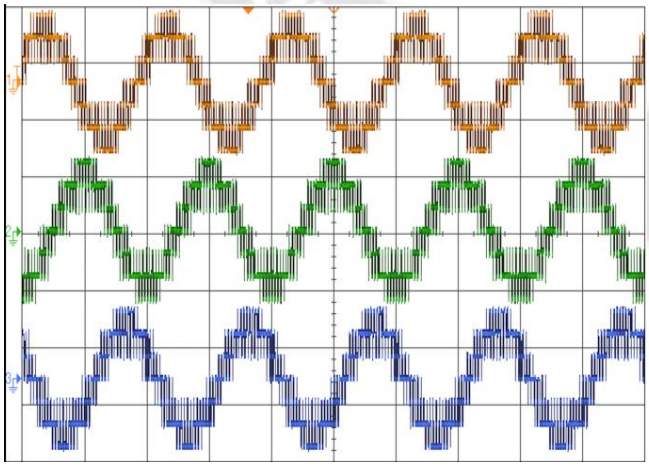
Line voltage transform is depicted in Figure. 4(b), the line energytransforms include seven levels viz. 0, ±100V, ±200V, ±300V. Figure 4(c) also presents the load progresstranformation. When the load resistance changes from 250 Ω to 500 Ω, the resultant current is halved and the output energy remains the same.

Table 2: the experimental set-up

Particulars	Specification
Input DC voltage source (V_{DC})	100V
Power frequency(f)	50Hz
Frequency of carrier waveforms	2 kHz
Load (three-phase star connected resistive)	R=250Ω, 500Ω
Modulation index (M)	0.95
Digital controller used to obtain gate signals	Texas Instruments TI F28379D



(a)



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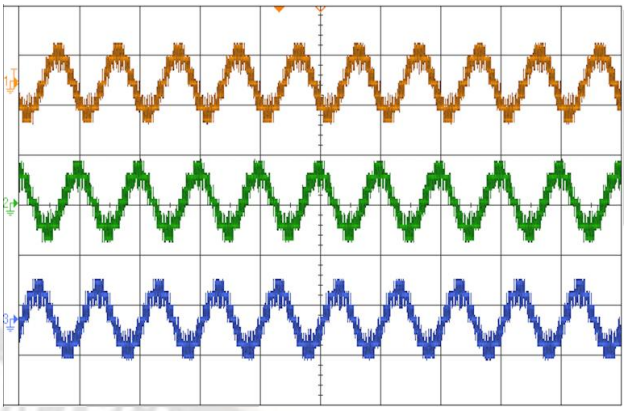

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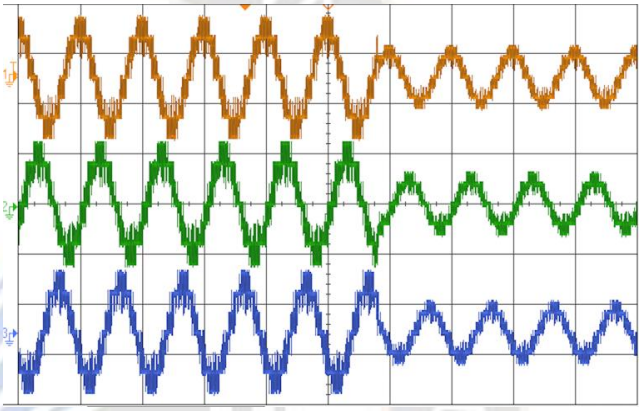

(d)

Fig.4: 3-phase suggestedconvertor for R-load (a) Pole voltage (200V/div); (b) line-to-line energy (200V/div); (c) resultant current; and (d) line current with sudden change in load resistance.

VII.CONCLUSION

This article endorsed a single-source 3-stage 7-phaseconvertor.The capacitors in each branch repeatedly go through charge and discharge modes, resulting in a self-balanced voltage with low ripple. Experimental findings confirm that the proposed inverter has amplification capability and self-balanced capacitor voltages, unlike conventional MLIs, which are characterized by uniform voltage gain. Conventional MLIs also use complex control methodologies to equalize capacitor voltages. This study shows that the proposed self-balanced 7-level inverter is appropriate for working with less energy DC originlike electric vehicles. The proposed structure works with a cost function of 5.429, while another topology with similar properties works with a cost function of 7.333. Thus, the proposed topology offers a significant reduction of 26%, which indicates that the cost spent on semiconductor devices and other components in the proposed topology will be lower while achieving a gain factor of three and a significantly reduced peak inversion voltage.

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