International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
***Article Received:** 26 August 2023 **Revised:** 20 October 2023 **Accepted:** 02 November 2023*

Design of SRAM Cell using Modified Lector and Dual Threshold Method Based on FINFET

[1]Ramesh Gullapally, [2]Dr. N. Siva Sankara Reddy, [3]Dr. P. Chandra Sekhar
[1]Research Scholar, Department of Electronics and Communication Engineering, University College of Engineering, Osmania University, Hyderabad, ramesh.gullapally@gmail.com.
[2]Associate Professor, Department of Electronics and Communication Engineering, Vasavi College of Engineering, Hyderabad, nssreddy69@gmail.com.
[3]Professor, Department of Electronics and Communication Engineering, University College of Engineering, Osmania University, Hyderabad, sekharpaidimarry@gmail.com.

Abstract: FinFET (Fin Field Effect Transistor) is a new technology that satisfies the demand for a superior storage system by improving transistor circuit design (SS). CMOS devices experience a wide range of issues due to the gate's diminishing ability to control the channel. Increased total production costs are a few of these disadvantages. But this store needs to dissipate less power, have a quick access time, and a low leakage current. The increased power dissipation and leakage current of traditional CMOS-based SRAM (Static RAM) architectures cause a sharp decline in performance. The nanoscale gadget called FinFET is being introduced for use in SRAM fabrication due to its 3D gate architecture. The adoption of FinFET has helped boost overall performance in terms of efficiency, power, and footprint. And because it is immune to SCEs, FinFET has become the transistor of choice. In this study, we have examined a number of FinFET-based SRAM cells and compared them with CMOS technology. We have also suggested a novel 14T SRAM design that uses the Dual Threshold Method and Modified Lector Approach with FinFET, and it is implemented for the 1bit, 4bit, and 8bit.

Keywords: FinFET, Dual Threshold, CMOS, Modified Lector, SRAM.

I. INTRODUCTION

The VLSI integration method has been the standard in the scientific community for quite some time (Very Large Scale Integration). VLSI refers to the method through which an IC (Integrated Circuit) is created by packing millions of transistors onto a single chip. New, cutting-edge technologies have emerged as a result of developments in VLSI, speeding up circuits and reducing design limitations. Miniaturization has become the norm for electronic devices. These days, every new Smart Gadget (SG) is miniaturized for easy portability. Memory and processing circuits are ubiquitous in such devices. Memory is becoming increasingly important in modern designs. In current technology, memory takes up more than 85–90% of the chip area. SRAM and DRAM, two types of memory chips, contribute greatly to SSD's impressive performance (Solid State Drives). However, many integrated devices require memory that is faster and more reliable. SRAM [1-2] contributes significantly to the low-power and high-performance capabilities that are necessary for VLSI applications. Due to process variances, SCEs, and leakage problems, rapid scale [3] has created reliability challenges. However, CMOS scaling [5, 6] triggered process differences in SRAM, despite its quicker speed, higher reliability, and lower power consumption. The scaling of dimensions is made feasible by the miniaturization of CMOS, but this in turn causes problems with stability and power consumption. Supply voltage scaling causes threshold voltage scaling, which is the primary issue with CMOS devices. The CMOS scaling made possible by Moore's law results in a nano-scale system [7]. Thus, technologies like CNTs (Carbon Nano Tubes), TFETs (Tunnel FETs) [10], and FinFETs [8, 9]. [11, 12] have emerged as viable alternatives to CMOS. Of these options, FinFET technology [11-12] is selected as the most promising successor to CMOS. Increased speed, greater drive current for a given transistor footprint, decreased leakage, elimination of random dopant fluctuation, decreased power consumption, enhanced mobility, and improved transistor scaling are just a few of the advantages of FinFET over bulk CMOS. Moreover, low power techniques including stacking, power gating, and self-controllable voltage level (SVL) are employed to reduce leakage current and power dissipation. SRAM is first designed using conventional CMOS design techniques. However, issues such as elevated leakage current and excessive power dissipation diminish the SRAM's efficiency. Low power dissipation, fast access times, and little leakage current are desirable characteristics for memory devices [13,14,15]. Shrinkage of semiconductor devices is the ideal method for electronic progress to acquire faster speeds, reduced costs, decreased both for improved semiconductor handy and power dissipation. Gordon Moore, a cofounder of Intel, in 1965 made the now-famous prediction that the number of semiconductors on a chip will quadruple at regular intervals. The

semiconductor industry has undergone tremendous change in recent years, with the number of semiconductors per chip increasing and the size of individual components decreasing. Present-day Very Large Scale Semiconductor Technology is based mostly on Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Integration as semiconductor sizes have reduced in accordance with Moore's Law (VLSI). The MOSFET's size has decreased from several microns to about 32 nm during the past two decades. Short channel impacts, channel-incited prevention reduction, limit MOSFET introduction is starting to be impacted by factors like voltage drop, etc. devices as the component size consistently decreases. When the oxide thickness on the door is reduced, the spillage current increases, causing the device to consume more energy and move more slowly. Non-ideal credits that aren't quite comparable to MOSFETs are recognized in the larger nanoscale framework.

Electronic reasoning structure plan, such as PC-based application, also relies heavily on semiconductor memories as critical microelectronic components. Semiconductor memory displays are able to store large amounts of the most up-to-date data, making them a vital component of all current systems. The quantity of semiconductors needed for limit work is more than for logic exercises and diverse applications, however this varies according on the type of use. The ever-increasing demand for extreme limit is what has pushed innovation and memory advancement in the direction of ever-increasing data accumulating densities. The usage of on-chip memory arrays as subsystems in VLSI circuits has become widespread, and the current commercially available single-chip read/form memory limit has been seen to be 1 GB. The semiconductor memory often has distinct sections for different data storage and retrieval types. Memory used for analysis and creation, known as The distinction between data bits reserved in the memory must be respected by random-access memory (RAM). display and their resumption interest. Reserved information is prone to fluctuations. Because to its fast speed and low power utilization, SRAM is mostly utilized for hold memory in chips, centralized worker PCs, planning workstations, and memory in controlled devices. Semiconductors are used to fabricate memory cells. As predicted by Moore's law, the number of semiconductors packed into a single chip is only going to expand in the future. However, their use declines as the area is reduced below 32nm, despite the fact that they provide quick of movement, lesser spillage, and reduced semiconductor count. The Integrated Technology Roadmap for Semiconductors (ITRS) details the history and current state of semiconductor technology.

The presence of tip top VLSI chips require a cutting edge method to store electronic data, on chip to address execution issues. SRAMs are the pinnacle of such courses of action. SRAMS are an essential piece of a wide extent of microelectronic contraptions. Customer demand advocates a reduction in size of memory storing devices. With advances in scaling growing, new hindrances are introduced on usage of sub 10nm MOSFETs in tremendous extension joined (VLSI) circuit plan, similar to affectability to deal with assortments and development in semiconductor spillage. Scaling has shown up at a fundamental apogee where the spillage streams have become a critical setback. Such results demand another FET development overall. An affable response to such demands was given by the presence of graphene.

FinFET technology is one of the most practical types of FET available now [17]. This allows transistor applications to be run and simulated more quickly in both the analog and digital worlds. FinFET's compact size, outstanding performance, low production costs, and low power consumption make it an attractive alternative for future nano electronics [18, 19]. Substituting FinFETs for bulkCMOS transistors is possible [20]. The low leakage current or standby power of this technology [21] makes it a strong contender in the construction of memory sub-systems.

In Fig. 1[22], a diagrammatic depiction of FinFET is shown for your perusal. Its name, "FinFET," alludes to the fact that the structure's many perpendicular channels resemble the "Fin" of a fish.

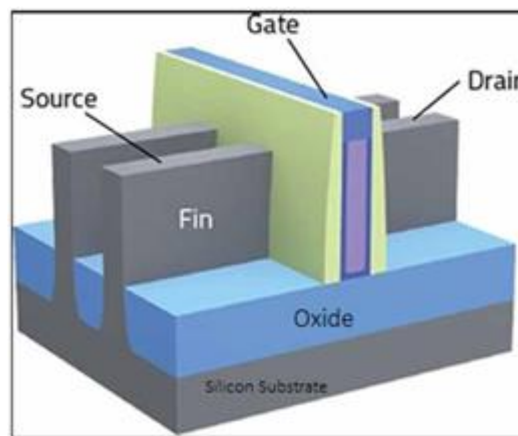


Figure 1: Structure of FinFET[22].

It is a substrate-based device that goes by the name "multi-gate device" (MGD). Double gate channels have the gate on two, three, or even all four of the channel's sides. The source or drain region is shaped like a 'Fin' on the silicon surface. FinFET is also known as a multi-gate transistor.

FinFET transistors have two possible modes of operation, known as Independent-gate (IG) and tied-gate (TG) modes [21]. In Fig. 2, we

have a three-dimensional illustration of the FinFET in both TG and IG mode.

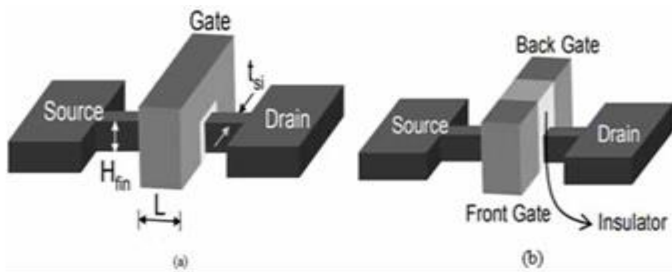


Figure 2: (a) 3D-view of TG FinFET (b) 3D-view of IG FinFET

Both the front and back gates (FBGs) are controlled by the same signal in TG-mode (CS). Using a shortened FBG, TG-FinFET design can be simplified. Due to stronger gate-to-channel coupling, the TG-mode stays away from the SCEsTo achieve equal rising and falling delays. Every FBG receives a different set of control signals while it is in IG-mode. Compared to CMOS technology, FinFET devices offer faster switching times and larger current densities. Furthermore, SCEs can be managed by restricting the off-state leakage. FinFET structures provide flexibility in design. It can operate in several different modes, including low power, hybrid, TG, and IG. Combined mode is IG plus low power mode, and its name comes from their combination [23]. From the perspective of fabrication, FinFET devices are equivalent to CMOS devices. In contrast, FinFET allows for significant performance boosts to be achieved while using a very little amount of power. FinFET devices are utilized to reduce gate-dielectric leakage currents known as SCEs. FinFET is a promising method for filling the void between bulk CMOS and cutting-edge devices like Graphene FETs and CNTFETs. FinFET technology is thus presented as a novel approach for producing a low-leakage SRAM cell.

II. 12T SRAM Cell

The proposed 12T piece cell in [24] drastically improves the compose edge by taking out the charge dispute because of the input design of a SRAM cell. Its inborn construction permits solid activity during composing by hindering the force supply course. There is no need to measure anything because there is no controversy on the charges. Adjusting the VTCs of successive inverters via pull-up devices can enhance RSNM by a much larger margin than can be achieved by measuring draw-down devices. As there is no sizing restriction in the suggested framework, any gadget can be estimated according to a unique presentation requirement. Due to the fault-free composition process, the proposed WSNM cell has a VTC that is comparable to the best bends recommended in Section 1. The 12T cell is more robust than the standard 6T and 8T cells, and it is on par with the 10T cell in the WSNM, CWMM, and BLWM senses of compose edge. In addition, compared to the 6T, 8T, and 10T cells, the suggested 12T cell is more robustly stable. The proposed cell achieves improved WSNM, BLNM, and DNM at the expense of neither BLNM nor DNM nor RSNM. Since the memory block space is equivalent to the fringe hardware space, the suggested 12T cell is well suited for extreme low force applications requiring low voltage activities while requesting relatively low limit. In addition, the WSNM conceptual model of the 12T cell is proposed for further study. The subthreshold model can account for 14.2% of errors, whereas the super-limit model can account for just 8.7% of them. Super-edge model fits data to within 6.17 percent and subthreshold model fits data to within 15.42 percent when proportion varies from one to five[31].

Two four-hook cross-coupled SRAM bit-cells are proposed by the authors of paper [25] for extremely reliable terrestrial uses. The QUCCE 10T and 12T, at nominal inventory voltage, have equivalent or better delicate blunder ruggedness, RSNMs, and HSNMs than the majority of proposed SRAM cells. About 2.0 and 3.4 times as powerful as the standard 6T basic charge are the QUCCE 10T and 12T, respectively. Despite having a high composition blunder rate at the edge voltage area, the QUCCE 10T's proven dependability makes it unsuitable for usage in low voltage applications. The great majority of contemporary delicate mistake tolerant SRAM bit-cells have region overheads that are lower or similar to those of the QUCCE 10T. Thus, the QUCCE 10T is a solid choice for Earthly applications with high thickness and extreme reliability at apparent stockpile voltage. About 56% more region and 50% less leakage power are punished by QUCCE 12T compared to the standard 6T. The QUCCE 12T has the best understood edge, with the exception of the 8T, as far as the / proportion in close to limit voltage district among the wide range of different cells which almost have no compose disappointment around there, and It is suitable for fast SRAM designs because it reduces read admission time by more than half when compared to the majority of referential cells, including the 6T. Since the suggested QUCCE 12T circumvents the three challenges associated with applying close/subthreshold voltage in SRAM schemes, it is a strong contender for exceptionally solid earthbound low-voltage applications in the future: increased postponement, decreased read steadiness, and increased composition blunder rate. In addition, the QUCCE framework can be used to plan delicate mistake tolerant hooks, travels back and forth, and registers, just as DICE and Quatro.

In the paper [26], Authors present a novel profoundly dependable 12T cell with decoupled peruse and compose ports. Recreation results have shown the ordinary capacities and delicate mistake resistance of the proposed. Contrasted and the

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: 26 August 2023 Revised: 20 October 2023 Accepted: 02 November 2023

wide range of various bitcells, the proposed 12T has the biggest RSNM, and it additionally saves 85.4% read admittance time by and large. Also, it shows 42.2% spillage power punishment over the customary 6T. These outcomes being thought of, the proposed double port 12T is reasonable for rapid exceptionally dependable applications.

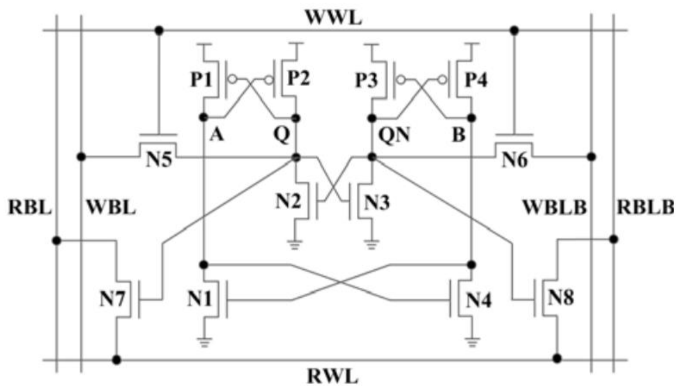


Figure 3: 12T SRAM cell

A fast and reliable RHPD-12T memory cell was proposed briefly in [27-28]. The suggested RHPD-12T cell outperforms other radiation-solidified memory cells in It is resistant to single-hub disruptions and operates with a low force supply voltage and high frequency. When compared to all other referential cells, including the DICE cell, RHPD-12T can save more than 40% of compose access time. keep up great composing capacity even in close limit voltage district, and it additionally has the best hold and compose edge among the wide range of various cells, which makes it reasonable for fast and high-unwavering quality SRAM plans. Consequently, the proposed RHPD-12T cell displayed in Figure 3 can be viewed as a decent plan for aviation applications, as it's anything but a decent harmony between radiation power and circuit execution. An error-tolerant RHMC-12T. This study proposes an SRAM cell using circuit level solidifying technique. The suggested design may correct for a SEU error from 0 to 1 or 1 to 0 at any critical hub. The total number of sensitive hubs is reduced from 4 in conventional radiation solidifying memory cells to 2 in the suggested design, making it more robust to error. The proposed cell has the greatest potential for SRAM cells to be used in radiation environments because to a decrease in the absolute touchy region.

III. PROPOSED 14T SRAM CELL

At last, the typical 6T SRAM cell is utilized as center putting away fragment and key piece of PC plans and construction in CMOS improvement. The immediate arrangement of 6T SRAM with colossal breaking point limit makes its appropriate part, yet experiences read/make fight, half-select unsettling effect and read upset [27]. Reliability of standard Si-CMOS SRAM cells is truly inconvenient at low stock voltage, which corrupts totally due to VMIN, supply voltage scaling and its display effect requirements [27].

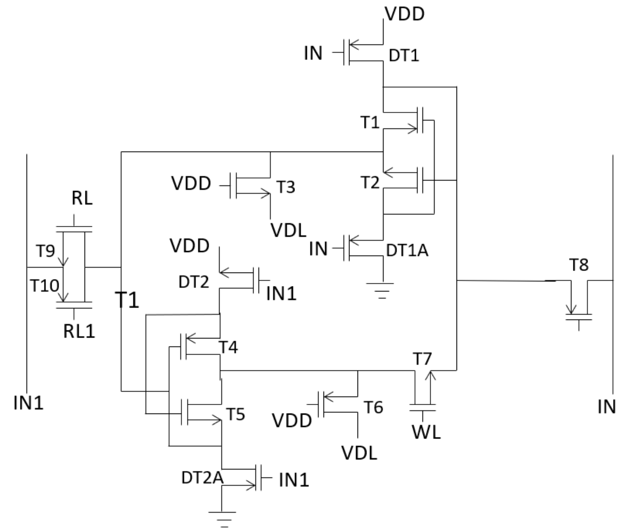


Figure 4 - Dual-threshold 14T SRAM cell using a modified Lector Approach

At last, The standard 6T SRAM cell is used in center putting away fragment and key piece of PC plans and construction in CMOS improvement. The immediate arrangement of 6T SRAM with colossal breaking point limit makes its appropriate part, yet experiences read/make fight, half-select unsettling effect and read upset [27]. Due to VMIN requirements, the consistency of a standard Low starting voltage Si-CMOS SRAM cell is incredibly uncomfortable. This corruption occurs in tandem with supply voltage scaling, which in turn has an effect on the display. There have been a number of suggestions from experts [28-30] to focus on overcoming anxiety and executing a SRAM scheme with low force and low storage voltage. In a range of SRAM cells, read maintains can be utilized to increase read security by continuously updating read SNM and hold SNM were identical as a result of the read steaming [29–31]. In SRAM cell research and structure support frameworks with isolation, negative-cycle line, word-line-over-drive, and transient-voltage breakdown are used to improve write jobs; covered digit line, negative-VSS, and word-line-under-drive are used to improve read jobs. By increasing the pull-down strength on a single read port, a disproportionate SRAM cell's read security can be enhanced and read upset can be decreased [35]. Even though the information system's attempts to lessen read upset have significantly increased consistency by limiting phone gathering operations related to read bitline, read upset still persists. Spilling current in the subthreshold region is changed as a result of the gliding focal point storage that the NMOS semiconductors activate, which could result in a number of cell disruptions [36]. By employing employing the piece interleaving technique in conjunction with fumble check and correction [37], you can lessen the disruption reasonable degree in each of the cells. Because chosen

wordline (WL) conduct pseudo read development consumes power, digit interleaving architecture is not a good fit for the standard 6T SRAM cell [38, 39]. It is possible to prevent the create half-select unpleasant effect on line and segment based structures by employing cross-point make planning. A single-finished marvel-free architecture and low stock voltage in the restrict voltage region. The suggested cell resolves the make half-select problem, while read cushion and single bitline are implemented using cross-point access to enhance read reliability and reduce power consumption, respectively. The twofold limit voltage method is a helpful strategy for power reduction in a working technique for activities because it significantly lowers the spillage current in the idle state. Since the LVT devices are closer to the voltage limits of the cell, an LVT cell has a higher SNM than an HVT cell. Because of this, the typical SRAM cell may quickly select a risk-averse voltage [40, 41]. In contrast to cells with high-edge voltage, those with low-limit voltage devices offer significantly greater resilience to disruptive influences. The proposed SRAM design requires a lower than 0.5V device stock voltage and employs 16 nm low leakage FinFET technology to minimize power consumption. For the 16 nm low leakage FinFET-based SRAM design, 325 mV is the ideal stock voltage. Due to its ability to drive with a manufacturing line and so lessen the conveyance way difficulty in the circuit, T10 semiconductors are frequently employed. T10 turns on when the production line is ready. To start, I'll choose T10, which is unquestionable for typical 6T and 8T SRAM cells, to narrow down my investigation. Utilizing a two-edged construction is an additional choice. When read/make conflicts arise, the industry standard 6T SRAM becomes less appealing and effective. An 8T SRAM cell physically divides the make bitline from the read bitline in order to minimize read upset. For this separation, a distinct read line (WL) is used. Half-select problems occur when the structural line (WL) modifies the charge flow from the bitline into the internal focus of the 8T SRAM cell during interleaving. The more memory cells on the bitline, the more troublesome the half-select problem got. Force spread in SRAM memory cells is greatly reduced by using a special finishing procedure. There is a significant reduction in both the chip pattern area and the leakage current. We can cut the remarkable dynamic in half with this one-step method. The degree of inspection/structure delays at the low stock voltage, in any case, distorts the familiarity of the SRAM cell. Analytical and make support methods that are straightforward have been suggested to tackle these problems. These include examination read/make support, unequal read/structure - support, double edge voltage, cross-point-information cautious, and force support. Based on single-finished FinFETs, we report on the construction of a new 14T SRAM cell. Figure 2 depicts the general design of a 14T single-ended, clash-free FinFET-based SRAM cell. In the suggested cell, two cross-coupled inverters, inv1 (T1 and T2) and inv2 (T5 and T4), respectively, are used to store the focus Q and Qn information. By adding an extra read/structure port (T5-T9), the suggested 9T SRAM cell's display capabilities can be improved. Taking into account the limited read port, the computed miracle obstacle of the new 14T SRAM cell is 2.8 times greater than that of an 8T SRAM cell with a similar area overhead (T7, T8, and T9). The semiconductor assessment degree (T5/T9) of the structure port has been raised to 1.8 in order to optimize the development and power of each SRAM cell. The components will be interleaved to lessen coupling problems and tidy up the delicate mess. The line section select line's massive number of cells are used to reduce region overhead and boost bunch capacity.

IV. LECTOR APPROACH

To address the issue of leaking power in CMOS circuits, Narender Hanchate et al. introduced a new method they dubbed LECTOR (see Fig. 5). Within the logic gate, he included a pair of PMOS and NMOS leakage control transistors (LCT). Every LCT's gate terminal is managed by its source. For any given set of inputs, one of the LCTs in this design will be very close to its breakdown voltage. Since there is a greater resistance between Vdd and ground, leakage currents are much decreased. When it comes to reducing leakage in both the on and off states of a circuit, this method is unparalleled. Based on the experimental results, there is an average 79.4% reduction in leakage in the MCNC reference circuits.

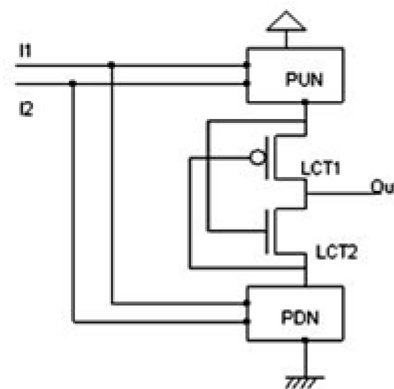


Figure 5: Technique of LECTOR

Static Random Access Memory is another term for SRAM. Central processing unit caches, workstations, PCs, routers, hard disk buffers, and router buffers all use this technology. DRAM needs to be refreshed frequently, whereas SRAM can be used indefinitely without losing its data. Information is lost when there is no power. A 6T SRAM cell consists of two PMOS and four NMOS transistors. An example of an SRAM cell in operation is a 6T SRAM cell. Figure 3 displays a working schematic of a 6T SRAM cell. There are three modes of operation for

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
***Article Received:** 26 August 2023 **Revised:** 20 October 2023 **Accepted:** 02 November 2023*

SRAM: read, write, and hold. When WL voltage is increased during a write operation, bit lines BL and BL' are linked to Vdd or other suitable voltages. This new value for the bit line replaces the previous one in full. Once the WL voltage is increased during a read operation, memory cells discharge either BL or BL', depending on the data that was previously stored at nodes Q and Q'. The BLs are either driven to Vdd or left floating while the WL voltage is maintained low during the Hold state. Eight transistors in a cross-coupled arrangement store each bit in an SRAM. With its two fixed states, this memory cell may represent the binary numbers 0 and 1. Two more access transistors control the flow of data to and from the storage cell during read and write operations.

V. RESULTS AND DISCUSSION

The proposed design has been simulated in HSpice. The design with dual threshold has been simulated by both using FinFET and CMOS. The table 1 displays a comparison between the FinFET and SRAM cell. CMOS, where the GNRFET shows the very accurate less power when compared with the FinFET. Figures 6 and 7 shows the waveforms for both FinFET and CMOS respectively. Table 4,5,6 shows the total technology Parameters.

Table 1: 14T SRAM Cell 1 bit comparison between FinFET and CMOS

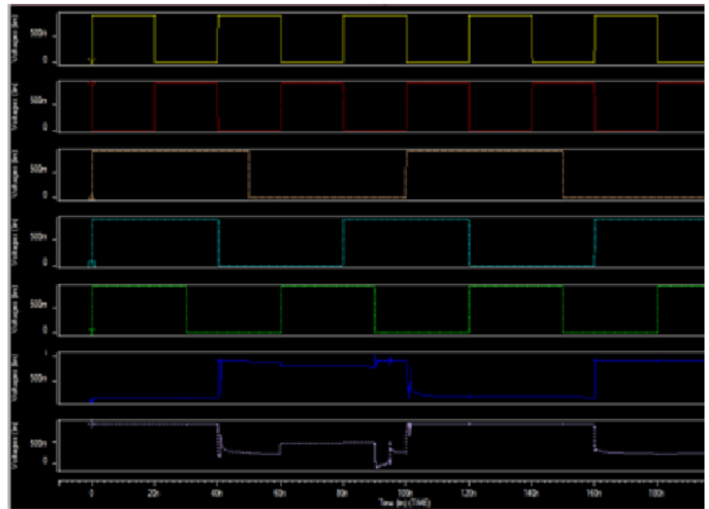
S.NO.	NM	Power in mW for CMOS	Power in mW for FinFET
1	22	6.08	3.57
2	14	5.32	3.28
3	10	5.76	2.67
4	7	5.68	2.53

Table 2: 14T SRAM Cell 4 bit comparison between FinFET and CMOS

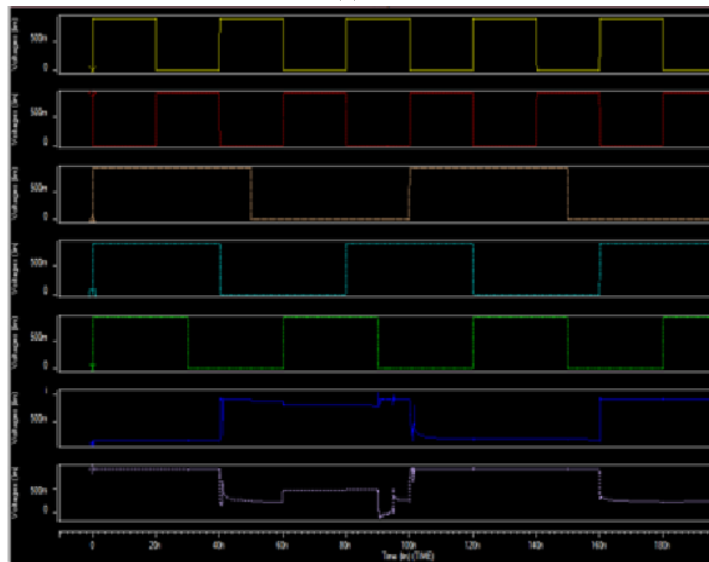
S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET
1	22	2.81	1.35
2	14	2.36	1.26
3	10	1.92	1.22
4	7	1.82	1.19

Table 3: Evaluation of 14T SRAM Cell 8 bit in comparison to FinFET and CMOS

S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET
1	22	3.01	1.92
2	14	2.62	1.72
3	10	2.21	1.65
4	7	1.98	1.58



(a)



(b)

Figure 5- FinFET Waveforms in Hspice and CMOS Waveforms in Hspice

Table 4- 22nm-1bit technology parameters

S.NO.	PARAMETER	VALUE
1	Power_avg	3.5702E-05 from= 0.0000E+00 to= 2.0000E-07
2	Avgpwr	3.5989E-05 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	Failed
4	Trig	not found
5	Tpd	2.7406E-11
6	qn_rise_delay	2.7406E-11
7	qn_fall_delay	-2.9433E-11
8	SupplyCurrent	1.5602E-05 from= 0.0000E+00 to= 1.0000E-08

International Journal on Recent and Innovation Trends in Computing and Communication
ISSN: 2321-8169 Volume: 11 Issue: 10
Article Received: 26 August 2023 Revised: 20 October 2023 Accepted: 02 November 2023

9	Static power	-7.8011E-06
10	high_low_total_energy	3.8728E-14
11	low_to_high_total_energy	3.9283E-14
12	dynamic_energy	7.8011E-14
13	total_dynamic_energy	3.9005E-14
14	total_dynamic_power	-1.2346E-29

Table 5- 22nm-4 bit technology parameters

S.NO.	PARAMETER	VALUE
1	Power_avg	1.3515E-09 from= 0.0000E+00 to= 2.0000E-08
2	Avgpwr	1.3515E-09
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	1.8714E-10
7	qn_fall_delay	3.8400E-11
8	SupplyCurrent	6.5328E-10
9	Static power	5.8795E-10
10	high_low_total_energy	5.8867E-18
11	low_to_high_total_energy	7.2297E-21
12	dynamic_energy	5.8795E-18
13	total_dynamic_energy	2.9398E-18
14	total_dynamic_power	1.2346E-29

Table 6 - 22nm-8 bit technology parameters

S.NO.	PARAMETER	VALUE
1	Power_avg	1.9230E-09 from= 0.0000E+00 to= 3.0000E-08
2	Avgpwr	1.9230E-09
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	2.1673E-11
5	Tpd	2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11
8	SupplyCurrent	1.3066E-09
9	Static power	-1.1759E-09
10	high_low_total_energy	1.1773E-17
11	low_to_high_total_energy	-1.4459E-20
12	dynamic_energy	1.1759E-17
13	total_dynamic_energy	5.8795E-18
14	total_dynamic_power	-1.2346E-29

VI. CONCLUSION

By performing this research we have analysed SRAM cell using modified lector and dual threshold method based on FinFET, which has been implemented for 1bit, 4bit and 8bit. Power has been decreased upto 60% when compared to CMOS. Successfully designed and tested the SRAM with dual threshold and modified lector approach.

REFERENCES

[1]. Agrawal, R., & Tomar, V. K. (2018). Analysis of Low Power Reduction Techniques on Cache (SRAM) Memory. In 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), IEEE, 1–7

[2]. Pasandi, G., Mehrabi, K., Ebrahimi, B., Fakhraei, S. M., Afzali-Kusha, A., & Pedram, M. Low-power data encoding/decoding for energy-efficient static random access memory design.IET Circuits, Devices & Systems,13(8),1152–1159

[3]. Lin, Z., Wu, X., Li, Z., Guan, L., Peng, C., Liu, C., & Chen, J. (2016). A pipeline replica bitline technique for suppressing timing variation of SRAM sense amplifiers in a 28-nm CMOS process. IEEE Journal of Solid-State Circuits, 52(3), 669–677

[4]. Chiu, P. F., Chang, M. F., Wu, C. W., Chuang, C. H., Sheu, S. S., Chen, Y. S., & Tsai, M. J. (2012). Low store energy, low VDDmin, 8T2R nonvolatile latch and SRAM with vertical-stacked resistive memory (memristor) devices for low power mobile applications. IEEE Journal of Solid-State Circuits, 47(6), 1483–1496

[5]. Mocuta, A., Weckx, P., Demuynck, S., Radisic, D., Oniki, Y., & Ryckaert, J. (2018). Enabling cmos scaling towards 3nm and beyond. In 2018 IEEE Symposium on VLSI Technology IEEE, 147–148

[6]. Yusop, N. S., Nordin, A. N., Khairi, M. A., & Hasbullah, N. F. (2018). The impact of scaling on single event upset in 6T and 12T SRAMs from 130 to 22 nm CMOS technology. Radiation Effects and Defects in Solids, 173(11–12), 1090–1104

[7]. Zhang, K. (2018 Nov 5). Circuit design in nano-scale CMOS technologies. In2018 IEEE Asian Solid-State CircuitsConference (A-SSCC) IEEE, 1–4

[8]. Ensan, S. S., Moaiyeri, M. H., Moghaddam, M., & Hessabi, S. (2019). A low-power single-ended SRAM in FinFETtechnology. AEU-International Journal of Electronics and Communications, 99, 361–368

[9]. Liautard, R., Trojman, L., Arevalo, A., & Procel, L. M. (2019). TFET and FinFET Hybrid Technologies for SRAM Cell: Performance Improvement over a Large VDD-Range. 2019 IEEE Fourth Ecuador Technical Chapters Meeting (ETCM) (pp. 1–5). IEEE

[10]. Jia, X., & Wei, F. (2019). Advances in production and applications of carbon nanotubes. Single-Walled Carbon Nanotubes (pp. 299–333). Cham: Springer

[11]. Birla, S. (2019). FinFET SRAM cell with improved stability and power for low power applications. Journal ofIntegrated Circuits and Systems, 14(2), 1–8

[12]. Birla, S. (2019). Variability aware FinFET SRAM cell with improved stability and power for low power applications.

[13]. Panchal, J., & Vishal, R. (2017). Design And Implementation

Of 6t Sram Using Finfet With Low Power Application. 2395-0056

[14]. Narendar, V., & Mishra, R. A. (2015). Analytical modeling and simulation of multigate FinFET devices and theimpact of high-k dielectrics on short channel effects (SCEs). Superlattices and Microstructures, 85, 357–369

[15]. Tripathi, T., Chauhan, D. S., & Singh, S. K. (2018). A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability. Journal of Low Power Electronics and Applications, 8(4), 41

[16]. C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao, " Device Design and Optimization Considerations for Bulk FinFETs", IEEE transactions on electron devices, Vol. 55, No. 2, pp. 609-615, February 2008.

[17]. Jurczak, M., Collaert, N., Veloso, A., Hoffmann, T., & Biesemans, S. (2009). Review of FINFET technology. In 2009 IEEE international SOI conference, pp. 1–4. IEEE

[18]. Dadoria, A. K., Khare, K., Gupta, T. K., & Singh, R. P. (2017). Leakage reduction by using FinFET technique for nanoscale technology circuits. Journal of Nanoelectronics and Optoelectronics, 12(3), 278–285

[19]. Guo, D., Karve, G., Tsutsui, G., Lim, K. Y., Robison, R., Hook, T., Vega, R., et al. (2016). FINFET technology featuring high mobility SiGe channel for 10nm and beyond. In 2016 IEEE Symposium on VLSI Technology, IEEE, 1–2

[20]. Yakimets, D., Bardon, M. G., Jang, D., Schuddinck, P., Sherazi, Y., Weckx, P., Miyaguchi, K., et al. (2017). Power awareFinFET and lateral nanosheet FET targeting for 3nm CMOS technology. 2017 IEEE International Electron Devices Meeting (IEDM) (pp. 20–24). IEEE

[21]. Garg, M., & Singh, B. (2017). A comparative performance analysis of cmos and finfet based voltage mode sense amplifier. In 2016 8th International Conference on Computational Intelligence and Communication Networks (CICN), IEEE, 544–547

[22]. T. Venkata Lakshmi, M. Kamaraju" A Review on SRAM Memory Design Using FinFET Technology", International Journal of System Dynamics Applications, Volume 11, Issue 6, 2021

[23]. Rajprabu, R., Raj, A., V., and, & Rajnarayanan, R. (2013). Performance Analysis of CMOS and FinFET Logic. IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), 2(1), 1–6

[24]. Qiang Zhao, Chunyu Peng , Junning Chen, Zhiting Lin , and Xiulong Wu, "Novel Write-Enhanced and Highly Reliable RHPD-12T SRAM Cells for Space Applications", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2020.

[25]. Suraj Singh Dohar, Siddharth R. K., Vasantha M.H., Nithin Kumar Y.B., "A Novel Single Event Upset Tolerant 12T Memory Cell for Aerospace Applications", 2159-3477/20/, 2020, IEEE.

[26]. Young Bok Kim, "Design methodology based on carbon nanotube field effect transistor (CNFET)", Computer Engineering Dissertations, 2011.

[27]. Sang Hoon Chae, Young Hee Lee, "Carbon NanoTubes and graphene towards soft electronics," Nano Convergence 2014, pp.1-15.

[28]. Narender Hanchate & N. Ranganathan, (2004),'A New Technique for Leakage Reduction in CMOS Circuits using Self-Controlled Stacked Transistors", Proceedings of the 17th International Conference on VLSI Design (VLSID"04) IEEE.

[29]. Z. Chen, Y.-M. Lin,M. J. Rooks, and Ph. Avouris, "Graphene nano-ribbon electronics," *Physica E: Low-dimensional Syst. Nanostruct.*, vol. 40, pp. 228–232, 2007.

[30]. M. Y. Han, B. O¨ zyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, pp. 206805- 1–206805-4, 2007.

[31]. X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultra smooth graphene nanoribbon semiconductors," *Science*, vol. 319, pp. 1229–1232, 2008.

[32]. Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in grapheme nanoribbons," *Phys. Rev. Lett.*, vol. 97, pp. 216803-1–216803-4, 2006.

[33]. K. S. Novoselov et al., "Electric field effect in atomically thin carbon films," Science, vol. 306, pp. 666–669, 2004.

[34]. Y. Zhang et al., "Experimental observation of the quantum Hall effect and Berry's phase in graphene," Nature, vol. 438, pp. 201–204, 2005.

[35]. C. Berger et al., "Electronic confinement and coherence in patterned epitaxial graphene," Science, vol. 312, pp. 1191–1196, 2006.

[36]. R. V. Noorden, "Moving towards a graphene world," Nature, vol. 442, pp. 228– 229, 2006.

[37]. X. Li et al., "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," Science, vol. 319, pp. 1229–1232, 2008.

[38]. Niraj K. Jha, Deming Chen, "Nanoelectronic Circuit Design", Springer, 2011.

[39]. C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao, " Device Design and Optimization Considerations for Bulk FinFETs", IEEE transactions on electron devices, Vol. 55, No. 2, pp. 609-615, February 2008.

[40]. Joerg Appenzeller, "Carbon nanotubes for high performance electronics - Progress and prospect", Purdue e-Pubs, 2008.

[41]. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris," Single- and multi-wall carbon nanotube field effect transistors", Applied Physics Letters, Vol. 73, no. 17, pp. 2447-2449, Oct. 1998.