Defence Science Journal, Vol. 74, No. 1, January 2024, pp. 85-90, DOI : 10.14429/dsj.74.19149

A Low Noise Variable Gain Amplifier with 97.2 dB Linear Gain Range for CW Radar

Vijay Kumar* and Sujatha Ravichandran
DRDO-Research Center Imarat, Hyderabad - 500 069, India
**E-mail: vijayk.rci@gov.in*

ABSTRACT

This manuscript reports the design of a low noise variable gain amplifier (VGA) having wide dB linear gain characteristics for a continuous wave (CW) radar. A pseudo-exponential gain control function has been adopted in this VGA for the wide dB-linear behavior. Also, a BJT-based gain stage has been proposed to improve the gain dynamic range and low noise performance due to its higher transconductance/gain and lower flicker noise contribution. This proposed 2-gain stage VGA has been implemented in 130 nm SiGe bipolar complementary metal–oxide–semiconductor (BiCMOS) technology. This design performance has been benchmarked by post-layout simulation results. It has demonstrated a voltage-controlled gain from -33.6 dB to 74.4 dB (total 108 dB), with a 97.2 dB linear gain range, input referred noise of 2.4 nV /√Hz, and power consumption of 4.25 mW. This VGA has a 3-dB bandwidth of 10 MHz at a maximum gain of 74.4 dB and 251 MHz at a minimum gain of -33.6 dB with a chip layout area of 0.0682 mm^2. Compared to the latest available CMOS/BiCMOS VGAs in the literature, this proposed VGA has the highest gain dynamic range and dB-linear gain range with minimum input referred noise simultaneously across the operation bandwidth.

Keywords: VGA; CW radar; dB-linear gain; Pseudo-exponential gain control; Low-noise

1. INTRODUCTION

Radars have well-established usages for various applications such as advanced driver assistance systems (ADAS) in automotive engineering[1], indoor localisation[2], health care systems[3], and drone systems[4-5], etc. Therefore, highly integrated silicon (Si)/silicon-germanium (SiGe) based system-on-chip (SoC) for radars have been developed by various researchers. This SoC approach enables the large-scale integration of analog, digital, and RF circuitry on a single chip, facilitating the system design with a smaller form factor and lesser power consumption at a lower cost[6].

Among the various types of radar, CW-type radar is used most frequently owing to its simpler architecture. Typically, a radar receives very low power ≤ -100 dBm, and can be as high as ≥ -40 dBm. Therefore, a VGA is vital to achieve the required wide dynamic range in the radar transceiver, as shown in Fig. 1. VGA is used in the transmitter and receiver chain to regulate the transmitted signal power and received signal amplitude, respectively[7]. This gain adjustment is required in the analog domain; therefore, VGAs with analog control voltage are preferred for precise gain control. An attenuator is the other way to control the signal amplitude; however, at the baseband signal level, VGAs are preferably used in CW radar[8].

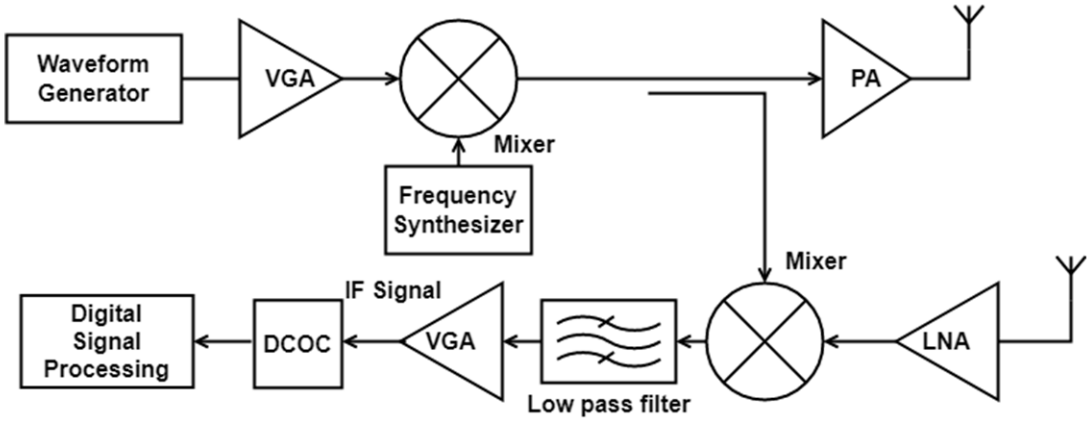

Figure 1. Typical outline of a generic CW radar transceiver.

Received : 23 May 2023, Revised : 20 September 2023
Accepted : 19 October 2023, Online published : 12 January 2024

The performance matrix of the VGA comprises dB-linear gain characteristics versus control voltage with low input

referred noise, low power consumption across the frequency band of operation, and a smaller silicon area. Various VGA topologies have been proposed to address the trade-off among these performance parameters.

Various VGA architectures have been proposed in the literature to meet application-specific requirements. A Gilbert cell-based VGA has been designed with a negatively compensated pseudo-exponential control function in[9]. However, it has a broadband frequency response of 7 GHz-to-8 GHz, with positive gain control of only 17 dB and a high power consumption of 27 mW. Likewise in[10], a VGA with 4 GHz bandwidth and low positive gain control of 21-dB is designed. These VGAs are[9-10] suitable for high-speed and RF-over-fiber communication applications[11]. In[12], a cell-based reconfigurable VGA with current steering at load has been designed for low power and wide linear gain range. However, it has a limited positive gain variation of 56 dB. A programmable gain amplifier (PGA) with complementary current-switching is designed with low power and a wide linear gain range in[13]. At the same time, this has a peak gain of up to 34.9 dB. A PGA with pseudo-exponential and binary-weighted switching is designed in[14] for low gain error performance. However, this PGA design has a limited gain of up to 25 dB and high input referred noise of 22.4 nV /√Hz.

This manuscript describes a low-noise and high-dB-linear gain characteristics VGA circuit for CW radar. In this VGA, a-dB linear control function generation circuit is adopted for a wider gain dynamic range, and a BJT-based amplifying stage has been used for the higher dB-linear gain requirement of CW radar. This 130 nm BiCMOS VGA exhibits a 97.2 dB linear-in-decibel gain with a flat input-referred noise of 2.4 nV /√Hz in the post-layout simulation results. This VGA has a power requirement of 4.25 mW with a minimal layout area of 0.0682 mm^2.

2. VGA ARCHITECTURE

The functionality of the variable gain amplifier is realized using the amplifying stage, control function generation circuit, and a buffer[7,9-12]. Figure 2 shows the block diagram of a VGA circuit, and the description of each sub-block is as follows:

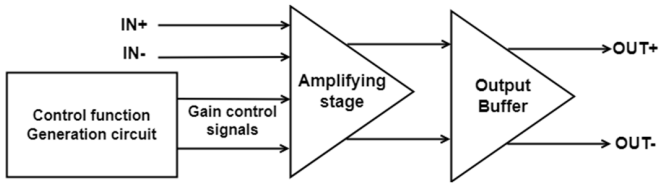

Figure 2. Block diagram of VGA circuit.

2.1 Amplifying stage

An amplifying stage is used for the variable gain functionality. Generally, the main transistors' current/ transconductance/device sizes are varied to realise the variable gain.

2.2 Control Function Generation

For the down-converted signal after the mixer, wide gain variation and dB-linearity in the gain variation of VGA with control voltage are highly important for better signal recovery. Therefore, an exponential/pseudo-exponential function generation control circuit is used.

2.3 Output Buffer

In case VGA is designed for application-independent usage, an output buffer with a standard impedance load such as 50 Ω is incorporated at the output of an amplifying stage.

The architecture given in Fig. 2 is an open-loop VGA. In the case of the open-loop VGA, an amplifying stage's gain is controlled by varying the transconductance (g_m) of the input transistors. Generally, the gain (A_v) of an amplifier with output load resistance is given by Eqn. (1)

$$A_v = g_m R_D \tag{1}$$

The g_m of the transistor can be changed by regulating its bias current. The g_m of an NMOS transistor in the saturated condition is specified by Eqn. (2).

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{bias}} \tag{2}$$

Once the circuit design is completed, $\mu_n C_{ox}$ and W/L cannot be varied further for a transistor used in the design. However, g_m can be adjusted by varying its bias current.

Gilbert cell has been the most popular gain block with a possibility of controlling gain by varying the bias current[10-12]. Because the transconductance of Gilbert cell ($g_{m\_Gilbert}$) has a relationship with a control voltage (V_{ctrl}). For an input transistor pair (M_{IN}) and input transistor pair (M_{TAIL}), $g_{m\_Gilbert}$ is given by Eqn. (3)

$$g_{m_{Gilbert}} = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)} \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{TAIL}} V_{ctrl} \tag{3}$$

3. PROPOSED VGA DESIGN

3.1 Control Function Generation Circuit

In a typical radar operation scenario, the signal received at the input of the radar varies dynamically by large amplitude. Therefore, to keep the signal amplitude level suitable for processing in the DSP, it is required to design a VGA with a wide dynamic range of the order of 100 dB or more. Also, the BiCMOS process used for designing this VGA can support a maximum supply voltage of 2.5 V. Considering the threshold voltage of the transistor, the maximum control voltage available for gain variation is from 0.575 V to 1.85 V i.e., 1.85 – 0.575 = 1.275 V. This 100 dB or more wide dynamic gain requirement for such low control voltage range of 1.275 V exponential gain control function generation (EGCFG) circuit is used and other gain control function generation based on logarithmic function are not able to meet this requirement. For meeting the specification of wide gain dynamic range along with dB-linearity requirement, an exponential gain control function generation (EGCFG) circuit is adopted[15]. The exponential approximation of $e^{\alpha x}$ is given by Eqn. (4)

$$f(x) = e^{\alpha x} = \frac{e^{\frac{\alpha x}{2}}}{e^{\frac{-\alpha x}{2}}} \cong \left| \frac{k+\left(1+\frac{\alpha x}{2}\right)^2}{k+\left(1-\frac{\alpha x}{2}\right)^2} \right| \tag{4}$$

In Eqn. (4) α and k are constant, such that $|\alpha x| < 1$ and $k < 1$. This approximation has been adopted in the proposed design considering its property of high input dynamic range and enhanced dB-linear range.

The drain current of the NMOS/PMOS follows the square law characteristics and is given by Eqn. (5)/Eqn. (6) in the saturation region.

$$I_{DN} = \frac{K_n}{2}(V_{GS} - V_{THn})^2 \quad (5)$$

$$I_{DP} = \frac{K_p}{2}\left(|V_{GS}| - |V_{THp}|\right)^2 \quad (6)$$

Eqn. (5), $K_n = \mu_n C_{ox} W_n/L_n$, and in Eqn. (6), $K_p = \mu_p C_{ox} W_p/L_p$, with mobility constant (μ), gate-oxide capacitance (C_{ox}), width (W) and length (L) of the respective NMOS/PMOS transistors. Considering the square law characteristics of NMOS/PMOS transistors, the numerator of Eqn. (4) can be realised by a constant current source (I_{f2}), a variable NMOS current source (I_{v2}), and is given by Eqn. (7). Similarly, the denominator of Eqn. (4) can be realised by a constant current source (I_{f1}), a variable PMOS current source (I_{v1}), and is given by Eqn. (8). Figure 3 shows the circuit for an exponential gain control function generation.

Therefore from Fig. 3,

$$I_{c2} = I_{f2} + I_{v2} \quad (7)$$

$$I_{c1} = I_{f1} + I_{v1} \quad (8)$$

The initial Wn/Ln and Wp/Lp ratio of NMOS and PMOS transistors used in this exponential gain control function generation (EGCFG) circuit are calculated by following Eqn. (1) to Eqn. (8). The size of transistors are further fine-tuned based on the simulation results.

3.2 Gain Stage Circuit

Various types of gain stage circuits have been explored based on the dynamic range of gain, noise, power, dB-linearity, etc. requirements[7,9–12,16-17]. In the case of a CW radar lowest signal level can be -110 dBm or less. Therefore, a wide gain dynamic range is a significant requirement for VGA used in the CW radar.

Figure 4(a) shows the circuit diagram of an amplifying stage, and Fig. 4(b) shows the circuit diagram for its common

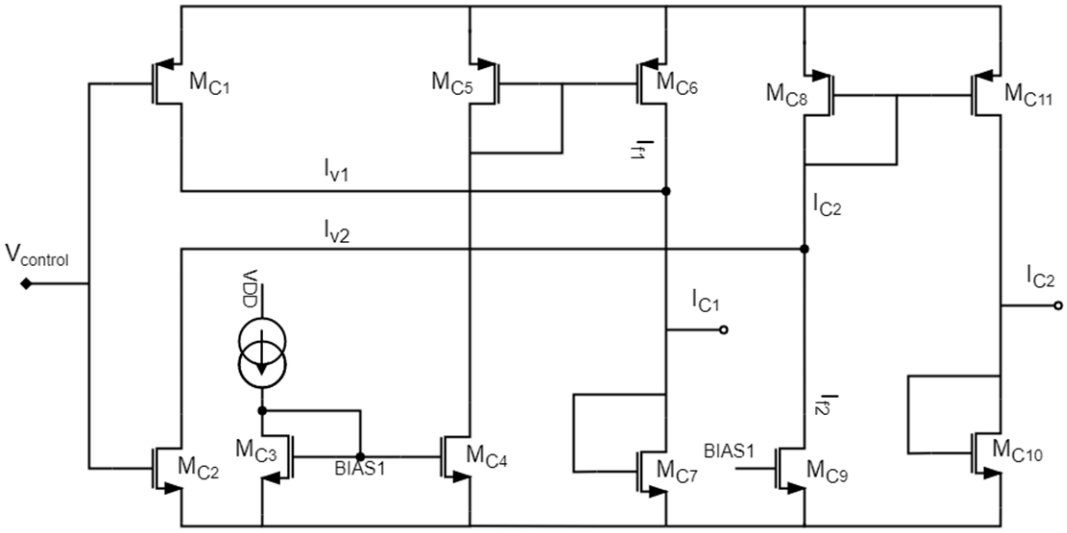

Figure 3. Circuit diagram of exponential gain control function generation.

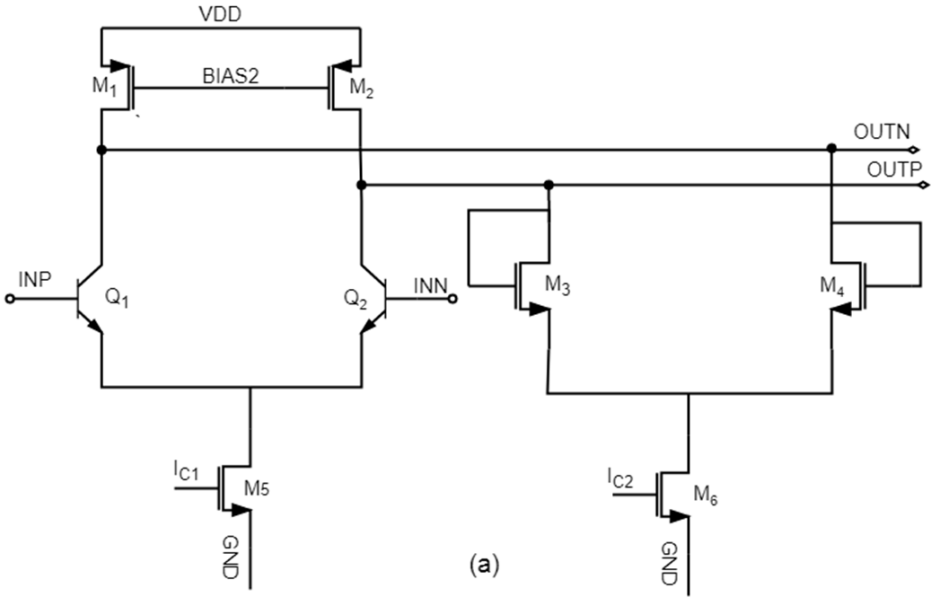

Figure 4. Circuit diagram of (a) gain stage, and its (b) common-mode feedback circuit.

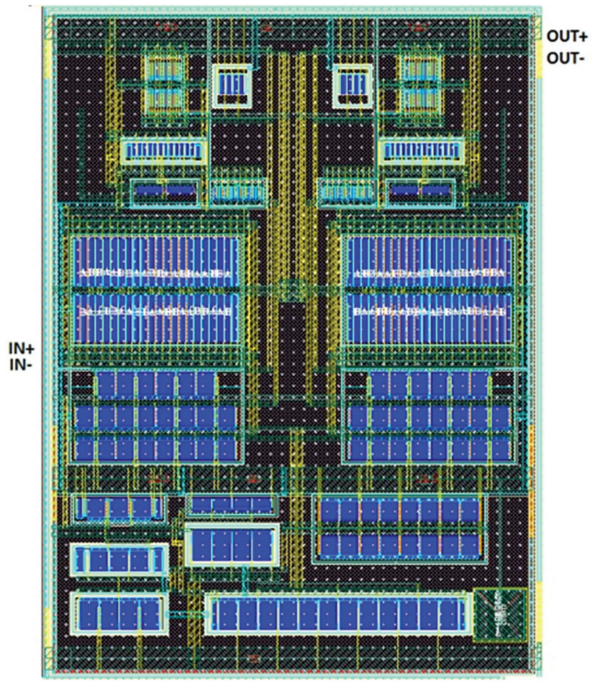

Figure 5. The Integrated layout of the VGA with a layout area of 0.0682 mm².

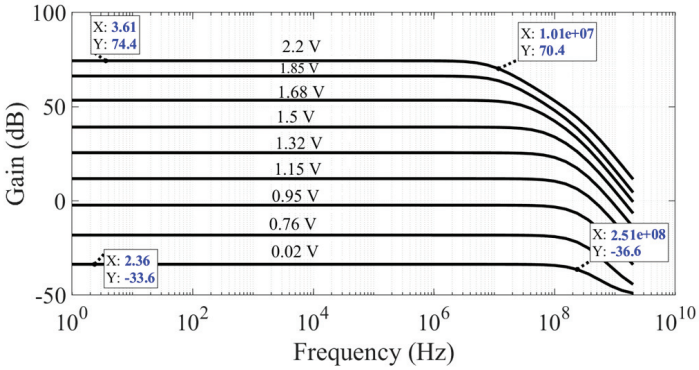

Figure 6. Gain characteristics of the VGA with frequency for different control voltages.

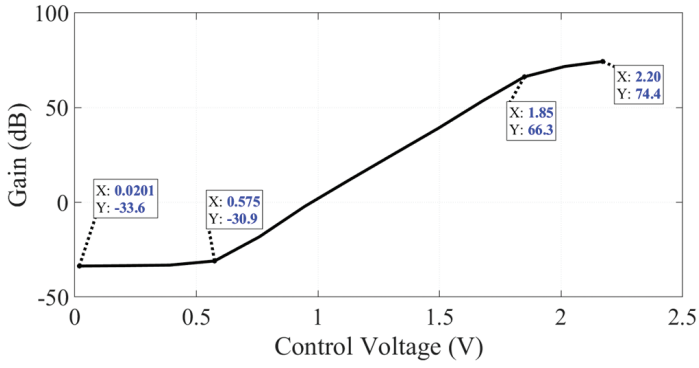

Figure 7. Variation of VGA gain for different control voltages.

mode feedback (CMFB) circuit. In the gain stage, input transistors are common-emitter-coupled BJT transistors, and the output is taken across the diode-connected MOS transistor. The voltage gain (A_v) for the proposed VGA configuration given in Fig. 2 is given by Eqn. (9)

$$A_v = \frac{g_{m-inBJT}}{g_{m-inNMOS}} \quad (9)$$

In Eqn. (9), $g_{m-inBJT}$ denotes the g_m for the input BJT transistor, and g_{m-} denotes the g_m of its output NMOS diode-connected transistor. Conventionally, in the gain stage, NMOS transistors are used at the input and output. However, the transconductance of NMOS is lower, and the noise contribution is higher than the BJT transistors. Therefore, emitter BJT transistors have been used at the input in the proposed gain stage for improved gain and noise performance.

3.3 Output Buffer

This VGA is proposed to be used between the low-pass frequency response filter and DC-offset cancellation circuit, as given in Fig. 1. Thus, its output impedance is not a low impedance or 50 Ω but a high impedance of the MOS gate. Therefore, an output buffer has not been incorporated into the design.

4. RESULTS AND ANALYSIS

This fully differential VGA's schematic and layout design has been carried out using a 130 nm SiGe BiCMOS process. The single gain stage designed for this VGA can have a maximum dynamic range of 60 dB. However, CW radar usually requires a wide dynamic range of 80 dB gain or more for its lowest signal on the receiver antenna. Therefore, 2-gain stages have been cascaded in the proposed VGA to realize the gain dynamic range of more than 100 dB. Figure 5 shows the combined layout of this VGA, having an area of 0.22 mm × 0.31 mm. The characteristics performance of the integrated VGA design has been done with Cadence electronics circuit automation (EDA) design flow. This VGA circuit's layout design has been done using Cadence Virtuoso Layout Suite. The performance of this VGA schematic has been verified and evaluated using post-layout simulation of the parasitic extracted model. The integrated VGA requires a power of 4.625 mW at the highest gain setting. Therefore, the power requirement of this VGA design is minimal, and it supports a wide gain dynamic range. Therefore, it has insignificant thermal heat dissipation.

Figure 6 gives the gain plots of the proposed VGA with frequency for different control voltages. It has demonstrated the highest gain of 74.4 dB at a -3 dB cut-off frequency of 10.1 MHz and the lowest gain of -33.6 dB at a -3 dB cut-off frequency of 251 MHz. This VGA uses BJTs as input transistors in the gain stage for improved gain performance.

Figure 7 shows the variation of gain with the control voltage of this VGA. It has shown a gain variation of -33.6 dB to 74.4 dB for the control voltage varying from 20 mV to 2.20 V. Hence, it has demonstrated a total gain dynamic range of 108 dB. This gain varies linearly from -30.9 dB to 66.3dB for the control voltage varying from 0.575 V to 1.85 V, as shown in Fig. 7. Therefore, this VGA has a linear gain dynamic range of 97.2 dB.

Figure 8 shows the input-referred noise variation with frequency for the proposed VGA. This demonstrated a very low flat noise performance of 2.4 nV /√Hz. The BJT used at the input of the gain stage has a very low flicker noise compared

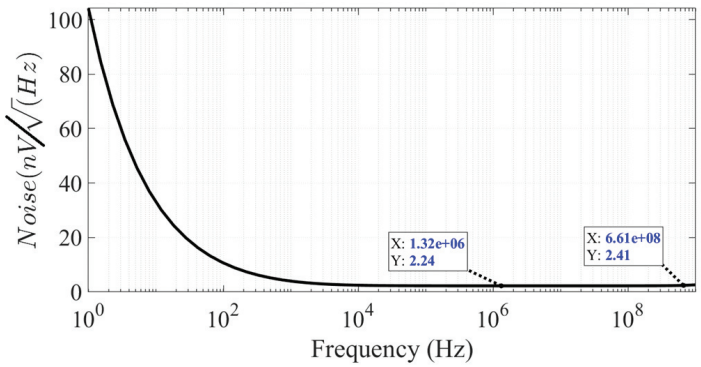

Figure 8. Variation of VGA input referred noise with frequency.

performance of the proposed VGA has been confirmed by its post-layout simulation results. The VGA has demonstrated a controlled gain range of 108 dB (-33.6 dB to 74.4 dB), specifically, 97.2 dB linear-in decibel gain behavior. Also, the proposed VGA has a 3-dB frequency up to 251 MHz with a flat input-referred noise of 2.4 nV /√ Hz, layout area of 0.0682 mm^2, and power requirement of 4.25 mW. In the future, this VGA design performance shall be evaluated as a part of an integrated radar transceiver, and suitable design modification will be carried out based on the integrated results. Further, this design can be modified for the gain performance across a wide-band frequency spectrum.

Table 1. Comparative performance of the latest VGA circuits

Reference	Ref[13]	Ref[14]	Ref[16]	Ref[17]	This work
Technology	65 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS	130 nm BiCMOS
Control type	Digital	Digital	Digital	Analog	Analog
Gain range (dB)	-24.7 to 34.9	-4.2 to 25.9	3.39 to 43.79	-20 to 21	-33.6 to 74.4
dB-linear gain range(dB)	59.7	30.1	40.4	41	97.2
Bandwidth (GHz)	0.27	0.63	0.014	0.58	0.01 to 0.251
Input Ref. noise (nV /√Hz)	22.3	22.4	29.3	NF=27 to 41 dB	2.4
Power (mW)	0.6	8.21	0.283	4.98	4.25
Area (mm^2)	0.05	0.11	7.02	0.1	0.0682

to NMOS. Hence, this VGA has shown outstanding noise performance.

Table 1, shows the relative behavior of the proposed VGA with state-of-the-art available VGA circuits. In comparison to the other VGAs designs13–17, this VGA has demonstrated superior performance with an overall gain range of -33.6 dB to 74.4 dB, dB-linear gain range of 97.2 dB, and input-referred noise of 2.4 nV /√Hz). The power requirement for the proposed VGA design is lower than the VGAs design in[14, 17], but higher than VGAs in[13,16]. Also, the silicon area requirement of the proposed VGA is lower than[14,16-17], and higher than[13]. The superior bandwidth supported by this VGA is due to using a pseudo-exponential generation circuit and a BJT-based amplifying stage with a better transconductance ratio and lower noise contribution. Apart from achieving the required performance in the post-layout simulation, this proposed differential VGA design offers the inherited advantages of differential architecture. These advantages include immunity to common mode noise, interference signal, and high gain compared to the single-ended design. Also, though this VGA has been designed targeted to a CW radar with low baseband frequency, like standard Gilbert cell architecture[9], this design can be adapted for other frequencies by suitable modification.

5. CONCLUSION

This manuscript has presented a miniaturized analog VGA implemented in SiGe BiCMOS technology with a dB-linear gain control generation circuit and a BJT-based amplifying stage. By considering applying this VGA for the CW radar, improvements have been demonstrated in the dB-linear gain range with minimum noise contribution. The superior

REFERENCES

1. Finocchiaro A.; Papotto G.; Ragonese E.; & Palmisano G. A 28-nm FD-SOI CMOS variable-gain amplifier with body-bias-based DC-offset cancellation for automotive radars. *IEEE Trans. Circuits Syst. II: Express Briefs.*, 2019, **66**(10), 1693-7. doi:10.1109/TCSII.2019.2921252.
2. El-Shennawy, M.;Al-Qudsi, B.;Joram, N.& Ellinger,F. A dual band FMCW radar receiver with integrated active balun and baseband AGC loop. *In* Proceedings 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore Marriott Waterfront, 2017. doi: 10.1109/ISCAS.2017.8050526.
3. Fioranelli, F.; & Le, Kernec J. Contactless radar sensing for health monitoring. Engineering and Technology for Healthcare. 2020 pp.24-29. doi: 10.1002/9781119644316.ch2
4. Lee, S.J.; Jung, J.H. & Yu, J.W. TX Leakage Canceller for Small Drone Detection Radar in 2-GHz Band. *IEEE Microw. Wirel. Compon Lett.*, 2020, **30**(2), 213-5. doi: 10.1109/LMWC.2019.2959441.
5. Park, J.; Park, S.; Kim, D.H. & Park, S.O. Leakage mitigation in heterodyne FMCW radar for small drone detection with stationary point concentration technique. *IEEE Trans. Microw. Theory Tech*., 2019, **67**(3), 1221-32. doi: 10.1109/TMTT.2018.2889045.
6. Pyo, G.; Kim, C.Y. & Hong, S. Single-antenna FMCW radar CMOS transceiver IC. *IEEE Trans. Microw. Theory Tech.*, 2016,**65**(3), 945-54. doi: 10.1109/TMTT.2016.2629476.
7. Yang, Y.; Gu, C.; Li, Y.; Gale, R. & Li, C. Doppler radar

motion sensor with CMOS digital DC-tuning VGA and inverter-based sigma-delta modulator. *IEEE Trans. Instrum. Meas.*, 2014, **63**(11), 2666-74.
doi: 10.1109/TIM.2014.2313032.

8. Kumar, V.; Saravanan, G.S. & Selvaraja, S.K. Bit topology selection algorithm in design of highly accurate CMOS digital attenuator for phased array system. *IOP Eng. Res. Expres*s., 2020, **2**(1), 015007-16.
doi: 10.1088/2631-8695/ab6266.
9. Dong, Y.; Kong, L.; Boon, C.C.; Yang, K.; Liu, Z.; Li, C. & Zhou, A. A wideband dB-linear variable-gain amplifier with a compensated negative pseudo-exponential generation technique. *IEEE Trans. Microw. Theory Tech*., 2021, **69**(6), 2809-21.
doi: 10.1109/TMTT.2021.3058266.
10. Kong, L.; Liu, H.; Zhu, X.; Boon, C.C.; Li, C.; Liu, Z. & Yeo, K.S. Design of a wideband variable-gain amplifier with self-compensated transistor for accurate dB-linear characteristic in 65 nm CMOS technology. *IEEE Trans. Circuits. Syst. I: Regular Papers.*, 2020, **67**(12), 4187-98.
doi:10.1109/TCSI.2020.2995725.
11. Kumar, V.; Selvaraja, S.K.; Saravanan, G.S. & Bhalke S.V. Experimental demonstration of 35 GHz RF-over-fiber silicon-photonics link. *In* Proceedings 2021 IEEE 2nd International Conference on Range Technology (ICORT), Balasore, Orissa, India.
doi: 10.1109/ICORT52730.2021.9581881.
12. Liu, H.; Zhu, X.; Boon, C.C. & He, X. Cell-based variable-gain amplifiers with accurate dB-linear characteristic in 0.18 µm CMOS technology. *IEEE J. Solid-State Circuits.*, 2014, **50**(2), 586-96.
doi:10.1109/JSSC.2014.2368132.
13. Park, G.H.; Kim, J.H. & Park, C.S. Low-power decibel-linear programmable-gain amplifier with complementary current-switching technique. *IEEE Trans. Circuits. Syst. I: Regular Papers*., 2023, **70**(5),1846 – 1855.
doi:10.1109/TCSI.2023.3241432.
14. Yin, Y.; Zhang, R.; Qi, H.; Wang, S.; Qiao, S.; Zhang, H. & Liu, L. Simultaneous bandwidth-extended and precisely-gain-controlled dB-Linear PGA based on active feedback and binary-weighted switches, *IEEE Trans. Circuits. Syst. II: Express Briefs.*, 2022, **69**(12), 4729-33.
doi: 10.1109/TCSII.2022.3205042.
15. Duong, Q.H.; Nguyen, T.K. & Lee, S.G. CMOS exponential current-to-voltage circuit based on newly proposed approximation method. *In* Proceedings 2004 IEEE International Symposium on Circuits and Systems (ISCAS), Vancouver, BC, Canada.
doi: 10.1109/ISCAS.2004.1329409.
16. Wang, L.S.; Ku, P.C.; Ko, P.T.; Chung, C.J. & Lu, L.H. A 40.4-dB range, 0.73-dB step, and 0.07-dB error programmable gain amplifier using gain error shifting technique. *IEEE Trans. Circuits Syst. II: Express Briefs*, 2018, **66**(7); 1109-13.
doi: 10.1109/TCSII.2018.2878919.
17. Song, X.; Lu, Z.H. & Yu, XP. An accurate dB-linear CMOS VGA based on double duplicate biasing technique. *IEEE Solid-State Circuits Lett.*, 2018, **1**(4), 98-101.
doi:10.1109/LSSC.2018.2855430.

ACKNOWLEDGEMENT

The authors would like to thank the Director, RCI, members of the RFSS group, and other competent authorities for the necessary support and encouragement in carrying out this research work.

CONTRIBUTORS

Dr Vijay Kumar obtained his PhD and M.Tech in CMOS/ BiCMOS Electronic-Photonic circuit design from Indian Institute of Science (IISc), Bangalore and working as Scientist 'D' at DRDO-RCI, Hyderabad.
Contribution to the current manuscript: He is primarily responsible for the conceptualisation, methodology, circuit/layout design, post-layout results analysis, and writing the manuscript.

Mrs Sujatha Ravichandran obtained her ME in Guided Missile Technology from Defence Institute of Advanced Technology (DIAT), Pune and working as Scientist 'H' and Group Director at DRDO-RCI, Hyderabad.
Contribution in the current manuscript: She has contributed towards the overall monitoring of the research work, review/ analysis of the results, and finalisation of the manuscript.