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A Temperature – and Supply- Variation Robust 2nd-Order Sigma-Delta Modulation for Capacitive Sensing

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A thesis submitted to the faculty of DGIST in partial fulfillment of the requirements for the degree of Master of Science in the Department of Information and Communication Engineering. The study was conducted in accordance with Code of Research Ethics[1]

01. 02. 2020

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[1] Declaration of Ethical Conduct in Research: I, as a graduate student of DGIST, hereby declare that I have not committed any acts that may damage the credibility of my research. These include, but are not limited to: falsification, thesis written by someone else, distortion of research findings or plagiarism. I affirm that my thesis contains honest conclusions based on my own careful research under the guidance of my thesis advisor.

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11. 28. 2019

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ABSTRACT

In this paper, I proposed a temperature- and supply variation robust 2nd-order sigma-delta modulation circuit for capacitive sensing. Capacitive sensing by conventional circuits is basically supply sensitive. Capacitance is sensed by reading the charge that is equal to the difference between the capacitance value of the capacitor and the capacitor to be sensed. In this method, the amount of charge is dependent on the supply, so it is insensitive to supply variation. In this paper, the capacitance is read by using the time determined by the discharge characteristics when a capacitor called T_{0V} meets the resistance component. The charge accumulated in the capacitor is certainly influenced by the supply value, but capacitive sensing is performed using the characteristic that the time taken to discharge the charge to zero is always constant. In the process, VCO (Voltage-Controlled-Oscillator) based ADC (Analog-to-Digital Converter) was used to increase the resolution by utilizing the noise shaping effect of sigma-delta ADC.

In the process, the resistor is switched to a switched capacitor to obtain robust characteristics against temperature variations. Unlike resistance whose values change with temperature, capacitance are relatively robust to temperature effects. By using the characteristics, a circuit having robust characteristics in temperature variation as well as robust in supply variation.

Keywords : Capacitance to digital converter, VCO quantizer, Sigma-Delta modulation, Supply variation, temperature variation

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I. INTRODUCTION

1.1 Motivation and Objective

The capacitive sensing method in the conventional capacitive sensing circuits using sigma-delta modulation (SDM) is shown in Fig.1.

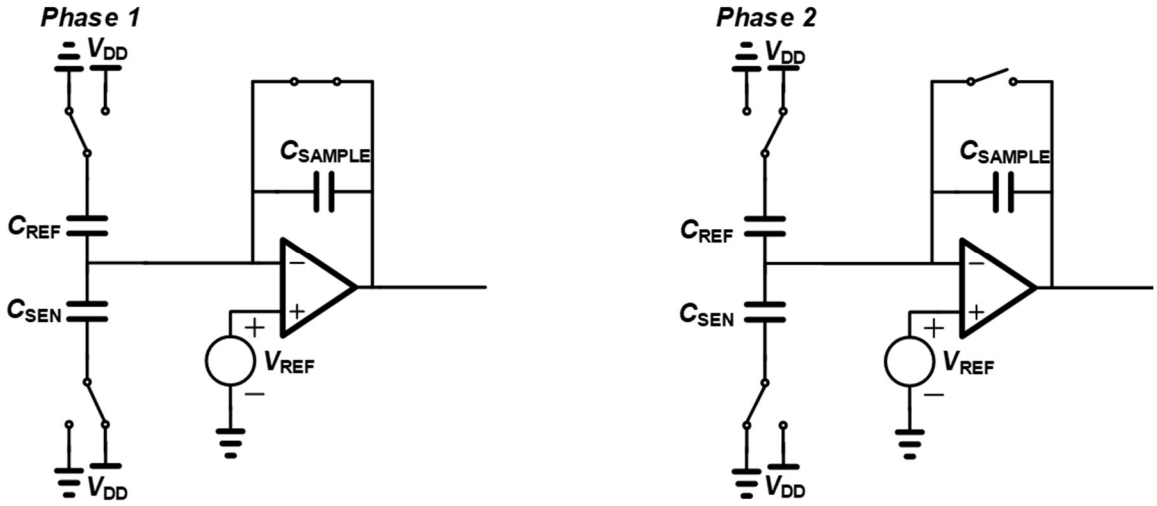


Figure 1 Conventional capacitance sensing technique

As can be seen in Figure 1, when φ_1, the nodes above and below C_{SENS} and C_{OFF} are located

at V_{DD} and GND, respectively. When φ_2, the upper node is switched from V_{DD} to GND, and the lower node is switched from GND to V_{DD}, and finally the value of C_{SENS} is determined by using the amount of charge due to the difference between the capacitor values of C_{SENS} and C_{OFF}. Depending on the digital output of the system, the C_{DAC} is connected in parallel to C_{SENS} or C_{OFF} to control the amount of charge in the integrator in the SDM method. Capacitive sensing circuits implemented in this way is a structure sensitive to supply voltage variation because the amount of charge varies depending on the supply voltage value. Finally, the output value of the entire system outputting the value of C_{SENS} depends on the state of the supply voltage, so the final output is unreliable. Therefore, we propose a temperature and supply variation robust 2^{nd}-order sigma-delta modulation circuits that sensing C_{SENS} value differently than conventional method. In a circuit consisting of a resistor and a capacitor, first apply a voltage of $V_{SENS} = -V_{DD}$ across the capacitor, and then discharge the capacitor. The time at which the voltage across the capacitor crosses 0V during discharge is independent of the supply value and is determined solely by the resistance value and the capacitor value. If the value of the capacitor is fixed, a SDM method is used to implement a system in which the average value of the R_{DAC}'s resistance is followed by a zero voltage across the capacitor.

Finally, the digital output of the capacitor value is the average value of R_{DAC} and is robust to supply voltage variation In addition, by replacing this Resistor DAC (Digital-to-Analog Converter) with a switched capacitor DAC, the voltage sensing part will be robust to temperature variation.

1.2 Thesis outline

In Chapter 2, we will talk about a 2nd-order sigma-delta modulation circuit that is robust to supply variations based on resistor DACs. We will discuss the VCO-based ADCs as well as the techniques that provide robust supply characteristics. We will introduce the full architecture created using these techniques, and also the schematic and layout. We will describe a circuit that can be robust to temperature variations by adding one technique to the circuit in Chapter 3, chaper2. We will examine the simulation and measurement results in Chapter 4. Finally, we will conclude in chapter 5.

II. Supply- Variation Robust 2nd-Order Sigma-Delta Modulation

2.1 Supply Independent Technique

The main difference between the existing sigma-delta modulation type capacitive sensing circuit and the proposed circuit is robust to supply variation. This characteristic is realized by using singularity of discharge time of capacitor.

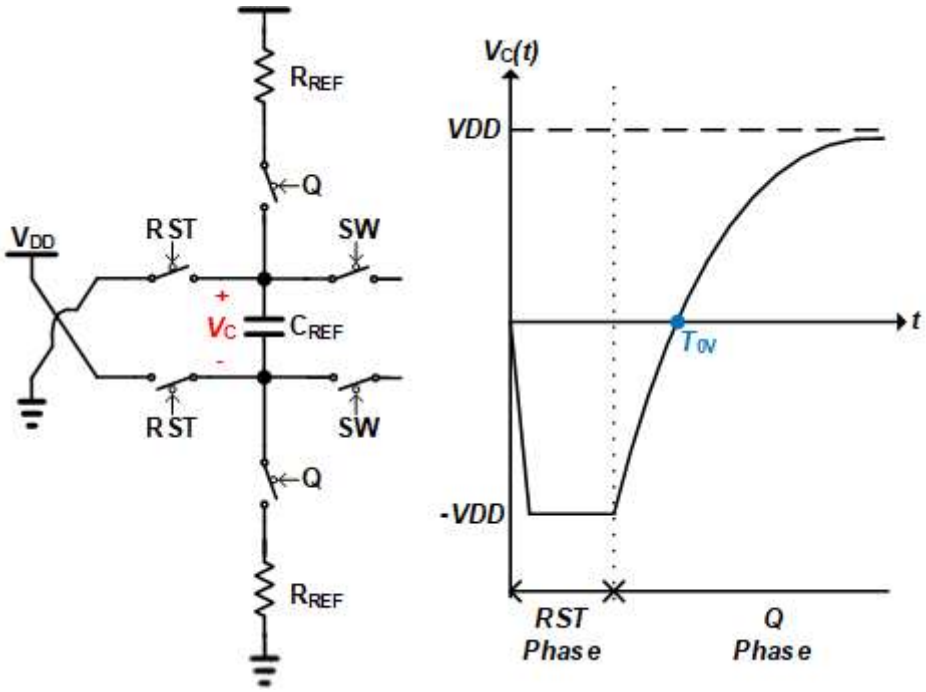


Figure 2 Operation of capacitive detector

RST, Q, and SW signals are designed so that the switch assigned to each signal does not turn

ON at the same time. First, -V_{DD} is applied across the C_{REF} in the RST phase. This voltage is then discharged in the Q phase. At this time, the voltage $V_C(t)$ applied to C_{REF} and the time when this $V_C(t)$ becomes 0V are as follows.

$$V_C(t) = V_{DD}(1 - 2e^{\frac{-t}{2R_{REF}C_{REF}}})$$

$$T_{0V} = 2\ln(2)\, R_{REF}C_{REF}$$

This $V_C(t)$ can be obtained using the current $I_C(t)$ flowing through C_{REF}.

$$I_C(t) = C_{REF}\frac{dV_C(t)}{dt} = \frac{V_{DD} - V_C(t)}{2R_{REF}}$$

$$\frac{dV_C(t)}{VDD - V_C(t)} = \frac{dt}{2C_{REF}R_{REF}}$$

$$\ln(V_c(t) - V_{DD}) = \frac{-t}{2C_{REF}R_{REF}} + D$$

$$V_c(t) = D'e^{\frac{-t}{2C_{REF}R_{REF}}} + V_{DD}$$

$$V_c(0) = -V_{DD} = D' + V_{DD}$$

$$\rightarrow D' = -2V_{DD}$$

$$\therefore V_C(t) = V_{DD} - 2V_{DD} \times D'e^{\frac{-t}{2C_{REF}R_{REF}}} = V_{DD}\left(1 - 2e^{\frac{-t}{2C_{REF}R_{REF}}}\right)$$

As can be seen from the above equation, T_{0V} at which C_{REF} becomes zero is independent from the value of V_{DD}. If the discharge time T_{0V} 'does not coincide with T_{0V}, the value of $V_C(t)$ is as follows.

$$V_C(t) = V_{DD}\left(1 - e^{\frac{-(T'_{0V} - T_{0V})}{2R_{REF}C_{REF}}}\right) = = V_{DD}\left(1 - e^{\frac{-\Delta t}{2R_{REF}C_{REF}}}\right)$$

Δ t, that is, the voltage determined by mismatch between T_{0V} and the value of T_{0V}' by the actually defined R_{REF} value, goes to the input of the integrator, the next block when SW is turned on. In the current proposed circuit, this T_{0V} time is set in advance. Since this T_{0V} is related to the time to eventually discharge, the value of this T_{0V} and the time of the Q phase are related. That is, it is important to adjust the average value of the R_{REF} resistance so that the time of the Q phase, which is the time of the phase for discharging the C_{REF}, and the T_{0V} determined by the C_{REF} and the R_{REF} which is determined by the Digital value and the sensor capacitance value, are important.

One important consideration in design is the switch. The switch used here is a MOSFET switch, not a mechanical switch. So ideally, the only resistor connected to C_{REF} is R_{REF}, but not only R_{REF} but also the turn-on resistance of the MOSFET.

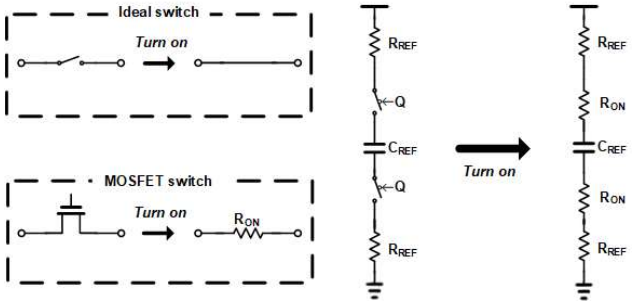


Figure 3 MOSFET switch's turn-on resistance

The MOSFET's turn-on resistance R_{ON} should be made smaller by increasing the switch MOSFET's aspect ratio W/L. Because the resistance value seen when the actual C_{REF} is discharging, not only the R_{REF} but also the R_{ON} value is shown. The formula for defining this R_{ON} is as follows.

$$R_{ON} = \left(\frac{W}{L}\mu_n C_{OX}(V_{DD} - V_{IN} - V_{TH})\right)^{-1}$$

The equation above shows that this R_{ON} cannot be free from supply variation. This means that T_{0V} can also be affected by supply variation. In order to minimize the effect of the change of R_{ON} due to the V_{DD} change, the design was carried out by increasing the W / L of the switch MOSFET to make the value of R_{ON} smaller and thus lowering the amount of change of R_{ON} itself.

2.2 Injection Locking Current Controlled Oscillator

The reference T_{0V} in the supply robust technique is very important. This technique is valid if this T_{0V} does not change during supply variation. We generate this T_{0V} using an injection locking current-control oscillator.

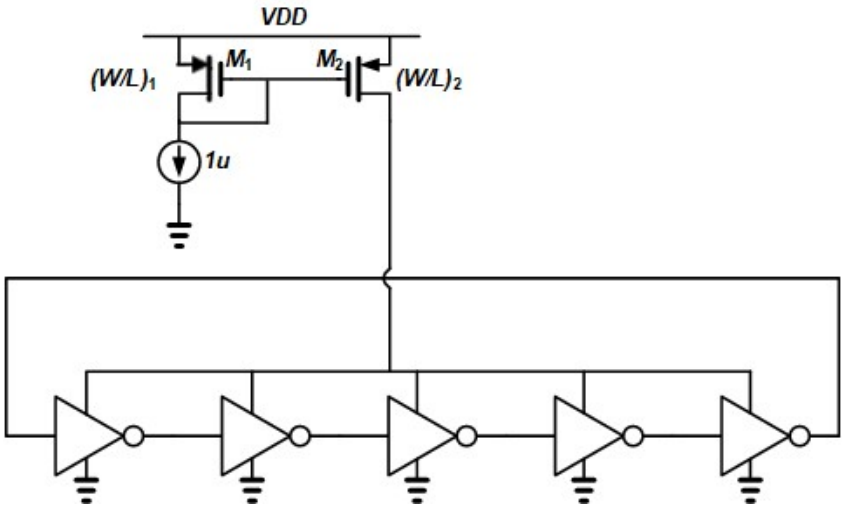


Figure 4 Current controlled oscillator

The overall structure is taken in the form of a Current-Controlled Oscillator current controlled oscillator. The reason for taking this form is that the free oscillation frequency of the ring oscillator changes in the supply voltage when brought into the VCO. Since the time of reference T_{0V} must also be independent of the supply, take it in the form of current controlled oscillator so that the effect of supply voltage is less affected by the free-running frequency of the ring oscillator. Using a current source of 1 uA, it delivers a constant current to the ring

oscillator through a current mirror. The output of this current controlled oscillator passes control logic to generate various control signals including T_{0V}. Here we use a technique called injection locking to ensure a certain frequency.

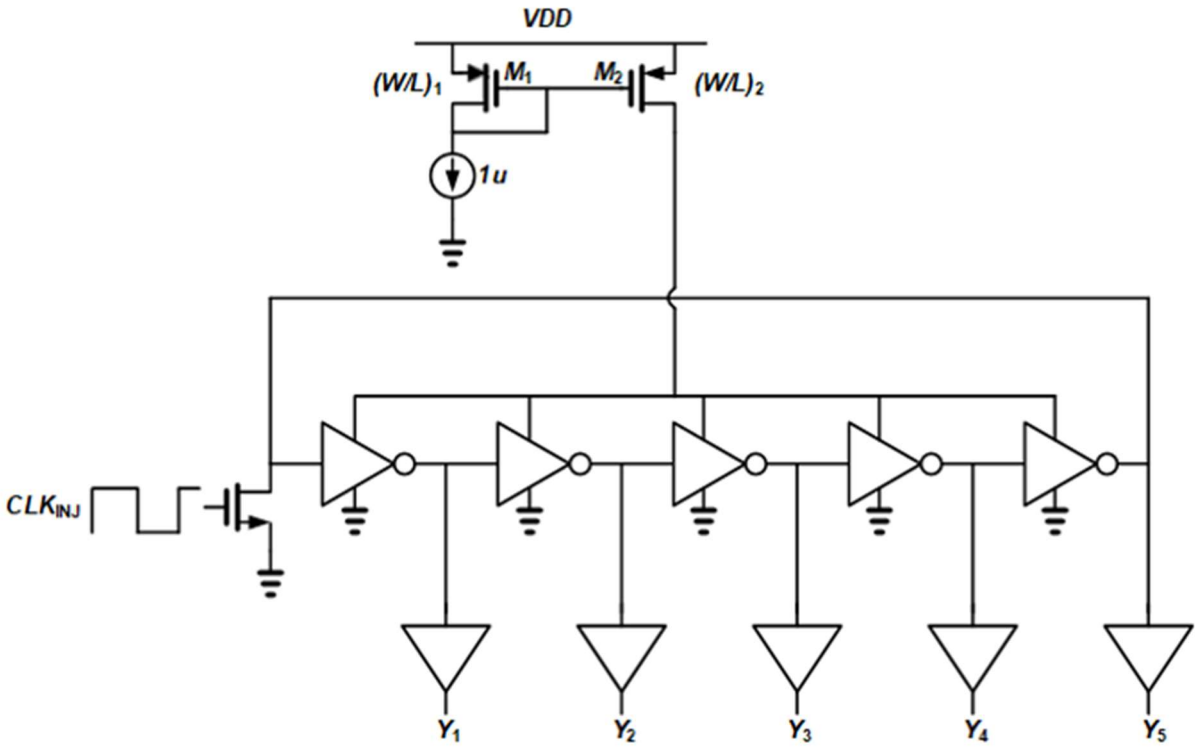


Figure 5 Injection locking current controlled oscillator

Even if the free running frequency of the ring oscillator is made through the actual process no matter how desired the frequency in the simulation, the desired frequency value may not

come out. Also, no matter how current controlled oscillator is implemented, we cannot guarantee that the effects of supply changes will not affect the ring oscillator. This results in an injection locking technique to make T_{0V} the most important reference constant under any circumstances. Injection locking is a technique that adjusts the frequency of the oscillator to the frequency of the reference clock by putting a reference clock externally.

The injection clock enters the input of the MOSFET additionally connected to one phase of the ring oscillator. When the injection clock is ON, the voltage of one phase of the ring oscillator is forced to VSS. By injecting this process in the form of the desired frequency, the frequency of the entire ring oscillator can be synchronized with the frequency of the injection clock. By using this technique, the output frequency of the current controlled oscillator can be locked to our desired frequency, 4 MHz.

Here, the swing range of the output of the injection locking current controlled oscillator is set to within 1V. This is because the bias voltage of the ring oscillator does not exceed 1V because the CCO structure is set to flow constant current. This may not be a big problem for a

nominal supply voltage of 1.4V, but a problem occurs for a supply with a large value such as 3V. If the supply of digital control logic is 3V, the threshold voltage that determines 0 and 1 in the control logic is 1.5V with the value of V_{DD} / 2. Since the output of the current controlled oscillator is swinging within 1V, it appears to be all zeros because the control logic reference does not appear to exceed the threshold voltage. To solve this problem, we put a buffer with two supplies at the output of the current controlled oscillator.

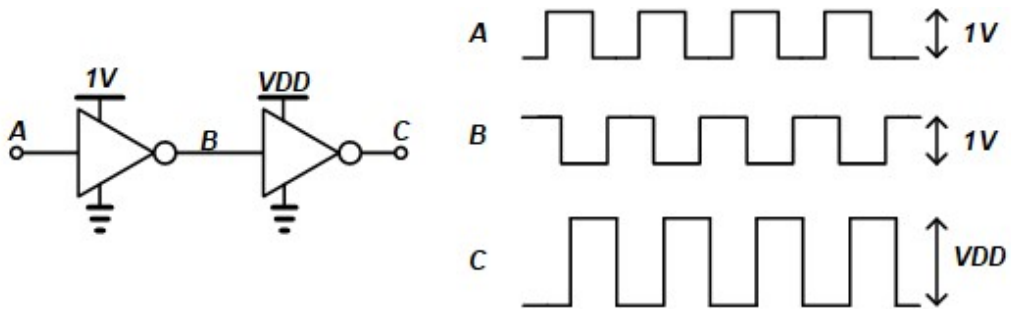


Figure 6 Buffer with two different supplies

First, make a square wave with 1V swing by passing the first inverter with 1V supply, and then go through the inverter with the actual supply value. The size of the inverter is important here. In the case of the first inverter, the swing of the output of the current controlled oscillator has a range of 0 ~ 1V, so it is safe to take the size of PMOS and NMOS of general inverter. In

other words, the pull-up power and the pull-down power may be the same. However, the second inverter must be designed so that the force to pull down the output is stronger. By increasing the pull-down force, it is possible to generate an output swing that matches the input swing even when the maximum value of the input swing is low.

2.3 VCO Based ADC

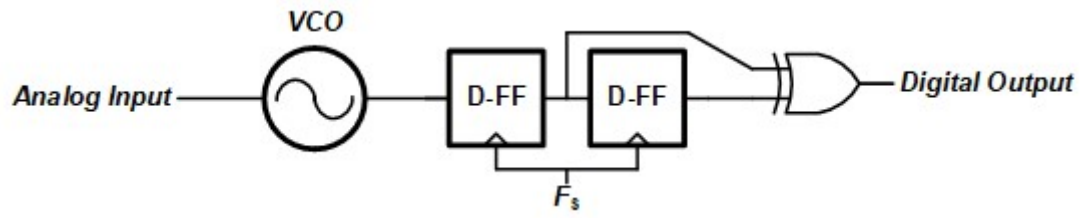


Figure 7 VCO based ADC

This circuit utilizes a VCO-based ADC to convert capacitance to digital values. VCO based ADCs are basically ADCs in the time domain, not ADCs in the voltage domain. The output frequency of the VCO depends on the analog input value. Detect the positive edge or negative edge of the output frequency using the VCO quantizer on the back. The VCO quantizer consists of two D-flipflops and one XOR. The two signals sampled by D-flipflop are compared using the XOR gate. Since the two inputs must be different for XOR to be 1, the edge of the VCO output can be detected through the output of the XOR. These blocks are assigned to different phases of the VCO. The final value of D_{out} is added by adding the output of XOR from all blocks. Detecting the edge of the VCO output is the same as detecting the phase of the VCO output and outputting 1 to the output every π.

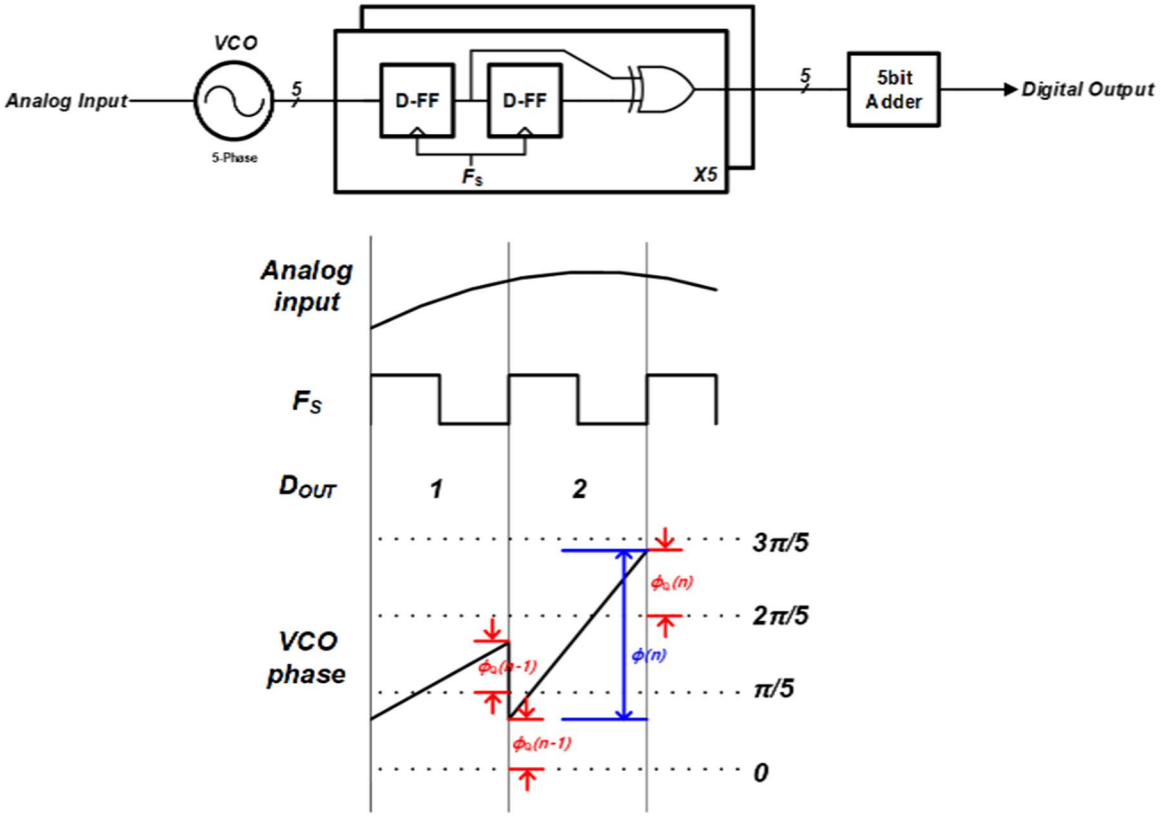


Figure 8 Operation and waveform of VCO based ADC

Figure 8 is a timing diagram to explain the operation of the VCO based ADC. Depending on the analog input, the output frequency of the VCO changes, which means that the amount of phase increase in a sampling clock changes. The result is output to the digital output. It is not just the amount of phase increase that affects the digital output. Residues in the previous sampling clock will also be affected.

As mentioned earlier, detecting an edge is the same as detecting when the output phase of

the VCO is a multiple of π. Within a sampling clock, the digital output changes depending on how many times the phase passes multiples of π. The important point here is that the digital output value is reset when the next sampling clock is reached, but the VCO output phase is not reset so that residues up to the next π will affect the digital output at the next sampling clock. Here, residue is expressed as $\phi_Q[n]$, which is equivalent to quantization error. If the phase increase by analog input is expressed as $\phi[n]$, digital output is expressed by y[n], the digital output can be expressed as

$$\text{Digital output } y[n] = \frac{5}{\pi}(\phi[n] + \phi_Q[n-1] - \phi_Q[n])$$

The above formula is transformed into z domain as follows.

$$\text{Digital output } Y[z] = \frac{5}{\pi}(\phi[z] + (z^{-1} - 1)\phi_Q[n])$$

In the above equation, the quantization noise is multiplied by $(z^{-1}-1)$, which has a high pass filter in the z domain. In other words, “first order noise shaping” was made. The noise shaping technique minimizes quantization noise in bandwidth. In other words, we can think of quantization noises as being "pushed" out of bandwidth. Currently, only the first order noise shaping is seen when looking at VCO ADC, but the NTF of quantization noise can be found in the entire block including the integrator.

2.4 Full Architecture

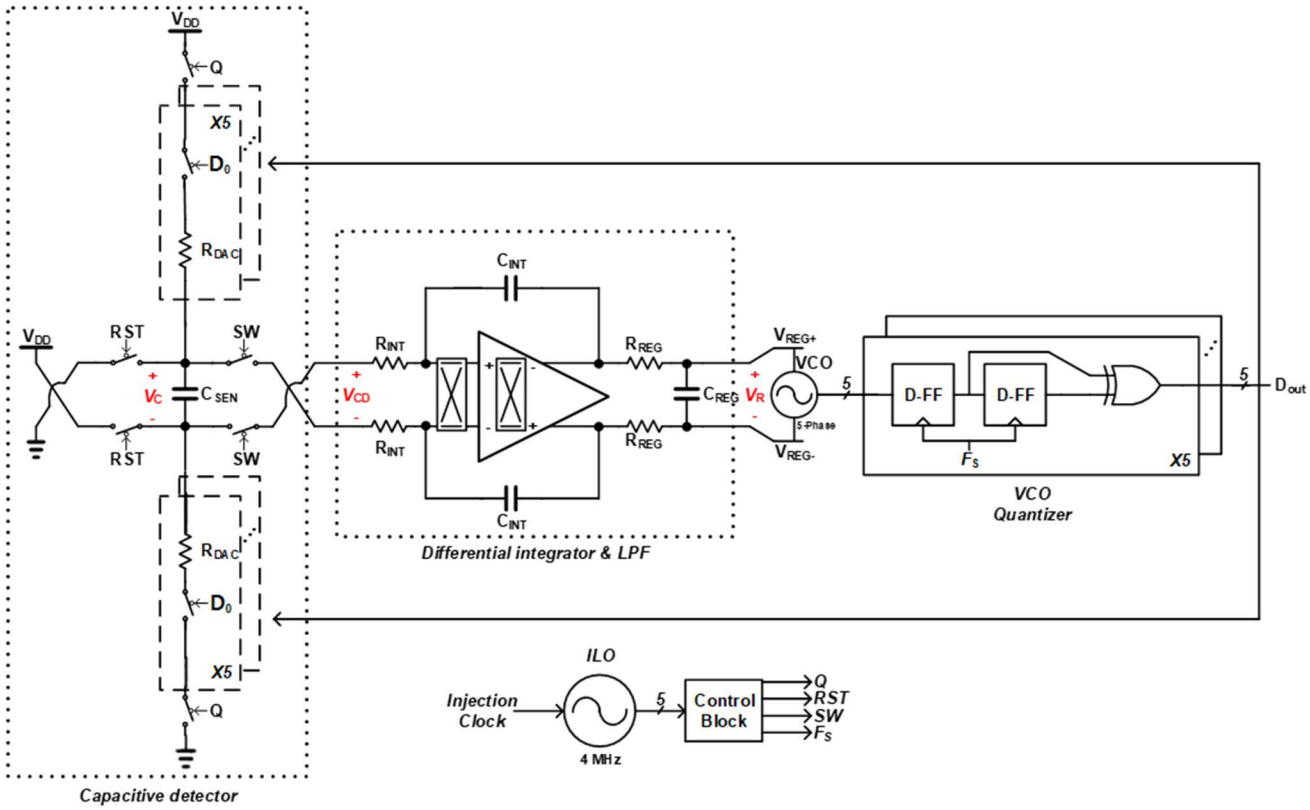


Figure 9 Full architecture of supply variation robust circuit

This circuit is a 2nd-order modulation for capacitance sensing circuit that is robust to supply variation designed by combining the aforementioned techniques. First, after $-V_{DD}$ is charged to C_{SEN} through RST phase and when Q phase, it is discharged by R_{DAC} and C_{SEN}. V_{CD}, which is the remaining value, enters the integrator input. The reason for using the Integrator is to compare V_{CD} with 0V. Using a common comparator and a 0V reference in the comparison may be affected by ground noise by the ground used as the reference. Instead, by using a differential integrator, the V_{CD} can be compared to 0V using the inherently virtual short characteristics

exhibited by the differential structure, reducing the effects of ground noise. A chopping technique has been added to remove the integrator's offset and flicker noise. Noises moved to high frequencies by the chopping technique are removed by an RC low-pass filter. The output goes to the input of the VCO. The VCO frequency determined by this input converts the VCOQ into a digital value, and the D_{OUT} value from the process adjusts the R_{DAC} value to help the average value of T_{0V} 'approach the T_{0V} value set as the reference. In the case of the Resistor DAC, five R_{DAC}s are connected in parallel, and the five Resistor DACs determine how many DACs are turned on by the 5-bit D_{OUT}.

In the above process, T_{0V} 'determined by D_{OUT} is somewhat different from T_{0V}. If the V_{CD} value is positive, T_{0V} 'is smaller than T_{0V}. On the contrary, negative value means that T_{0V}' is larger than T_{0V}. It is the resistor DAC that can be controlled to bring T_{0V} 'close to T_{0V}. That is, according to the value of the current V_{CD} value, the Resistor DAC should be controlled in a direction that can compensate the error of the V_{CD} value is 0. In other words, the input of the VCO, V_R, should be adjusted in such a way as to compensate for the corresponding error. The integrator of the currently proposed circuit can perform this operation.

$$\mathrm{H_{INT}}(s) = -\left(1 - e^{\frac{T_{0V}}{5}\frac{1}{2R_{INT}C_{SEN}}}\right)\frac{C_{SEN}}{sC_{INT}} \cong -\frac{T_{0V}/5}{2R_{INT}C_{INT}}$$

As can be seen from the above equations, the integrator gain has a negative value. That is, the difference between the values of 0V and V_{CD} affects the output of the integrator in the opposite polarity direction. The output frequency of the VCO also has a characteristic that is proportional to the output of the integrator, so that in the end D_{OUT} is compensated to make the average value of T_{0V} 'close to T_{0V}. In addition, since the integrator's output acts as a bias for the VCO, the effect of supply is removed from the VCO's operation.

2.4.1 Control Block

The control block receives the output of the current controlled oscillator and generates control signals such as RST, SW, Q and Chopping control signals.

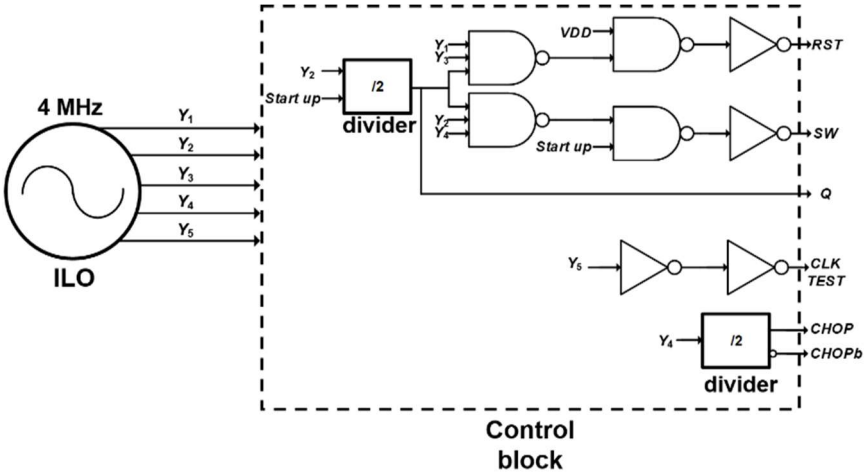


Figure 10 Control block of circuit

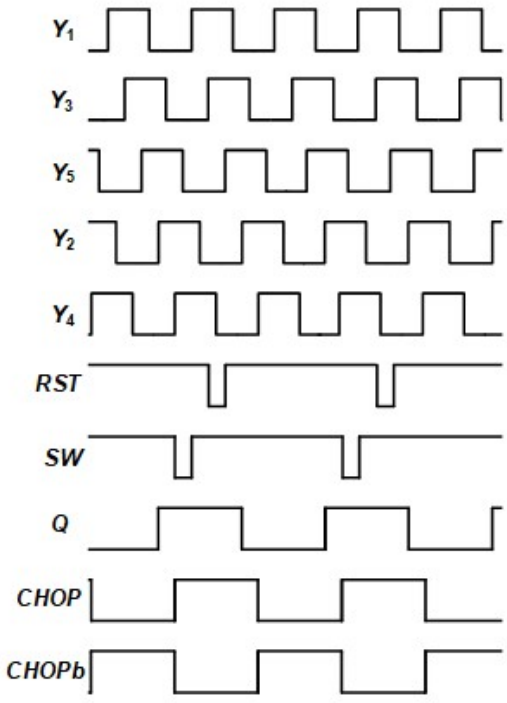


Figure 11 Input and output waveform of control block

Four phases of the five phase inputs are used to generate the control signal, and one signal is used as a test point to confirm the operation of the current controlled oscillator. The overall frequency of the signal is 2 MHz, coming from the frequency divider to the output of the 4 MHz current controlled oscillator. The signal that made the frequency of Y1 halved becomes Q, and the signals that are made by dividing the section in more detail based on this Q are RST and SW. Since the period during which Q is turned on is set at T_{0V}, T_{0V} is set at 250 ns. In the case of chopping signal, Y3 is generated through a divider.

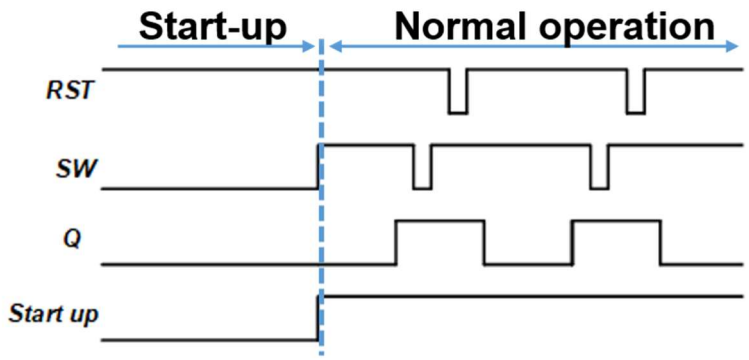


Figure 12 Start-up operation

In the case of the start-up signal, when the circuit is first driven, it is a signal to make the value of V_R, the input voltage of the VCO, high enough to enable the initial driving of the VCO. When this start up signal is 0, RST is turned off and Q and SW are turned on to increase V_R.

2.4.2 Block Diagram

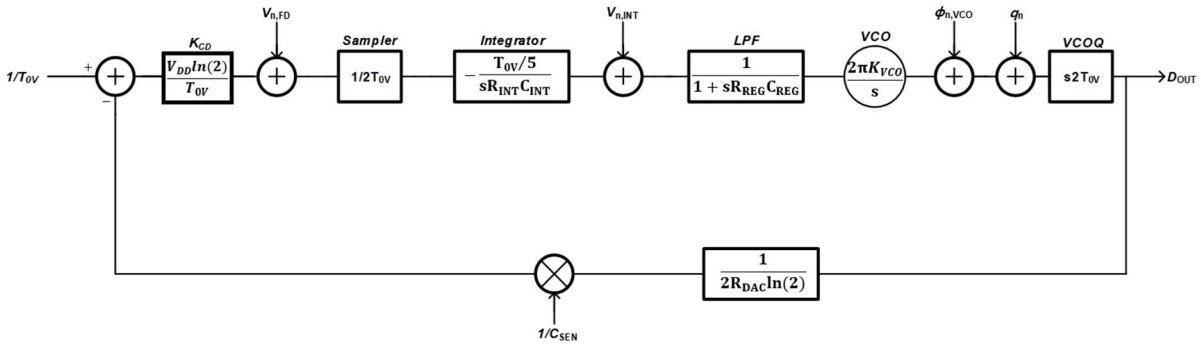


Figure 13 Block diagram of circuit

The figure above shows a block diagram of the circuit to obtain the transfer function. Dominant noises are represented by adding them to the back of the block that is the noise source. K_{CD} is the gain of capacitive detector and its value is as follows.

$$K_{CD} = T_{0V} * VDD * \ln(2)$$

Through the block diagram above, the transfer function from $1/T_{0V}$ to D_{OUT} and C_{SEN} to D_{OUT} are as follows.

$$\frac{D_{OUT}}{\frac{1}{T_{0V}}} = \frac{K_{CD} \times sampler \times Int \times LPF \times VCO \times VCOQ}{1 + K_{CD} \times sampler \times Int \times LPF \times VCO \times \frac{1}{2R_{DAC}\ln(2)} \times \frac{1}{C_{SEN}}}$$

For convenience, the feedforward gain is set to A, and the feedback factor excluding C_{SEN} is marked as β.

$$\frac{\mathrm{D_{OUT}}}{\frac{1}{T_{0V}}} = \frac{A/s}{1 + (\frac{A\beta}{s}) \times \frac{1}{C_{SEN}}} \approx \frac{\frac{A}{s}}{\left(\frac{A\beta}{s}\right) \times \frac{1}{C_{SEN}}} = \frac{C_{SEN}}{\beta} = 2R_{DAC}ln(2)C_{SEN}$$

$$\frac{D_{OUT}}{C_{SEN}} = \frac{1}{\beta \times T_{0V}} \frac{2R_{DAC}ln(2)}{T_{0V}}$$

The above equation shows the relationship between C_{SEN} and D_{OUT}. Since T_{0V} is a constant provided as a reference, the range that C_{SEN} can theoretically change is determined by (R_{DAC} / D_{OUT}). The current circuit's R_{DAC} is set to 50 kohm and D_{OUT} is 5bit, so the (R_{DAC} / D_{OUT}) can vary from 50 kohm maximum to 10 kohm minimum. Since T_{0V} is set to 250 ns through the injection locking current controlled oscillator and control block, the following is the range to detect C_{SEN} using this.

$$\mathrm{C_{SEN,MIN}} = \frac{T_{0V} \times D_{OUT}}{2R_{DAC} \times \ln(2)} = \frac{250 \times 10^{-9}}{2 \times 50 \times 10^{3} \times \ln(2)} = 3.6\ pF$$

$$\mathrm{C_{SEN,MAX}} = \frac{T_{0V} \times D_{OUT}}{2R_{DAC} \times \ln(2)} = \frac{250 \times 10^{-9}}{2 \times 10 \times 10^{3} \times \ln(2)} = 18\ pF$$

The transfer function of quantization noise can be obtained as follows.

$$\frac{\mathrm{D_{OUT}}}{\mathrm{Q_n}} = \frac{\mathrm{s2T_{0V}}}{1 + (\frac{\mathrm{A\beta}}{\mathrm{s}}) \times \frac{1}{\mathrm{C_{SEN}}}} \approx \frac{s2T_{0V}}{\left(\frac{A\beta}{s}\right) \times \frac{1}{C_{SEN}}} = \frac{s^2 C_{SEN} \times 2T_{0V}}{A\beta}$$

The above equation shows that quantization noise is 2nd-order noise shaping.

2.5 Schematic and Layout

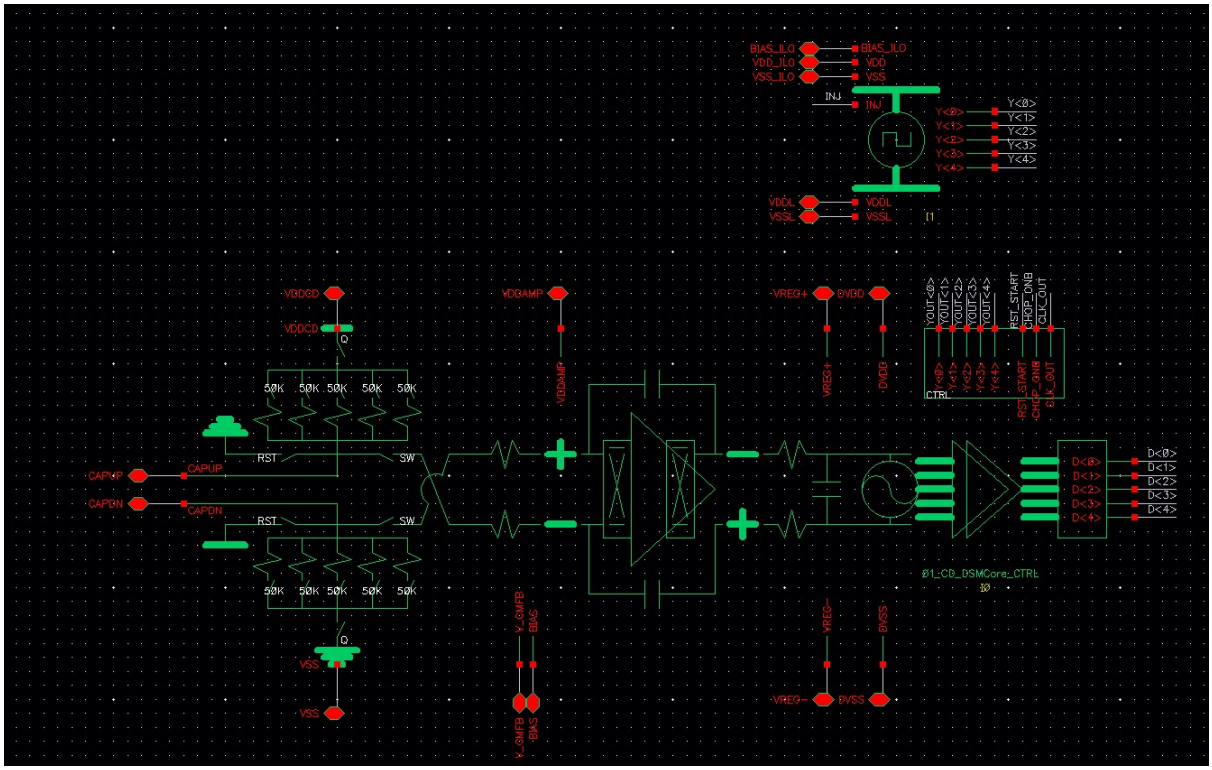


Figure 14 Schematic of full architecture

The figure 14 is schematic designing the full architecture through cadence simulation program. The upper oscillator block is the injection locking oscillator, and the large block below is the entire circuit including the control block.

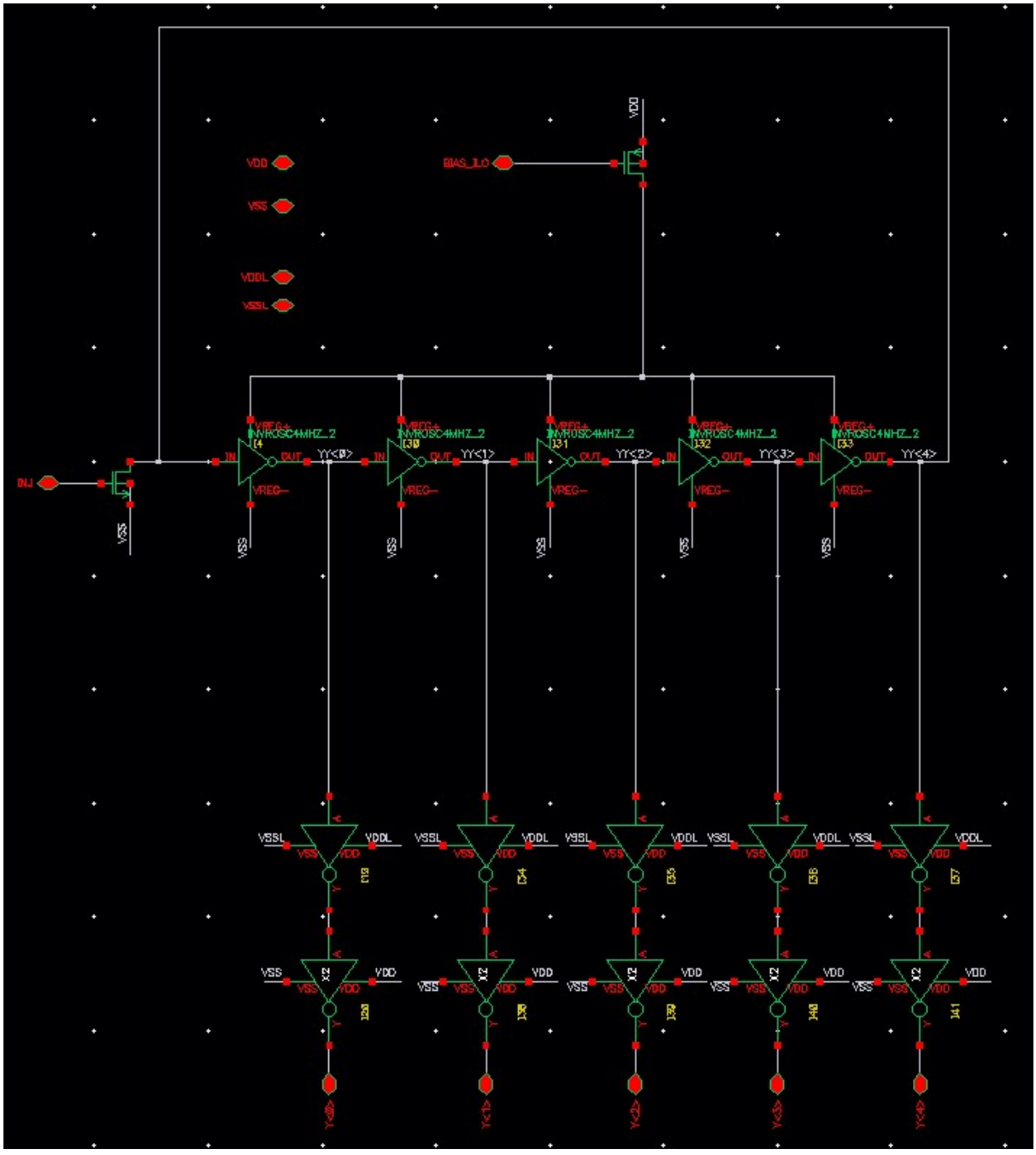


Figure 15 Schematic of 5-phase injection locking current controlled oscillator

The figure 15 is the injection locking current controlled oscillator. Since the 5phase ring oscillator is based, five inverters are configured in a ring shape, and there is a PMOS transistor

that acts as a current mirror on the ring oscillator. On the far left, a MOSFET for injection locking is attached to one phase of the ring oscillator. Each phase of the ring oscillator has a buffer that enters the control block.

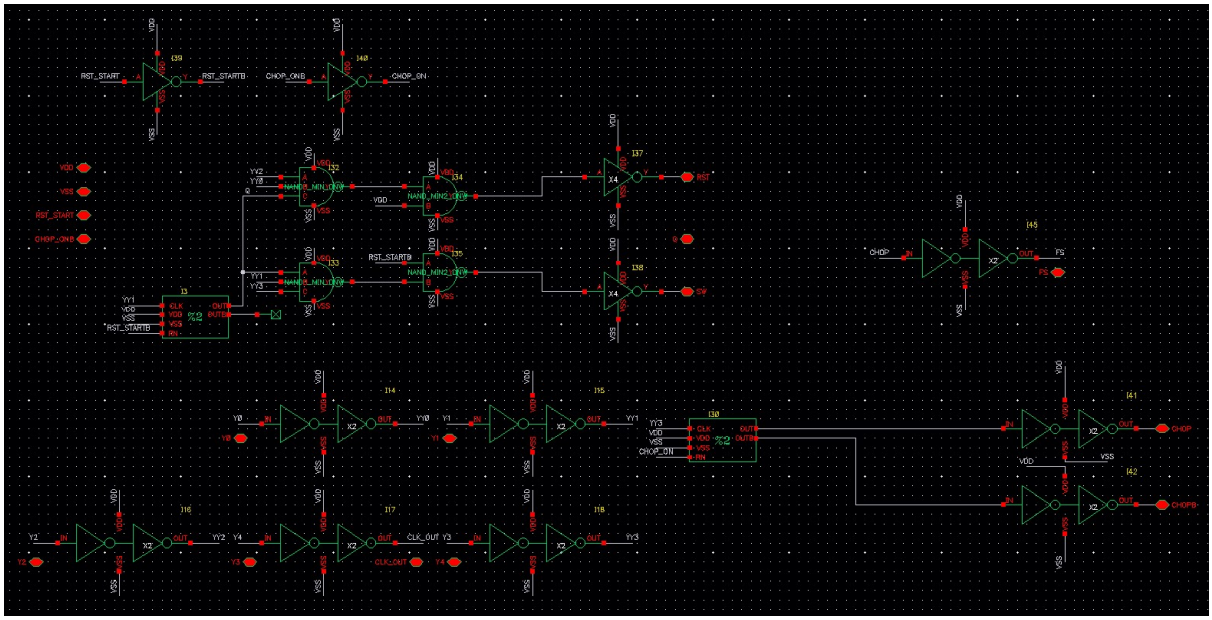


Figure 16 Schematic of control block

The figure 16 is a control block. This block produces basic RST, Q, SW and chopping signals. The lower left buffers are the buffers for the input signal. When control signals generated through the control block are output to the output, they are output after passing through the buffer.

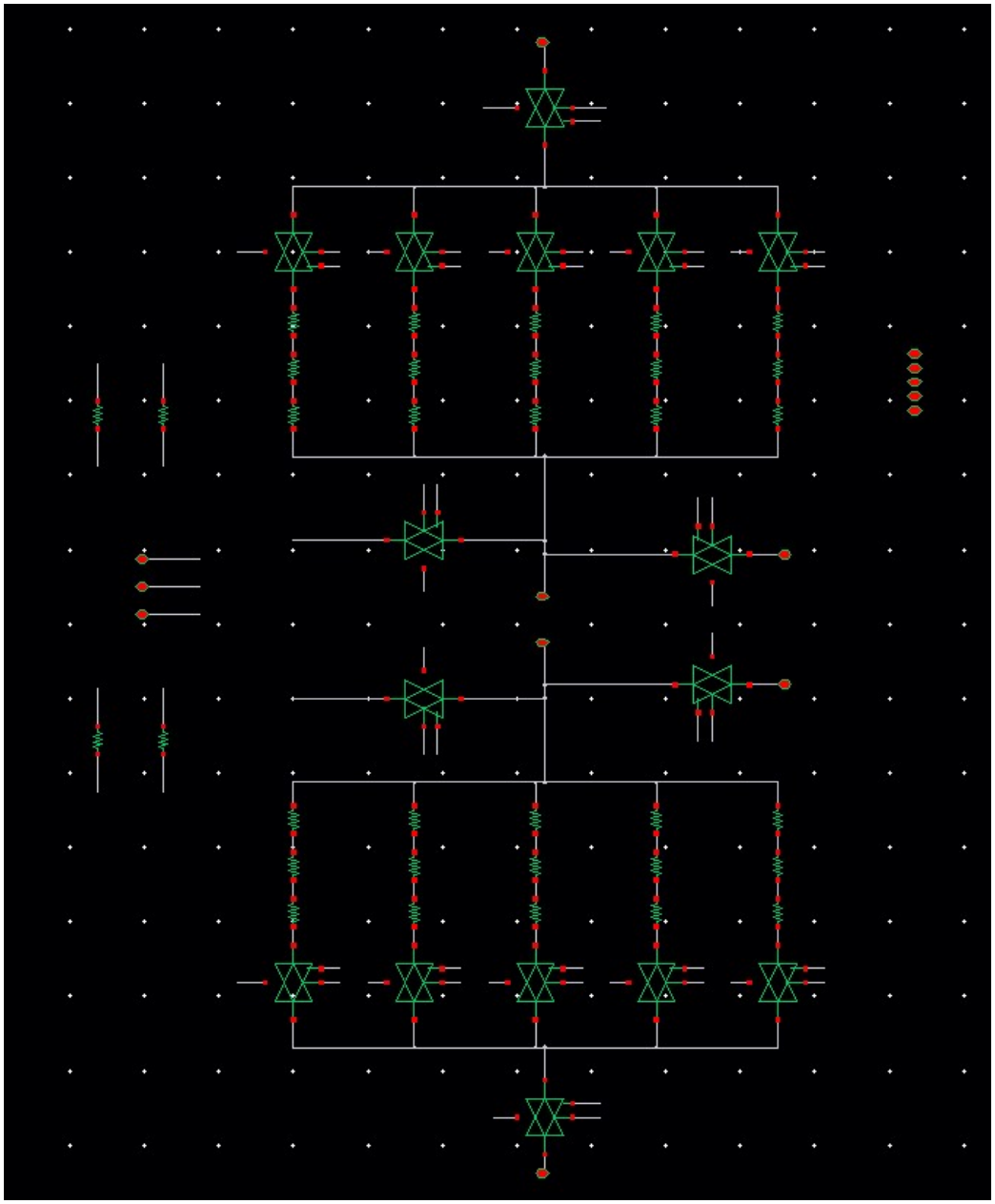


Figure 17 Schematic of capacitive detector

The figure 17 is a capacitive detector. Five Resistor DACs are connected in parallel and each DAC determines whether it is turned on or off by a switch controlled by D_{OUT}. The one R_{DAC} value is 50 kohms.

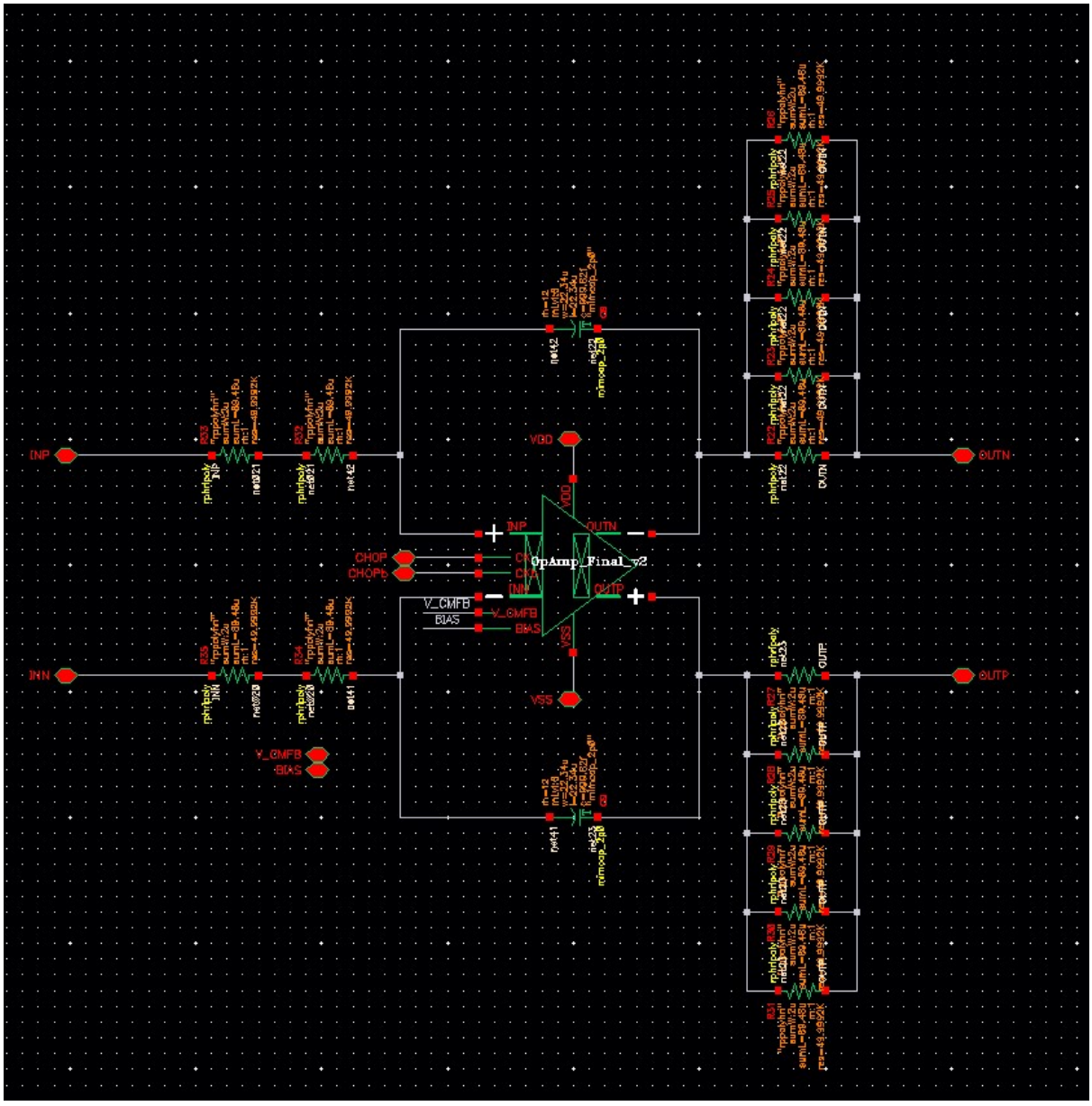


Figure 18 Schematic of differential integrator

The figure 18 is a differential amplifier. The two signals that enter the center of the differential opamp are CHOP and CHOPb, which control the chopper to remove the opamp's offset and flicker noise. 100 kohm was used as the R_{INT} and 1 pF was used as the C_{INT}.

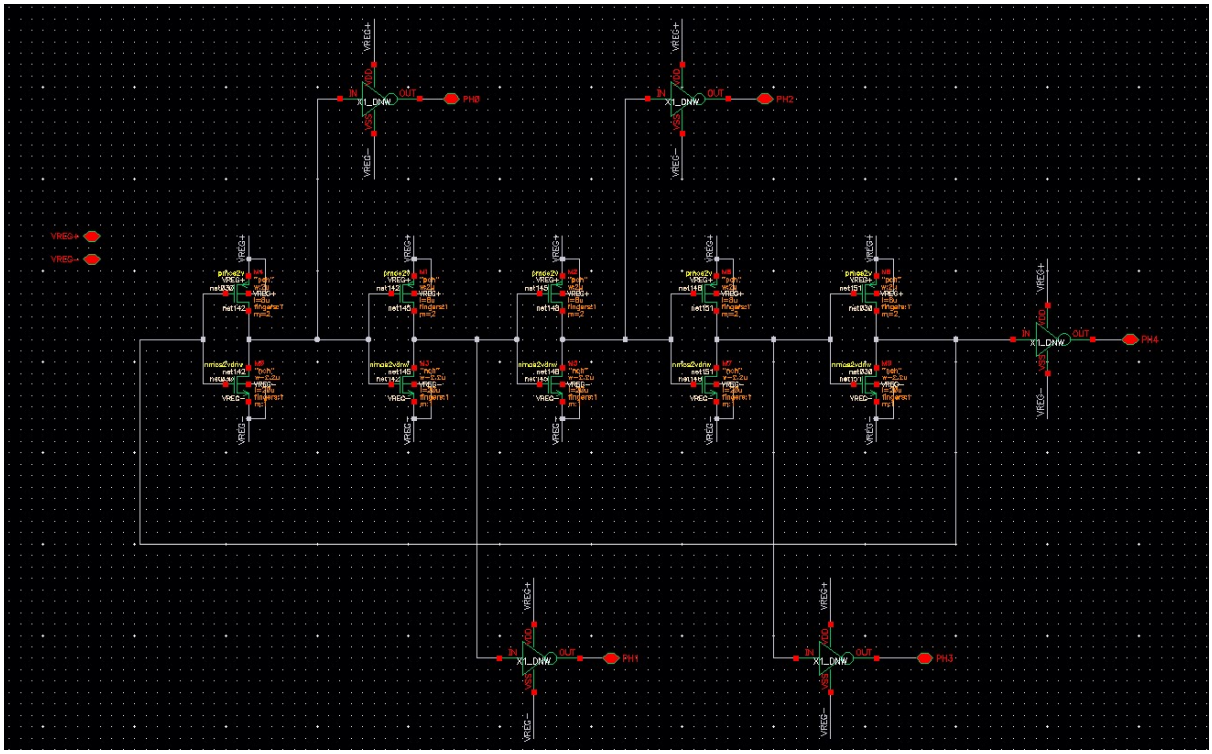


Figure 19 Schematic of VCO

The figure 19 is a schematic of a VCO. As it is a 5phase oscillator, five inverters are connected in the form of rings. The output of each phase is equipped with a buffer. The supply of this buffer is also composed of V_R, the bias of the VCO, so that the buffer is not affected by the supply at all.

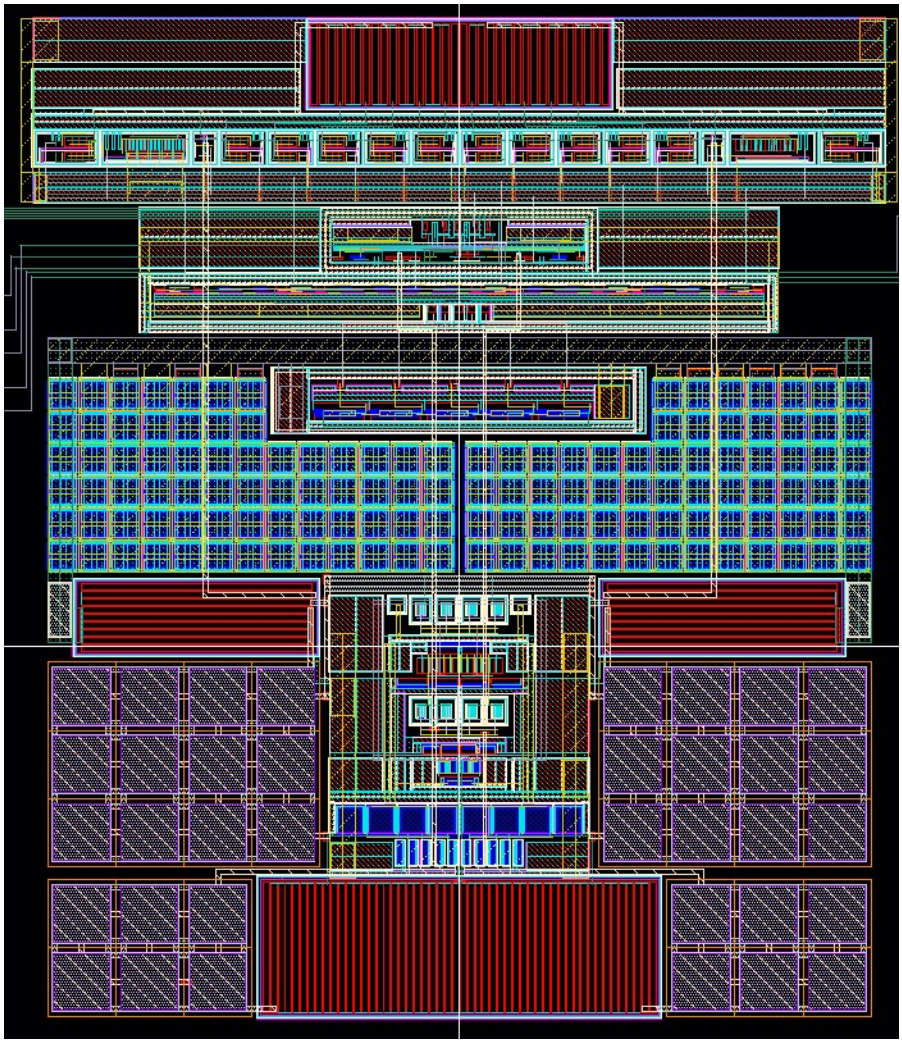


Figure 20 Layout of full architecture

The figure 20 shows the layout of the core, excluding the PAD and input output buffer. TSMC 180 nm process was used. At the top is the layout of the capacitive detector, underneath the control logic. The bottom part is the layout of the rest of the block, such as the integrator.

III. Temperature- and Supply- Variation Robust 2nd-Order Sigma-Delta Modulation

The circuit implemented earlier is a circuit that is robust to supply. Here, the first part that needs to be modified in order to have a temperature resistant characteristic is the capacitive detector. In a capacitive detector, a constant T_{0V} must be maintained even during supply or temperature variations, which cannot be constant under the influence of temperature variation in a circuit implemented earlier. This is because the resistance value of the R_{DAC} varies with the temperature according to the temperature coefficient of the R_{DAC}. In the proposed circuit, the R_{DAC} is implemented using a switched capacitor rather than a resistor to produce a constant T_{0V} even during temperature variation.

3.1 Switched Capacitor DAC

In order to obtain the robustness against temperature variation, we implemented the R_{DAC} as a switched capacitor DAC using a capacitor. Unlike resistors, capacitors are not sensitive to temperature changes. This is used to replace the resistor with a switched capacitor using a capacitor. If you look at the operation of the switched capacitor, you can see the operation as if the resistor is connected.

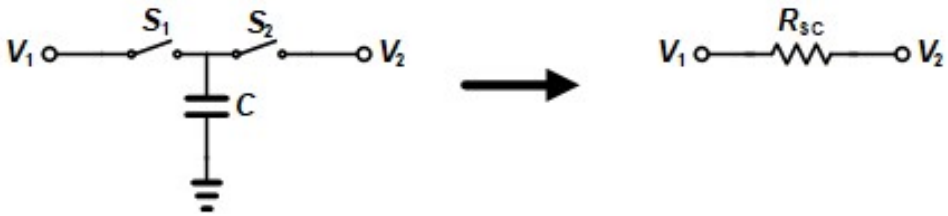


Figure 21 Switched capacitor acting like resistor

Suppose that S1 and S2 do not turn on at the same time. When S_1 is turned on, a charge with CV_1 accumulates in C. After that, when S_1 is turned off and S_2 is turned on, the charge of CV_2 must be accumulated in C. Therefore, the charge of C (V_1-V_2), which is a difference from the existing CV_1, moves toward the V_2 node. Moving the charge means creating a current. If the cycle of turning on S_1 and S_2 is f_{SC}, the following equation is established.

$$C(V_1 - V_2) = I \times \frac{1}{f_{SC}}$$

$$\frac{(V_1 - V_2)}{I} = R_{SC} = \frac{1}{C \times f_{SC}}$$

The movement of charge from V_1 to V_2 can be seen as if current flows through the resistor. It can be seen that the resistance value is determined by the combination of capacitor size and f_{SC}. That is, a combination of different capacitor sizes and switching frequencies can be used to achieve the desired resistance.

The full architecture replaces the R_{DAC} with this switched capacitor is:

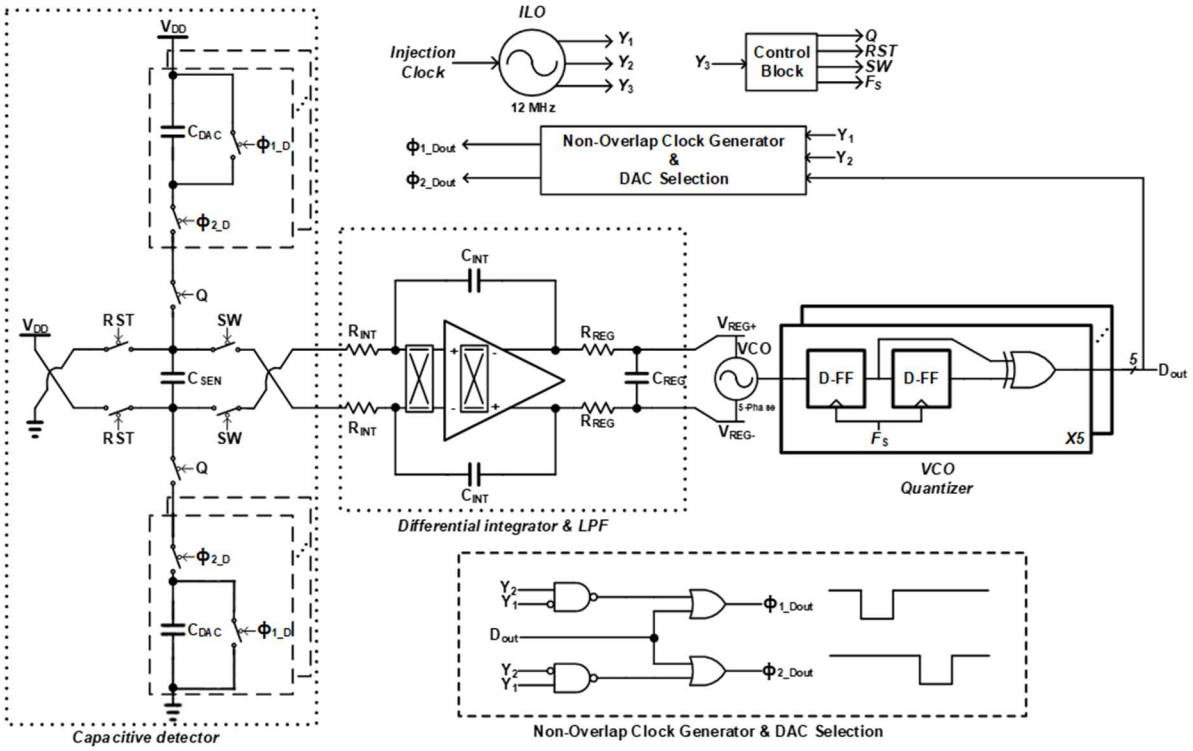


Figure 22 Full architecture of proposed circuit

The basic operation is similar to the circuit using R_{DAC} described above. The change there is the addition of a capacitive detector and a non-overlap clock generator. First of all, the switched capacitor is different from the one described above, but the operation is the same. This is because the amount of charge stored in C_{DAC} is determined by the voltage facing the opposite plate with a constant bias on one plate of the capacitor.

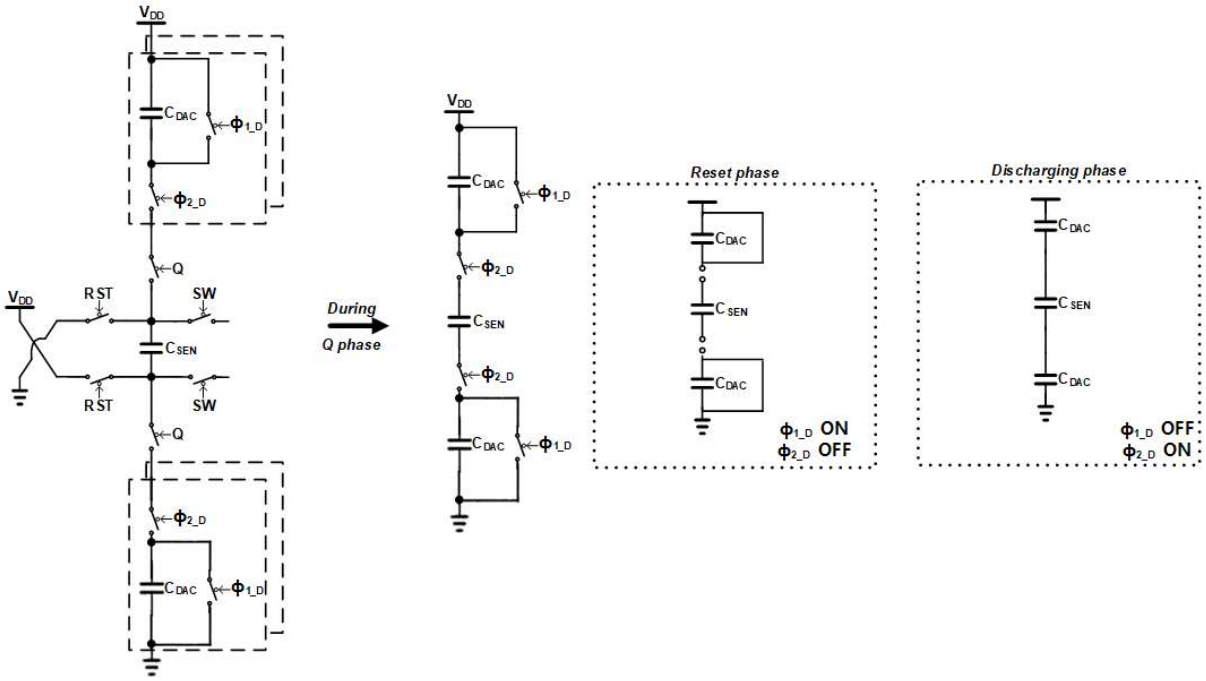


Figure 23 Capacitive detector operation using switched capacitor DAC

Switched capacitor DACs are important for operation in the Q period that discharges the C_{SEN}. Assume that the phase in which the ϕ_1 switch is turned on is the reset phase, and the

phase in which the ϕ_2 switch is turned on is the discharge phase. In the reset phase, the charges of the two C_{DAC}s are zero. The charge in the C_{SEN} then moves to both C_{DAC}s in the discharge phase and the C_{SEN} is discharged. During this process, the voltage of C_{SEN} changes as follows.

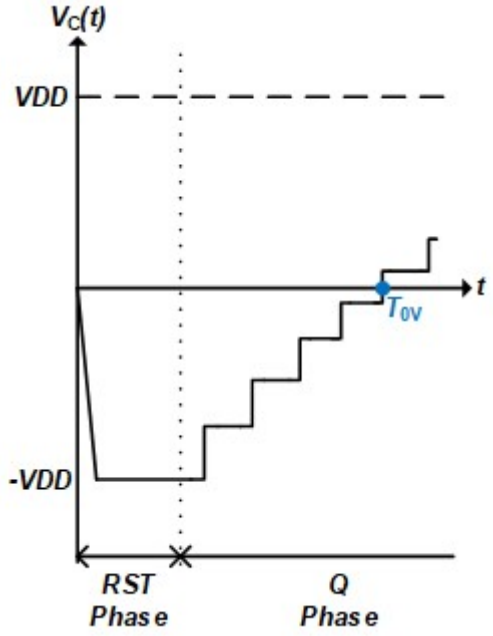


Figure 24 Waveform of capacitive detector

$$V_C(n) = \frac{2C_{SEN}V_C(n-1) + C_{DAC}V_{DD}}{C_{DAC} + 2C_{SEN}} = \frac{2C_{SEN}}{C_{DAC} + 2C_{SEN}} V_C(n-1) + \frac{C_{SEN}V_{DD}}{C_{DAC} + 2C_{SEN}}$$

As the two phases alternate, VC continues to increase and then passes through 0V at T_{0V}. It is not a Continuous operation like when using Resistor DAC, but it basically has a characteristic of T_{0V}, so it is still strong in supply variation.

There are two important considerations for switching capacitor operation. The first is that

basically two switches should not be turned on at the same time. This is because it is a technique that takes advantage of the fact that a constant charge is delivered at both ends of voltage difference and capacitor size. If two switches are turned on at the same time, some of the charge will move directly without passing through C, so it will not return to the desired state. To prevent this, there must be additional clock generator for switch. The second is the switching frequency. As mentioned earlier, RSC is determined by the capacitance of the switched capacitor DAC and the switching frequency. For smooth operation in the process, several switching must occur within the Q period. In other words, since the switching must occur several times within 250 ns set to T_{0V}, the switching frequency must be at least 4 MHz to repeat the two phases once. However, as can be seen from the figure above, the switched capacitor DAC must be switched several times in the Q period to become continuous. To make this high frequency clock, it need to make a clock that generates higher frequency than the clock used in existing Resistor DAC.

3.2 Switched Capacitor Clock Generator

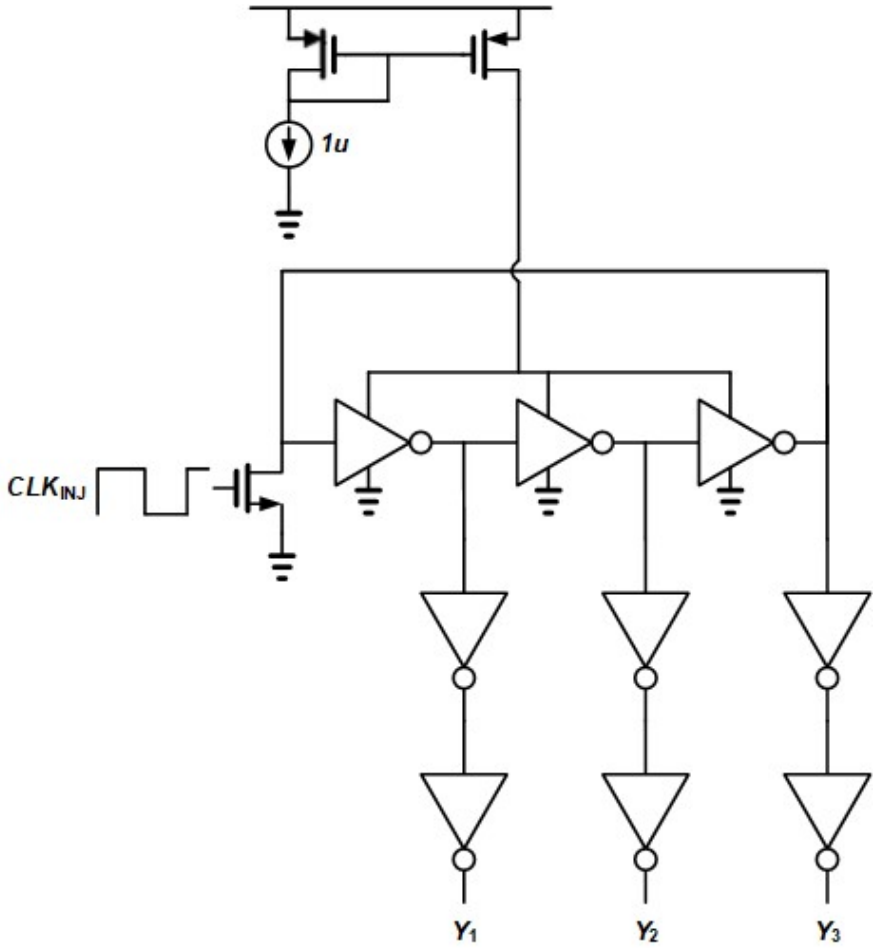


Figure 25 3 phase injection locking current controlled oscillator for switched capacitor

A high frequency injection locking current controlled oscillator was used to create the switching frequency of the switched capacitor. The free running frequency of the ring oscillator is 12 MHz, locking the 12 MHz with injection locking. The output buffer is made from a series connection of inverters with two different supplies as used in the injection locking current controlled oscillator used in the resistor DAC. The ring oscillator uses only 3 phases because it is

no longer necessary to use multi phases to create a control signal. This is explained in section

One of the three phase outputs enters the input of the control block to produce a control signal, and the other two phases are used by a non-overlap clock generator to be used for switched capacitor operation. Non overlap clock generator is composed as follows.

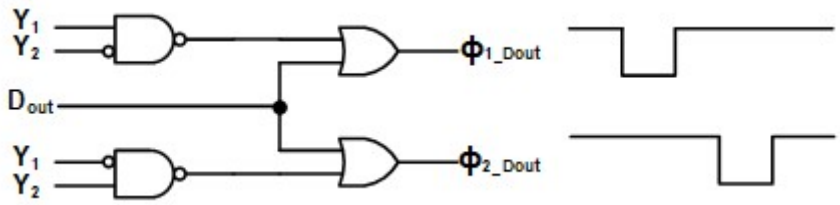


Figure 26 Non-overlap clock generator with DAC selection

Using the phase difference between the two phases, we create two non overlap clocks with a frequency of 12 MHz. The reason DOUT is included is to put two clocks only in the DAC that is turned on by D_{OUT}. Because it is a high frequency clock, it is efficient in terms of power consumption when there is no clock going to DAC when it is not turned on. Use D_{OUT} to perform the operation.

3.3 Control Block

As mentioned in Section 3.2, the control block used in a switched capacitor DAC-based circuit requires only one clock input. If the Resistor DAC-based circuit generates a control signal using multiple phases, this circuit generates a control signal using the frequencies generated by dividing a high frequency clock several times.

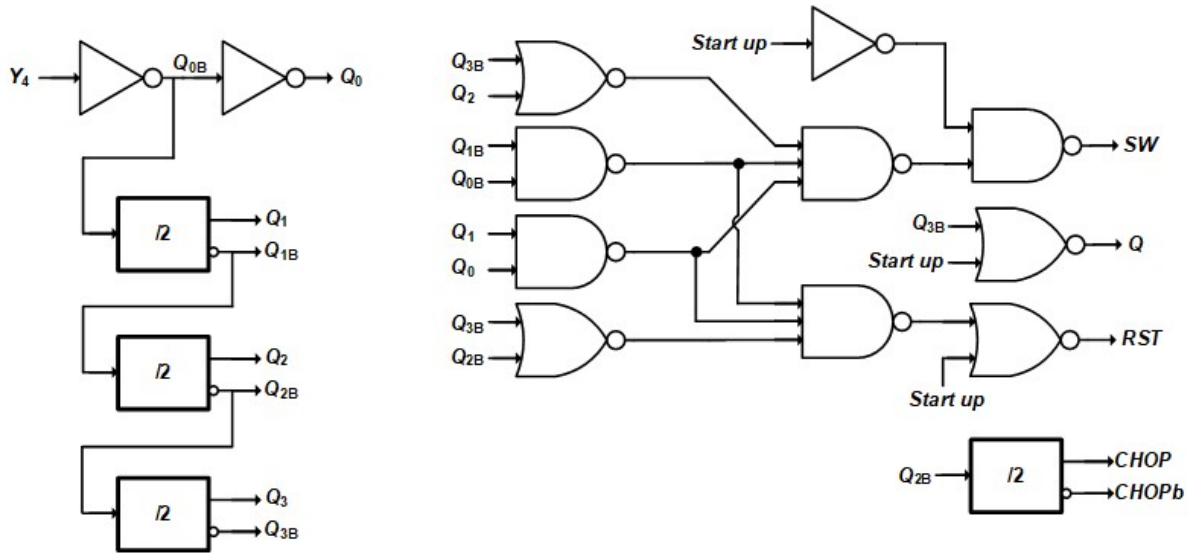


Figure 27 Control block of proposed circuit

As you can see, a clock of 6 MHz, 3 MHz, and 1.5 MHz is generated using a high frequency of 12M and a divider. The frequency of the overall control signals is set to 1.5M. That is, the period of 1.5 MHz is divided into two, four, and eight times frequencies of 1.5 MHz. The output control signals are the same as the control signals used in the Resistor DAC circuit.

3.4 Schematic

Proposed circuit is basically a circuit based on the circuit using Resistor DAC. Since the big frame hasn't changed, only the blocks that make the biggest difference in Schematic are introduced.

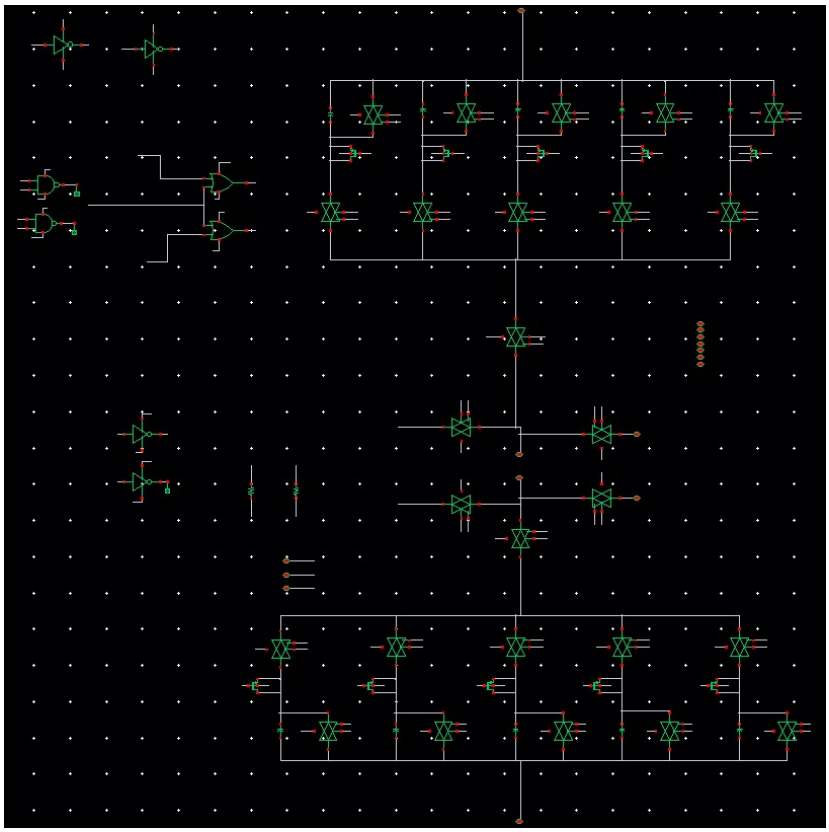


Figure 28 Schematic of capacitive detector using switched capacitor DAC

The figure 28 shows a capacitive detector using a switched capacitor DAC. The capacitor and the switch are located where the R_{DAC} was. The MOSFET between the two switches exists

to hold charge injection with a dummy switch. The top left digital blocks are non-overlap clock generators.

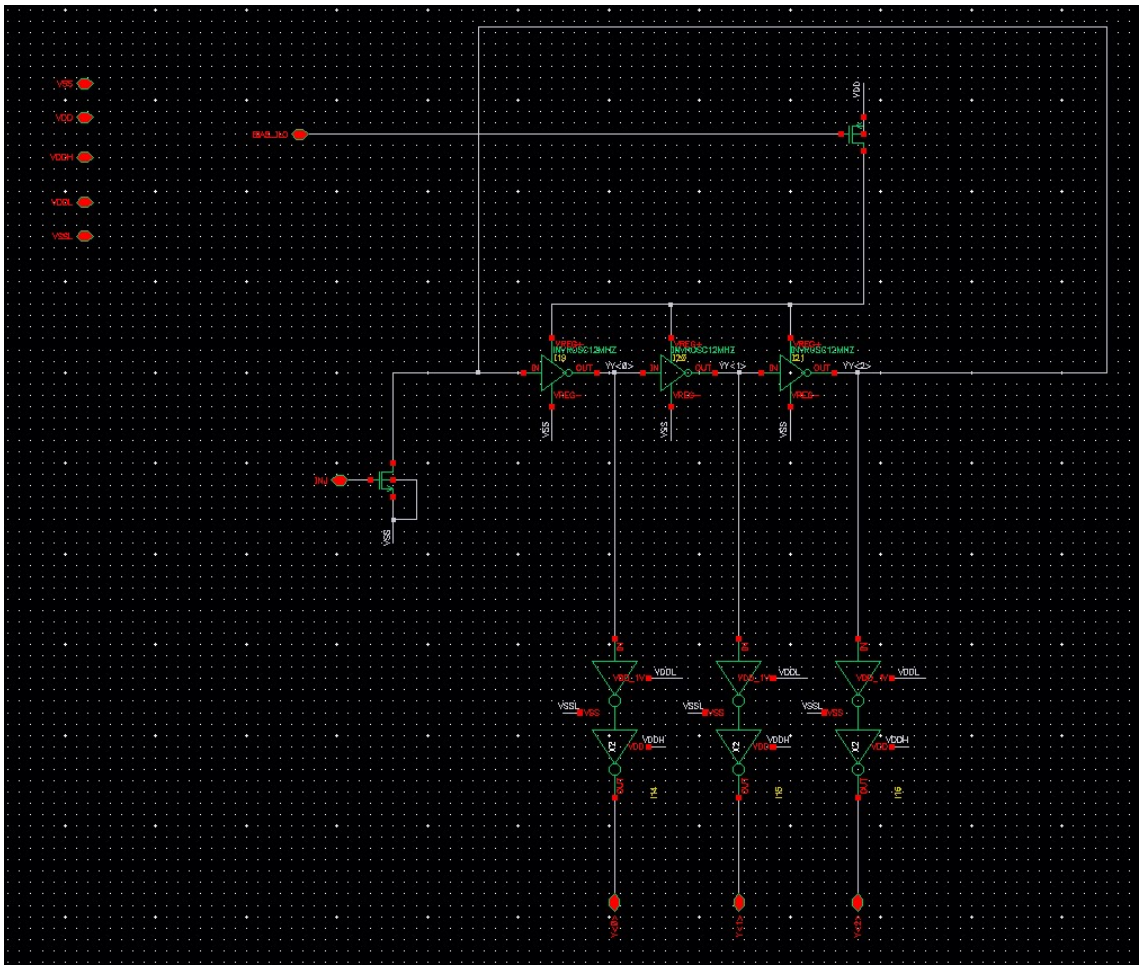


Figure 29 Schematic of 3 phase injection locking current controlled oscillator

The figure 29 is an injection locking current controlled oscillator. Since it has 3 phases, 3 inverters are connected in ring form. At the far left is a MOSFET for injection locking. The output of each phase has a buffer through which it is output.

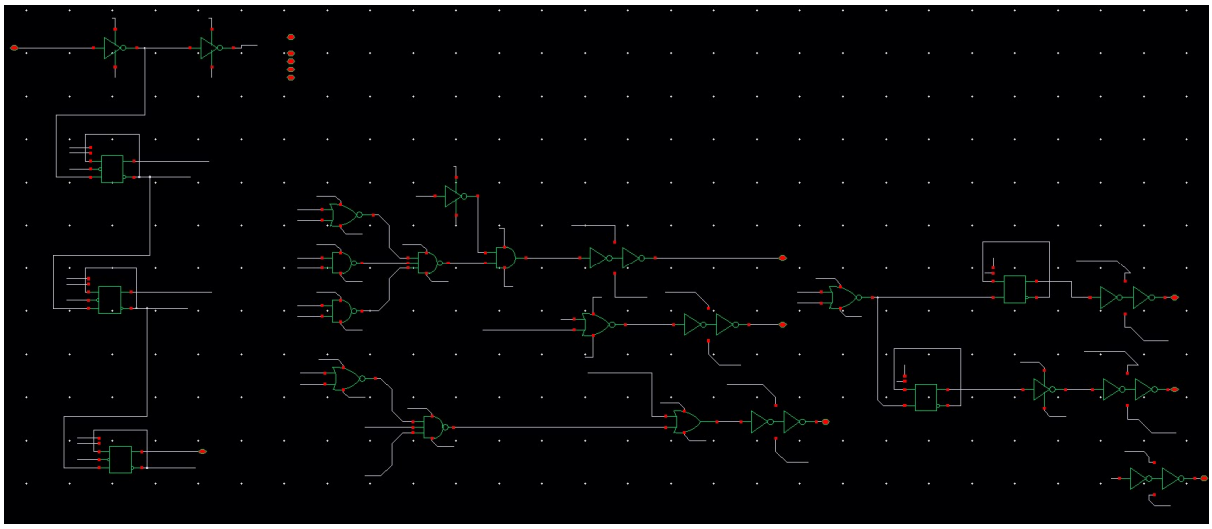


Figure 30 Schematic of control block of proposed circuit

The figure 30 is a schematic of the control block. The three dividers are arranged vertically on the far left. Using the high frequencies created for the switched capacitor operation, the digital blocks produce a control signal using multiple frequencies from this divider.

IV. Simulation and Measurement Result

4.1 Resistor DAC Circuit

4.1.1 Measurement Result

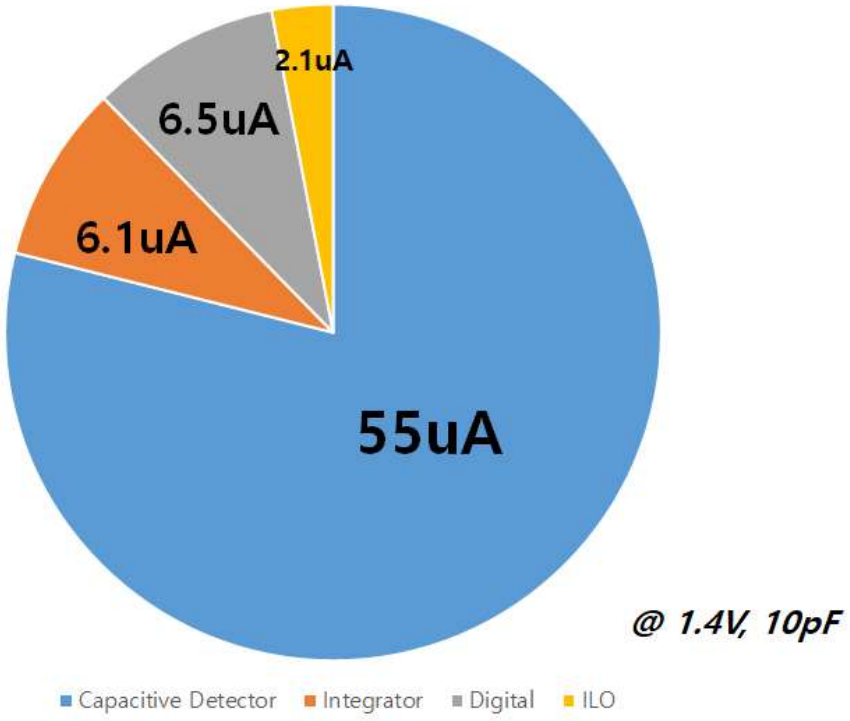
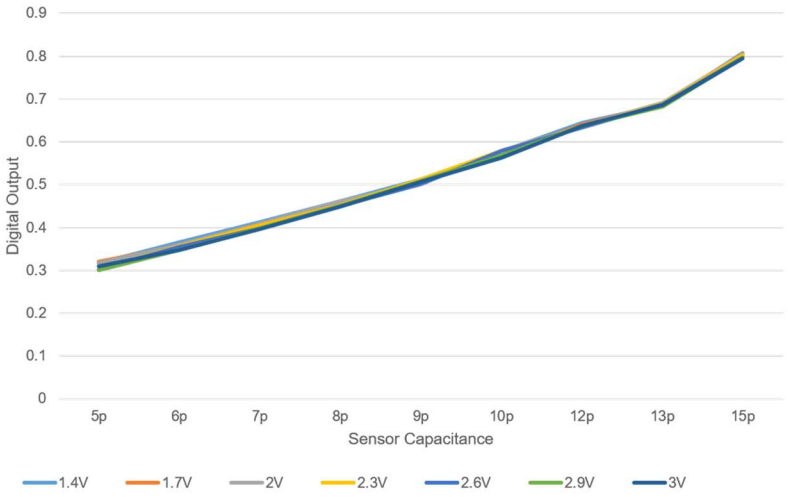


Figure 31 Power consumption distribution of Resistor DAC circuit

This figure 31 is the Power consumption distribution. The total power was 97.6 uW, and the block that consumes the most power is the capacitive detector. This block consumes a lot of power because of RST and Q operation. In each loop, a lot of charge goes through C_{SEN} and power is consumed. Except for the capacitive detector, the power consumption is roughly similar.



Capacitance[pF]	$5pF$	$6pF$	$7pF$	$8pF$	$8pF$	$10pF$	$12pF$	$13pF$	$15pF$
Difference[%]	$\pm 0.47\%$	$\pm 0.59\%$	$\pm 0.56\%$	$\pm 0.533\%$	$\pm 0.23\%$	$\pm 0.51\%$	$\pm 0.33\%$	$\pm 0.4\%$	$\pm 0.49\%$

Figure 32 Measured Dout versus capacitance

The figure 32 is the change of D_{OUT} value according to supply variation. This is the result of changing the supply while measuring several capacitances. You can see that it changes linearly as the capacitance value changes. The rate of change of D_{OUT} according to supply variation also converges to within 0.6%.

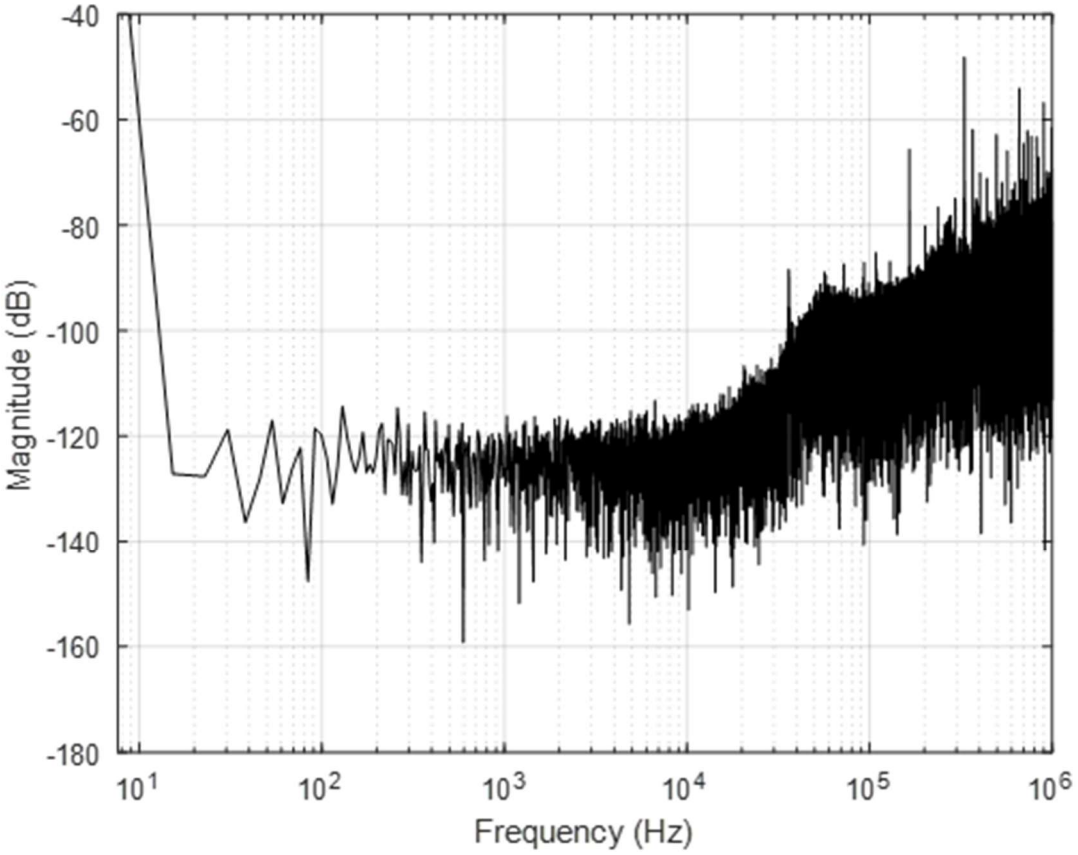


Figure 33 Power spectral density(PSD) of circuit

The figure 33 is a measured PSD. Thermal noise is spread around -120dB and then we can see 40dB/decade noise shaping start from bandwidth of 10 KHz.

4.2 Switched Capacitor DAC Circuit

4.2.1 Simulation Result

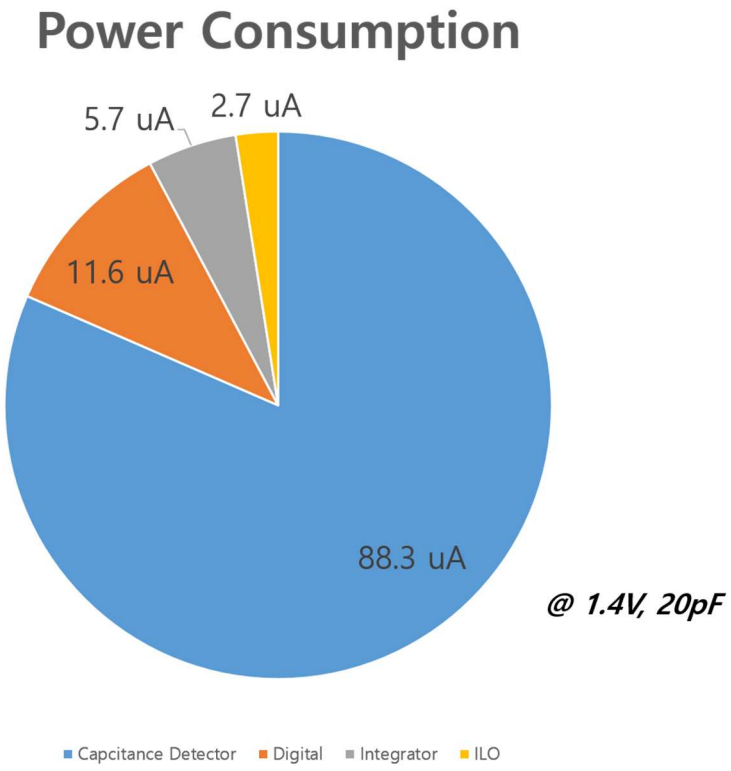


Figure 34 Power Consumption distribution of switched capacitor DAC

Power consumption distribution. The total current is 151.6 uW, and the block that consumes the most power is the same capacitive detector as the resistor DAC circuit. The increase in current draw compared to conventional resistor DAC-based circuits is due to the current used in the switched capacitors. Unlike resistor DACs, switched capacitor DACs must switch at a high rate of 12 MHz. In this process, switching power loss is caused by the switch MOSFET.

This power loss is caused by the MOSFET's channel formation, which is proportional to the MOSFET's size. In the case of the capacitive detector, the size of the capacitive detector has to be large in order to lower the turn-on resistance of the MOSFET, and thus trade-off occurs. In the case of digital blocks, power loss is increased due to the addition of blocks operating at a high frequency of 12 MHz, such as a non-overlap clock generator.

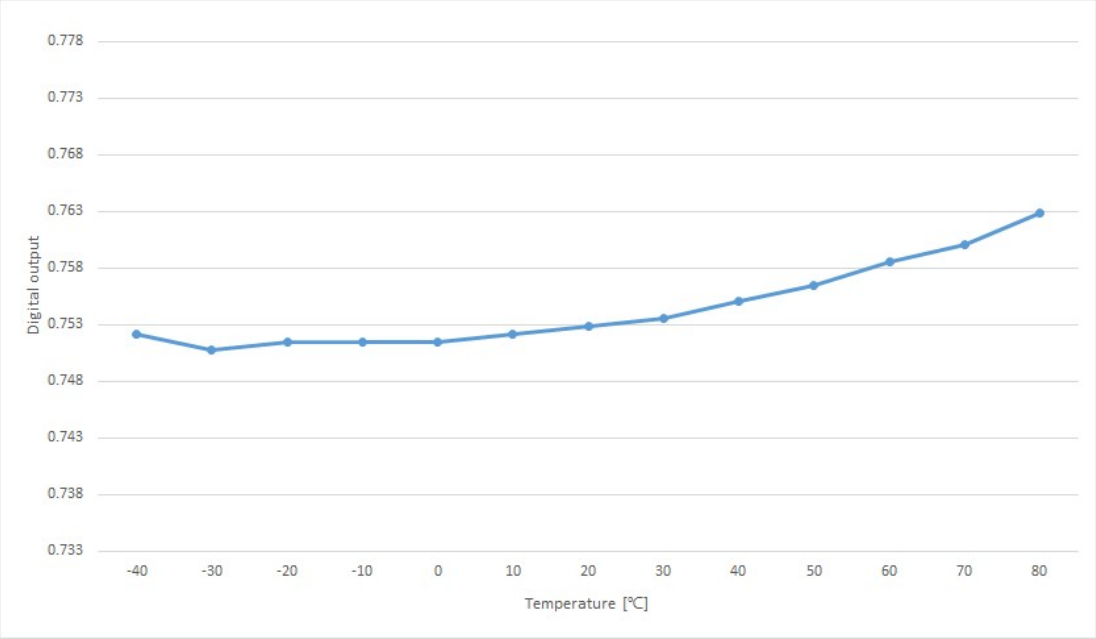


Figure 35 Measured Dout versus temperature

The figure 35 shows the digital output measured by the temperature variation of the circuit. 20pF was used as the capacitance. As you can see from the results, the variation of the digital output from -40℃ to 80℃ is within 1%. Capacitance, unlike resistance, can be obtained be-cause it is not sensitive to temperature change**.**

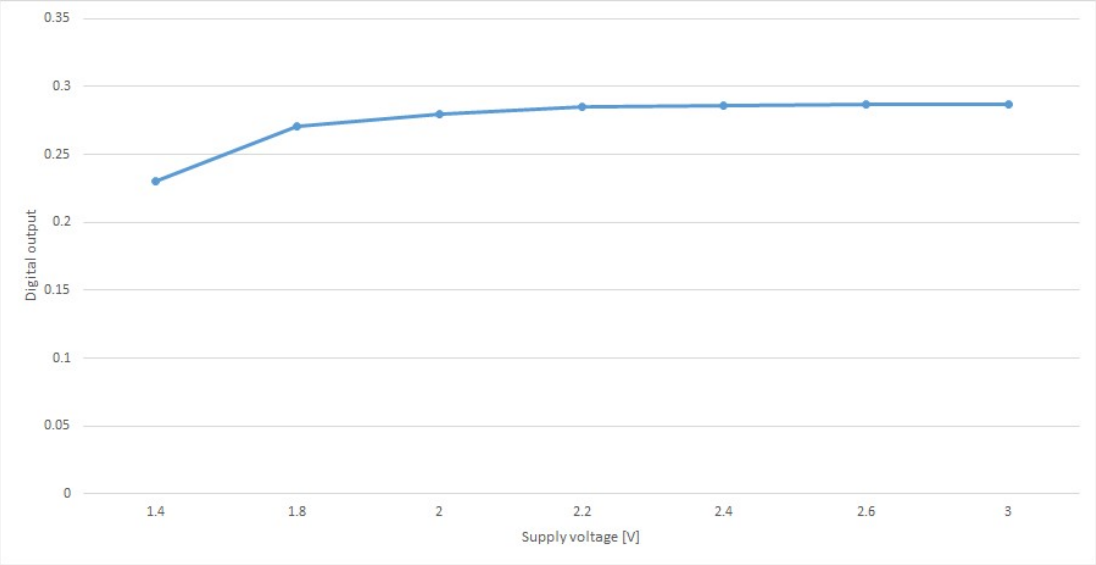


Figure 36 Measured Dout versus supply variation

The figure 36 is the change of digital output according to supply variation. The variation appears to be getting lower and lower. In the capacitive detector, it seems to be caused by the difference in the discharge form of the sensor capacitor. Unlike resistor DAC, in which charge is discharged continuously, switched capacitor DAC discharges charge discretely. For this reason, it is analyzed that the supply variation is sensitive to the change in the low interval. To reduce this variation, it can be improved by increasing the switching frequency of the switched capacitor to make it more like a resistor. However, in the process, power consumption will increase, so appropriate adjustment is necessary.

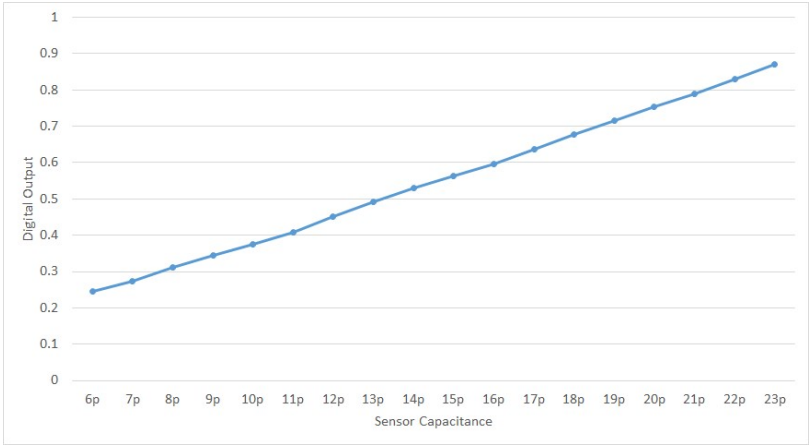


Figure 37 Measured Dout versus sensor capacitance

The figure 37 is the change of digital output according to sensor capacitance. As the sensor capacitance increases, the digital output value increases almost linearly.

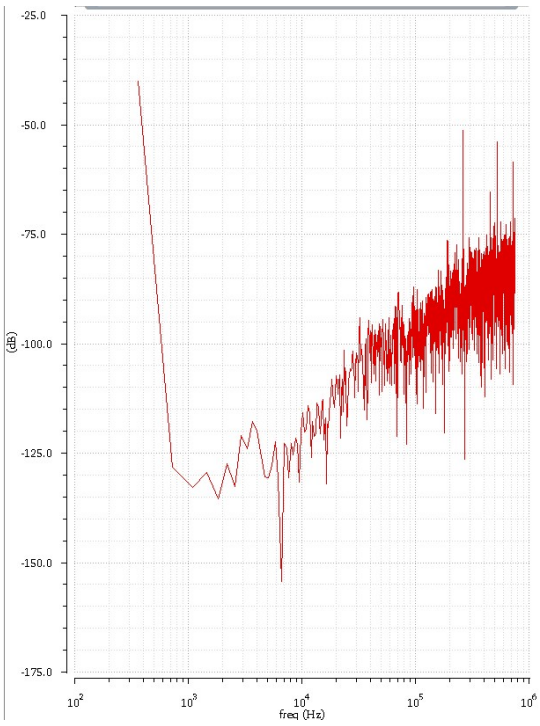


Figure 38 Power Spectral Density of proposed circuit

The figure 38 is the PSD of the proposed circuit. Since it is a 2nd-order sigma delta based

circuit, we can see that it has 40dB of noise shaping. Since the thermal spectral density is not considered, it can be seen that there is no noise in the shape of white noise

Table 1 Comparison with Sate-of-the-Art

	ISSCC 12 (S.Xia)	VLSI 16 (Omran)	VLSI 18 (Arup)	RDAC	SCDAC
Process	350 nm	180 nm	180 nm	180 nm	180 nm
Conversion method	SDM(3^{rd})	SAR	SB-PM	SDM(2^{nd})	SDM(2^{nd})
Supply voltage	3.3	0.8	1	1.3~3.3	1.4~3
Temperature	N/A	N/A	-40~125	27	-40~80
Power	14.9 mW	7.35 uW	140 uW	97.6 uW	153 uW
Measurement time	20 us	16 us	29.3 ms	50 us	250 us
Cap range [pF]	8.4~11.6	0~12.66	0~40000	5~15	6~23
Cap resolution	65 aF	1.1 fF	114 aF	360 aF	853 aF
SNR	84.8 dB	64.2 dB	N/A	78.5 dB	78 dB
FoM [pJ/c-s]	20.9	0.035	4.04	0.708	5.9

Table 1 compares state-of-the-art and proposed circuits. RDAC is a resistor DAC based circuit and SCDAC is a switched capacitor DAC based circuit. The biggest advantage over other circuits is their robustness to supply variation and temperature variation.

V. Conclusion

In this paper, I proposed a temperature- and supply variation robust 2nd-order sigma-delta modulation circuit for capacitive sensing. By using the T_{0V} parameter, which is a capacitor and resistor parameter that is not affected by the supply, it is robust even in supply variation. The above characteristics are shown through the discharge time of the capacitor and resistance. Here, the resistor is replaced with a switched capacitor so that it can have robust characteristics against temperature variation. Unlike resistance, which changes in value due to temperature change, capacitance has a relatively strong characteristic against temperature variation. Combining these characteristics makes it possible to create a circuit with robustness to supply and temperature variation.

In addition, we used a differential integrator rather than a comparator that affected the accuracy of the reference. By taking advantage of the fact that the two inputs of the differential opamp are inherently virtual short, the output voltage of the capacitance detector can be compared to 0V. Differential opamp offset and flicker noise were removed using chopping technique. Corresponding noises raised by high frequency by chopping are removed by RC LPF. VR, the voltage output through this process, acts as a bias of the VCO, and the VCO also moves

away from the effect of supply. The ADC used a VCO based ADC. The noise shaping effect is used to push quantization noise out of the bandwidth.

The robustness to supply and temperature variations pursued by this circuit could be used in many applications. For example, applications that need to be implanted should deliver power wirelessly. In the process, supply variation will greatly affect the circuit. Even under these circumstances, the ability to stably extract capacitance values is sufficient for many applications.

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요 약 문

전원변화 및 온도변화에 강인한 정전용량 측정용 2차 시그마-델타 변조기 설계

본 논문은 전원변화 및 온도변화에도 안정적으로 정전용량을 읽어낼 수 있는 2차 시그마-델타 변조기 회로이다. 커패시터의 방전 시간이 전원의 영향이 아닌 정전용량과 저항 값에만 영향을 받는다는 점을 이용하여 회로를 구성하였다. 또한 저항이 온도변화에 따라서 일정한 값을 유지하기 힘들다는 점을 보완하기위해 switched capacitor 기법을 사용하였다. 커패시터는 저항에 비해 상대적으로 온도변화에도 정전용량을 안정적인 값으로 유지할 수 있다. 이 점을 이용하여 전원변화뿐 만이 아닌 온도변화에도 강인한 특성을 가질 수 있게 된다.

또 전압제어발진기를 활용한 아날로그-디지털 변환기법도 사용되었다. 전압제어발진기에 '전압제어발진기 기반 양자화기'라는 양자화를 할 수 있는 회로를 연결하여 동작이 진행된다. 이 기법을 사용하게 되면 양자화오류의 성분들이 백색잡음처럼 모든 주파수대역에 걸쳐서 골고루 존재하는 것이 아닌, 고주파 쪽을 향해 20dB 의 기울기를 가지며 상승하는 형태로 나타난다. 최종적인 전체 루프의 특성을 확인하면 40dB 의 기울기를 가지며 상승하는 형태를 갖는다. 이 특성을 통하여 동작 대역폭이 아닌 더 고주파 영역으로 양자화 오류 성분들을 밀어낼 수 있다는 장점이 있다. 그 결과, SNR 이 상승하게 되어 최종적으로 정전용량을 읽어낼 수 있는 분해능 성능이 좋아지게 된다.

핵심어 : 정전용량-디지털 변환기, 전압제어발진기 기반 양자화기, 시그마-델타 변조, 전원변화, 온도변화