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A High Efficiency Low Noise RF-to-DC Converter Employing Gm-Boosting Envelope Detector and Offset Canceled Latch Comparator

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Abstract: This work presents a high efficiency RF-to-DC conversion circuit composed of an *LC-CL* balun-based *Gm*-boosting envelope detector, a low noise baseband amplifier, and an offset canceled latch comparator. It was designed to have high sensitivity with low power consumption for wake-up receiver (WuRx) applications. The proposed envelope detector is based on a fully integrated inductively degenerated common-source amplifier with a series gate inductor. The *LC-CL* balun circuit is merged with the core of the envelope detector by sharing the on-chip gate and source inductors. The proposed technique doubles the transconductance of the input transistor of the envelope detector without any extra power consumption because the gate and source voltage on the input transistor operates in a differential mode. This results in a higher RF-to-DC conversion gain. In order to improve the sensitivity of the wake-up radio, the DC offset of the latch comparator circuit is canceled by controlling the body bias voltage of a pair of differential input transistors through a binary-weighted current source cell. In addition, the hysteresis characteristic is implemented in order to avoid unstable operation by the large noise at the compared signal. The hysteresis window is programmable by changing the channel width of the latch transistor. The low noise baseband amplifier amplifies the output signal of the envelope detector and transfers it into the comparator circuit with low noise. For the 2.4 GHz WuRx, the proposed envelope detector with no external matching components shows the simulated conversion gain of about 16.79 V/V when the input power is around the sensitivity of −60 dBm, and this is 1.7 times higher than that of the conventional envelope detector with the same current and load. The proposed RF-to-DC conversion circuit (WuRx) achieves a sensitivity of about −65.4 dBm based on 45% to 55% duty, dissipating a power of 22 µW from a 1.2 V supply voltage.

Keywords: baseband amplifier; comparator; conversion gain; envelope detector; LC-CL balun; offset cancellation; programmable hysteresis; RF-to-DC conversion; wake-up receiver

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1. Introduction

Internet of Things (IoT) is an emerging and fast-growing heterogeneous network that will interconnect a variety of devices (including smartphones, home appliances, sensors, and other network devices), people, data, and processes for a wide range of applications including smart home, building, and cities, agriculture, transportation, and health. Eventually, it allows them to communicate with each other seamlessly. It is expected that the number of connected IoT devices will increase from 27 billion in 2017 to 73 billion in 2025 [1]. One of the most important challenges for a truly innovative IoT solution is extending the lifetime of IoT sensor nodes. Because it is almost impossible to replace the battery periodically in outdoor environments, IoT sensor nodes should be driven by a self-powered energy-harvesting system without a battery by significantly reducing its

power consumption. The self-powered IoT sensor nodes enable its applications to expand into outdoor environments, and this will give us incalculable economic value.

Various wireless technologies have been proposed for low-power IoT applications, such as IEEE802.15.4 (ZigBee), Bluetooth Low Energy (BLE), IEEE802.15.6 (Medical Body-Area Networks, MBAN), and IEEE802.11a/b/g/n (Wi-Fi) [2–4]. Unfortunately, however, one single wireless technology may not be sufficient to cover both short- and long-range IoT applications. For instance, BLE and ZigBee are competing to provide the IoT with an ultra-low-power and low-cost wireless connectivity solution, but their application is limited by the transmission range (within a few hundred meters). Recently, sub-GHz low power wide area network (LPWAN) technologies have been introduced for long range and low-power IoT applications [5,6]. Many LPWAN technologies such as SigFox, long-range wide area network (LoRaWAN), narrowband IoT (NB-IoT), and long-term evolution (LTE)-M have been developed to ensure a long transmission range of more than multiple kilometers with long battery life operation while showing low transmission data rates with small packet data sizes. Consequently, the optimum wireless technology is strongly dependent on IoT applications, and hybrid (short and long range) wireless connectivity solutions optimizing communication range, data rate, and power consumption will be an essential technology in the near future for truly innovative IoT solutions. In addition, because the most power-hungry building block in IoT devices is the wireless communication part, reducing and optimizing the power consumption of the wireless transceiver can make the IoT device intelligent by decreasing the overall power consumption of the complete IoT system and providing opportunities to add many additional functionalities.

It is very important to reduce or eliminate the wasted power in the idle state to decrease the total power consumption of the wireless transceiver. The idle state is when the transceiver is listening to the channel to check for an incoming message [7]. Several techniques such as duty cycling method in [8], asynchronous scheme in [9], and wake-up radio in [10] have been devised to reduce the power in the idle state. Among them, the wake-up radio has been a popular transceiver architecture in recent years for battery-powered IoT applications because of its simple hardware configuration and system application. As shown in Figure 1, the RF to DC converter circuit composed of RF envelope detector (RFED), baseband amplifier, and comparator has been employed as a separate wake-up receiver (WuRx) in order to monitor the communication channel continuously and enable the main radio when it is needed. The most important consideration in implementing a WuRx is low power dissipation while maximizing sensitivity, and as a result, WuRx is typically designed by a simple RFED consisting of Schottky diodes or MOSFETs in the weak inversion region without active filtering or amplification of the input signal [11]. This implies that the sensitivity of WuRx is strongly dependent on the efficiency of the RF to DC conversion and noise performance of RFED. In order to avoid a false wake-up by strong interferers coming from nearby terminals with high transmit power such as mobile phones and WiFi devices, the RFED should have good out-of-band (OOB) rejection characteristic. In addition, it is important to minimize the effect of DC offset of the comparator circuit to avoid sensitivity degradation.

In this paper, a high efficiency RF-to-DC conversion circuit, which is composed of an *LC*-*CL* balun-based *Gm*-boosting RFED, a low noise baseband amplifier, and an offset canceled latch comparator, is proposed for 2.4-GHz WuRx applications. The rest of this paper is organized as follows. In Section 2, we discussed the architecture of the proposed envelope detector. The programmable hysteresis comparator including the proposed DC offset cancellation scheme is analyzed and explained in Section 3. Section 4 discusses the post-layout simulation result and finally, the conclusion is described in Section 5.

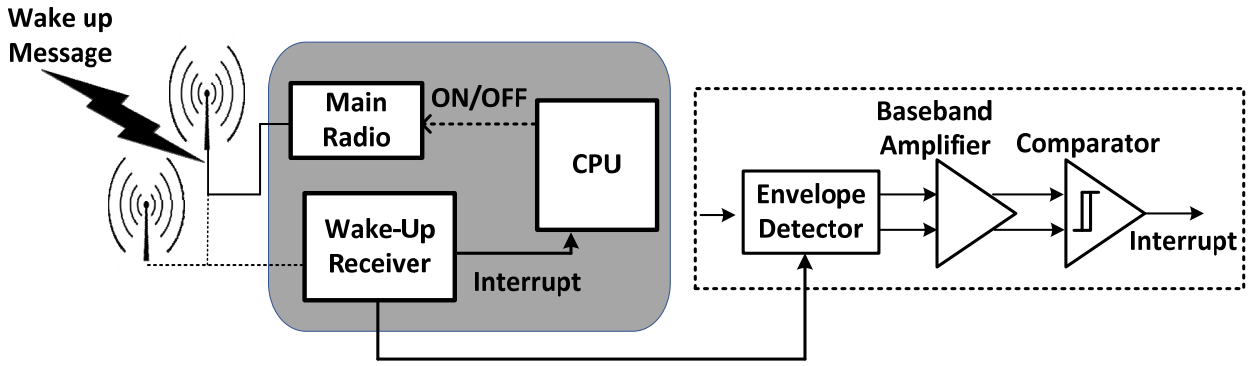


Figure 1. Typical block diagram of a wireless part of IoT sensor node with a separate wake-up receiver.

2. Design of RF Envelope Detector

2.1. Conventional RF Envelope Detector

Generally, the RF-to-DC conversion exploits the non-linearity feature of devices. There are two types of envelope detector which are passive and active topology. The passive one can operate without a bias current, however, it exhibits various disadvantages such as low input impedance and power loss. The MOSFET with a limited threshold voltage is a key device in an active envelope detection circuit which is commonly used in RF demodulation. Figure 2 shows the schematic of the conventional RFED [12]. It has been built based on the inductively degenerated common-source amplifier with current source load. The envelope of the original signal is extracted by down-converting the incident RF signal V_{in} to baseband frequencies by using the exponential transfer function of the input transistor M_1 operating in subthreshold region. The high frequency component is then removed by an RC ($R_1 - C_1$) low-pass filter to achieve a pure baseband envelope signal. The most important specifications of an envelope detector are conversion gain, efficiency, and noise performance. The conversion gain is defined as the ratio of output DC voltage (baseband frequency) and input modulated signal (carrier signal). The saturated drain current of the input MOSFET M_1 biased in the subthreshold region can be expressed as

$$I_D \simeq I_{D0}\left(\frac{W}{L}\right)\exp\left(\frac{V_{GS}}{nV_T}\right), \tag{1}$$

where I_{D0} is a current constant independent of gate-to-source voltage, (W/L) is the aspect ratio of the transistor, n is a process-dependent term related to depletion region characteristics, and V_T is the thermal voltage (=kT/q; 26 mV at room temperature) [13]. When the small sinusoidal wave $V_a cos(w_c t)$ and DC bias voltage V_{bias} are applied to the gate of the input transistor M_1, Equation (1) can be modified based on a Taylor series as

$$\begin{aligned} I_D &\simeq I_{D0}\left(\tfrac{W}{L}\right)\exp\left(\tfrac{V_{bias}+V_a\cos(w_c t)}{nV_T}\right) \simeq I_{B0}\exp\left(\tfrac{V_a\cos(w_c t)}{nV_T}\right) \\ &\simeq I_{B0}[1+(\tfrac{V_a}{2nV_T})^2+\tfrac{V_a}{nV_T}\cos(w_c t)+(\tfrac{V_a}{2nV_T})^2\cos(2w_c t)], \end{aligned} \tag{2}$$

where I_{B0} is the DC drain current of the input transistor M_1. This drain current is converted into the output voltage through a current source with RC ($R_1 - C_1$) load, and the RC low-pass filter attenuates the high frequency carrier component of the output voltage leaving a signal DC component $I_{B0}(V_a/2nV_T)^2$. Because the transconductance (g_m) of the MOSFET biased in the subthreshold region is given by (I_{B0}/nV_T), the output voltage (V_o) and conversion gain (K_v) of the RFED are calculated as

$$V_o \simeq \frac{1}{4}g_m R_{out}\left(\frac{{V_a}^2}{nV_T}\right) \text{ and } K_v \simeq \frac{1}{4}g_m R_{out}\left(\frac{V_a}{nV_T}\right), \tag{3}$$

where R_{out} is the output impedance of the RFED. From (3), the conversion gain, which is the effectiveness of peak detection from carrier frequency to baseband frequency, is directly proportional to g_m, R_{out}, and V_a. The matching network composed of L_2, C_2, and L_3 is adopted to match the input impedance of the RFED to the source impedance. The passive voltage gain by the matching network should be added to (3) for the complete conversion gain of the RFED.

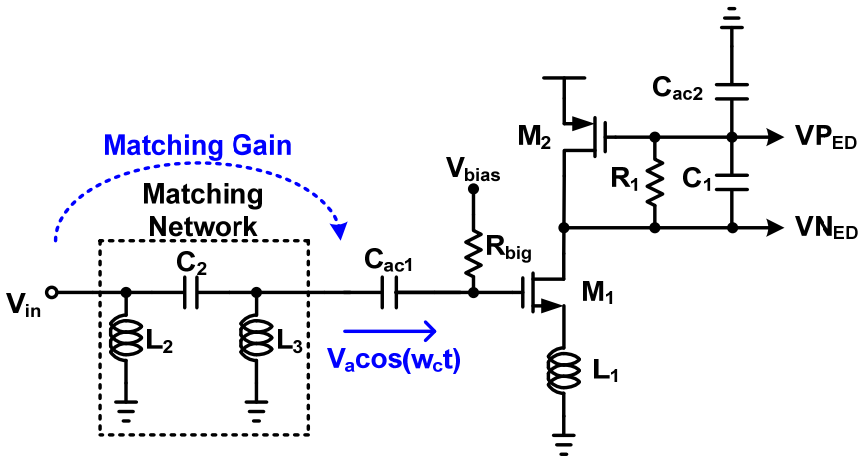


Figure 2. Conventional RF envelope detector.

2.2. Proposed LC-CL Balun-Based Gm-Boosting RF Envelope Detector

Figure 3 shows the schematic of the proposed *LC-CL* balun-based *Gm*-boosting RFED. Like the conventional RFED of Figure 2, this configuration is originated from an inductively degenerated common source amplifier with a current source. The key part of this detector is the *LC-CL* balun playing a role as a voltage doubler that converts the single-ended to differential signal across the gate and source of the input transistor M_1. As a result, the transconductance of input transistor M_1 is doubled because the gate-source voltage increase twice. This directly increases the conversion gain of the RFED from (3) without any extra power consumption. The input matching network composed of a series capacitor C_3 and a shunt inductor L_3 is employed to match the input impedance of the RFED to the source impedance. The C_{ac1} is a DC blocking capacitor for the input signal. Although this technique requires one additional inductor for the implementation of *LC-CL* balun, the number of inductors including the matching network is the same as that of the conventional RFED of Figure 2 because of the simpler input matching network.

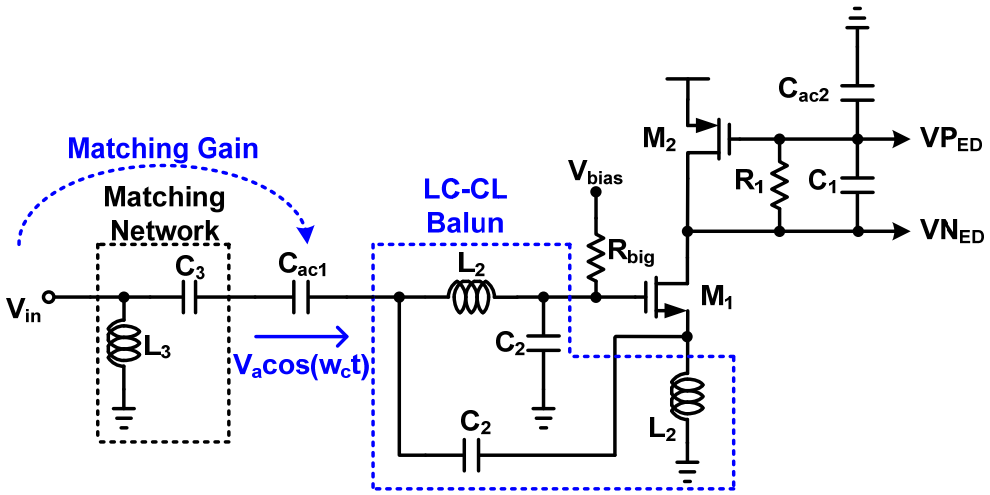


Figure 3. Proposed *LC-CL* balun-based Gm-boosting RF envelope detector.

Figure 4 compares the simulated conversion gain of the conventional RFED (Figure 2) and proposed RFED (Figure 3). Input power is scaled in dB and output voltage is on a logarithmic scale. The summary of device size and component value for both detector circuits is presented in Table 1. Both detectors are designed to consume an identical current of 10 µA from a 1.2 V power supply, and the value of R_1 and C_1 is set to have a cut-off frequency of 50 KHz. In addition, all components excepting C_{ac2} are fully integrated into the single chip for the implementation of highly miniaturized WuRx with low cost. In the simulation, the performance of the RFED is evaluated using an AM signal with a modulation index of 0.75, a modulation rate of 50 KHz, and a carrier frequency of 2.4 GHz. As shown in Figure 4, the proposed RFED shows a conversion gain of 16.79 V/V which is 1.7 times higher than that of the conventional RFED. The output voltage of the proposed RFED is approximately 2.8 mV for an −60 dBm input signal.

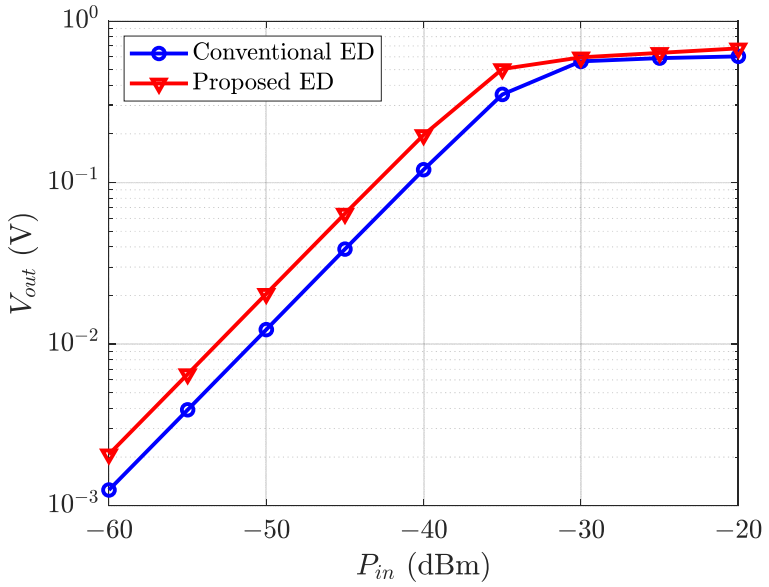


Figure 4. Simulated conversion gain of the conventional and proposed RFED.

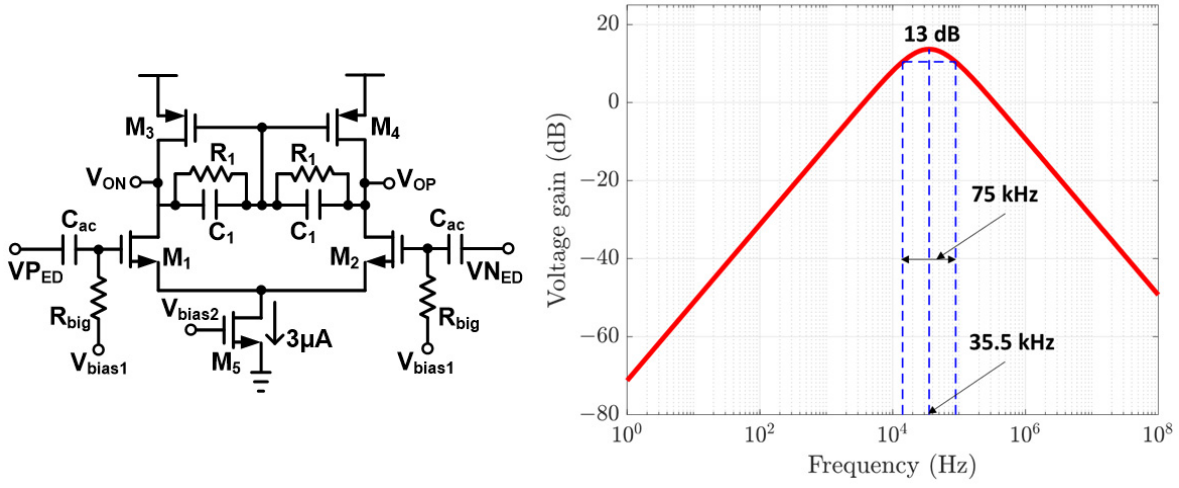
Table 1. Component values of the conventional and proposed RFED.

Type	Component	Value	Component	Value
Conventional RFED	M_1	28 µm/0.24 µm	L_3	6.5 nH
	M_2	90 µm/0.7 µm	C_1	2 pF
	R_1	1.5 MΩ	C_2	0.7 pF
	R_{big}	100 kΩ	C_{ac1}	5 pF
	L_1	6.5 nH	C_{ac2}	1 µF
	L_2	1.3 nH		
Proposed RFED	M_1	28 µm/0.24 µm	C_1	2 pF
	M_2	90 µm/0.7 µm	C_2	0.66 pF
	R_1	1.5 MΩ	C_3	12 pF
	R_{big}	100 kΩ	C_{ac1}	5 pF
	L_2	6.5 nH	C_{ac2}	1 µF
	L_3	1.2 nH		

3. Design of Baseband Amplifier

Figure 5a shows the schematic of the designed fully differential baseband amplifier. It is based on a single-stage operational transconductance amplifier (OTA) biased in the subthreshold region. It amplifies the differential outputs of RFED and reduces the effect of DC offset caused by the next comparator circuit. The RC ($R_1 - C_1$) load provides some OOB rejection characteristic, and the value of R_1 and C_1 is chosen for a bandwidth greater than 50 KHz. For a low power operation, the tail transistor is biased with as low a current

as 3 µA. As shown in the frequency response of Figure 5b, it shows a maximum voltage gain of 13 dB at the center frequency of 35.5 KHz and a 3-dB bandwidth of 75 KHz in the simulation.



(**a**) (**b**)

Figure 5. Schematic and simulation result of designed baseband amplifier: (**a**) schematic and (**b**) frequency response.

4. Design of Comparator

4.1. Conventional Hysteresis Comparator

The hysteresis characteristic is required to avoid unstable operation by the large noise at the compared signal. Figure 6 shows the conventional hysteresis comparator employing internal positive feedback to achieve a hysteresis [14]. The first stage is the PMOS differential pair with diode-connected load transistor M_3 (M_6) and lath transistor M_4 (M_5). Intuitively, the amount of hysteresis is determined by the channel width ratio between the diode-connected load transistor and latch transistor because it is directly related to the amount of feedback by latch transistor. The common source stage M_7 (M_8) amplifies the differential outputs of the first stage, and the differential outputs are converted into the single-ended output through the current mirror M_9 and M_{10}.

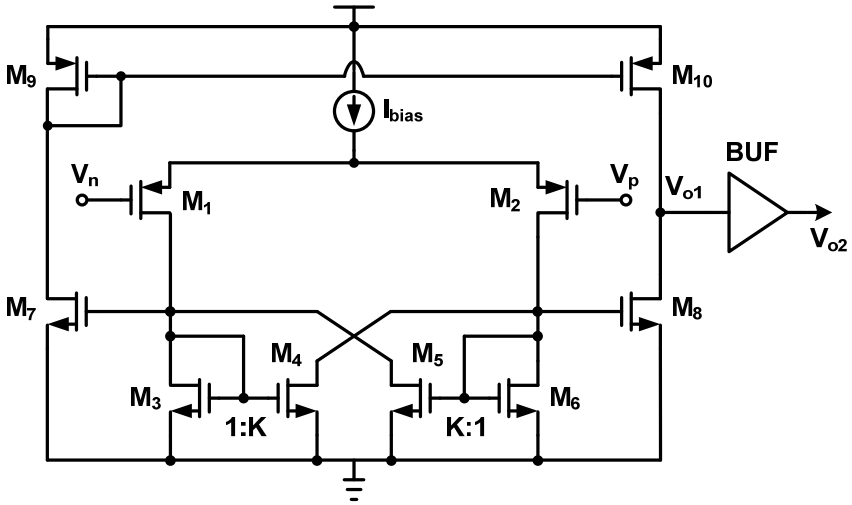


Figure 6. Conventional hysteresis comparator.

When the input signal is higher than the reference voltage by an amount of V_{hys}, the output is at logic high "1". In contrast, the output is at logic low "0" when the input

signal is smaller than the reference voltage by a value of V_{hys}. This relationship can be represented by

$$V_o =' 1' \text{ if } V_p > V_n + V_{hys} \text{ and } V_o =' 0' \text{ if } V_p < V_n - V_{hys}. \quad (4)$$

As a result, it is important to calculate the upper trip point ($+V_{hys}$) and lower trip point ($-V_{hys}$) of the comparator circuit. As the differential voltage heads toward the upper trip point, M_1 turns on. Once it reaches the supply current such that $I_{D5} = K \cdot I_{D6}$, where K is the channel width ratio between M_3 (M_6) and M_4 (M_5), the comparator trips. The process occurs in a similar way when there is a transition from "1" to "0". In summary, the conditions for the upper trip point ($+V_{hys}$) are given by

$$I_{bias} = I_{D1} + I_{D2},\ I_{D2} = I_{D6},\ I_{D3} = I_{D4} = 0, \text{ and } I_{D1} = I_{D5} = KI_{D6}, \quad (5)$$

where I_{bias} is the tail current of the input differential pair. Based on Equation (5), the absolute value of the upper trip point ($+V_{hys}$) and lower trip point ($-V_{hys}$) is derived as

$$|+V_{hys}| = |-V_{hys}| = \frac{\sqrt{K}-1}{\sqrt{K+1}}\sqrt{\frac{2I_{bias}}{\mu_p C_{ox}(W/L)_{1,2}}}, \quad (6)$$

where μ_p is the mobility of input PMOS transistors, C_{ox} is the oxide capacitance, and (W/L) is the ratio between channel width and channel length of input PMOS transistors. The hysteresis window is the difference between these two trip points and can be easily varied by controlling the value of K.

4.2. Proposed Programmable Hysteresis Comparator with Body-Biasing-Based DC Offset Cancellation

Figure 7 shows the proposed programmable hysteresis comparator with body-biassing-based DC offset cancellation. In order to vary the hysteresis window of the conventional hysteresis comparator of Figure 6, the diode-connected load transistor M_3 (M_6) and common-source transistor M_7 (M_8) are constructed with several switched MOSFET branches in parallel, each of which consists of a unit MOSFET in series with a cascode switch. The channel width of unit MOSFET in the switched MOSFET branches is designed to be binary-weighted to vary total channel width linearly adopting the minimum number of branches. The channel length of unit MOSFET in all branches is identical. By digitally turning on or off the cascode switch in each branch, the value of K, which is directly related to the feedback factor by latch transistor, can be changed for the programmable hysteresis characteristic.

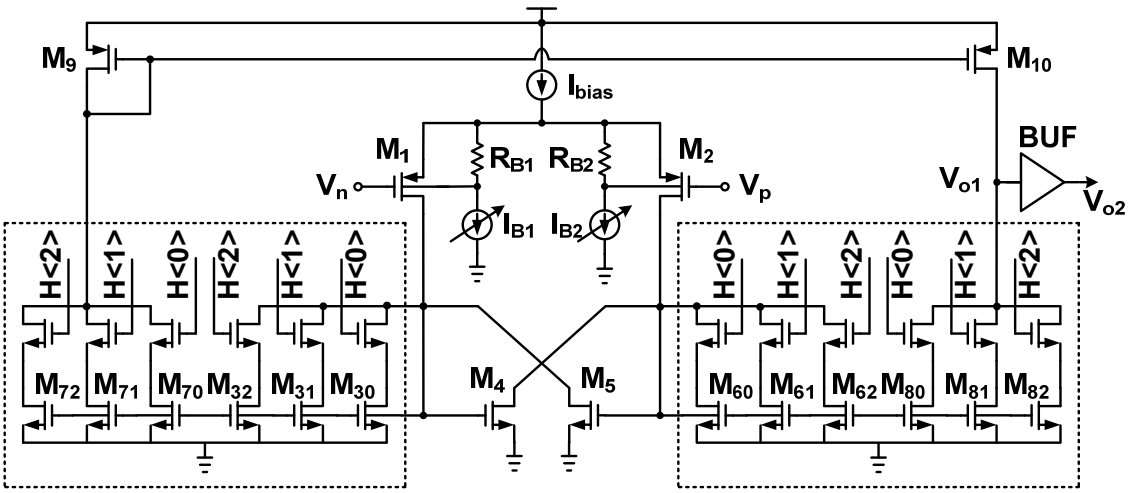


Figure 7. Proposed programmable hysteresis comparator with body-biasing-based DC offset cancellation.

It is highly required to cancel the DC offset caused by the comparator circuit in order to improve the sensitivity of the wake-up radio. Many offset cancellation techniques, which are based on using pre-amplifiers with input/output offset storage (IOS/OOS) in [15], unbalanced output loads in [16], and auxiliary shunt calibrating transistors at input nodes in [17], have been reported recently. However, the simpler offset cancellation method with extremely low power consumption and small occupied area is highly required for WuRx applications. The work of [18] presented an offset cancellation technique based on a body bias control of the transistor. The offset is sampled and digitalized by the flash analog-to-digital converter (ADC), and the voltage signals generated from the reference digital-to-analog converter (DAC) are injected into the body nodes of the input differential pair to cancel the DC offset. One of the main drawbacks of this technique is that the voltage biasing is quite sensitive to process, voltage, and temperature (PVT) variations. Two voltage signals traveling along a pair of long conductor lines can cause an additional DC offset by some mismatches.

As shown in the proposed DC offset cancellation technique of Figure 7, the current biasing is employed to control the body bias voltage of a pair of differential input transistors. The current generated from the adjustable current source is converted into the voltage near the body node of the input transistor, and this voltage is directly injected into the body node. The hardware complexity of the proposed scheme is very simple, and it is more robust over PVT variations than the conventional voltage biasing-based technique of [18]. Assuming the input offset voltage is modeled as a voltage source, V_{OS}, in series with the inverting input node of the comparator and the input voltage V_p and V_n are the same, V_{OS} can be expressed as

$$\begin{aligned} V_{os} &= -V_n - V_{sg1} + V_{sg2} + V_p = -V_{sg1} + V_{sg2} \ (\because V_n = V_p) \\ &\simeq \sqrt{\frac{2I_{D2}}{\mu_p C_{ox}(\frac{W}{L})_2}} - \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(\frac{W}{L})_1}} + (|V_{thp2}| - |V_{thp1}|), \end{aligned} \tag{7}$$

where $|V_{thp1}|$ and $|V_{thp2}|$ are the threshold voltage of input transistors M_1 and M_2. On the other hand, the threshold voltage of PMOS transistor is given by

$$|V_{thp}| \simeq |V_{th0,p}| + |\gamma|(\sqrt{2\phi_f + |V_{sb}|} - \sqrt{2\phi_f}), \tag{8}$$

where $|V_{th0,p}|$ is the threshold voltage at $V_{sb} = 0$, ϕ_f is the Fermi voltage, and γ is the body-effect coefficient [19]. From (7) and (8), the specific body bias voltages of input transistors can make the exact value of $|V_{thp2}| - |V_{thp1}|$ to cancel a given DC offset voltage V_{OS} completely.

The programmable hysteresis and offset cancellation characteristics of the proposed comparator are verified through the simulation. Its current consumption is nearly constant for hysteresis characteristics and approximately 2.4 µA from a 1.2 V supply voltage at the initial state without DC offset cancellation. Figure 8a shows the simulated programmable hysteresis window through a digital code. As the 3-bit digital code H<2:0> decreases from "111" to "001" in the proposed comparator of Figure 7, the hysteresis window becomes wider (2.4 mV~141.6 mV). This is well-matched to the predicted result from Equation (6). Figure 8b presents the simulated output voltage (V_{o2}) of the comparator according to the variation of calibration current (IB_2) when the DC offset voltage V_{OS} ranges from 3 mV to 15 mV with a step size of 2 mV. Both of the calibration current IB_1 and IB_2 are 125 nA at the initial state, and they are designed to vary from 125 nA to 750 nA with a step size of 125 nA through a digital switch control. It can be seen that the proposed comparator cancels the given DC offset voltage V_{OS} through the adjustment of calibration current (IB_2) and the IB_2 to make V_{O2} zero increases when the V_{OS} becomes significant.

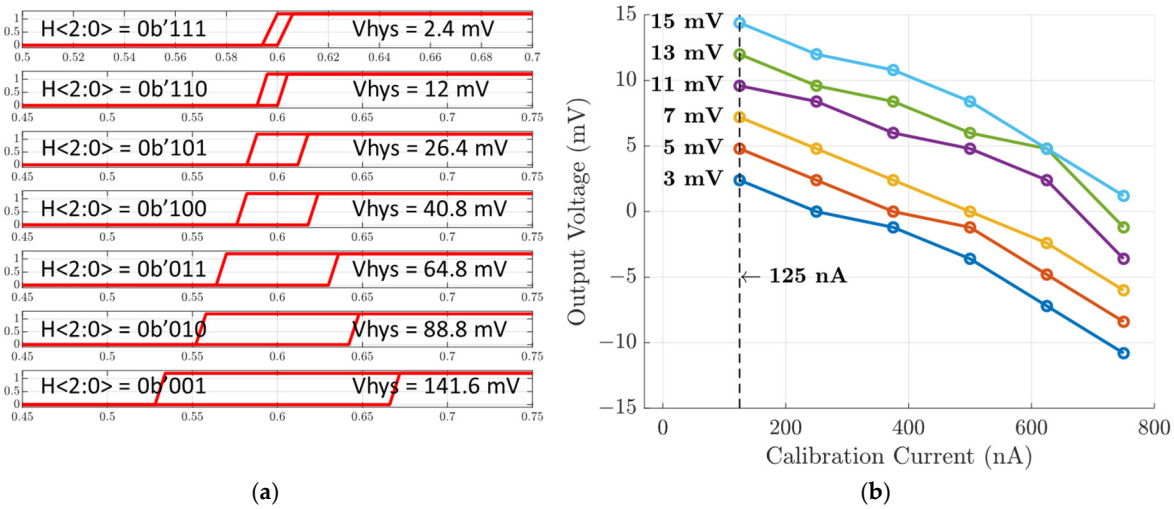


Figure 8. (**a**) Simulated programmable hysteresis window through a digital code; (**b**) simulated output voltage (V_{o2}) of the comparator according to the variation of calibration current (IB_2).

5. Post Layout Simulation Results of Proposed RF-to-DC Conversion Circuit for WuRx

The proposed high efficiency RF-to-DC conversion circuit for 2.4 GHz WuRx applications was designed and simulated in Cadence/Spectre environment using a 65-nm CMOS process. Figure 9 shows the layout photograph of the designed circuit. It occupies an active area of 500 × 840 μm^2. All input matching components including inductors are fully integrated into the single chip for the implementation of highly miniaturized WuRx with low cost. The power consumption of the proposed WuRx is 22 μW at a 1.2 V power supply voltage. In order to enhance the accuracy of the simulation, the commercial process design kit (PDK) having high accuracy modeling was used and the post layout simulation removing some errors caused by parasitic resistance and capacitance was proceeded. Because the input matching network is integrated into the chip and all circuit components excepting a by-pass capacitor C_{ac2} of the proposed RF envelope detector are PDK elements, it is expected that the magnitude of error between the simulation and measurement results is quite small.

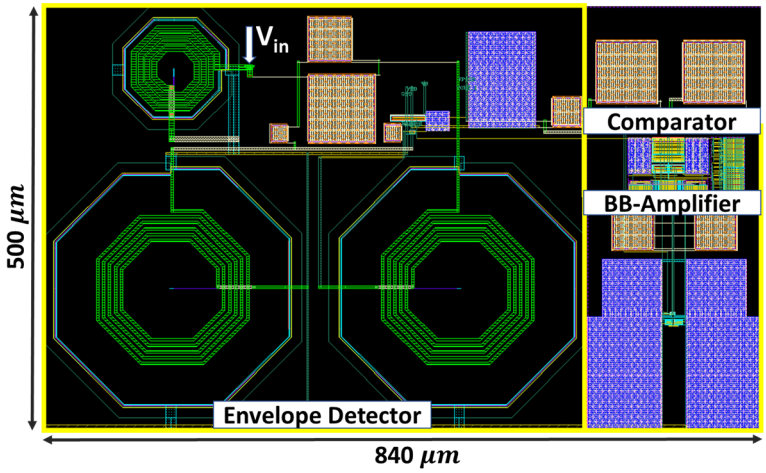


Figure 9. Layout photograph of the designed circuit.

Figure 10 shows the post layout simulated input reflection coefficient (S_{11}) of the proposed WuRx. The S_{11} of the proposed WuRx is less than −15 dB at 2.4 GHz. Figure 11 presents the post layout simulated voltage waveforms of the input node of WuRx and output node of RFED, baseband amplifier, and comparator. In the simulation, an AM

modulated signal with a modulation index of 0.75, a modulation rate of 50 kHz, a carrier frequency of 2.4 GHz, and an input power of −60 dBm is applied to the input of WuRx. When the power of the AM modulated input signal is −60 dBm, the amplitude of the envelope signal at the input node of WuRx is about 0.8 mV_{pp}. The RFED down-converts it into the baseband frequency and generates the envelope signal with the amplitude of 14 mV_{pp}. The baseband amplifier amplifies the output of RFED with about 13 dB voltage gain, and the envelope signal with the amplitude of 67 mV_{pp} is injected into the comparator circuit. The last stage of the comparator generates the final output bit pattern. Based on the requirement of the duty cycle for the common ASK demodulators ranging from 40% to 60%, the proposed WuRx achieves a sensitivity of −64.5 dBm for a square-wave bit pattern with 45%~55% duty cycle in the post layout simulation.

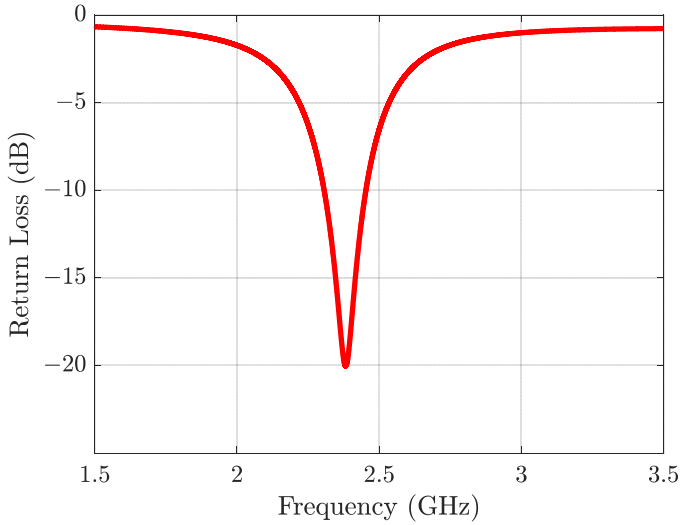


Figure 10. Post layout simulated input reflection coefficient (S_{11}) of the proposed WuRx.

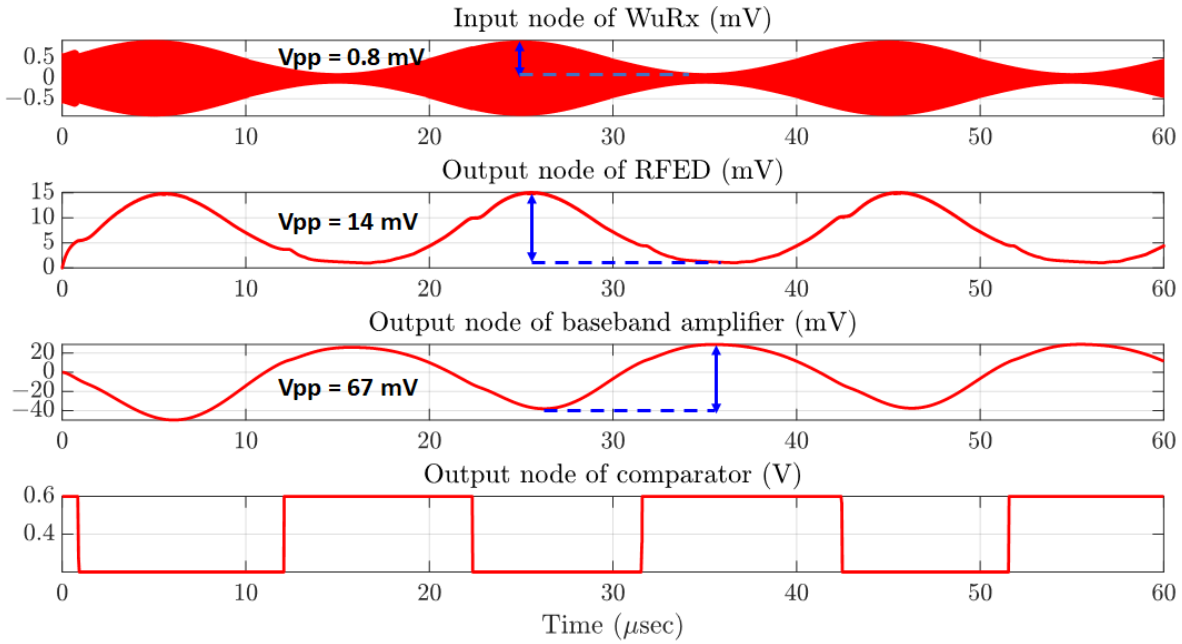


Figure 11. Post layout simulated voltage waveforms of input node of WuRx and output node of RFED, baseband amplifier, and comparator.

In Table 2, the post layout simulation results of the proposed WuRx are summarized and compared to the traditional 2.4 GHz WuRx circuits. One reference work of [20] report-

ing the simulation results is added in the comparison table. This reference is a touchstone that evaluates the performance of the proposed work because it is designed using the same process technology. Despite of adopting the fully integrated on-chip passive elements for the input matching network, it shows better sensitivity performance while consuming a similar current consumption due to the *LC*-*CL* balun-based *Gm*-boosting technique of RFED and body-biasing-based DC offset cancellation technique of programmable hysteresis comparator. In addition, the proposed WuRx adopting a single-ended RFED can reduce the cost and PCB size by eliminating an external transformer compared to the traditional WuRx circuits with a differential RFED.

Table 2. Performance summary and comparison with the traditional 2.4 GHz WuRx circuits.

Parameters	[1] [12]	[2] [20]	[1] [21]	[1] [22]	[3] This Work
Carrier Frequency (GHz)	2.4	2.4	2.4	2.4	2.4
Modulation Rate (kHz)	100	2000	100	2.5	50
Sensitivity (dBm)	−65	−60	−50	−61.5	−65.4
Off-chip Matching Components (?)	Yes	No	Yes	[4] No	No
Differential or Single-ended	Differential	Single-ended	Differential	Single-ended	Single-ended
Power Consumption (μW)	10	22	4.5	0.365	22
Supply Voltage (V)	0.5	1	0.8	0.8	1.2
CMOS Technology	180 nm	65 nm	180 nm	65 nm	65 nm

[1] Measurement results, [2] simulation results, [3] post layout simulation results, [4] rectifier-antenna co-design.

6. Conclusions

The high efficiency RF-to-DC conversion circuit composed of an *LC*-*CL* balun-based *Gm*-boosting RFED, a low noise baseband amplifier, and an offset canceled latch comparator is implemented using a 65-nm CMOS process technology for low power WuRx applications. It provides a new way to increase the conversion gain of RFED and improve the sensitivity by doubling the transconductance of the input transistor without additional power consumption. The programmable hysteresis makes it flexible for the comparator to cover different noise conditions. The offset cancellation scheme, which is implemented without complex circuitry, helps to mitigate the offset due to mismatch error. Taking advantage of technology scaling, the implemented system has become a significant potential solution for many WuRx and wireless communication systems.

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