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Analysis of performance of SiC bipolar semiconductor devices for grid-level converters

Analysis of Performance of SiC Bipolar Semiconductor Devices for Grid-level Converters

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A dissertation submitted to the University of Bristol in accordance with the requirements for award of the degree of *Doctor of Philosophy* in the Faculty of Engineering.

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Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Parts of this thesis are published by the author in peer-reviewed research papers listed. A work done in collaboration with, or with the assistance of others is indicated as such. Any views expressed in the dissertation are those of the author.

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"I dedicate this work
to my beloved parents
and supporting family."

Publications List

Journal Papers:

1. **C. Shen**, S. Jahdi, J. Yang, O. Alatise, J. Ortiz-Gonzalez, R. Wu and P. Mellor

   'Impact of Carriers Injection Level on Transients of Discrete and Paralleled Silicon and 4H-SiC NPN BJTs'

   IEEE Open Journal *of the Industrial Electronics Society*, vol. 3, pp. 65, 80, January 2022.

2. **C. Shen**, R. Yu, S. Jahdi, P. Mellor and S. P. Munagala and A. Hopkins and N. Simpson and J. Ortiz-Gonzalez and O. Alatise

   'FEM-based analysis of avalanche ruggedness of high voltage SiC Merged-PiN-Schottky and Junction-Barrier-Schottky diodes'

   Microelectronics Reliability, vol. 138, pp. 114686, September 2022.

3. **C. Shen**, S. Jahdi, P. Mellor and S. P. Munagala and N. Simpson and J. Ortiz-Gonzalez and O. Alatise

   'Electrothermal Power Cycling of 15 kV SiC PiN Diodes'

   Microelectronics Reliability (Submitted - Under Review).

Conference Papers:

4. **C. Shen**, S. Jahdi, P. Mellor, X. Yuan, O. Alatise and J. Ortiz-Gonzalez

   'Analysis of Dynamic Transients of High Voltage Silicon and 4H-SiC NPN BJTs'

   Presented at the **PCIM 2021** *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-8, May 2021.

5. **C. Shen**, S. Jahdi, P. Mellor, J. Yang and E. Bashar and O. Alatise and J. Ortiz-Gonzalez

   'Analysis of on-state static and dynamic transients of high voltage 4H-SiC Merged-PiN-Schottky diode'

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6. **C. Shen**, S. Jahdi, P. Mellor, J. Yang and E. Bashar and J. Ortiz-Gonzalez and O. Alatise

   'Investigation of the Static Performance and Avalanche Reliability of High Voltage 4H-SiC Merged-PiN-Schottky Diodes'

   Presented at the **EPE 2022** *24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, pp. 1-9, Hanover, Germany, 5-9 September 2022.

7. **C. Shen**, S. Jahdi and J. Yang and O. Alatise and J. Ortiz-Gonzalez and P. Mellor

   'Electrothermal Ruggedness of High Voltage SiC Merged-PiN-Schottky Diodes Under Inductive Avalanche & Surge Current Stress'

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Abstract

Recent commercialization of SiC bipolar devices, including SiC BJT, SiC MPS diode and SiC PiN diodes have enabled potential candidates to replace their SiC unipolar counterparts. However, the prospects of 4H-SiC power bipolar devices still need further investigation. This thesis compares the static and dynamic performance and reliability for the commercial SiC bipolar devices including SiC BJT, SiC MPS diode and SiC PiN diode and their similarly rated Silicon counterparts mainly by means of experimental measurements.

Through comprehensive double-pulse measurements, the turn-on and turn-off transition in Silicon BJT is seen to be much slower than that of the SiC BJT while the transient time will increase with temperature and decreases with collector currents. The common-emitter current gain (β) of SiC BJT is also found to be much higher than its Silicon counterpart. Significant turn-off delay is observed in single Si BJT which becomes worse when in parallel connection as it aggravates the current mismatch across the two devices, while this delay is almost non-existent in SiC devices. The current collapse seen in single SiC BJT is mitigated by parallel connection. These are dependant on temperature and base resistance, especially in the case of Silicon BJT.

The static performance of power Silicon and SiC BJT has also been evaluated. It has been found that the higher base-emitter junction voltage of SiC BJTs enables quasi-saturation mode of operation with low on-resistance, which is also the case for Silicon BJTs only at high base currents. In terms of DC gain measured under steady state operation, the observed negative temperature coefficient (NTC) of β in SiC BJTs and the positive coefficient (PTC) in Silicon BJTs can make the β of SiC BJT lower than that in Silicon at high temperatures. It has been found that parallel connection promotes both the on-state conductivity and current gain in Silicon BJTs and conductivity in SiC BJTs.

The characterization of power diodes reveals that the superior switching performance of the SiC MPS & JBS diode when compared with the Si PiN diode is due to the absence of the stored charge. This also leads to the larger on-state voltage in both SiC diodes and becomes worse at high currents under high temperatures. Through comprehensive Unclamped Inductive Switching (UIS) measurements, it is seen that the avalanche ruggedness of SiC MPS & JBS diodes outperform that of the closely rated Silicon PiN diode taking advantage of the wide-bandgap properties of SiC. Higher critical avalanche energy and thus better avalanche ruggedness can also be observed in SiC JBS diode compared with the SiC MPS diode. SiC MPS diodes can compete with Si PiN diodes in terms of the surge current limits, while the SiC JBS diode failed under a lower electrothermal stress. This is observed by the dramatic increase in its reverse leakage current at lower voltages.

The 15 kV SiC PiN diodes feature smaller device dimensions, less reverse recovery charge and less on-resistance when compared to the 15 kV Silicon PiN diodes. Nevertheless, when evaluating its long-term reliability by using the aggravated power cycling configuration, the high junction temperature together with the dislocation defects in the SiC PiN diode accelerate its degradation. Such degradations are not observed in Silicon PiN diodes for the same junction temperature and high-temperature stress periods.

List of Abbreviations and Symbols

AC	Alternating Current
BJT	Bipolar Junction Transistor
BPD	Basal Plane Dislocation
CE	Common-Emitter
CSC	Current Source Converter
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DUT	Devices Under Test
EMF	Electromagnetic Force
FB	Full Bridge
HB	Half Bridge
HLI	High-level Injection
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
JBS	Junction barrier Schottky
LCC	Line Commutated Converter
MMC	Modular Multilevel Converters
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPS	Merge-PiN-Schottky
PCB	Printed Circuit Board
PFC	Power Factor Correction
REDG	Recombination Enhanced Dislocation Glide
SBD	Schottky Barrier Diode
SCC	Self-Commutated Converter
SM	Switching Modules
SMU	Source Measurement Unit
SSF	Shockley Stacking Fault
TED	Threading Edge Dislocation
UIS	Unclamped Inductive Switching

VFD	Variable Frequency Drive
VSC	Voltage Source Converter
WBG	Wide Bang-gap

GaN	Gallium Nitride
Si	Silicon
SiC	Silicon Carbide

A	effective Richardson's constant (A/cm^2K^2)
C_{bank}	Bank Capacitance (F)
C_{DC}	DC-link Capacitance (F)
D_{nB}	Diffusion Constant of Electrons in Base Region (m^2/s)
D_n	Diffusion Constant of Electrons (m^2/s)
D_p	Diffusion Constant of Holes (m^2/s)
E_{ava}	Avalanche Energy (J)
E_G	Bandgap energy (eV)
E_{Surge}	Surge Current Energy (J)
I_F	Forward Current (A)
$I_{R(BE)}$	Base-Emitter Leakage Current (A)
I_{RP}	Peak reverse Current during reverse recovery (A/cm^2)
J_{BR}	Reverse Base Current Density (A/cm^2)
J_B	Base Current Density (A/cm^2)
J_C	Collector Current Density (A/cm^2)
J_F	Forward Current Density (A/cm^2)
J_{RP}	Peak reverse Current Density during reverse recovery (A/cm^2)
J_R	Reverse Current Density (A/cm^2)
J_W	Webster Current Density (A/cm^2)
k	Boltzmann Constant (J/K)
L_{Load}	Load Inductance (mH)
L_n	Diffusion Length of Electrons (m)
L_p	Diffusion Length of Holes (m)
L_{Stray}	Stray Parasitic Inductance (H)
n_{0B}	Minority Carrier Concentration in Base Region (cm^{-3})
N_A^-	Density of Ionized Acceptors (cm^{-3})
N_{base}, N_B	Doping Concentration of Base Region (cm^{-3})
n_{base}, n_B	Electron Concentration in Base Region (cm^{-3})
$n_B(0)$	Electron Concentration in Base Closest to Base-Emitter Junction (cm^{-3})
N_{drift}, N_D	Doping Concentration of Drift Region (cm^{-3})
N_D^+	Density of Ionized Donors (cm^{-3})

n_i	Intrinsic carrier concentration (cm^{-3})
q	Electrical Charge (C)
Q_F	Stored Charge in Drift Region (C)
Q_{SC}	Stored Charge in Drift Region (C)
R_{base},R_B	Base Resistance (Ω)
R_{drift}	Drift Region Resistance (Ω)
R_{gate},R_G	Gate Resistance (Ω)
R_{on}	Collector-Emitter (Drain-Source) On-state Resistance (Ω)
t_{ava}	Avalanche Period (s)
T_j	Device Junction Temperature (C)
t_{Q1}	Length of Charging Pulse (s)
t_{Surge}	Surge Current Period (s)
$t_{transit}$	Base Transit Time (s)
V_{AVA}	Induced Drain-Source Avalanche Voltage (V)
V_{BD}	Breakdown Voltage (V)
V_{bi}	Junction Built-in Voltage (V)
V_B	Base-Emitter Voltage (V)
V_{CE}	Collector-Emitter Voltage (V)
V_{DC}	DC-link Voltage (V)
V_{drift}	Voltage Drop on Drift Region (V)
$v_{sat(n)}$	Electron saturation velocity ($10^7\times$ cm/s)
$v_{sat(p)}$	Holes saturation velocity ($10^7\times$cm/s)
V_{th-BE}	Threshold Voltage of Base-Emitter Junction (V)
W_B	Width of Base Region (m)
W_D	Width of Drift Region (m)
W_{NM}	Width of Conductivity-Modulated Region in Drift Region (m)
n_{ava}	Density of Electrons Generated by Avalanche (cm^{-3})
p_{ava}	Density of Holes Generated by Avalanche (cm^{-3})
p_B	Effective Hole Concentration in Base Region (cm^{-3})
$p_{NS(0)}$	Hole Concentration at Base-Collector Junction (cm^{-3})

β	Common-Emitter Current Gain ($-$)
λ	Thermal Conductivity (W/cm·K)
$\mathscr{E}_C$	Critical Electric Field (MV/cm)
μ_n	Electron Mobility (cm^2/V·s)
μ_p	Hole Mobility (cm^2/V·s)
Φ_B	Schottky Barrier Height (eV)
τ_A	Auger Lifetime (s)
τ_n	Electron Lifetime (s)
τ_p	Hole Lifetime (s)

τ_{Rad}	Radiative Lifetime (s)
τ_{SRH}	Shockley-Read-Hall Lifetime (s)
ε_r	Relative Dielectric Constant $(-)$
ε_s	Semiconductor Permittivity (F/m)

Chapter

1 Introduction

1.1 Background and Motivation

Power semiconductor devices play a determining role in the efficiency and reliability of power electronics applications such as High Voltage Direct Current (HVDC) transmission systems. Silicon Carbide (SiC) based power semiconductor devices have a bright future to replace traditional Silicon (Si) devices due to the much higher critical electric field and higher thermal conductivity. This in turn increases the blocking voltage for applications in converters that satisfy the increasing demand of electricity.

SiC power semiconductor devices can be divided as Unipolar and Bipolar devices. Unipolar devices such as Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) can block high reverse voltage but incur high on-state resistance due to the thick voltage-blocking drift region. Bipolar devices such as Bipolar Junction Transistor (BJT) and Merge-PiN-Schottky (MPS) diode can facilitate both high voltage blocking and low on-resistance because the onset of conductivity modulation effect [1,2] injects minority carriers into the drift region, but undergo severe reverse recovery to remove the stored charge

and thus larger power dissipation during turn-off when compared to unipolar counterparts.

For power applications lower than 1700 V, SiC BJT can compete with SiC MOSFET because of the absence of defective gate oxide [3–5] as well as its close static and dynamic power dissipation performance at various temperatures [6, 7]. This even makes it a potential candidate to replace Silicon Insulated Gate Bipolar Transistor (IGBT) for Hybrid electric vehicle applications [8]. SiC MPS diode is expected to outperform SiC pure Schottky diode owing to the lower reverse leakage current and the conductivity modulation effect provided by the wide P^+ region [1, 9]. In power applications with voltages above 10 kV the SiC PiN diode is the key, as it facilitates a lower on-state resistance compared to Schottky diodes thanks to its conductivity modulation.

In addition to these performance metrics, the reliability of power semiconductor devices and lifetime prediction has been a major topic of research in the last few decades [10, 11]. The main challenges of power bipolar devices include carrier lifetime in conductivity modulation and reverse recovery, bipolar degradation and avalanche ruggedness [12]. The superiority of electrothermal robustness for SiC bipolar devices compared to their Silicon counterparts requires further investigation. This stems from two competing factors consisting of the higher thermal conductivity in SiC and the larger dimensions of die in Silicon facilitating effective heat extraction.

To this end, the aim of this thesis is to compare the electrothermal ruggedness for commercially available bipolar SiC power devices and their similarly rated Silicon counterparts by means of extensive experimental measurements, while comparisons of static and dynamic switching characteristics are also conducted. These devices are characterized in power electronics circuits in single-pulse, double-pulse, and continues switchings. Also of key interest is the static and dynamic performance and electrothermal ruggedness at larger on-state currents and under room or elevated operating temperatures.

1.2 Thesis Outline

This thesis is divided into seven chapters, where this Chapter is the first. Chapter 2 introduces the key power electronics applications of power semiconductor devices, followed by the properties of SiC as a wide-bandgap material. It will then discuss the fundamentals of bipolar device structures that are studied in this thesis together with the measurements that will be done on them in each of the following chapters.

Chapter 3 compares the switching characteristics for commercially available SiC BJT and their similarly rated Silicon BJT by using the double-pulse configuration under various operating temperatures at various collector currents. Due to the low current rating of SiC BJT, these tests are also repeated for two paralleled-connected Silicon and SiC BJTs to understand the impact of high-level currents and paralleling of BJTs.

Chapter 4 first compares the static properties for Silicon & SiC BJTs, sharing the same part number with that investigated in Chapter 3, by using a Source/Measure Unit (SMU) test equipment under various operating temperatures at various base currents and collector currents. This includes analysis of forward I-V characteristics, on-state resistance, DC gain, forward transfer characteristics and reverse leakage current. These measurements are also repeated for two-paralleled BJTs and compared with the case of single devices.

Chapter 5 first compares the switching performance of commercially available SiC MPS diodes and their similarly rated SiC Junction barrier Schottky (JBS) and Silicon PiN diodes by using the designed double-pulse test circuit under various operating temperatures and switching rates. Their on-state performances are also characterized under various temperatures and forward currents. Unclamped Inductive Switching (UIS) test configuration is introduced to apply significant electrothermal stress to these power diodes

until failure by avalanche breakdown, which is repeated under high initial temperatures. Finally, the forward current conducted by the power diodes is significantly increased during the surge current measurements until observation of pronounced degradation trends in the device properties, measured by the SMU test equipment.

Chapter 6 which initially compares the switching performance of commercially available 15 kV SiC PiN diode and the 15 kV Silicon PiN diode by using a double-pulse test circuit. Their on-state voltages are measured at various forward currents. The conduction mode reliability of both 15 kV devices is also assessed by means of aggravated power cycling where the repetitive current pulses increase the junction temperature until thermal equilibrium is established. This led to the degradation of the I-V characteristics captured by using the SMU test equipment.

Finally, Chapter 7 summarizes the main conclusions arising from the work conducted in this thesis as well as proposes future work.

Chapter

2 Fundamentals of Bipolar Power Devices in Power Electronics

Various applications can be achieved by using power electronic devices, from the low voltages switch-mode power supplies in home appliances and medium voltages electric vehicles and robots, welding machines, to power converters for high-voltage direct current (HVDC) transmission systems rated at several gigawatts [13, 14]. Fig. 2.1 shows the application spaces, the operation switching frequency and power handling capability of different power semiconductor devices [15]. One of the main applications of power devices in this thesis is power transmission with power rating of 100 kVA and above.

High voltage power converters are built based on power semiconductor devices, these devices have been fabricated based on Silicon (Si) material. They are quite cheap and have been fully studied since the research of this material span a few centuries. In the past few decades, significant advances in the fabricating process of power devices have been achieved, which leads to massive fabrication of Silicon power devices. However, the new emerged Silicon Carbide (SiC) has become an alternative choice. This is mainly because of the higher breakdown voltage, higher operating temperature, high switching speed etc. In this chapter, common power converter topologies for HVDC transmission schemes as

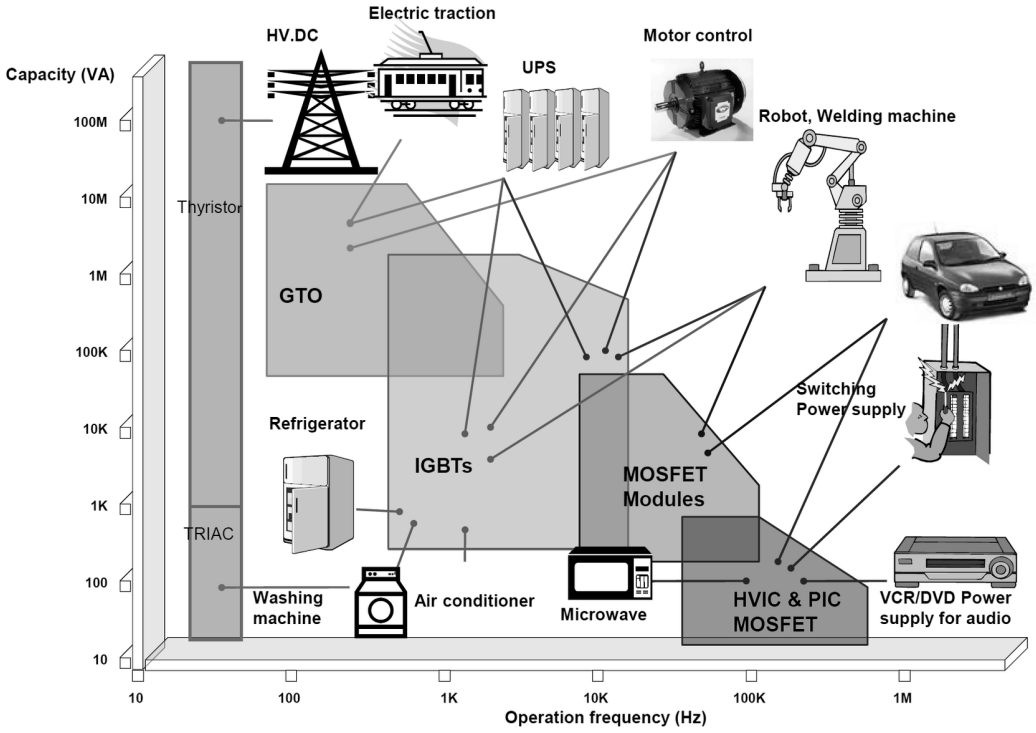

Figure 2.1: Applications of power semiconductor devices by power and frequency [15].

one of the key application spaces of power semiconductor devices, are firstly introduced. Next, the fundamental properties of Silicon Carbide together with the fundamentals and common structure of power bipolar semiconductor devices are introduced.

2.1 Power Converters for HVDC Transmission

2.1.1 Line Commutated Current Source Converters

Line commutated current source converter using mercury arc valves (which is also called thyratron valves) were developed for the first time in the Gotland Island transmission link to the mainland of Sweden in 1954 [16]. The introduction of silicon solid-state power devices, initially the thyristor, also known as the Silicon-controlled rectifier (SCR),

displace the use of mercury arc valve. This is because of the reduced maintenance time and improved reliability, together with higher rating and greater grid flexibility.

This Current source converters (CSC) need to reverse voltage to change power direction. Though this Line Commutated Converters (LCC) are simple, mature and of high efficiency, it can only operate in strong AC systems in order to receive commutation voltages. Furthermore, LCC schemes require large reactive power [17, 18]. These disadvantages can be eliminated in Self-Commutated Converter (SCC) configurations whose insulated gate bipolar transistor (IGBT) based Voltage Source Converter (VSC) with turn-off capability are favoured for HVDC transmission at the current time, if a very long-distance high voltages DC transmission is not required.

2.1.2 Voltage Source Self Commutated Converters

The first commercial self commutated VSC HVDC systems using IGBT were developed in Sweden in 1999 [19]. Since VSCs are required to conduct forward and reverse current, antiparallel diodes were connected to each IGBT in VSC-HVDC schemes. VSCs can operate at a higher frequency than that of LCCs (50 or 60 Hz) because IGBT can be turned off by removing the gate voltage and thus suits self-commutation schemes. Two-level or three-level VSC-HVDC converters are simpler to control, however had many challenges as hundreds of series-connected devices had to be switched simultaneously [20]. These led to the introduction of Modular Multilevel Converters (MMC) in 2010 [21] with isolated voltage source units creating sinusoidal voltages with little, if any, filtering requirement. For a conventional three-phase MMC with reference to Fig 2.2, it consists of six arms with n number of Switching Modules (SM), which is also called cells, series connected in each arm as indicated in Fig 2.3. The SM topologies can be of either Half Bridge (HB) or Full

Bridge (FB). HB configuration can only generate positive output voltage while that of FB can be bi-directional. Every submodule contains its own capacitor, generating a voltage of certain value when the submodule is turned on. The output voltage increases like stairway when a sufficient number of submodules are connected, resembles a sinewave. with very low levels of harmonic distortion. Hence, it does not need large filters to improve the waveform. However, it requires massive computing power and high-speed communication between the central control unit and arms, in order to control the voltage in every submodule. It is customary to trade-off between the complexity of control system and the size of filter when designing the MMC-based HVDC system.

Additionally, a very high current can flow through the antiparallel diode when fault occurs and is hard to be quickly removed or consumed. This problem does not hold true for the LCC systems since the fast converter control system and the current limiting reactors are capable of quick troubleshooting before restarting the system [18], alongside the excellent surge current ruggedness of Thyristors to avoid destruction. More details of catastrophic faults in VSC-HVDC configurations will be discussed in Section 2.5.4. To clear the fault current in VSC systems, the introduction of protective Thyristors is currently the most cost-effective method [24].

In order to deal with the increasing electricity demand while Silicon power devices reach their practical limit in terms of the power handling capability, research has shifted towards the Wide-Bandgap (WBG) semiconductor materials since the development of HVDC systems depends heavily on the performance of the power semiconductor devices.

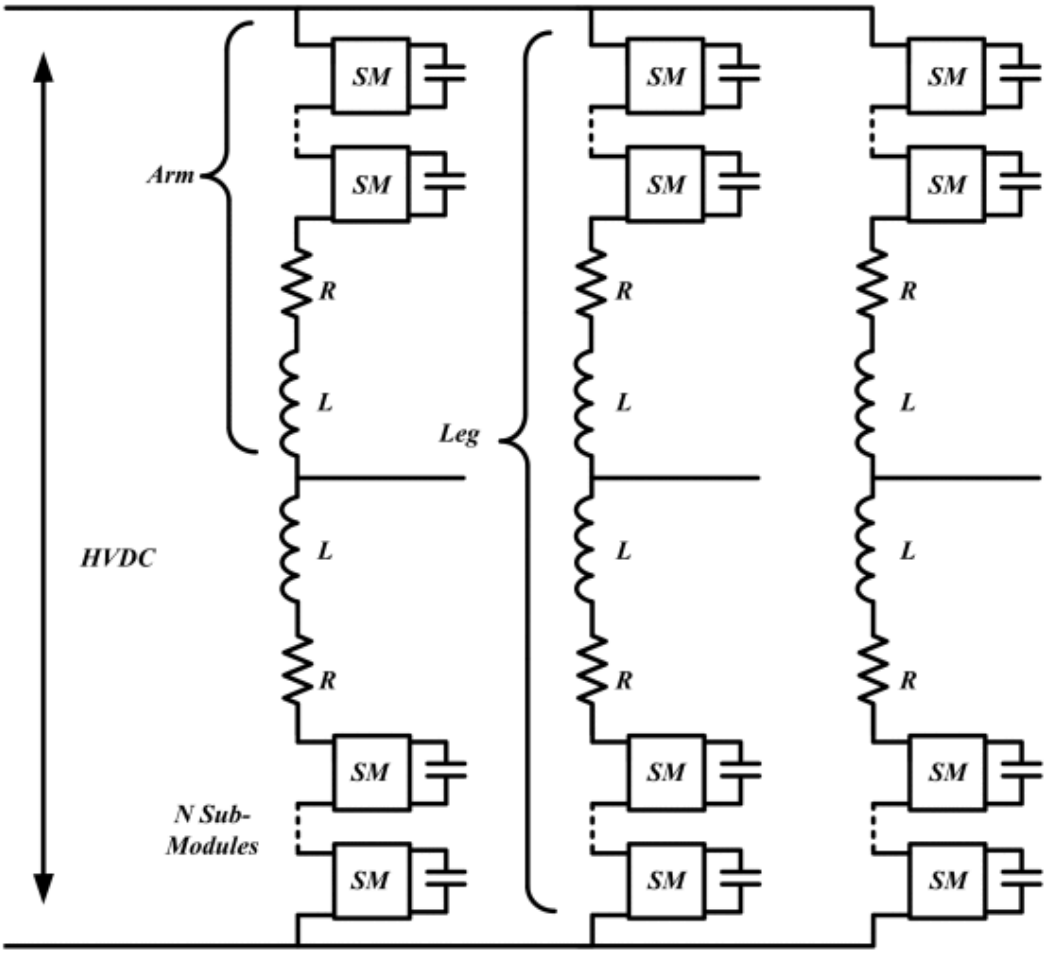

Figure 2.2: Schematic of three-phase Modular multilevel converter (MMC) in the VSC-HVDC system [22].

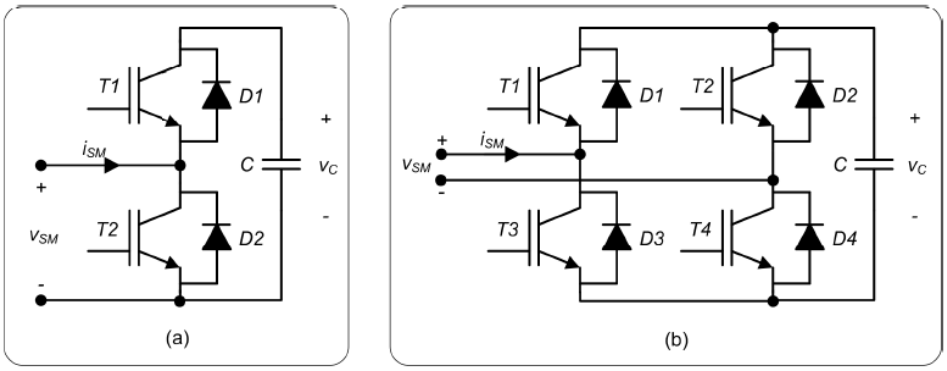

Figure 2.3: Topologies of SM: a) Half-bridge and b) Full bridge [23].

2.2 Bipolar Semiconductors

Power devices with different features are created to fit different applications. For example, power transistors usually act as power switches for power electronics converters. The power losses of devices consist of the on-state power losses, off state power losses, turn-on power losses and turn-off power losses. Trade-offs in device performance are necessary for real applications. For example, devices used for HVDC systems is required to introduce a thick voltage blocking (or drift) region where electric field can be easily expanded on it. However, it causes large on state resistance because of its low doping concentration. In order to reduce the on-state resistance while maintain the voltage blocking capability, bipolar devices, such as BJTs, thyristors and PiN diodes are attractive choices as the minority carriers (holes) can be attracted by the majority carriers (electrons) and be injected into the drift region, which can significantly reduce the on-state resistance. This is referred to as conductivity modulation effect as will be explained further in the rest of this chapter. On the other hand, unipolar devices like MOSFET, where only the majority carriers dominate the current conduction without the conductivity modulation, can lead to higher on-resistance when compared to bipolar devices. However, bipolar devices may suffer slow switching transition since extra time is spent on the electron-hole recombination process during turn-off, also referred to as reverse recovery process. For this reason, these devices are not suitable for high frequency applications.

Nowadays, the development of power semiconductor devices steps into the era of wide-bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) [25]. The scope of power semiconductor devices studied in this thesis is limited to SiC bipolar power devices which combine the capability of high operating frequency with the capability of high power-handling as shown in Fig. 2.1.

2.3 Fundamentals of Semiconductor Physics and Materials

SiC consists of covalent bonded Silicon and Carbon atoms and can be formed in different polytypes with distinct characteristics. Hexagonal 4H-SiC is the most common polytype because of its superior characteristics as shown in Table. 2.1 [1, 17, 18, 26, 27]. The wider band gap (E_G) between the conduction band and the valence band in WBG materials leads to higher critical electric field ($\mathscr{E}_C$) [28] especially for 4H-SiC which is over eight times higher than that of Silicon. The higher critical electric filed in 4H-SiC leads to better trade-offs between on-state resistance and breakdown voltage [15]. i.e., for unipolar devices, the on resistance of 4H-SiC can be 500 times smaller than that of Silicon for the same breakdown voltage while a 10 times higher breakdown voltage can be achieved for the same width of the drift region [29]. The higher band gap also delivers the much lower intrinsic carrier concentration (n_i) leading to low leakage current in 4H-SiC power devices. The low intrinsic carrier concentration also results in a much larger built-in voltage and thus larger on-state power dissipation. The two times higher electron saturation velocity in 4H-SiC means a faster switching transient than that of Silicon. The relative dielectric constant plays a dominant role in determining the junction capacitance of Schottky diode and thus its switching performance. The higher thermal conductivity of 4H-SiC favors high temperature applications since heat can be removed from the junction more quickly. The most dominant SiC polytype to date is the 4H-SiC because of the higher carrier mobility and wider band gap compared to its counterparts. Hence, from this point onwards the 4H-SiC will be referred to as the 'SiC'. Though SiC bipolar devices have clear advantages for high temperatures and high voltage applications, its disadvantages, such as high capital

cost and low current rating cannot be ignored.

Table 2.1: The material properties of Silicon and SiC polytypes at 300 K [1,17,18,26,27].

Parameter	Unit	Silicon	4H-SiC	3C-SiC	6H-SiC
Bandgap (E_G)	eV	1.12	3.26	2.36	3.02
Critical electric field ($\mathscr{E}_C$)	MV/cm	0.25	2.2	2	2.5
Intrinsic carrier density (n_i)	cm^{-3}	1.5×10^{10}	5×10^{-9}	0.1	1×10^{-6}
Elec. saturation velocity ($V_{sat(n)}$)	10^7 × cm/s	1	2	2.5	2
Relative dielectric constant (ε_r)	-	11.7	9.7	9.72	9.66
Thermal conductivity (λ)	W/cm·K	1.5	3.3-5	3.3-5	3.3-5
Hole Mobility (μ_p)	cm^2/V·s	495	120	40	80
Electron Mobility (μ_n)	cm^2/V·s	1360	1140	1000	500

Most of power semiconductor devices includes P-N junction. It is a junction formed between P-type semiconductor and N-type semiconductor. These two regions are created by adding dopants into the intrinsic Silicon or SiC. When the P-N junction is formed, electrons in the N-type region move toward the P-type region and recombine with holes while the holes in the P-type region move toward the N-type region and recombine with electrons. This causes a depletion region where only contains immobile ionized atoms. In steady state with zero-bias, the Built-in voltage (V_{bi}) exists at the depletion region that prevents carriers from diffusing across it [2]:

$$V_{bi} = \frac{kT}{q} ln[\frac{N_A^- N_D^+}{{n_i}^2}] \tag{2.1}$$

Where kT/q is the thermal voltage (V_T) in which k is the Boltzmann constant, q is the charge of an electron (1.6×10^{-19} Coulombs). The N_A^- and N_D^+ are the density of ionized acceptors and ionized donors on the two sides of the P-N junction. For the same ionized impurity concentration, the built-in voltage of P-N junction for Silicon is about 0.7 volts and about 2.8 volts for 4H-SiC [2,17]. The higher built-in voltage in SiC arises due to the much lower intrinsic carrier concentration.

When the P-N junction is forward biased, the applied potential reduces the size of depletion region as it pushes majority carriers to the other region. This in turn leads to the smaller potential difference by the level of the applied voltage, which promote the current flow. On the other hand, the depletion region expands when the device is reverse biased since the direction of applied voltage is same as that of potential barrier, thus only the reverse leakage current can flow through the device. When the applied reverse voltage exceeds a certain level, significant electric field imposed on the junction allows large current to flow. For high voltage power devices, this phenomenon usually happens at the lower doped side with a wide depletion region where carriers have extra room to be accelerated and collide with others [1,30]. This leads to more generated carriers as they collided to pass their kinetic energy on other atoms. This process is called Avalanche multiplication. Power devices can recover from the avalanche conduction when a low reverse current flows through, as can be observed in Chapter 5. However, if a significant current flows through junctions during the breakdown, it can lead to the destruction of power devices.

2.3.1 Carrier Mobility & Lifetime

Carrier mobility characterises how quick an electron or hole can drift under electric field. n and p are the concentration of electrons and holes separately. Carrier mobility for holes (μ_p) and electrons (μ_n) in Silicon reduces with temperature [1], as in Eq. 2.2 and Eq. 2.3:

$$\mu_n(Si) = 1360 \left(\frac{T}{300}\right)^{-2.42} \tag{2.2}$$

$$\mu_p(Si) = 495 \left(\frac{T}{300}\right)^{-2.20} \tag{2.3}$$

And for SiC this is as in Eq. 2.4 and Eq. 2.5 [1]:

$$\mu_n(SiC) = 1140 \left(\frac{T}{300}\right)^{-2.70} \tag{2.4}$$

$$\mu_p(SiC) = 120 \left(\frac{T}{300}\right)^{-3.4} \tag{2.5}$$

The higher mobility of the electron in the conduction band compared to the hole in the valence band, results in a lower on state resistance for N-drift region based (n-type) semiconductor devices than P-drift region-based (p-type) semiconductors, especially for unipolar power devices. Such inequality between the mobility of holes and electrons stems from the differences between the shapes of the conduction and valence band minima [1], which is the nature for indirect band gap semiconductor materials such as Silicon and SiC. The temperature dependence of diffusion coefficient, obtained by using the Einstein equation, is given by [1]:

$$D_n(Si) \propto \frac{1}{T^{1.42}} \quad D_n(SiC) \propto \frac{1}{T^{1.70}} \tag{2.6}$$

$$D_p(Si) \propto \frac{1}{T^{1.20}} \quad D_p(SiC) \propto \frac{1}{T^{2.40}} \tag{2.7}$$

Where D_n is the diffusion constant of electrons while D_p is that of holes. When a large current flow through devices, the injected minority carrier exceeds the doping concentration of base region causing the surge of both carriers with respect to the charge neutrality $n = p$, the mobility of both carriers decreases because of the amplified mutual Coulombic interaction [1]. And the current dependence of diffusion coefficient is the same according to the Einstein equation.

Another important factor in a semiconductor device is the carrier lifetime, which is a measure of the rate of recombination of minority carriers. Three fundamental approaches have been studied [1, 2, 18] for the dissipation of energy in carriers. The first method is based upon the emission of a radiative photon to reduce energy level, which is called radiative recombination or direct band-to-band recombination. The second method entails the introduction of recombination centres formed by intrinsic defects or impurities and thus electrons and holes can drop and recombine at deep energy levels in the band gap. The third method is by releasing the energy to a third electron or hole with the participation of phonon, this process is referred to as Auger recombination. Thus, the total carrier lifetime can be expressed as [18]:

$$\frac{1}{\tau_{tot}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Rad}} \tag{2.8}$$

Where τ_{rad} and τ_{SRH} are the lifetime because of the radiative and the Shockley-Read-Hall (SRH) recombination processes. The effects of radiative recombination can be assumed to be negligible since both the Silicon and 4H-SiC are indirect band gap materials [31]. SRH lifetime is proportional to the level position of recombination centres. Inserting Recombination centres, such as gold or platinum into bandgap in Silicon [1], or Vanadium (V) [32] into SiC, can reduce the carrier lifetime intentionally. These extra diffused impurities

and intrinsic defects have energy states between the conduction bands state and valence band state and function as traps to assist them to lose their energy. The Auger lifetime is dominant in the heavily doped regions, or in lightly doped regions under high-level injection conditions. For low level injection (low currents), the SRH lifetime plays the most significant role. The Auger lifetime plays a more important role at high currents, leading to the decrease of total lifetime. The temperature dependence for the carrier lifetime of holes and electrons in Silicon and SiC for temperature less than 500 K can be expressed as [33–35]:

$$\tau_n(Si) \propto T^{2.20} \qquad \tau_n(SiC) \propto T^{1.72} \tag{2.9}$$

$$\tau_p(Si) \propto T^{2.80} \qquad \tau_p(SiC) \propto T^{2} \tag{2.10}$$

Since the carrier lifetime is the reciprocal of the recombination rate, the carrier lifetime of 4H-SiC is much smaller than Silicon, leading to a weak temperature dependence and faster switching transition. Another important metric in relation to the carrier lifetime is the diffusion length, which is the distance the minority carriers can move before they recombine. This is derived as:

$$L_{n,p} = \sqrt{D\tau} \tag{2.11}$$

In SiC, carrier lifetime is inhibited by intrinsic defects arise due to imperfections in the crystal, which also introduce deep energy states into the bandgap. In particular, the $Z_{1/2}$ E_C—0.65 eV) and $EH_{6/7}$ E_C—1.55 eV) centres [18, 36–39] have been identified as major carrier-lifetime killers in 4H-SiC and are introduced during epitaxy and ion implantation. These reduced lifetimes result in reduced carrier diffusion lengths, which in high voltage

bipolar devices means conductivity modulation cannot occur at optimum levels though the switching losses of devices for high frequencies are reduced. Due to this reason, high voltage bipolar devices (IGBTs and Thyristors) in SiC remain problematic unlike in Silicon where minority carrier lifetime can be engineered to yield optimal conductivity modulation. This leads to the low current rating of SiC bipolar devices compared to their Silicon counterparts. In [36], carrier lifetime is increased in a 220 μm drift layer (to support $\geq$ 25 kV) from 1.1 μs to as much as 33 μs using a 1400°C, 48 hours oxidation process. However, given the very thin drift regions required to sustain kVs in SiC, a modest lifetime of 10 μs will minimize forward voltage drop significantly. This is true for layers up to 200 μm (approximately 25 kV). Despite this, the p-n junctions in SiC still impose a minimum forward voltage of 3 V. Therefore, further increase in carrier lifetime is still desirable.

2.4 Fundamentals of Power PiN Diodes

Power PiN diode has a thick, very low doped 'almost intrinsic' ('i') region in order to block high voltages, sandwiched between a heavily doped N^+ region (the cathode) at one end and a heavily doped P^+ region (the anode) at the other end. This P-i-N structure gives rise to the term PiN diode. It is designed to conduct high currents in one direction with low on state resistance due to the conductivity modulation, while block high voltages with minimal reverse leakage current in the other direction. The typical structure of PiN diode is illustrated in Fig. 2.4.

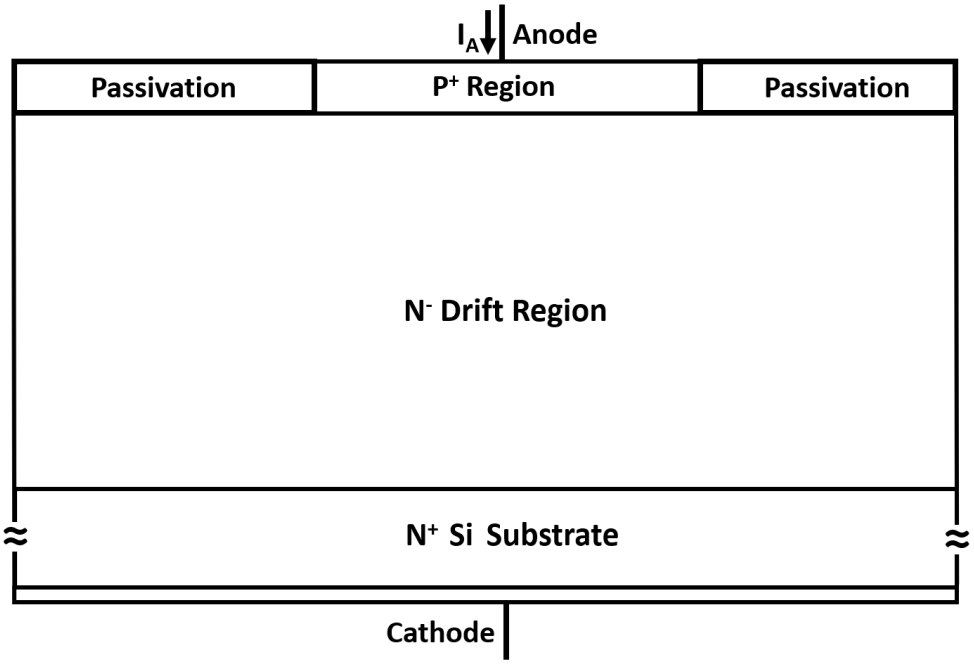

Figure 2.4: Simplified device structures for the Silicon PiN diode.

2.4.1 Forward Conduction Characteristic

When PiN diode is forward biased, the applied forward voltage exceeds the built-in voltage and pushes holes in the P^+ region to diffuse into the drift region while electrons in the N^+ region are pushed into the drift region to allow current conduction. Electrons reach the P^+N^- junction earlier than holes reaches the N^-N^+ junction because of the rapid diffusion rate of electrons. When the forward current is further increased, the excess minority carriers (holes) in the drift region can reach the N^-N^+ junction as the density of excess minority carriers is much larger compared to the doping concentration of the drift region. Such high density of holes in the vicinity of the N^-N^+ junction also attracts electrons in the high doped N^+ region to be injected into the middle region, in order to satisfy charge neutrality [1, 9]. This holds true for the excess electrons in the vicinity of the P^+N^- junction. This process leads to the presence of high density of both types of

carriers in the low doped drift region, which is much higher than the doping concentration. Therefore, it leads to the significant reduction of the on-state resistance and the conduction losses. This phenomenon is called 'Conductivity Modulation'. This is the determining factor of the on-state performance for almost all bipolar devices mentioned in this thesis, including PiN diodes, MPS diode and BJT. The carrier distribution of electrons and holes under high currents is shown in the Fig. 2.5.

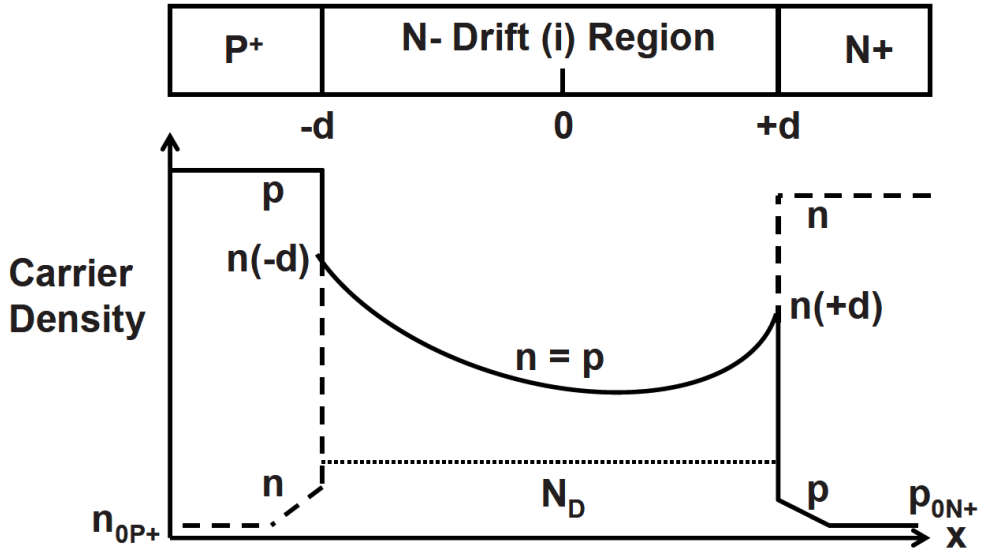

Figure 2.5: Carrier Distribution under High-Level Injection for a PiN diode [1].

It is worth to point out that the carrier density at the P^+N^- junction is higher than that of N^-N^+ junction, this is because of the higher mobility of the electrons compared with holes. The stored charge in the drift region can be calculated as in [40]:

$$Q_F = \frac{I_F W_D^2}{(\mu_p + \mu_n) V_{drift}} \tag{2.12}$$

where V_{drift} is the voltage across the drift region. The total on-state resistance for the PiN diode under high level injection is determined primarily by the resistance of the drift

region [9]:

$$R_{drift} = \frac{W_D}{(\mu_p + \mu_n) J_F \tau} \tag{2.13}$$

where J_F is the on-state current density. For the same forward current density, the degree of conductivity modulation for different devices is determined by the carrier lifetime since the carrier mobility decreases with the increasing of current as was described in Section 2.3.1. The combination of low carrier lifetime of holes as the minority carrier in the drift region and the low mobility of electrons as the majority carrier, means the conductivity modulation is imperfect in SiC devices when compared with those fabricated in Silicon where minority carrier lifetime can be engineered to yield optimal conductivity modulation.

2.4.2 Reverse Blocking Characteristic

When PiN diode is reverse biased and enter the reverse blocking mode, the reverse voltage draws the holes in the P^+ region and electrons in the N^+ region away from the junction leading the expansion of the depletion region. The depletion region will further expand with the increase of applied voltage. Such expansion of the depletion region mainly happens in the low doped N^- region due to the significant difference of the doping concentration with the high doped P^+ region, though there are very limited depletion region penetrated into the P^+ region. Therefore, the breakdown voltage (V_{BD}) is mainly determined by the width and the doping concentration of the drift region:

$$V_{BD} = W_D \cdot (\mathscr{E}_C - \frac{qN_{drift}}{2\varepsilon_S} W_D) \tag{2.14}$$

Where ε_S is the semiconductor permittivity, W_D is the width of the drift region and N_{drift} is the doping concentration of the drift region. The 10 times higher critical electric field in SiC compared to Silicon, as can be seen in Table. 2.1, leads to a 10 times smaller drift region width alongside a 100 times larger drift region doping in SiC power devices for the same breakdown voltage.

2.4.3 Switching Characteristic

For power electronics applications, diode operates in the conduction mode and the reverse blocking mode alternatively. The transition between these two modes can also lead to power losses. The transition from the off state to the on-state can incur overshoot in the anode voltage. This is mainly caused by the parasitic inductance, i.e., when the diode turns on and IGBT turns off, the *dI/dt* of the IGBT created at the parasitic inductance induce a voltage spike. While the more significant phenomenon happens during turn-off since the stored charge within the drift region of the power rectifier, which favours the low on state voltage drop, must be removed to enable the formation of the depletion region that can support high voltages. This leads to a large reverse current for a short time. This phenomenon is referred to as reverse recovery.

2.4.3.1 Reverse Recovery

The reverse recovery process, as illustrated in Fig. 2.6, consists of four stages.

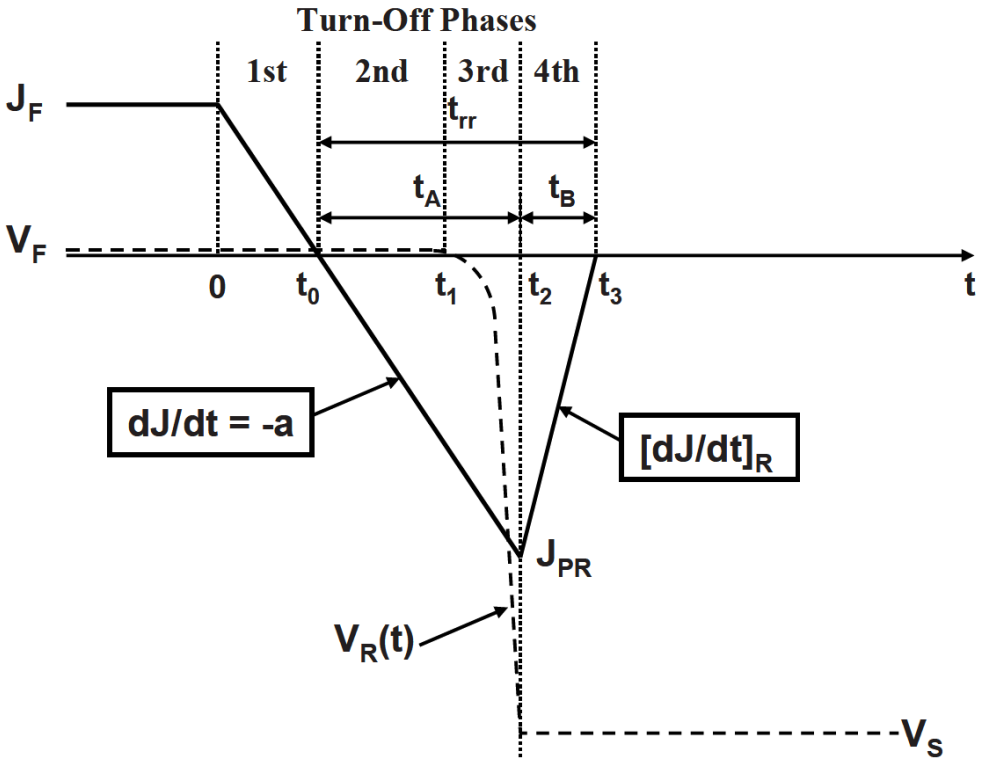

Figure 2.6: Typical voltage and current waveforms for the PiN diode during the reverse recovery process [9].

At time t = t_0, a reverse bias voltage is applied to the diode when using power electronics circuits with an inductive load. At this point the charge in the drift region of the device begins to be swept out and the recovery process begins. Between t_0 and t_1, the current gradually decreases at a constant rate ("a"), as shown in Figure 2.6. This constant rate is due to the fact that the full reverse voltage is applied across the load inductor before the PiN diode is able to block the voltage. At time t = t_1, the direction of the current flowing through the diode changes, causing the diode to begin conducting reverse current. During the time period from t_0 to t_1, the PiN diode remains forward biased and experiences a low forward voltage drop. Meanwhile, the reverse current continuously increases, as determined by the constant a. From t_1 to t_2, the majority of the charge

is removed from the drift region, allowing for the formation of the depletion region to support reverse voltage. At time t=t_2, the peak reverse current I_{RP} (or J_{RP}) occurs when the carrier concentration at the $P^+\backslash N^-$ junction reaches zero, allowing the formation of a depletion layer. During t_2 and t_3, the reverse current decays to the level of the static leakage current.

During this reverse recovery process, the excess carriers are removed from the drift region and depletion layers form at the P^+N^- and N^+N^- junction [1,2,17,18], eventually combining once all of these carriers has been removed. This process gives rise to a period of time during which both the current and voltage are large and negative and leads to large power dissipation during reverse recovery. The device's maximum switching frequency can be restricted and it may be necessary to reduce the device's operating current due to these limitations.

Apart from the forward overshoot and the reverse recovery process, the switching characteristic of 'Passive' power diodes, where both voltage and current commutes between 10% and 90% of its on-state value, is mainly controlled by the switching characteristic of power switch like IGBT and MOSFET [41–43]. Furthermore, the switching characteristic is also determined by parasitic elements, as will be discussed later in Chapter. 5.

2.4.4 High voltage SiC PiN Diodes

Despite the much thinner drift region allowing faster switching speed for SiC PiN diodes, the larger knee voltage in this device compared with the Silicon PiN diode [44] arises due to the larger bandgap of SiC [1]. To this end, the SiC Junction barrier Schottky (JBS) and Merge-PiN-Schottky (MPS) diodes are favourable because of the low voltage across the Schottky contact, and will be discussed in Section 2.5.

For High Voltage applications, typically more than 10 kV, bipolar power devices like PiN diode provide lower conduction losses compared to unipolar power devices like Schottky diodes. For example, PiN diodes connected in anti-parallel to the power Insulated Gate Bipolar Transistors (IGBTs), are required in a Self-Commutated Converter (SCC) high voltage transmission scheme [18] to enable bi-directional current flow. Due to the presence of conductivity modulation of the drift region, SiC PiN diodes merge high frequency with high voltage blocking while securing the low conduction losses and favors the high voltage applications. However, the static and dynamic characteristics of commercial 15 kV single SiC PiN diodes have not been fully studied yet, such as the self-heating effect and the conductivity modulation effect, alongside the lack of like-for-like comparison with the similarly rated Silicon counterpart, as will be explored in Chapter 6.

2.4.4.1 Principles of Bipolar Degradation

When SiC PiN diodes are subjected to long-term forward conduction, the drift of forward voltage can be observed which is called bipolar degradation, as one of the main reliability issues [12, 45] for SiC bipolar devices. This is because of the conventional dislocation defects in bulk SiC [18]. In this case, the formation of Shockley Stacking Faults (SSFs) in crystal, when a type of dislocation defect moves through the crystal lattice and leaves behind a misaligned layer of atoms, mainly arises from the basal plane dislocations (BPD) which propagate from the substrate into the epitaxial layer. Under forward bias, the propagation of these dislocation can happen at low temperatures [46,47] since the electron-hole recombination under high level injection provide sufficient energy to aid the formation and motion of dislocations. This process is also called recombination enhanced dislocation glide (REDG). An example of the expansion of SSFs is shown in [45]. The propagation of stacking faults decreases the degree of conductivity modulation and thus the increasing

on-state resistance leads to the upward drift of the forward voltage as shown in Fig. 2.7. To suppress stacking faults, a high-doped buffer layer has been introduced to convert the BPDs into the threading edge dislocations (TED) in substrates to avoid bipolar voltage drift [12].

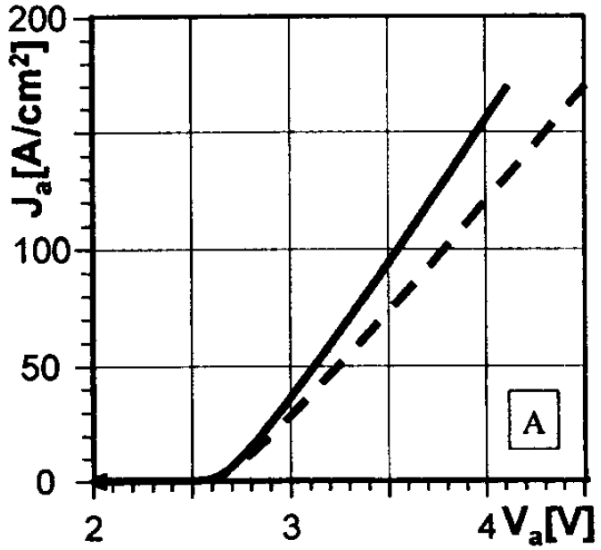

Figure 2.7: The forward I-V characteristic before (solid line) and after (dashed line) long term continuous operation [48].

Previously, long-term reliability of "own-made" high voltage SiC PiN diodes has been assessed [12, 45, 47, 48]. Nevertheless, these studies have not delivered a like-for-like comparison of long-term reliability among commercial power diodes with close power ratings. In Chapter. 6 of this thesis, power cycling tests are conducted to evaluate the long-term reliability of commercially available 15 kV SiC PiN diode and to provide a comparison with the similarly rated Silicon PiN diode.

2.5 Fundamentals of SiC Merge-PiN-Schottky (MPS) Diode

Schottky diode or Schottky Barrier Diode (SBD) is a unipolar device and contains metal-semiconductor contact proposed in 1938 [49]. The blocking voltage of early Silicon Schottky diode was up to 100 V [1, 2], albeit with fast switching performance because of the absence of stored charge. SiC Schottky diode has a better trade-off curve between the on resistance and the blocking voltage, which arises due to the much higher critical electric field in wide-bandgap materials. The simplified device structure of SiC Schottky diode is illustrated in Fig. 2.8.

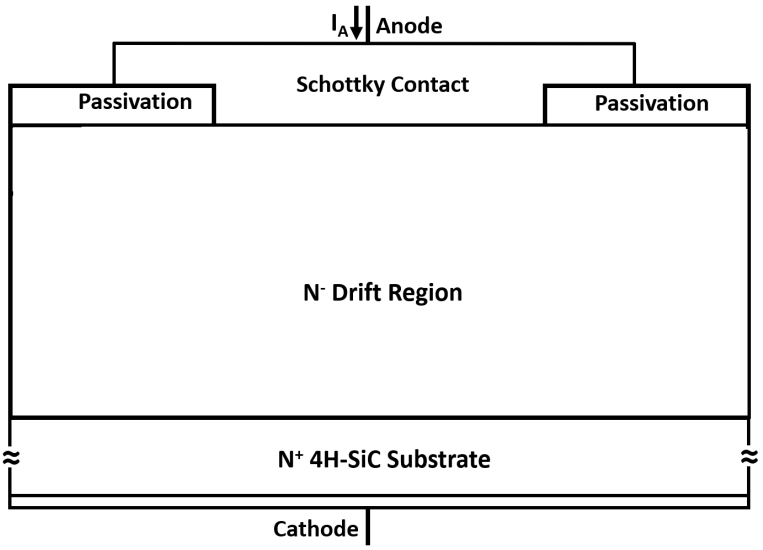

Figure 2.8: Simplified device structures for the SiC Schottky diode.

However, SiC SBDs, unlike other SiC power devices like SiC MOSFETs and SiC JFETs, still suffer from a poor reverse blocking performance. This is because the leakage current of SiC SBD is much larger compared to the aforementioned SiC devices even at low reverse blocking voltage of about 300 V before the onset of avalanche breakdown [1, 2, 9].

One of reasons for this significant leakage currents is the presence of surface defects at the Schottky contact [50]. In addition, the Schottky barrier height is reduced by the image force [1, 50] when the electric field is applied at the metal-semiconduction junction.

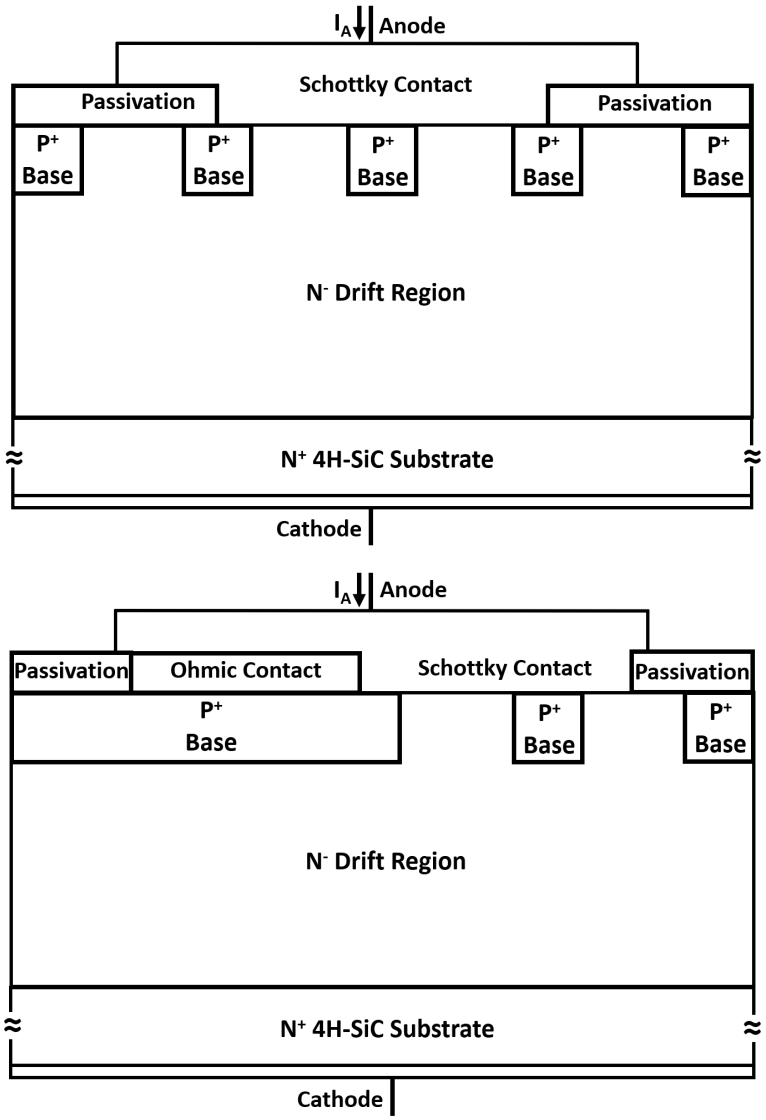

Figure 2.9: Simplified device structures for the SiC JBS diode and SiC MPS diode, respectively.

To solve this problem, 4H-SiC device manufactures moved towards the Merged PiN Schottky (MPS) structure which contains additional implanted P^+ well located just below

the Schottky contact, as can be seen in Fig. 5.1. This effectively enables to become one of the few available bipolar SiC devices. The space between P-N junctions in the MPS structure pinches off at small reverse bias voltage since the depletion region between P^+ and N^- region is formed to protect the Schottky contact from the high electric field. The greatly reduction of electric field at Schottky contact suppress both the Schottky barrier lowering and the surge of energy states at Schottky contact, both achieves a further reduction of leakage current in SiC MPS diode than that in Silicon MPS diode as the absence of surface defects in the latter devices. Junction Barrier Schottky (JBS) and MPS diode [9] are built based on this merged structure. JBS diode leads to the unipolar operation which favors high switching speed because of the absence of stored charge. To further improve the on state performance, the wide P^+ region in MPS diode promotes the conductivity modulation effect and thus it has low on state losses [51, 52].

Hefner [53] compares the dynamic and static characteristics between the Silicon PiN diode and the closely rated SiC MPS diode. The low on-state voltage drop and fast switching characteristic have been found in SiC MPS diode albeit with negligible conductivity modulation effect. When the forward bias exceeds the threshold voltage of the P^+N^- junction, the injection of holes from the implanted region starts to allow low on-resistance than the pure SiC Schottky diode. Nevertheless, previous studies have not delivered a comprehensive comparison of static and dynamic characteristics among commercial power diodes with close power ratings, as will be explored in Chapter 5.

2.5.1 Forward Conduction Characteristic

For the forward conduction characteristic of SiC JBS/MPS at very low current levels, thermionic emission process [1, 9] across the Schottky contact barrier height dominates,

the voltage drop across the Schottky contact is given by [9]:

$$V_{j,MPS/JBS} = \Phi_B + \frac{kT}{q} ln[\frac{J_F}{AT^2}] \tag{2.15}$$

Where Φ_B is the Schottky barrier height, A is the Richardson constant. Current transport via the Schottky contact is true at low current due to the larger potential required for the injection of holes into the drift region from the P-N junction. In this regime of operation, the on-state voltage drop of the MPS rectifier is smaller than that for the P-i-N rectifier. The increase of load current will lead to the occurrence of resistive voltage drop (V_R) across the drift region and substrate. The forward voltage drop (V_F) for the MPS/JBS diode is now given by [9]:

$$V_{F,MPS/JBS}(Low) = V_{j,MPS/JBS} + V_R = R_S J_F + \Phi_B + \frac{kT}{q} ln[\frac{J_F}{AT^2}] \tag{2.16}$$

R_S is the total on-state resistance as the sum of neutral region resistance and substrate resistance. At larger forward current densities of MPS diode [9], the injected minority carrier concentration in the drift region is much higher than the drift doping concentration leading to conductivity modulation resembles that in PiN diode, allowing the transport of a high current density through lightly doped drift regions with a low on-state voltage drop. However, the degree of conductivity modulation in MPS diode is lower than that in PiN diode because of the low carrier concentration for the MPS rectifier in the proximity of the implanted P^+ region, as can be observed in Fig. 2.10, while a uniform carrier concentration for PiN diode can be observed in Fig. 2.5.

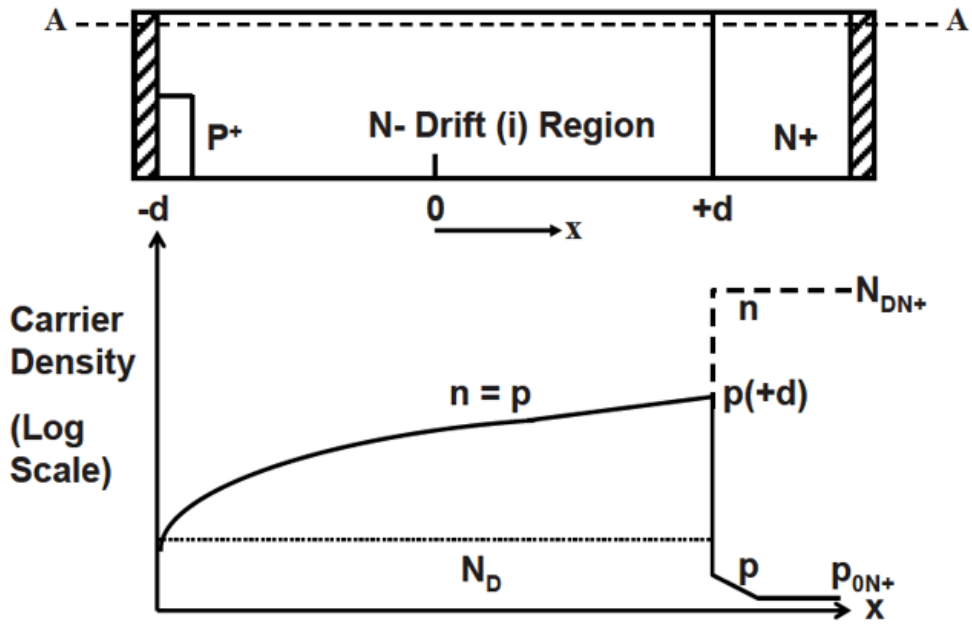

Figure 2.10: Carrier Distribution under High-Level Injection for a MPS diode [1].

2.5.2 Reverse Recovery

Although the high-level injection occurs in the MPS diode, it also increases the turn-off losses because of the reverse recovery process. However, this problem is less acute compared to that in PiN diodes because of the less stored charge in the drift region. This also allows the device to begin supporting a reverse voltage much faster than in the case of the P-i-N rectifier which shortens the reverse recovery process making the peak reverse recovery current of the MPS rectifier much smaller than that of the P-i-N rectifier. Consequently, this device is able to support a reverse blocking voltage immediately after the current reverses direction as illustrated in Fig. 2.11.

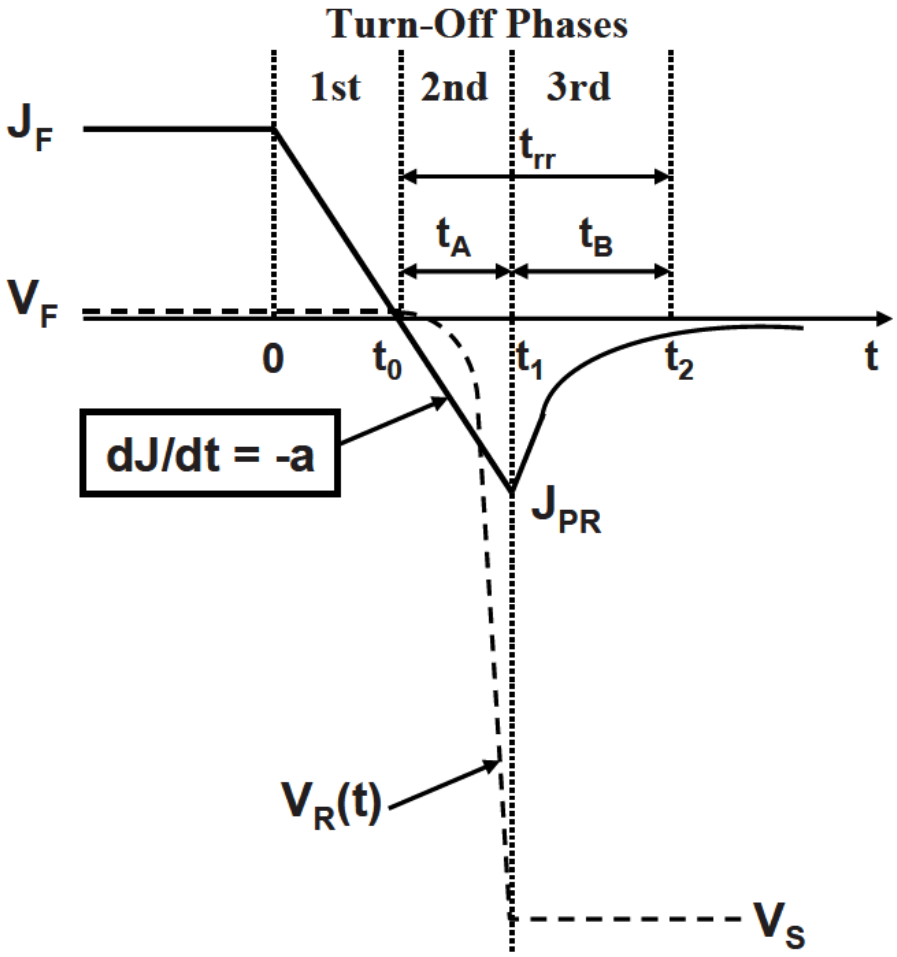

Figure 2.11: Current and Voltage waveform of reverse recovery performance for MPS diode [9].

2.5.3 Principles of Avalanche Breakdown

The aforementioned avalanche breakdown may happen when wires/cables are thin and long to cause large stray inductance in the power loop, where the load current flows through [30]. For high-frequency high-switching-speed applications, typically more than 50 kHz, the magnetic field of inductors will induce a counter Electromagnetic Force (EMF) to resist the abrupt change of inductor current when power switches turn off [54,55]. The

induced Drain-Source Avalanche Voltage (V_{AVA}) can be derived [54] as:

$$V_{AVA} = L_{Load} \times \frac{dI_{off}}{dt} + V_{DC} \tag{2.17}$$

Where L_{Load} is the load inductance, $\frac{dI_{off}}{dt}$ is the rate of change of current at turn-off. V_{DC} is the DC-link voltage. Such voltage usually reaches the breakdown voltage (V_{BR}) [56] and conducts large current, which is commonly referred to as Static avalanche breakdown. Power diodes also undergo avalanche breakdown during the reverse recovery process where devices operate with a high reverse current and a high reverse voltage [1], which has been referred to as Dynamic avalanche breakdown.

In avalanche, the electron-hole pairs are generated under high electric fields due to impact ionization [1, 2], where carriers traversing through the depletion region collide with atoms to create more carriers. More carriers can be generated with the increase of reverse current density j_R [1, 57]:

$$n_{ava} = \frac{j_R}{v_{sat(n)} \cdot q} \tag{2.18}$$

$$p_{ava} = \frac{j_R}{v_{sat(p)} \cdot q} \tag{2.19}$$

Where $v_{sat(n)}$ and $v_{sat(p)}$ are the saturation drift velocity for electrons and holes, n_{ava} and p_{ava} are the generated electrons and holes concentration during avalanche. The generated holes and the positively charged ionized donors increase the effective doping concentration [2], the electric field becomes large and may exceed the critical electric field $\mathscr{E}_C$ at the P^+N^- junction and diode fails due to the significant avalanche multiplication [1].

After the destructive avalanche breakdown, diode usually fails into short-circuit [58] and cannot withstand any breakdown voltage. The failure spots are usually found from the edge of the device located between the active region and the junction termination [1,30,59] as provided in Fig. 2.12.

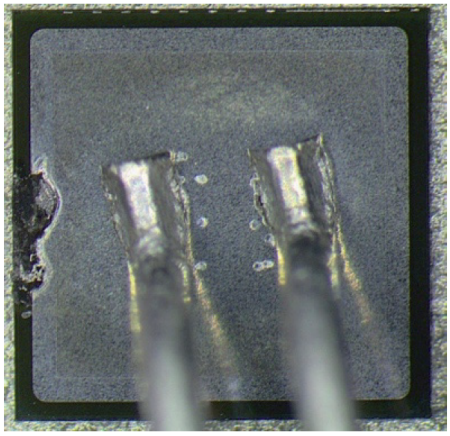

Figure 2.12: Failure pattern of SiC MPS diode after avalanche breakdown [60].

If the avalanche process happens at high temperatures, more free carriers are created. However, these carriers cannot gain enough kinetic energy to create more electron-holes pairs since they are restricted by the collision with atoms [1, 30, 61].

Previously, Static avalanche robustness of SiC MPS diode have been assessed [60, 62, 63] under Unclamped Inductive Switching (UIS) circuit, which will be described later in Chapter. 5. Nevertheless, these studies have not delivered a like-for-like comparison of Avalanche ruggedness among commercial power diodes with close power ratings at different operating temperatures, as will be explored in Chapter. 5.

2.5.4 Surge Current Robustness

Despite all the advantages of HB-MMC-VSC-HVDC configuration mentioned, pole-to-pole DC fault impose significant risk of cascade failure on IGBT/diode pairs. These

faults occur when the positive pole is directly connected to the negative pole, as shown in Fig. 2.13, because of mechanical damages leading to cable insulation failure [64]. Despite these fault types are not usual, serious effects on the system can be caused such as the annihilation of power electronic devices and the interruption of the whole DC transmission system since a very high faulty current flows through the network components. In addition to the network impedance, VSC operates as an uncontrolled full-bridge rectifier following the shutting down of the main switches, and the grid continues to supply the fault from the AC grid [64, 65]. This grid feeding current is the most dominant portion of the faulty current in MMC VSCs shown in Fig. 2.2 and 2.3, and may cause damage of the freewheeling diode.

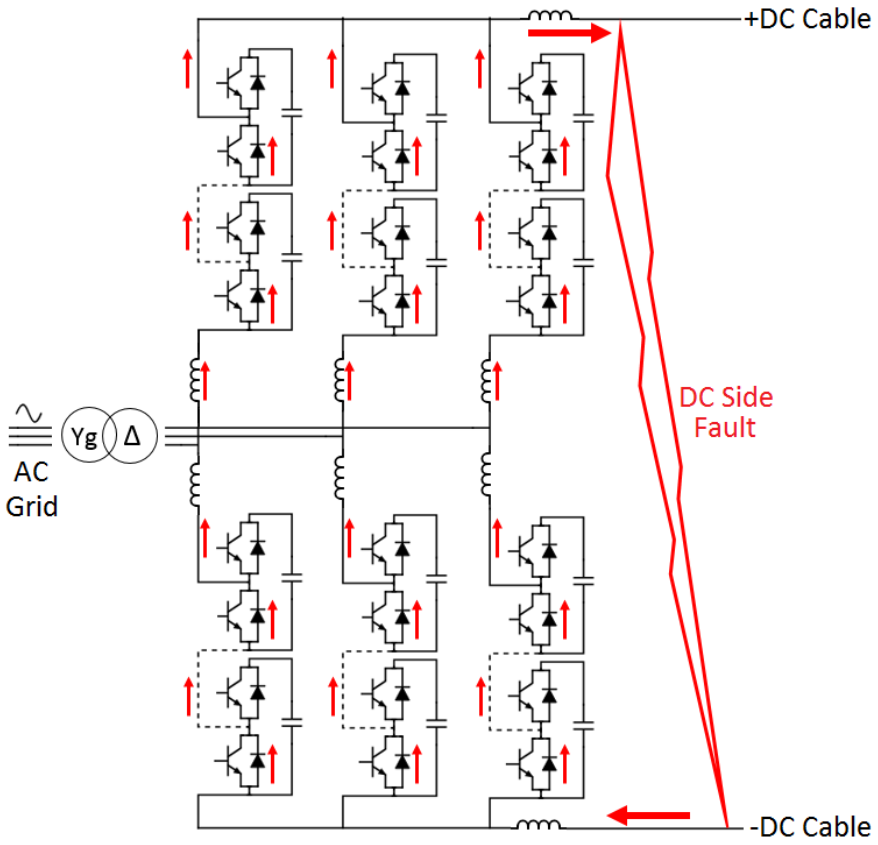

Figure 2.13: The pathways for DC fault current [24].

After the significant current-flow with long pulse length, failure can be found from the edge termination and from the middle of the chip as shown in Fig. 2.14 [66]. While for shorter pulses with high chip temperature, the melting metallization is observed due to the presence of high localised temperature around the bond feet. Brunt [67] also observed that the failure pattern is located close to the wire bonds for short surge current pulses.

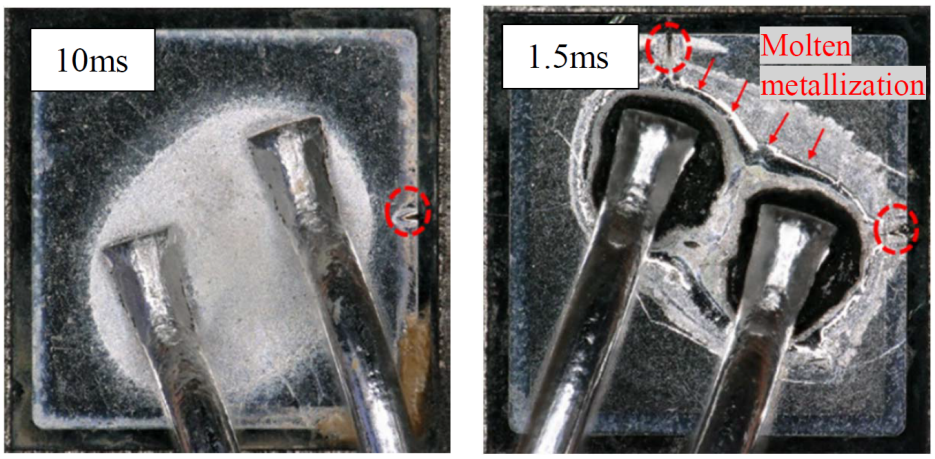

Figure 2.14: Failure pattern after surge current tests for various pulse lengths [66].

Palanisamy [68] found cracks at the back side of the chip after the surge current test. Hotspots lead to a much higher leakage current when the device operates in the reverse blocking mode.

Previously, surge current robustness of SiC MPS diode have been assessed [66, 67, 69–73]. Nevertheless, these studies have not delivered a like-for-like comparison of surge current robustness among commercial power diodes with close power ratings at different operating temperatures, as will be explored in Chapter 5.

2.6 Fundamentals of Power BJTs

Power Silicon bipolar junction transistor (BJT) is usually applied as switch in low and medium voltage ($\leq$1700 V) applications. In the common-emitter (CE) configuration, BJTs require continuous base current to control the current flowing from collector to emitter in the NPN structure, the low common-emitter current gain (β) in vertical Silicon BJTs makes it not an attractive choice for power applications because a complicated base driver is required for large base currents. However, this is set to change with the emergence of the 4H-SiC BJTs which enable a significantly higher DC current gain and faster switching speed than Silicon BJTs [2,3,5]. SiC BJTs have the potential to displace gated transistors, i.e. MOSFETs and IGBTs, in DC-DC boost converter [74] due to advantages such as low on-state resistance due to the conductivity modulation effect and the absence of the gate channel, especially when compared with SiC MOSFETs, as the gate oxide imposes ruggedness instabilities at high temperatures [3–5]. Furthermore, SiC BJTs have higher transconductance when compared with SiC JFETs [3].

Novel structures of base drivers are recently proposed [75] and installed on DC/DC step-up converters fabricated by SiC BJTs, minimising the base current and hence the power loss. The theoretical capabilities of 4H-SiC BJTs, such as the small on-state and switching losses have made it a potential candidate for high voltage converters [76].

The higher current gain, namely, $\beta = I_C/I_B$, in SiC is mainly due to the smaller dimensions of the base and the drift region for the same blocking voltage, achieved by the much higher critical electrical field in SiC. At the low doped base region, the injected electron concentration can become much higher than the base doping concentration when the density of collector current is high. This is referred to as the high-level injection (HLI) in the base area with a large concentration of both electrons and holes. This reduces the

base resistance to allow a lower on-state voltage-drop. However, it is reported [1, 77] that the DC current gain is reduced under the same circumstance resulting in a low efficiency of the base driver.

For both the static characteristics including DC current gain and the dynamic characteristics including the turn-on and turn-off transitions, the variation of temperature and collector current play an important role. Although [5] investigated the temperature dependence of the switching performance of SiC BJT, the impact of collector current (or collector voltage) on static and dynamic performance of the single commercially available SiC BJT, as well as to compare with the similarly rated single Silicon BJT, will be explored in Chapter 3 and Chapter 4, respectively.

Although the smaller size of SiC devices assists in reducing the parasitic capacitance enabling less oscillation for the output current [5] and, above all, improve the switching rate and current gain [5], the fabrication of large defect-free SiC discs is still a challenge limiting the current rating at on-state [78], as discussed in Section 2.3.1. Since the lifetime-enhancement technique [18] is not adequately mature at present, the improvements in the dynamic and static performance of SiC BJT by means of parallel connection will be shown in Chapter 3 and Chapter 4, respectively, as well as to compare with the Silicon BJTs.

2.6.1 BJT Switching Characteristic

This section provides the analytical modelings needed to understand the dynamic performances of power BJTs.

2.6.1.1 Turn-On Transient

BJTs require a positive base current for turn-on as well as to remain in on-state [1]. To turn-on the transistor, a positive base-emitter current is required to forward bias the base-

emitter junction. It takes time for the electrons injected from the base-emitter junction to diffuse and arrive the base-collector junction. This time interval is known as base transit time, given by [1]:

$$t_{transit} = \frac{W_B^2}{2D_n} \tag{2.20}$$

After this time interval, the depletion region generated by the reverse biased base-collector junction sweep the electrons toward the collector region to produce a collector current. The large collector current produced by a small base current leads to a high current gain. The minority carriers in the base region (electron) starts to develop. The time taken for the collector current to rise from zero to the on-state value can be derived as [1]:

$$t_{I-on} = \frac{W_B^2 J_C}{2D_n \beta J_B} = \frac{W_B^2}{2D_n} \tag{2.21}$$

The collector voltage remains constant during the rise of collector current because of the inductive load, which is used in Chapter 3. Afterward, the collector voltage drops to the on-state level while the collector current remains constant. This voltage-drop time is defined as the space charge built on both sides of the base-collector junction (Q_{sc}) per collector current as [1]:

$$t_{V-on} = \frac{Q_{SC}}{J_C} = \frac{qW_B N_B + qW_D N_D}{J_C} \tag{2.22}$$

The on-state voltage is limited by the stored charge in the drift region, i.e. the depleted part of the drift region become smaller which lead to a smaller voltage level. Faster voltage transition is expected at high collector currents. However, the smaller J_C is predicted in high temperatures because the diffusion coefficient decreases with temperature, which

results in t_{V-on} to increase with temperature. This is given by [1]:

$$J_C = \frac{2tJ_{Base}\beta D_n}{W_B^2} \tag{2.23}$$

2.6.1.2 Turn-Off Transient

To turn-off power BJT, a reverse base current is applied to extract the stored carrier from the base and drift regions. This time is known as the storage time or delay time and is defined by [1]:

$$t_S = \left(\frac{J_C}{J_{BR}}\right)\left(\frac{W_{NM}^2}{4D_n}\frac{J_C D_P}{J_C D_P + J_{BR} D_n} + \frac{W_B^2}{2D_n}\right) \tag{2.24}$$

where J_{BR} is the Reverse base current density, W_B is the width of the base region and the width of the conductivity-modulated region (W_{NM}) is:

$$W_{NM} = \frac{2qD_n}{J_c}\left(P_{NS}(0) - N_D\right) \tag{2.25}$$

Which will be discussed later in detail. This time is longer than the turn-on transit time because the stored charge removal happens at both the base and drift regions. The first term can also be expressed as β so the whole expression will not be directly influenced by the base current and the collector current. For higher temperatures, the diffusion coefficient will decrease leading to a slower depletion process while the conductivity-modulated width W_{NM} decreases with increasing collector currents [1] which is the dominant factor to reduce the delay time.

The voltage turn-OFF time is given by [1]:

$$t_{V-off} = \frac{\sqrt{2\varepsilon q N_D V_C}}{2\frac{p(W_S)}{W_S} q D_p} \tag{2.26}$$

The variation of t_{V-off} under different temperatures or at different currents is determined by the diffusion coefficient. This leads to a larger t_{V-off} at high temperatures or at high collector currents.

After the voltage rise phase, the collector current drops to off-state. This time is decided by the remaining carriers in the base after the voltage transients, and can be written as [1]:

$$t_{I-off} = \frac{W_E - X_V}{\frac{2W_E D_n}{\beta W_B^2} - \frac{D_n}{L_n}} \tag{2.27}$$

where X_V is the turned-off length in the base region by the voltage rise phase and W_E is the width of the half of the Emitter Finger. The diffusion length Ln can be expressed as:

$$L_n = \sqrt{\tau_n D_n} \tag{2.28}$$

2.6.2 On-State Characteristics

To analyse the static performance of SiC BJTs and compare with their Silicon counterparts, the basic principle of operation of power BJT during on-state must be first discussed. As was described in Section 2.6.1.1, the forward-biased base-emitter junction and the reverse-biased base-collector junction initiate the current conduction. However, there are some other modes of operation during on-state at low collector voltage for the

resistive load circuit. Similar to MOSFET [17], these modes are formed by the variation of the applied base-emitter current and the applied collector-emitter voltage, which determines the electrical conductivity and current gain of BJTs.

When the collector-emitter voltage is smaller by the magnitude of the threshold voltage of the base-collector junction compared to the base voltage ($V_{CE} \leq V_B - V_{th\text{-}BE}$), BJT operates in the saturation region as shown in Fig. 2.15. Both the base-collector and the base-emitter junction are forward biased. The base current flowing into the emitter region initiates the injection of electron from the emitter region into the base region, while the component of the base current flowing into the drift region allows the injection of minority carriers into the low-doped drift region and eventually lead to conductivity modulation of this region and low on-state resistance [9]. The base current flowing into the drift region is also required to maintain such stored charge.

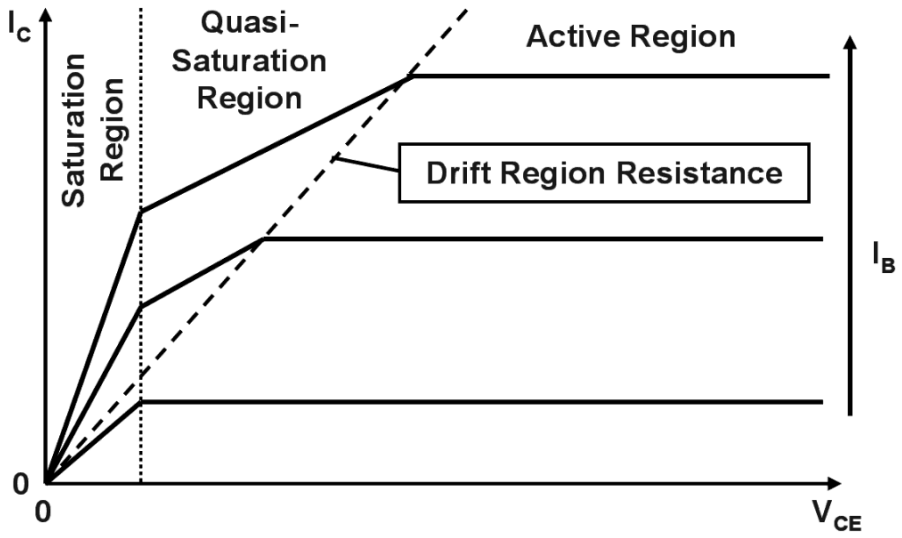

Figure 2.15: Output (I-V) characteristic for BJT at various collector voltages [1].

When the collector voltage is increased to reduce the base-collector voltage to less than the knee voltage of the base-collector junction, BJT enters the quasi-saturation

mode. The degree of conductivity modulation in the drift region becomes smaller as the width of the conductivity-modulated region (W_{NM}) reduces as illustrated in Fig. 2.16.

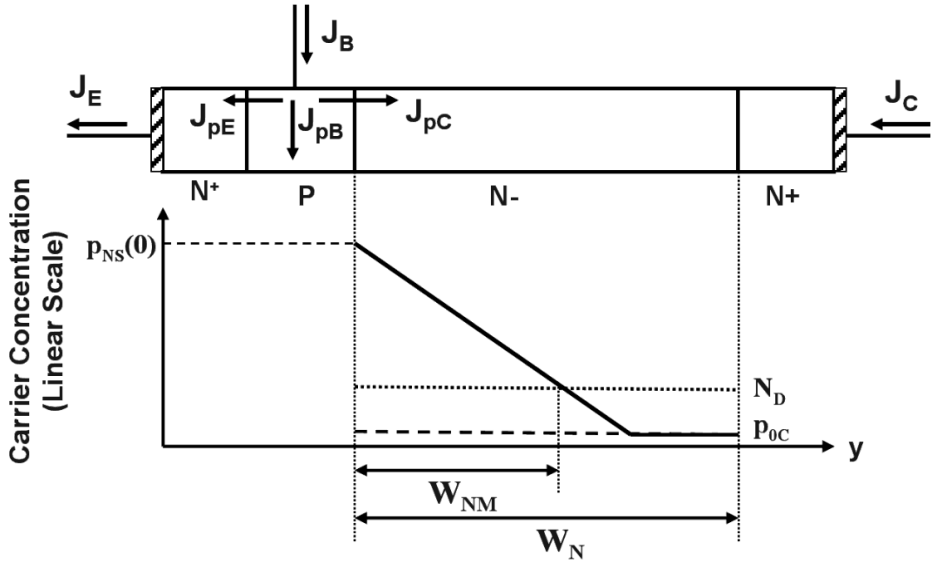

Figure 2.16: Reduction of the minority carrier concentration for BJT in the drift region when operates in the quasi-saturation region [1].

Such width is given by [1]:

$$W_{NM} = P_{NS}(0)\frac{2D_n q}{J_c} \tag{2.29}$$

where $P_{NS}(0)$ is the hole concentration at the base-collector junction. Therefore, the stored charge in the drift region alongside the base current flowing into this region becomes smaller. Eventually, this modulated region becomes very small, and the on-state resistance of the drift region is reduced to:

$$R_{drift,no-modulation} = \frac{W_D}{qN_D\mu_n} \tag{2.30}$$

Which is similar to Eq. 2.13. BJT enters the active region when the collector voltage is

further increased to reverse-bias the base-emitter junction. The collector current almost remains constant which is determined by the product of the base current and the current gain. The DC current gain is further increased because of the expansion of the depletion region on both sides of the base-collector junction resulting in less recombination of carriers in the base and drift region. The common-emitter current gain, which is mainly determined by the emitter injection efficiency (γ_E), can be expressed as [1]:

$$\beta \approx \gamma_E = \frac{J_n(0)}{J_p(0)} \tag{2.31}$$

where $J_p(0)$ is the hole current density at the base-emitter junction, $J_n(0)$ is the electron current density at the base-emitter junction.

With the further increase of collector current, the injected electron density in the base region can exceed the effective hole density at base p_B. This leads to the increase of $J_p(0)$ to maintain the charge neutrality at the base-emitter junction:

$$J_p(0) \propto 1 + \frac{n_B}{p_B} \tag{2.32}$$

where n_B is the injected electron concentration into the base region. Eq. 2.32 indicates that J_p become proportional to n_B, this leads to the extra recombination in the emitter region and thus the reduced current gain. Such decrease of current gain is referred to as high-level injection (HLI) or Webster effect in the base region. The boundary between the increasing β with collector current and the decreasing β with collector current is determined by the Webster current density J_w [1, 5, 79]:

$$J_W = \frac{qD_{nB}p_B}{W_B} \tag{2.33}$$

The onset of Webster effect can be experimentally seen when the increased collector current density approaches J_W.

When the base-emitter voltage is increased by the larger base-emitter current, this can lead to the rise of electron concentration in the base region and thus promote the on-state current flow. The maximum electron concentration in the base region closest to the base-emitter junction ($n_B(0)$) is given by [1]:

$$n_B(0) = n_{0B} \cdot e^{\frac{V_{BE}}{kT}q} \tag{2.34}$$

Where n_{0B} is the minority carrier concentration in the base region:

$$n_{0B} = \frac{n_i^2}{N_B} \tag{2.35}$$

2.7 Summary

This Chapter discussed the basic fundamentals of high voltage grid-connected power converters as one of the key applications spaces of power semiconductor devices. This was followed by the fundamental of Silicon Carbide whose material properties are superior to conventional Silicon. Additionally, a review of previous studies highlighted the reliability issues of SiC bipolar devices. The physics of operation and basic failure mechanism of power bipolar devices were also discussed to enhance understanding and to explain the experimental results shown in Chapters 3 to 6.

Chapter

3 High Voltage Silicon & SiC NPN BJTs: High Level Injection & Paralleled Dynamics

The results published in journal paper 1 and conference paper 1 in Publications list at the outset of the thesis are used in writing of this Chapter. I acknowledge the contribution of my supervisors for laying out the specific objectives, and my co-authors on the methodology and accuracy of the analysis. I have done the Measurements at Bristol's EEMG research laboratory, analysed the results and drafted the papers.

SiC BJTs are already demonstrated in applications such as the 200 A and 50 kW DC power converter in [80], which was integrated by 4H-SiC BJTs, delivering very high efficiency for application in electric vehicles. It is demonstrated in [80] that each SiC BJT has a current density of over twice that of Silicon IGBTs together with a larger current handling capability than that of SiC MOSFET [7]. High-voltage ($\geq$800 V) BJTs are also still in demand as deflection transistors in specific electronic screens [81]. In absence of a need for reverse conduction, as the case of boost converters, SiC BJTs are also shown to have an outstanding conduction efficiency when compared with unipolar devices [82].

As discussed in section 2.6, this chapter demonstrates the dynamic performance of commercially available 4H-SiC BJTs together with its Silicon counterpart by using the

double-pulse configuration under a wide range of temperatures (25°C to 175°C) and collector currents (about 1 A to 8 A). Since it is common practice to connect devices in parallel to increase the total current rating, especially true for SiC BJT with low current rating shown in Table 3.3. The switching performance of paralleled SiC and Silicon BJTs is also studied. Section 2.6.1 and Section 2.6.2 have already presented the theoretical models required to understand the switching transients and current gain of power BJTs, the experimental set-ups are shown in Section 3.1. Section 3.2 presents the measurement results followed by Section 3.3 concludes the chapter. The simplified device structure of Silicon BJT and that of SiC BJT are shown in Fig. 3.1.

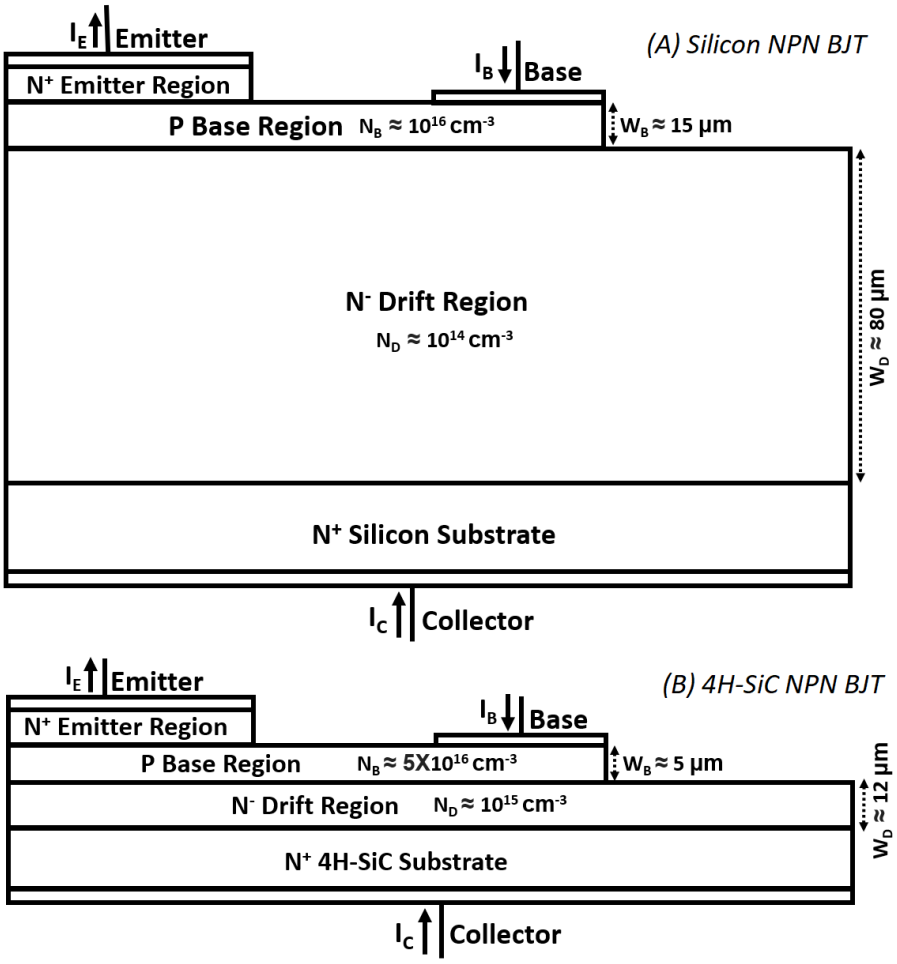

Figure 3.1: Simplified device structures with half-cell for (a) Silicon and (b) 4H-SiC power NPN BJTs [5, 83].

3.1 Experimental Set-Up

A wide range of experimental measurements and LTSpice simulations are done to observe the effect of collector current and temperature on single and paralleled high-voltage Silicon and 4H-SiC power BJTs. These devices are tested on the commercial double-pulse test board GA100SBJT12-FR4 driven by the commercial isolated gate driver GA03IDDJT30-FR4, with parameters shown in Table. 3.1 and Table. 3.2 separately.

Table 3.1: Parameters of the double-pulse test Board GA100SBJT12-FR4 [84].

Parameter	Symbol	Value
$C_{bank}(C_{DC})$	Bank Capacitance (DC-link capacitance)	5 μF
L_{Stray}	Estimated Parasitic Inductance	62.5 nH
$V_{DS,MAX}$	Maximum allowable test voltage	1200 V
$I_{D,MAX}$	Maximum allowable drain current	100 A

Table 3.2: Parameters of the isolated gate driver GA03IDDJT30-FR4 [85].

Symbol	Parameter	Value
V_{CC}	Input Supply Voltage of driver	12 V
$V_{isolation}$	Isolation Voltage	3000 V
t_{rise}	Base Voltage Rise Time	21 ns
t_{fall}	Base Voltage Fall Time	14 ns
$I_{B,peak}$	Peak Base Current	4 A
$I_{B,steady}$	Continuous Base Current	0.35 A
$R_{B,pre}$	pre-installed base resistance	3.75 Ω

A 1.2 kV SiC freewheeling diode C4D10120H and a 2.2 mH load inductor are also connected to this double pulse board. During the double-pulse test, the power switch (BJT in this chapter) firstly turns on to allow the load current to linearly increases during the time period of the first pulse from 0 to t_{Q1}. The load current is determined by the following expression:

$$I_{load} = V_{DC} \frac{t_{Q1}}{L_{load}} \tag{3.1}$$

where t_{Q1} is the length of the first pulse, L_{load} is the load inductance. The maximum load (collector-emitter) current within the first pulse is controlled by its pulse length t_{Q1}, which is linearly increased from 5 μs to 40 μs in steps of 5 μs by using an Agilent 33220A 20 MHz arbitrary waveform generator. Every 5 μs roughly equals to an increase of 1 A in collector current up to its maximum value of 8 A. However, the turn-off delay in Silicon BJT incurs the higher load current as discussed later in this chapter.

Then BJT switches off to evaluate its turn-off performance and remains off-state for 30 μs. During this period, the load current is commutated from BJT to the freewheeling diode. Then BJT switches on to evaluate its turn-on performance and remains on-state for 8 μs, followed by the last switch-off to end each double-pulse experiment.

The maximum load current was set to 8 A due to the lower current rating of SiC BJTs, especially at high temperatures as shown in Table. 3.3. The base resistance of the driver is changed between 3.75 Ω and 11.75 Ω by connecting the external gate resistor of up to 8 Ω to the gate driver board. The operating temperature is increased from 25°C to 175°C in increments of 25°C by using ITC-100RL PID Temperature Controller, together with a small aluminum heating blocking.

Table 3.3: BJTs' parameters from datasheets [86, 87] (T = 25°C unless otherwise noted).

	Silicon BJT	4H-SiC BJT
Model	FJL6920	GA04JT17-247
Manufacturer	Fairchild/ON	GeneSiC
Max Collector-Emitter Voltage (V)	800	1700
Max Collector Current (A)	20	15
Max Collector Current at >160°C (A)	20	4
Junction to case Thermal Resistance (°C/W)	0.625	1.41
Max DC Current Gain - β (-)	8	100
Base-Emitter Saturation Voltage (V)	1.5	3.45

Power BJTs characterized in this chapter are Fairchild Silicon BJTs FJL6920 and GeneSiC 4H-SiC BJTs GA04JT17-247 where the detailed parameters are shown in Table. 3.3. The higher voltage rating of SiC devices is the key parameter that gives SiC its edge on performance and efficiency, and this limits the options within Silicon BJTs. Double pulse testing under supply voltage of 800 V, provided by an ETPS power supply with rating voltage up to 4 kV, is reasonably high voltage to demonstrate the capability of the power BJTs to enable a fair comparison between the two device technologies. Two GW-Instek GDP-100 100 MHz voltage probes and a PEM CWTMini50HF current Rogowski coil with bandwidth of 50 MHz are connected to a Keysight MSO7104A 1 GHz 4 GSa/s oscilloscope to obtain waveforms of measurement.

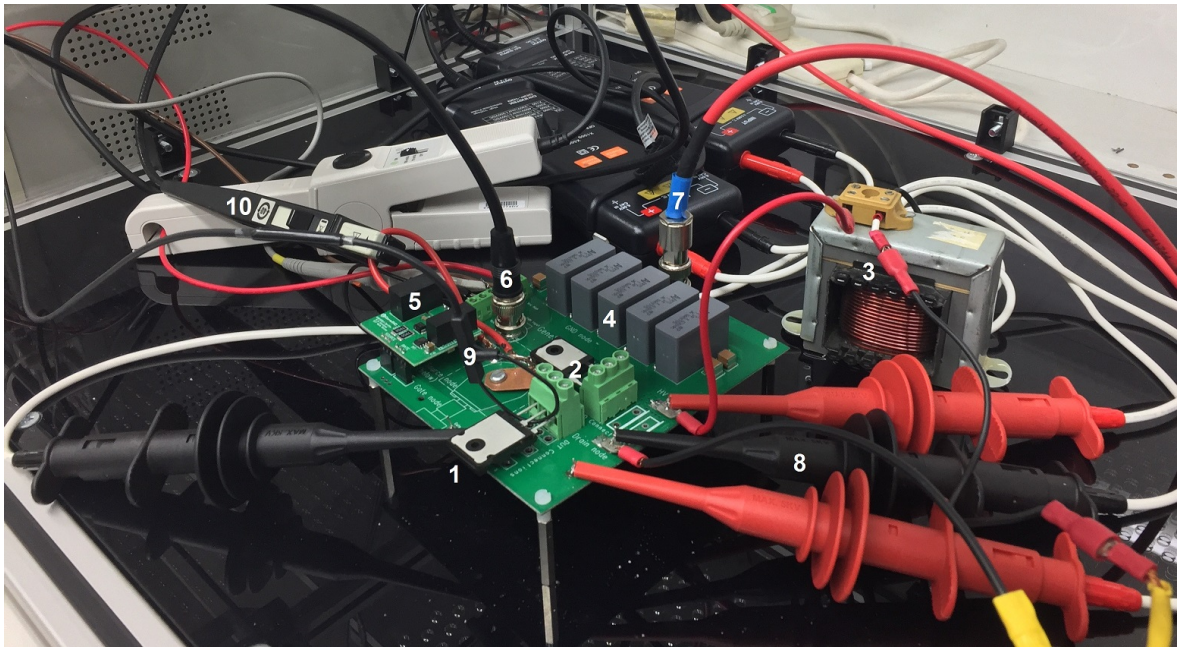

Figure 3.2: Components on the test board: 1- BJTs, 2- Schottky Diode, 3- Load Inductor, 4- DC Capacitors, 5- BJT Base Driver, 6- Input Signal, 7- HV power supply, 8- Voltage Probes, 9- Rogowski Coil and 10- Current Probe [5].

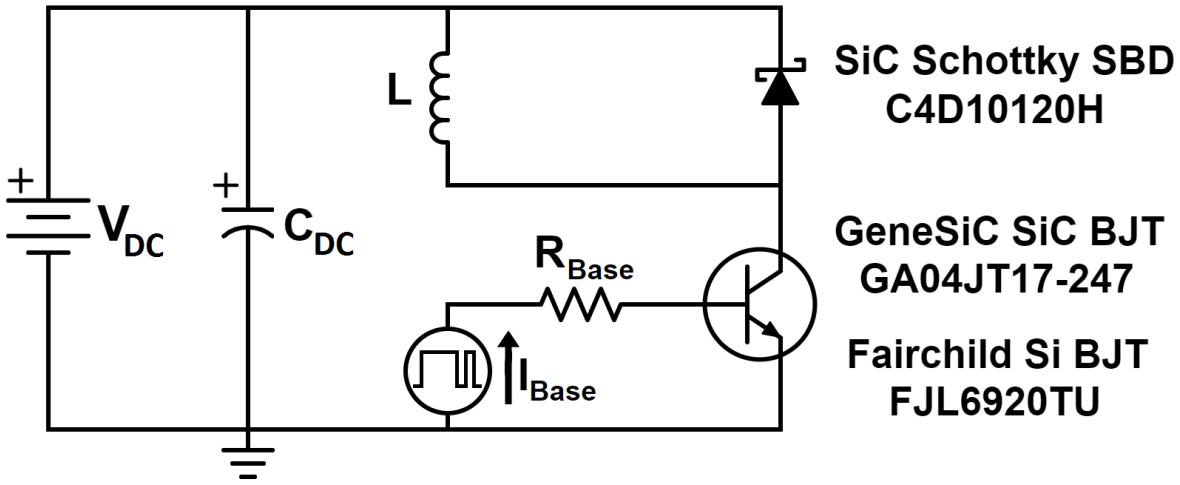

Figure 3.3: Circuit diagram of double-pulse board for single device tests [5].

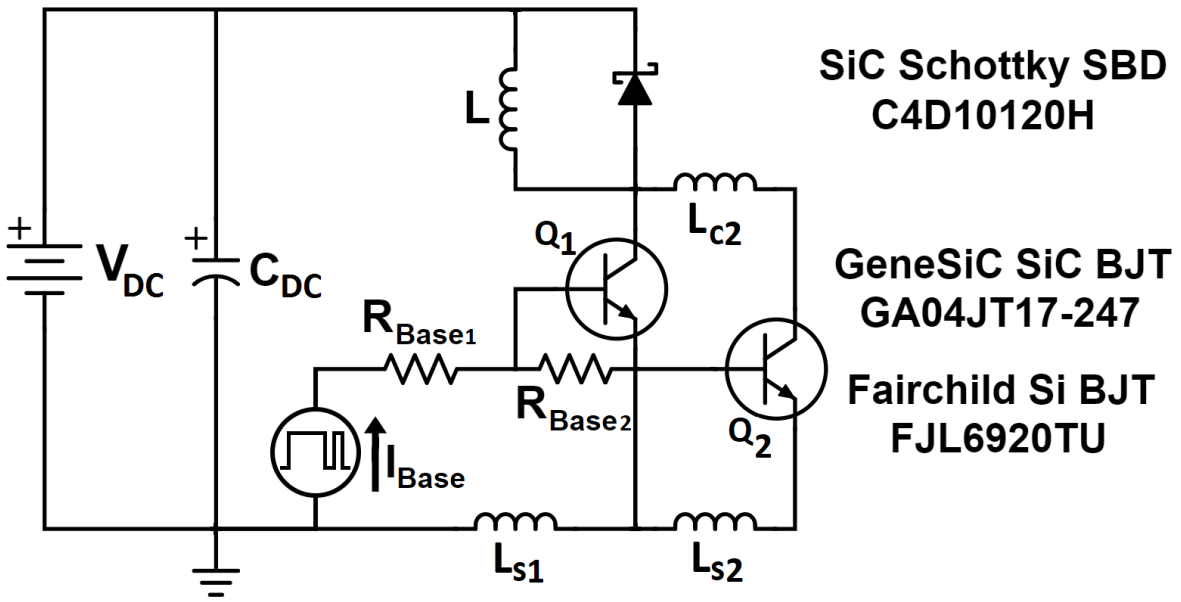

Figure 3.4: Circuit diagram of the double-pulse board for paralleled devices tests, indicating the additional parasitic components on the test circuits.

The dynamic performance of two paralleled BJTs is also experimentally analyzed. The measurements of single devices are done using the set-up shown in Fig. 3.3 while the measurements of paralleled devices are done using the set-up shown in Fig. 3.4. A similar circuit model is designed in LTSpice to model switching transients to confirm the these experimental results.

3.1.1 Error Analysis and Calibration

The sources of measurement error were identified and analyzed to ensure the reliability of the results in this chapter. Measurement of the Base current of BJT is achieved using a Tektronix current probe TCP312 connected to a Tektronix current amplifier TCPA300, which is then fed to a Keysight Mixed Signal Oscilloscope MSO7104A. Current measurement for the Collector current of BJT is achieved by using a PEM CWT Ultra-mini

Rogowski Current Coil CWTUM/1/B connected to the same oscilloscope. Two GW INSTEK voltage probes GDP-100 are used to measure the voltage of the load inductor and the collector voltage of BJT, connected to the same oscilloscope. A brief specification of these aforementioned equipments can be found in Appendix C.

In terms of measuring the Base current of BJT, a reading accuracy of ±2.515% is found from the combination of TCP312 and TCPA300. This error of the MSO7104A oscilloscope is ±0.2% full scale. When measuring the Base current with the maximum value of 1 A in this chapter, the overall error is ±0.027 A (±2.72%). In order to measure the Collector current of BJT, a reading accuracy of ±2% is found from the datasheet of Rogowski Current Coil CWTUM/1/B. Therefore, to gauge the collector current of up to 8.5 A, the overall error is ±0.187 A (±2.20%).

In order to gauge the collector voltage of BJT and the voltage of the load inductor, the GW INSTEK voltage probe GDP-100 donates an error of ±2% to the final read-outs. Therefore, the overall error is ±17.63 V (±2.20%) for collector and load voltage of up to 800 V.

To ensure precise results, it is necessary to calibrate and test measurement equipment prior to taking measurements. When conducting high-frequency measurements, it is important to apply certain techniques to remove temporary de-calibration, also known as delay, from the oscilloscope and probes. The most crucial technique is called deskewing. For double-pulse measurements in this chapter, the deskewing of the voltage waveforms and current waveforms are very important to ensure that all waveforms of the oscilloscope are well in-phase. In this case, the waveform of collector voltage is selected as reference. To de-skew the collector voltage waveform and the load voltage waveform, two GW INSTEK voltage probes are connected to the fixed voltage-calibration point of the oscilloscope and the results are shown on the oscilloscope screen. Phase difference of -1.3 ns

is found from the load voltage waveform with respect to the collector voltage, followed by manual deskewing to shift the load voltage waveform to become in-line with that of collector voltage.

To de-skew the base current waveform and the collector current waveform with respect to the collector voltage waveform, voltage and current probes for these waveforms are connected to a pure resistive load, where the applied voltage produces an in-phase current. Phase difference of +4.7 ns to the collector voltage waveform is found from the base current waveform gauged by using the combination of TCP312 and TCPA300 while phase difference of +11.9 ns to the collector voltage waveform is found from the collector current waveform gauged by using Rogowski Current Coil CWTUM/1/B. Then manual deskewing is performed to shift the base current and collector current waveform to become in line with that of collector voltage.

3.1.2 BJTs in Parallel Connection

The charge stored or released from the base determines the switching performance of the BJTs. Gate driver GA03IDDJT30-FR4 generates current peaks to rapidly turn-on/off the device while maintaining a low on-state base current to minimize the driver losses. The key factors to consider when paralleling BJTs are [88]:

1. Differences in the device parameters.
2. Differences in position within the circuit layout.
3. Differences between the base drivers connected.

Here, to eliminate the mismatch from multiple drivers the same base driver is used. The difference in the electrical parameters such as the DC current gain and the amount of stored charge may also cause the imbalance of output current. The circuit layout [88] also

affects the switching performance of the paralleled devices, so the additional parasitic elements must be considered. To turn-on the transistor, a positive base current pulse is required to rapidly develop the stored charge in the base region and forward bias the base-emitter junction. After the BJTs are turned-on, the base-emitter junction is forward biased whilst the injection of electrons from the base-emitter junction to the base-collector junction starts. The base current is reduced to the steady-state value. For device Q1 from Fig. 3.4, this can be written as Eq. 3.2 [85]:

$$I_{Base1,Steady} = \frac{V_{GL} - V_D - V_{BE,sat}}{R_{Base} + 0.6\ \Omega} \tag{3.2}$$

where V_{GL} is the drive voltage (5V) at the steady state, V_D is the Schottky diode voltage drop (about 0.3 V), $V_{BE,sat}$ is the saturation voltage of the base-emitter junction (about 1.5 V for Silicon BJT and 3.45 V for SiC BJT at operating temperature of 25°C) and 0.6 Ω is added to consider the resistance of the components on the base driver. The steady base current for the other BJT, Q2, can be written as Eq. 3.3:

$$I_{Base2,Steady} = \frac{V_{GL} - V_D - V_{BE,sat}}{R_{Base} + 0.6\ \Omega + R_{Base2}} \tag{3.3}$$

where R_{Base2} is the extra base resistance between Q1 and Q2 on the base loop as shown in Fig. 3.4. The extra base resistance added to the second device decreases the base current and thus increase the device on-resistance, this leads to the mismatch of collector current between paralleled BJTs. The extra parasitic inductance L_{s2} can increase the rise time of the current pulse during both the turn-on transition and turn-off transition.

3.2 Result Analysis

3.2.1 Single BJTs

Fig. 3.5 shows the double-pulse test result in two different base resistances and temperatures at 800 V with the preset pulse length t_{Q1} of 40 μs. It is noteworthy that some of the results of the SiC BJT for the case of 175°C are not included since it failed when temperature rises above 150°C. The Silicon BJT, on the other hand, worked well until the charging pulse length exceeds 40 μs at 175°C. Therefore, during single device measurements and due to the risk of damages in high temperatures and high currents, the temperature is restricted to up to 150°C with a pulse length of up to 35 μs to avoid failures.

Fig. 3.5(A) shows a period of delay between the base turn-off and the collector current drop in Silicon BJT, which increases with the rise of temperature. This is because the diffusion coefficient is inversely proportional to temperature, leading to an increase of storage(delay) time as expected by Eq. 2.7 and 2.24. The base current is constant in steady-state. The delay time slightly decreased in Fig. 3.5 (B) since the stored charge is reduced by the higher base resistance. In Fig. 3.5 (C), both the base and collector current are turned on and off almost instantaneously for the 4H-SiC BJT, due to the much lower carrier lifetime and the significantly smaller dimensions enabling the decrease of the storage time. However, the collapse of collector current is observed. This can be explained by the reduction of current gain at high collector currents in SiC BJT [87]. Such current drop is observed to worsen by increase the base resistance as shown in Fig. 3.5 (D), which leads to the increase of collector voltage via the load inductor and thus incur significant power dissipation. This explains the failure of SiC BJT during the double-pulse test.

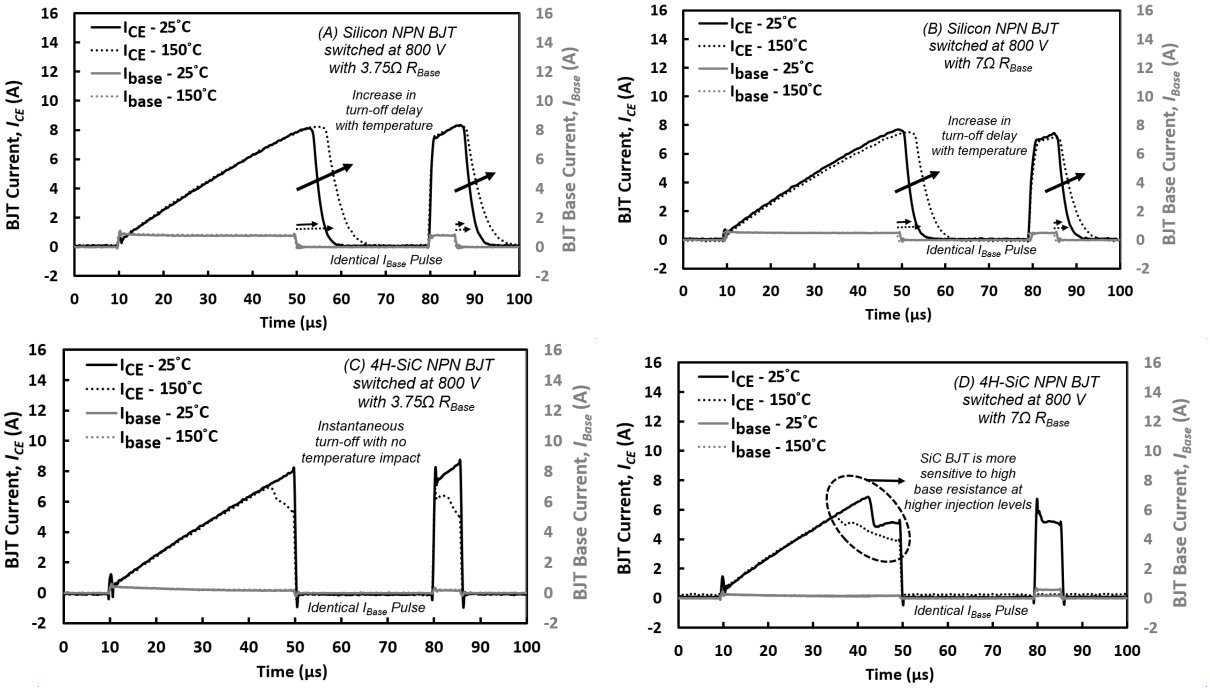

Figure 3.5: Double pulse test results of the collector and base current for Silicon BJT with R_B of (A) 3.75 Ω and (B) 7 Ω and for SiC BJT with R_B of (C) 3.75 Ω and (D) 7 Ω indicating the temperature-dependent delay under the same base current.

Fig. 3.6 shows the double-pulse test result with respect to different collector currents at 800 V when T=150°C. The t_{Q1} applied in this case is 5 μs and 40 μs separately, all other parameters are same for a fair comparison. For the case of pulse length of 5 μs, this delay is indicated by the solid line arrow while the dotted line arrow is used for the pulse length of 40 μ. The average delay time is 15 μs for the Silicon BJT which inhibits its function, especially at high frequency as extra power losses are caused by the prolonged collector current, which was also shown in Fig. 3.5 (A) and (B). The decrease of delay time at long pulses (high collector currents) can be contributed to the decrease of the conductivity-modulated region (W_{NM}). This is expected in line with Eq. 2.24 and Eq. 2.29.

Fig. 3.7 shows the delay time under various temperatures and collector currents. A

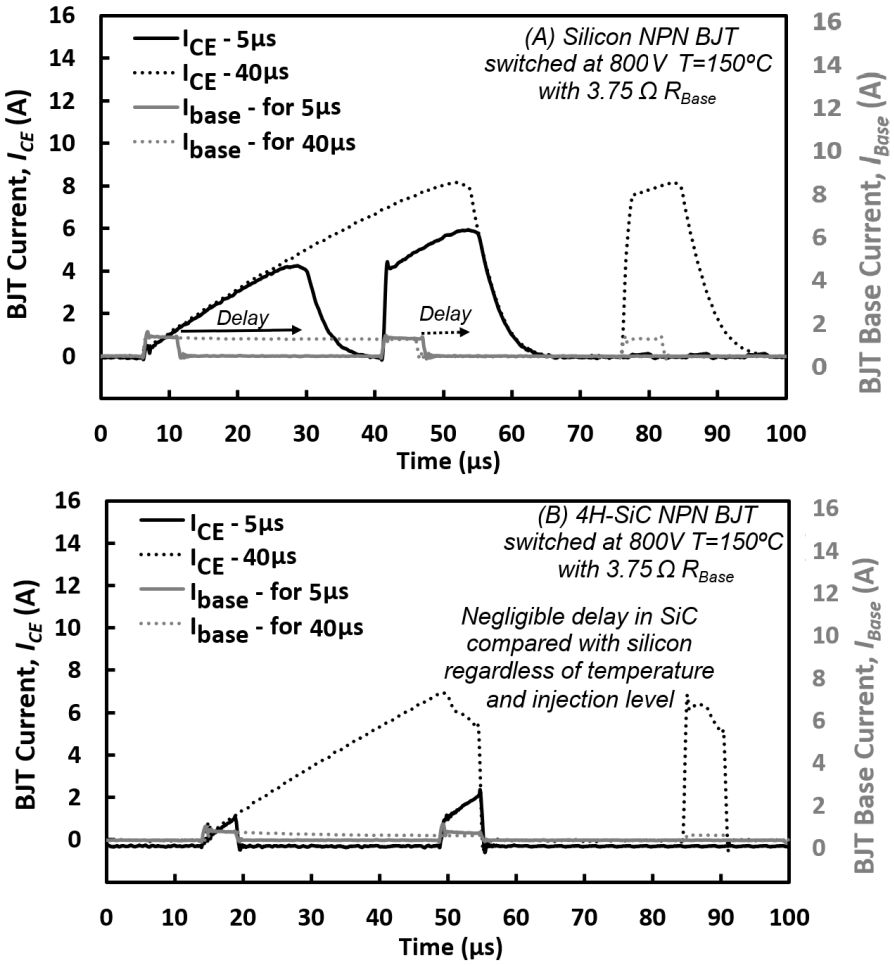

Figure 3.6: Double pulse test results regarding the collector and base current at 150°C for (A) Silicon and (B) 4H-SiC BJT, with R_{base} of 3.75 Ω to analyze the turn-OFF delay with respect to different collector currents under the same amplitude of base current.

significant delay can be seen during the switching transition of the Silicon device with the average value of 10 μs while the turn-off delay in SiC device is about two orders of magnitude smaller, thanks to the much smaller base width in SiC BJT. The delay increases at elevated temperatures because the diffusion constant of electrons (D_n) decreases with increasing temperature as in Eq. 2.7. It is shown in Fig. 3.7 that at higher currents, due to the smaller W_{NM}, the delay is reduced in-line with Eq. 2.24.

The collector current at turn-on and turn-off transients are shown in Fig. 3.8 and

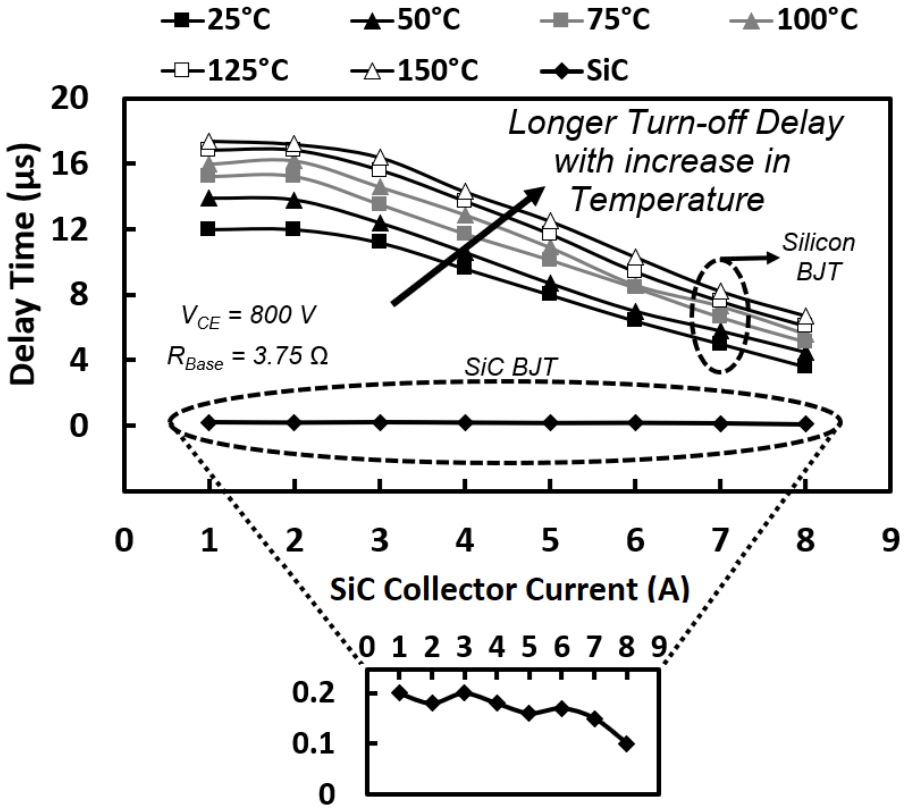

Figure 3.7: The turn-OFF storage time is much longer in Silicon BJT with significant temperature dependence and current dependence, whereas this value is negligible in the SiC BJT. The rise of collector from 1 A to 8 A corresponding to the increase of pulse length from 5 μs to 40 μs.

Fig. 3.9 for both Silicon and SiC BJT. The turn-off delay is previously shown to get worse at elevated temperatures, which will in turn lead to the increased the collector current. When comparing Fig. 3.8 (A) and Fig. 3.8 (B), the much smaller W_B can be seen to play a significant role to reduce the t_{Ion} for the SiC BJT in-line with Eq. 2.21, while the increase of turn-ON period is expected by the decreasing of the diffusion coefficient at high temperatures as in Eq. 2.6, so the longer t_{Ion} is seen at higher temperatures as shown in Fig. 3.8 (B). The increase of temperature also impacts the turn-OFF transients as shown in Fig. 3.9 (B). This is because of the increased carrier lifetime, and the lower diffusion coefficient which leads to a larger t_{I-off}, whereas the t_{I-off} is always lower for

the SiC device because of the much lower carrier lifetime and the smaller dimensions of the die.

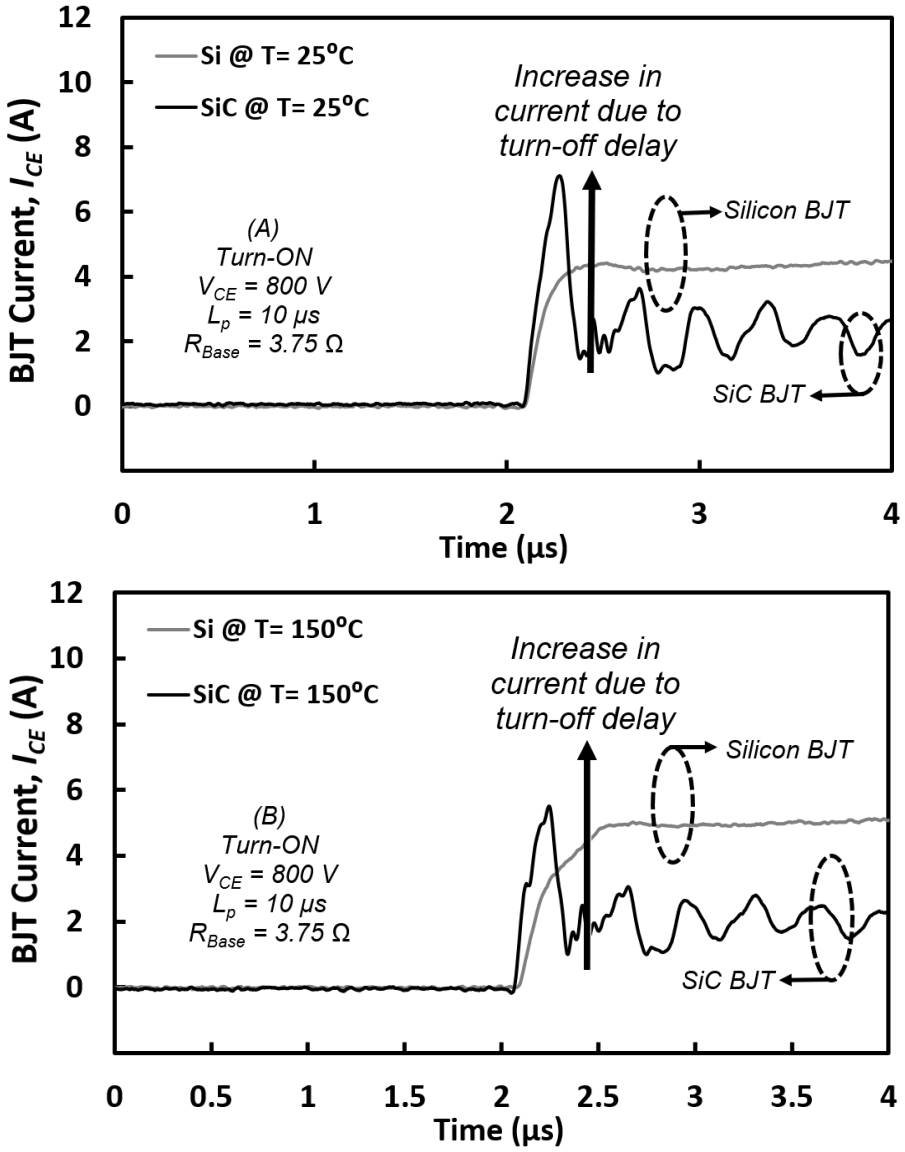

Figure 3.8: Turn-on transient of Silicon and 4H-SiC BJT with pulse length of 10 μs with at (A) 25°C and (B) 150°C for the BJT collector current.

The temperature dependence of switching transients can also be seen in Fig. 3.10 and Fig. 3.11 for a wide range of temperatures for the Silicon and 4H-SiC BJT. The

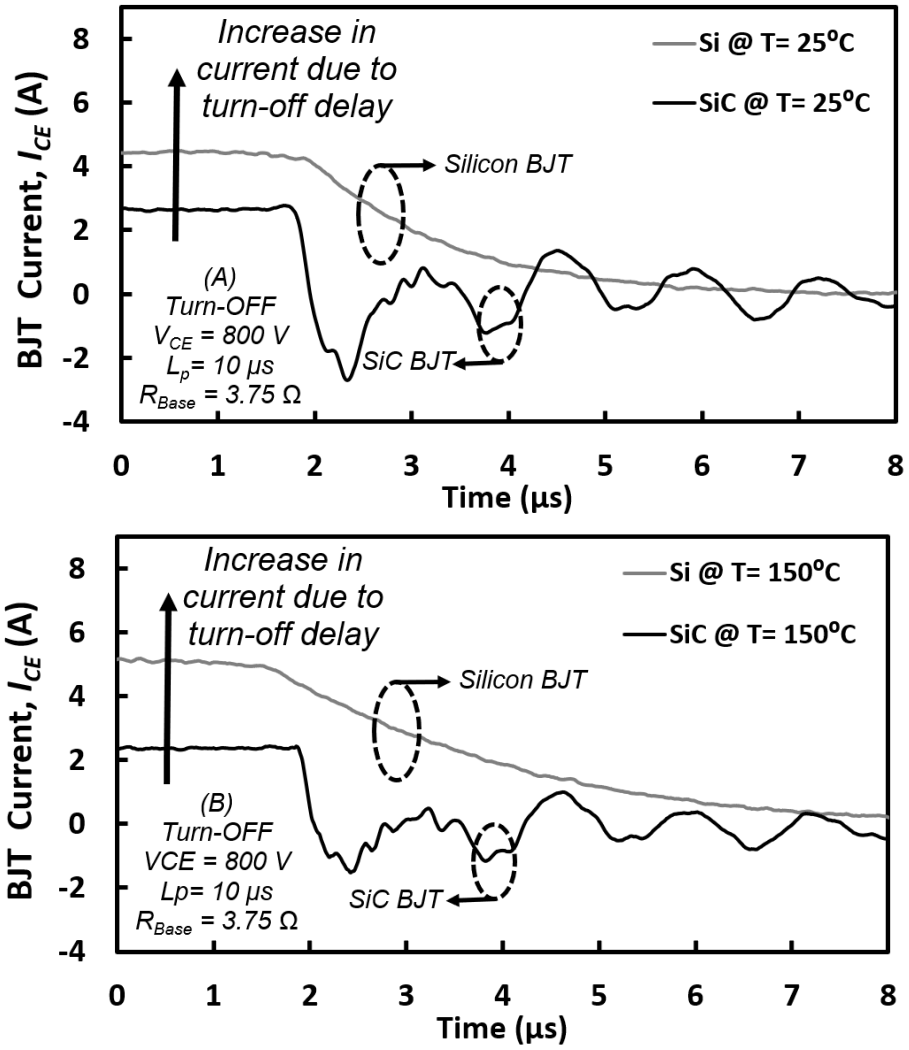

Figure 3.9: Turn-off transient of Silicon and 4H-SiC BJT with pulse length of 10 μs with at (A) 25°C and (B) 150°C for the BJT collector current.

t_{I-on} of Silicon BJT in Fig. 3.10 (A) is found to increase with increasing temperature because of the negative temperature dependence of the diffusion coefficient. At the turn-off transition in Fig. 3.11 (A), collector current increases with the increase of turn-off delay which also makes t_{I-off} larger. The turn-Off transient of the SiC BJT, however, is almost temperature-invariant as was the case of the turn-on transient.

SiC BJT has faster voltage transients in Fig. 3.12 and Fig. 3.13 as predicted by the

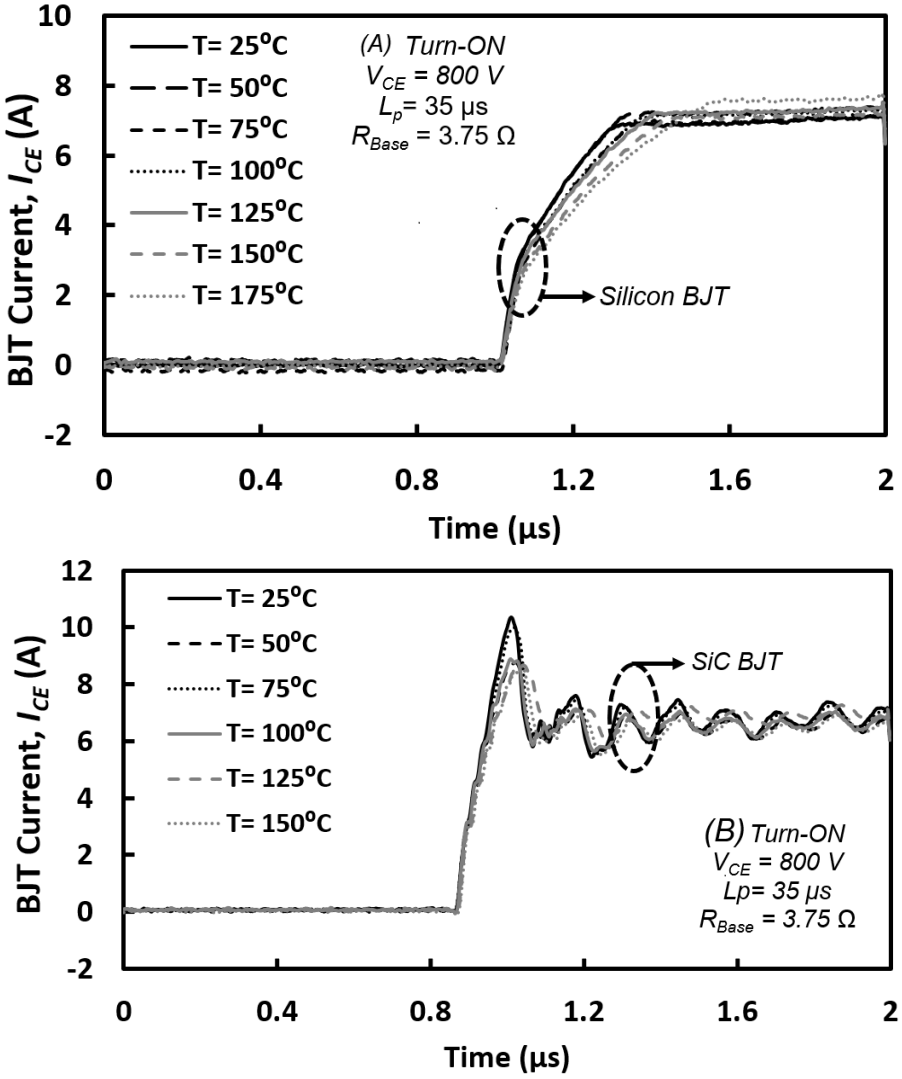

Figure 3.10: Turn-on transient with pulse length of 35 μs for the (A) Silicon and (B) 4H-SiC BJT, for collector current at all temperatures.

models. At turn-on transients in Fig. 3.12, the temperature-dependent diffusion coefficient decreases the J_C as in Eq. 2.23, leading to the prolonged voltage turn-on period (t_{von}) as in Eq. 2.22, resulting in the slower transient in Fig. 3.12 (B). The lower collector voltage in Silicon BJT is mainly because of the larger collector current consume the electrical energy stored in the bank capacitor C_{DC} which cannot maintain high DC link voltage as that of SiC BJT.

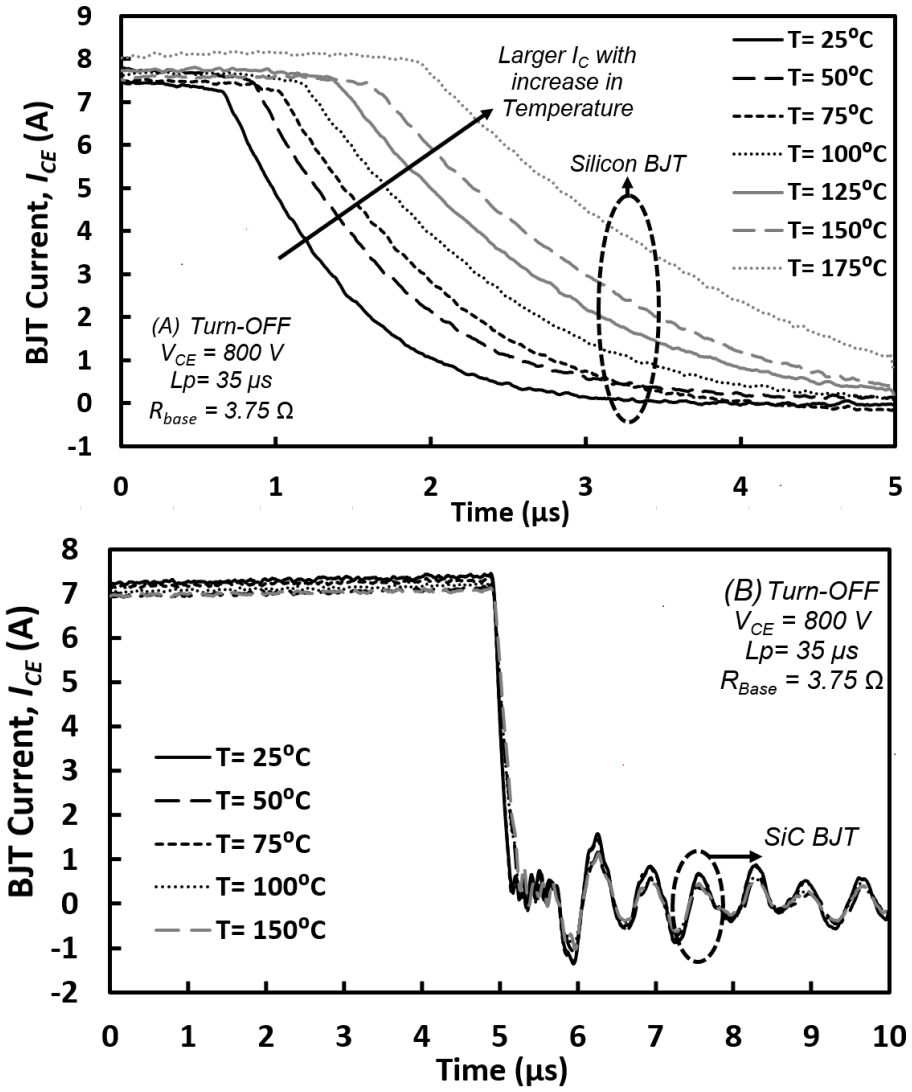

Figure 3.11: Turn-Off transient with pulse length of 35 μs for the (A) Silicon and (B) 4H-SiC BJT, for collector current at all temperatures.

At turn-off transients shown in Fig. 3.13 (A) and (B), turn-OFF process of the voltage is slower at high temperatures because of the temperature-dependent diffusion coefficient which increases the value of the voltage turn-OFF phase ($t_{v\text{-}off}$) as in Eq. 2.26. The lower collector voltage in Silicon BJT can be explained by the loss in energy in capacitor bank. However, the collector voltage starts to increase earlier before the collector current starts

to drop and thus Silicon BJT undergoes high power dissipation during this period. This does not hold true for SiC BJT with negligible turn-off delay.

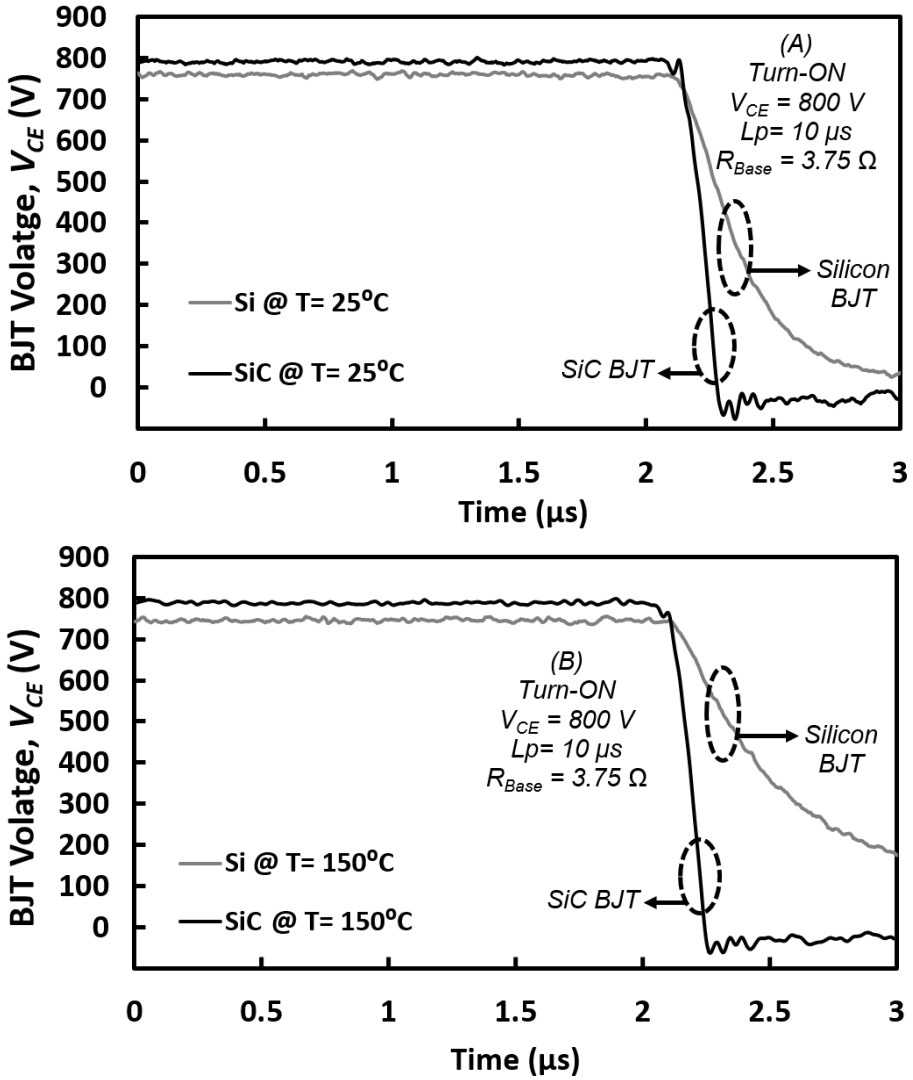

Figure 3.12: Turn-on transient of Silicon and 4H-SiC BJT with pulse lengths of 10 μs at (A) 25°C and (B) 150°C for BJT collector voltage.

The switching waveform of base current for both BJTs during turn-off and turn-on are shown in Fig. 3.14 and 3.15. Both the positive and negative current pulse is observed to accelerate the turn-on transition and turn-off transition of BJT, respectively. The

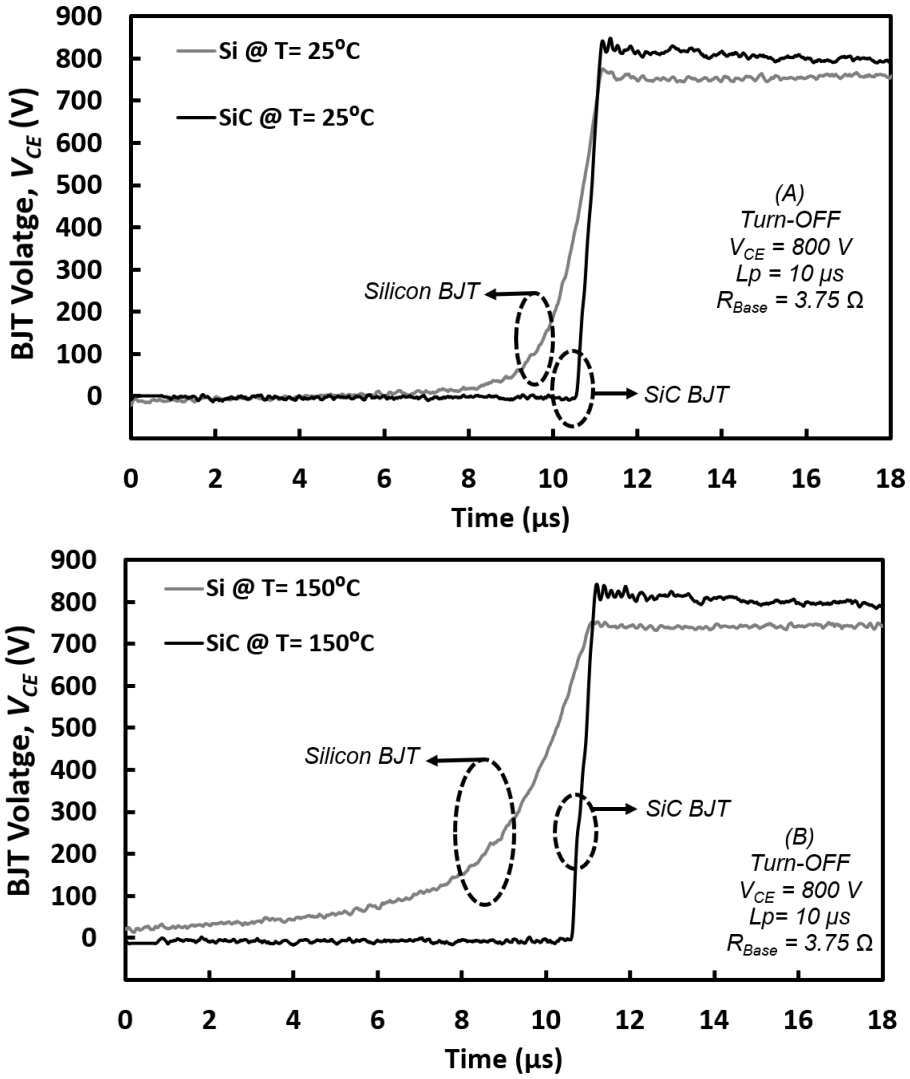

Figure 3.13: Turn-off transient of Silicon and 4H-SiC BJT with pulse lengths of 10 μs at (A) 25°C and (B) 150°C for BJT collector voltage.

lower steady base current and pulsed base current in SiC BJT is attributed to the much larger base-emitter saturation voltage $V_{BE,sat}$, which is expected in line with Eq. 3.2. The resonance between the large base capacitance and the stray inductance in the gate loop causes significant oscillation in the base current for Silicon BJT. This is mitigated by the smaller parasitic capacitor because of the smaller device dimensions in SiC BJT [5].

The time taken to turn-on and turn-off for different collector currents (pulse lengths)

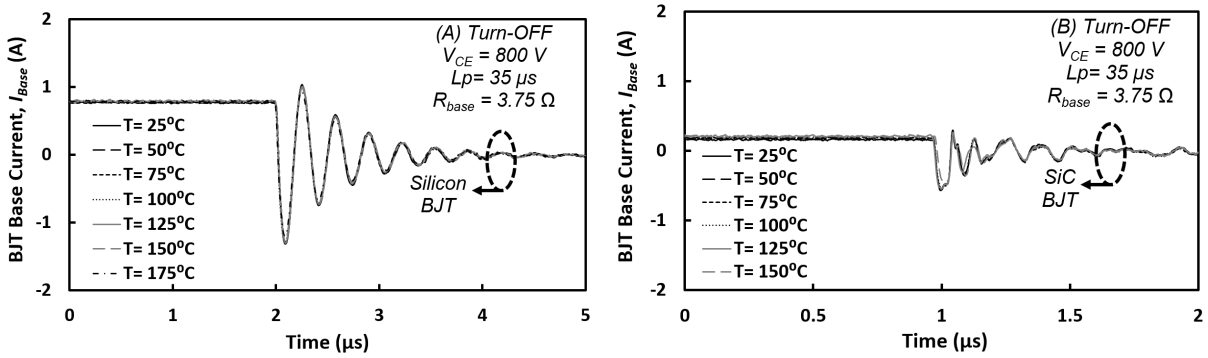

Figure 3.14: Turn-off transient for the (A) Silicon and (B) 4H-SiC BJT for base current at all temperatures.

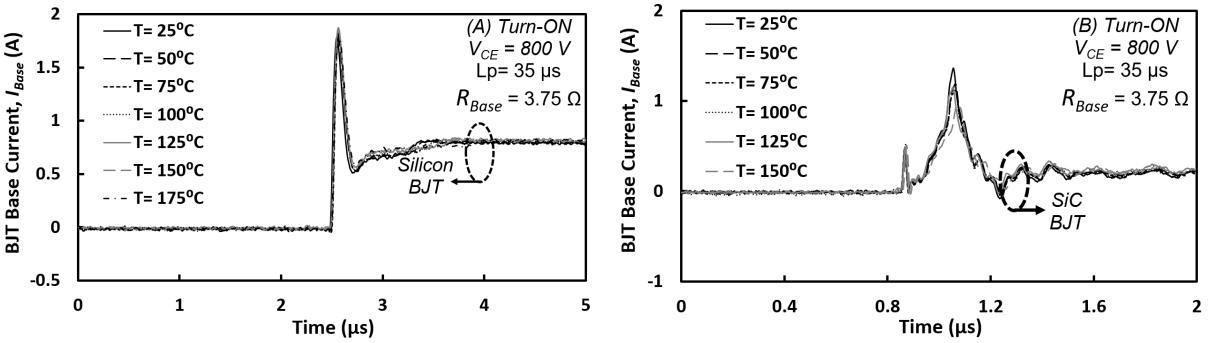

Figure 3.15: Turn-on transient for the (A) Silicon and (B) 4H-SiC BJT for base current at all temperatures.

are shown in the Table. 3.4 for both the Silicon and SiC NPN BJTs. At the turn-on transient, the $t_{transit}$ as in Eq. 2.20 of the Silicon BJT is increased with increase of the collector current as a result of the decreased diffusion constant of electrons (D_n) in high currents. The current turn-on period ($t_{I\text{-}on}$) is also increased for the same reason. The voltage turn-ON period ($t_{V\text{-}on}$), on the other hand, decreases with collector current density (J_C) which as per Eq. 2.22 is the most dominant component to reduce the total turn-ON time at high collector currents. A faster turn-on for the SiC BJT is predicted due to the significantly smaller dimensions of the base and drift region.

At the turn-off transient, the voltage turn-OFF period ($t_{V\text{-}off}$) of the Silicon BJT increases as the holes diffusion coefficient D_p is decreased at high currents as per Eq. 2.26.

The current turn-off period ($t_{I\text{-}off}$) also increases because the decrease in D_n is dominant. Nevertheless, the increase in these two terms is compensated by the reduction of charge stored period at turn-off (t_S), as the decreased width of conductivity modulated region (W_{NM}) is more significant compared to the drop of D_n to reduce the total turn-Off time at high collector currents. These trends hold true for the SiC BJT at turn-OFF, while the much smaller width of the base (W_B) and storage region (W_S) contributes to a reduction of the turn-off time by an order of magnitude when compared to that in Silicon BJT. It is seen that the t_S is much larger than the $t_{transit}$ since the charge depletion phase removes more carriers than those built initially.

Table 3.4: Measured switching time of Silicon and 4H-SiC NPN BJT during different phases at $T = 25$°C with $R_{Base} = 3.75\ \Omega$. N.B.: 'Stored Charge' at Turn-ON is the transit time ($t_{transit}$) while 'Stored Charge' at Turn-OFF is the storage time (t_S).

	Turn-ON		Turn-OFF	
	Silicon	SiC	Silicon	SiC
Stored Charge at 10 μs	0.4 μs	0.06 μs	12 μs	1.2 μs
Stored Charge at 40 μs	0.44 μs	0.05 μs	4.3 μs	0.09 μs
Current Transient at 10 μs	0.405 μs	0.132 μs	4.8 μs	0.104 μs
Current Transient at 40 μs	0.415 μs	0.130 μs	5.12 μs	0.106 μs
Voltage Transient at 10 μs	1.97 μs	0.3 μs	3.6 μs	0.7 μs
Voltage Transient at 40 μs	1.38 μs	0.28 μs	4.0 μs	0.75 μs

As for the comparison between the simulation and measurement results in Fig. 3.16, all the simulation results are denoted as 'Sim', e.g. 'SiC Sim @ T = 25°C' is the line of simulation. With the identical I_{base} pulse, the results of Fig. 3.8 and Fig. 3.9 match well with results of the simulations in Fig. 3.16. Although there is some error about modeling

of the oscillations by the LTSpice, the *dI/dt* is found to be a good match in the model. It can be seen that although the frequency of oscillations in the SiC measurements are higher than what is predicted by the simulations, the slew rates in all case of simulations are close to that of the measurements, indicting that the modelling approached commonly used for the Silicon BJTs can be applicable to the case of high voltage SiC BJTs as well.

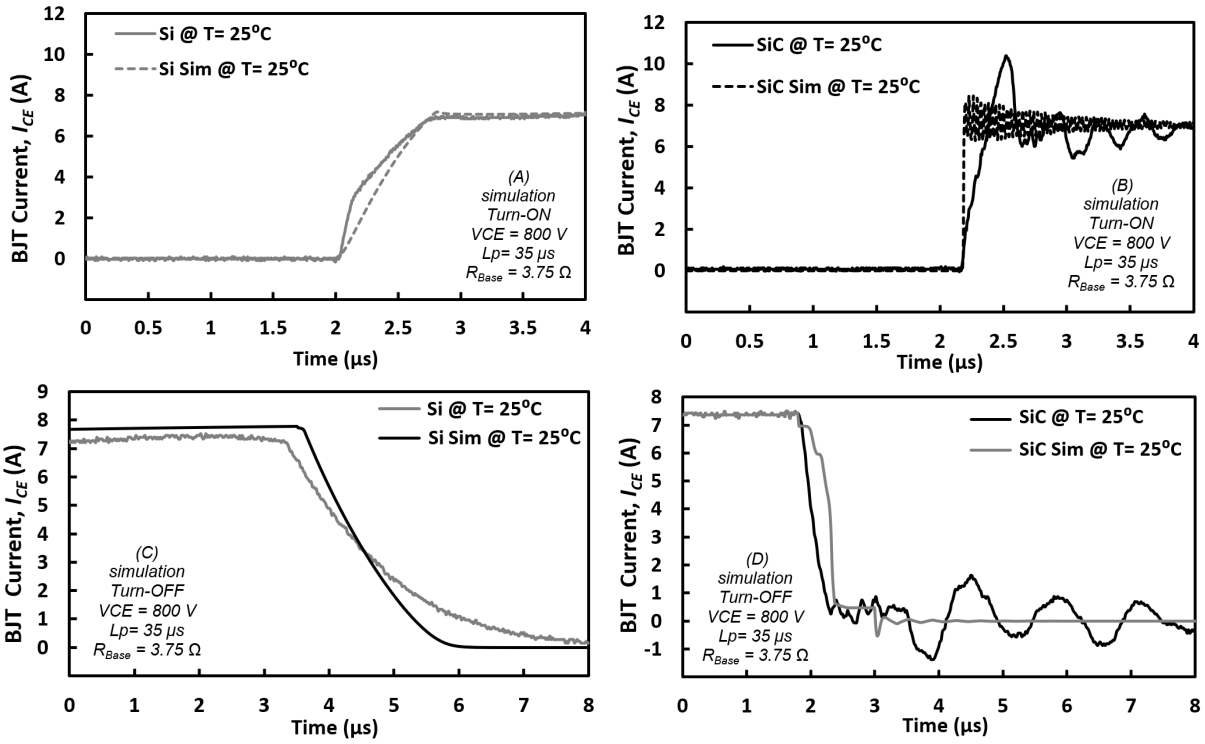

Figure 3.16: Simulation results for the measurements shown in Fig. 3.8 and 3.9 for turn-ON transients of (A) Silicon and (B) SiC BJT and turn-OFF transients for (C) Silicon and (D) SiC BJT, to evaluate the validity of the models.

The switching performance of the two device technologies indicate that the SiC device has a significant edge in terms of the switching rate over all temperatures, all base resistances and all collector current levels, while the numerical indications of the provided simulations have reconfirmed this advantage. To investigate the impact of temperature and collector current on switching energy, it is calculated for both the turn-on and turn-off

transients by integrating the transient power over its period as Eq. 3.4:

$$E_{Switching} = \int_{t_1}^{t_2} I_C(t) \cdot V_C(t) dt \tag{3.4}$$

The energy loss for turn-off is assessed in the time interval between 10% of the rising collector voltage and 10% of the dropping collector current. The energy loss for turn-on is assessed in the time interval between 10% of the rising collector current and the 10% of the dropping collector voltage. As can be seen in Fig 3.17, the switching losses by the SiC device are one to two orders of magnitude smaller at both turn-on and turn-o transients, while the switching energy in both Silicon and SiC device increases with temperature as expected by the transient waveforms in Fig 3.10-3.11 for the current transients and Fig. 3.12-3.13 for the voltage transients.

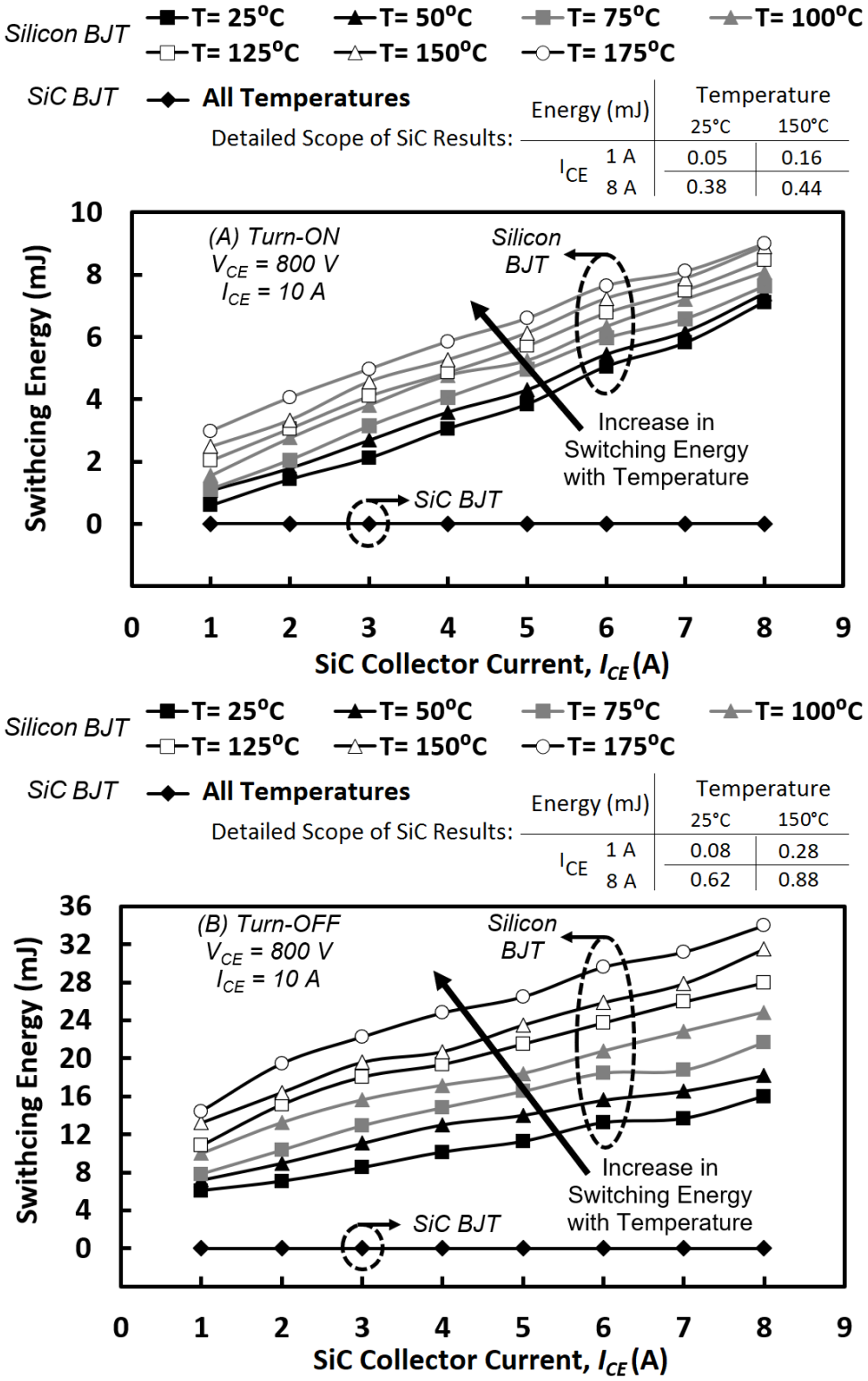

Figure 3.17: Calculated switching energy of Silicon and 4H-SiC BJTs at (A) turn-ON and (B) turn-OFF transients in a range of collector currents. The rise of collector current from 1 A to 8 A corresponding to the increase of pulse length from 5 μs to 40 μs.

The current gain β during double-pulse testing are calculated by taking the maximum collector current within the pulse length (t_{Q1}) divided by the corresponding base current. High collector currents lead to a damping effect on the current gain (β) as the collector current increases as shown in Fig. 3.18. This confirms the theory that as collector current increases the high-level-injection effect (Webster) will eventually saturates the current gain [1, 2]. In regard to trends with temperature, as in Fig. 3.18, the current gain of Silicon BJT is found to increase with temperature at low collector current($\leq$4 A). If the collector current continues to increase (>4 A), the DC current gain is limited primarily by the onset of high-level-injection (Webster effect). With the increase of temperature at high collector currents, the lower diffusion coefficient in Eq. 2.6 leads to the fall of J_W in Eq. 2.33 and thus shifts the boundary of the high-level injection to lower current levels. Similar trend can also be seen at the SiC device, however, at a significantly higher DC gain.

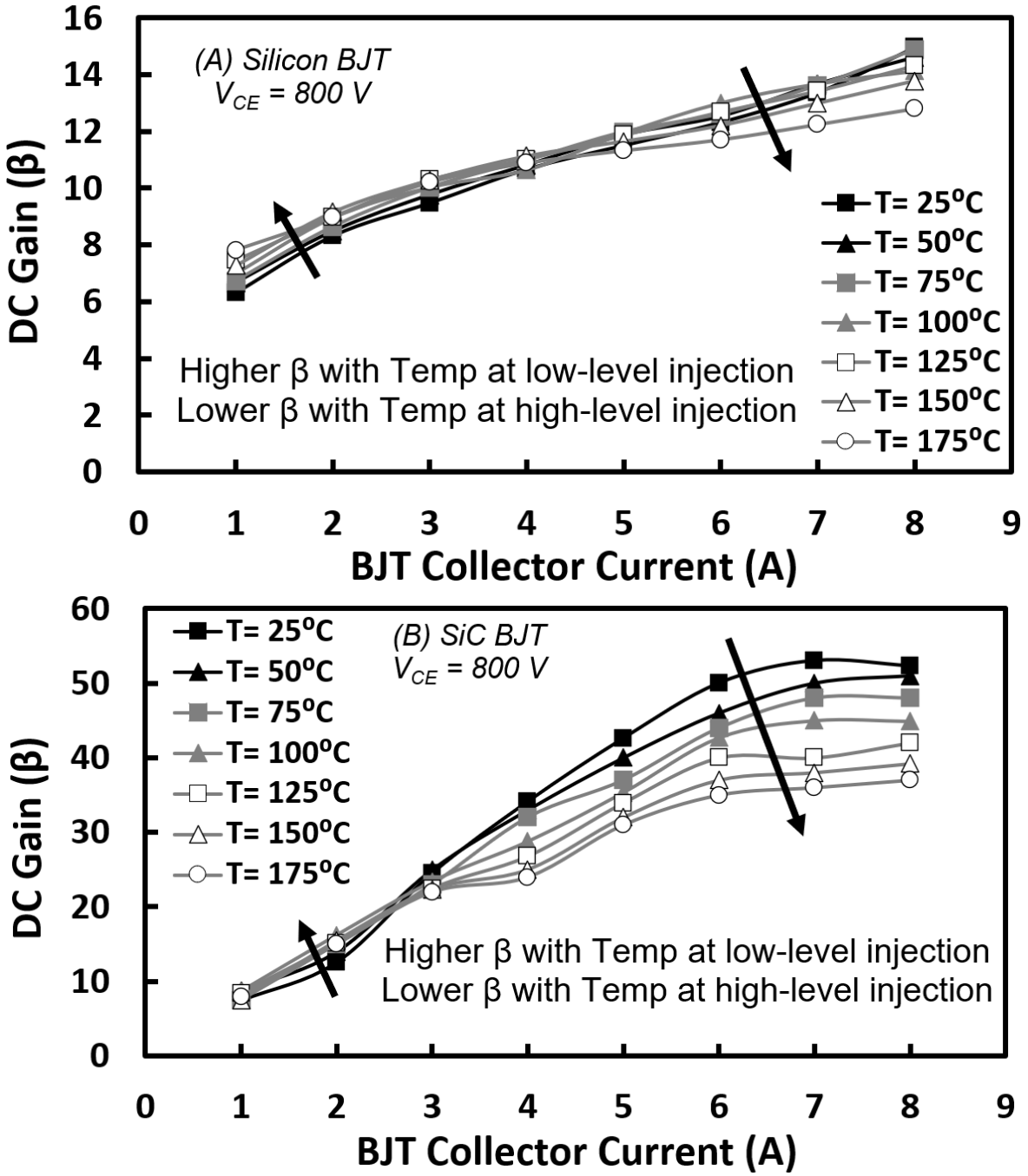

Figure 3.18: The common emitter DC current gain (β) for (A) Silicon and (B) 4H-SiC NPN BJT in a range of collector currents & temperatures, indicating the opposing temperature dependence at high collector currents. The rise of collector current from 1 A to 8 A corresponding to the increase of pulse length from 5 μs to 40 μs.

3.2.2 Paralleled BJTs

As for the dynamic performance of paralleled BJTs, the current imbalance among paralleled BJTs can attributed to the smaller base current in the second device Q2, together with the significant stray inductance in the power loop of Q2 reducing the value of dI/dt as expected by Eq. 3.1. The turn-off delay as in Eq. 2.24 also exists among the paralleled Silicon BJTs. This delay time between paralleled devices deteriorates as temperature rises as seen in Fig. 3.19 (A) leading to the worse current mismatch, while the turn-off delay and current imbalance is less significant when the base resistance increases as in Fig. 3.19 (B) as the charge stored in both the base and drift region reduces. This suggest that turn-Off delay at higher temperatures can be counterbalanced by increasing the base resistance at the cost of slower switching speed. As seen in Fig. 3.20, paralleled SiC devices do not exhibit turn-OFF delay which is evident in Silicon devices in Fig. 3.19. Although the sudden drop of collector current is also observed, this is not observed at the same base resistance when compared with that in Fig. 3.19. Additionally, the failure of SiC BJTs is not observed at high temperatures and high collector currents.

Fig. 3.21 shows the trend of turn-OFF delay in single discrete and paralleled Silicon BJTs with temperature with first pulse length of 40 μs, where it can be seen that paralleled BJTs exhibit a longer delay period compared to single devices with both base resistances. The turn-OFF delay increases with temperature due to the increase of the minority carriers lifetime with temperature in Silicon as in Eq. 2.11, while in SiC the low minority carrier lifetime means there is effectively no turn-OFF delay which would be dependant on temperature.

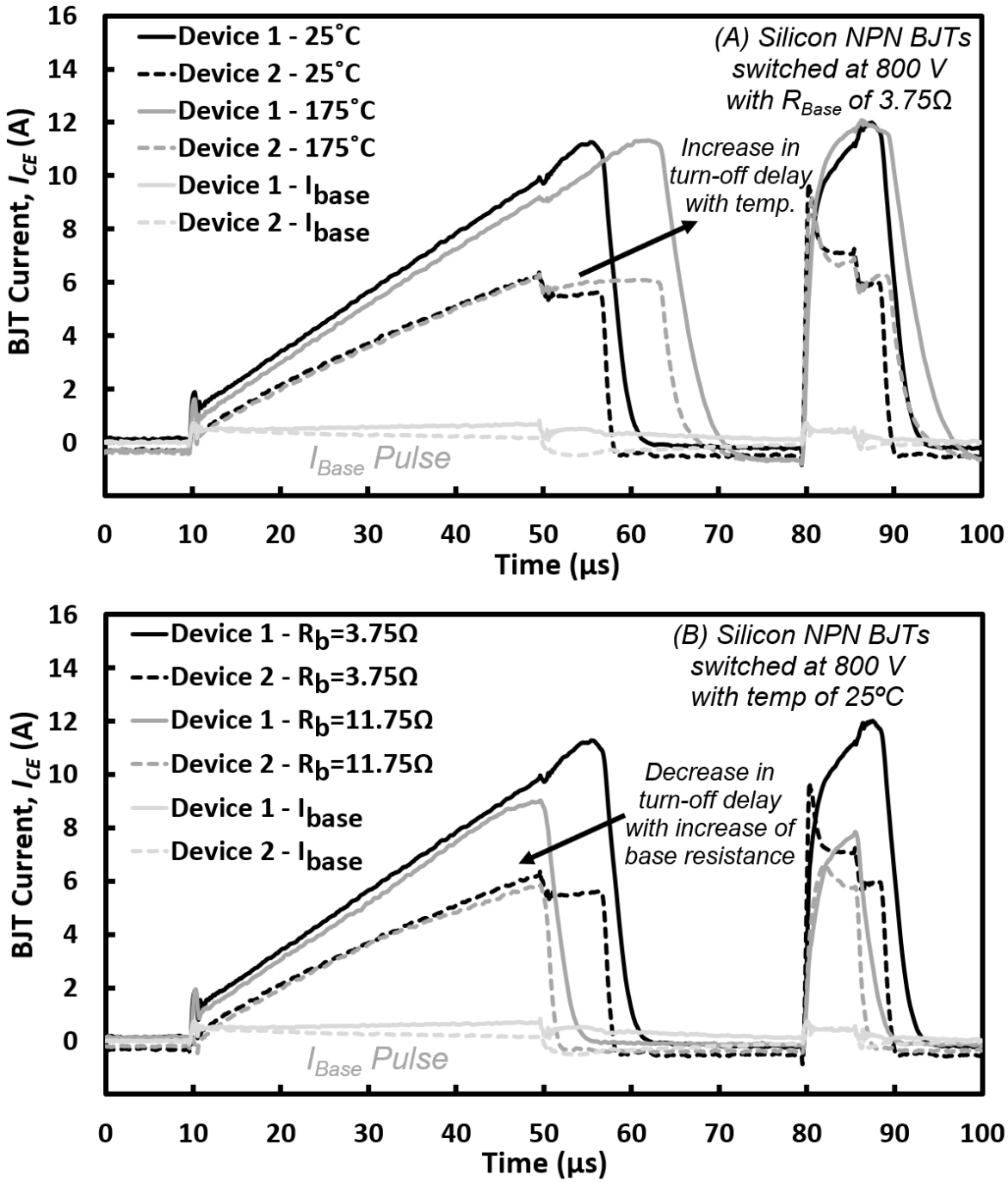

Figure 3.19: The trends of turn-OFF delay and current imbalance in paralleled Silicon BJTs with (a) temperature and (b) base resistance.

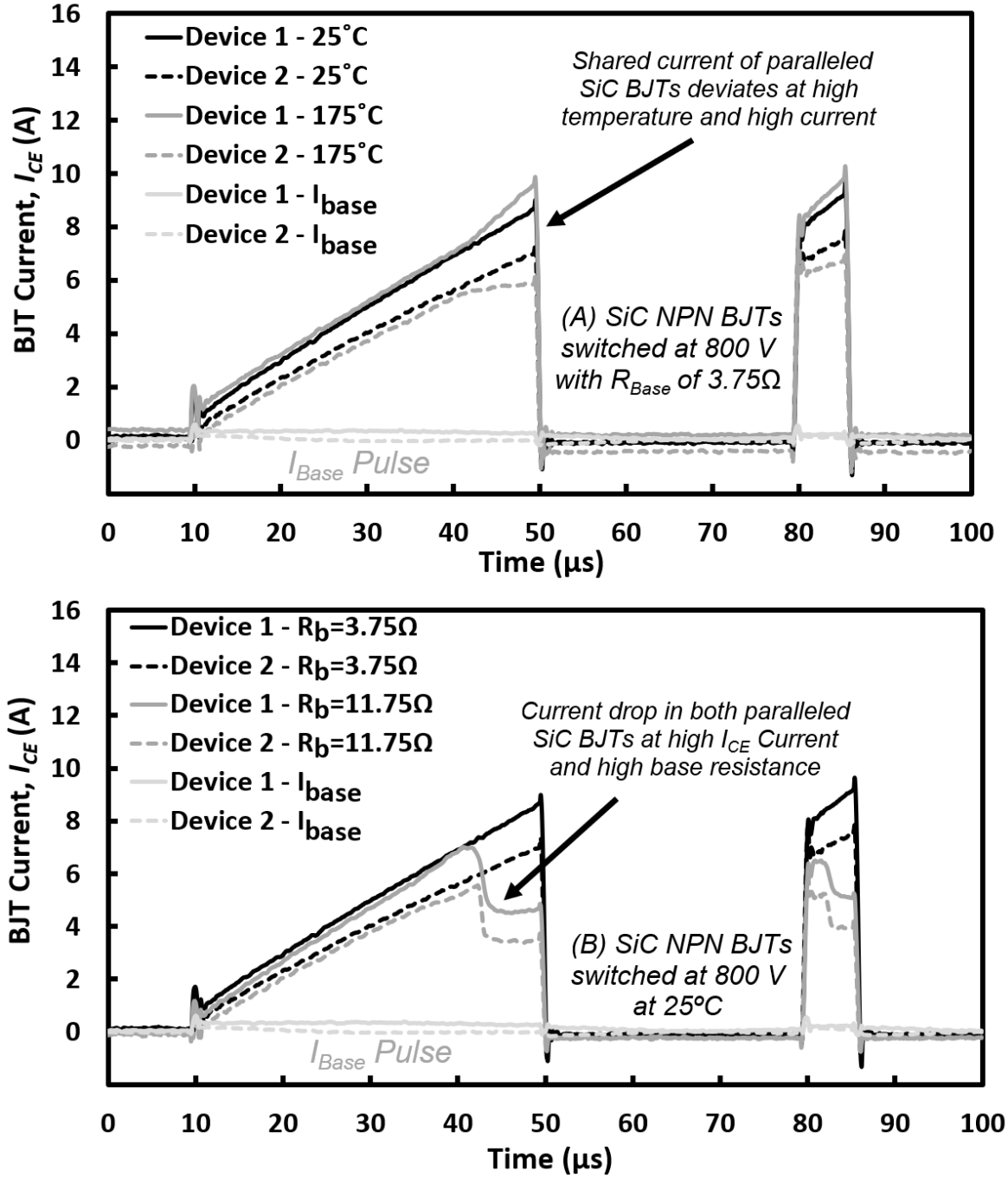

Figure 3.20: The trends of shared current distribution and current collapse in paralleled SiC BJTs, with (a) temperature and (b) base resistance.

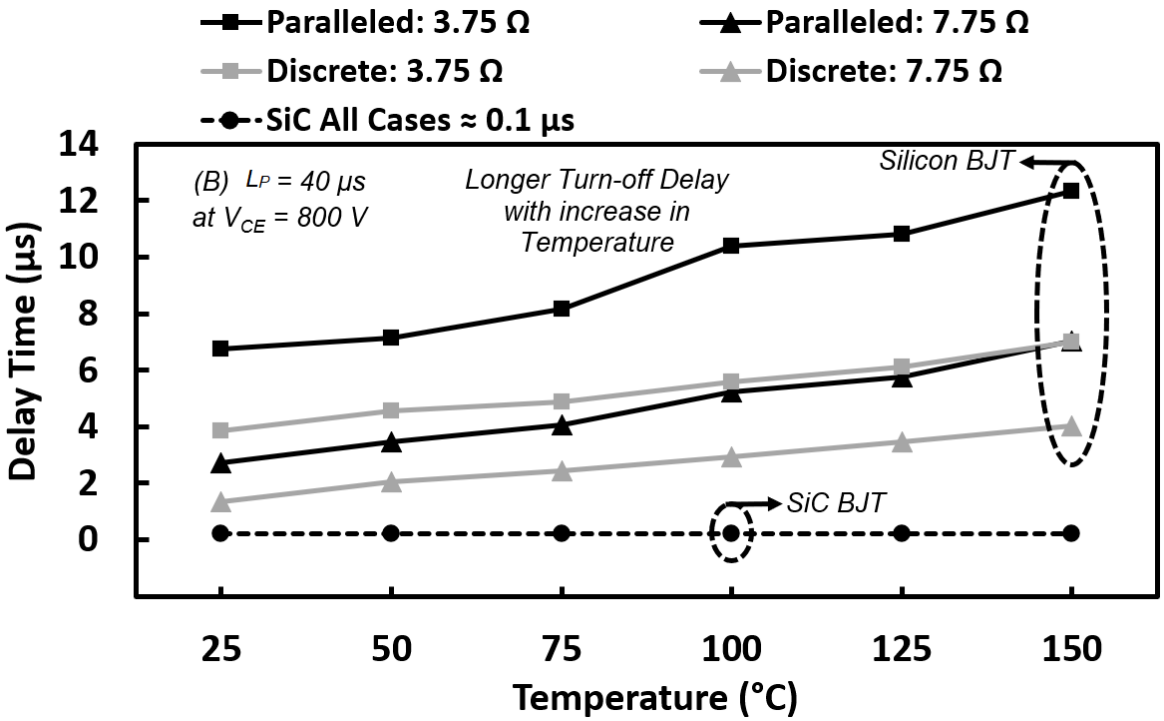

Figure 3.21: Turn-OFF delay comparison between discrete and paralleled Silicon and SiC BJTs when switched at 800 V and 8 A.

The results of the simulations indicate that the model match well with the measurements for both paralleled devices, representing the expected differences in the transient currents. Fig. 3.22 show the case of the two paralleled Silicon BJTs where the substantial current mismatch between the two devices seen in Fig. 3.19 is represented by the simulations, while Fig. 3.23 presents the results of the measurements and simulations of the case of two paralleled SiC BJTs, where the current mismatch, albeit at smaller value due to the absence of the turn-OFF delay [89, 90], is represented by both the measurements and simulations.

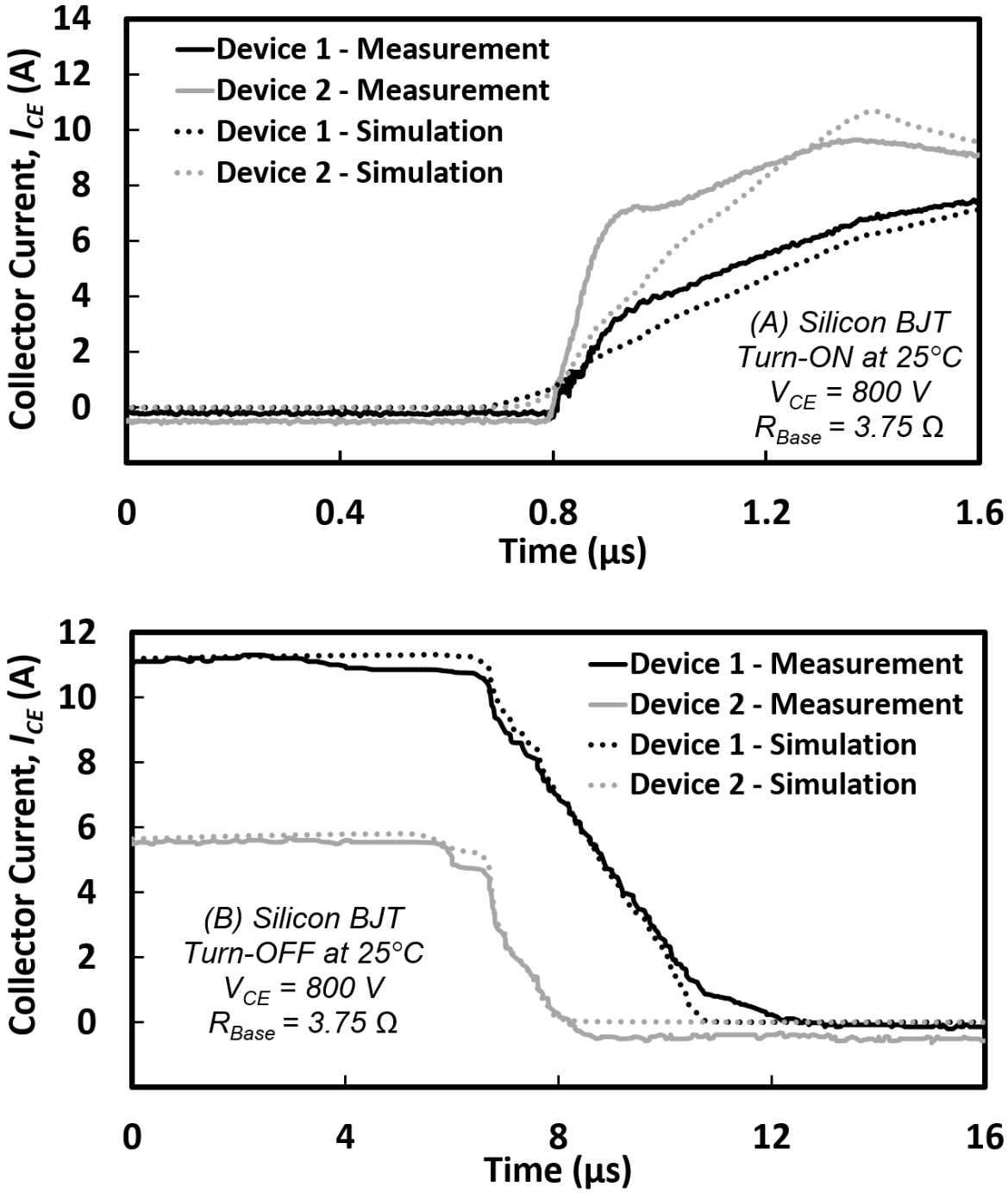

Figure 3.22: The simulations versus measurements of the collector current (A) turn-ON and (B) turn-OFF transients of the paralleled Silicon BJTs at 800 V.

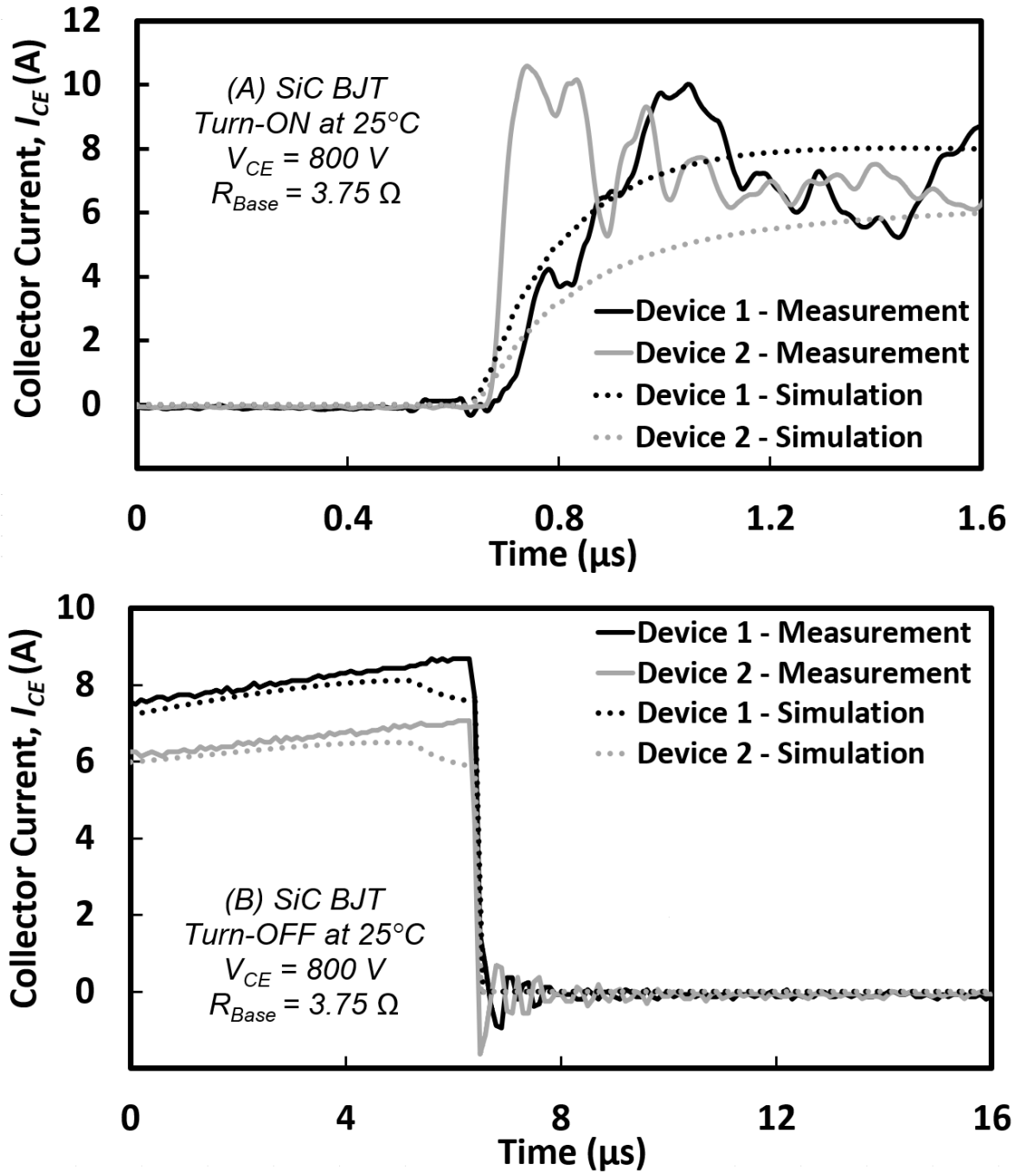

Figure 3.23: The simulations versus measurements of the collector current (A) turn-ON and (B) turn-OFF transients of the paralleled SiC BJTs at 800 V.

3.3 Summary

In this chapter, the dynamic characteristics of single and paralleled commercially available Silicon and 4H-SiC NPN BJTs are characterized by means of high-voltage double-pulse measurements, together with LTSpice modeling to confirm the validity of experimental results. Both the turn-on and turn-off time is found to decrease at high collector currents while both switching transitions become slower at high temperatures. The switching transient times in 4H-SiC BJT are, as demonstrated experimentally, at least 10 times shorter than that in Silicon BJT because of the smaller width in the base and drift region. At high collector currents, the high-level injection (Webster) effect leads to the saturation of the negative-temperature-coefficient (NTC) current gain, which is positive (PTC) at low collector currents. The significant turn-off delay in Silicon BJT can lead to the discharge of the capacitor bank and the early increase of collector voltage, which also holds true for SiC BJT as the sudden drop of collector current induce the rise of collector voltage. The significant power dissipation during this period can lead to the failure of the single SiC BJT. When connecting two BJTs in parallel, the longer turn-off delay in Silicon BJTs is observed to incur higher power dissipation and larger current mismatch between paralleled devices. The paralleling of two SiC BJTs mitigates the sudden current drop, as well as avoiding device failure. Therefore, the superior switching performance of SiC BJT favors high-frequency applications since the current drop issues can be resolved by parallel connection and low base resistance. while the significant turn-off delay in Silicon can only be addressed at high collector currents with large base resistances.

Chapter

4 Properties of Discrete & Paralleled High Voltage Silicon & SiC NPN BJTs: Gain, Leakage, IV & R_{ON}

The results published in journal paper 1 and conference paper 1 in Publications list at the outset of the thesis are used in writing of this Chapter. I acknowledge the contribution of my supervisors for laying out the specific objectives, and my co-authors on the methodology and accuracy of the analysis. I have done the Measurements at Bristol's EEMG research laboratory, analysed the results and drafted the papers.

As was seen in Chapter 3, the device temperature and the collector current determine the common-Emitter current gain (β) of power BJT. However, the approach used to measure current gain in Chapter 3 carry with it a serious weakness, i.e., the BJT collector current through the inductive load is smaller than the maximum collector current without the load. The restriction from the load inductor is why the calculated current gain in SiC BJT is much smaller than the expected value from Table. 3.3. To properly measure the current gain and to further study the static performance of commercial SiC BJT, static measurements were conducted to measure the following electrical properties:

- Transfer characteristic
- Base-Emitter leakage Current ($I_{R(BE)}$)

- Collector-Emitter on Resistance (R_{on})
- DC common-Emitter current gain (β)
- Output (I-V) characteristics

4.1 Experimental Set-Up

This chapter characterizes the above-mentioned static properties for the cases of single and the two-paralleled SiC power BJTs GA04JT17-247 and compare with the similarly rated Silicon BJTs FJL6920 by means of extensive experimental measurements. The key electrical parameters of Silicon and SiC BJTs can be found in Table 3.3. To conduct experiments, a B2902A Source/Measure Unit (SMU) is directly connected to either power Silicon or SiC BJTs through high-temperature test leads as shown in Figure 4.1. To connect in parallel, two discrete BJTs are directly connected to each other via their leads for minimal parasitic resistance and parasitic inductance. BJTs are placed in a TAS LTCL600 climatic test chamber, as shown in Figure 4.2 to adjust the operating temperature from −50°C to 150°C in steps of 25 degrees.

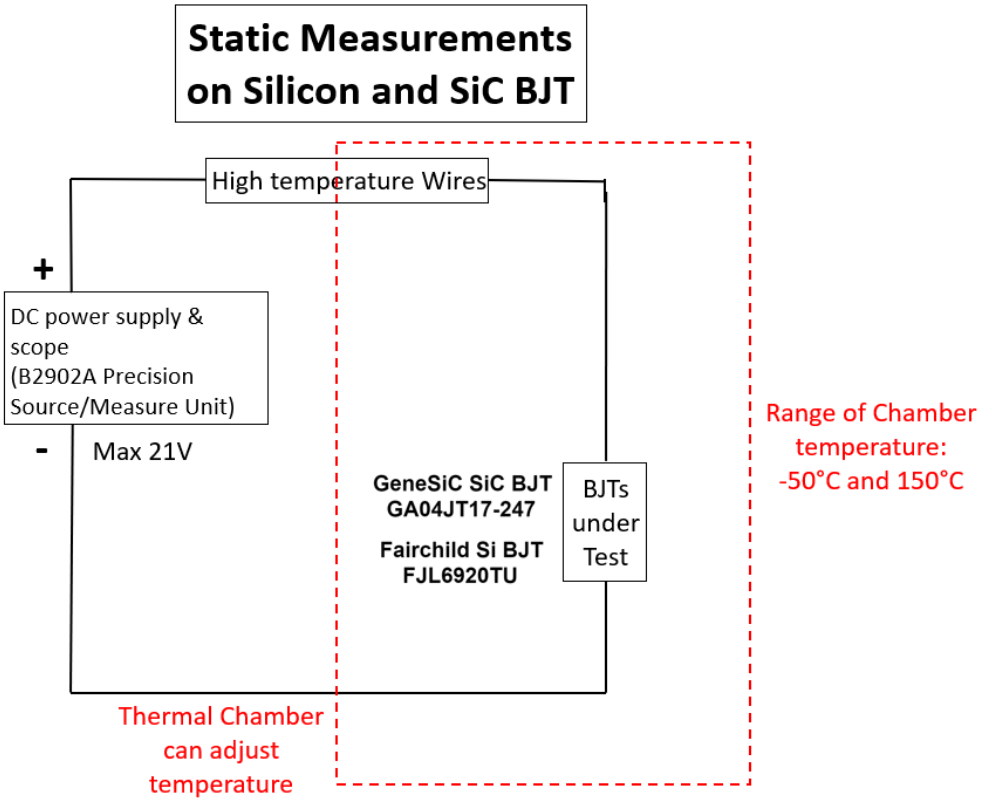

Figure 4.1: Schematic of the experimental rig for static measurements of power BJTs.

Figure 4.2: The thermal chamber and the SMU unit used for the measurements.

4.2 Output Characteristics

To characterize the forward output characteristic, the Collector-Emitter current (I_{CE}) is measured while sweeping the Collector-Emitter voltage (V_{CE}) from 0 to 4 V in 0.04 V increments, with the fixed Base-Emitter current (I_{BE}) of 10 mA, 20 mA and 30 mA used in each set of measurements between −50°C to 150°C. This setting is chosen to ensure the safe operation of both Silicon and SiC BJTs because of the low current rating of SiC BJT at high temperatures while enabling fair and practical comparison between performance of the two devices both in single and paralleled configurations.

4.2.1 Single Silicon BJT

Fig. 4.3 shows the output characteristic of a single Silicon BJT under various Base-Emitter currents. It is clearly observed that the Collector-Emitter current increases with increasing Collector-Emitter voltage for the constant base current. This can be attributed to the increase of current gain because of the reduced density of holes in the drift region with increasing collector bias. It should be noted that the BJT operates in the saturation region only at a very low Collector-Emitter voltage due to the low Base-Emitter voltage as presented in Fig. 4.4. When the base current increases, the rise of electron concentration in the base region promotes the on-state current conduction as discussed in Section. 2.6.2. The observed decrease in Base-Emitter voltage with temperature stems from the positive temperature dependence of the intrinsic carrier concentration resulting in the decrease of built-in voltage as described by Eq. 2.1.

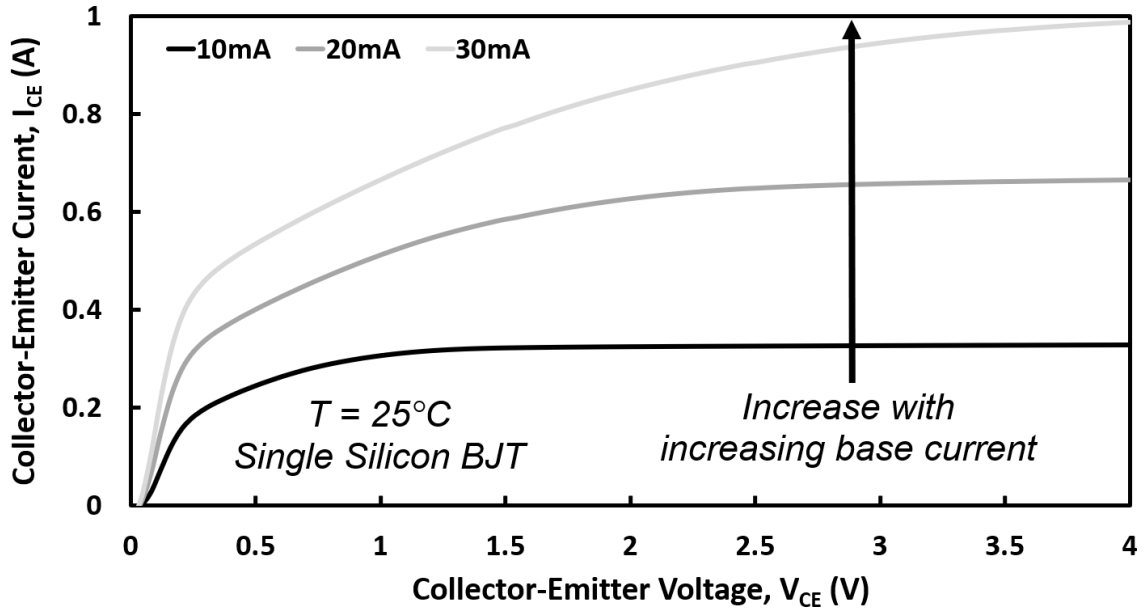

Figure 4.3: Forward I-V characteristics for single Silicon BJT at different Base-Emitter currents (I_{Base}) under 25°C.

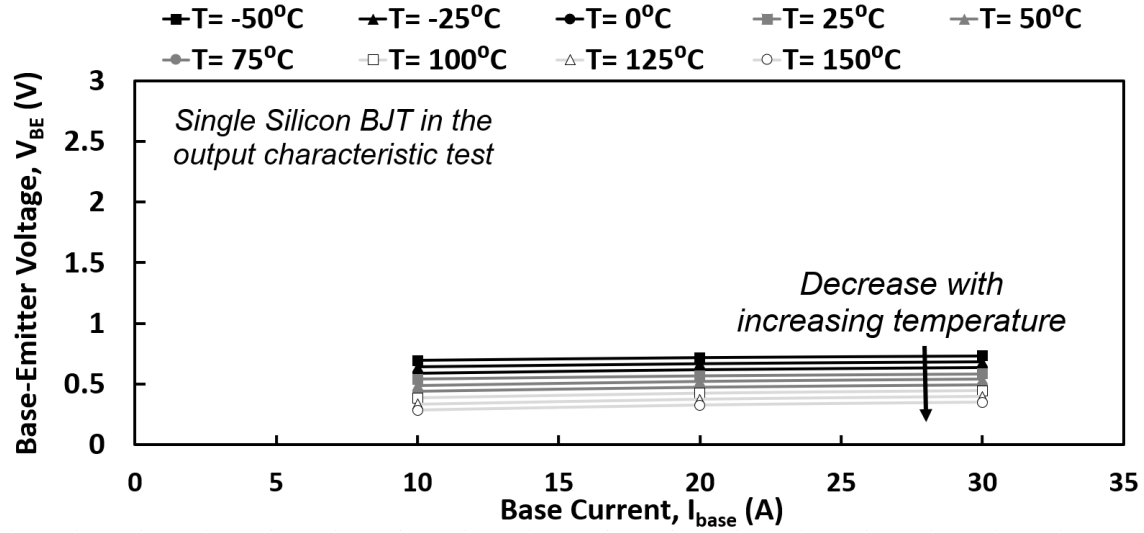

Figure 4.4: Base-Emitter voltage for single Silicon BJT in the output characteristic test.

Fig. 4.5 to Fig. 4.7 shows the output characteristic of single Silicon BJT under various chamber temperatures. At low collector voltage, the collector current increases with in-

creasing temperature because the increasing minority carrier lifetime causes the increase of hole concentration in the drift region, which promotes the conductivity modulation effect to reduce the on-state resistance while the larger Collector-Emitter voltage is required to sweep out the excess of hole concentration and enter the active mode of operation.

Whereas the decrease of Collector-Emitter current is observed in Fig. 4.7 when the operating temperature is higher than 50°C at high base current and at high collector voltage. This was expected due to the reduced Emitter injection efficiency at high collector currents [1, 2]. This is because the increased electron concentration in the base region enhances the injection of holes from the base region into the Emitter region for satisfying charge neutrality. For high temperatures, the onset of Webster effect is shifted to lower collector currents expected by Eq. 2.33 where the temperature dependence of the diffusion coefficient is negative.

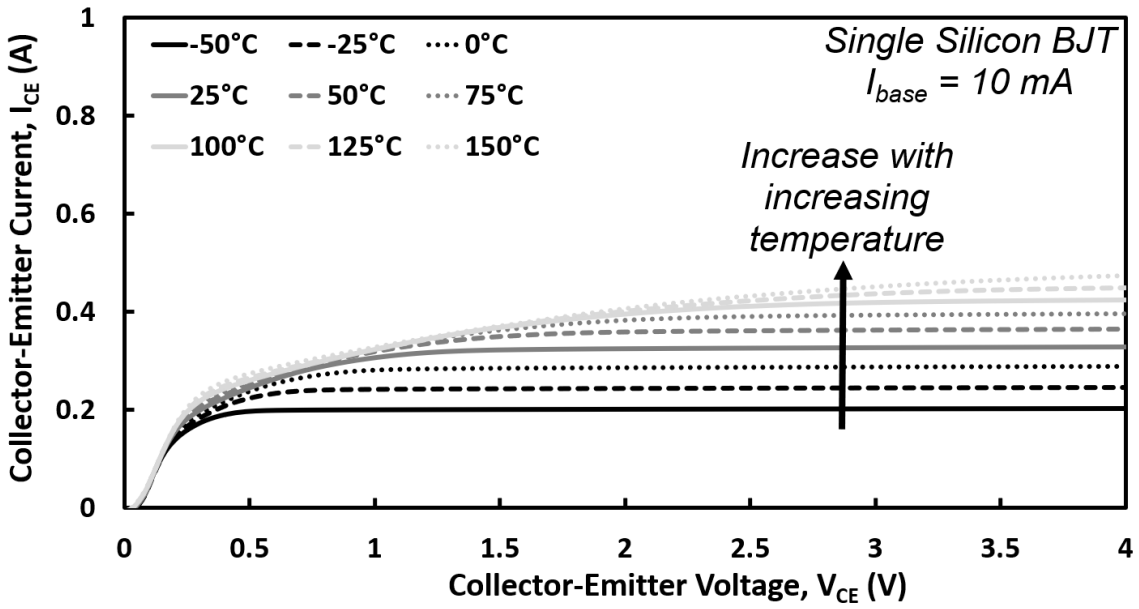

Figure 4.5: Forward I-V characteristics for single Silicon BJT at I_{Base} of 10 mA under different chamber temperatures.

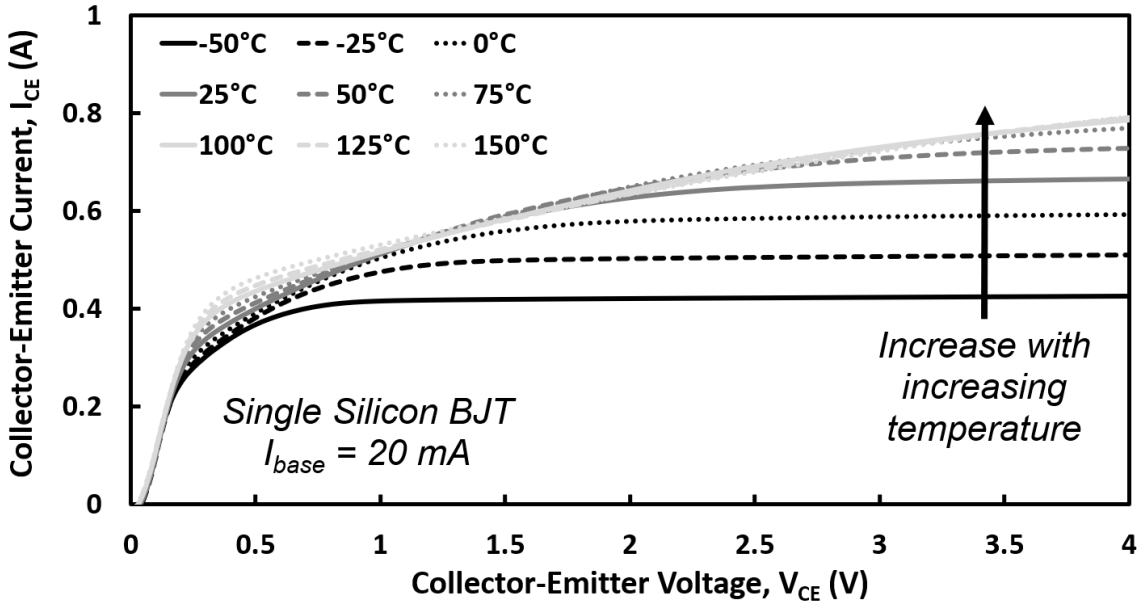

Figure 4.6: Forward I-V characteristics for single Silicon BJT at I_{Base} of 20 mA under different chamber temperatures.

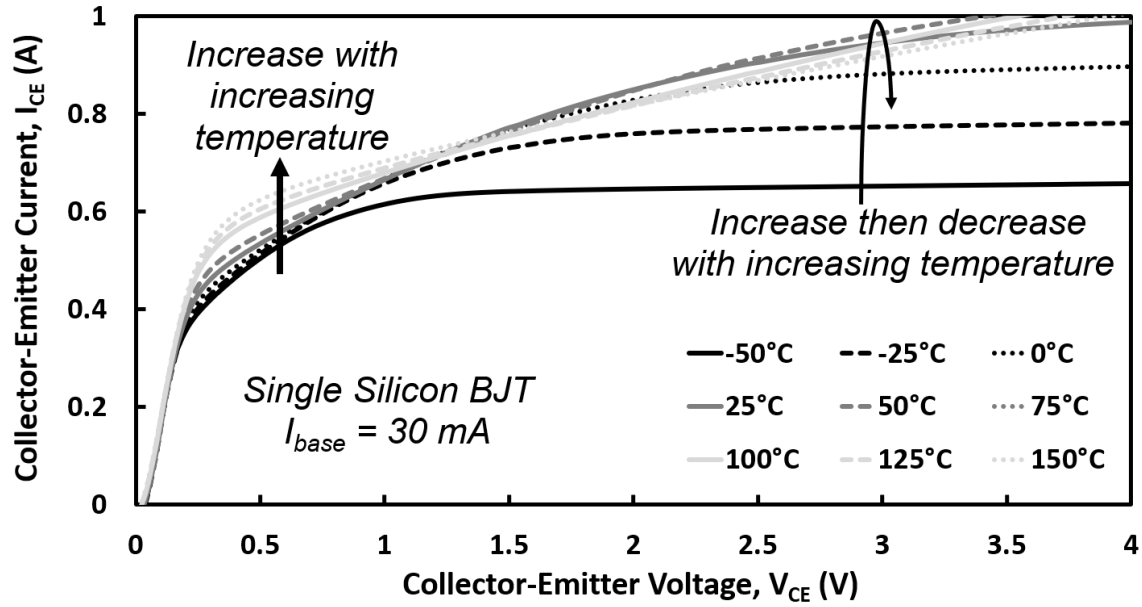

Figure 4.7: Forward I-V characteristics for single Silicon BJT at I_{Base} of 30 mA under different chamber temperatures.

4.2.2 Single SiC BJT

As for the output characteristic of single SiC BJT shown in Fig. 4.8, the collector current saturation implies that the SiC BJT enters the active mode of operation. This is due to the higher doping concentration and smaller thickness of the base and drift region in SiC BJT [5], together with the smaller minority carrier lifetime to suppress the onset of conductivity modulation in the drift region as the on-state resistance is determined by Eq. 2.30 which indicates that the thickness of the voltage blocking drift region, the mobility of carriers and the doping level are key factors in determining the overall resistance as was the case in other device structures.

To push the SiC BJT into the active mode of operation, the low stored charge in the two regions can be easily removed, albeit the Base-Emitter junction is not reverse biased because of the high Base-Emitter voltage as can be observed in Fig. 4.9. The Collector-Emitter voltage is also found to reduce with increasing Collector-Emitter current at 30 mA in Fig. 4.8 after the onset of collector current saturation. This can be accounted for by the negative temperature dependence of the carrier mobility resulting in the increase of drift resistance during self-heating as expected by Eq. 2.30. From Fig. 4.9, the large built-in voltage across the Base-Emitter junction in SiC BJT is caused by the lower intrinsic carrier concentration which also leads to the less temperature dependence of this voltage. Further increase of temperature increases the intrinsic carrier concentration and activate additional dopants to be ionized which are not contributing at room temperature, though the impact of intrinsic carriers released will be more pronounced leading to reduction of the junction voltage.

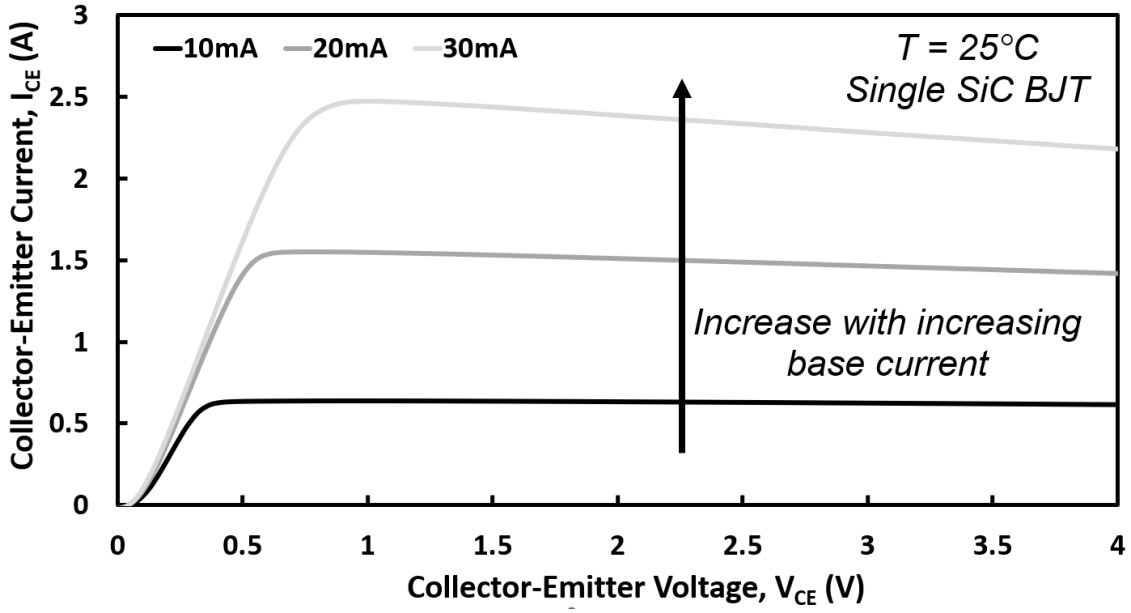

Figure 4.8: Forward I-V characteristics for single SiC BJT at different Base-Emitter currents (I_{Base}) under 25°C.

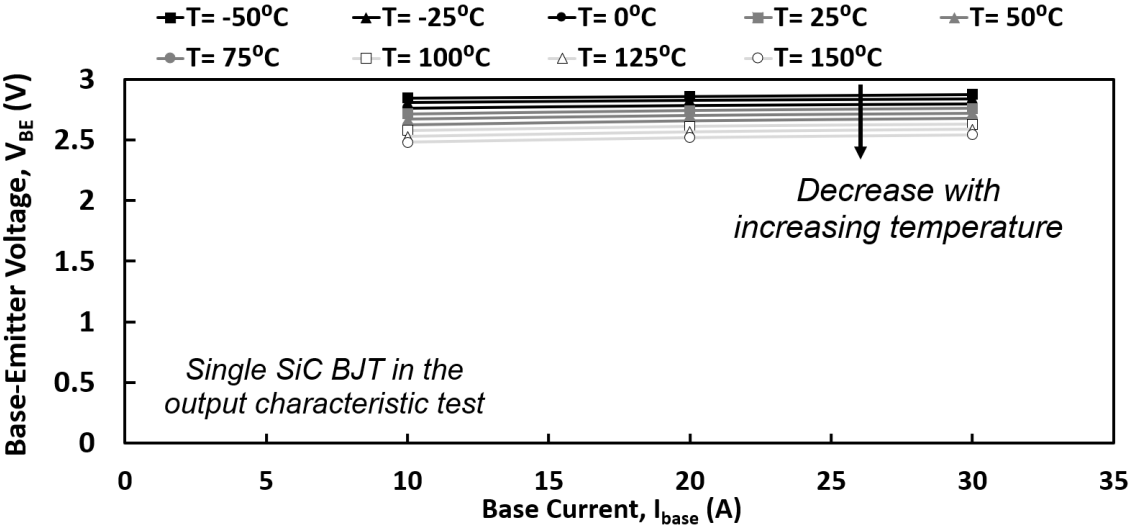

Figure 4.9: Base-Emitter voltage for single SiC BJT in the output characteristic test.

Fig. 4.10 to Fig. 4.12 shows the output characteristic of single SiC BJT under various chamber temperatures. The uncompleted sampling is because of the maximum current

rating of 3 A in the SMU test equipment. Nevertheless, these indicate a much higher current gain than Silicon BJT where β is larger than 150 in the case of 20 mA. This is due to the much higher critical electric field of wide-bandgap SiC leading to the reduction of the width of the base and drift region as depicted in section 2.3. Consequently, the less recombination of carriers in these two regions can lead to a much higher current gain. The negative temperature dependence of the collector current is determined by two important factors. Firstly, the negative temperature dependence of carrier mobility leads to the increase of drift resistance in-line with Eq. 2.30. Additionally the increased hole concentration in the base region at elevated temperatures reduces the Emitter efficiency. This can be explained by the fact that the incomplete ionization of acceptors in the base region of SiC BJT and the increase in hole concentration at higher temperatures [5], i.e., Under room temperature, only 0.4% of dopant is ionized in the base region in 4H-SiC, while the hole concentration is increased to ∼8% of the acceptor density at 150°C [33,91].

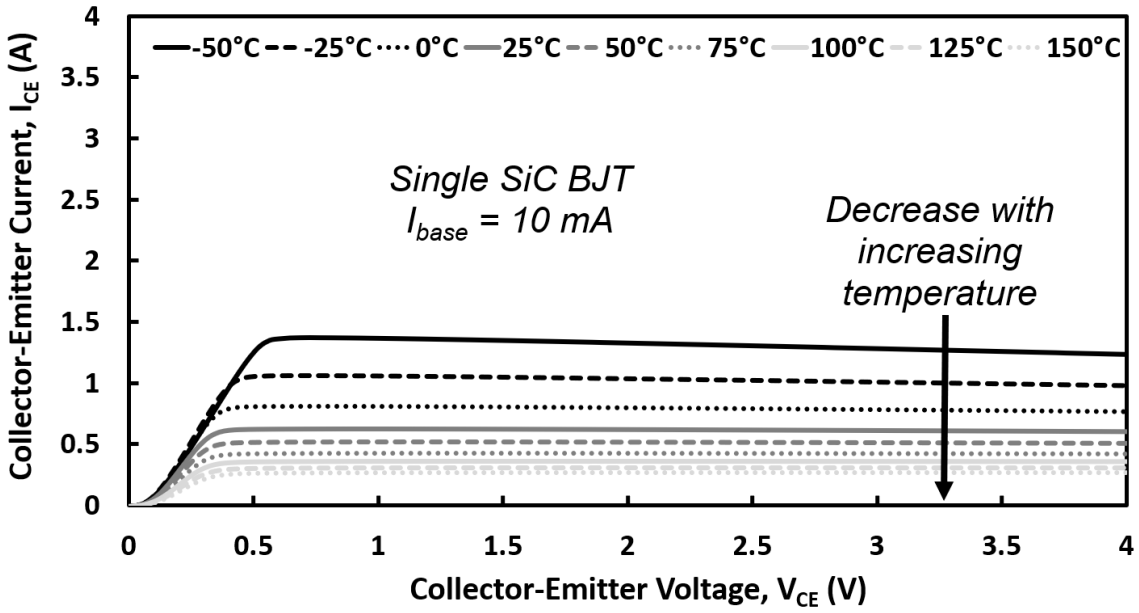

Figure 4.10: Forward I-V characteristics for single SiC BJT at I_{Base} of 10 mA under different chamber temperatures.

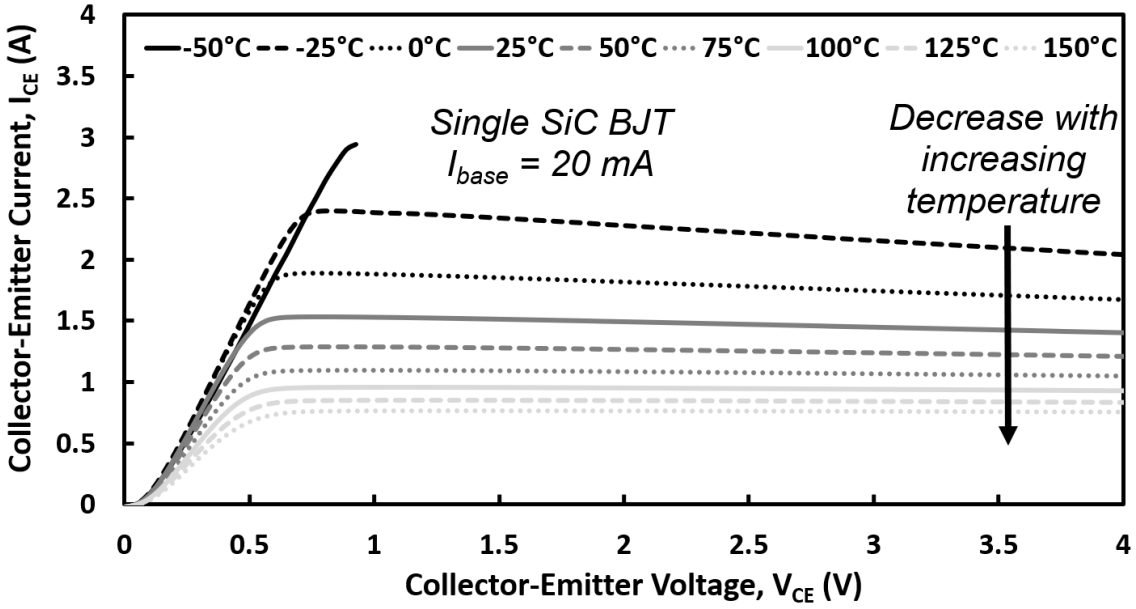

Figure 4.11: Forward I-V characteristics for single SiC BJT at I_{Base} of 20 mA under different chamber temperatures.

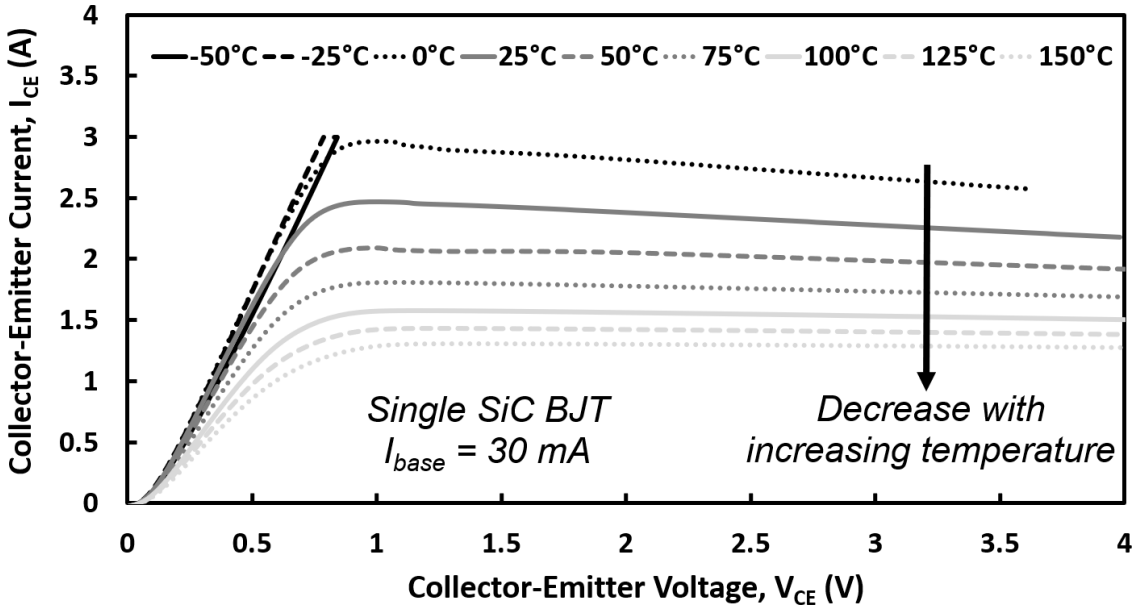

Figure 4.12: Forward I-V characteristics for single SiC BJT at I_{Base} of 30 mA under different chamber temperatures.

4.2.3 Paralleled Silicon BJTs

In terms of paralleled BJTs, the maximum V_{CE} was set to 1 V from the SMU since the sweeping of V_{CE} cannot continue at higher voltages. Fig. 4.13 to Fig. 4.15 show the output characteristics of the two-paralleled Silicon BJTs under various chamber temperatures. Under such low Collector-Emitter voltages, the increase of collector current with increasing temperature is associated with the increased stored charge in the drift region. This is because with increase of temperature additional carriers will be released intrinsically to contribute to the current conduction while the carrier lifetime also increases [33–35]. The mobility is reduced with temperature, however, the impact of the two aforementioned parameters is more pronounced in increasing the Collector-Emitter current. This in turn leads to increase of the DC gain (β) with temperature in the Silicon BJT as will be shown later.

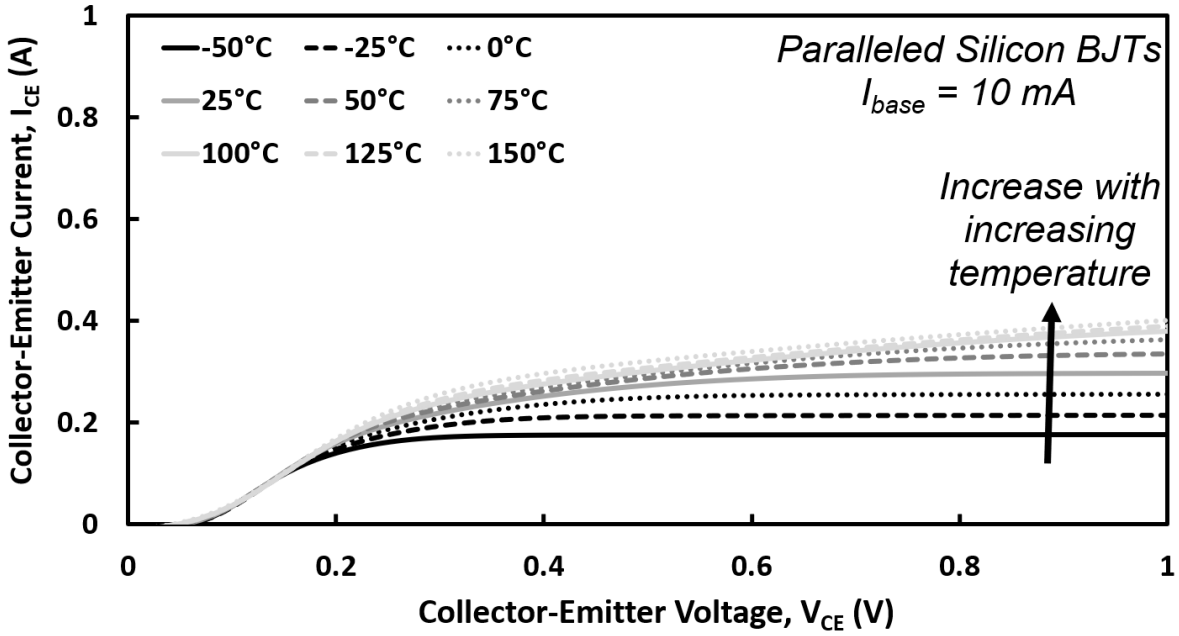

Figure 4.13: Forward I-V characteristics for paralleled Silicon BJTs at I_{Base} of 10 mA under different chamber temperatures.

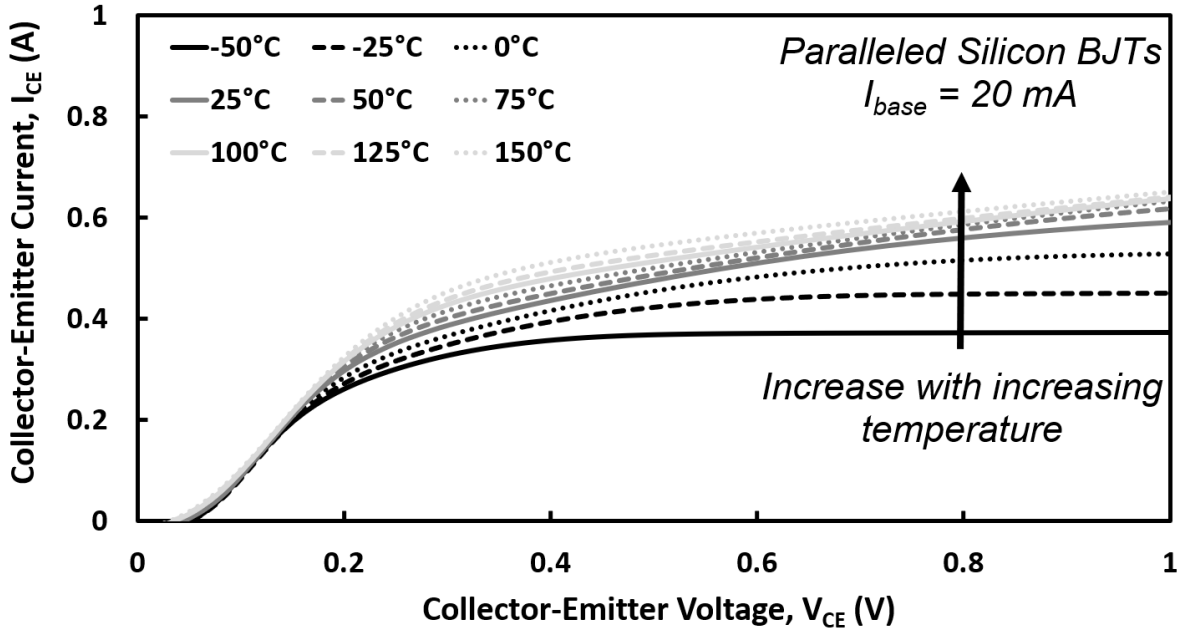

Figure 4.14: Forward I-V characteristics for paralleled Silicon BJTs at I_{Base} of 20 mA under different chamber temperatures.

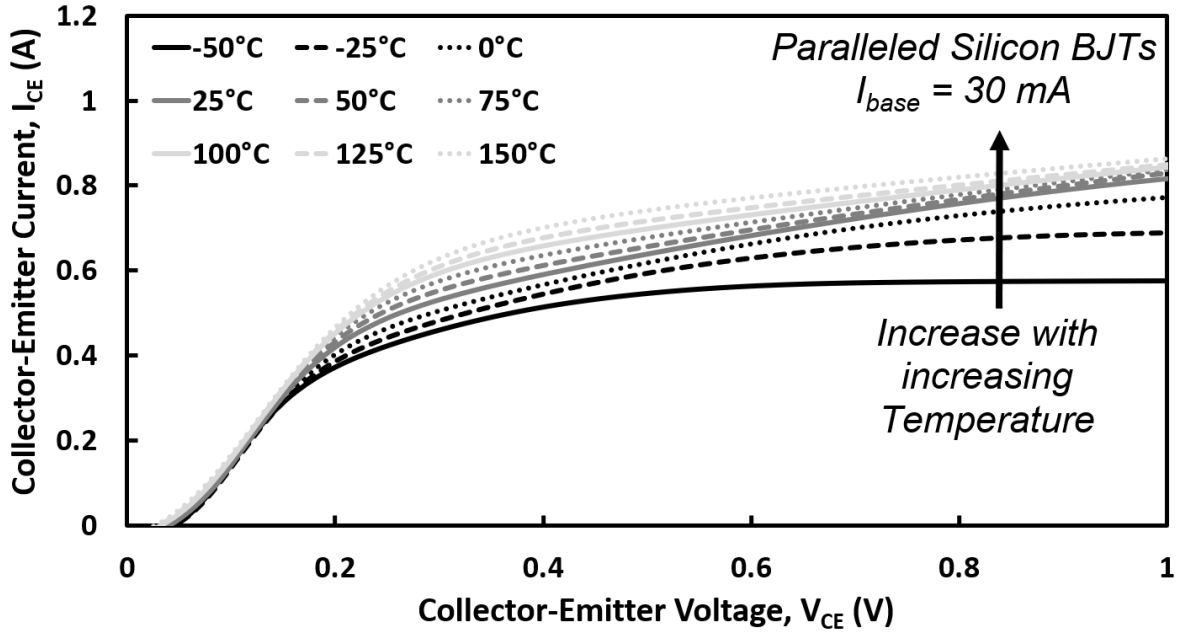

Figure 4.15: Forward I-V characteristics for paralleled Silicon BJTs at I_{Base} of 30 mA under different chamber temperatures.

The comparison between the I-V curves of single Silicon BJT and paralleled Silicon BJTs can be found in Fig. 4.16 to Fig. 4.18. When parallel BJTs are conducting a current, the slight difference in device parameters, namely, the on-state resistance of the Base-Emitter region, can cause current mismatch where the low resistivity one carriers more base current and thus more collector current. At high base currents, the base current imbalance between paralleled becomes worse. At high chamber temperatures, the higher current device is prone to higher junction temperatures and attracts more current since it is more difficult to extract heat. Both conditions produce a huge difference in collector current between two devices together with a huge difference in Collector-Emitter conduction resistance. Such current imbalance can lead to the smaller on-state resistance of paralleled Silicon BJTs than that of single BJT and thus the larger collector as can be seen in Fig. 4.18.

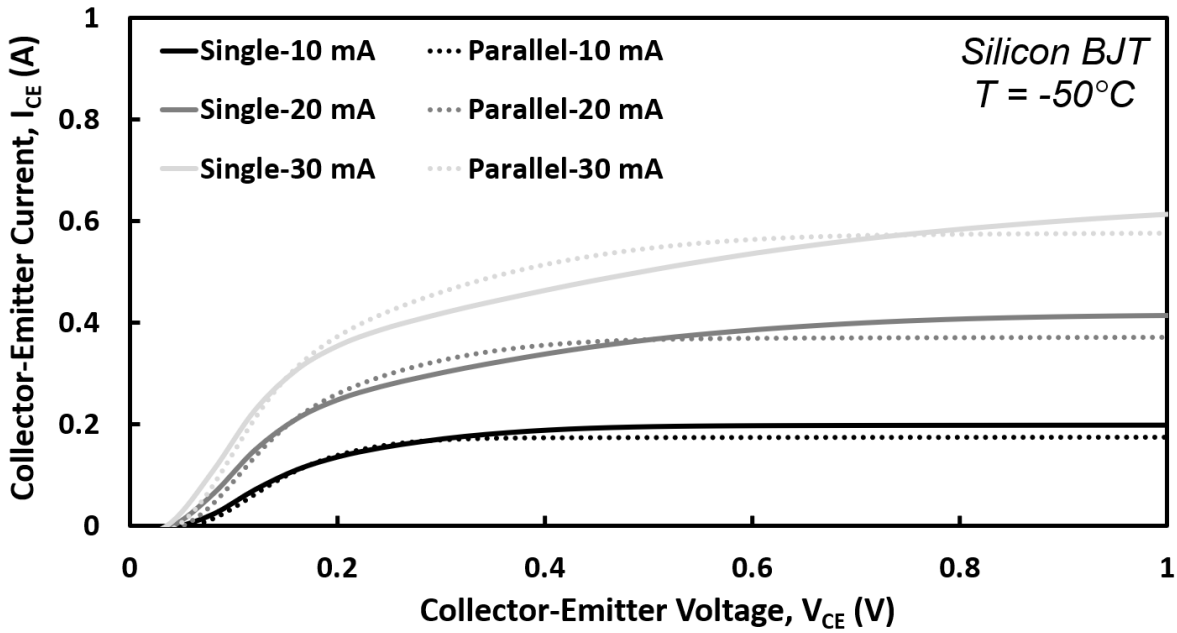

Figure 4.16: Comparison of I-V characteristics for the single and paralleled Silicon BJTs at different base currents under −50°C.

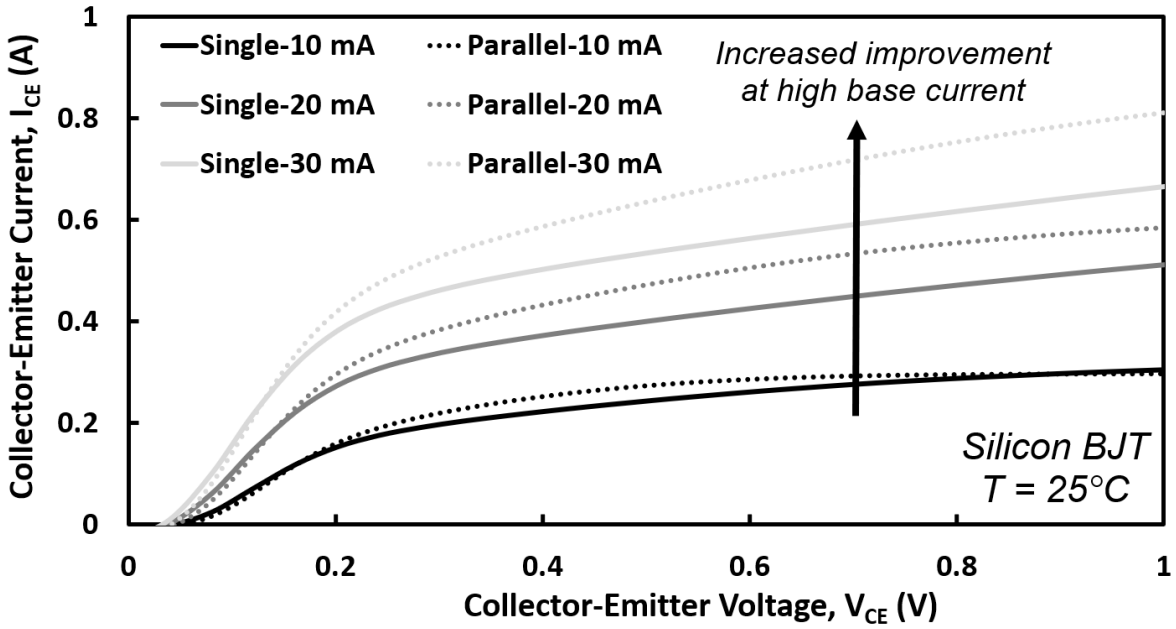

Figure 4.17: Comparison of I-V characteristics for the single and paralleled Silicon BJTs at different base currents under 25°C.

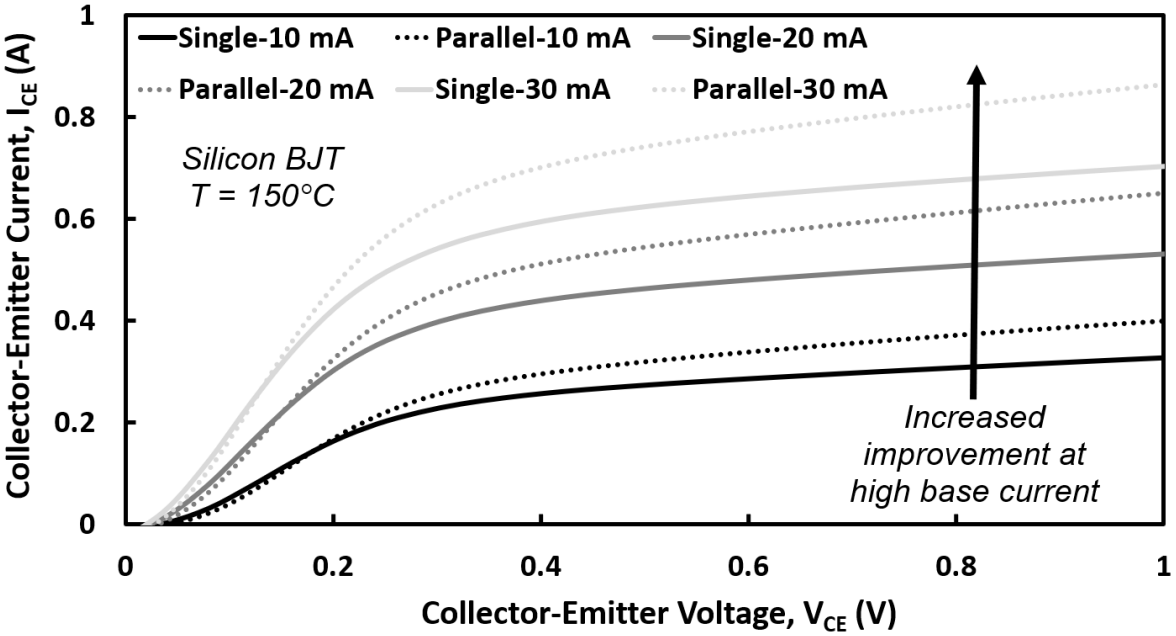

Figure 4.18: Comparison of I-V characteristics for the single and paralleled Silicon BJTs at different base currents under 150°C.

4.2.4 Paralleled SiC BJTs

For paralleled SiC BJTs as shown in Fig. 4.19 to Fig. 4.21, the decrease of collector current is also observed because of the significant incomplete ionization of acceptors at room temperature in the base region. This in turn leads to the surge of hole concentration at high temperatures and reduces the current gain. The incomplete sweeping of Collector-Emitter voltage is caused because the collector current reaches the limit of the SMU.

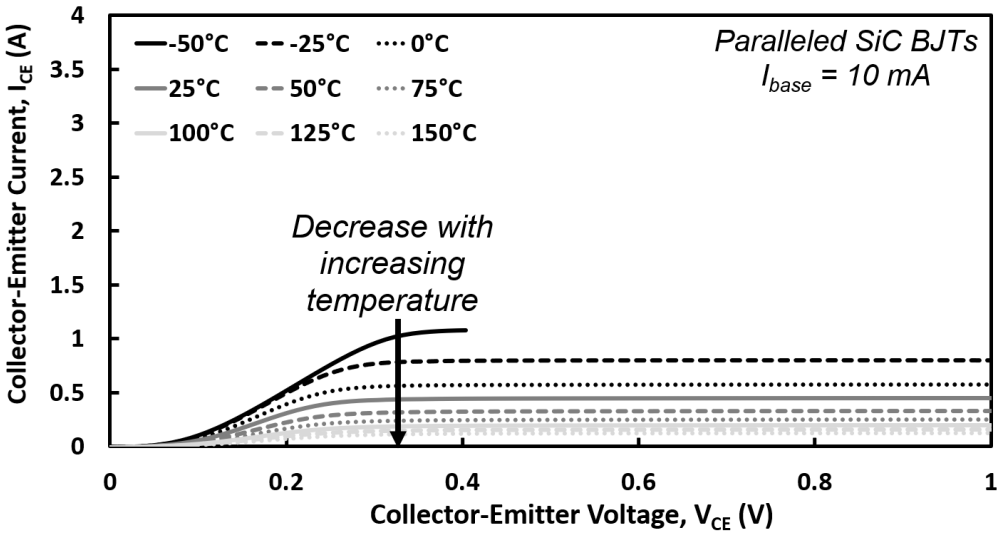

Figure 4.19: Forward I-V of parallel SiC BJTs at I_{Base} of 10 mA by temperatures.

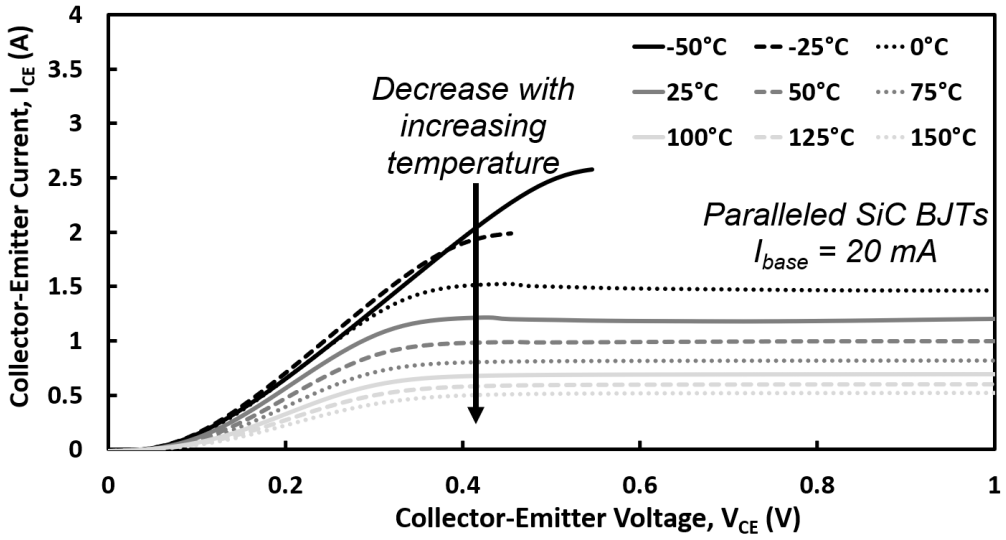

Figure 4.20: Forward I-V of parallel SiC BJTs at I_{Base} of 20 mA by temperatures.

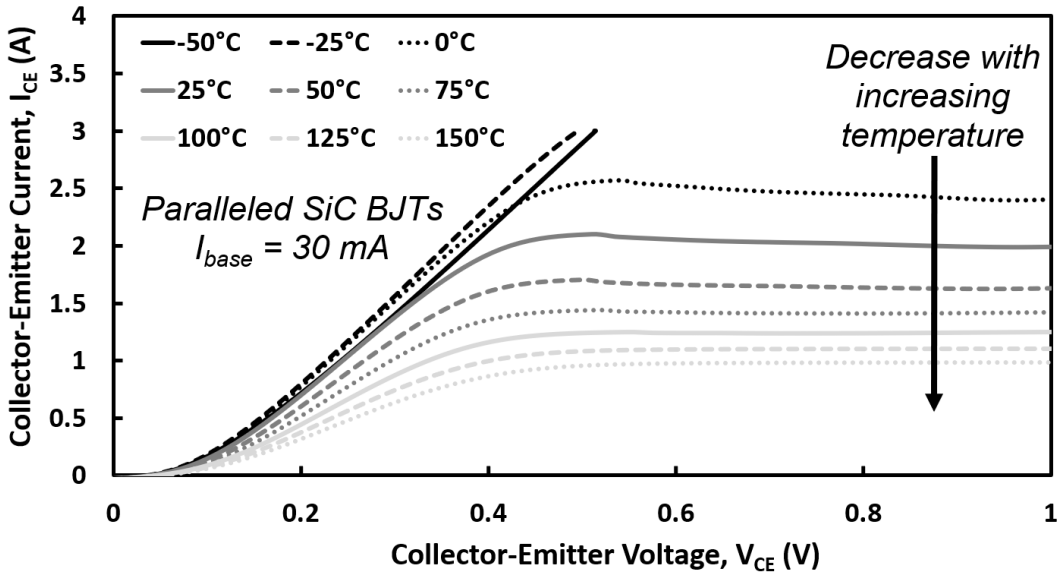

Figure 4.21: Forward I-V of parallel SiC BJTs at I_{Base} of 30 mA by temperatures.

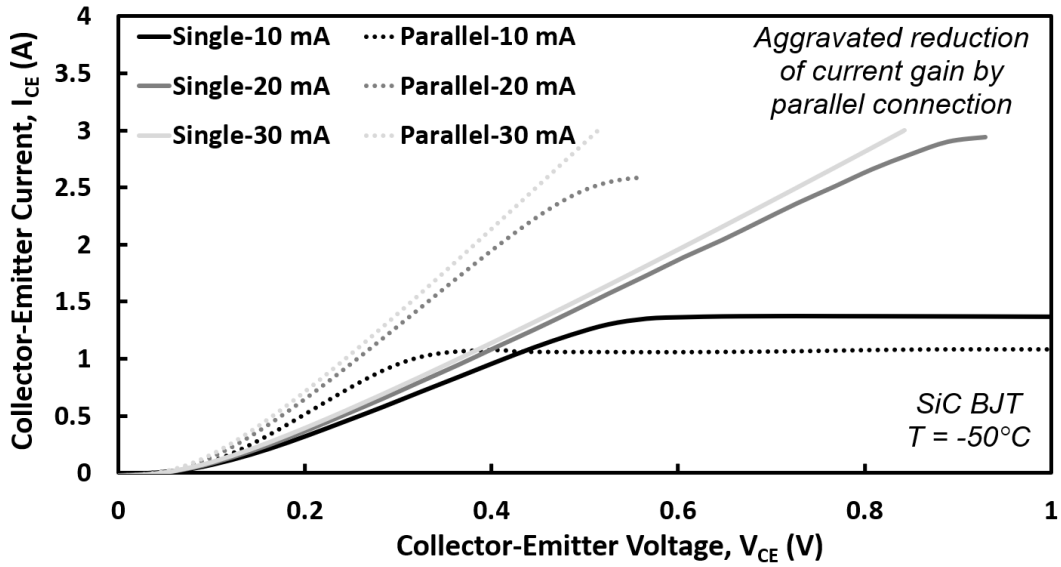

Figure 4.22: Comparison of I-V characteristics for the single and paralleled SiC BJTs at different base currents under −50°C.

Unlike the paralleled Silicon BJTs, the current gain in paralleled SiC BJTs reduces compared to its single device, as observed in Fig. 4.22 to Fig. 4.24. This is due to the fact the two devices are sharing the same base current supplied by a single base driver,

and at lower base current the Collector-Emitter current drops more than expected due to reduced injection efficiency. This was previously seen in Fig. 4.8 where the relationship between base current and the Collector-Emitter current was shown not be fully linear.

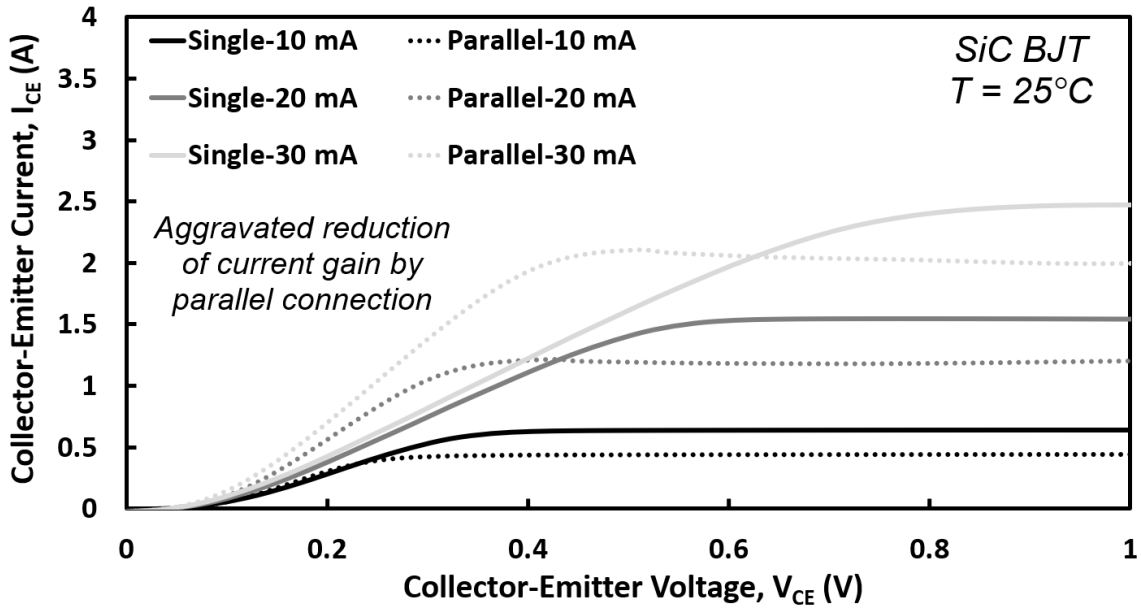

Figure 4.23: Comparison of I-V characteristics for the single and paralleled SiC BJTs at different base currents under 25°C.

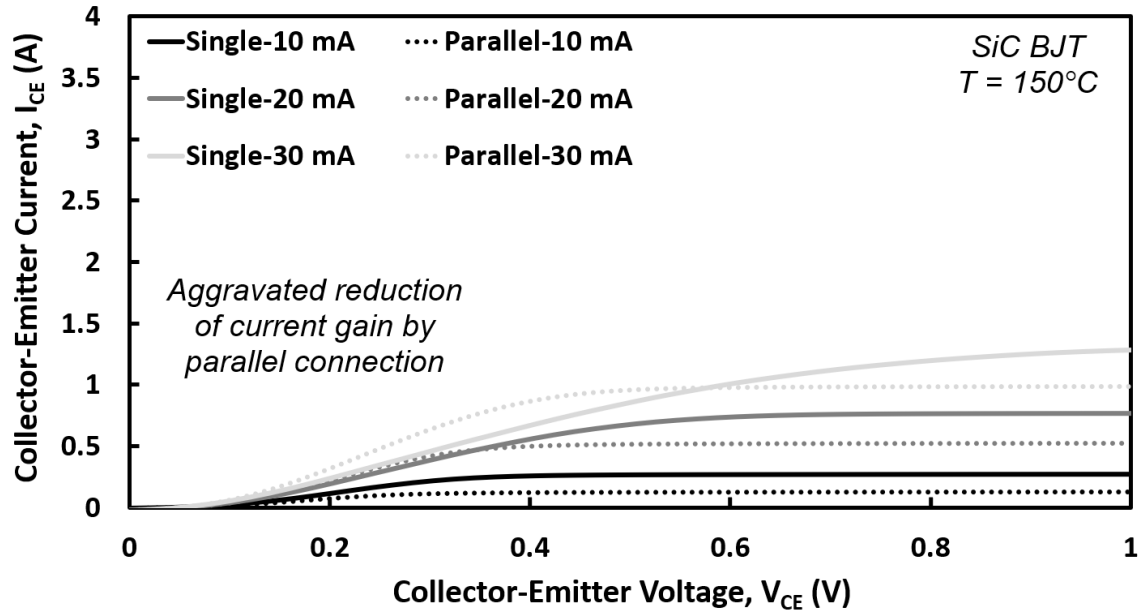

Figure 4.24: Comparison of I-V characteristics for the single and paralleled SiC BJTs at different base currents under 150°C.

4.2.5 Single and Paralleled BJTs: Silicon vs. SiC

4.2.5.1 Single BJTs

Fig. 4.25 to Fig. 4.27 provides the comparison of output characteristics for Single Silicon and Single SiC BJT. The output characteristic of SiC BJT always outperforms that of Silicon BJT under most test conditions, especially at high gate currents and in low temperatures. However, the opposite temperature dependence of I-V curves of Silicon BJT and SiC BJT leads to the poor I-V curve in SiC BJT under high temperatures as can be observed in Fig. 4.27. Here, the Collector-Emitter current in Silicon BJT is slightly increased with temperature while it is significantly decreased in the case of the SiC device to the degree it falls below the Silicon counterpart, i.e. SiC exhibiting a lower DC gain (β) in high temperature with low base current. This is primarily due to the activation of the ionized dopants in SiC in higher temperature, reducing the Emitter injection efficiency in the base region, while in Silicon most dopants have already been activated in room temperature and only benefiting from higher carrier lifetime.

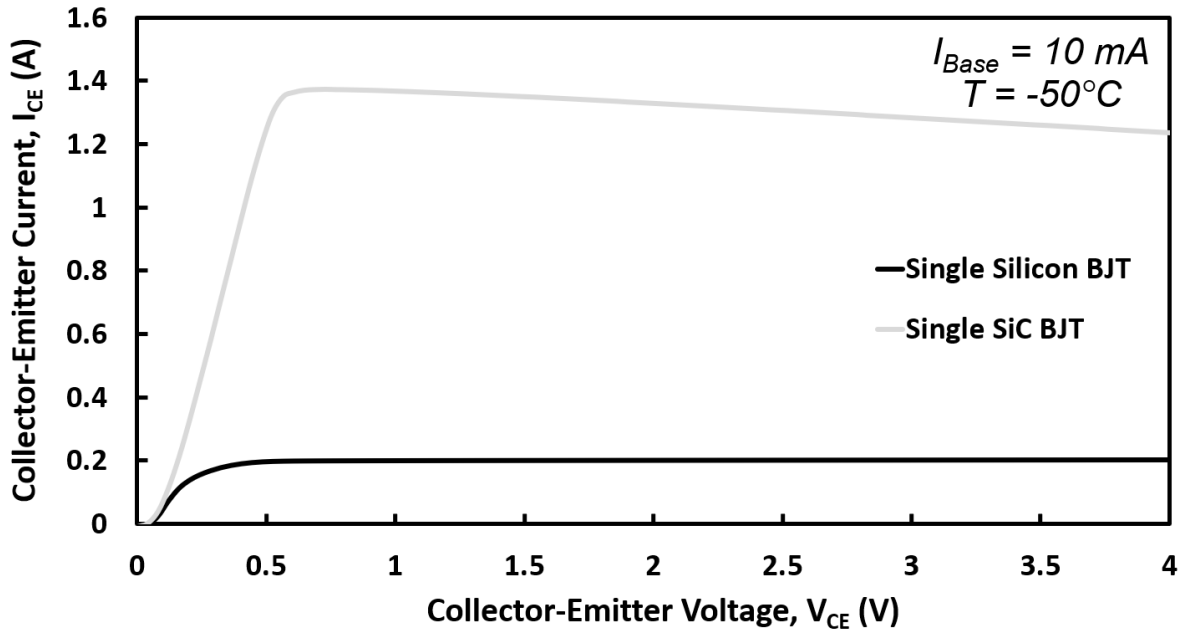

Figure 4.25: Comparison of I-V characteristics of single Silicon and SiC BJT at I_{Base} of 10 mA under −50°C.

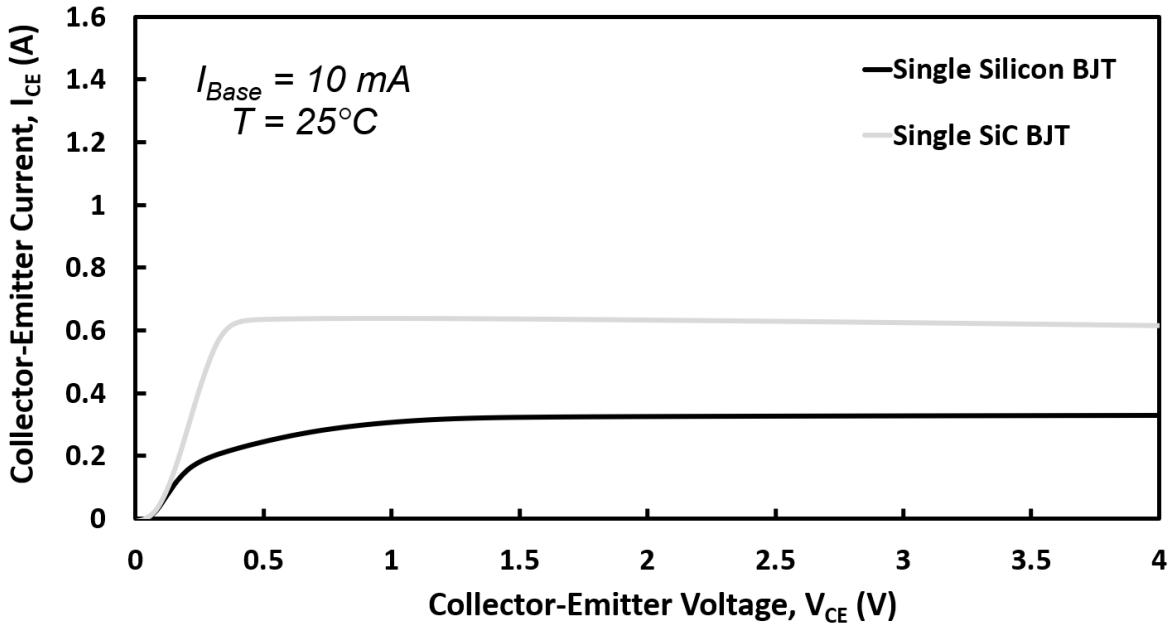

Figure 4.26: Comparison of I-V characteristics of single Silicon and SiC BJT at I_{Base} of 10 mA under 25°C.

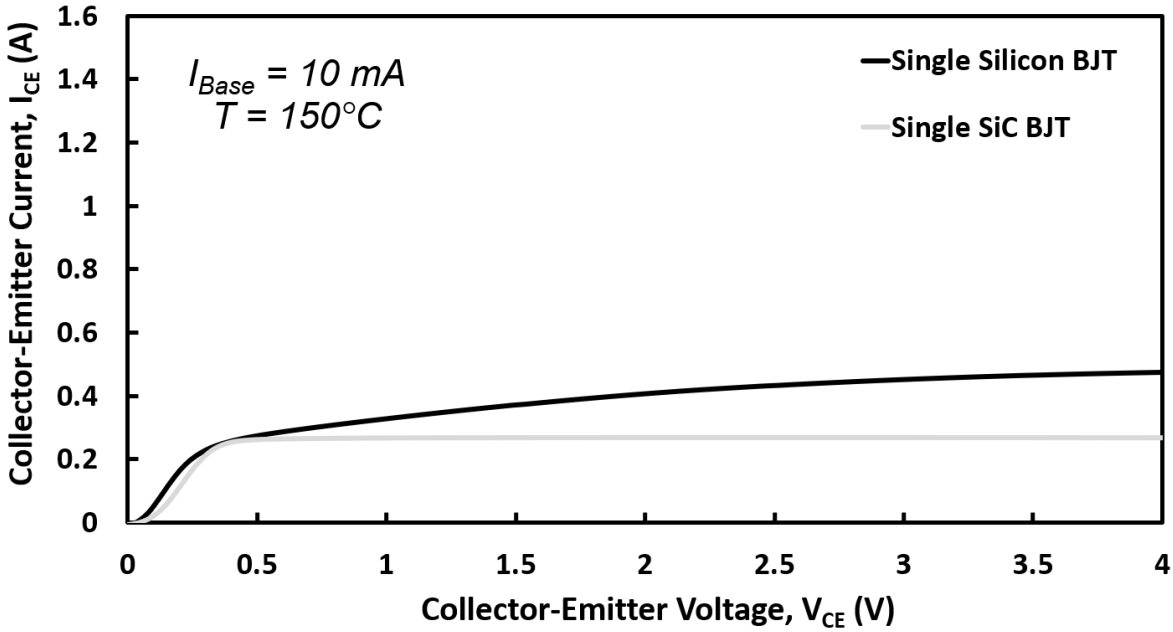

Figure 4.27: Comparison of I-V characteristics of single Silicon and SiC BJT at I_{Base} of 10 mA under 150°C.

4.2.5.2 Paralleled BJTs

Such instability problem of current gain in SiC BJT is even worse when in parallel connection as the reduction of Emitter efficiency can occur in both SiC devices, where the difference of current gain between paralleled Silicon BJTs and paralleled SiC BJTs is about 28 at 1 V as shown in Fig. 4.30 while the current gain gap is approximately equal to 20.5 at 4 V as found from Fig. 4.27. It can be seen that the same trend in the single devices is once again observed further intensifying. It must be noted that in the case of the paralleled device the base current is supplied by the same base driver and shared between the two paralleled devices, further reducing the base current supplied per device which as expected has led to further reduction of the DC current gain in the SiC.

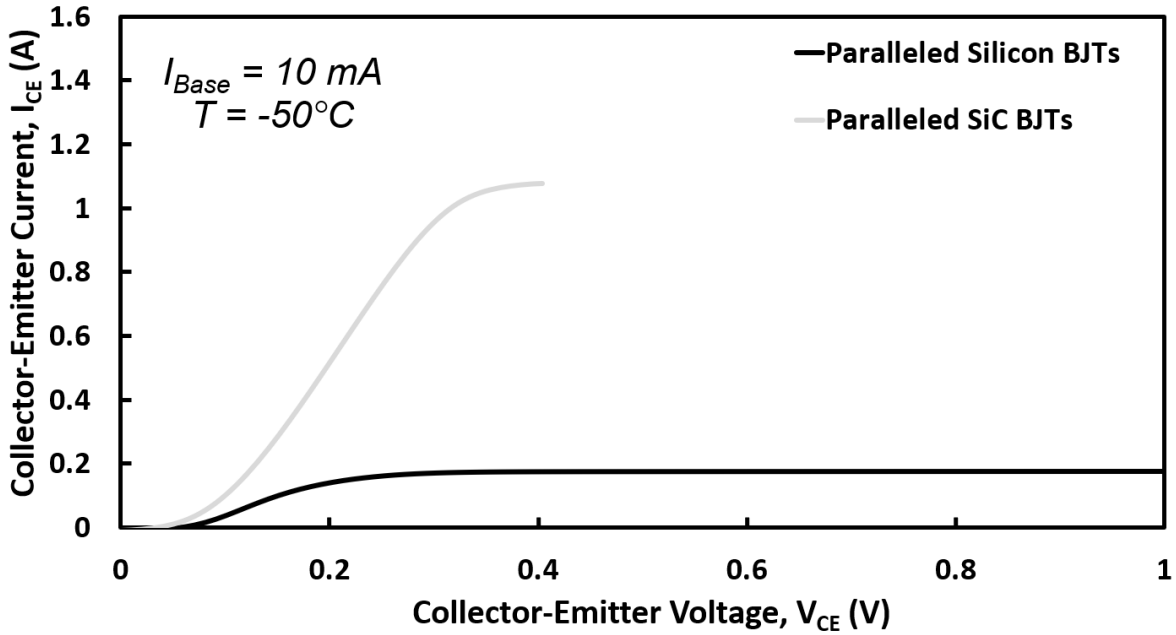

Figure 4.28: Comparison of I-V characteristics of paralleled Silicon and SiC BJTs at I_{Base} of 10 mA under −50°C.

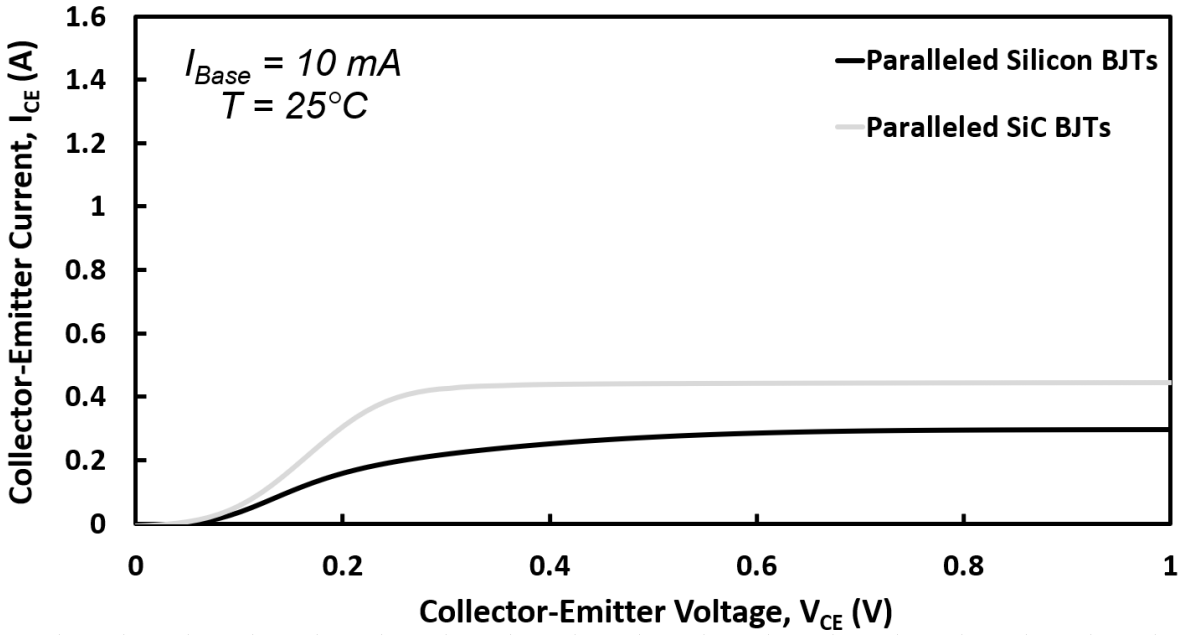

Figure 4.29: Comparison of I-V characteristics of paralleled Silicon and SiC BJTs at I_{Base} of 10 mA under 25°C.

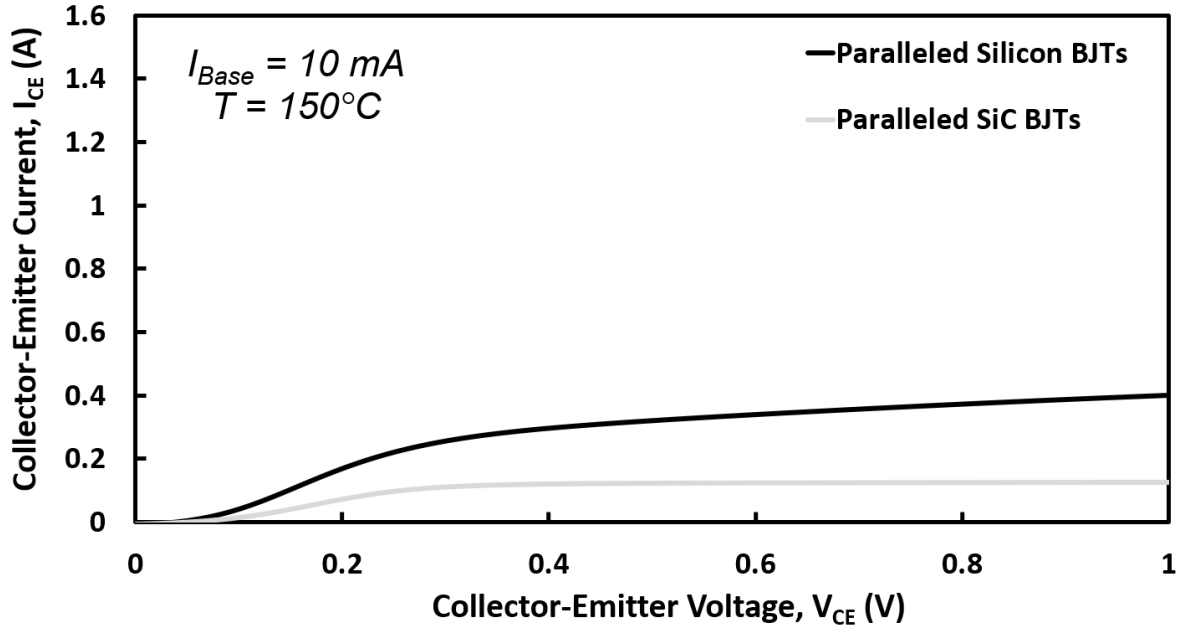

Figure 4.30: Comparison of I-V characteristics of paralleled Silicon and SiC BJTs at I_{Base} of 10 mA under 150°C.

4.3 Static DC Current Gain

The output characteristics and I-V curves of power BJTs are mainly determined by the on-state resistance and current gain. The calculations of DC common-Emitter current gain (β) are based on values taken from Section. 4.2, i.e., the maximum collector current within the Collector-Emitter voltage of 1 V was used to calculate the maximum current gain. The selection of 1 V is due to the crash of the SMU test equipment whenever the Collector-Emitter voltage exceeds 1 V for parallel-connected SiC BJTs.

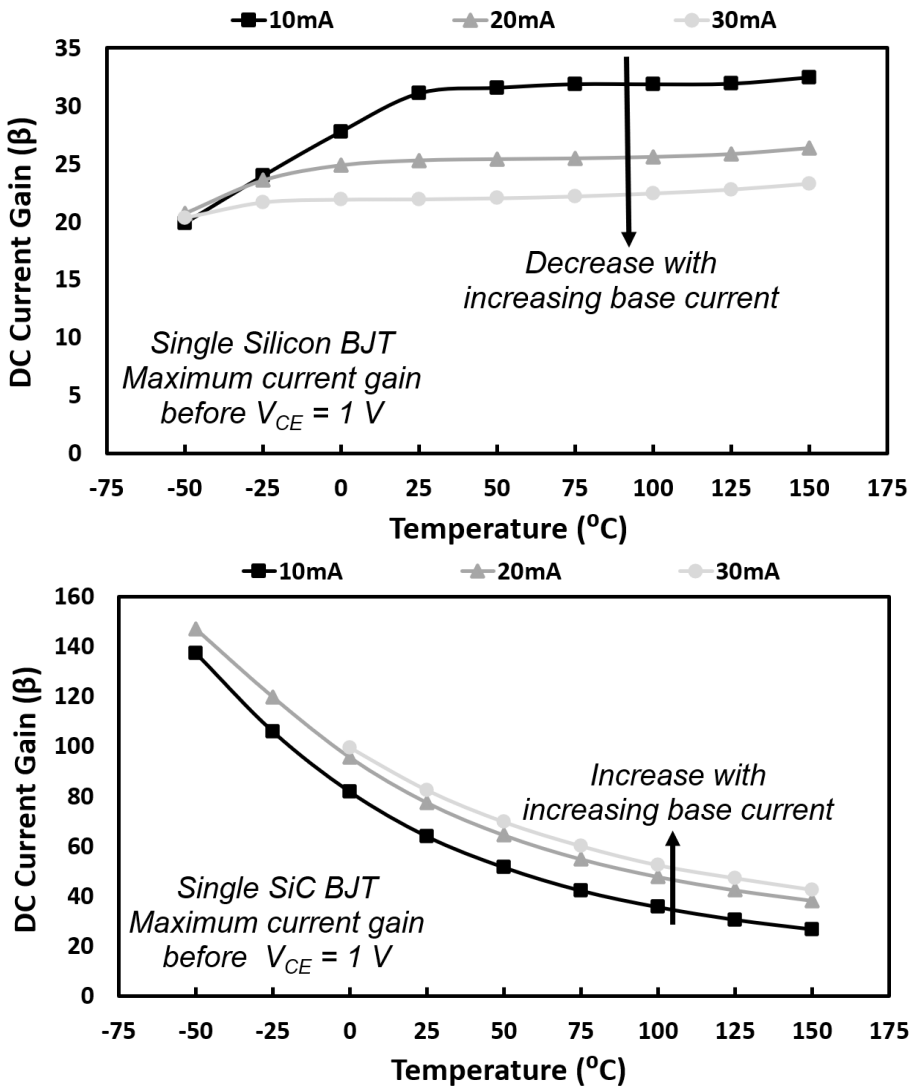

Figure 4.31: Common-Emitter current gain of single Silicon BJT & SiC BJT.

Fig. 4.31 shows the calculated DC current gain for single Silicon BJT and single SiC BJT under various base currents. The positive temperature coefficient (PTC) of current gain in Silicon BJT is associated with the increased stored charge in the drift region, while the negative temperature coefficient (NTC) in SiC BJT can be explained by the partial ionization of acceptors in the base region as discussed in Section. 4.2.

Although the collector current was found to increase with increasing base current from Section. 4.2, the current gain for Silicon BJT decreases with increasing base current, which reflects the reduced efficiency of current transport during the on-state. This is due to the increased portion of the base current injected into the drift region to maintain the stored charge. The abrupt junction profile with high doping concentration on the base region and low doping concentration on the drift region promotes the diffusion of holes from the base region into the drift region based upon Fick's flux of carriers law [1, 17]. However, this does not hold true for SiC BJT as the difference between the doping concentration of the base and the drift region is small because of the significant incomplete ionization in the base region, which in turn limits the diffusion of holes into the drift region. Therefore, the current gain increases with increasing base current.

In terms of current gain for paralleled devices as observed in Fig. 4.32, the current gain of paralleled Silicon BJT is slightly lower than that of single BJT under low temperatures but higher current gain under high temperatures. This is in-line with results shown in Fig. 4.16 to Fig. 4.18 as the improvement in current gain becomes evident at high temperatures. In contrast, the paralleled SiC BJTs lead to the lower current gain as discussed in Section. 4.2.

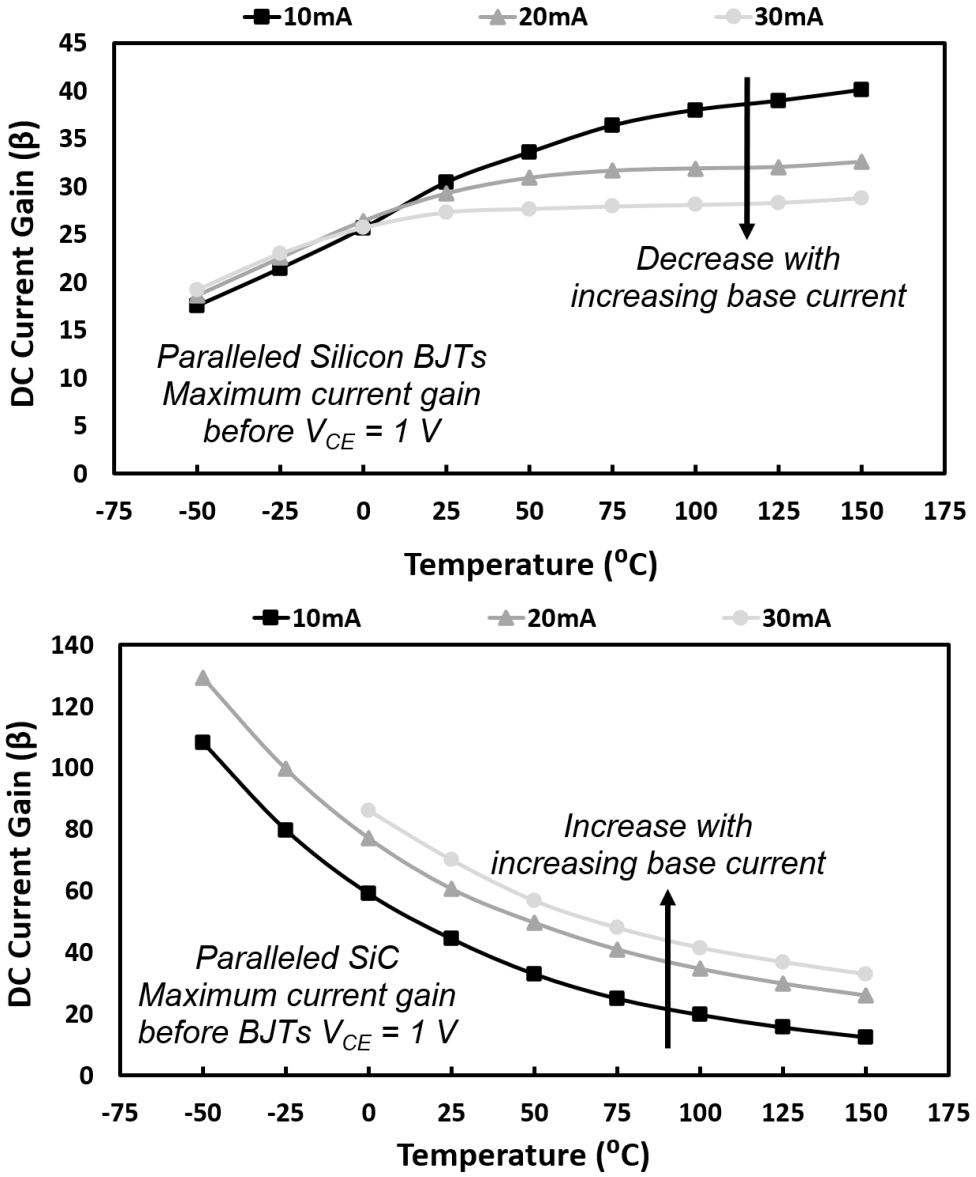

Figure 4.32: Common-Emitter current gain for Paralleled Silicon BJTs and SiC BJTs.

4.4 On-State Resistance

In this section, those BJTs are characterised at higher collector currents. The on-state resistance (R_{ON}) is measured by applying a fixed base current increased from 0.2 A to 0.5 A while applying a pulse of collector current ranged from 1 A to 3 A.

4.4.1 Single Silicon BJT

Fig. 4.33 to Fig. 4.35 shows the on-state resistance of single Silicon BJT under various chamber temperatures at different collector currents. The increase of base current can lead to the increase of electron concentration in the base region and thus the lower on-state resistance. The positive temperature dependence of the on-resistance, which is similar to the I-V curves at high collector voltages displayed in Fig. 4.7, indicates the active mode of operation of Silicon BJT together with the onset of Webster effect. The negative temperature dependence of base voltage further increases the on-resistance. As can be seen, higher base currents are required for higher collector current, otherwise the device may undergo high on-resistance with the insufficient base current. The increased base current can switch the Silicon BJT from the active mode to the quasi-saturation mode for the case of the collector current of 3 A.

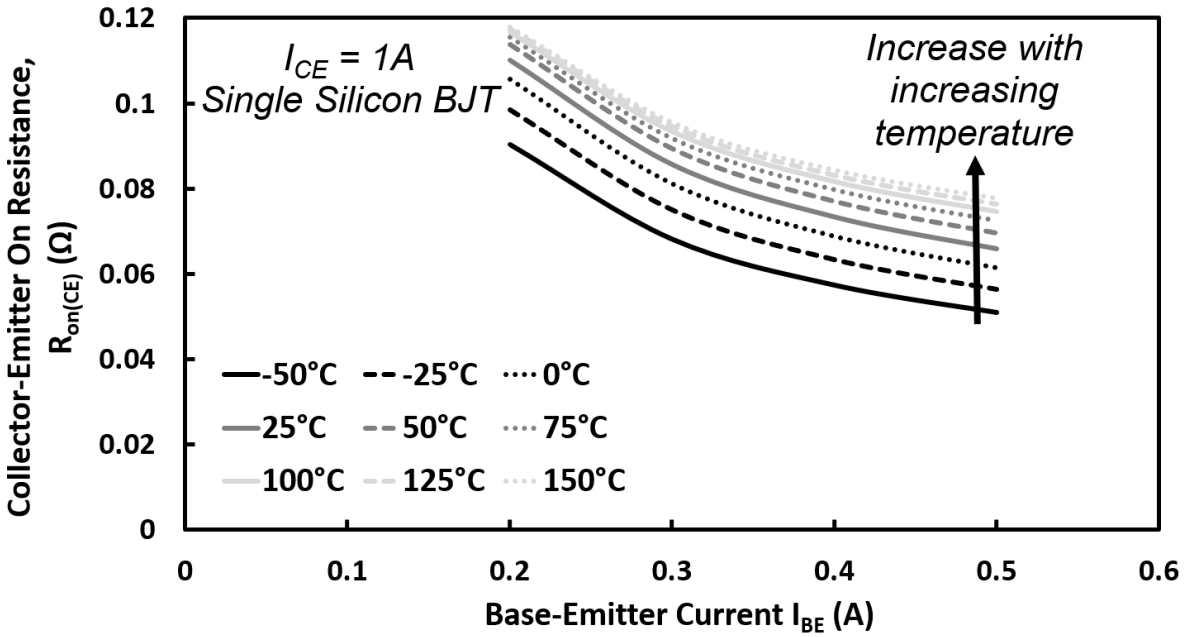

Figure 4.33: On-state resistance for single Silicon BJT at I_{CE} of 1 A under different chamber temperatures.

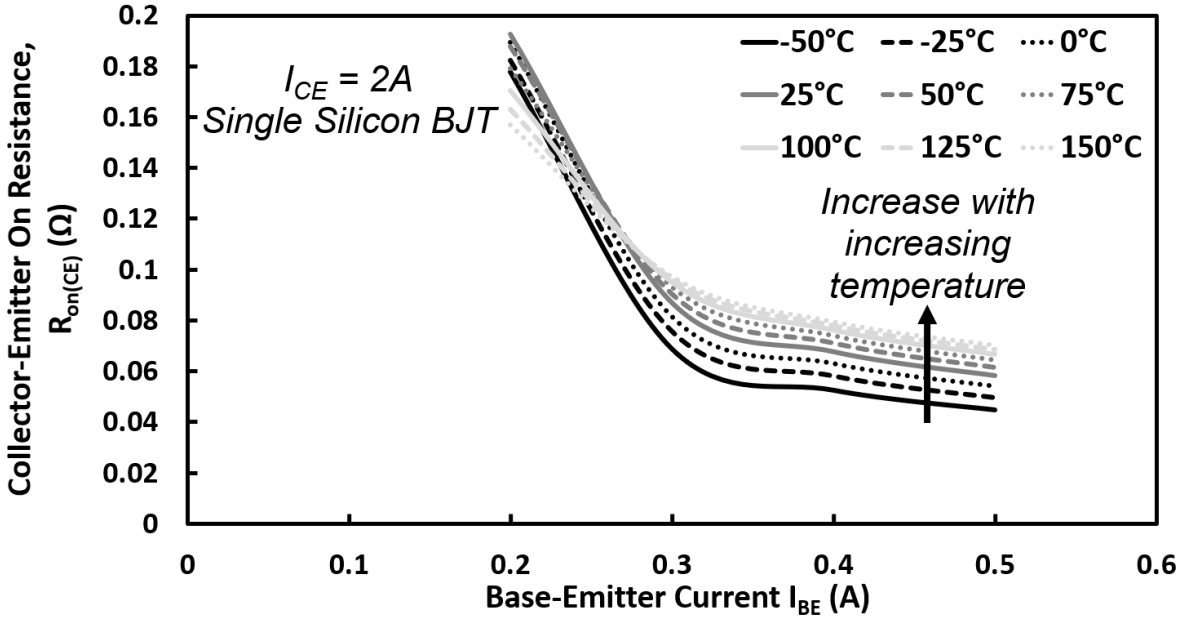

Figure 4.34: On-state resistance for single Silicon BJT at I_{CE} of 2 A under different chamber temperatures.

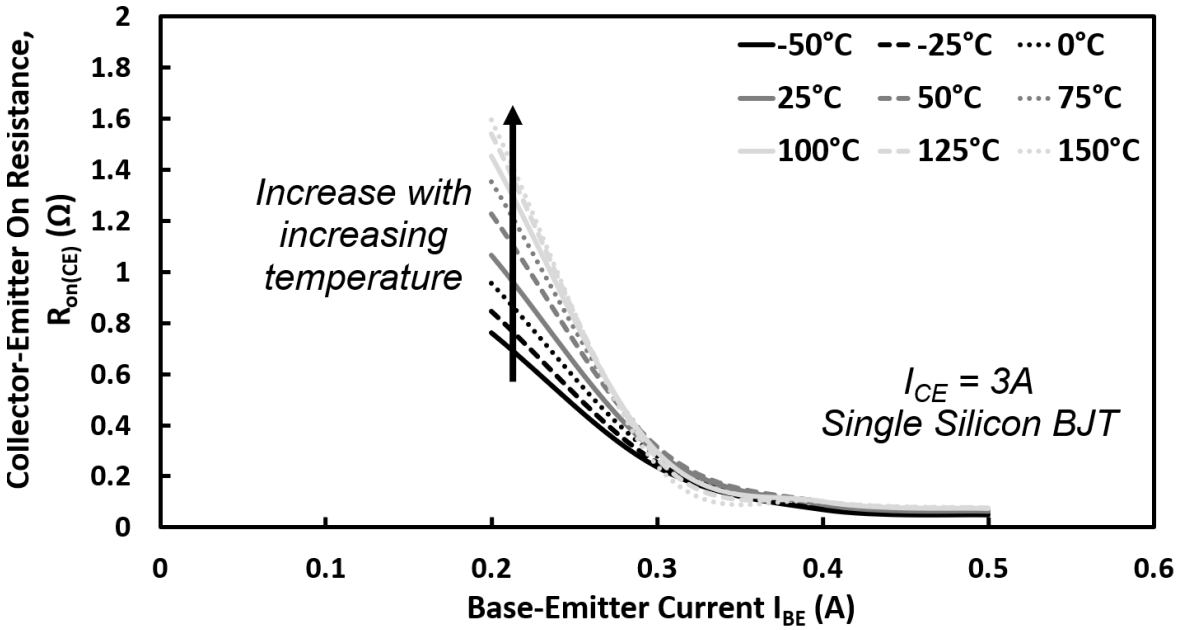

Figure 4.35: On-state resistance for single Silicon BJT at I_{CE} of 3 A under different chamber temperatures.

4.4.2 Single SiC BJT

Fig. 4.36 to Fig. 4.38 shows the on-resistance of single SiC BJT under various chamber temperatures at different collector currents. Unlike the Silicon BJT, SiC BJT always operates in the quasi-saturation region as the Base-Emitter voltage is much larger than the base-collector voltage. The temperature dependence of SiC BJT is mainly determined by the drift resistance and the increase of base doping concentration with temperature. The increased base doping with temperature leads to promote the hole diffusion to reduce the on-resistance at high temperatures while the drift resistance increases with temperature as expected by Eq. 2.30. These competing effects lead to the NTC of on-resistance at low temperatures while PTC at high temperatures. At high collector currents, the temperature dependence of the drift region plays the dominant role to have PTC of on-resistance.

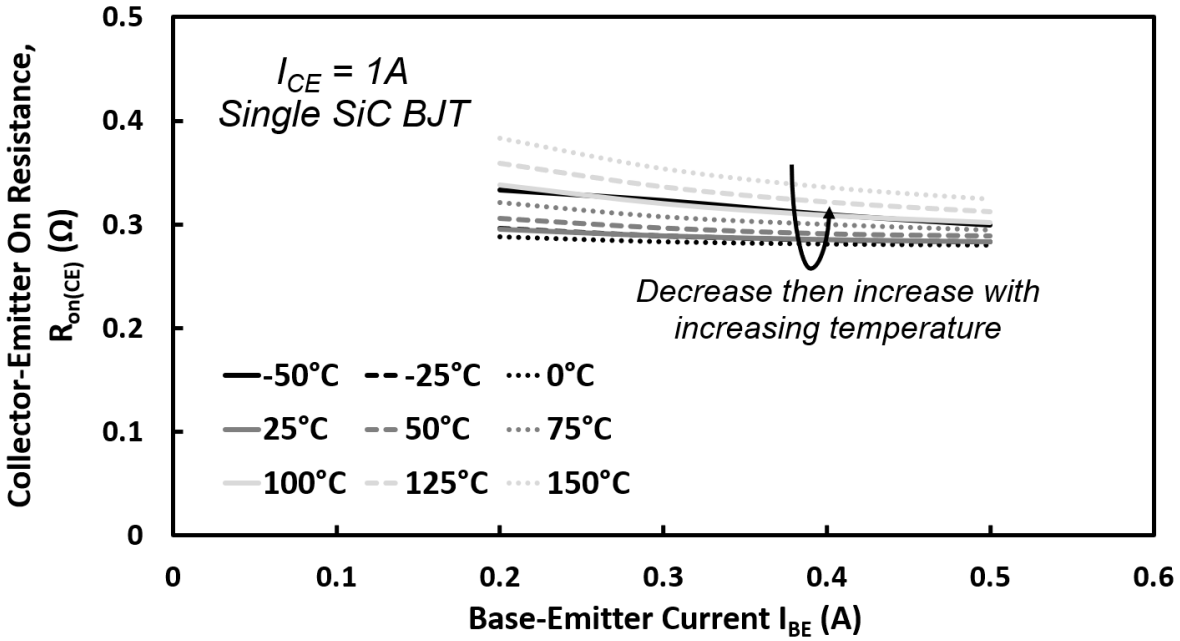

Figure 4.36: On-state resistance for single SiC BJT at I_{CE} of 1 A under different chamber temperatures.

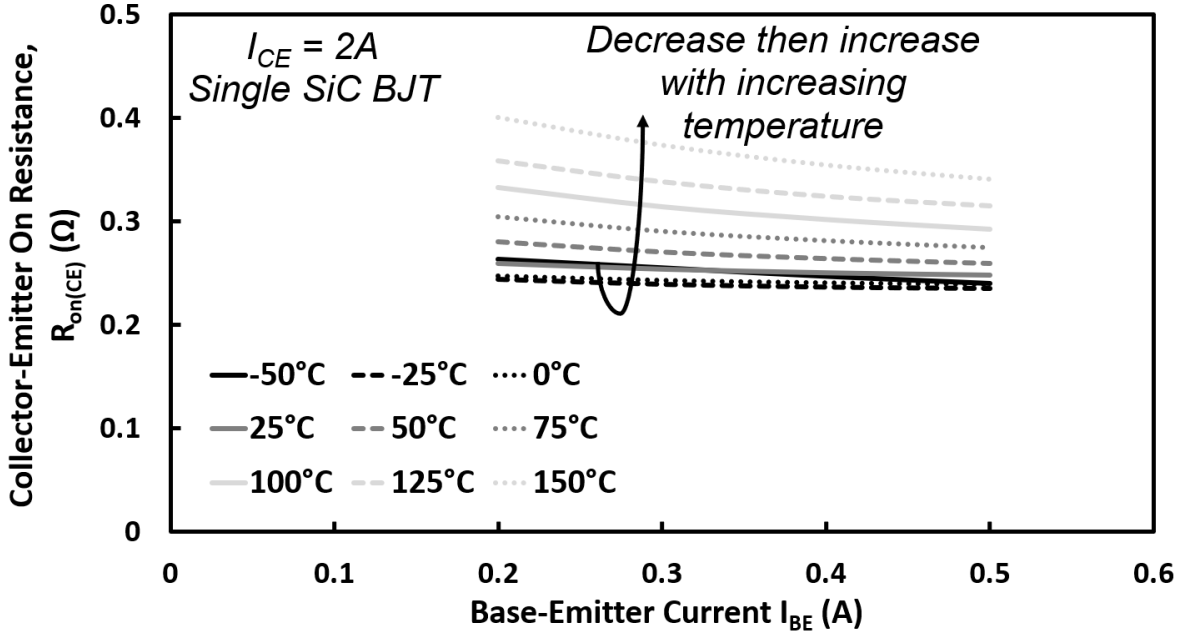

Figure 4.37: On-state resistance for single SiC BJT at I_{CE} of 2 A under different chamber temperatures.

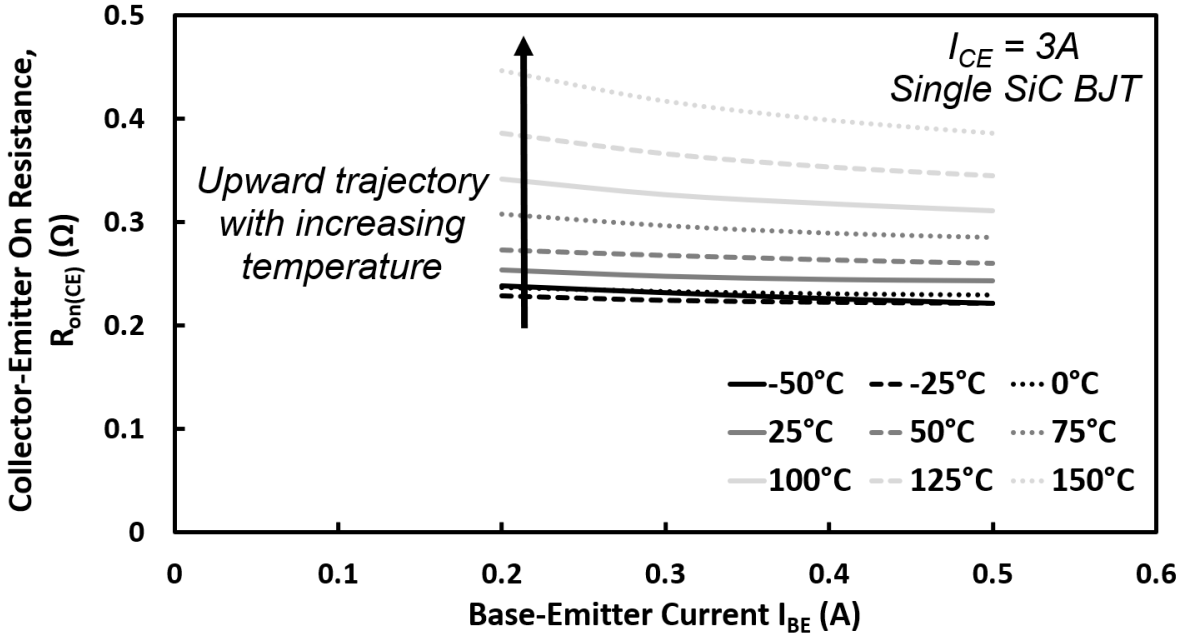

Figure 4.38: On-state resistance for single SiC BJT at I_{CE} of 3 A under different chamber temperatures.

4.4.3 Single BJT: Silicon vs. SiC

The on-resistance of Silicon BJT is found to be smaller than that of SiC BJT at collector current of 1 A. This arises due to the sufficient base current to maintain the quasi-saturation mode of operation leading to good conductivity modulation of the drift region. Fig. 4.39 to Fig. 4.41 shows such comparison at 3 A. The insufficient base current of Silicon BJT switches the device to the high resistance active mode, which is mitigated and outperforms SiC BJT at large base currents. Nevertheless, the invariance of the on-state resistances of SiC BJT means that a lower base current can be used to reduce losses in the driver.

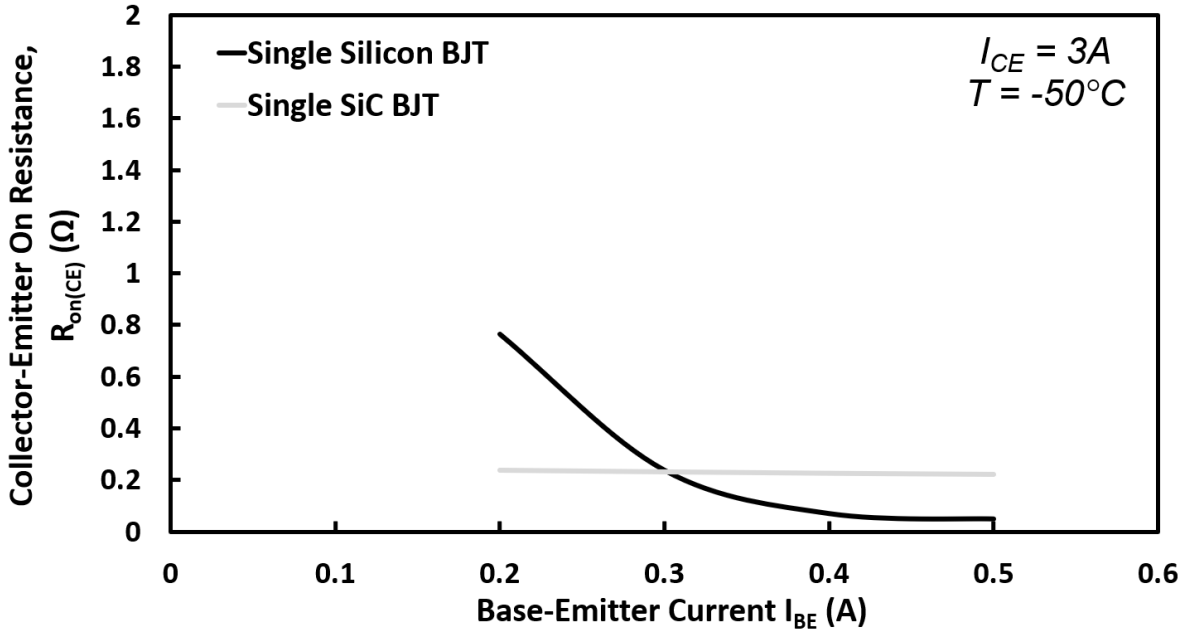

Figure 4.39: Comparison of on-state resistance of single Silicon and SiC BJT at I_C of 3 A under −50°C.

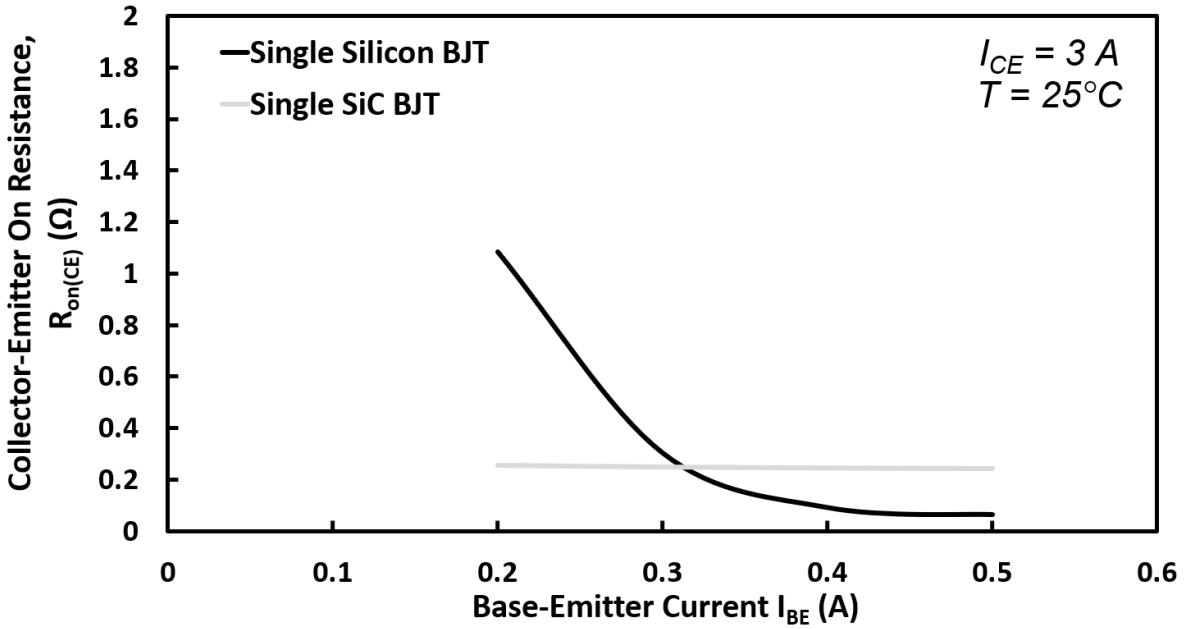

Figure 4.40: Comparison of on-state resistance of single Silicon and SiC BJT at I_C of 3 A under 25°C.

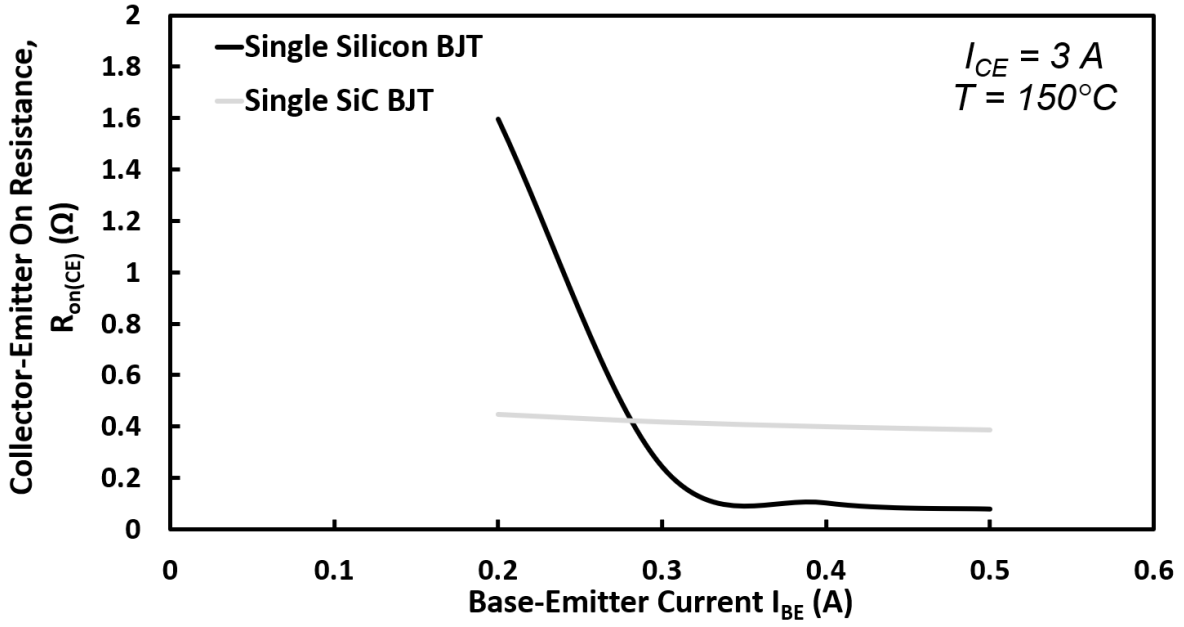

Figure 4.41: Comparison of on-state resistance of single Silicon and SiC BJT at I_C of 3 A under 150°C.

4.4.4 Paralleled Silicon BJTs

Fig. 4.42 to Fig. 4.44 shows the on-resistance of two-paralleled Silicon BJTs under various chamber temperatures at different collector currents. It can be seen that the parallel connection leads to the reduction of the on-resistance when compared with Single Silicon BJT. High temperatures further enhance the conductivity because of the worse heat extraction for the hotter device, while the higher collector currents result in the aggravated current mismatch to reduce the on-resistance. A turn-around of measurements is seen in Silicon BJTs where the resistance first slightly increases with temperature between −50°C to 0°C at low base current and then drops with further increase of temperature. This is because at low base current and low temperature the impact of additional carrier generation by temperature is very critical, however, as the temperature rises the role of reduced lifetime and mobility by scattering between carriers becomes more effective. For this reason at high base current the resistance always increase with temperature.

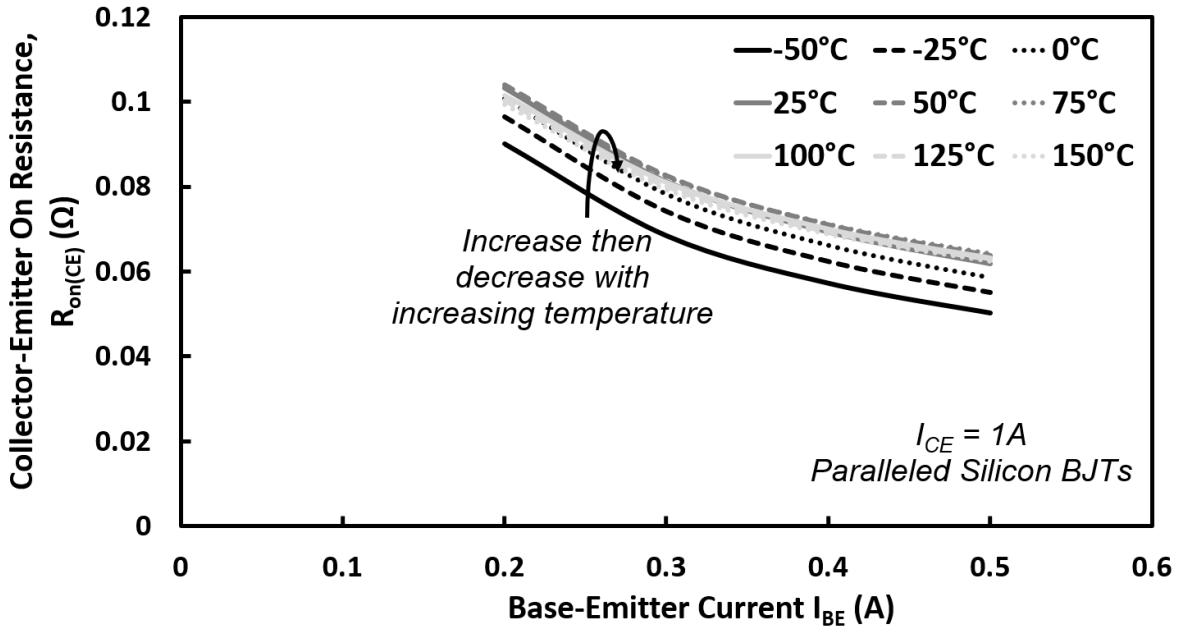

Figure 4.42: On-state resistance for paralleled Silicon BJTs at I_{CE} of 1 A under different chamber temperatures.

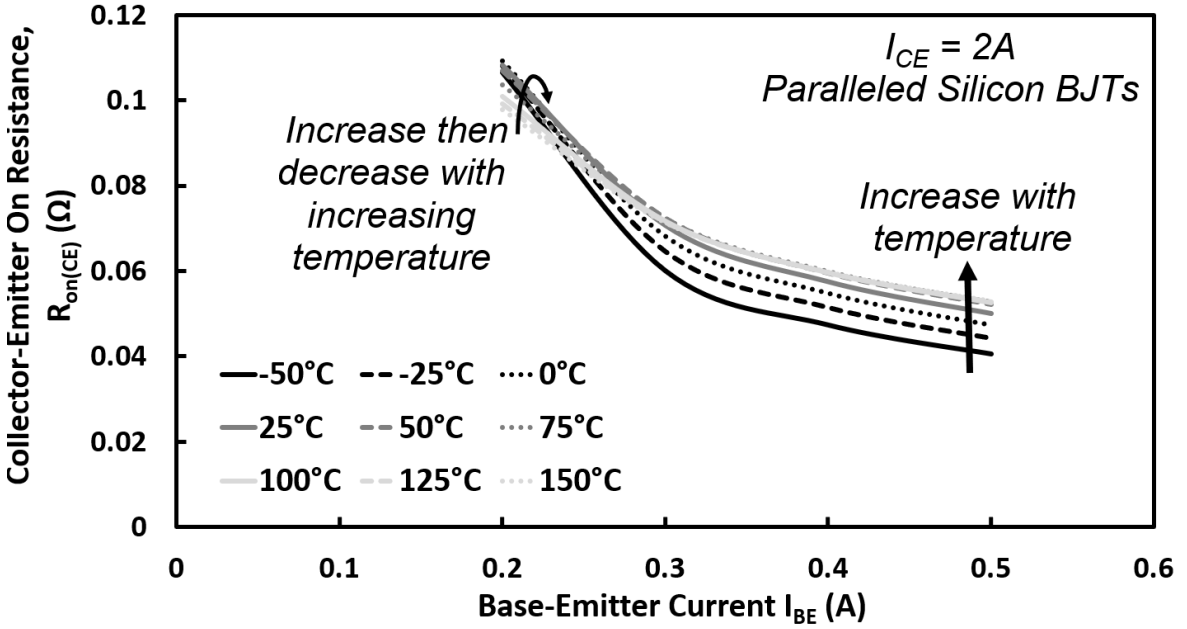

Figure 4.43: On-state resistance for paralleled Silicon BJTs at I_{CE} of 2 A under different chamber temperatures.

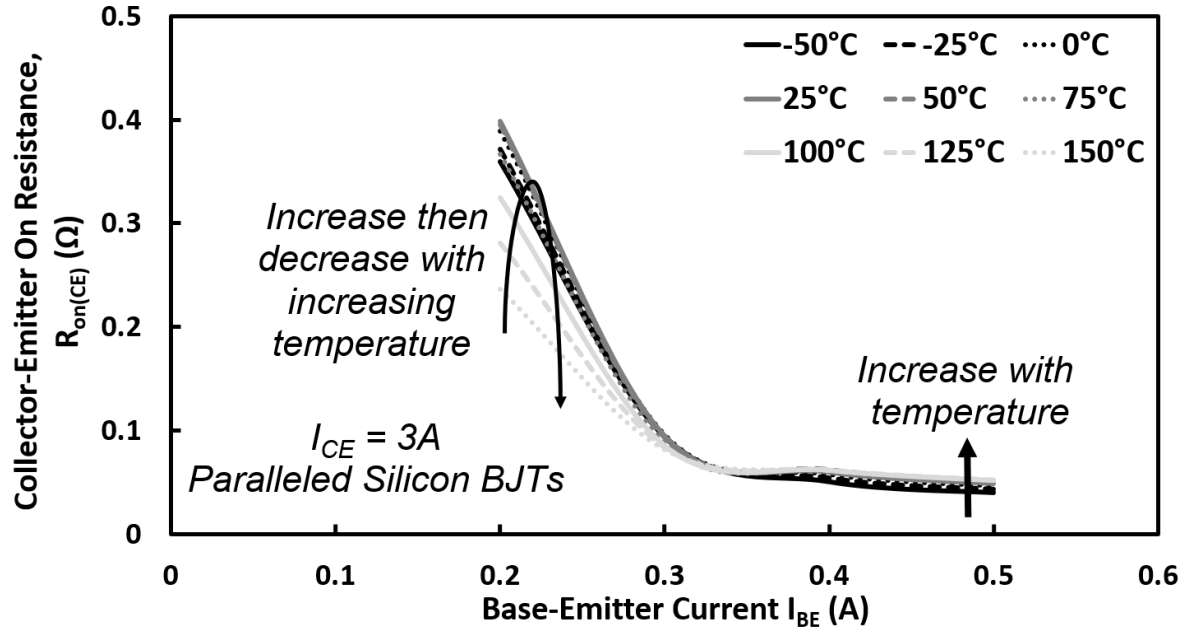

Figure 4.44: On-state resistance for paralleled Silicon BJTs at I_{CE} of 3 A under different chamber temperatures.

4.4.5 Paralleled SiC BJTs

Fig. 4.45 to Fig. 4.47 shows the on-resistance of two-paralleled SiC BJTs under various chamber temperatures at different collector currents. Parallel connection of SiC BJTs can reduce the on-resistance when compared with Single SiC BJTs. This is more pronounced in comparison with single Silicon BJT at low base current. Both the poor current balance at high collector currents and the poor heat extraction at high temperatures further impede the conductivity of paralleled SiC BJTs especially at low base current. Parallel-connected SiC BJTs introduce the stronger negative temperature dependence of on-resistance, albeit it occurs only at low temperatures ranging from −50°C to 0°C. The turn-around seen here is similar to what was seen in the Silicon BJT, where at low base current and low temperature the impact of additional carrier generation by temperature becomes more critical, though with the rise of temperature the role of reduced lifetime and mobility by scattering becomes more effective.

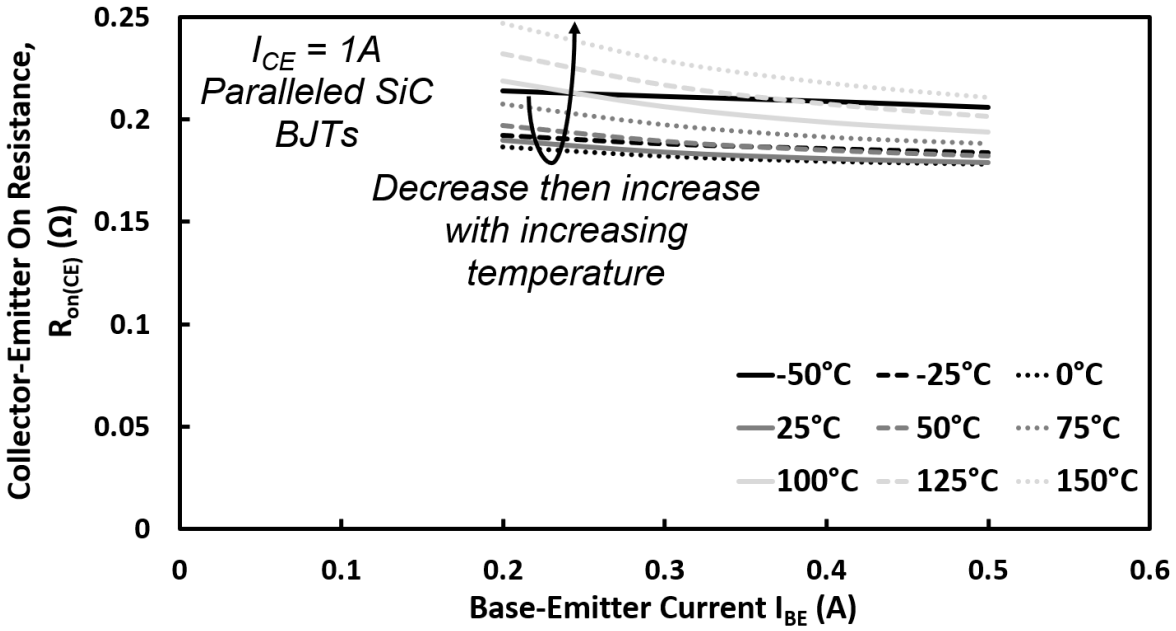

Figure 4.45: On-state resistance for paralleled SiC BJTs at I_{CE} of 1 A under different chamber temperatures.

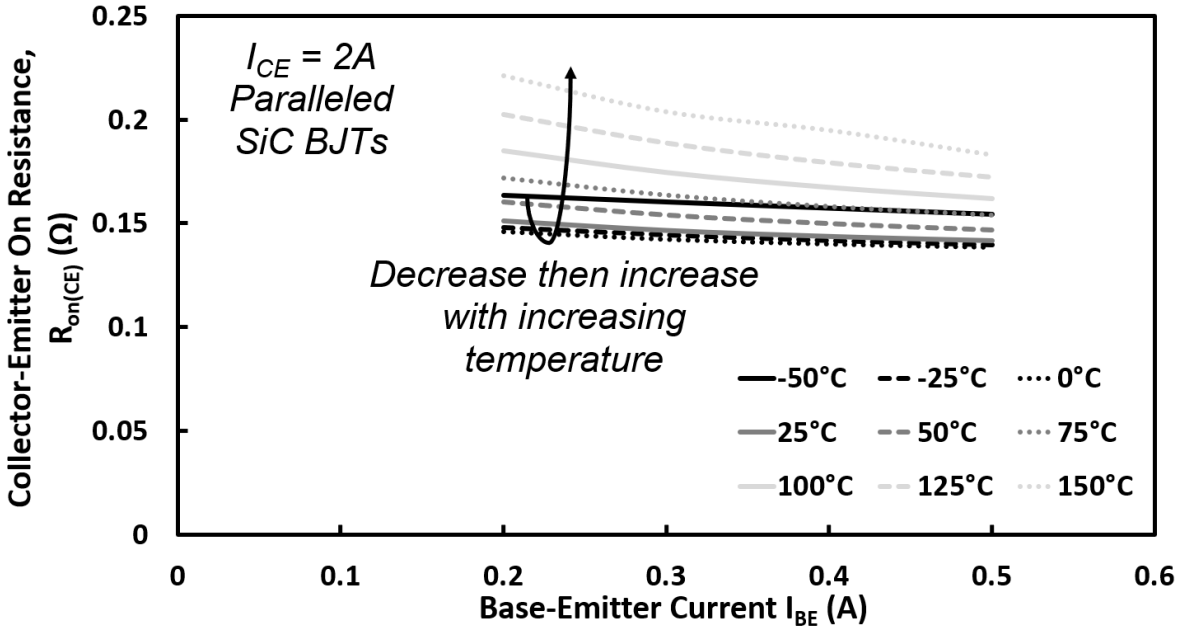

Figure 4.46: On-state resistance for paralleled SiC BJTs at I_{CE} of 2 A under different chamber temperatures.

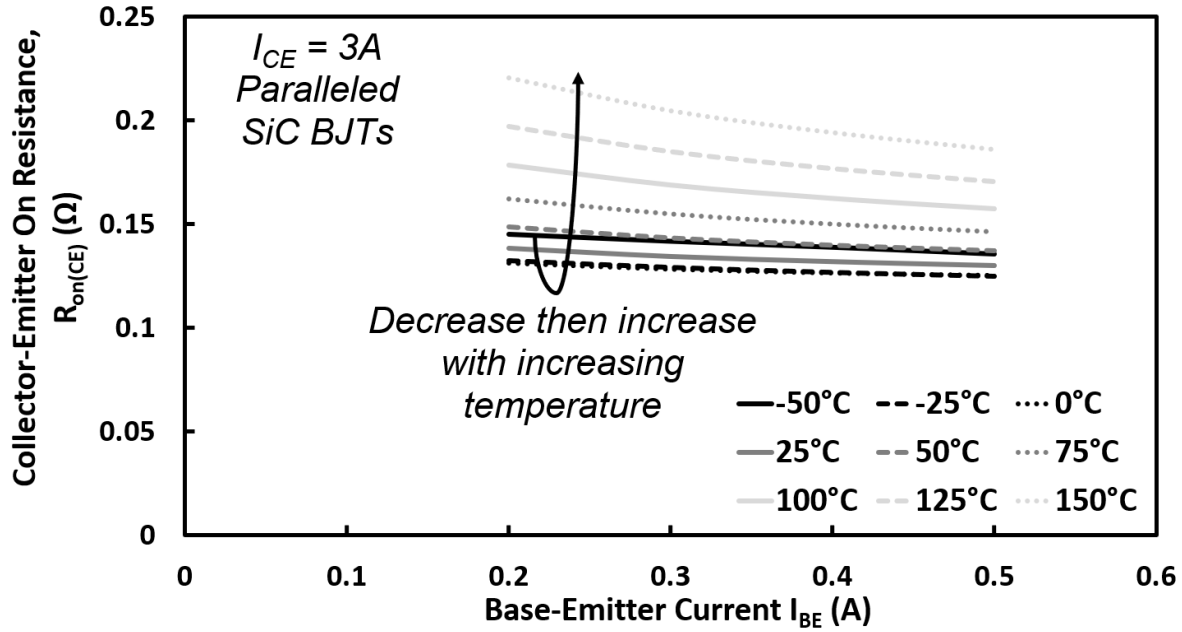

Figure 4.47: On-state resistance for paralleled SiC BJTs at I_{CE} of 3 A under different chamber temperatures.

4.4.6 Paralleled BJTs: Silicon vs. SiC

Similar to the comparison between single devices, the on-resistance of paralleled Silicon BJT is found to be smaller than that of paralleled SiC BJTs at a collector current of 1 A. The decrease of on-resistance with base current for paralleled Silicon BJTs, as shown in Fig. 4.48, indicates the gradual transition between the active mode and the quasi-saturation mode of operation. In general, parallel connection can promote the conductivity of both Silicon and SiC BJTs especially at elevated temperatures and at low base currents, where the on-resistance of single Silicon BJT at I_{base} of 0.2 A under 150°C is reduced by 1.36 Ω when connects in parallel. In essence, the same advantage seen in the single BJT section for the SiC device can be observed here, with the caveat that the base current is divided between two devices, leading to higher resistance per device and there is a slight decreasing trend with the base current.

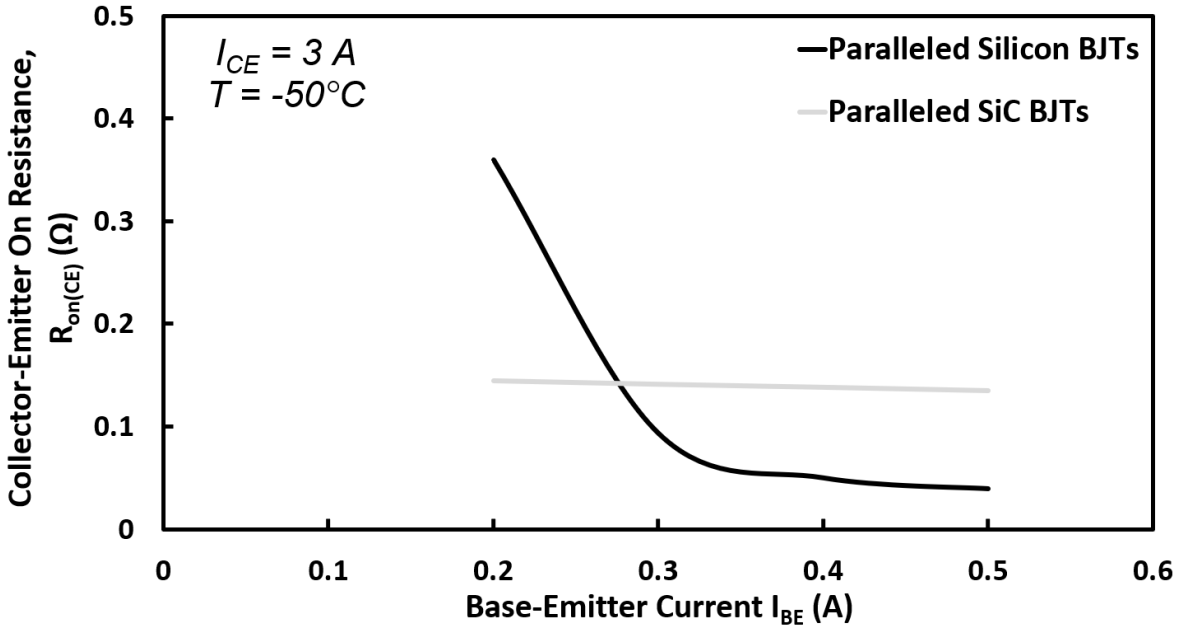

Figure 4.48: Comparison of on-state resistance of paralleled Silicon and SiC BJTs at I_C of 3 A under −50°C.

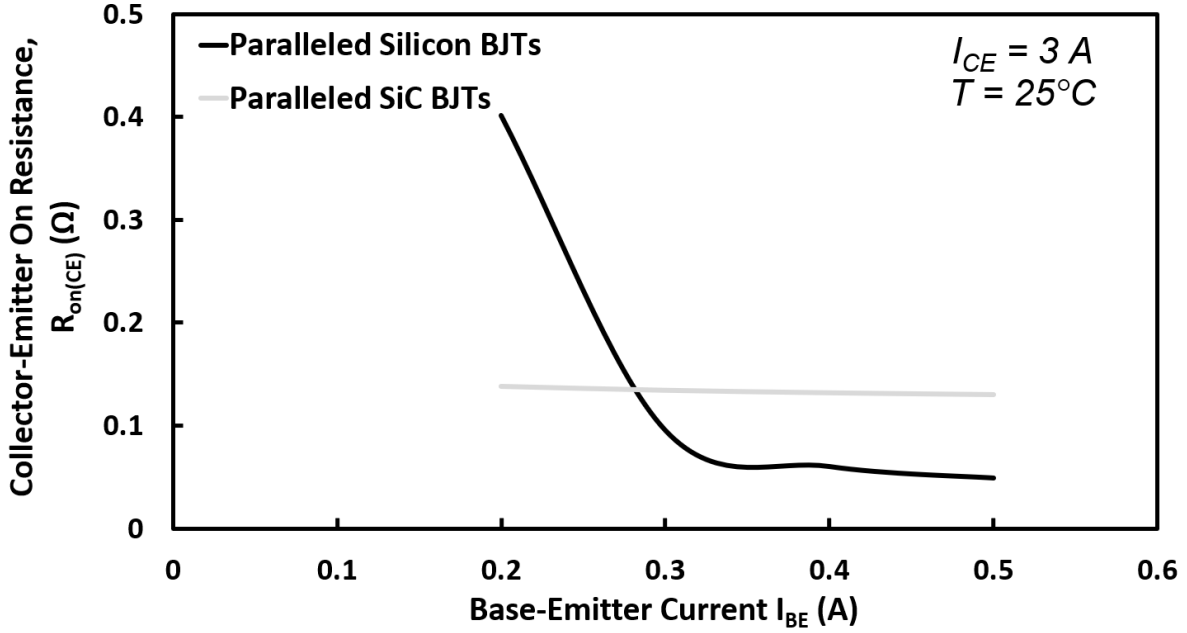

Figure 4.49: Comparison of on-state resistance of paralleled Silicon and SiC BJTs at I_C of 3 A under 25°C.

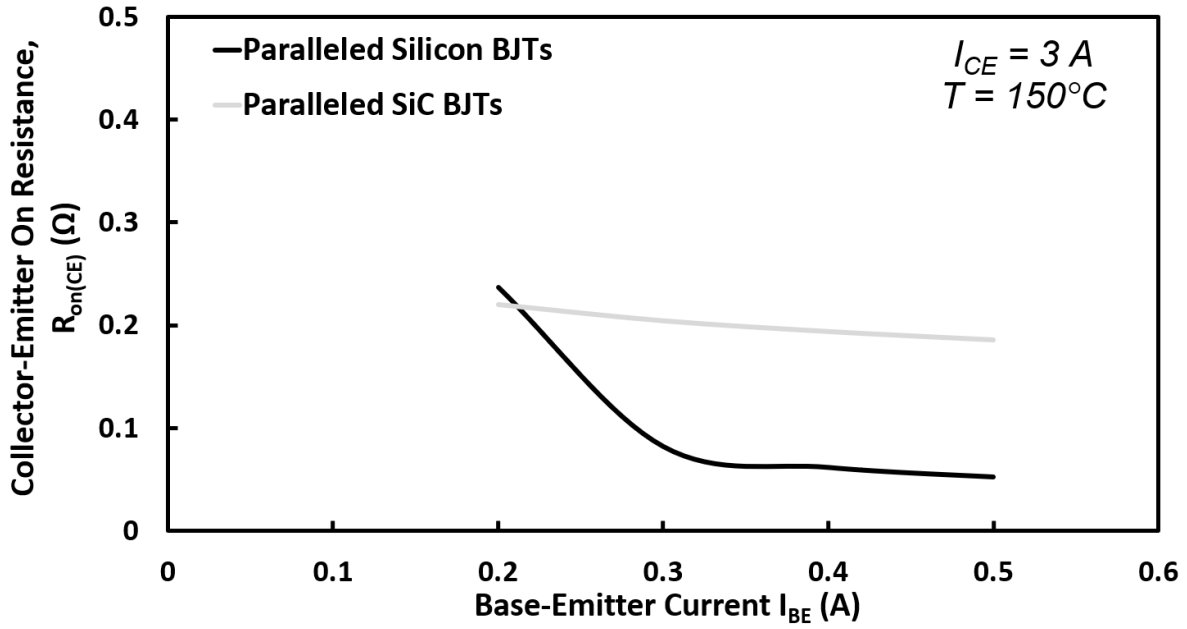

Figure 4.50: Comparison of on-state resistance of paralleled Silicon and SiC BJTs at I_C of 3 A under 150°C.

4.5 Forward Transfer Characteristics

To characterize the forward transfer characteristic, the Collector-Emitter current (I_{CE}) is measured while sweeping the Base-Emitter voltage (V_{BE}) from 0 to 4 V in 0.05 V increment while fixed Collector-Emitter voltage (V_{CE}) of 0.3 V is used. The temperature is increased from −50°C to 150°C and the forward characteristics are measured and plotted.

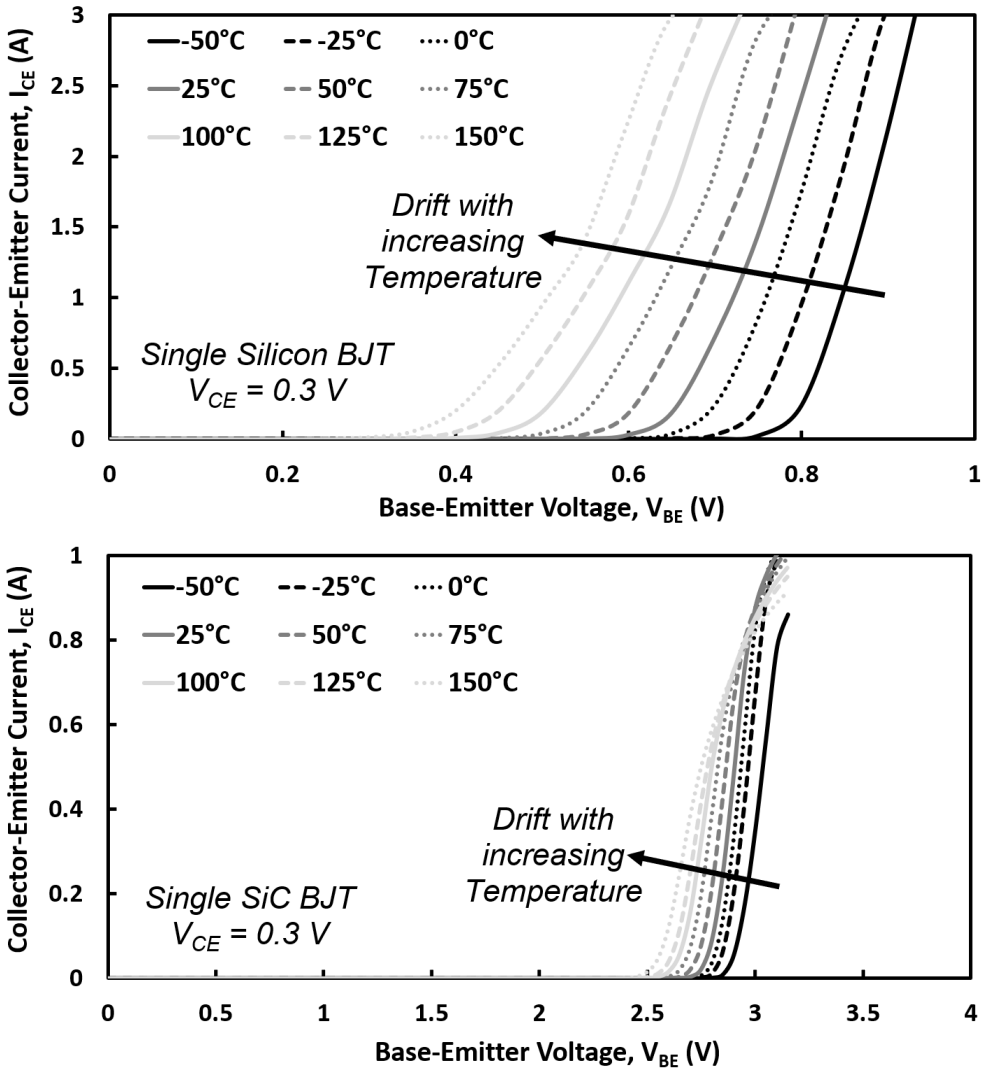

Figure 4.51: Forward transfer characteristics for single (A) Silicon BJT and (B) SiC BJT under different chamber temperatures.

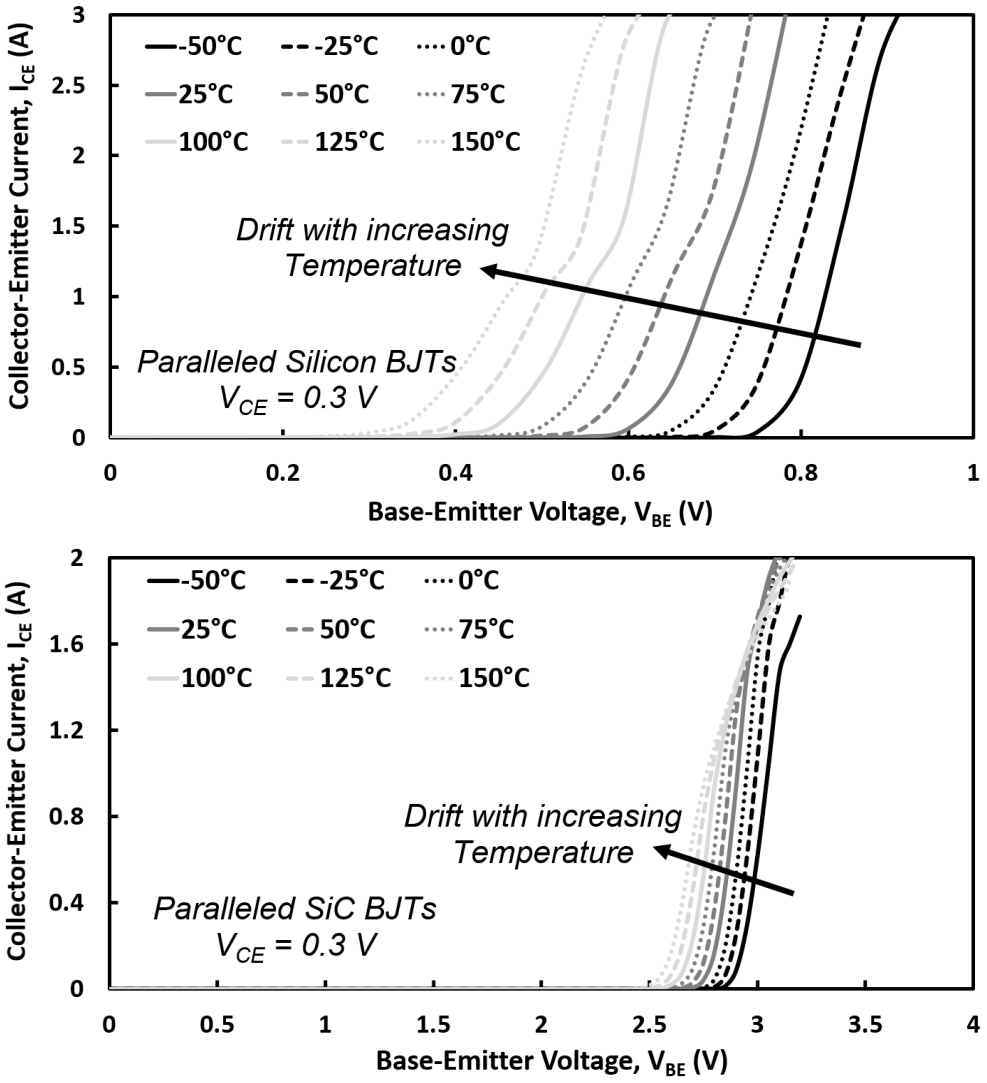

Figure 4.52: Forward transfer characteristics for paralleled (A) Silicon BJTs and (B) SiC BJTs under different chamber temperatures.

Fig. 4.51 to Fig. 4.53 show the transfer characteristic measured for the Silicon BJT and SiC BJT under various chamber temperatures for single device and paralleled devices, respectively. The BJTs start to conduct current when the Base-Emitter voltage becomes larger than the built-in voltage to forward-bias the Base-Emitter junction. The smaller built-in voltage in Silicon BJTs when compared to SiC BJTs stems from the much higher

intrinsic carrier concentration as discussed in Section. 2.3 which as a results of its narrow bandgap of 1.12 eV compared with 3.26 eV in 4H-SiC. Both Silicon and SiC devices exhibit a lower built-in voltage at high temperatures since the intrinsic carrier concentration increases with temperature, while the temperature increase from −50°C to 150°C reduces the Base-Emitter voltage by 0.4 V in both cases of Silicon and SiC devices, though this is seen as a more pronounced impact on the Silicon device due to its low base voltage.

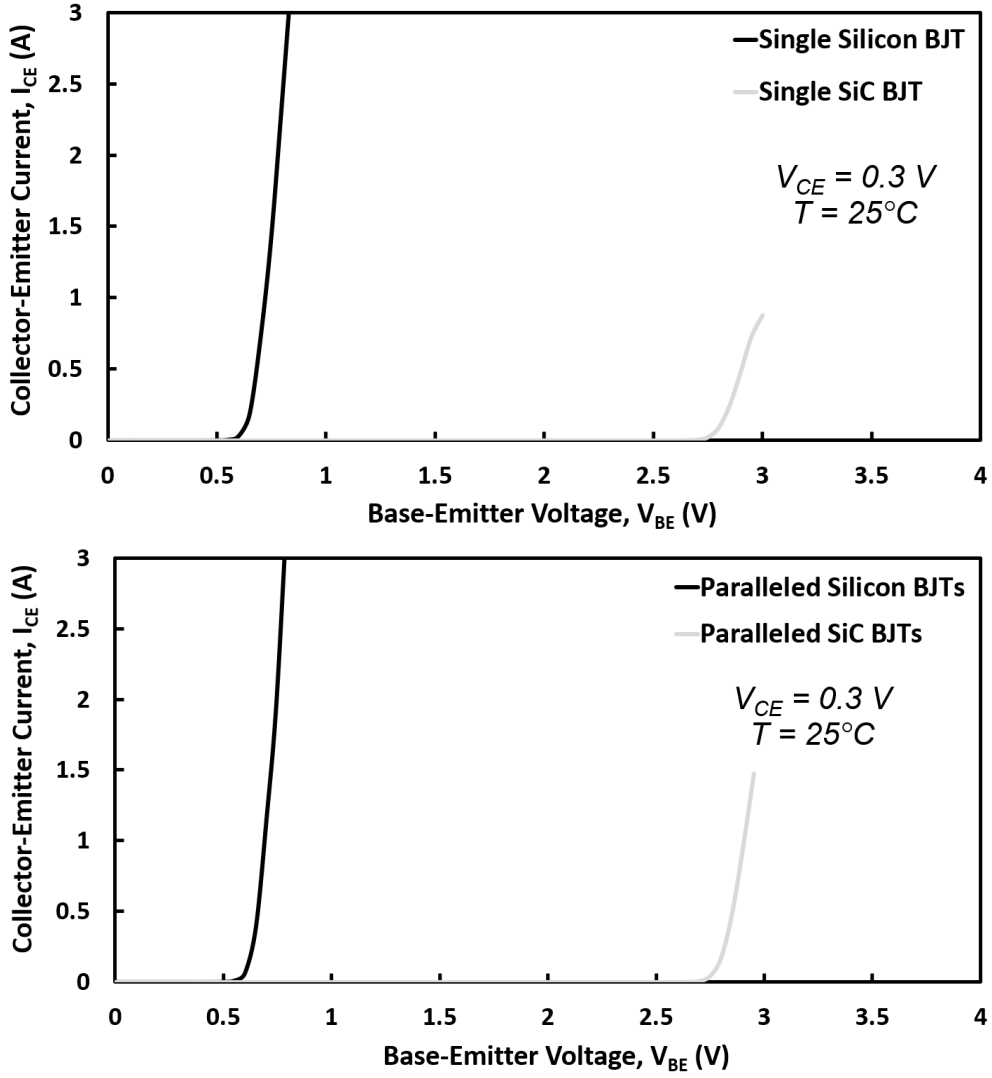

Figure 4.53: Transfer characteristics of Silicon vs. SiC BJTs in single & paralleled connection.

4.6 Reverse Base-Emitter Leakage Current

To determine the voltage blocking capability of the Base-Emitter junction, the reverse Base-Emitter current (I_{RBE}), which is also referred to as the Base-Emitter current (I_{EB}), is measured when sweeping the Base-Emitter voltage from 0 to 20 V in the negative direction. The collector terminal is open-circuited. The measurements are done between −50°C to 150°C and for both cases of single and paralleled devices.

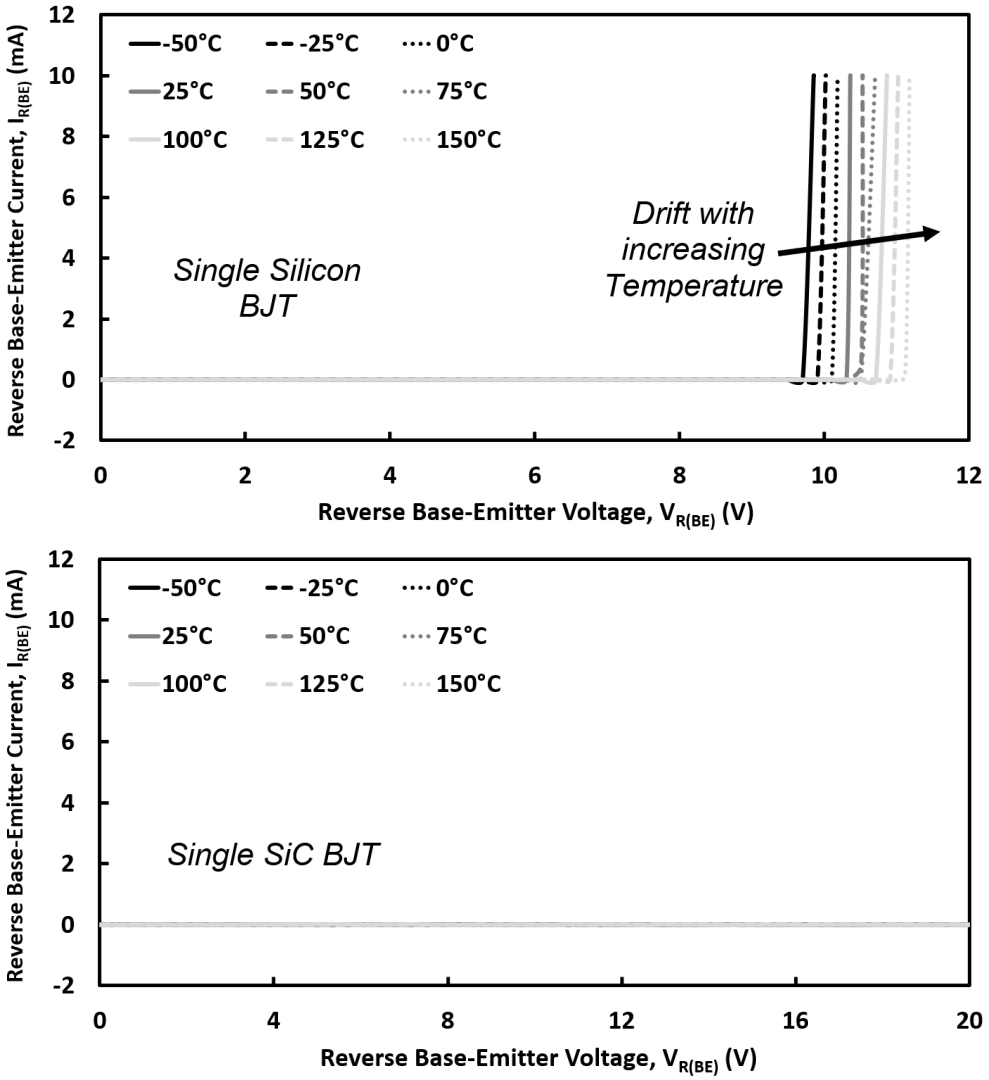

Figure 4.54: Base-Emitter leakage current for single (A) Silicon BJT and (B) SiC BJT under different chamber temperatures.

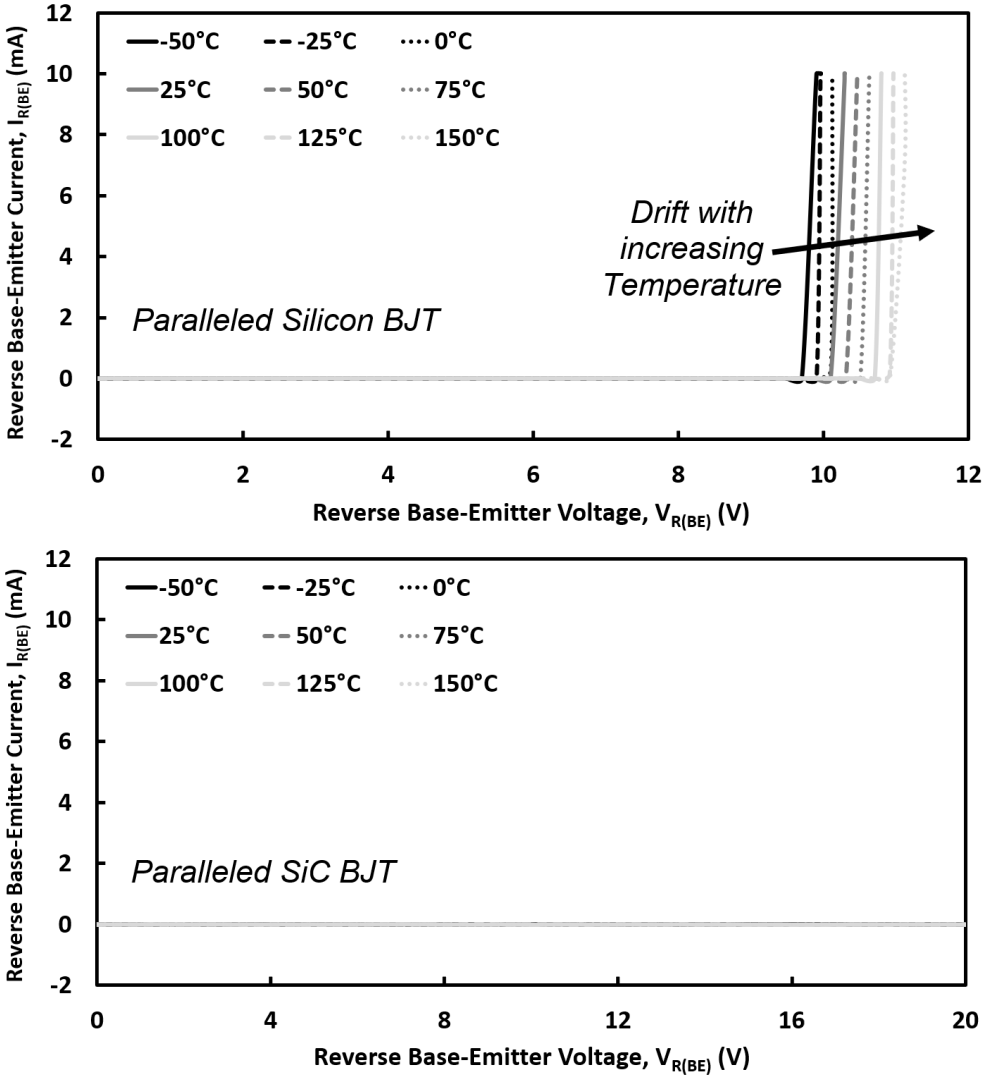

Figure 4.55: Base-Emitter leakage current for paralleled (A) Silicon BJTs and (B) SiC BJTs under different chamber temperatures.

Fig. 4.54 to Fig. 4.56 show the reverse Base-Emitter current of Silicon BJT and SiC BJT under various chamber temperatures for single device and paralleled devices, respectively. The much higher breakdown voltage in SiC BJTs than that in Silicon BJTs is because they can withstand a much higher electric field before initiating the avalanche breakdown. The incomplete ionization of SiC further promotes the voltage-blocking ca-

pability since the low-doped base region allows further expansion of the electric field on this side of the Base-Emitter junction even though it is much narrower than the case of the Silicon device. The positive temperature dependence of the breakdown voltage of Silicon BJTs can be explained by the fact that the movement of free carriers is restricted by the collision with atoms at high temperatures [1, 30, 61], which in turn generates less electron-hole pairs and thus less leakage current, noting that in Silicon almost all dopants are ionized in room temperature.

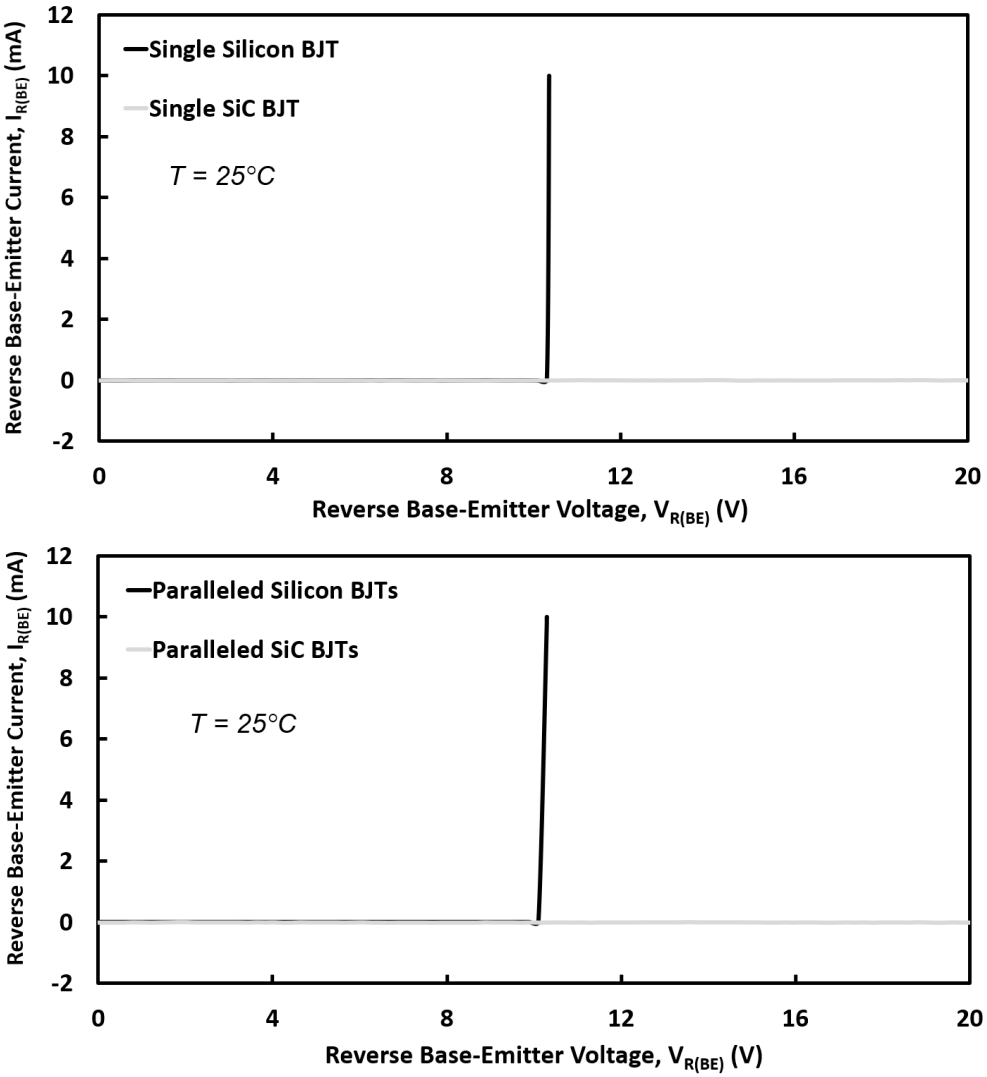

Figure 4.56: Base-Emitter leakage current of Silicon vs. SiC BJTs in single & paralleled connection.

4.7 Applications

In real applications, the Current imbalance between paralleled BJTs can lead to reliability problems. The Differences in the electrical and thermal parameters of the individual devices always hold true even though they may share the same part number or be fabricated from the same batch. The low-resistance device under parallel connection attracting more current becomes hotter and requires more current if this device exhibits a PTC for the current gain (or NTC for on-resistance), while the cooler device requires less current [92, 93]. Such positive feedback loop can result in thermal runaway until the destruction of the device.

Here it is shown that the current gain of Silicon BJT has improved at high temperatures. Thanks to the parallel connection, the current gain and the conductivity of Silicon BJTs are further enhanced together with their temperature coefficient. However, SiC BJTs are favourable for long-term operation since the negative temperature coefficient counteracts the decrease of on-resistance with temperature and thus suppresses the current imbalance between paralleled devices.

4.8 Summary

This chapter explored the static characteristics of the single commercially available SiC BJT and two paralleled SiC BJTs by means of extensive experimental measurements, as well as to compare with the similarly rated single Silicon BJT and paralleled Silicon BJTs. The onset of reverse breakdown at Base-Emitter junction in Silicon BJTs is because of the low critical electric field when compared with SiC BJTs. During the forward transfer characteristic test, the larger built-in voltage of Base-Emitter junction in SiC BJTs is

found to ensure the low on-resistance quasi-saturation mode operation which holds also for Silicon BJTs only at high base currents.

When adequate base currents are applied to the Silicon BJTs, the conductivity modulation plays a determining role to reduce their on-resistance to be lower than that in SiC BJTs. However, SiC BJTs require a lower base current to operate with low on-resistance. In terms of the DC common-Emitter current gain, the much higher current gain of SiC BJTs is compromised and becomes lower than that in Silicon BJT at elevated temperatures. This stems from the negative temperature coefficient of the current gain in SiC BJTs and the positive temperature coefficient in Silicon BJTs. It can also be observed that the current gain increases with base current for SiC BJTs while decreases with base current for Silicon BJTs.

Parallel connection is found to promote both the conductivity and current gain for Silicon devices, this also leads to lower on-resistance in paralleled SiC BJTs when compared with the single device whereas the current gain is reduced in parallel configuration. Nevertheless, SiC BJT may become preferable to be connected in parallel from the reliability point of view since the negative temperature dependence of on-resistance suppress the current imbalance and thermal runaway.

Chapter

5 Analysis of High Voltage Silicon Carbide JBS & MPS Diodes

The results published in journal paper 2 and conference paper 2, 3, & 4 in Publications list at the outset of the thesis are used in writing of this Chapter. I acknowledge the contribution of my supervisors for laying out the specific objectives, and my co-authors on the methodology and accuracy of the analysis. I have done the Measurements at Bristol's EEMG research laboratory, analysed the results and drafted the papers.

Power diodes are key components in power electronics converters in automotive and renewable energy sectors [94]. Experimental [95] and simulation-based [96] analysis of these devices have been at the center of power electronics research. Diodes are either Unipolar, i.e. Schottky diodes, or Bipolar, i.e PiN diodes.

Power rectifiers are used for high frequency and medium voltage applications as output diodes in Power Factor Correction (PFC) circuit [97] and freewheeling diodes in the Variable Frequency Drive (VFD) control circuit [1]. During the reverse recovery, the large reverse recovery current, especially in the PiN diode, not only produces significant power dissipation in the diode, but also impose substantial power dissipation to the Power switch, IGBT in the PFC and MOSFET in the VFD circuit, as the peak reverse recovery current of diode is also added to the power switch during the turn-on transient.

In some applications such as grid-level converters, power diodes can experience high voltage transients that they may be led into the avalanche rating conduction, and potentially failure [96], which has been discussed in Section 2.5.3. As discussed in the previous Section 2.5.4, DC faults can lead to overcurrent in antiparallel diodes.

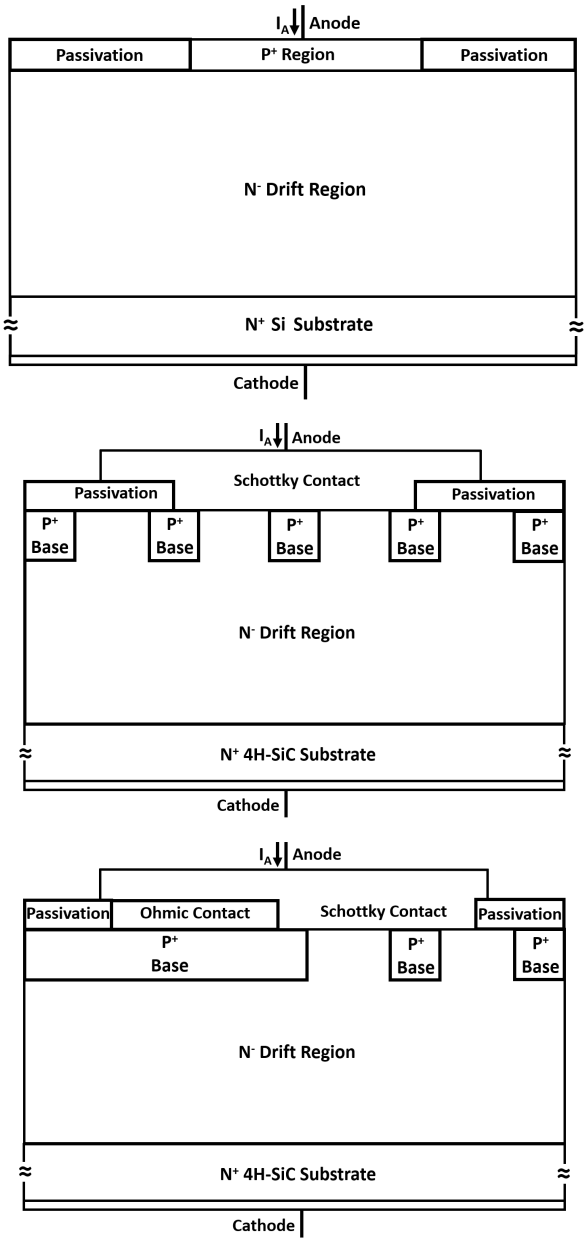

Figure 5.1: Simplified device structures for Silicon PiN, SiC JBS and SiC MPS diodes, respectively.

This chapter explores the switching performances and static characteristic of SiC MPS diode in contrast to Silicon PiN and SiC Junction Barrier Schottky (JBS) diode, the reverse recovery current and on-state voltage drop are characterized in a wide range of temperature ranged from 25°C to 175°C. This chapter also explores the surge current ruggedness of commercially available SiC MPS diodes in contrast to closely rated Silicon PiN and SiC JBS diode, the single event avalanche performance of these three devices is also evaluated by means of experimental measurements. Section 5.1 provides the dynamic switching transients of the three diode rectifiers seen in experimental results while section 5.2 analyses the static performance following with the UIS test-results in section 5.3 and the surge current performance analysis in section 5.4. Table. 5.1 includes the key parameters of the three diodes to be used for studies in this chapter.

Table 5.1: Electrical parameters of the three diodes under test at T= 25°C.

	Silicon PiN	4H-SiC JBS	4H-SiC MPS
Model	DSI30-12A	C4D20120A	GC20MPS12-220
Manufacture	IXYS	CREE	GeneSiC
Blocking Voltage	1200 V	1200 V	1200 V
Forward Current	30 A at 130°C	26 A at 135°C	30 A at 135°C
Leakage Current	40 μA	200 μA	10 μA

5.1 Dynamic Performance

The dynamic performance of Silicon PiN, SiC JBS and SiC MPS diode have been investigated through a wide range of experimental measurements. All the devices are TO-220 packaged. These power rectifiers are tested on a double-pulse testing board shown in Fig. 2 with a N-channel SiC power MOSFET SCT3160KL acting as power switch. The

design of this PCB is shown in Appendix B. This SiC MOSFET is driven by a gate driver generating output voltage in a range between +15 V and 0 V. The gate resistance (R_G) provided in Fig. 5.2 is increased from 10 to 100 Ω to adjust the switching speed of the MOSFET while the operation temperature of diodes rises from 25°C to 175°C in 25-degree increments via ITC-100RL PID Temperature Controller. The length of the charging pulse (the first pulse) is adjusted through an Agilent 33220A 20 MHz arbitrary waveform generator to provide on-state current. The Drain-Source (DC-link) voltage (V_{DS}) applied to all power rectifiers is 650 volts. Although this is a low voltage and current application for all three devices which can sustain much higher forward currents, the voltage and current level is selected carefully after exploring many operating voltages to ensure the safe operation. Two GW-Instek GDP-100 100 MHz voltages probes and a CWT Ultra-mini 50 MHz Rogowski current coil (CWT1) are used to capture voltage and current waveforms while both are shown in a Keysight MSO7104 A 1-GHz 4 GSa/s oscilloscope.

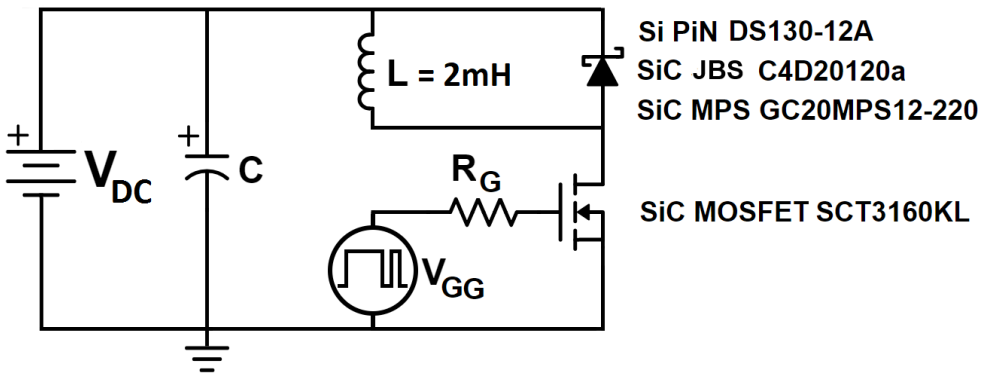

Figure 5.2: The switching performance test circuit for diode rectifiers.

Fig. 5.3 shows the double-pulse testing result including the turn-on/off switching transients of all three diodes. Since the power switch dominates the switching characteristic in the double pulse circuit, the current turn-off rate is same for all passive diodes. As also indicated in this figure, the reverse recovery process of Silicon PiN diode leads to extra

turn-off time while the absence of substantial stored charge in SiC JBS and MPS diode almost remove this process and thus switch faster with small ringing generated by the resonance between diode internal capacitance and load capacitance with the path stray inductance. The turn-off voltage is found to be lower than 650 V because of the low bank capacitance making its energy drop more evident.

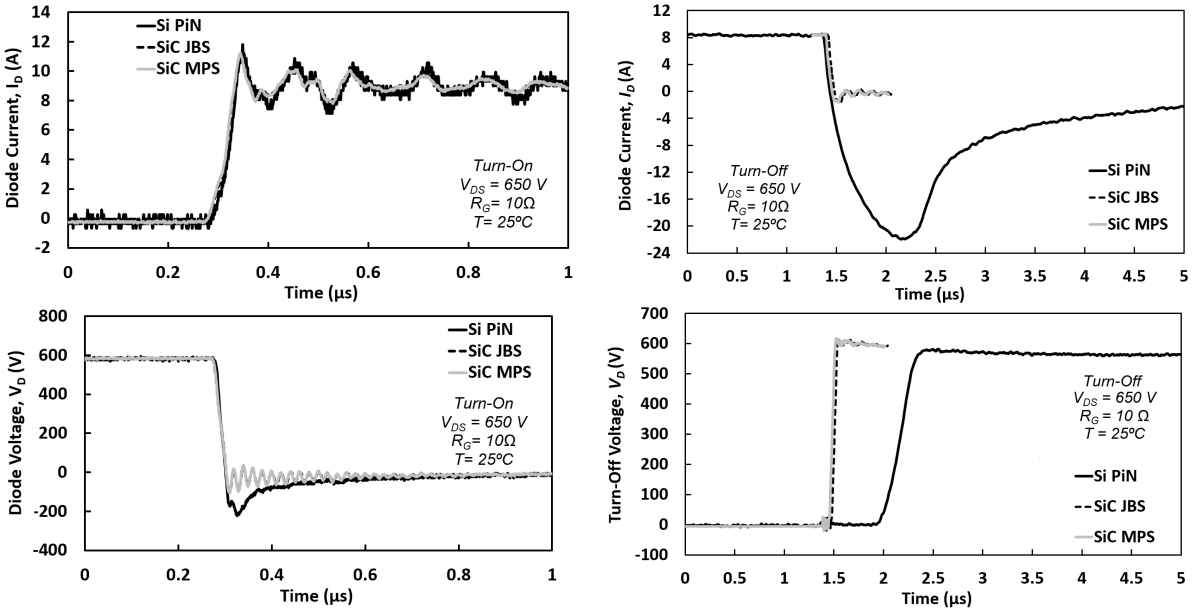

Figure 5.3: The diode current and diode voltage at turn-off for all three rectifiers at 25°C with DC-link voltage of 650 V.

The impact of operating temperature and switching speed on turn-off current transient can be seen in Fig. 5.4. It can be seen that the reverse current of both SiC JBS and MPS diodes are independent to temperature variations. The main reason is that the lack of reverse recovery charge in JBS and MPS which is dependent to temperature. The switching transients of JBS and MPS diode under various switching speed are also observed as a result of different gate resistances. This is because that the increasing gate resistance increases the RC time constant of the MOSFET and thus the slower switching [1, 17]. As for the voltage and current switching transient shown in Fig. 5.3,

the SiC JBS and MPS diode start to sustain voltage much earlier than Silicon PiN diode since the latter device is required to remove substantial amount of free carrier before it is capable of supporting voltage.

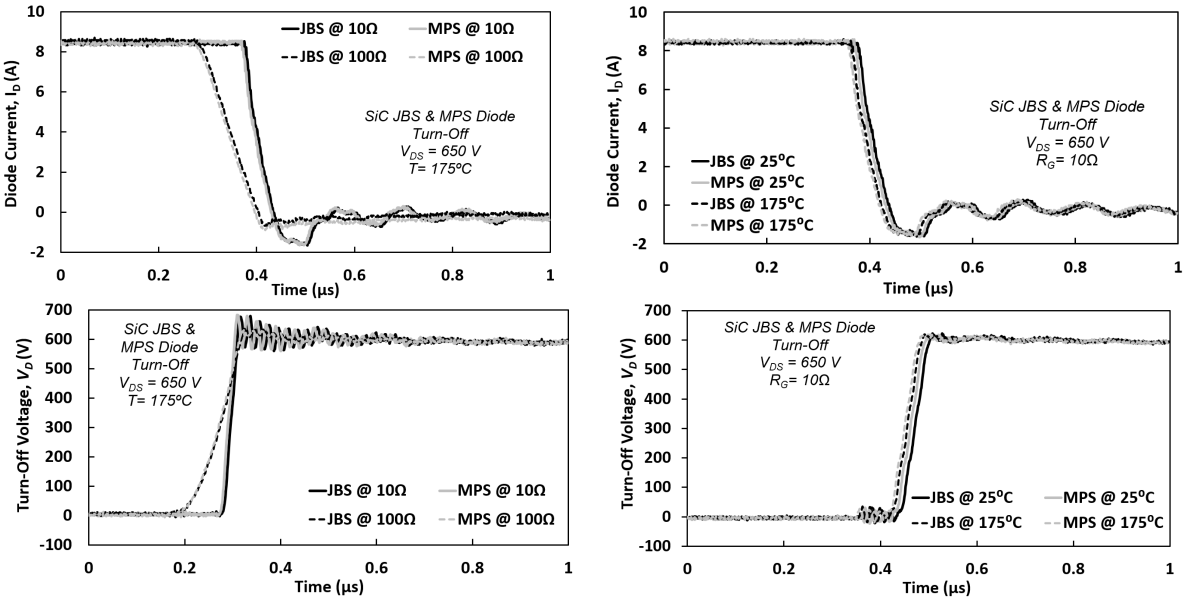

Figure 5.4: Turn-Off current and voltage with DC-link voltage of 650 V for SiC JBS & MPS diodes at 25 to 175°C and at 10 to 100 Ω.

Fig. 5.4 shows the current and voltage transition of the diodes, in which SiC JBS diode are almost identical to that of SiC MPS diode. The voltage ringing arises due to the parasitic inductance, which is mitigated by the slower switching speed.

Fig. 5.5 show the turn-on switching transient of current and voltage of the diodes. It is worth pointing out that the voltage ringing of SiC JBS and MPS diode is because of the parasitic inductance, which is mitigated by the slower switching speed. The turn-on current overshoot also stems from the parasitic capacitance, which is mitigated by the slower switching speed.

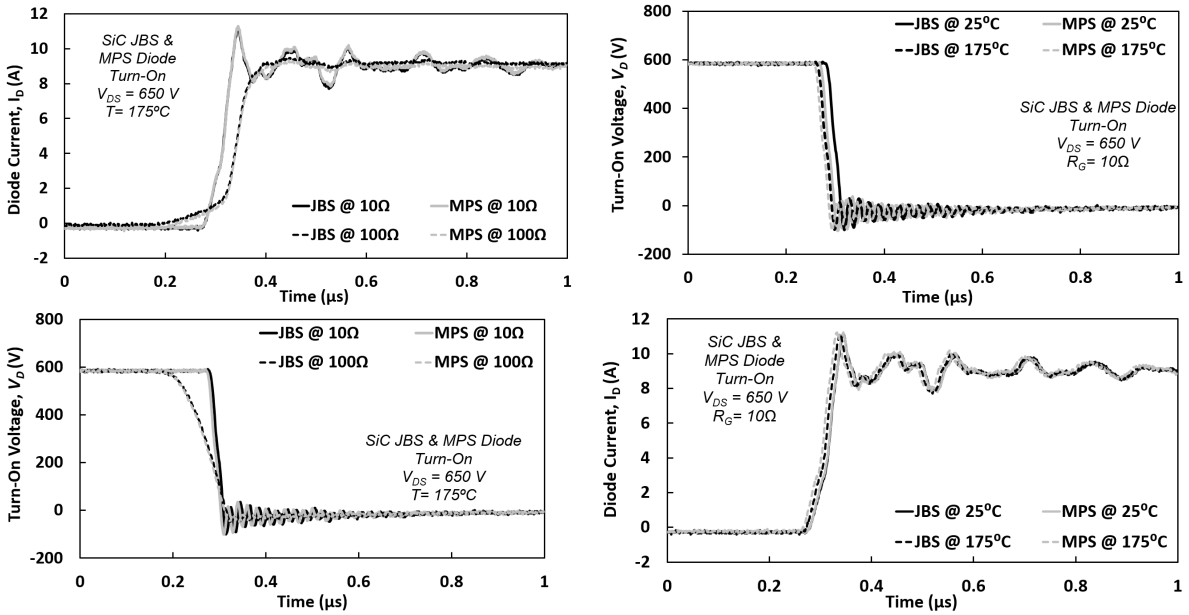

Figure 5.5: Turn-On current and voltage with DC-link voltage of 650 V for SiC JBS & MPS diodes at 25 to 175°C and at 10 to 100 Ω.

5.2 Static Performance

The Static performance of Silicon PiN, SiC JBS and SiC MPS diode have also been characterized. In this case, same power rectifiers are tested on a static tests circuit shown in Fig. 5.6 with the same power switch. Unlike the configuration for previous measurements, this SiC MOSFET connected in series to diodes is used to accurately control the current conduction time through the diode under test while the same MOSFET driver is used. The gate resistance used for the gate driver circuit is 10 Ω for enabling the fastest dynamic switching transient to minimize the switching power losses while the operation temperature rises from 25°C to 175°C in 25-degree increments via the aforementioned Temperature Controller. The ELC ALR3206D power supply outputs the on-state current ranged from 1-6 A in 1 A increments while the conducting period of 3 s for all three diodes is set by the waveform generator. Tektronix current probe model TCP312 in conjunction

with a probe amplifier model TCPA300 was used for measuring the diode currents while a JAMECO P6100 100 MHz voltage probe was used to measure the diode voltage.

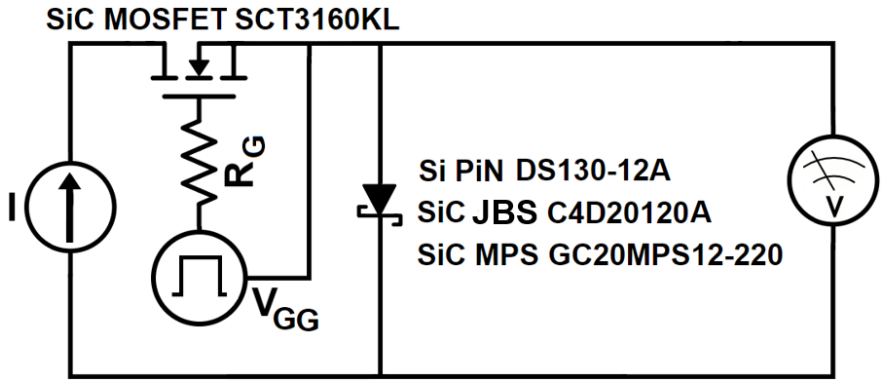

Figure 5.6: The Static test circuit for on-state measurements of the rectifiers.

5.2.1 Low Current Measurements

Fig. 5.7 shows the voltage drop of three diode rectifiers under the conduction mode. It is observed that the on-state voltage of SiC JBS and MPS diode is larger than that of Silicon PiN diode because of the higher built-in voltage of SiC devices due to the much lower intrinsic carrier concentration even though the P-N junction usually exhibits a higher voltage than that for Schottky junction. Fig. 5.7 shows that the decrease of the on-state voltage during the conduction mode for Silicon PiN diode as the junction voltages plays important role during self-heating because of the positive temperature coefficient of the intrinsic carrier concentration which is inverse related to the junction voltage [98].

In the case of SiC JBS and MPS diode, the forward voltage decreases with increasing temperature due to increased thermionic emission of electrons across the Schottky contact barrier height. Temperature dependence of on-state voltage is shown in Fig. 5.8, which shows that Silicon PiN diode exhibits a negative temperature coefficient for the on-state voltage drop as expected because of the temperature dependence of junction voltage.

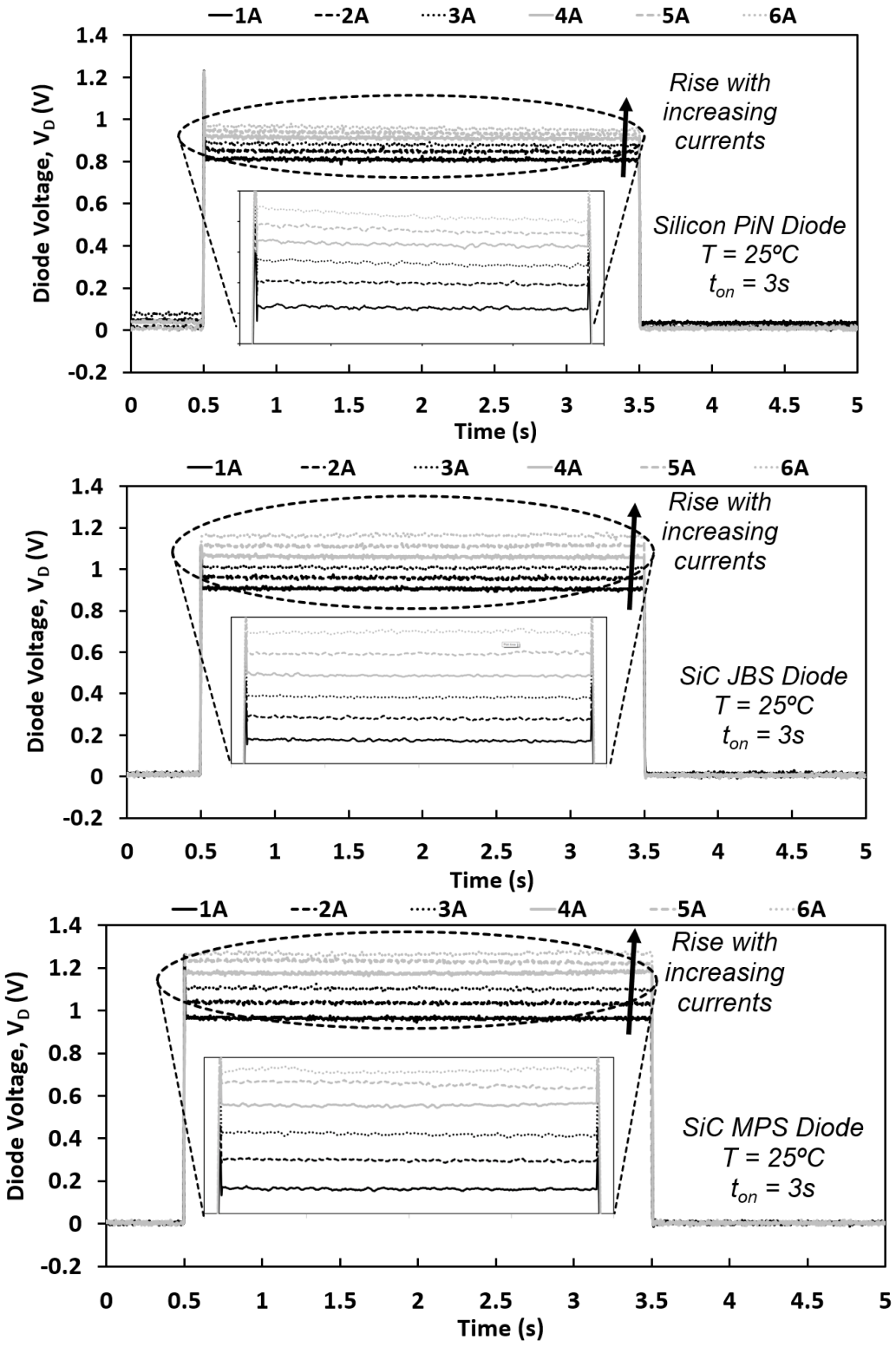

Figure 5.7: On-state voltage during self-heating for all three devices with ambient temperature of 25°C and for each of Silicon PiN, SiC JBS and SiC MPS diodes at various current levels up to 6 A.

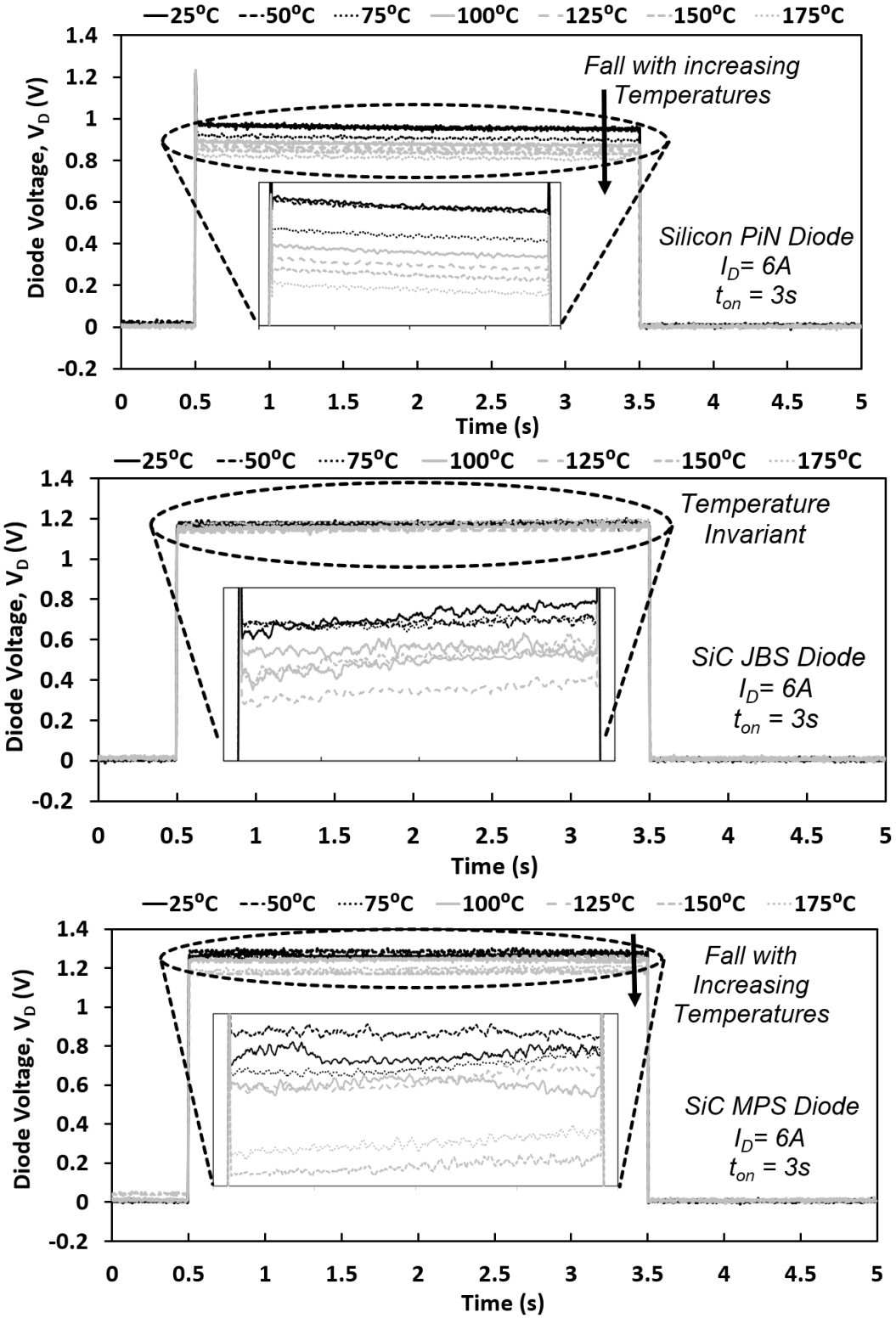

Figure 5.8: On-state voltage during self-heating with 6 A for (a) Silicon PiN, and for (b) SiC JBS and for (c) SiC MPS diode at various operating temperatures.

The on-state voltage of SiC JBS diode decreases with increasing of temperature from 25°C to 125°C but increases with increasing of temperature from 125°C to 175°C at high temperatures. This is because of the voltage drops across the drift resistances become dominant with the increasing temperature, hence, the total on-state voltage increases with temperature at high temperatures. The negative temperature dependence of MPS diode means that the junction voltage dominates the forward voltage at 6 A. Since the diode current under test is lower than that shown in table. 5.1, the on-state current has been increased to investigate the temperature dependence of diode voltage at high currents, and to validate the existence of conductivity modulation.

5.2.2 High Current Measurements

For high current Static measurements, the same static test circuit is used while the C4D20120A SiC JBS diode is replaced by a 1200 V/26 A SiC JBS diode with reference C4D10120H, the DSI30-12A Silicon PiN diode is replaced by a 1200 V/30 A Silicon PiN diode with reference DSEP30-12B due to chip shortages. The diode current is now linearly increased from 5 A to 20 A in 5 A steps. Although the on-state voltage of the new Silicon PiN diode is higher than that of its counterparts, as shown in Fig. 5.9 and 5.10, due to the different device structure, the conductivity modulation effect is observed since a less voltage increment is observed at high currents. The improved conductivity modulation effect in Si PiN diode is observed at 175°C from Fig. 5.11 where the on-state voltage further reduced. This is in-line with the trend expected by Eq. 2.13. However, minor conductivity modulation effect is observed in SiC JBS and MPS diode at low and high temperature. This is because of the large built-in voltage of the SiC P-N junction (about 3 V) when compared with the conduction state voltage from experiments.

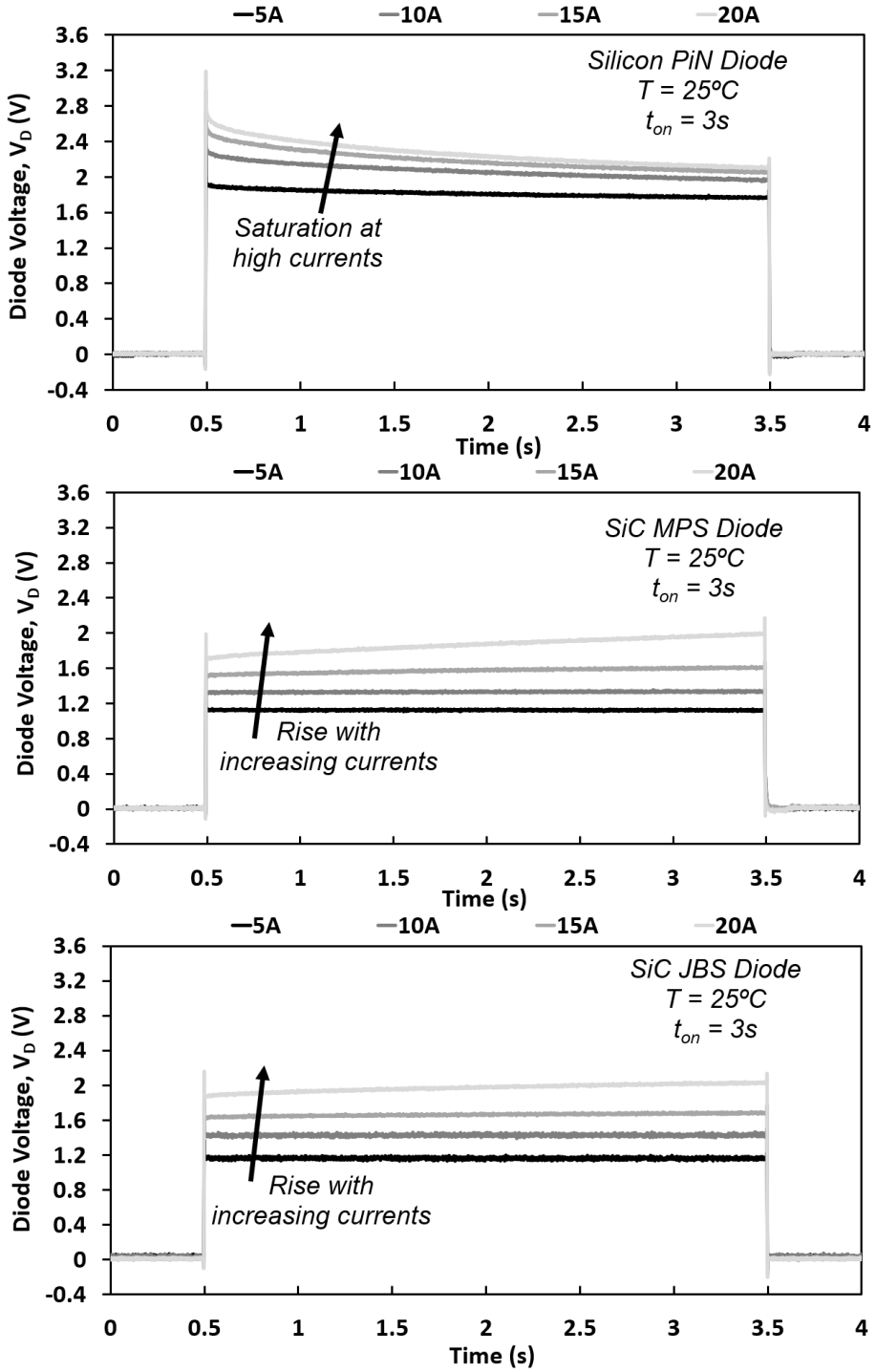

Figure 5.9: On-state voltage during self-heating for all three devices with temperature of 25°C and for each of Silicon PiN, SiC JBS and SiC MPS diodes at various current levels up to 20 A.

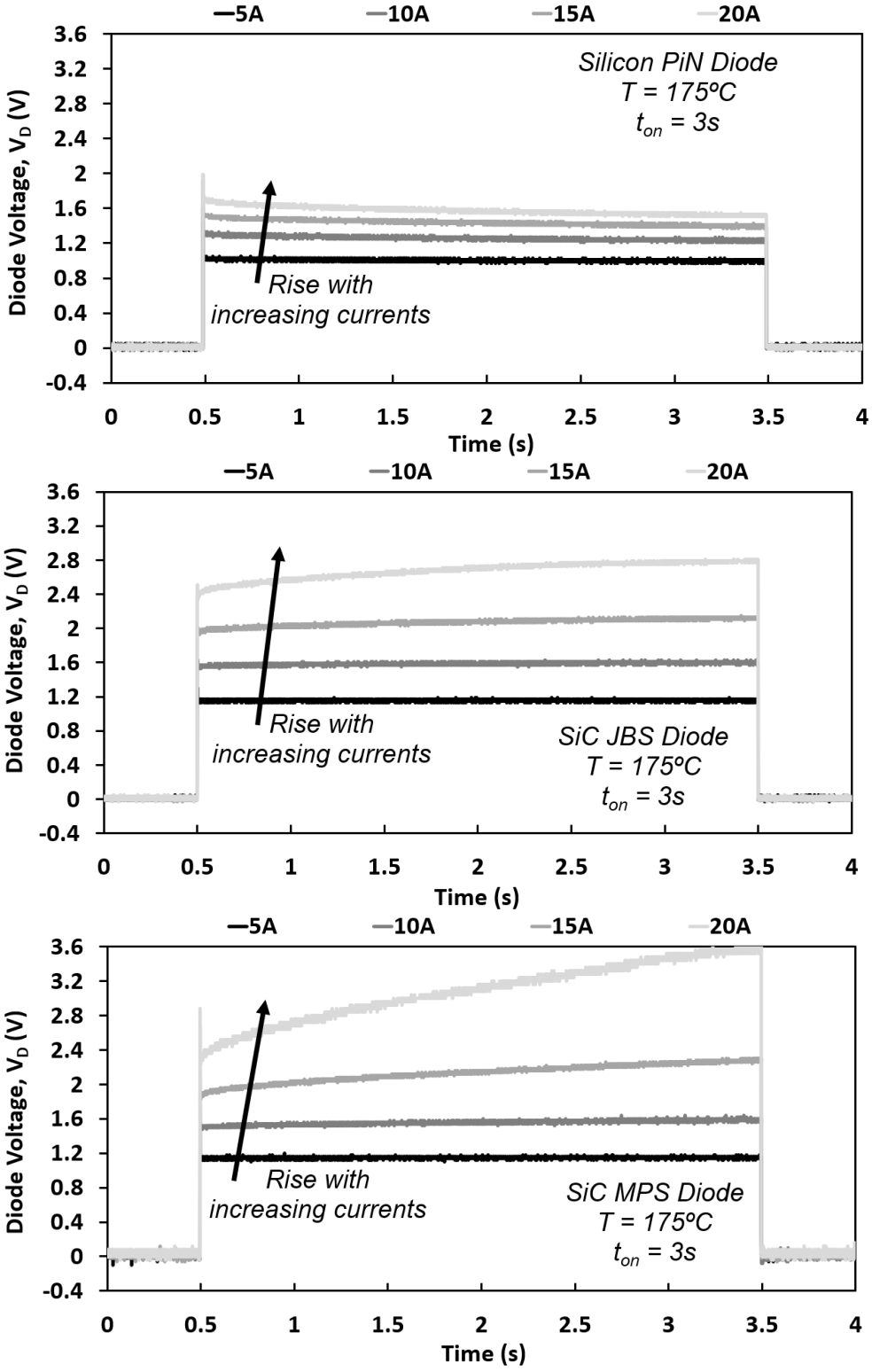

Figure 5.10: On-state voltage during self-heating for all three devices with temperature of 175°C and for each of Silicon PiN, SiC JBS and SiC MPS diodes at various current levels.

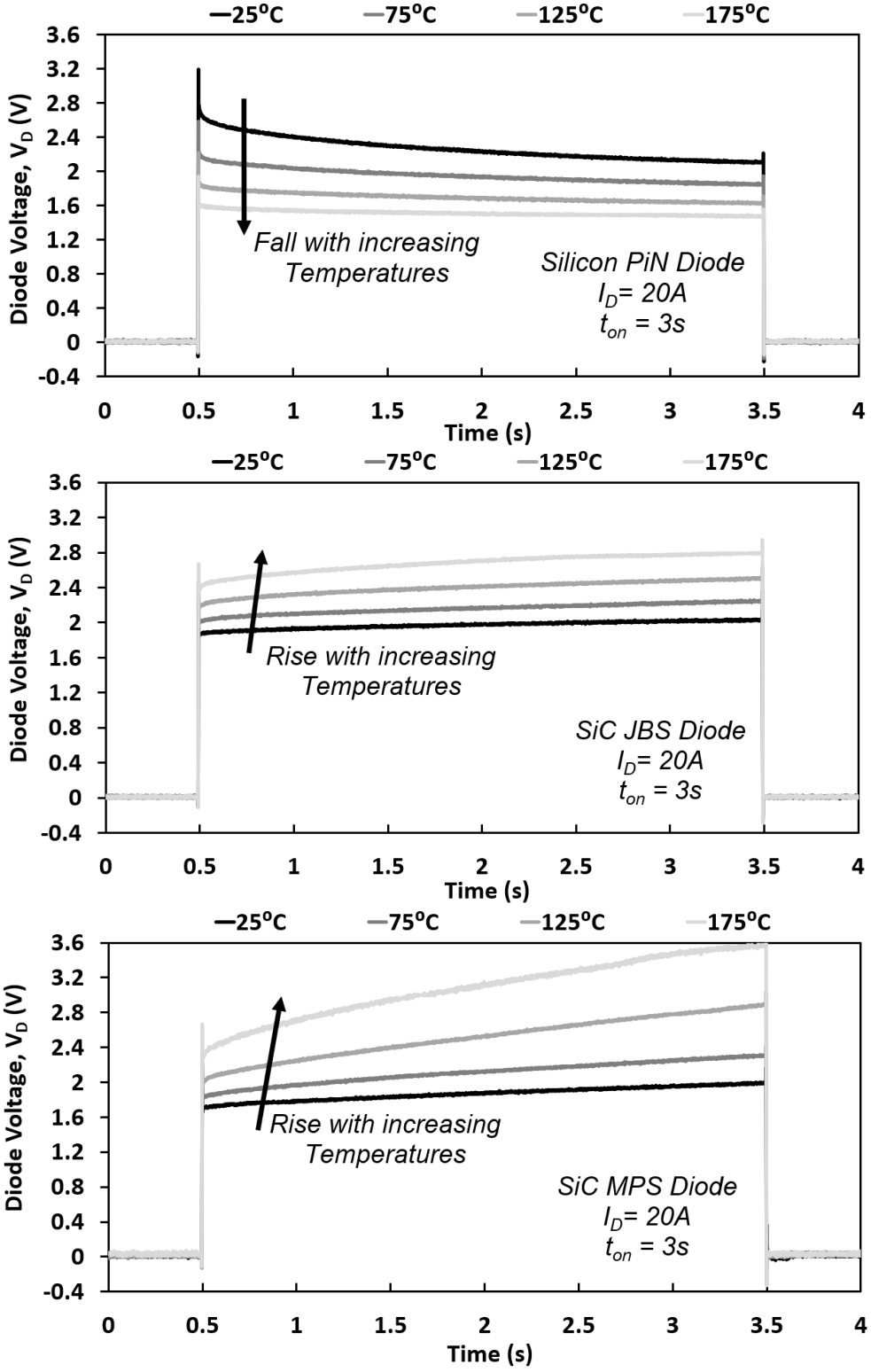

Figure 5.11: On-state voltage during self-heating for (a) Silicon PiN, (b) SiC JBS and (c) SiC MPS diode at various operating temperatures.

Figure. 5.9, 5.10 and 5.11 show the negative temperature dependence of the on-state voltage of Si PiN diode at the beginning of the on-state and during the on-state, as it was explained in the last section. In contrary to the Silicon PiN diode, the reversal of temperature dependence for SiC devices, especially for SiC MPS diode when compared with that in Fig. 5.8 is observed. This is because the increased voltage drop across the drift resistance causes the forward voltage to have a positive temperature coefficient. The absence of conductivity modulation is beneficial for the JBS diode because it favours the unipolar conduction through the JBS structure which is designed to block high voltage while secure its unipolar conduction mode [9].

However, this is a disadvantage of MPS diodes which is expected to have some conductivity modulation effect. Figure. 5.9, 5.10 and 5.11 also show larger on-state voltage at high currents and at high temperatures, further increases during the on-state. The on resistance is further increased due to the negative temperature coefficient of the carrier mobility. For power system applications with long steady-state operation, it is prone to destructive consequences as the increased power dissipation can create extra heat and thus the thermal runaway. But this is suitable for high frequency application as the low stored charge and thus the fast-switching transient is secured. To optimise the conductivity modulation effect of the MPS diode, it is necessary to increase the minority carrier lifetime to reduce the voltage and current required to enter the high-level injection mode [9]. However, the lifetime-enhancement technique is not adequately mature at present. Nevertheless, it is not beneficial for the Silicon PiN diode with negative temperature dependence of on-state voltage for paralleling. A positive feedback loop between current and temperature is generated since the hotter diode with lower voltage can conduct more current that will continue to increase until failure.

5.3 Unclamped Inductive Switchings (UIS)

The single event static avalanche ruggedness of Silicon PiN, SiC JBS and SiC MPS diodes have been investigated through a wide scale of UIS measurements. All the devices are fabricated in a standard TO-220 package as shown in Table. 5.1. The UIS testing board is shown in Fig. 5.12 with a high voltage IGBT (IXBX55N300) acting as the power switch [99]. The design of this PCB is shown in Appendix B. The initial temperature of diodes before each UIS event is controlled in the same way as that of static measurements. During the on-state when IGBT switches on, a load inductor of 1.25 mH is charged to store the avalanche current which is proportional to the length of the gate pulse L_P, ranging at 80 μs & 160 μs, and also proportional to the initial DC link voltage V_{DC} increased from 90 V to 360 V. The avalanche current(maximum load current) can be expressed as:

$$I_{ava} = V_{DC}\frac{L_P}{L_{load}} \tag{5.1}$$

During this UIS test, L_P and V_{DC} are increased alternatively to apply more stress to diodes. Two GW-Instek GDP-100 100 MHz voltages probes and a CWT Ultra-mini 50 MHz Rogowski current coil (CWT1) are used to capture voltage and current waveforms while both are shown in the same oscilloscope as that for the on-state measurement. Typical current and voltage waveforms during the single UIS event is shown in Fig. 5.13.

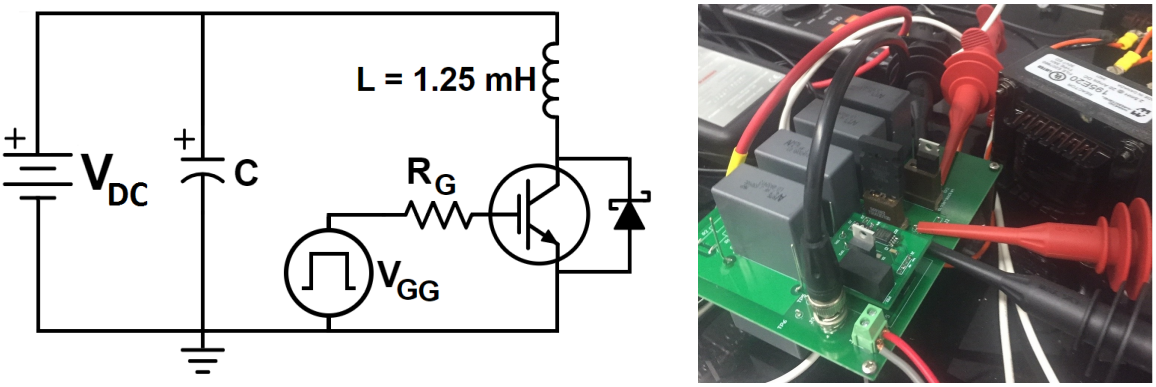

Figure 5.12: The UIS test circuit schematic and the test board.

When the IGBT switches off, the current flowing through the inductor starts to decrease. Since a counter Electromagnetic Force (EMF) will be induced by the magnetic field of the inductor to resist the abruptly change of inductor current, the induced avalanche voltage V_{ava} can be derived [30, 54] as:

$$V_{ava} = L_{load} \times \frac{dI_{off}}{dt} + V_{DC} \tag{5.2}$$

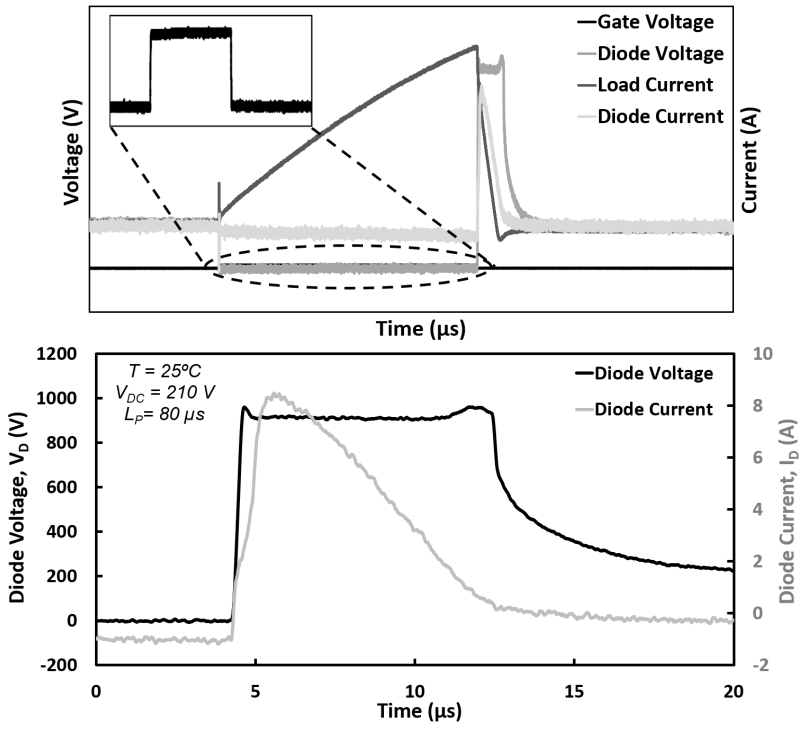

Figure 5.13: Typical waveforms under UIS test and its zoomed-in version.

The avalanche voltage usually reaches the breakdown voltage [56] of the diode (V_{BR}), conducting the avalanche current. Unlike the power diodes which will suffer high electrothermal stress, the IGBT will stay safe due to the much higher voltage/current ratings (voltage of 3 kV & steady-state current of 55 A at 110°C). If the avalanche current is high enough to generate substantial electron-hole pairs as expected from section 2.5.3, these extra carriers can lead to high junction temperatures, degrades the diode breakdown capability or destroys the device as the hotspot at junction termination with potential for melting of the anode metallization [60].

To monitor the device degradation before & after each single UIS test, the I-V characteristic of all three diodes has also been measured. Fig. 5.14 shows the degradation of the I–V characteristics of those diodes under test. Unlike the repetitive UIS test which imposes the same thermal stress for all UIS pulses, the single UIS tests aim to fail the device with just a one pulse with increased electrothermal stress. Meanwhile, all three devices under test show stable behaviour with minor degradation at 25°C and at 175°C during the single UIS tests, when compared with the forward degradation in [63]. Therefore, this single UIS test methodology are shown to be reliable while the devices' degradation is also found to have a limited impact on their failure.

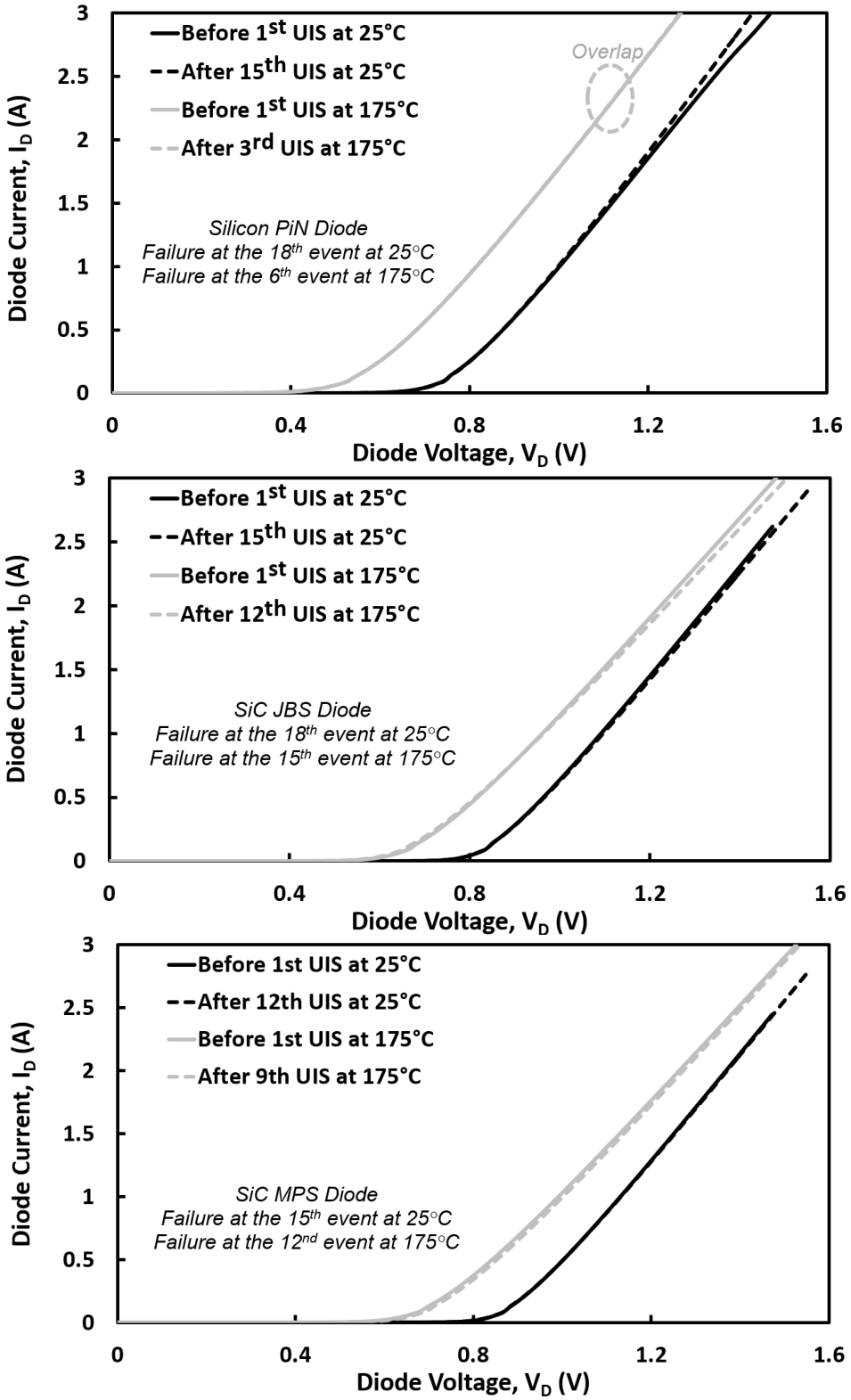

Figure 5.14: Forward voltage drift of the IV characteristics at 25°C and at 175°C for Silicon PiN, SiC JBS and SiC MPS diode.

Fig. 5.15 and Fig. 5.16 show the zoomed-in view of UIS waveforms for diodes with different technologies with load current increased until failure of devices. At load current of 5 A, the diode voltage cannot reach the breakdown voltage in Silicon PiN diode. This is because the rate of switching of current (dI/dt) combined with the inductor cannot generate enough voltage. Although all three diodes are rated at 1.2 kV, a much higher effective breakdown voltage can be observed. It can also be seen in Fig. 5.16 and in Fig. 5.17 that the avalanche duration (t_{ava}) increases with increase of load current. This is because:

$$t_{ava} = \frac{I_{ava} L_{load}}{V_{ava} - V_{DC}} \tag{5.3}$$

while the tail current indicates the process to discharging the capacitors.

When the load current is further increased, this leads to the short circuit failure of diodes. Diodes conduct in the reverse direction with increasing current exceeding the preset load current levels because of the discharge of bank capacitors, while the diode voltage drops to zero as the blocking capability is lost. Silicon PiN diode failed at lower load current compared with the SiC JBS & SiC MPS while the recovery process, as in Fig. 5.16, has been skipped as the device cannot handle such high induced avalanche current.

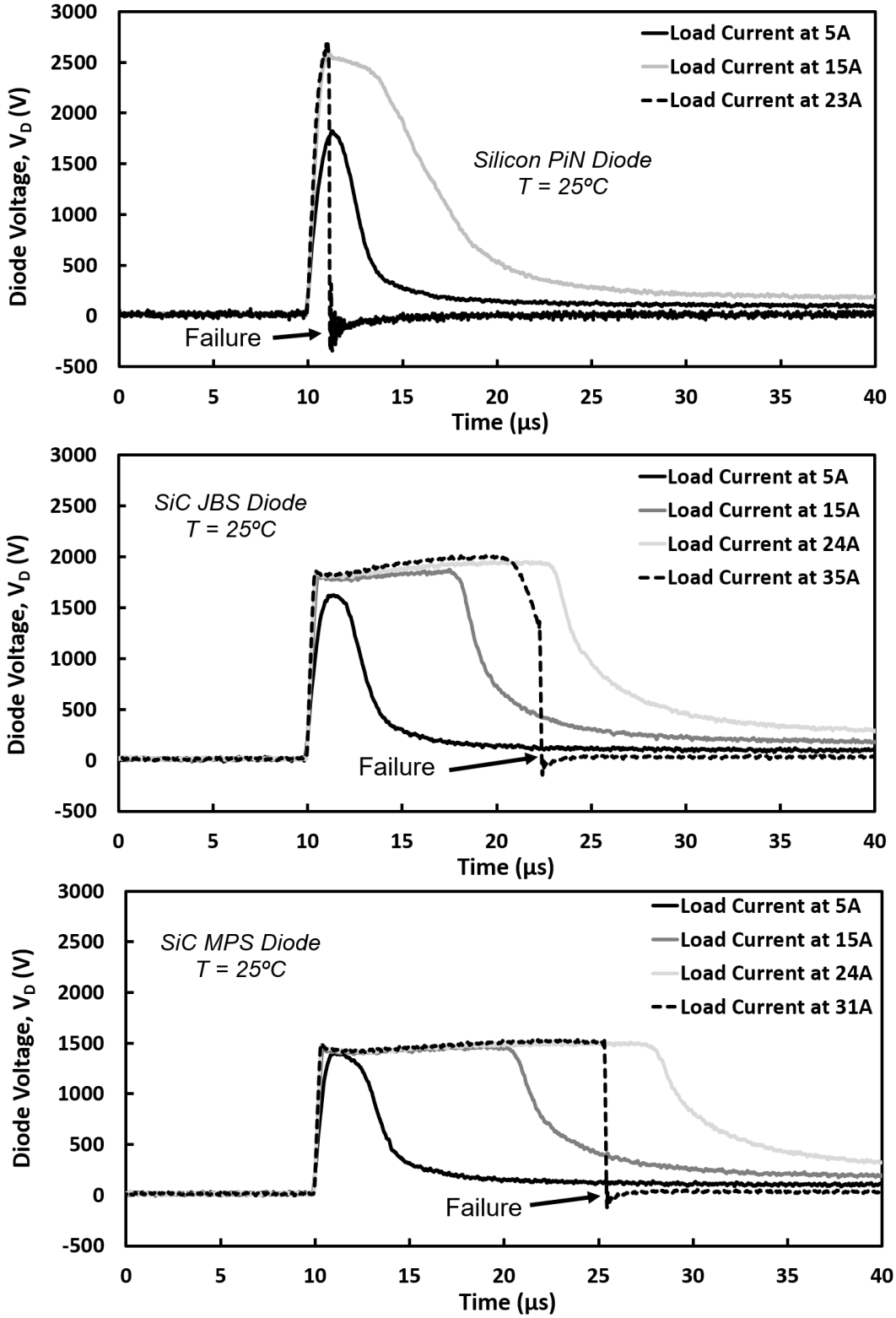

Figure 5.15: Avalanche diode voltage as a function of time for different load currents until device failure for Silicon PiN diode, SiC JBS diode and SiC MPS diode.

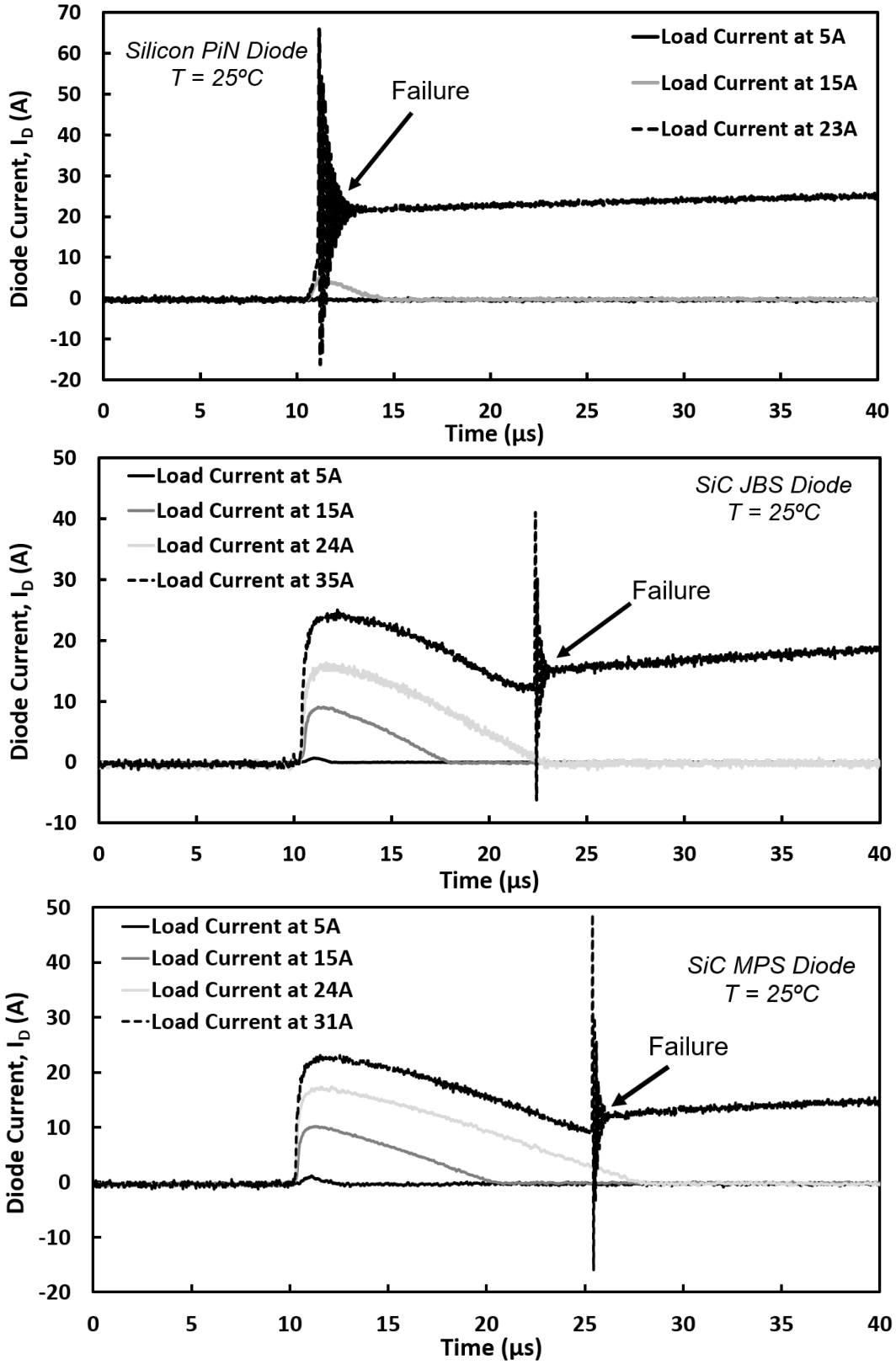

Figure 5.16: Avalanche diode current as a function of time for different load currents until device failure for Silicon PiN diode, SiC JBS diode and SiC MPS diode.

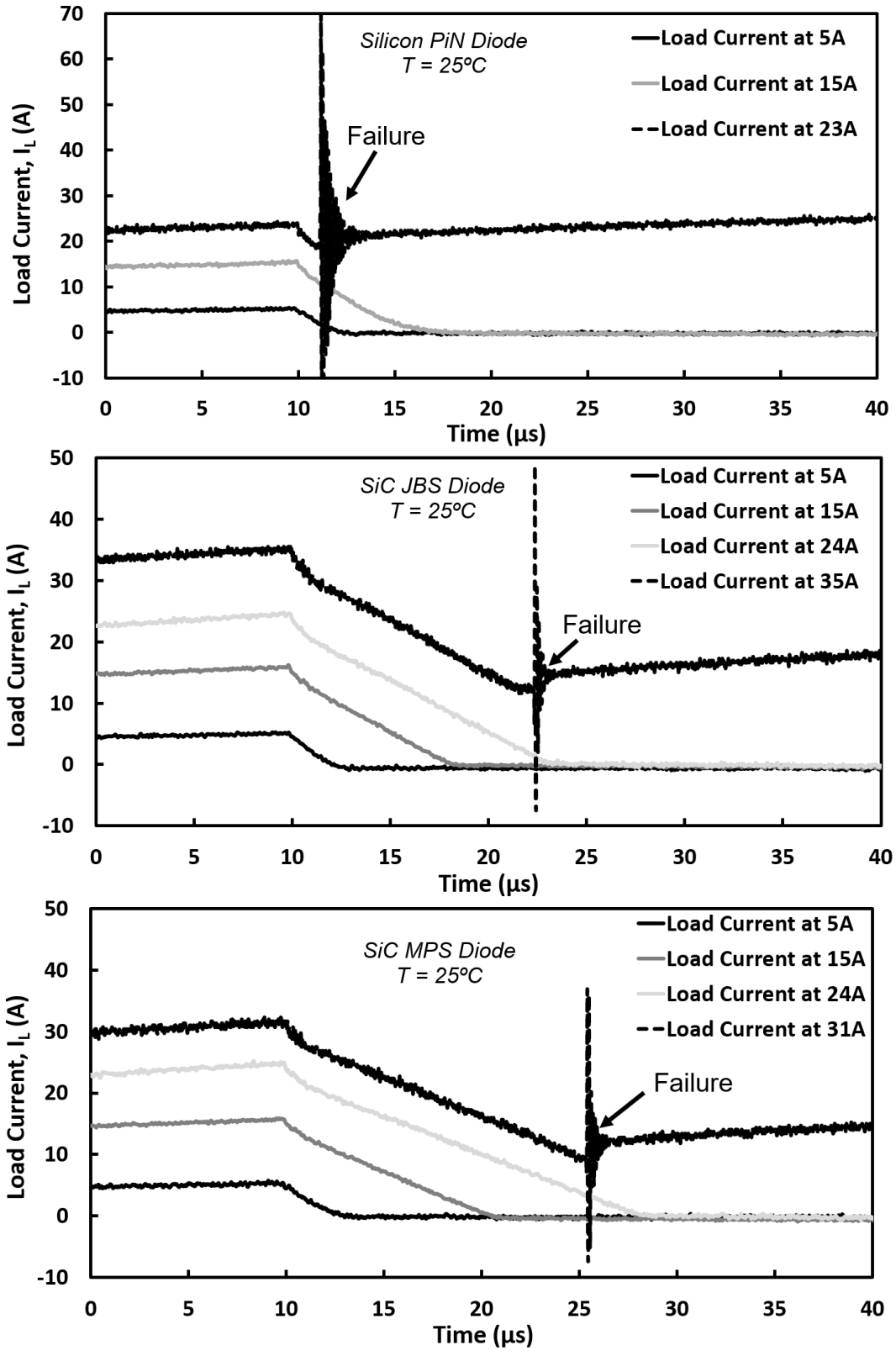

Figure 5.17: Avalanche load current as a function of time for different load currents until device failure for Silicon PiN diode, SiC JBS diode and SiC MPS diode.

Fig. 5.18 and Fig. 5.19 emphasize the difference in avalanche ruggedness among three different diodes at failure mode. It is seen that the SiC devices can sustain the avalanche conduction for a longer time than that of Silicon device before the avalanche multiplication is triggered. It can also be seen that the highest effective breakdown voltage in Silicon PiN diode, followed by that of SiC JBS and that of MPS. At high base temperatures, all devices is found to fail at lower currents with shorter recovery period. This can be explained by the fact that there is less headroom to reduce junction temperature allowed during the recovery process when the temperature of controller is increased and thus they can withstand less avalanche energy.

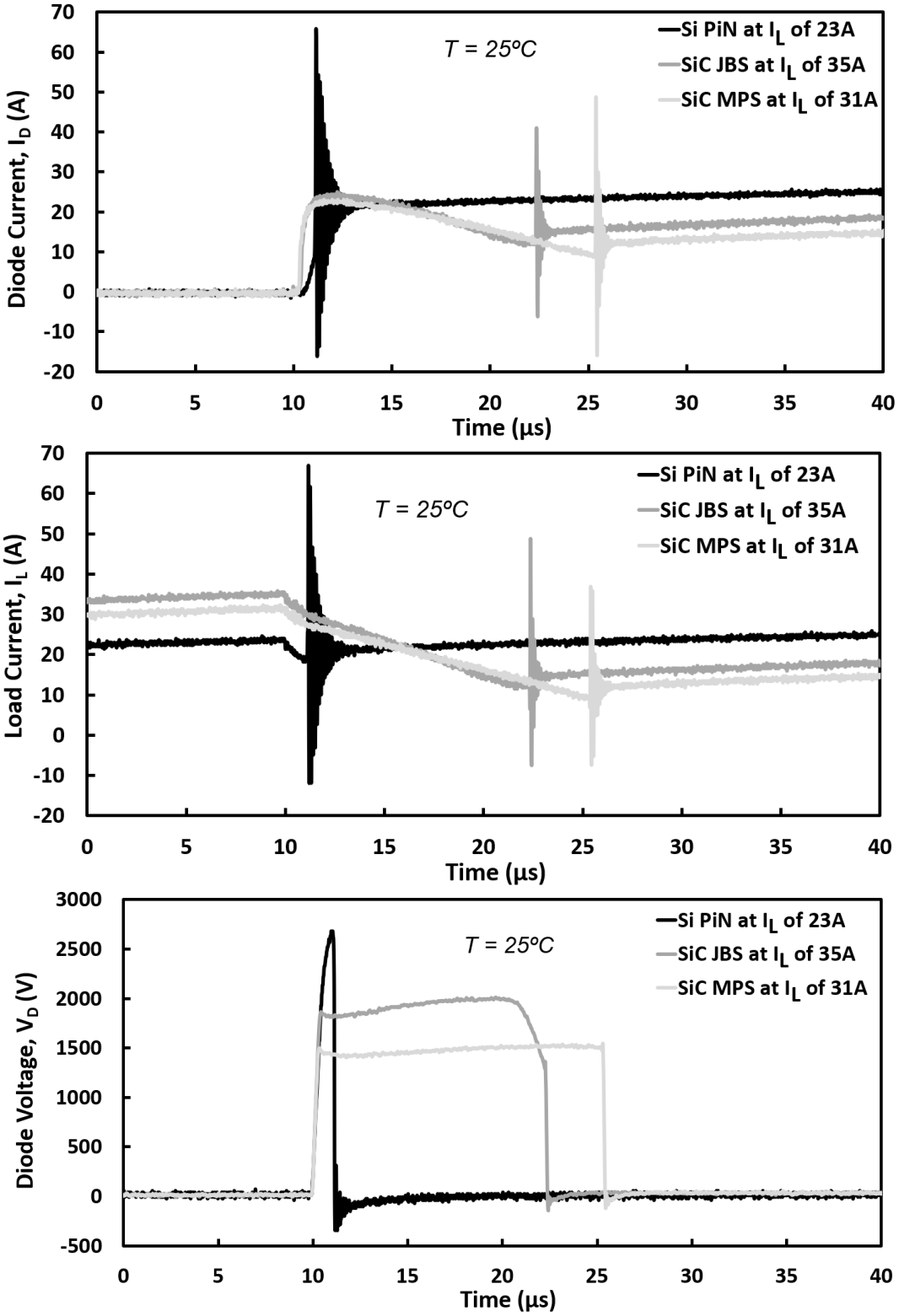

Figure 5.18: The diode current, load current, and diode voltage when failure occurs at 25°C.

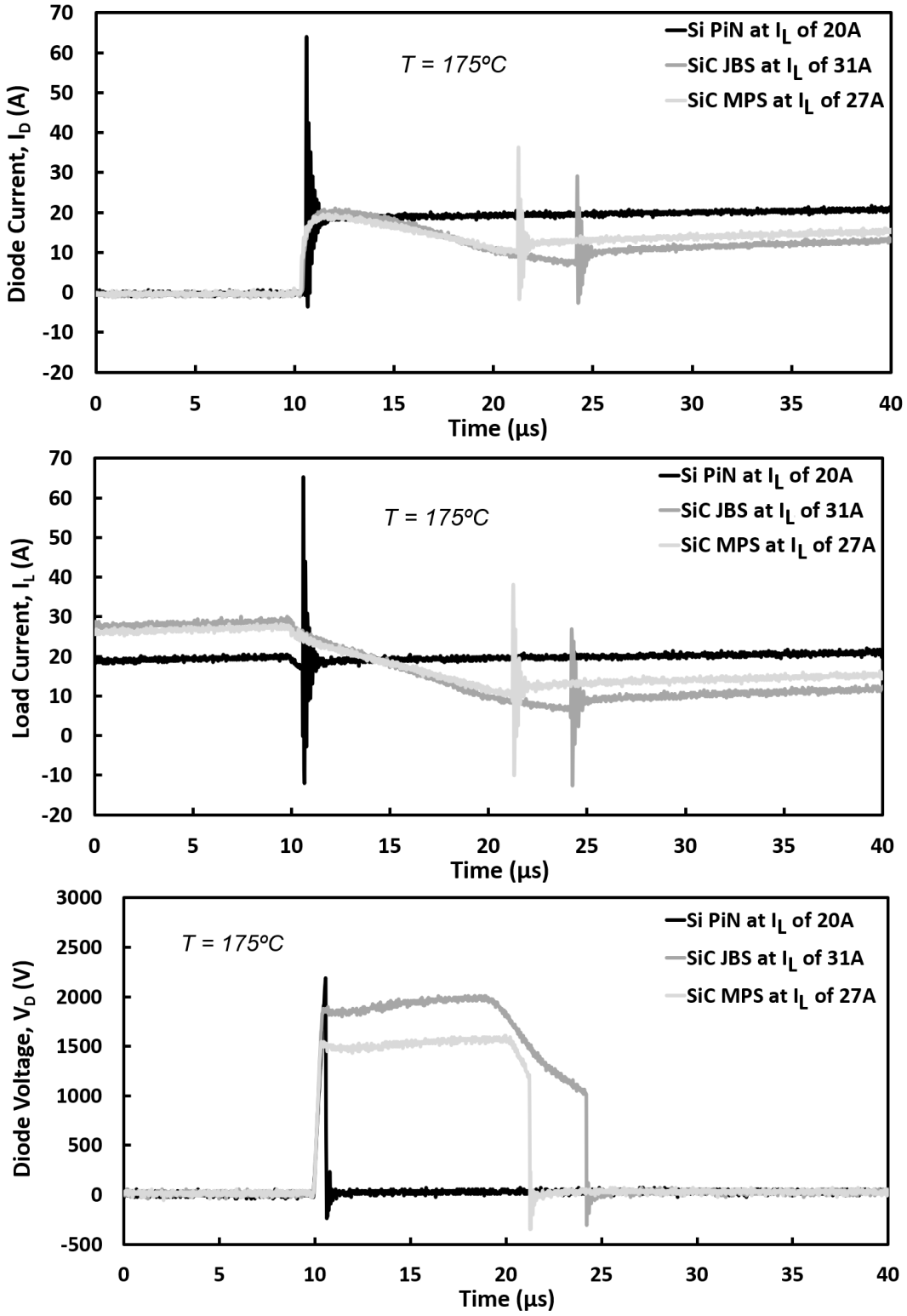

Figure 5.19: The diode current, load current, and diode voltage when failure occurs at 175°C.

The avalanche energy is an important metric to evaluate avalanche ruggedness of the devices. The critical avalanche energy is defined as the energy extracted from the last-pass waveform [51] before the failure of the device during the progressive single UIS tests as highlighted in Fig. 5.20, can be derived as:

$$E_{ava} = \int_0^{t_{ava}} V_{diode}(t) \cdot I_{diode}(t) \cdot \mathrm{d}t \tag{5.4}$$

where t_{ava} is the time duration of device avalanche.

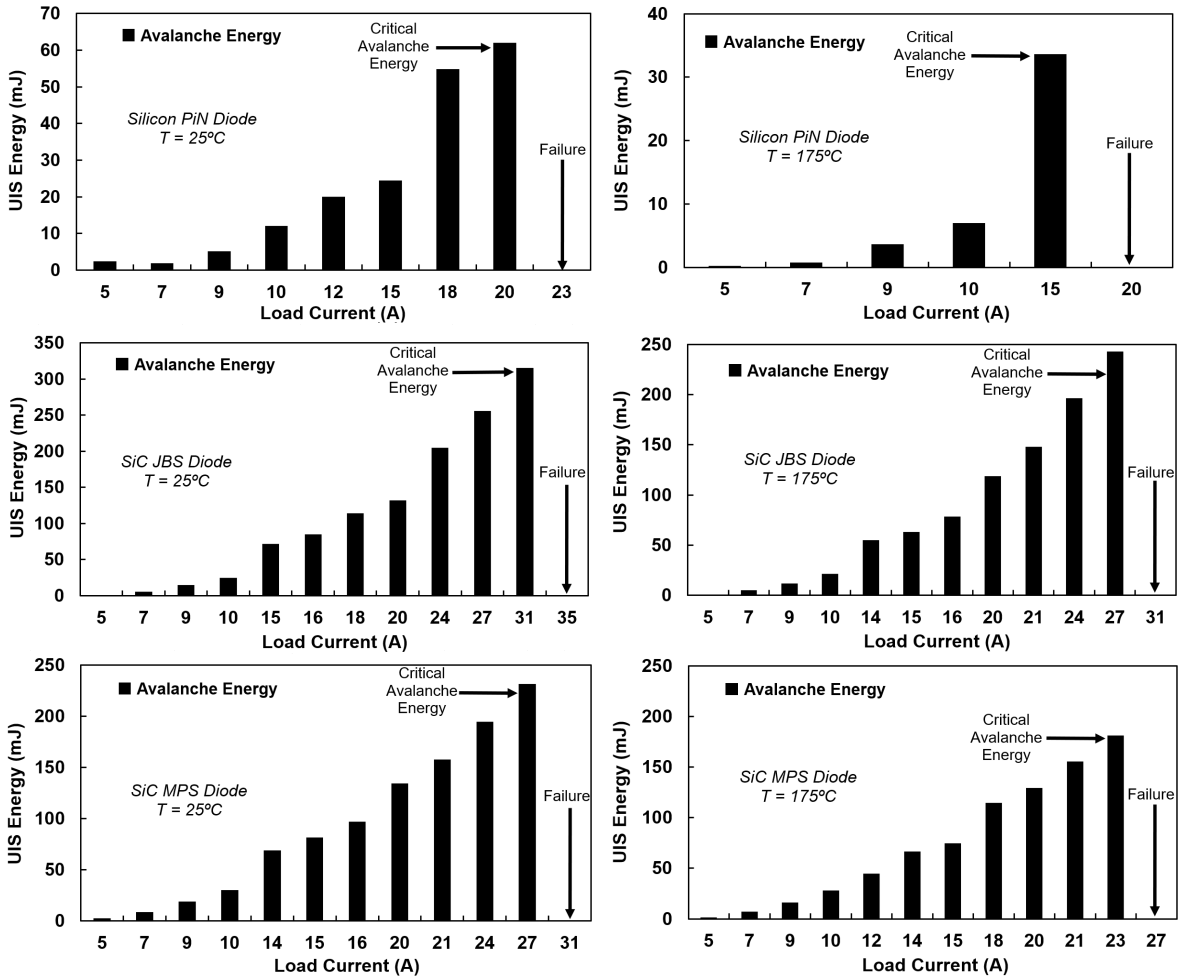

Figure 5.20: The critical avalanche energy calculated by UIS tests at 25°C and at 175°C.

The critical avalanche energy of SiC JBS, as shown in Fig. 5.22, is the highest, followed by that of SiC MPS, and then that of Silicon PiN diode. This is expected from Fig. 5.16 and Fig. 5.15 as the recovery time after the event dominates the avalanche energy. The critical energy is found to be lower at higher temperatures. This is because of the shorter recovery period observed at high temperatures, primarily due to the smaller difference between the junction temperature and the base temperature making the heat extraction more difficult. Despite the Silicon PiN diode is able to sustain a higher reverse voltage compared to SiC devices before the actual failure takes place, this device always failed at lower load currents during the single UIS tests. To enable analyzing the avalanche energy density of the devices, the failed devices have been CT-Scanned using a Nikon® XT H 225 ST CT-Scanner at the XTM Facility, Palaeobiology Research Group, University of Bristol and have been analyzed using the Dragonfly® software. The results of the scans, together with measurements of die sizes are included in Fig. 5.21. It can be seen that the Silicon PiN diode has the largest die, followed by the SiC JBS and MPS. The three devices have similar packaging, though with different dies areas, and thus it is conceived that the packaging has limited impact on difference between the results of devices.

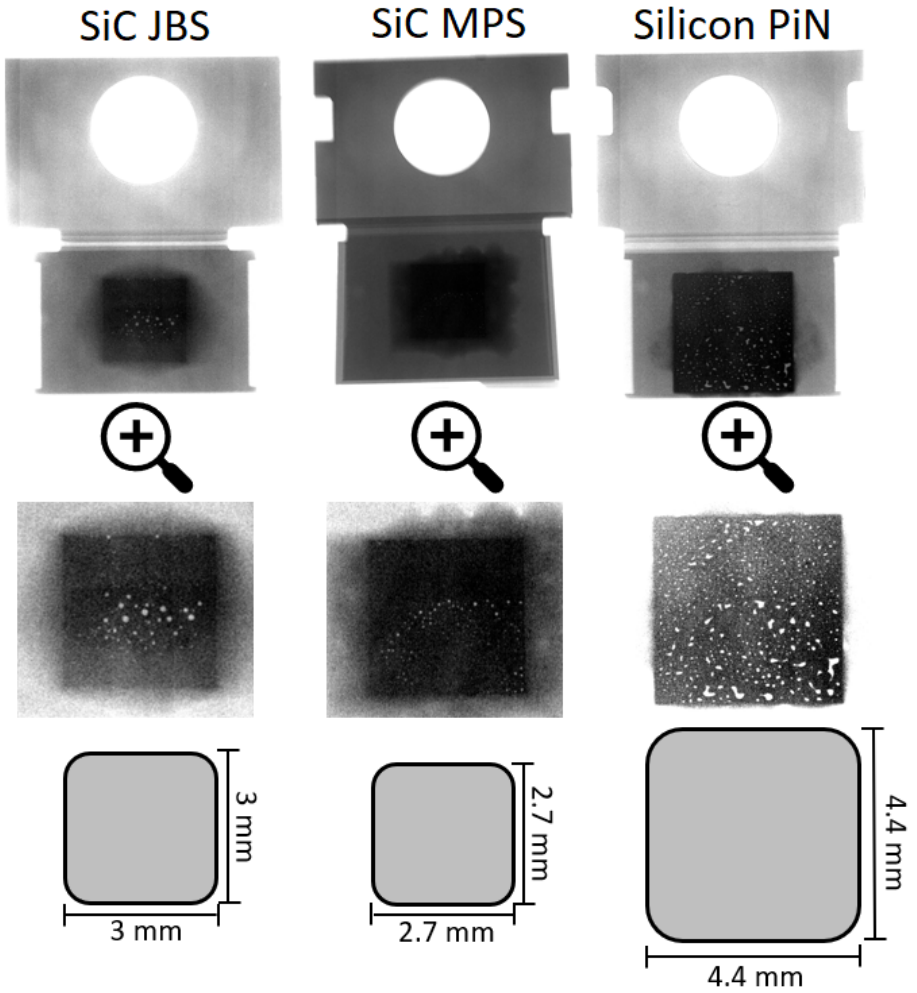

Figure 5.21: Corresponding front side CT scan image of the failed devices from Fig. 5.18 for Silicon PiN diode, SiC JBS and SiC MPS diode.

The factors that lead to the higher avalanche ruggedness of the SiC devices compared with the Silicon PiN, excluding the packaging, can be listed as follows. Firstly, The thermal conductivity of SiC is over two times higher than that of Silicon enabling a more effective heat dissipation. In addition, the wide-bandgap of SiC limits the generation of additional carriers due to the higher thermal energy [100, 101]. Additionally, the higher saturation velocity of SiC devices, as shown in Table 2.1, can lead to less electron-hole pairs being generated during the UIS event. This is in-line with the trend expected by

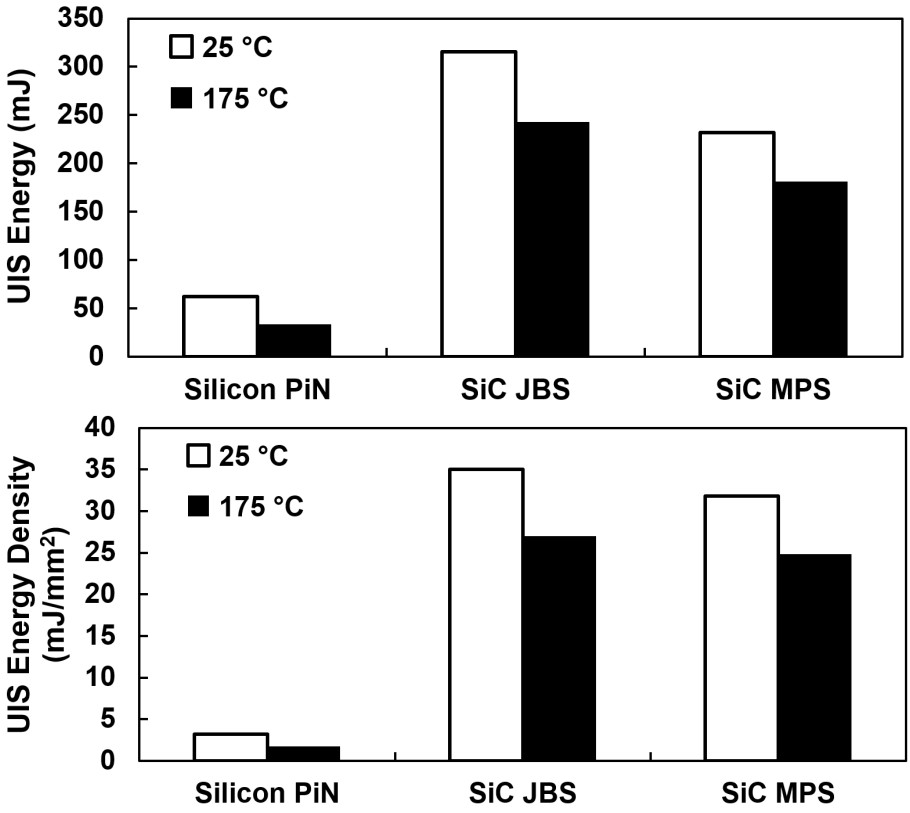

Figure 5.22: Comparison of critical avalanche energy and energy density for Silicon PiN, SiC JBS & SiC MPS diode at different temperatures.

Eq. 2.18 and Eq. 2.19. In contrast, the lower electron saturation velocity in Silicon leads to excess carriers being generated and trigger avalanche multiplication. Additionally, the impact ionization coefficient of SiC devices is smaller than Silicon, so less electron-hole pairs are generated at reverse bias. All of these would lead to a better performance of the SiC diodes than the Silicon counterparts as demonstrated in the measurements of this chapter. It can also be concluded that the failure in Silicon diode arises due to the significant electric field while such electric field as well as the heat generated during t_{ava} cause failure in SiC devices.

Silvaco TCAD finite element models have been developed to study the failure mechanisms of all three devices which indicate that the avalanche current of SiC JBS diode is

more evenly distributed in the device active region when compared with that of SiC MPS diode and Silicon PiN diode. This is because the higher electric field in the middle of Schottky contacts lead to a more evenly distribution of avalanche current as it is diverted to two different edges of the P^+ region. In contrary, current crowding is observed in the case of SiC MPS diode due to the smaller electric field formed at the Schottky contact.

5.4 Surge Current Test

For surge current measurements [102–104], the C4D20120A SiC JBS diode is replaced by a 1200 V/26 A SiC JBS diode with reference C4D20120H while the DSI30-12A Silicon PiN diode is replaced by a 1200 V/30 A Silicon PiN diode with reference DSEP30-12B due to chip shortages. The surge current testing board and the typical current and voltage waveforms in a single surge current event [101] is shown in Fig. 5.23. The design of this PCB is shown in Appendix B. Four parallel connected Silicon power IGBTs IXGK400N30A3 are used to accurately set the current conduction time of 100 μs through the diode [56, 99]. A 2052 μF capacitor bank consisting of three electrolytic capacitors was used to deliver the surge current peak. The initial temperature before the circuit turn-on is controlled from 25°C to 175°C via the same temperature controller used for UIS measurements. The charge stored in the capacitors is proportional to the DC link voltage V_{DC} increased from 40 V to 160 V. When the IGBTs switch on, the charge stored in capacitors will be released to induce the surge current I_{Surge}.

The resulting power dissipation cause the surge of junction temperature, degrades the diode blocking capability or destroys the device as the hotspot at junction termination with potential for melting of the aluminum anode metallization [52, 67, 105]. Unlike the power diodes which will suffer high electrothermal stress, the IGBTs will stay safe because

of the increased current rating from the parallel connection. Unlike the UIS measurements where the failure of devices can be directly observed from the waveforms, a B2902A Source/Measure Unit (SMU) is used to capture both the forward I-V characteristic and reverse leakage current of all three diodes to trace degradation and detect failure.

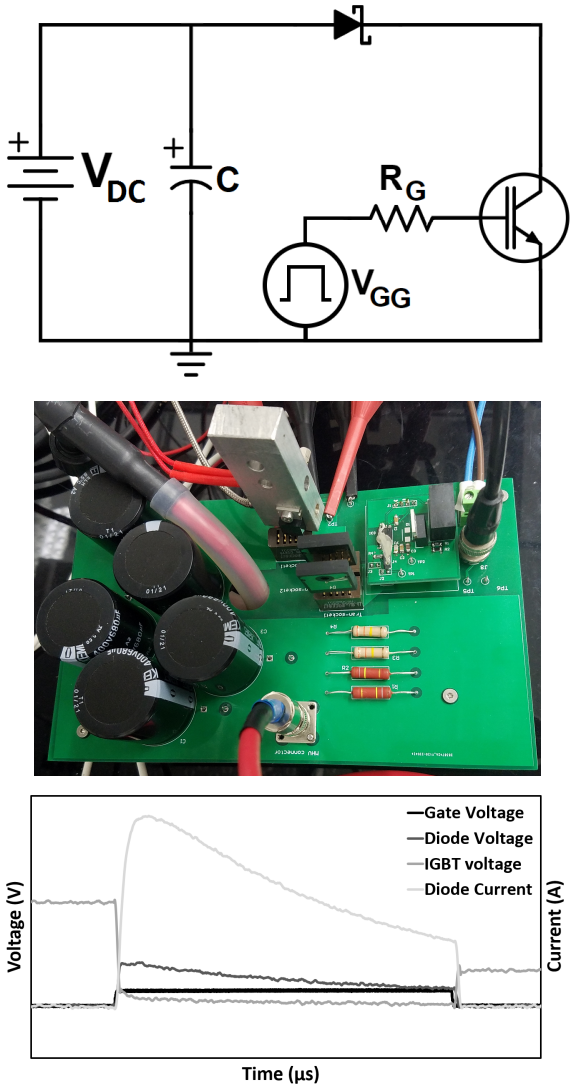

Figure 5.23: The Surge Current test circuit schematic, the surge current test board and the typical waveforms under surge current.

Fig. 5.24 to 5.26 show the forward voltage drop and the forward surge current of three diode rectifiers under non-repetitive surge testing. It is observed that the forward surge

current increases with DC link voltage, as expected, while the on-state voltage across diodes is increasing with increased surge current. For Silicon PiN diode, the less voltage increment is observed at high currents as a indicator of conductivity modulation, which also hold true at elevated temperatures. However, the conductivity modulation, is less evident in the case of SiC devices at both low and high temperatures. This is mainly because of the low carrier lifetime in SiC impeding adequate conductivity modulation in the drift region in on-state, contributing to additional on-resistance. This problem becomes aggravated if the current imbalance between Schottky junction and PN junction within the device occurs after the injection of hole from P^+ region, leading to the smaller effective area for carrying the surge current and dissipating the surge energy [106–108].

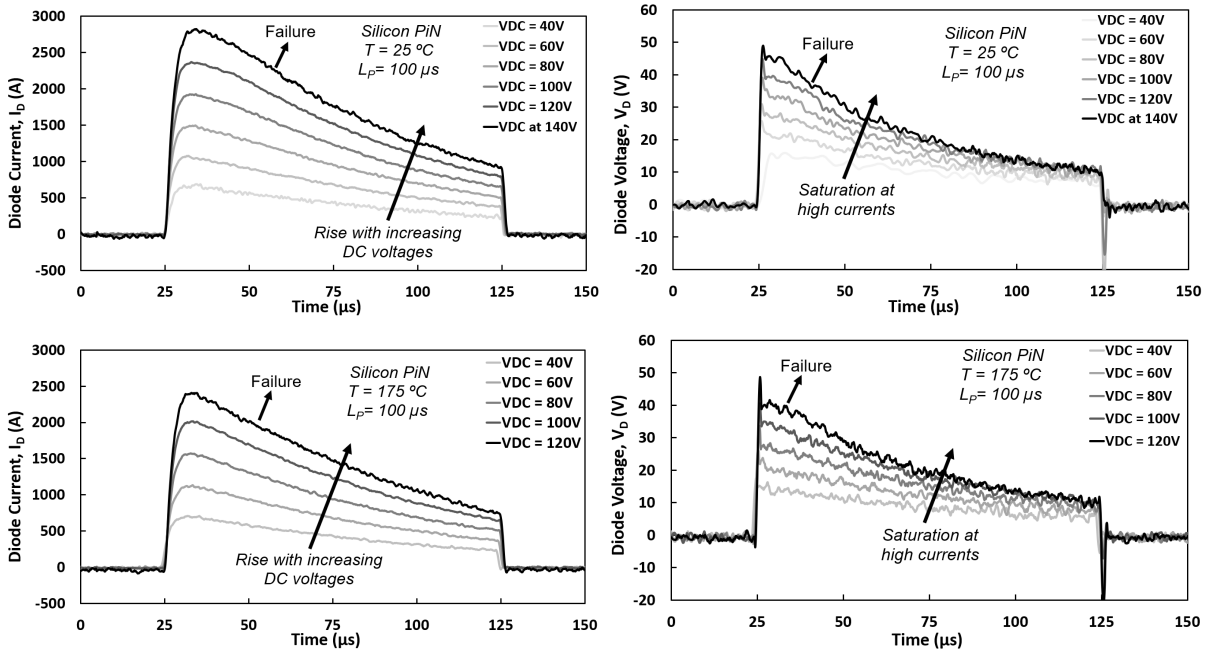

Figure 5.24: Forward voltage and current during the non-repetitive surge testing for Silicon PiN diode at 25°C & 175°C.

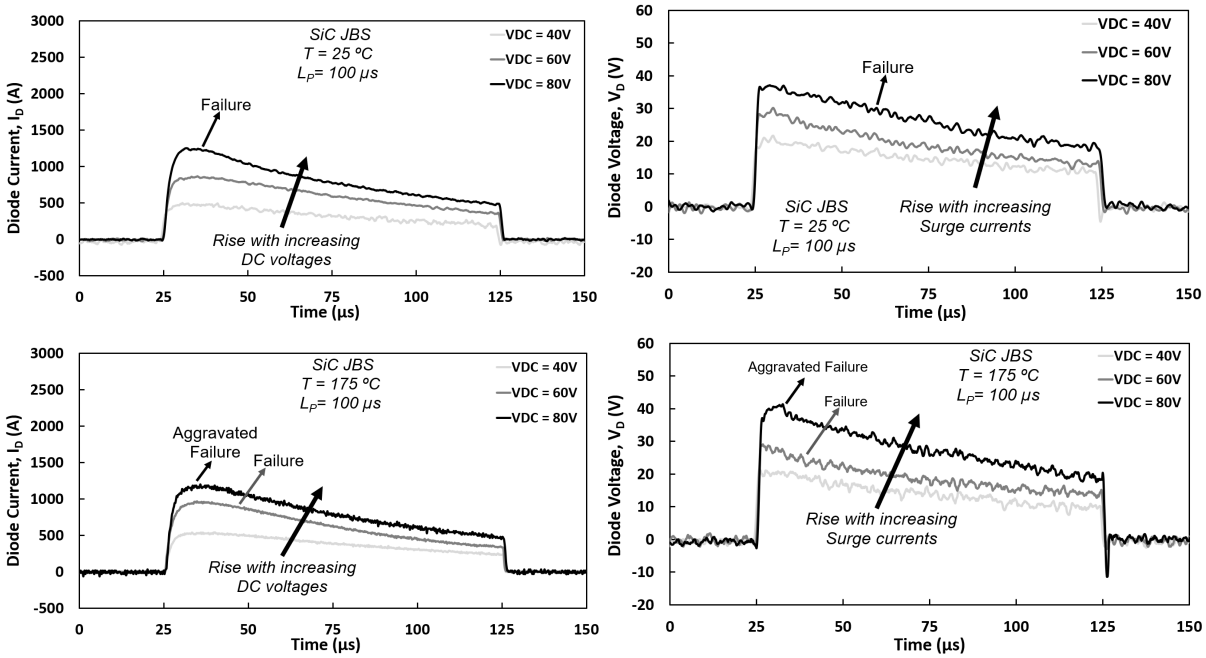

Figure 5.25: Forward diode voltage and current during the non-repetitive surge testing for SiC JBS diode at 25°C & 175°C.

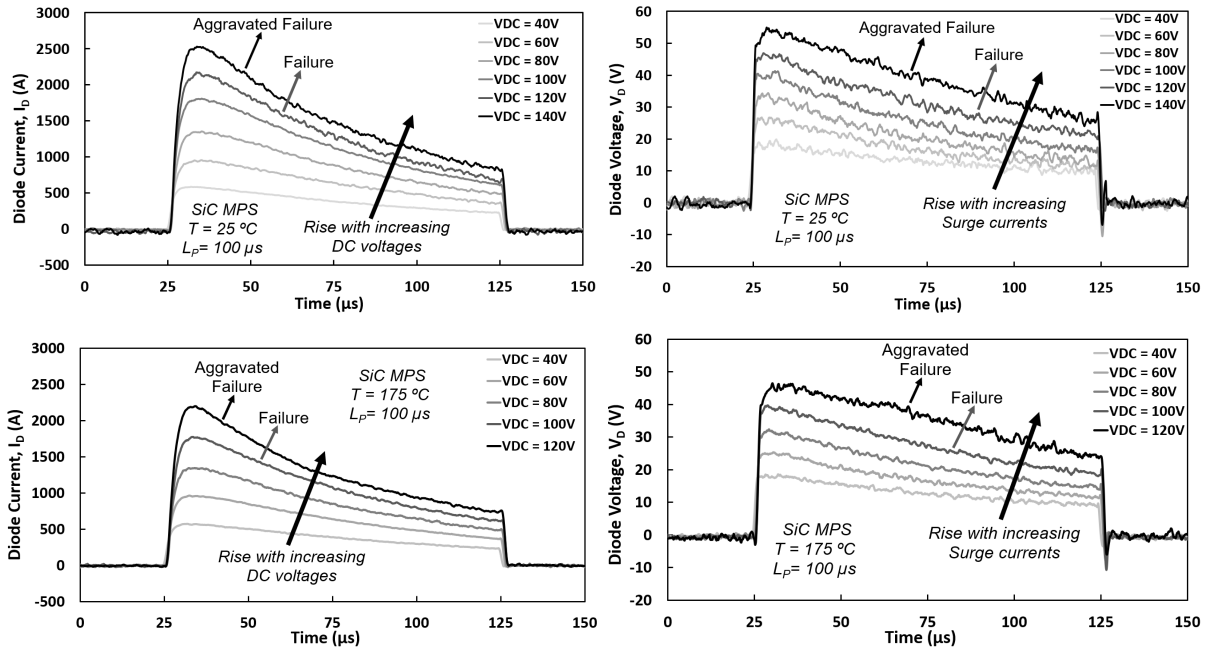

Figure 5.26: Forward diode voltage and current during the non-repetitive surge testing for SiC MPS diode at 25°C & 175°C.

Fig. 5.27 emphasizes the difference in forward voltage and surge current among three different diodes at surge current mode. It can be seen that the surge current for Si PiN diode is the largest, followed by that of SiC JBS and that of MPS. This can be attributed to the differences in device resistance. The on-state voltage of SiC JBS diode is the highest followed by that of SiC MPS diode and Silicon PiN diode while the minor conductivity modulation provided by the wide P^+ region in MPS diode provides a lower voltage compared to that of JBS diode. These are true at both low and high temperatures.

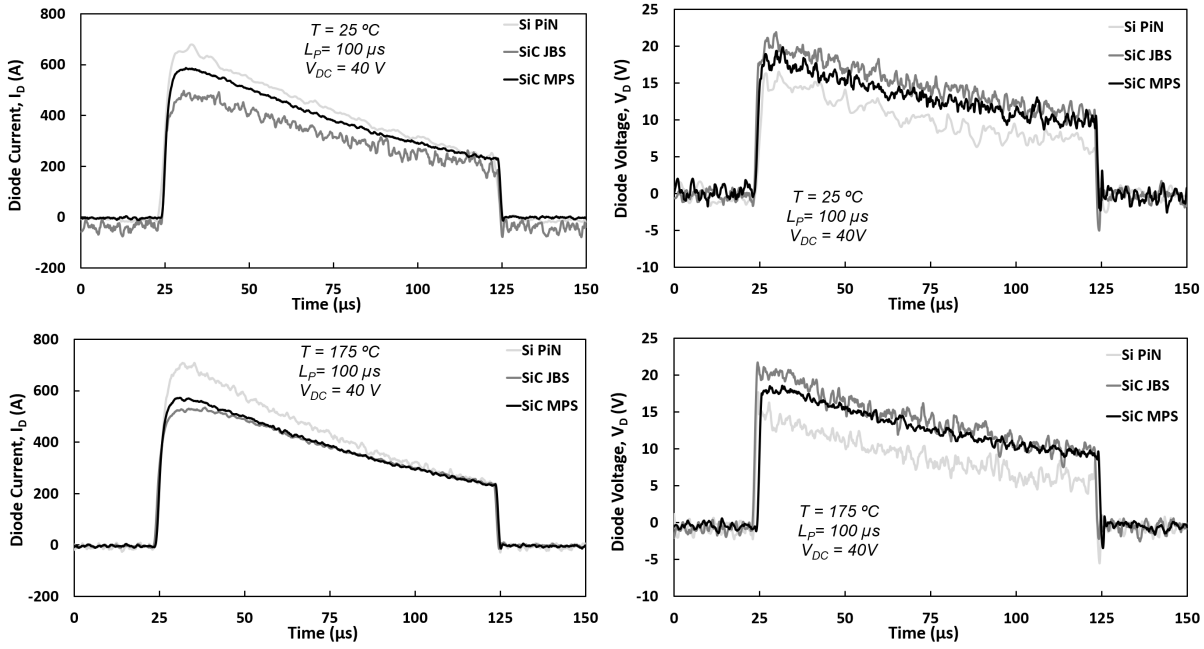

Figure 5.27: Forward diode voltage and current during the non-repetitive surge testing for three devices at 25°C & 175°C.

Fig. 5.28 and Fig. 5.29 provide a comparative illustration of the failure limit of the three devices under surge testing at 25°C and 175°C, respectively. The occurrence of device failure during the surge testing is identified by means of monitoring the I-V characteristic and leakage current as shown in Fig. 5.30-5.32. When the electrothermal stress is increased, the threshold voltage is found to decrease together with the on-state resistance. In terms of leakage current, significant degradation is observed where the leakage current starts to rise at low blocking voltages. The faulty reverse mode performance is found to be aggravated when the surge current is further increased, as shown in Fig. 5.31 and Fig. 5.32, where the breakdown voltage is reduced to almost zero and the leakage current increases akin to that in a conductor. In contrast, Fig. 5.30-5.32 shows that minor degradation is observed in I-V characteristic when the surge testing is repeated at higher DC-link voltages after the failure is observed from the leakage current, especially for the case of SiC JBS diode where the convergence between the normal condition I-V characteristic and faulty I-V characteristic is observed. Fig. 5.24-5.26 and Fig. 5.28-5.29 also illustrate that the diode can still conduct surge current during measurements even though the failure is already caused inside the device. In all cases, the SiC JBS diode failed at the lowest surge current, followed by SiC MPS and Silicon PiN diode. When the temperature is increased, all devices is found to be failed at lower voltages. This can be explained by the fact that there is less headroom to dissipate power during the recovery process when the temperature is increased.

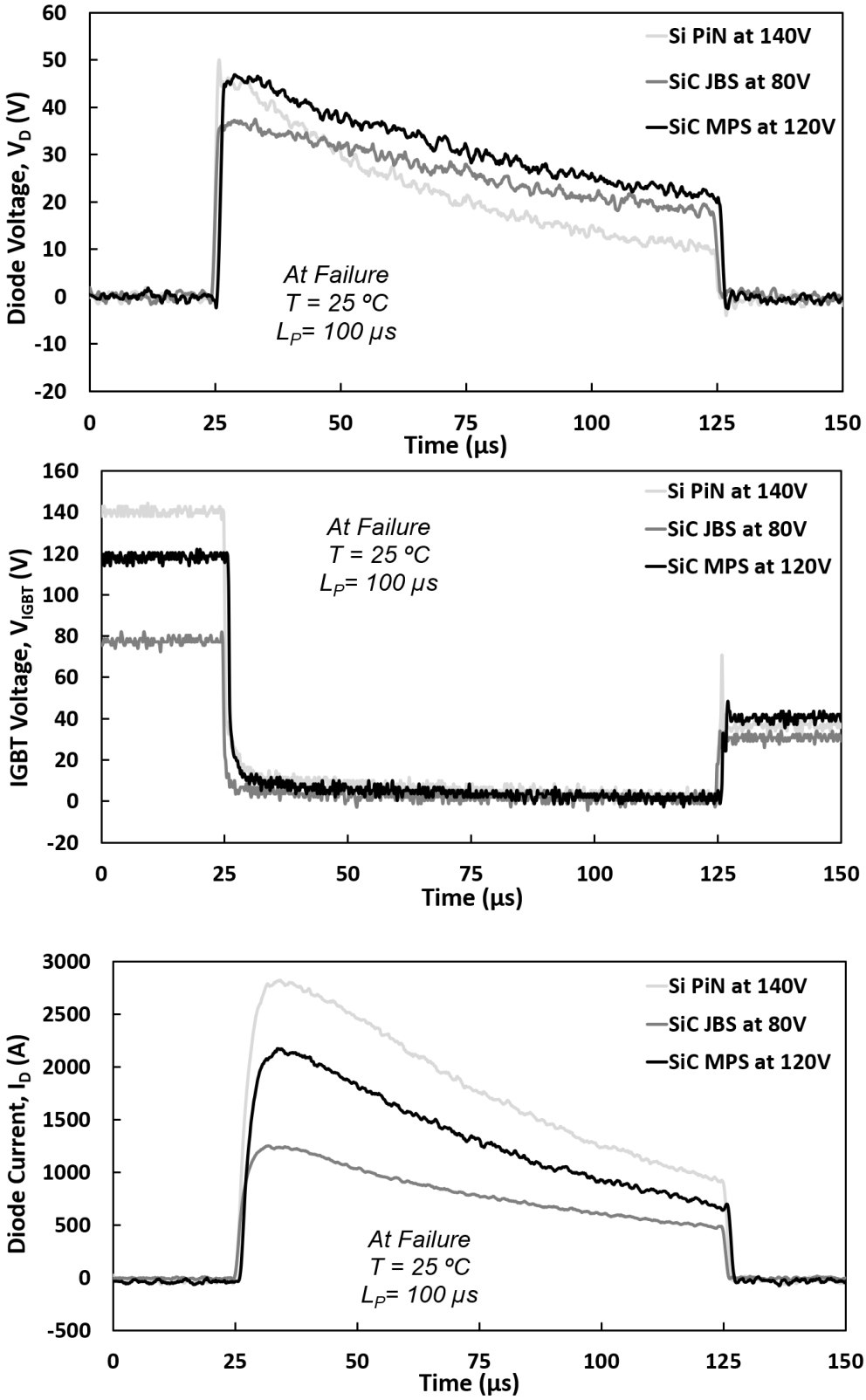

Figure 5.28: Forward diode voltage, IGBT voltage and diode current when failure occurs for three devices at 25°C.

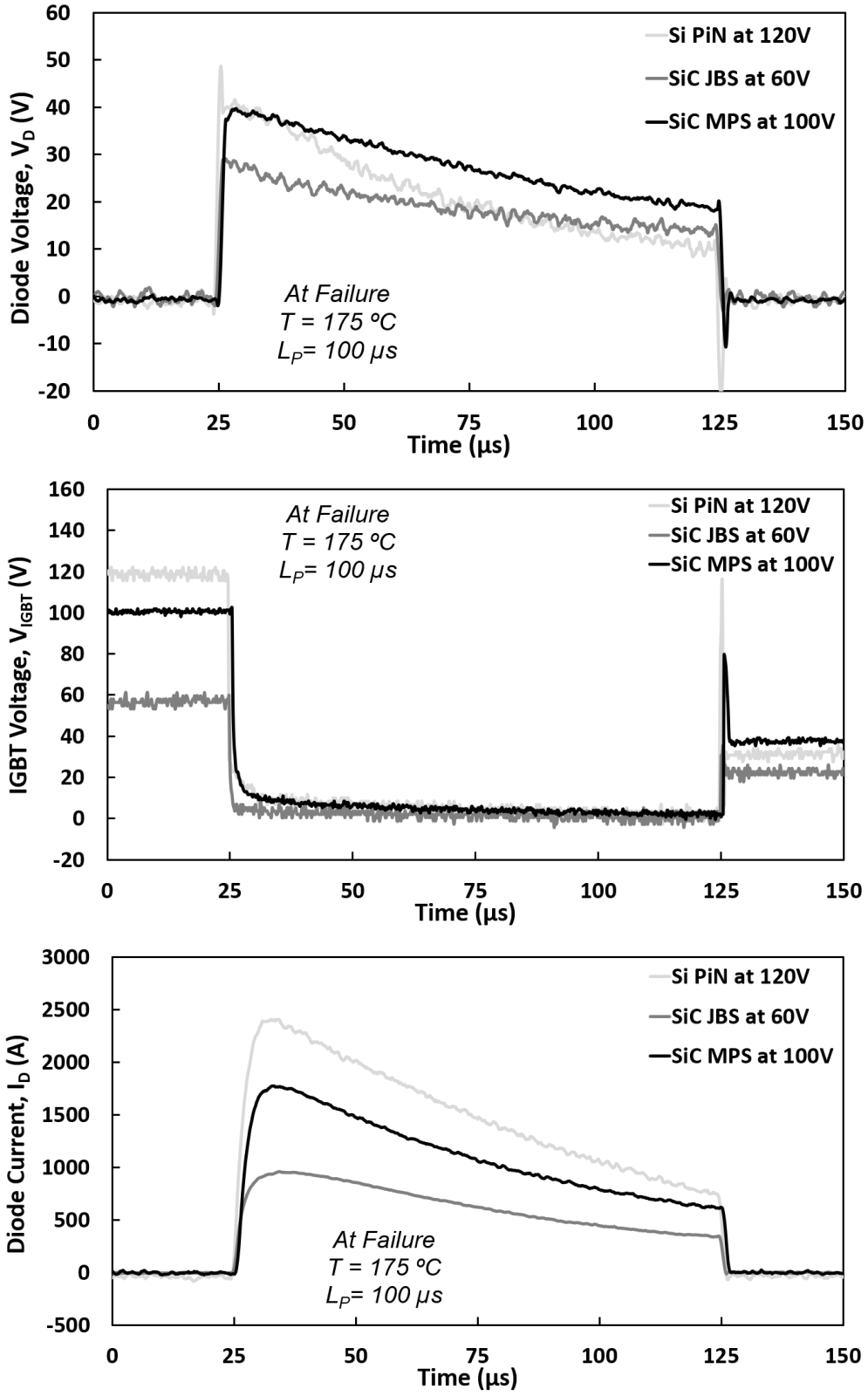

Figure 5.29: Forward diode voltage, IGBT voltage and diode current when failure occurs for three devices at 175°C.

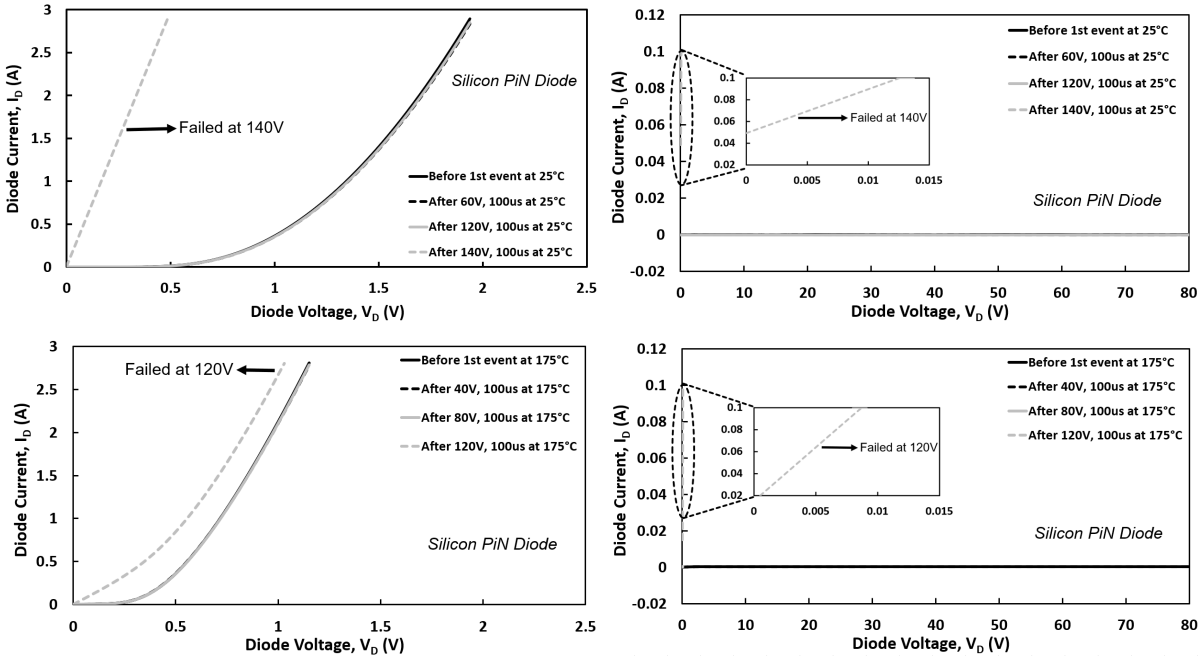

Figure 5.30: Forward I-V characteristics and reverse leakage current captured during the non-repetitive surge testing for Silicon PiN diode at 25°C & 175°C.

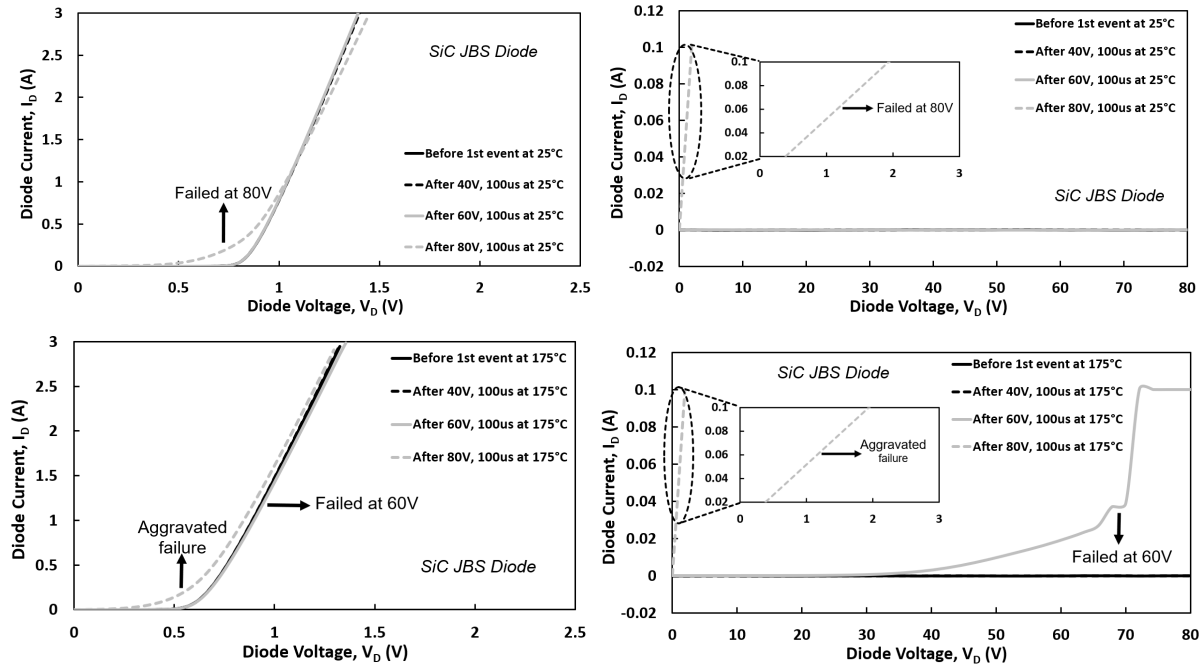

Figure 5.31: Forward I-V characteristics and reverse leakage current captured during the non-repetitive surge testing for SiC JBS diode at 25°C & 175°C.

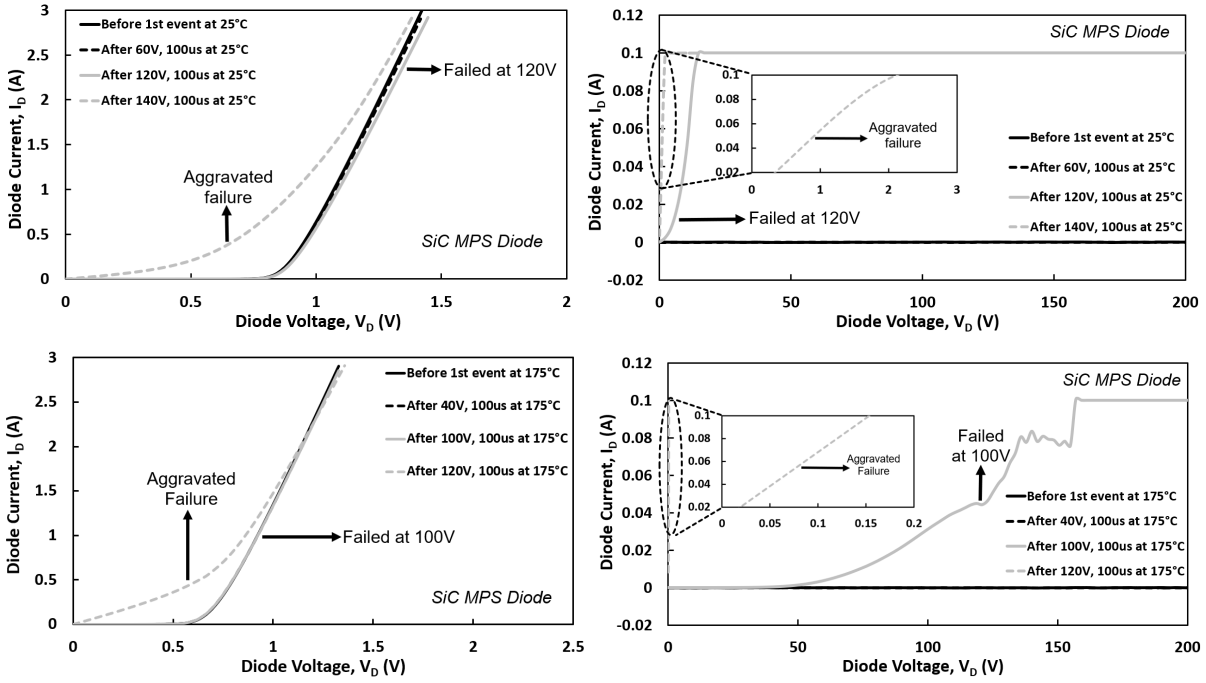

Figure 5.32: Forward I-V characteristics and reverse leakage current during the non-repetitive surge testing for SiC MPS diode at 25°C & 175°C.

Since the degradation or destruction of devices under the surge testing can be linked to high dissipated energy leading to molten metallization [66, 105], the dissipated surge energy is also calculated akin to that in UIS measurements. The critical surge energy is determined as the energy extracted from the last-pass measurement before failure of the device during the progressive surge tests as highlighted in Fig. 5.33-5.35, can be derived as:

$$E_{Surge} = \int_0^{t_{surge}} V_{diode}(t) \cdot I_{diode}(t) \cdot \mathrm{d}t \tag{5.5}$$

where t_{surge} is the time duration of surge current conduction. At low temperature, the critical Surge energy of Silicon PiN is the highest, followed by that of SiC MPS, and then that of SiC JBS diode. This is also expected from Fig. 5.24-5.26 as the SiC JBS diode failed at a lower DC-link voltage. The larger die size of Silicon PiN diode also causes a

lower current density and energy dissipation per area [109], which increase the reliability. The critical energy is found to be lower at higher temperatures. This is primarily due to the smaller difference between the junction temperature and the preset temperature making the energy dissipation more difficult. The critical energy of Silicon PiN diode is found to be lower than that of SiC MPS at elevated temperatures. This is because the thermal conductivity of SiC, which is two times higher than that of Silicon, become dominant to have a more effective heat dissipation.

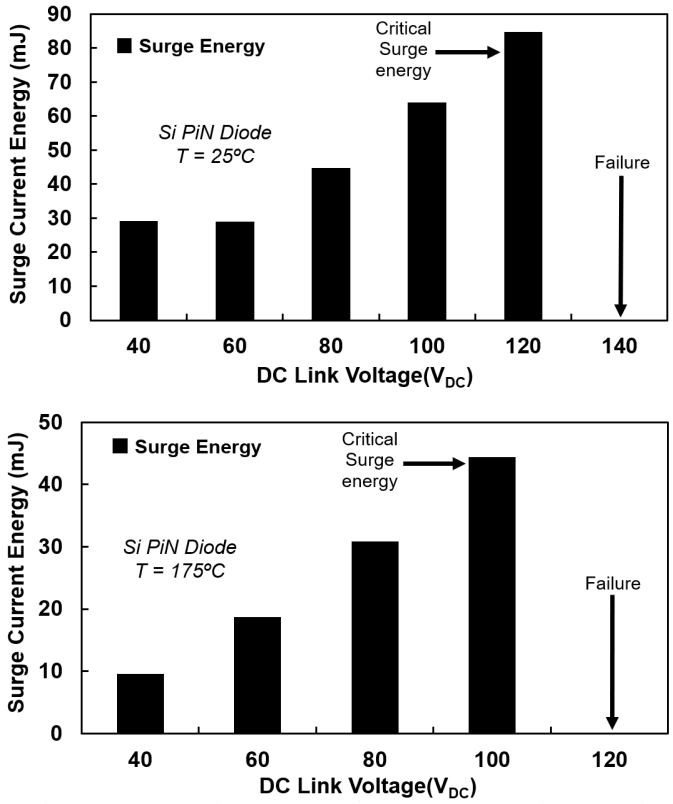

Figure 5.33: Critical surge energy for Silicon PiN diode by surges at 25°C and at 175°C.

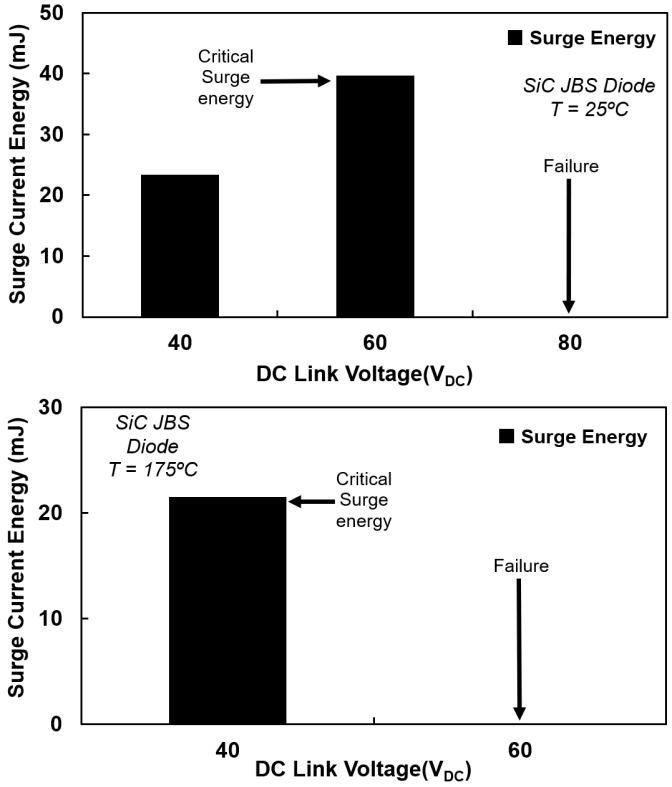

Figure 5.34: Critical surge energy for SiC JBS diode by surges at 25°C and at 175°C.

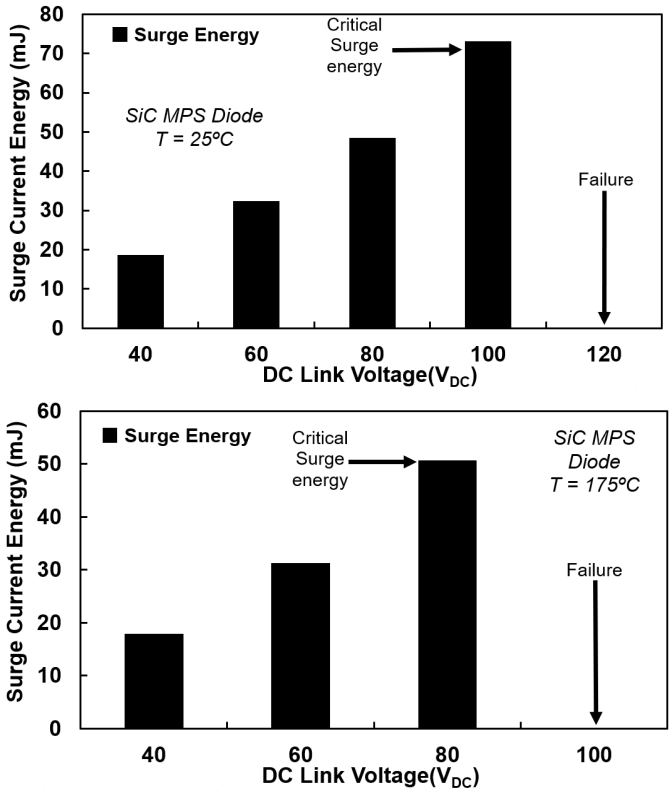

Figure 5.35: Critical surge energy for SiC MPS diode by surges at 25°C and at 175°C.

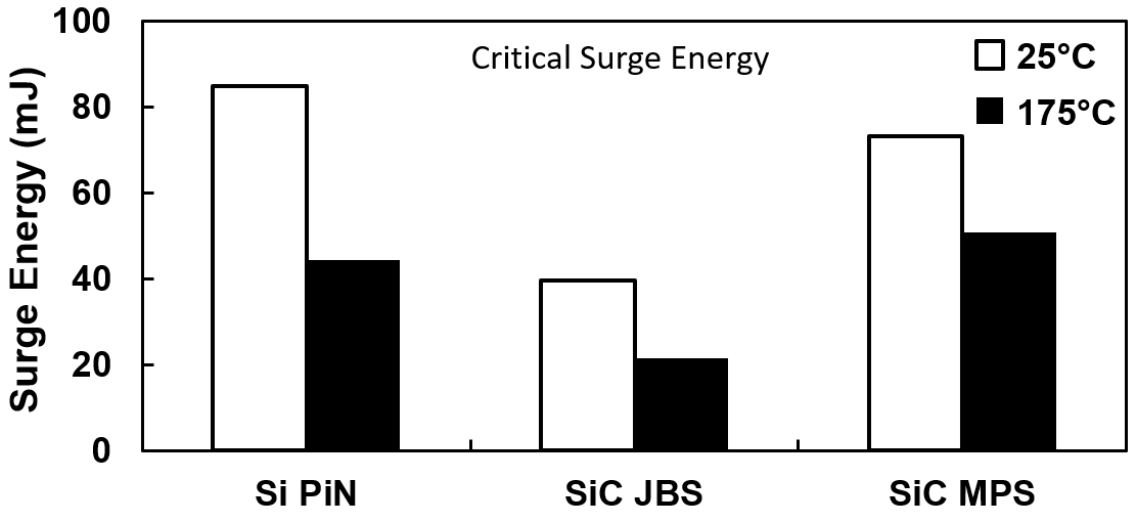

Figure 5.36: Comparison of critical surge energy for Silicon PiN, SiC JBS & SiC MPS diode at different temperatures.

For power system applications with long steady-state operation, the lack of conductivity modulation is prone to destructive consequences as the increased power dissipation can create extra heat while the negative temperature dependence of on-state resistance can lead to thermal runaway. But the minor modulation is suitable for high frequency application as the low stored charge and thus the fast-switching transient is secured. To optimise the conductivity modulation effect of the MPS diode, it is necessary to increase the minority carrier lifetime to reduce the voltage and current required to enter the high-level injection mode [9].

5.5 Summary

This chapter explores the dynamic and static performance of the commercially available SiC MPS diode together its avalanche and surge current capability by means of extensive experimental measurements, as well as to compare with its similarly rated Silicon PiN and

SiC JBS diode. In contrast to the physical expectation where conductivity modulation exists in the MPS diode, the switching performance of SiC MPS and SiC JBS diodes are superior to the Silicon PiN diode due to the low reverse recovery charge and therefore the smaller switching power loss. However, because of the high intrinsic carrier concentration in Silicon, the on-voltage of Silicon PiN diode is lower than that of SiC counterparts, while the conductivity modulation effect further reduces on-resistance at high temperatures and high currents. In contrast, a higher on-state voltage is observed in SiC JBS and MPS diode which becomes worse at high currents and high temperatures.

Although the Silicon PiN diode has the highest reverse voltage among these three power diodes, the avalanche ruggedness of SiC MPS & JBS diodes is superior to that of closely rated Silicon PiN diodes due to the less extra carries generated in wide bandgap SiC. The greater critical avalanche energy and hence better avalanche ruggedness of SiC JBS diode than SiC MPS diode can be explained by the fact that the avalanche current in SiC JBS diode is more uniformly distributed in the device active area when compared to SiC MPS diode.The poor avalanche capability at high temperatures differs from the expectation. The avalanche failure mechanism in Silicon PiN diode is primarily by the significant electric field at the junction, however in case of the SiC devices it is primarily by the excess generated heat.

As part of the surge current measurements, the forward I-V characteristic and the reverse leakage current are measured to trace diode degradation. Despite failure has been observed from the reverse characteristics of diodes, where the breakdown voltage is drastically decreased, all the devices can still conduct current in the on-state like a pure conductor. Due to the conductivity modulation effect and high thermal conductivity, SiC MPS diodes can endure electrothermal stresses that are comparable to those experienced by Si PiN diode, but SiC JBS diodes failed under a lower surge current energy.

Chapter

6 Static, Dynamic & Power Cycling of 15 kV SiC PiN Diode

The results submitted in journal paper 3 in Publications list at the outset of the thesis are used in writing of this Chapter. I acknowledge the contribution of my supervisors for laying out the specific objectives, and my co-authors on the methodology and accuracy of the analysis. I have done the Measurements at Bristol's EEMG research laboratory, analysed the results and drafted the papers.

For High Voltage (HV) applications of more than 10 kV, the better trade-off between switching losses and conduction losses can be achieved in SiC PiN diode when compared to Silicon PiN and SiC Schottky/Junction Barrier Schottky (JBS) diode [110], while the series connection of Silicon PiN chips, as illustrated in Fig. 6.1, are required to get the equal blocking capability [12,111] to the single-chip 15 kV SiC PiN diode shown in Fig. 6.2. These two commercial 15 kV PiN diodes have been CT-Scanned using a Nikon® XT H 225 ST CT-Scanner at the XTM Facility, Palaeobiology Research Group, University of Bristol and have been analyzed using the Dragonfly® software to obtain Fig. 6.1 and Fig. 6.2. The equivalent device structure of the 15 kV diode rectifier consisting of 16 series-connected Silicon PiN diodes and that of SiC PiN diode are shown in Fig. 6.3.

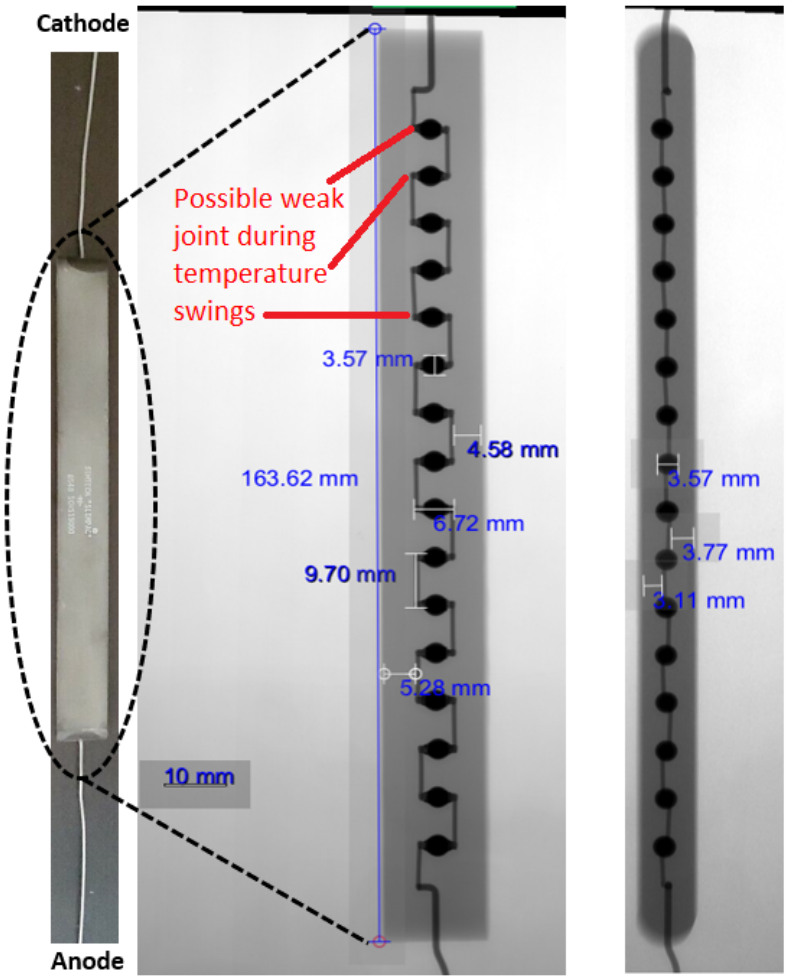

Figure 6.1: CT scan for the (left) front view and (right) side view of the 15 kV Silicon PiN rectifier SCHS15000, by Palaeobiology Research Group of University of Bristol.

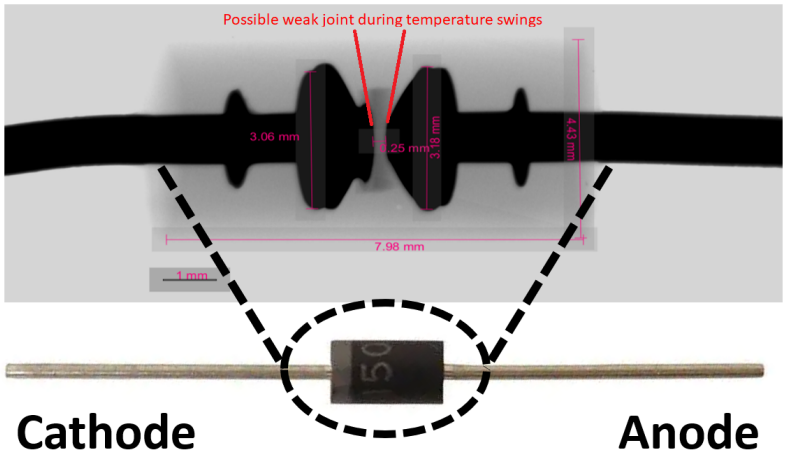

Figure 6.2: CT scan of 15 kV SiC PiN diode GA01PNS150-201, by Palaeobiology Research Group of University of Bristol.

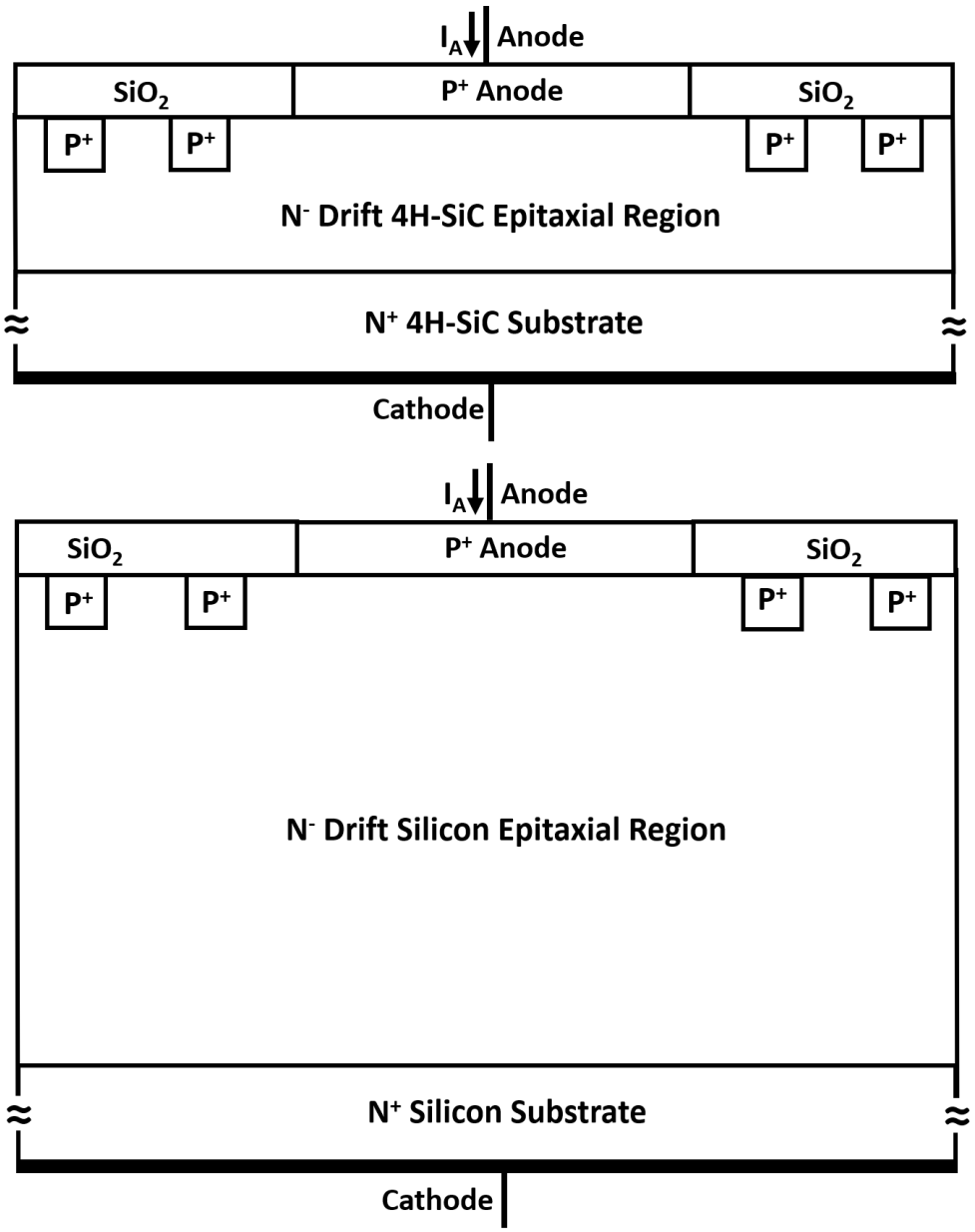

Figure 6.3: Simplified device structures for (Upper) the 15 kV SiC PiN diode GA01PNS150-201 and (Lower) the 15 kV Silicon diode rectifier SCHS15000.

15 kV SiC PiN diodes have been found to be successful for full-Bridge DC-DC converter [12, 111], which can be used for solar and wind power generation systems [112] [113] [114]. However, the electrical characteristics and the electrothermal ruggedness of

commercial 15 kV single SiC PiN diodes have not been fully studied yet, such as the conductivity modulation effect and the reliability of long-term conduction, alongside the lack of like-for-like comparison with the similarly rated Silicon counterpart. This chapter explores the static and dynamic performances of a SiC PiN single diode and compare with the similarly rated Silicon diode rectifier by means of extensive experimental measurements, together with the bipolar degradation during power cycling (repetitive current pulses) for both devices. Other preliminary power cycling tests are also conducted to explore the degradation from different material interfaces as a result of repeated temperature swings.

6.1 Dynamic Performance of 15 kV PiN Diodes

The dynamic transient performance of 15 kV Silicon and SiC PiN diode have been investigated using a double-pulse test configuration shown in Fig. 6.4, together with a 3000 V Silicon IGBT IXBH32N300 acting as a power switch, which is driven by a gate driver generating output voltage in a range between +15 V and 0 V. The design of this PCB is shown in Appendix B. The gate resistance R_G provided in Fig. 6.4 is 100 Ω. The load inductance of 35 mH and the charging pulse of 20 μs, adjusted via an Agilent 33220A 20 MHz arbitrary waveform generator, are used to provide the peak forward current of 0.5 A during this test. The voltage applied to both power devices is 800 V. This test is completed under room temperature. Table 6.1 includes the key parameters of both diodes to be used for further analysis.

The turn-off performance of both diodes is shown in Fig. 6.5. Since the power switch dominates the switching characteristic during the double pulse test, the switching rate of current and voltage of Silicon and SiC device are almost same. As also indicated in this

figure, the reverse recovery process of Silicon PiN diode leads to extra turn-off time while the minimal stored charge in their SiC counterparts accelerate the recovery process and thus the device switches faster. This is due to the much smaller dimension of the SiC PiN diode as well as the low minority carrier lifetime in SiC.

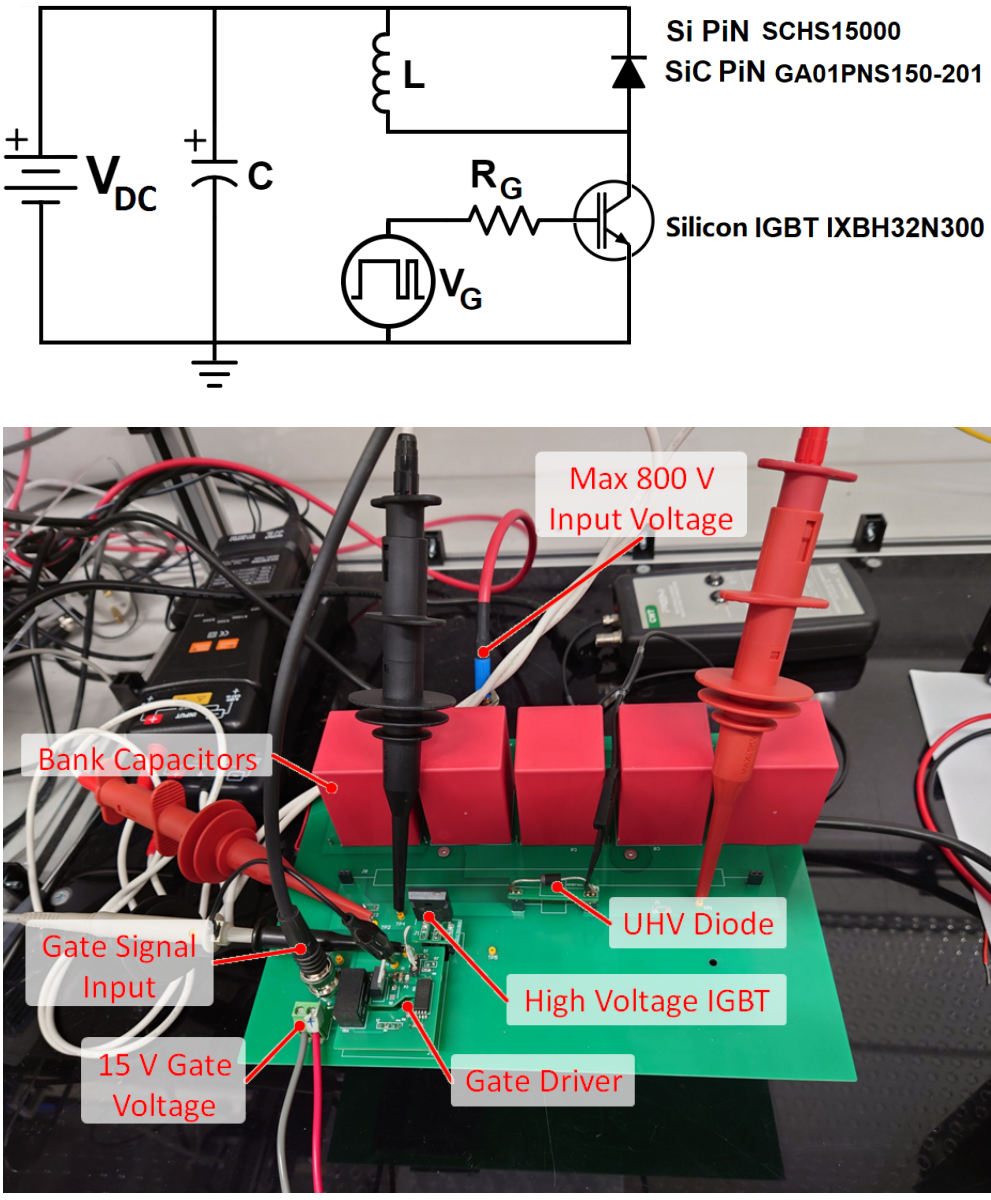

Figure 6.4: Double pulse set-ups for 15 kV Silicon and SiC diode.

Table 6.1: Features of the 15 kV Silicon PiN & 15 kV 4H-SiC PiN diode.

	15 kV Silicon PiN	15 kV SiC PiN
Model	SCHS15000	GA01PNS150-201
Manufacture	SEMTECH	GeneSiC
Blocking Voltage	15,000 V	15,000 V
Forward Current	2 A	1 A

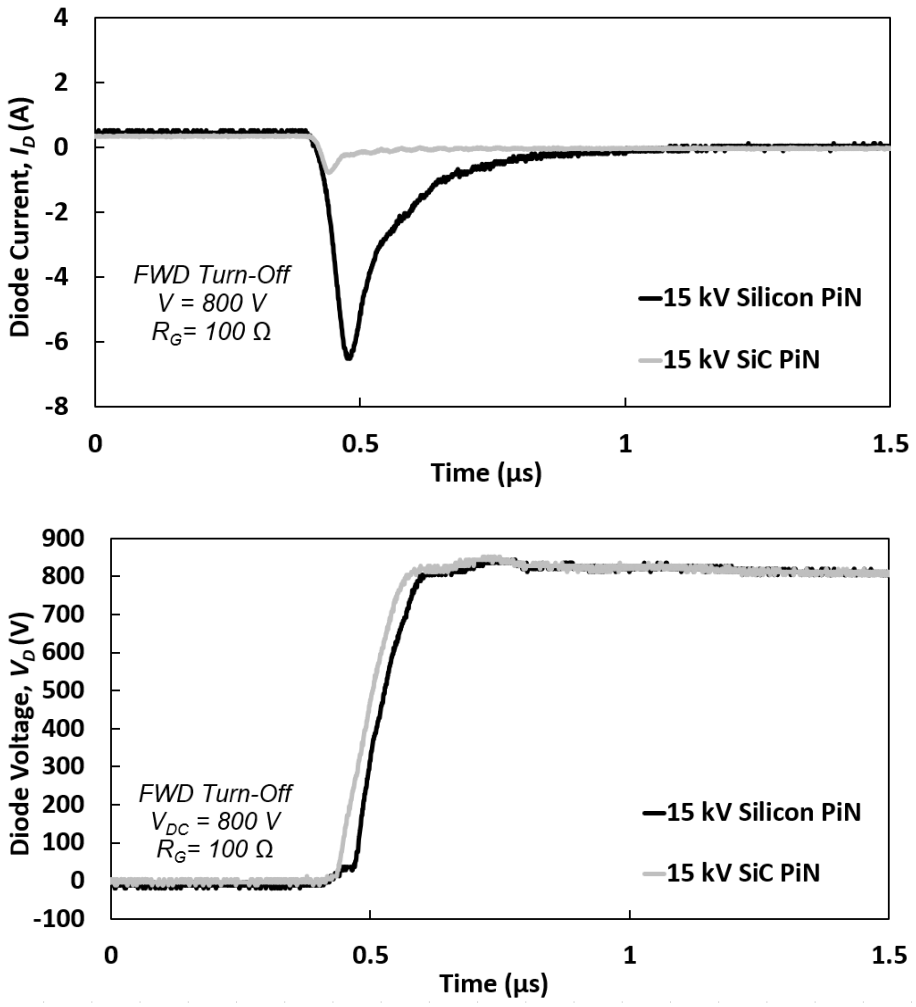

Figure 6.5: (Upper) Diode current and (Lower) diode voltage at turn-off for both 15 kV devices under DC link voltage of 800 V.

6.2 Static Performance of 15 kV PiN Diodes

6.2.1 Conductivity Modulation and Self-heating

In this case, both power diodes conduct a constant heating current for 3 second, ranged from 0 to 1 A in 0.25 A increments. All static tests are completed under room temperature. The ELC ALR3206D power supply is directly connected to devices under test (DUT) to supply the heating current.

Fig. 6.6 shows the voltage drop of both diodes during the self-heating. Although the on-state voltage of conventional SiC devices was deemed to be higher than that of Silicon because of the wide bandgap, the forward voltage of 15 kV Silicon diode rectifier is larger than that of SiC PiN diode. This is because the 16 series connected Silicon PiN diodes, as can be seen in Fig. 6.1, are required to achieve high blocking voltage, in contrast to a single die installed in the SiC PiN diode. The conductivity modulation effect is observed in both devices since the less voltage increment is observed after 1 second at higher currents because of the reduced equivalent on-state resistance. This is also illustrated in Table 6.2. It can be seen that both devices undergo similar conductivity modulation during the rise of forward current though the stored charge in SiC devices is much smaller. The negative temperature dependence of forward voltage during the self-heating is observed for both devices. This is because the positive temperature coefficient of the intrinsic carrier concentration leads to the decrease of the junction voltage [78].

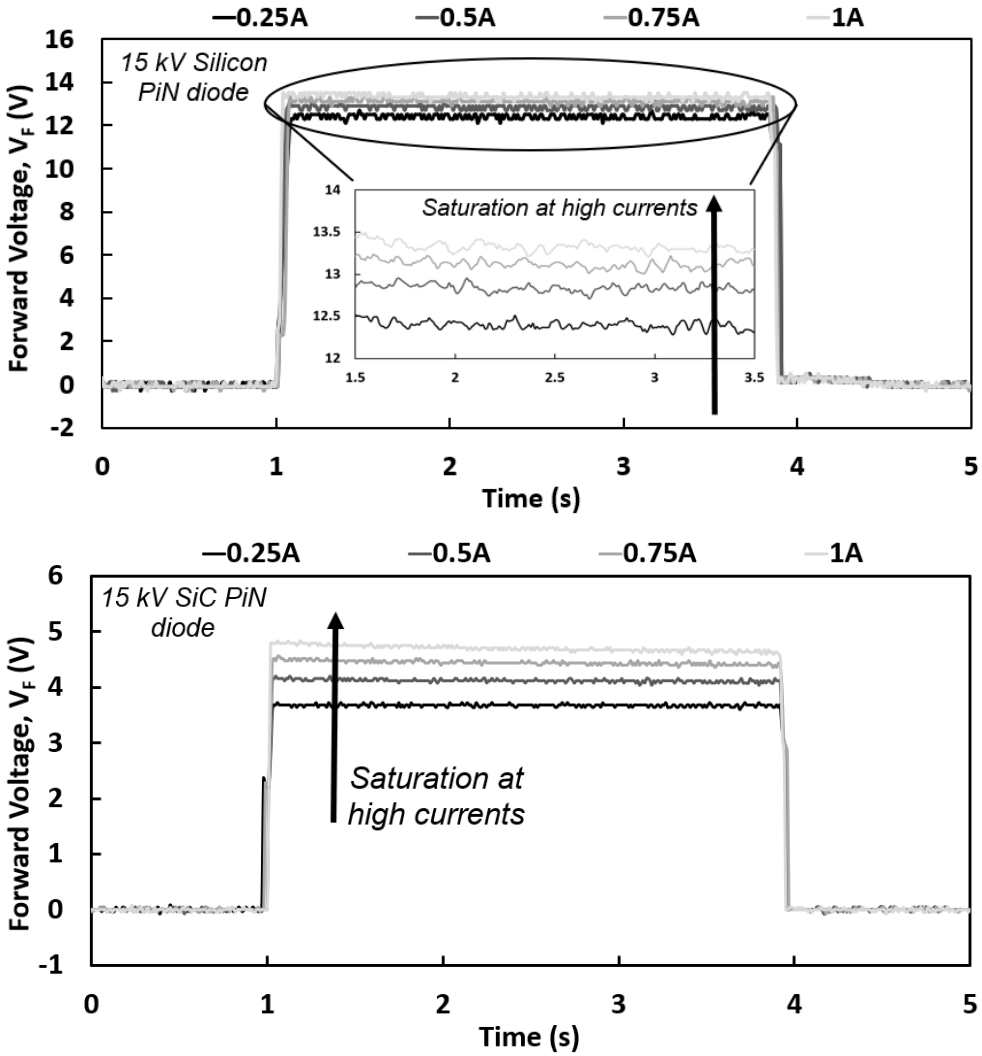

Figure 6.6: Forward voltage during self-heating for (Upper) 15 kV Silicon PiN and (Lower) SiC PiN diode at various current levels.

Table 6.2: The reduction of equivalent on-resistance at 1 second for both devices when compared to their 0.25 A case as the reference.

	15 kV Silicon PiN	15 kV SiC PiN
0.5 A	47.90%	43.6%
0.75 A	64.51%	59.15%
1 A	72.90%	67.41%

6.2.2 Static Performance Under a Range of Temperatures

A B2902A Source/Measure Unit (SMU) is used to capture both the forward I-V characteristic and the reverse leakage current of both diodes under chamber temperature increased from −50°C to 150°C by increments of 25-degrees using a TAS LTCL600 climatic test chamber. The junction temperature (T_j) of both devices is assumed to be the same as the chamber temperature since they were heated or cooled for one hour before the measurements. This SMU has the capability to supply and measure both voltage and current with the maximum output up to 210 V and 1.515 A. The maximum current is set to 1 A to ensure operation within the safe limits.

Fig. 6.7 shows the I-V characteristic of both diodes. It is clearly observed that the forward voltage of Silicon PiN diode is higher which is in line with that in Fig. 6.6. At high temperatures, the built-in voltage is found to decrease with the increase of intrinsic carrier concentration, while the much smaller intrinsic carrier concentration in SiC device leads to the less reduction of the built-in voltage. In addition, the increasing free carrier at elevated temperatures further reduce the on-resistance and thus promote the conductivity modulation effect because of the increase in diffusion length with temperature [1]. Fig. 6.8 shows the reverse leakage current of both diodes. The lower reverse leakage current of SiC device is because of the much smaller drift region and the much smaller intrinsic carrier concentration. At high temperatures, the positive temperature dependence of the intrinsic carrier concentration leads to the surge of leakage current in both PiN diodes.

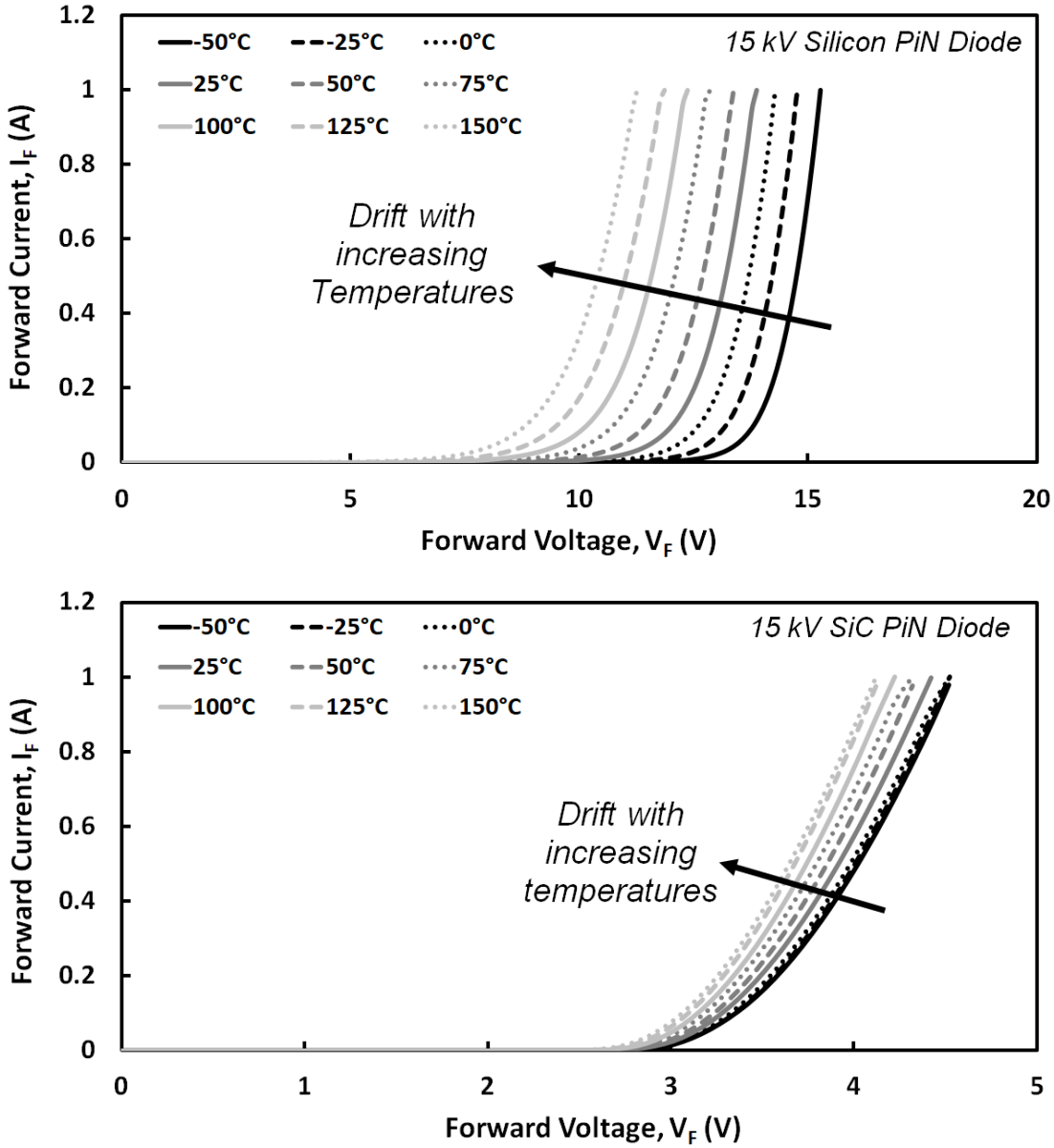

Figure 6.7: I-V characteristics for 15 kV (Upper) Silicon PiN, (Lower) SiC PiN diode under different junction temperatures.

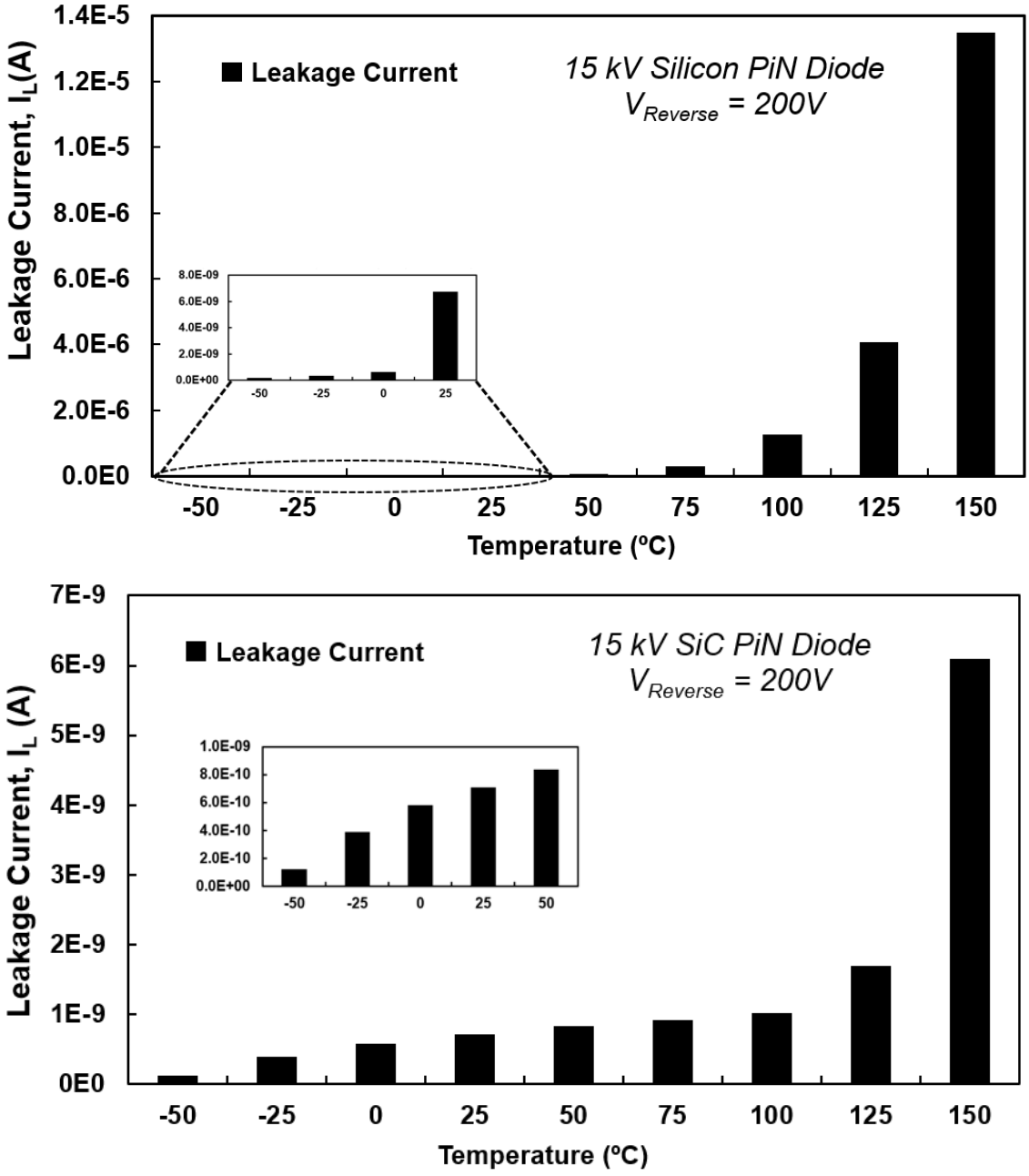

Figure 6.8: Reverse leakage current as a function temperature for 15 kV (Upper) Silicon PiN and (Lower) SiC PiN diode reverse voltage of 200 V.

6.3 Power Cycling Tests

As mentioned in Section 2.4.4.1, bipolar degradation is one of the long-term reliability issues of SiC bipolar devices. In this section, power cycling (repetitive current pulses) tests are performed to evaluate this issue for commercially available 15 kV Silicon and SiC PiN diode. The caused degradation arises due to high temperature during long-term operation. Repetitive current pulses are also applied to evaluate the other reliability of these diodes, where the die-to-package interfaces may suffer degradation when significant temperature swings are applied, as will be discussed in Section 6.3.2.

6.3.1 Bipolar Degradation via Power Cycling

SMU directly provides 1 A heating current to both PiN diodes with a pre-defined duty cycle with constant heating and cooling time, as can be seen in Fig. 6.9 and 6.10. Devices cool down as the heating current is removed.

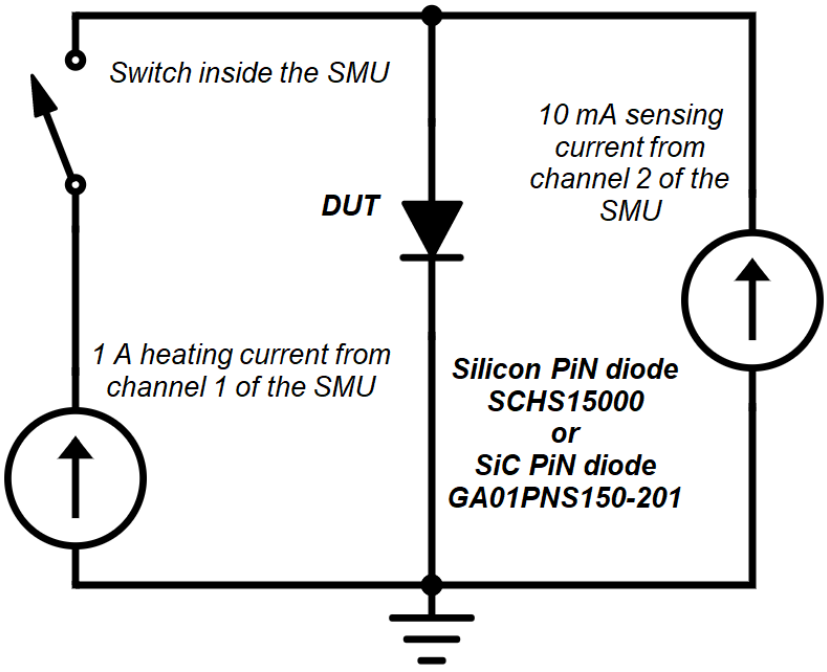

Figure 6.9: Power cycling test circuit for 15 kV PiN diodes.

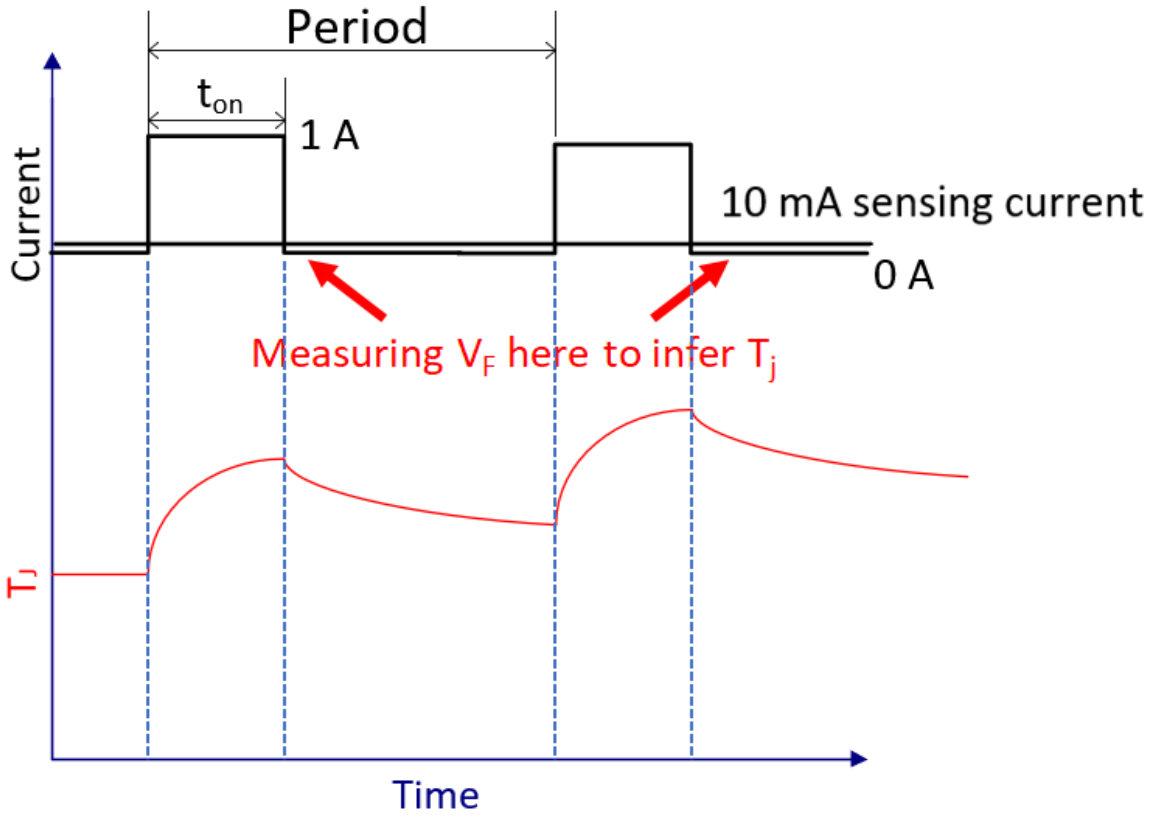

Figure 6.10: The variation of junction temperature during power cycling.

Unlike conventional power cycling schemes in [115], the junction temperature keeps rising until it reaches a saturated value. During this process, minor temperature swings are caused as can be seen from the lower portion of Fig. 6.10. The high junction temperature during power cycling leads to accelerated degradation, and potentially failure. The detailed test plans can be found in Table 6.3 to mimic the real operation of the PiN diode in a high voltage converter. The increase of duty cycle and cycle numbers lead to the rise of the peak temperature and the prolonged test duration separately.

Table 6.3: Test plan to evaluate high temperature reliability for 15 kV PiN diodes. All tests are conducted with sensing current of 10 mA except test 18.

Test number	t_{on}(ms)	Period (ms)	Cycle number
Test 1	10	100	100
Test 2	10	100	200
Test 3	20	200	100
Test 4	20	200	200
Test 5	100	1000	100
Test 6	100	1000	200
Test 7	100	1000	500
Test 8	200	2000	200
Test 9	200	2000	500
Test 10	200	2000	1000
Test 11	500	2000	200
Test 12	500	2000	500
Test 13	500	2000	1000
Test 14	500	1000	1000
Test 15	1000	2000	1000
Test 16	2000	2500	1000
Test 17	2000	4000	1000
Test 18 (100 mA)	2000	4000	1000
Test 19	2000	4000	2000
Test 20	3000	4000	1000

Since it is difficult to directly measure the junction temperature of these fully isolated packaged devices, it is common practice to measure the forward voltage of diode which

is a temperature-sensitive electrical parameter (TSEP), i.e., a continuous 10 mA sensing current is also applied to monitor the forward voltage of both devices immediately after t_{on}, as shown in Fig. 6.9 and Fig. 6.10, and to infer the instantaneous device junction temperature. Typical current and voltage waveform for both devices during cycling test 16 are shown in Fig. 6.11. To properly calculate the junction temperature, the forward voltage immediately after each heating pulse is measured to exclude the impact of cooling. This sensing current is small enough to avoid any other impacts on the cycling test.

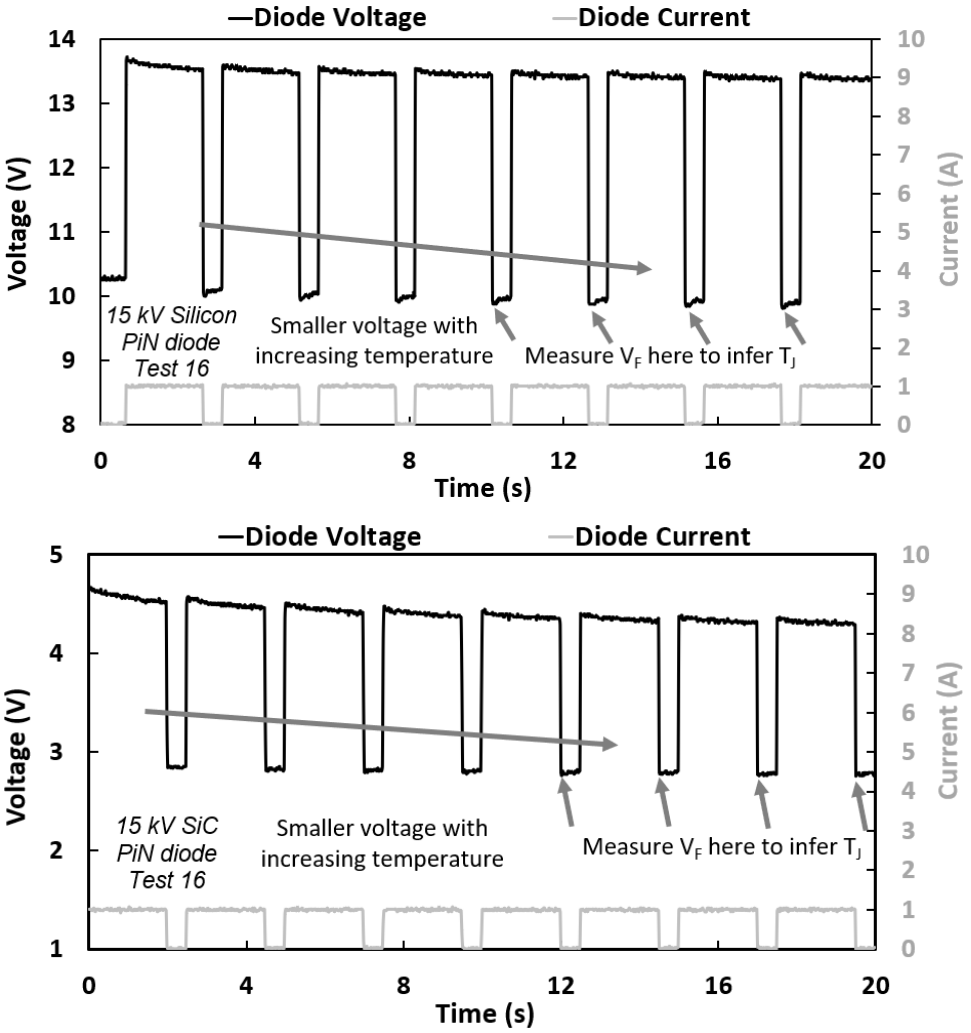

Figure 6.11: The variation of forward voltage and DC heating current during cycling test 16 for 15 kV (Upper) Silicon and (Lower) SiC PiN diode.

The forward voltage needs to be calibrated in advance to facilitate calculating junction temperature during the cycling test. To create these calibration curves, both PiN diodes were placed in the climatic chamber to obtain the forward voltage with sensing current of 10 mA and 100 mA separately under various chamber temperatures increased from 25°C to 150°C in 25-degree increments. The junction temperature of both devices is assumed to be the same as the chamber temperature since they were heated or cooled for one hour before the measurement started.

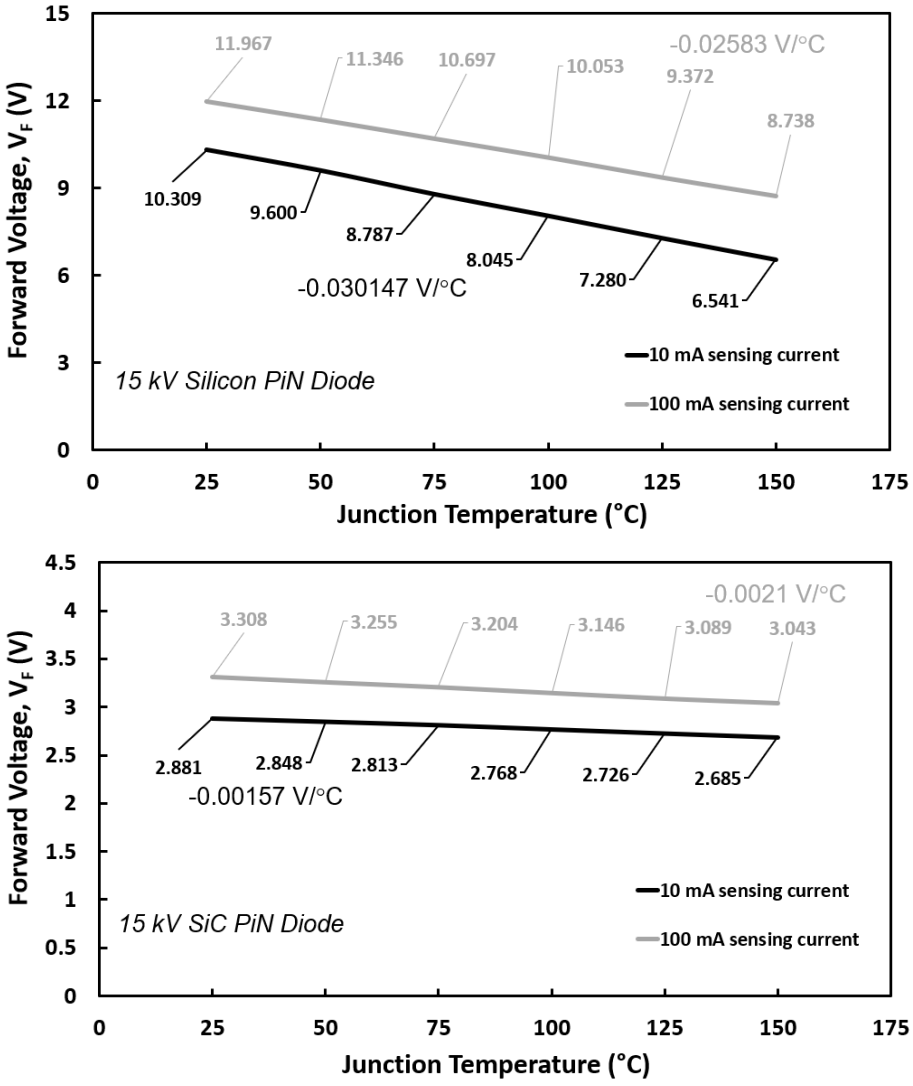

Figure 6.12: Calibration of the on-state voltage as TSEP at low currents for the 15 kV (Upper) Silicon and (Lower) SiC PiN diode.

The calibration curves in Fig. 6.12 show the less temperature dependence of SiC diode than Silicon counterparts. This is an issue for measuring the junction temperature of SiC PiN diode because the ringing in forward voltage leads to more significant error when compared to that in Silicon PiN diode. Nevertheless, the larger sensing current results in the higher junction temperature in test 18 than that in test 17, as illustrated in Fig. 6.30 and Fig. 6.48. This was then reduced back to 10 mA for test 19 and test 20.

SMU is also used to capture the forward I-V characteristic of both diodes to trace degradations and detect failure during power cycling tests. During these cycling tests, severe degradation on forward I-V characteristics have been found after test 16 as shown in Fig. 6.13. Cycling test continues to investigate the impact of the duration of high temperatures on bipolar degradation. Based upon the calibration curves, the estimated junction temperature for both devices during cycling test 1, test 4, test 7, test 10, test 13, test 16, test 17, test 18 and test 20 can be found from Fig. 6.14 to 6.31.

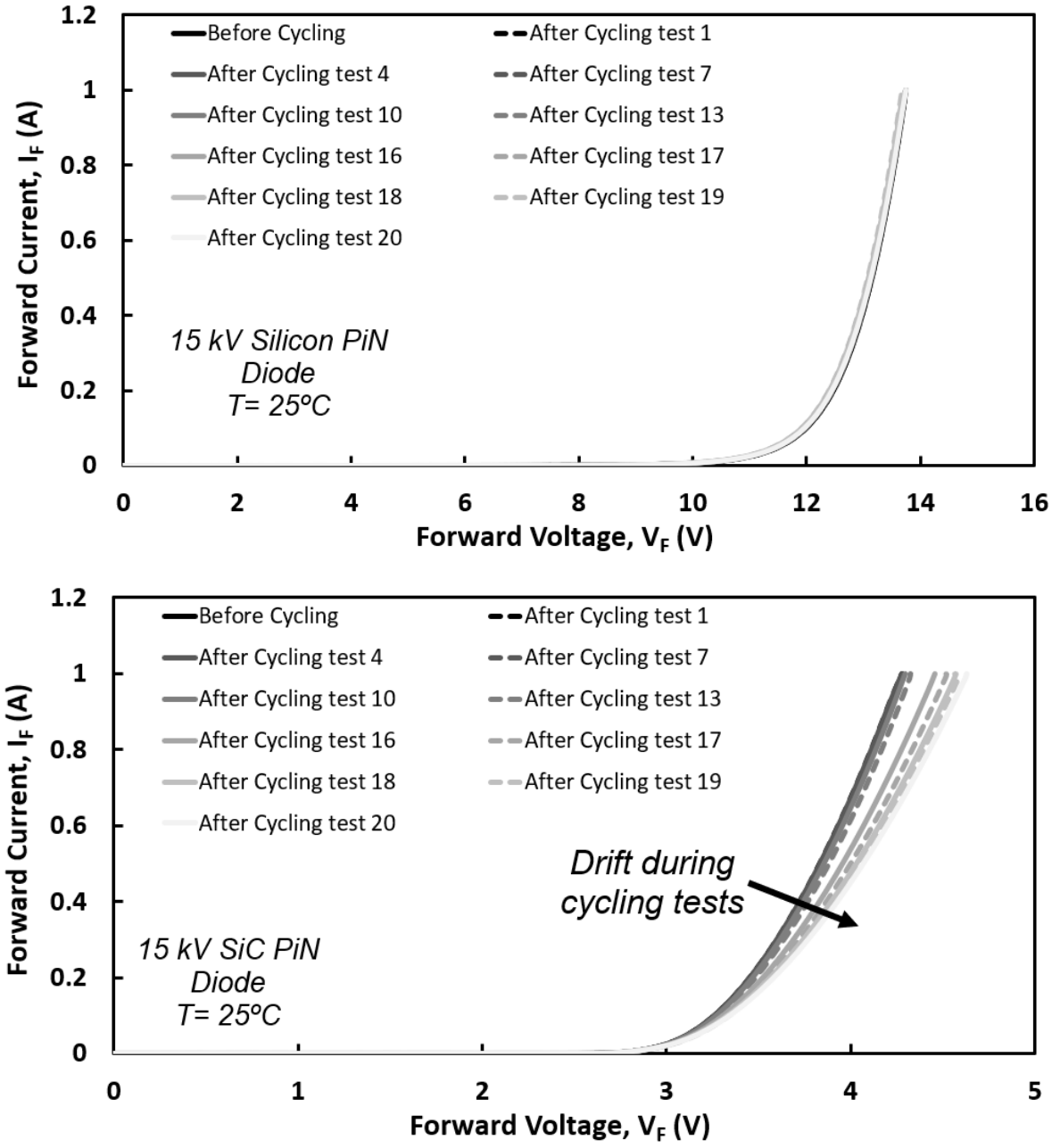

Figure 6.13: Forward I-V characteristics after each cycling test for (Upper) 15 kV Silicon PiN diode and (Lower) 15 kV SiC PiN diode.

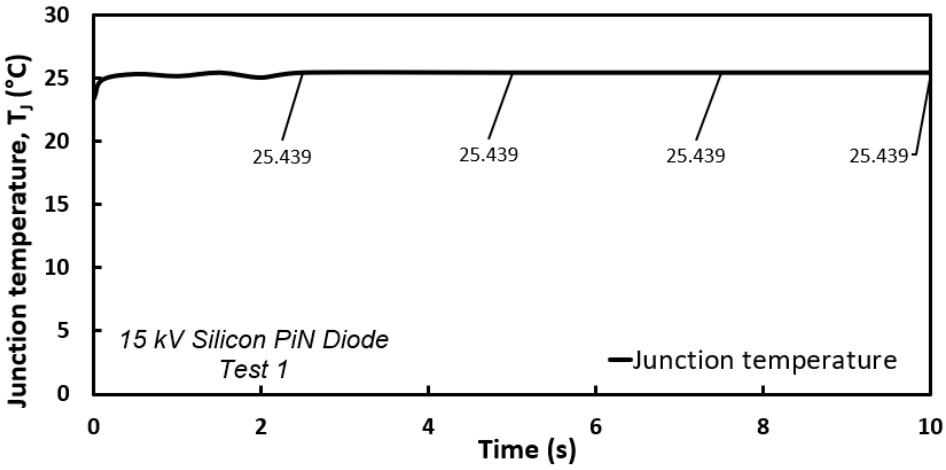

Figure 6.14: Estimated junction temperature of 15 kV Silicon PiN diode during test 1.

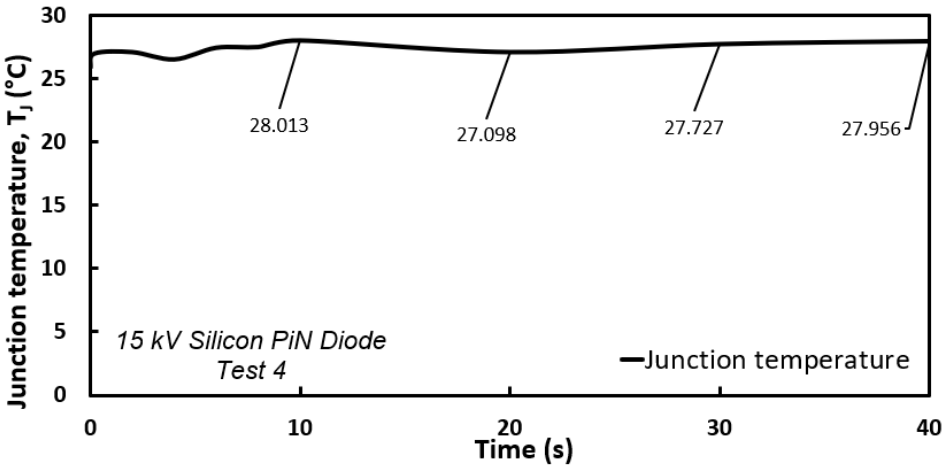

Figure 6.15: Estimated junction temperature of 15 kV Silicon PiN diode during test 4.

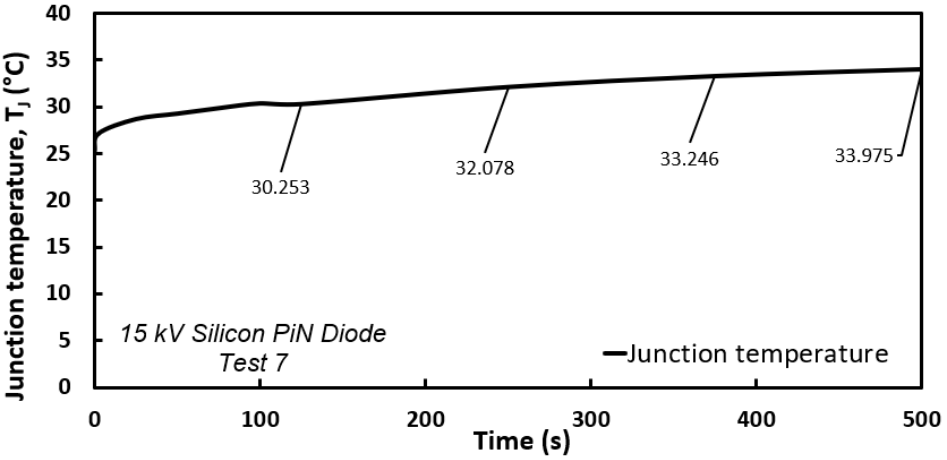

Figure 6.16: Estimated junction temperature of 15 kV Silicon PiN diode during test 7.

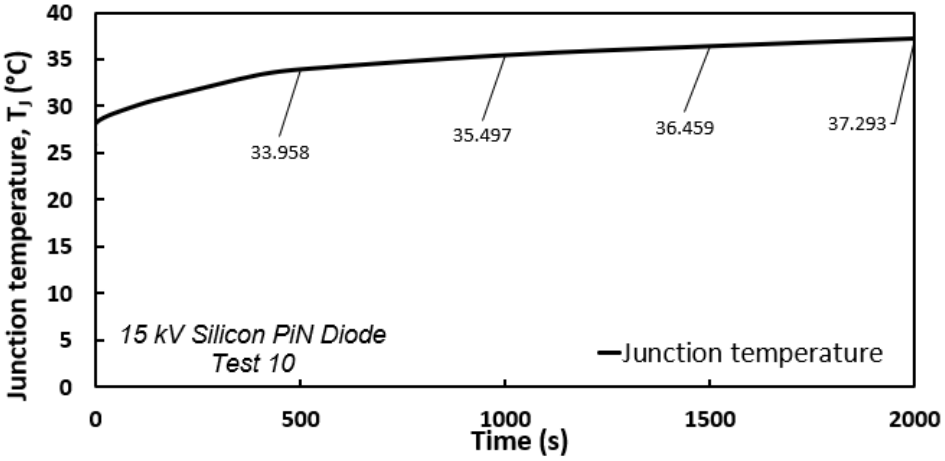

Figure 6.17: Estimated junction temperature of 15 kV Silicon PiN diode during test 10.

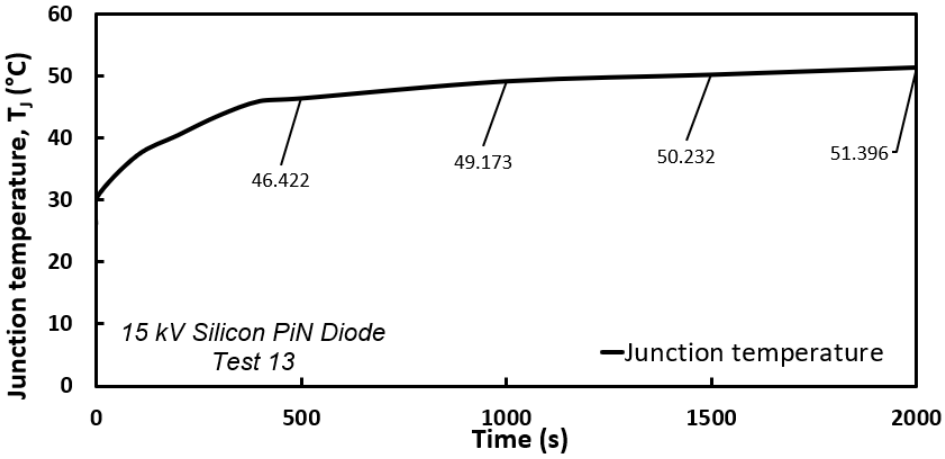

Figure 6.18: Estimated junction temperature of 15 kV Silicon PiN diode during test 13.

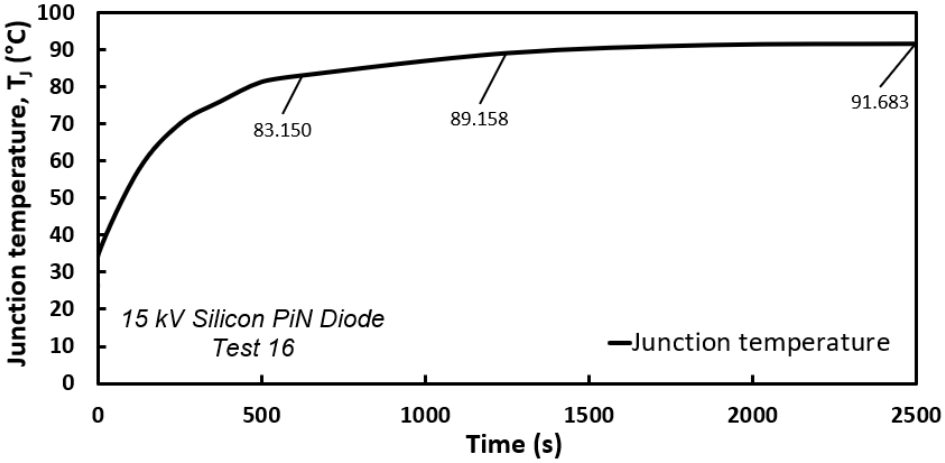

Figure 6.19: Estimated junction temperature of 15 kV Silicon PiN diode during test 16.

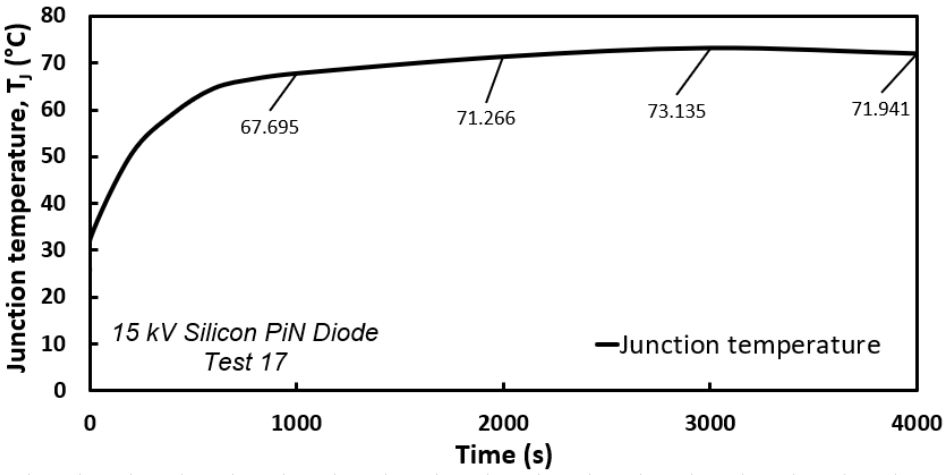

Figure 6.20: Estimated junction temperature of 15 kV Silicon PiN diode during test 17.

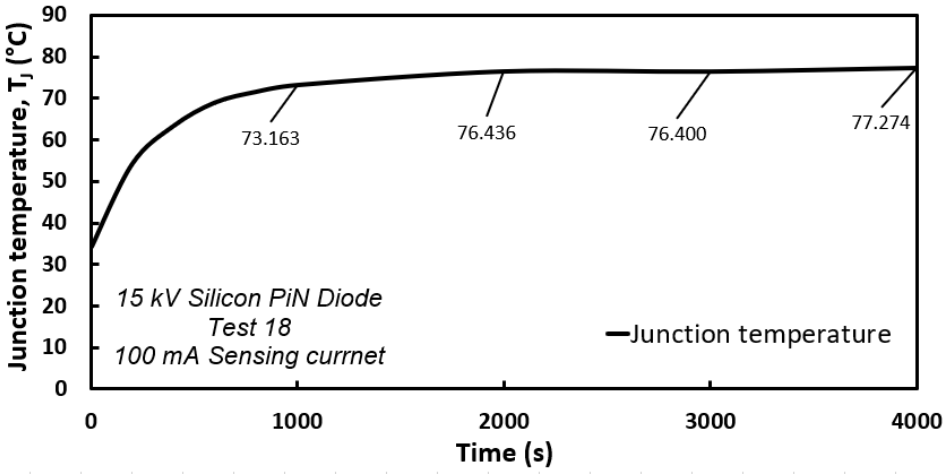

Figure 6.21: Estimated junction temperature of 15 kV Silicon PiN diode during test 18.

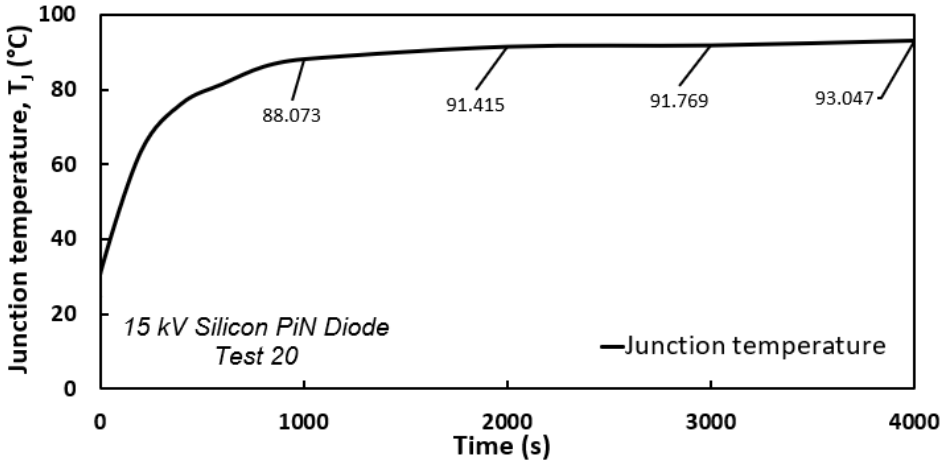

Figure 6.22: Estimated junction temperature of 15 kV Silicon PiN diode during test 20.

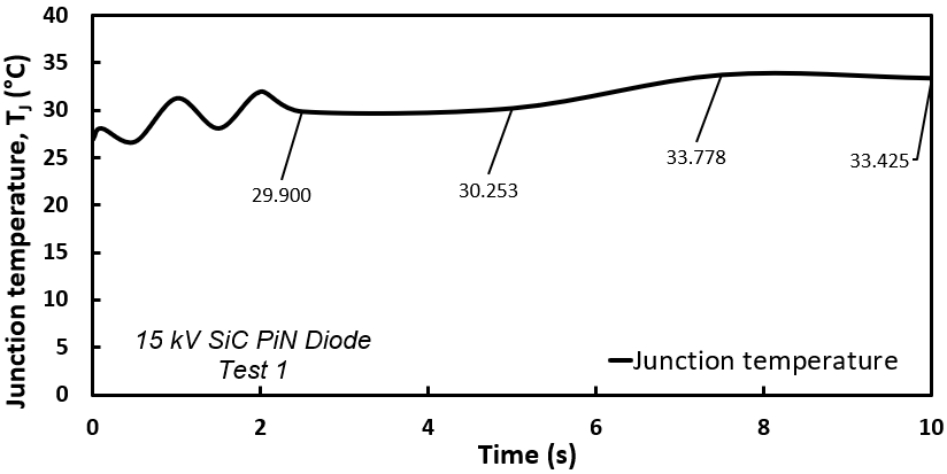

Figure 6.23: Estimated junction temperature of 15 kV SiC PiN diode during test 1.

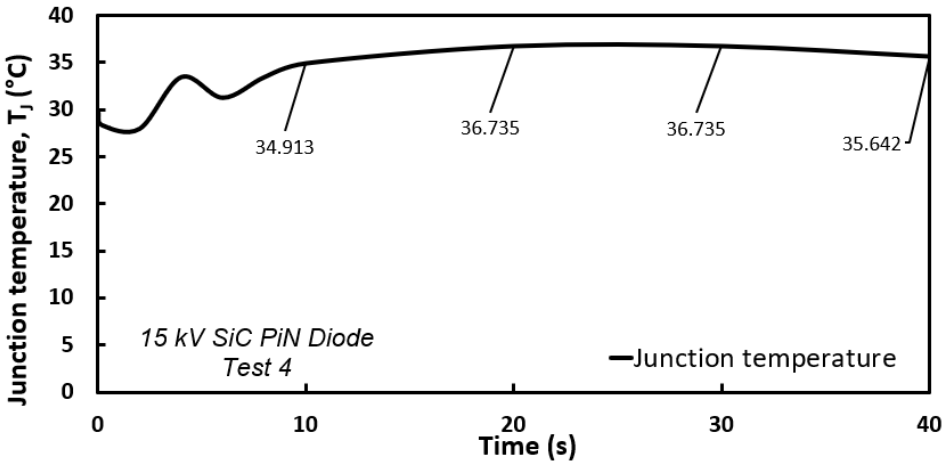

Figure 6.24: Estimated junction temperature of 15 kV SiC PiN diode during test 4.

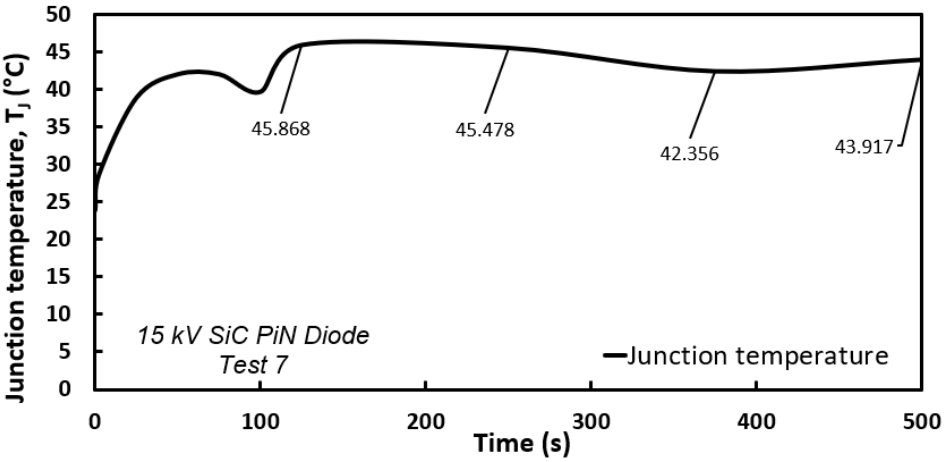

Figure 6.25: Estimated junction temperature of 15 kV SiC PiN diode during test 7.

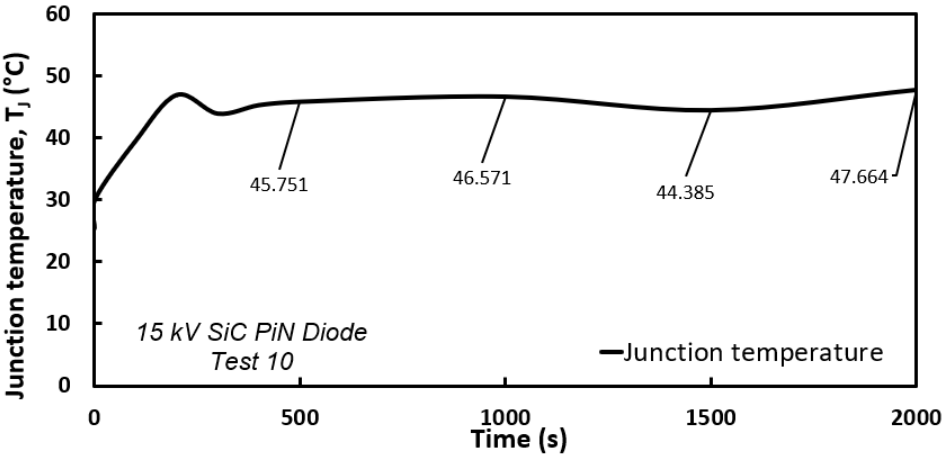

Figure 6.26: Estimated junction temperature of 15 kV SiC PiN diode during test 10.

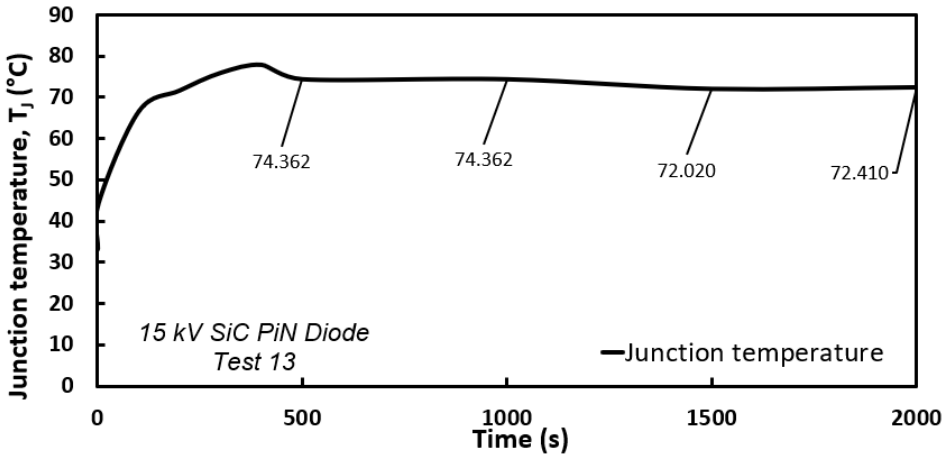

Figure 6.27: Estimated junction temperature of 15 kV SiC PiN diode during test 13.

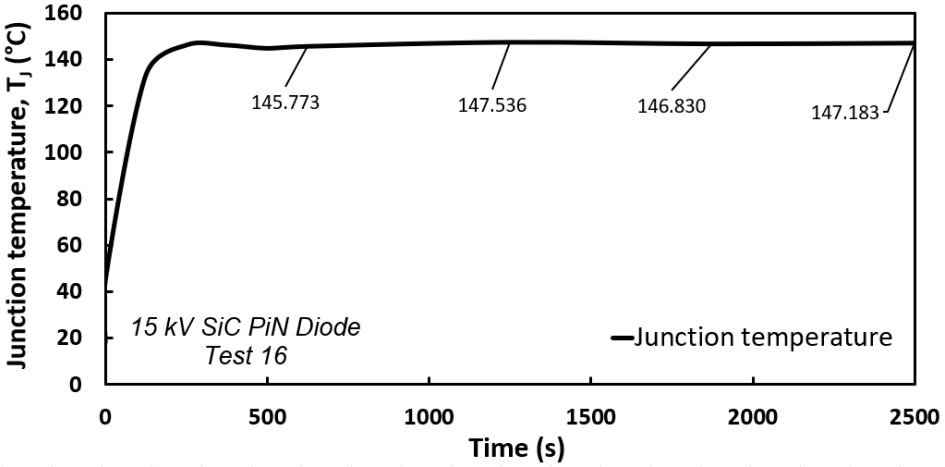

Figure 6.28: Estimated junction temperature of 15 kV SiC PiN diode during test 16.

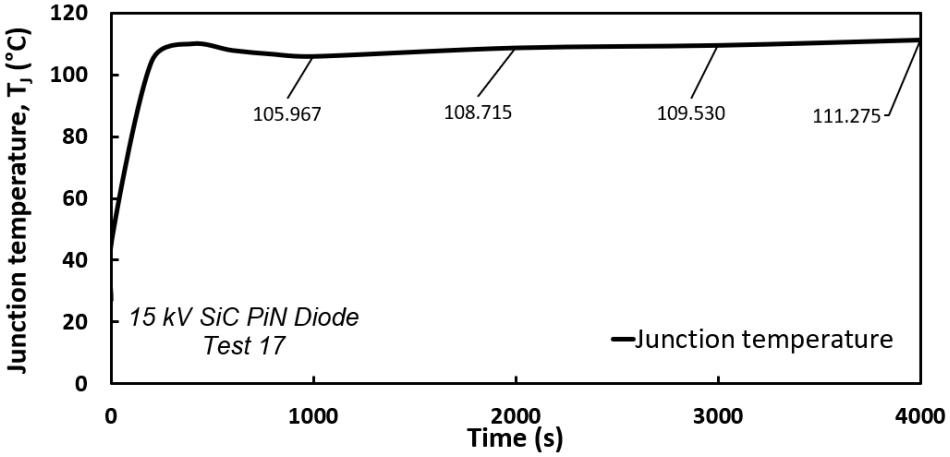

Figure 6.29: Estimated junction temperature of 15 kV SiC PiN diode during test 17.

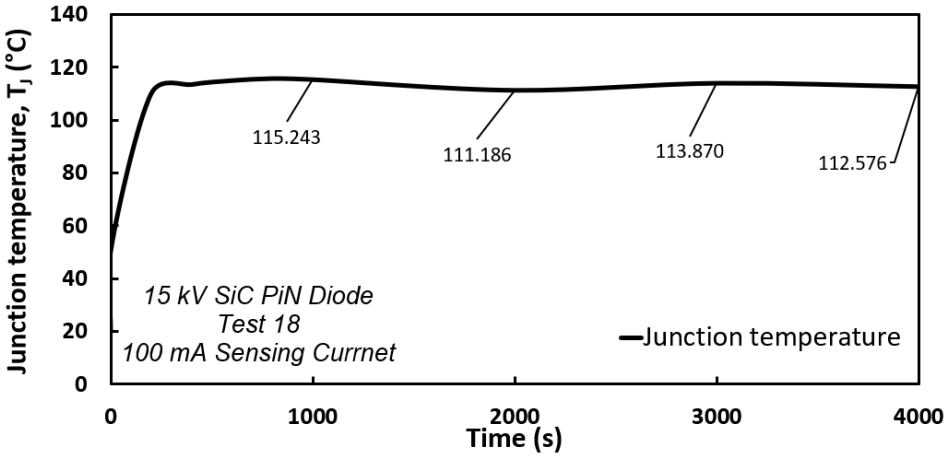

Figure 6.30: Estimated junction temperature of 15 kV SiC PiN diode during test 18.

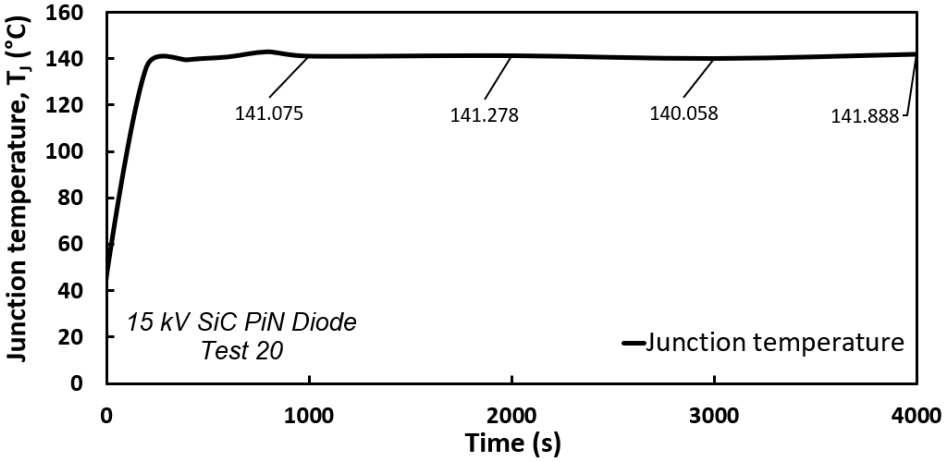

Figure 6.31: Estimated junction temperature of 15 kV SiC PiN diode during test 20.

It can be seen that the junction temperature in both diodes saturates after a certain number of power cycles since the generation and extraction of heat balances out. The low ramp rate and the low saturated value of the junction temperature in the 15 kV Silicon PiN diode are primarily due to the larger thermal resistance and thermal capacitance in the Silicon device. Additionally, each Silicon PiN chip inside the whole Silicon rectifier has low forward voltage and thus low power dissipation. The strong negative temperature dependence of the diode voltage leads to the reduction of the internal power dissipation at elevated temperatures. Although the saturated temperature in test 17 is small when compared with test 16, the elongated test duration leads to the larger thermal stress and thus aggravated ageing on I-V characteristics for SiC PiN diode. This is also true for test 20.

In order to validate the estimation of junction temperature in both PiN diodes, the case temperature of both power devices during aforementioned tests are monitored via infrared camera FLIR E5-XT, as can be found in Fig. 6.32 to 6.49. The higher case temperature in SiC PiN diode is in agreement with those of junction temperature in Fig. 6.14 to 6.31.

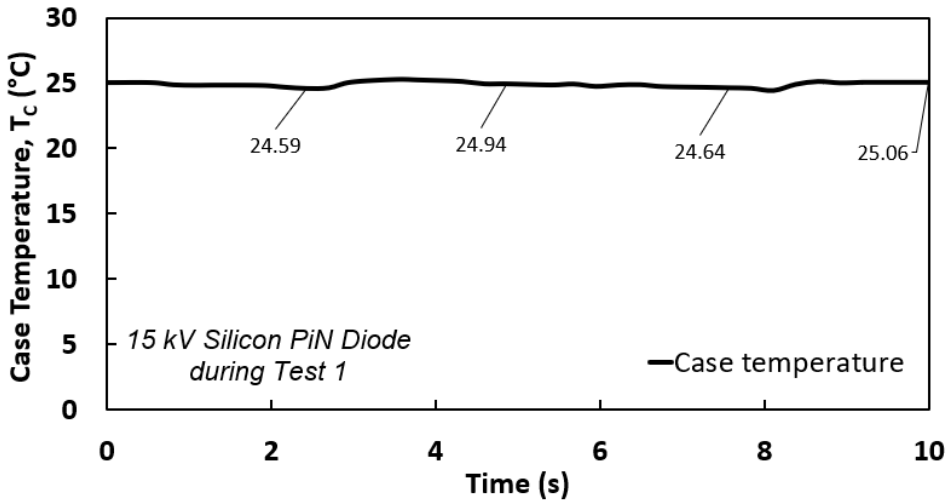

Figure 6.32: Case temperature of 15 kV Silicon PiN diode during test 1.

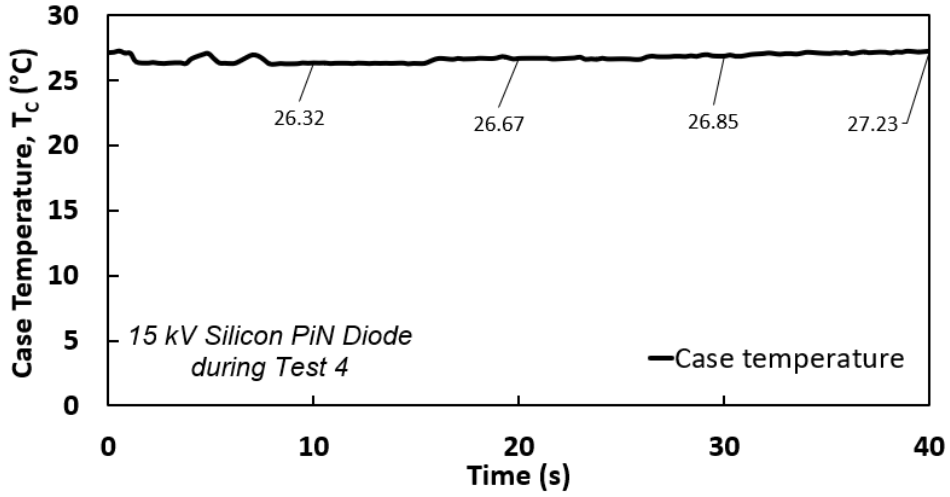

Figure 6.33: Case temperature of 15 kV Silicon PiN diode during test 4.

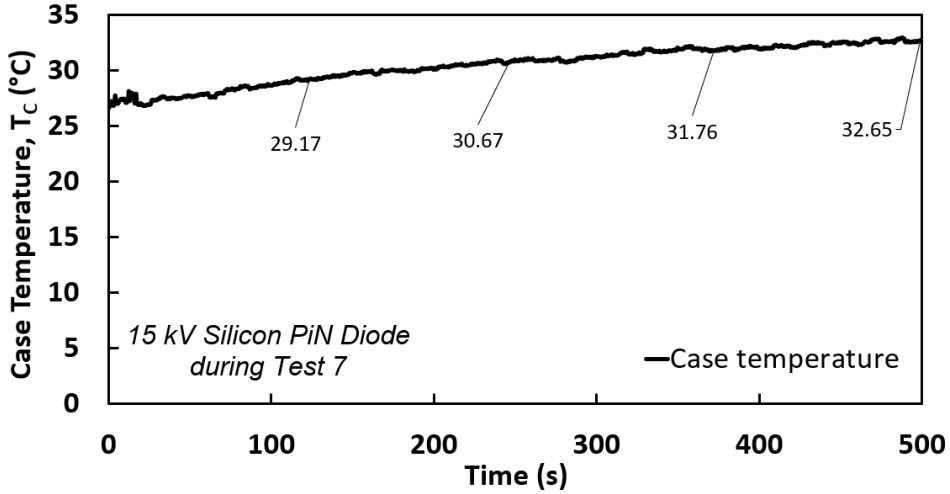

Figure 6.34: Case temperature of 15 kV Silicon PiN diode during test 7.

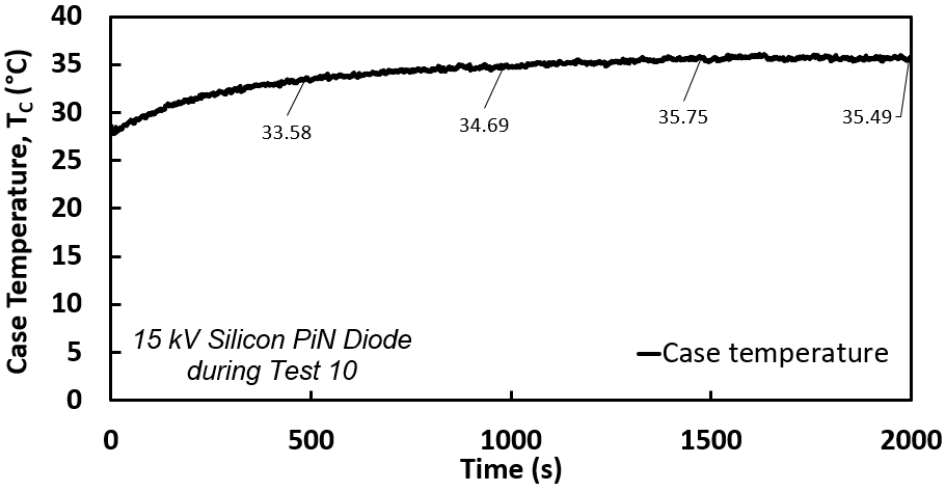

Figure 6.35: Case temperature of 15 kV Silicon PiN diode during test 10.

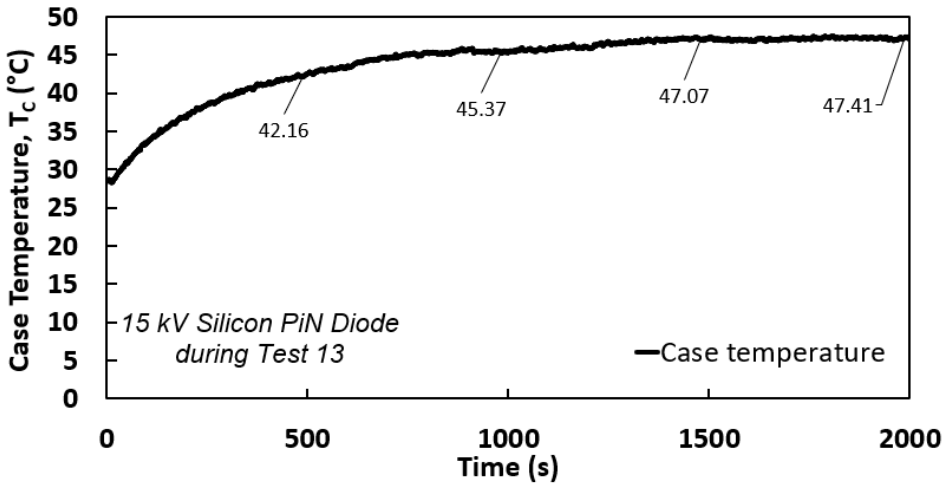

Figure 6.36: Case temperature of 15 kV Silicon PiN diode during test 13.

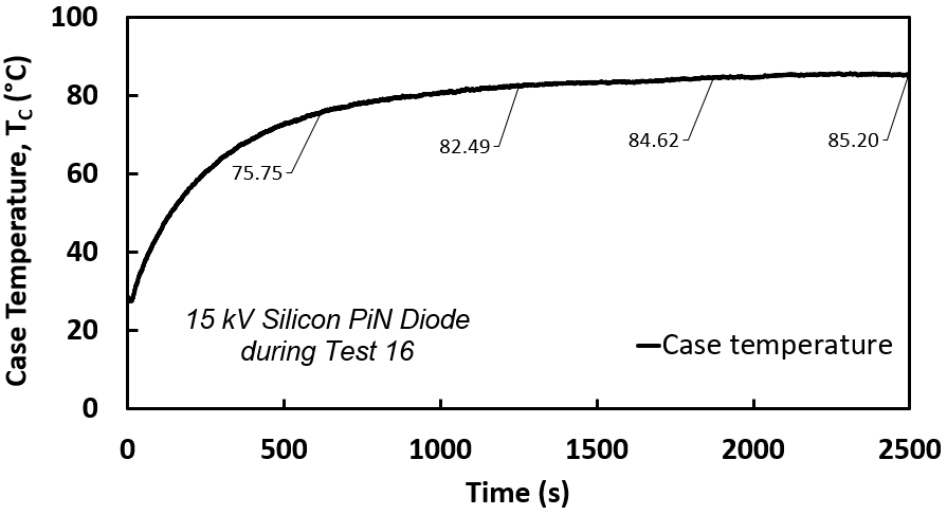

Figure 6.37: Case temperature of 15 kV Silicon PiN diode during test 16.

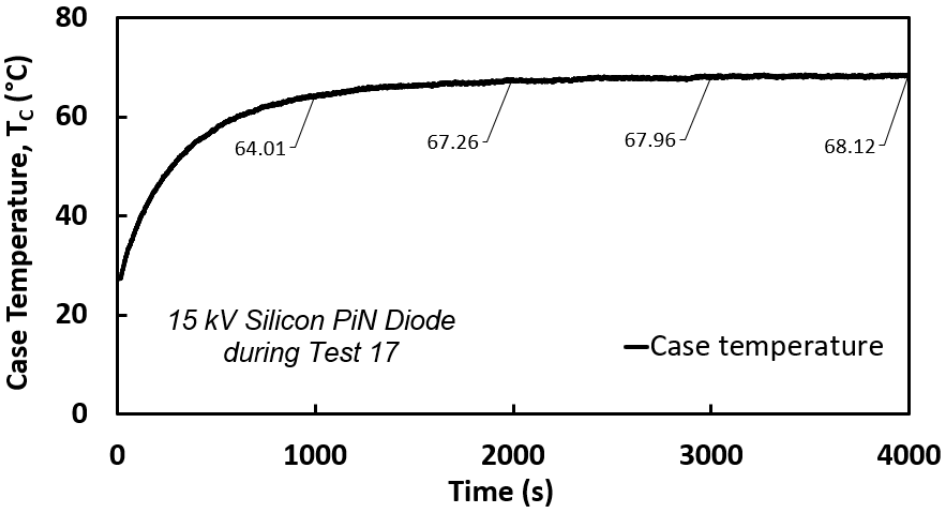

Figure 6.38: Case temperature of 15 kV Silicon PiN diode during test 17.

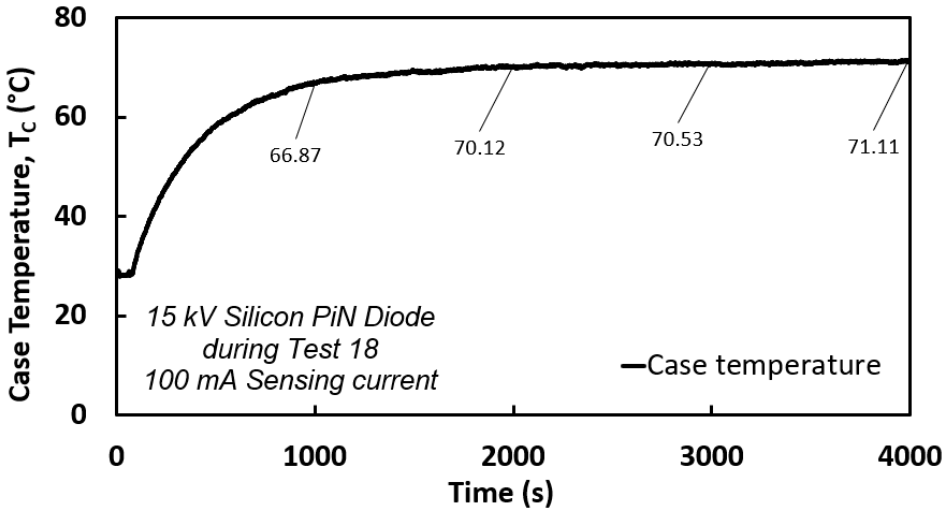

Figure 6.39: Case temperature of 15 kV Silicon PiN diode during test 18.

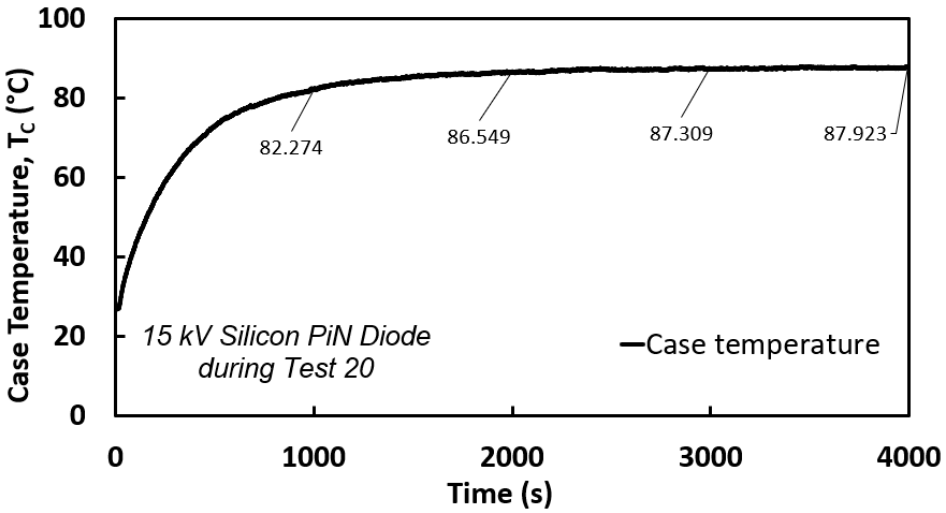

Figure 6.40: Case temperature of 15 kV Silicon PiN diode during test 20.

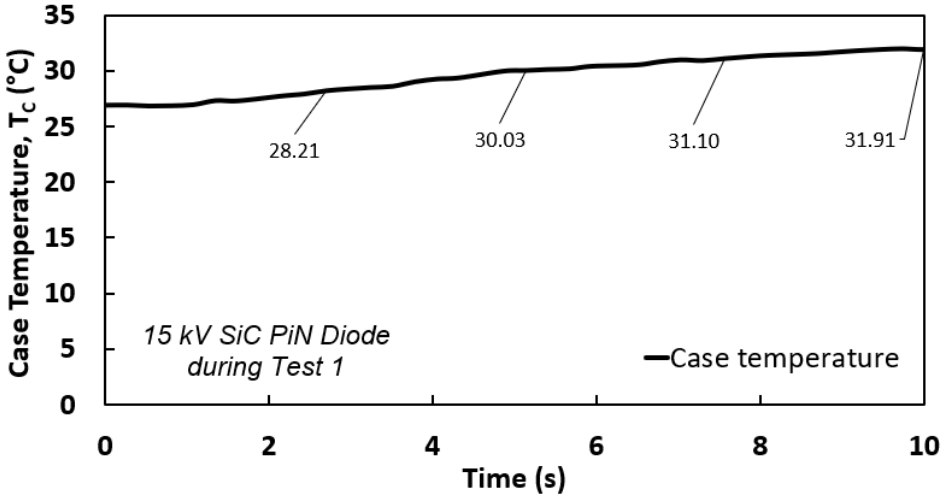

Figure 6.41: Case temperature of 15 kV SiC PiN diode during test 1.

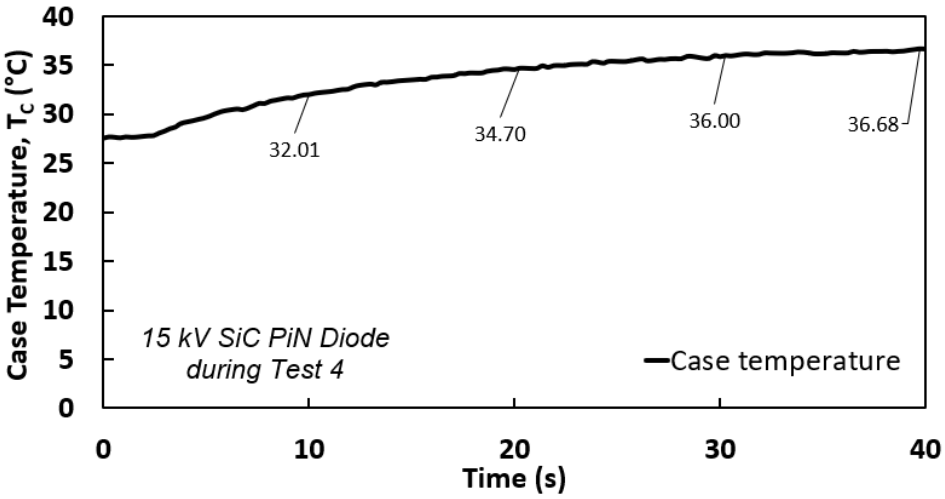

Figure 6.42: Case temperature of 15 kV SiC PiN diode during test 4.

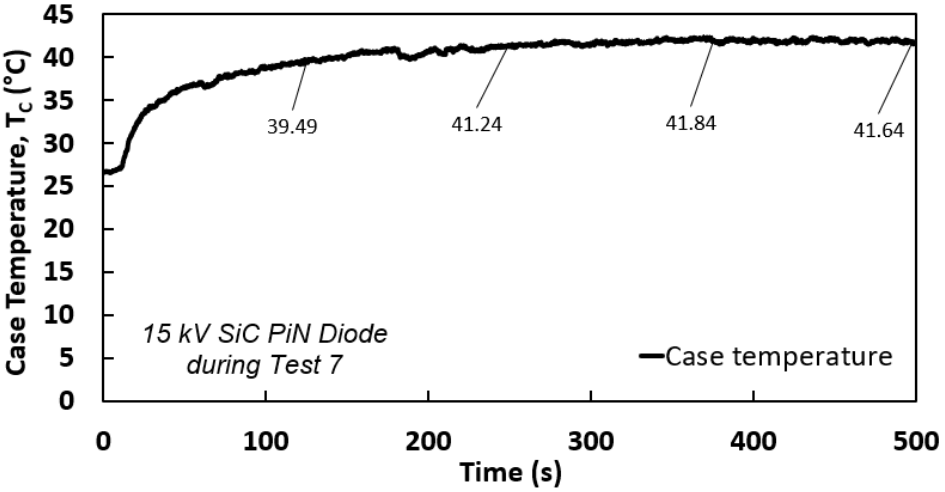

Figure 6.43: Case temperature of 15 kV SiC PiN diode during test 7.

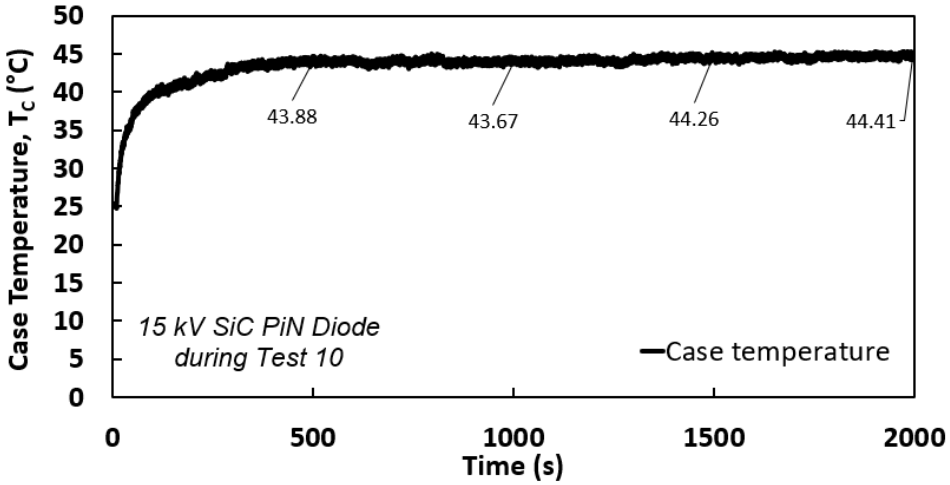

Figure 6.44: Case temperature of 15 kV SiC PiN diode during test 10.

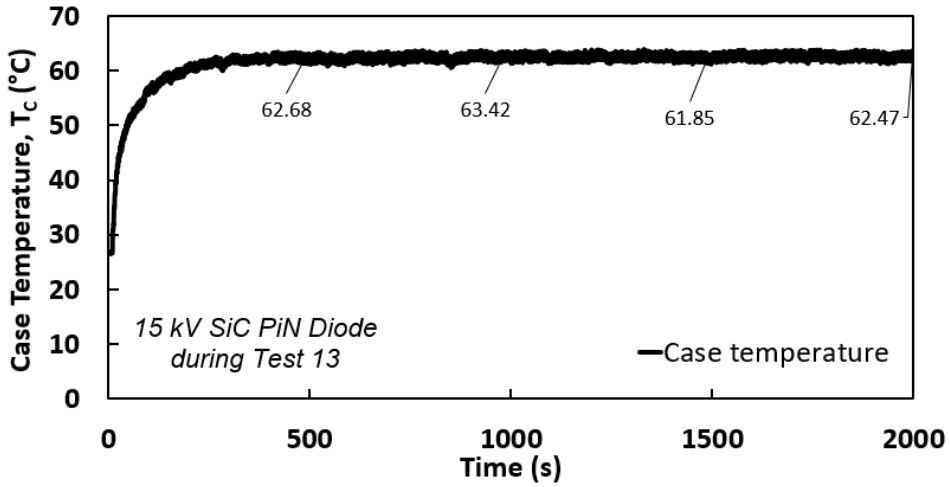

Figure 6.45: Case temperature of 15 kV SiC PiN diode during test 13.

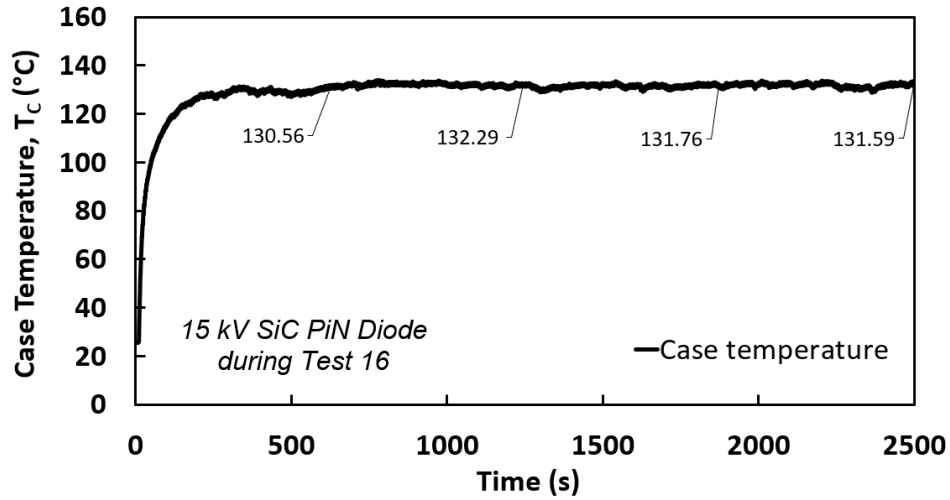

Figure 6.46: Case temperature of 15 kV SiC PiN diode during test 16.

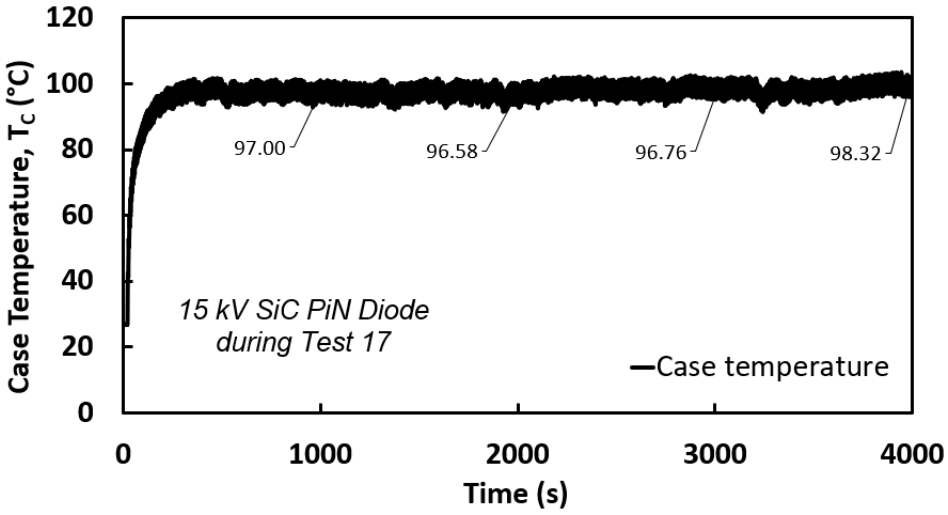

Figure 6.47: Case temperature of 15 kV SiC PiN diode during test 17.

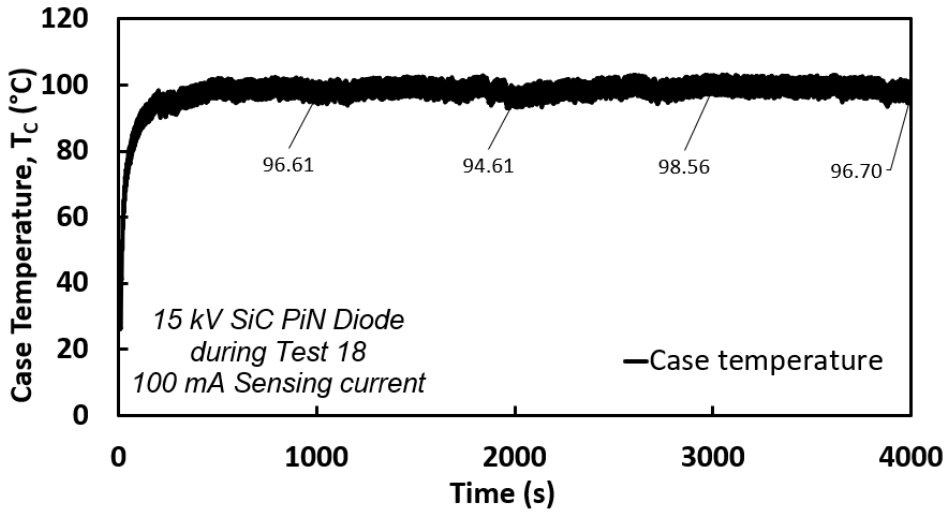

Figure 6.48: Case temperature of 15 kV SiC PiN diode during test 18.

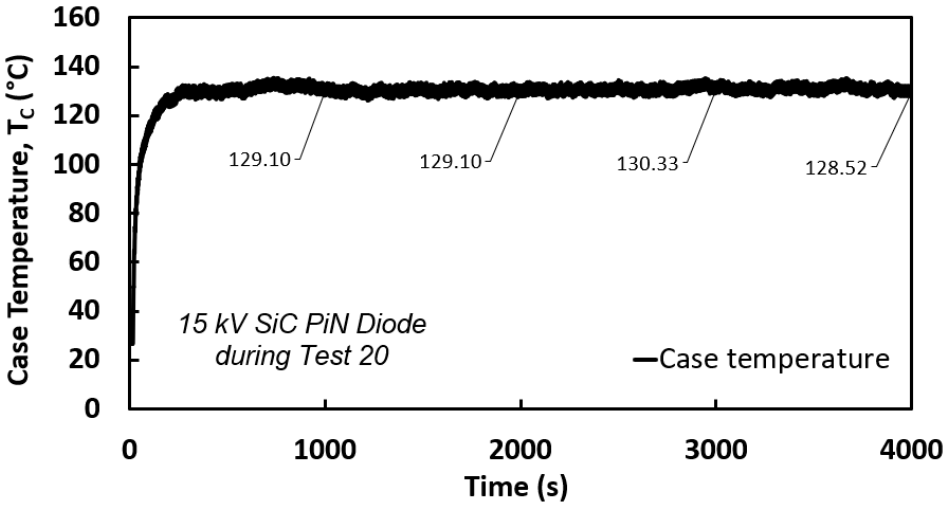

Figure 6.49: Case temperature of 15 kV SiC PiN diode during test 20.

Fig. 6.13 shows that the drift of forward voltage in SiC PiN diode during cycling tests. This mainly arises from the bipolar degradation because of the basal plane dislocations (BPDs) as mention in Section. 2.4.4.1. For the long-term operation of this 15 kV PiN diode, a positive feedback loop between forward voltage and temperature is formed leading to thermal runaway as the increased on-resistance continues to cause larger power dissipation and higher temperatures.

However, there is no degradation found during cycling tests for Silicon PiN diode which was subjected to a less junction temperature compared to that of SiC PiN diode. To generate the similar thermal stress in Silicon PiN diode, the heating current is increased to 1.5 A together with the rise of duty cycle as depicted in Table 6.4 to increase the junction temperature to about 147°C, which is the maximum junction temperature of SiC PiN diode during test 16 as shown in Fig. 6.28.

Table 6.4: Test plan for high T_j in the 15 kV Silicon PiN diode only with heating current of 1.5 A.

Test number	t_{on} (ms)	Period (ms)	Cycle number
Test 21 - t_{rise}	2400	2500	1000 (2500 ms)
Test 21 - t_{highT}	∼2150	2500	
Test 22 - t_{rise}	2400	2500	∼288 (720 ms)
Test 22 - t_{highT}	∼2150	2500	∼860 (2150 ms)

During test 21, a high duty ratio is applied to increase the junction temperature to about 147°C during t_{rise} as indicated in Fig. 6.50, followed by the lower duty ratio during t_{highT} to avoid overheating, the total test duration is same as that in test 16 for SiC PiN diode. However, the high temperature duration t_{highT} is shorter than that in test 16 for

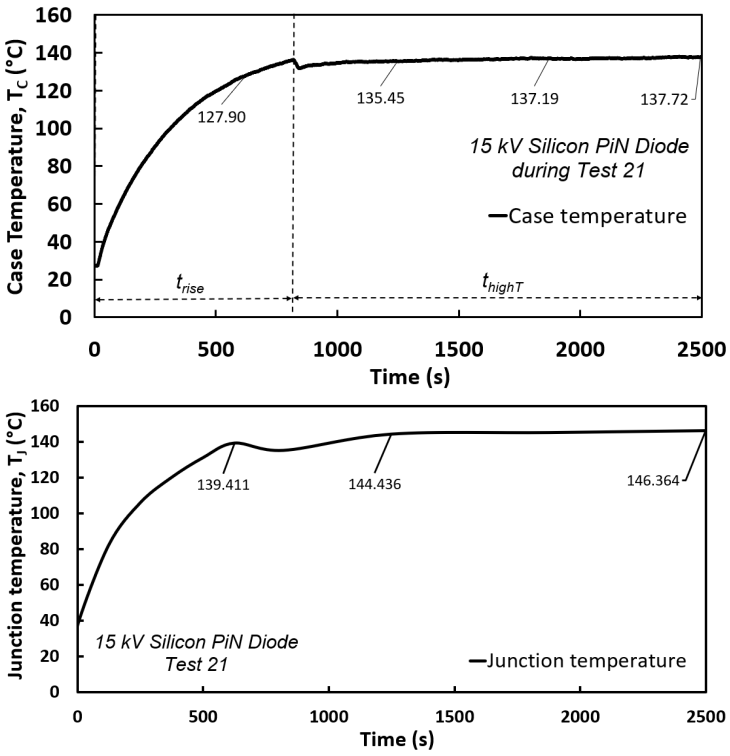

Figure 6.50: (Upper) Case temperature and (Lower) junction temperature of 15 kV Silicon PiN diode during test 21.

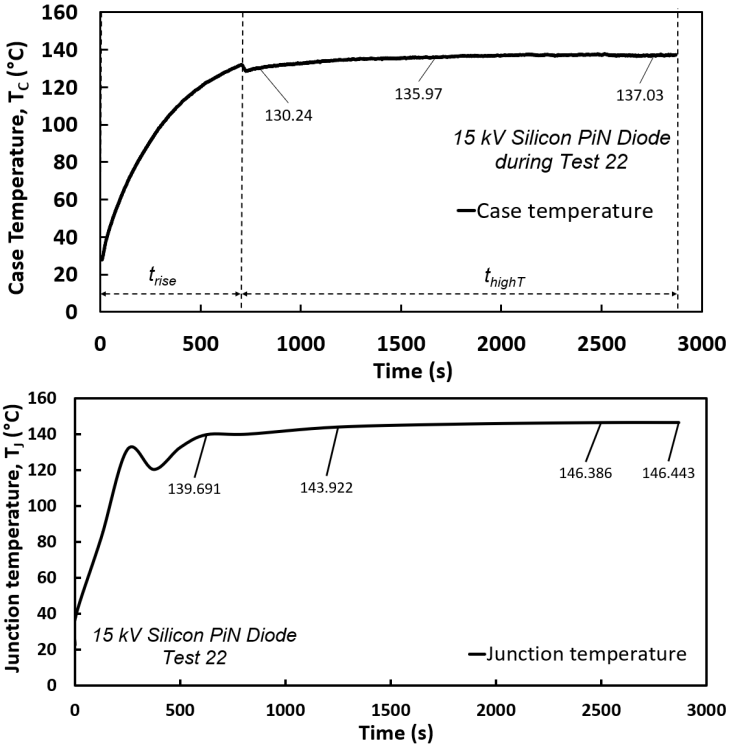

Figure 6.51: (Upper) Case temperature and (Lower) junction temperature of 15 kV Silicon PiN diode during test 22.

SiC PiN diode because of the long t_{rise} in Silicon. For the same t_{rise}, t_{highT} is increased to 2150 ms in test 22 as shown in Fig. 6.50. There is still no degradation found during cycling tests for 15 kV Silicon PiN diode as can be observed in Fig. 6.52. This is mainly because of the low density of defects in Silicon substrates.

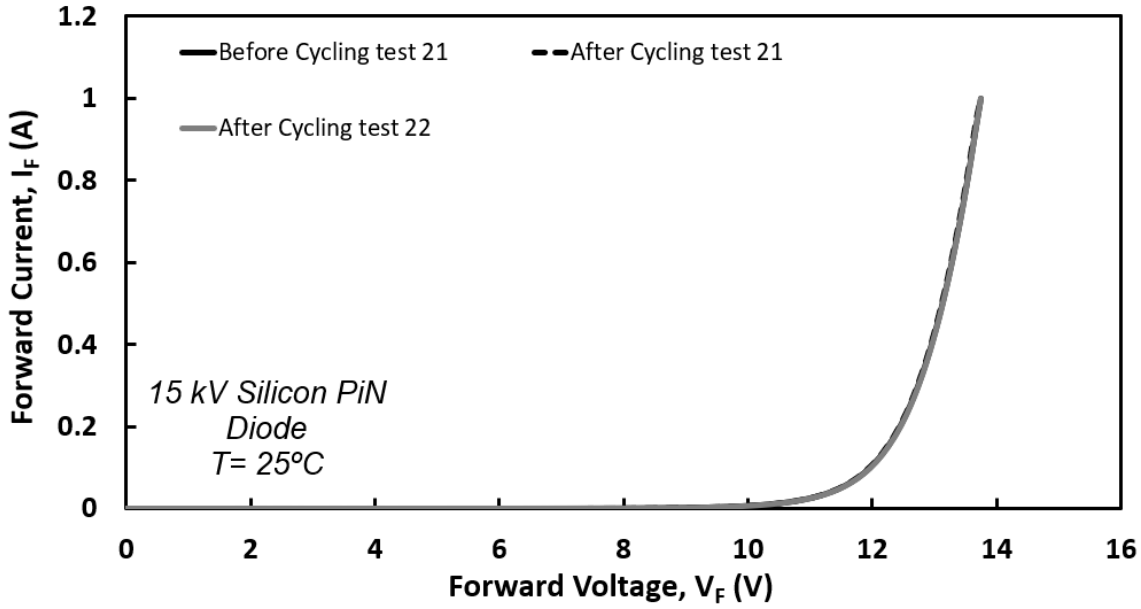

Figure 6.52: Forward I-V characteristics after test 21 and test 22 for the 15 kV Silicon PiN diode.

6.3.2 Temperature Swing via Power Cycling

When power semiconductor devices are subjected to temperature variations, different materials will response to these temperature changes in different ways because of their unique coefficient of thermal expansion (CTE) [92]. Thermal mechanical stresses and, in the extreme case, cracks and voids can be caused at these different material interfaces. For 15 kV PiN diodes in axial package, the possible weak element is the joints between leads and dies as marked in Fig. 6.1 and Fig. 6.2. To estimate the lifetime and evaluate the reliability of device packaging and the die-to-package interfaces in this section, tem-

perature swings generated by repeated power pulses is required to apply tensile stresses at these interfaces [92, 115]. This can be introduced by increasing the cooling duration as depicted in Table. 6.5.

Table 6.5: Initial test plan to evaluate the ruggedness of die-to-package interfaces for 15 kV Silicon PiN diode and 15 kV SiC PiN diode.

Test number	t_{on} (ms)	Period (ms)	Cycle number
Test 23	4,000	10,000	500
Test 24	6,000	15,000	500

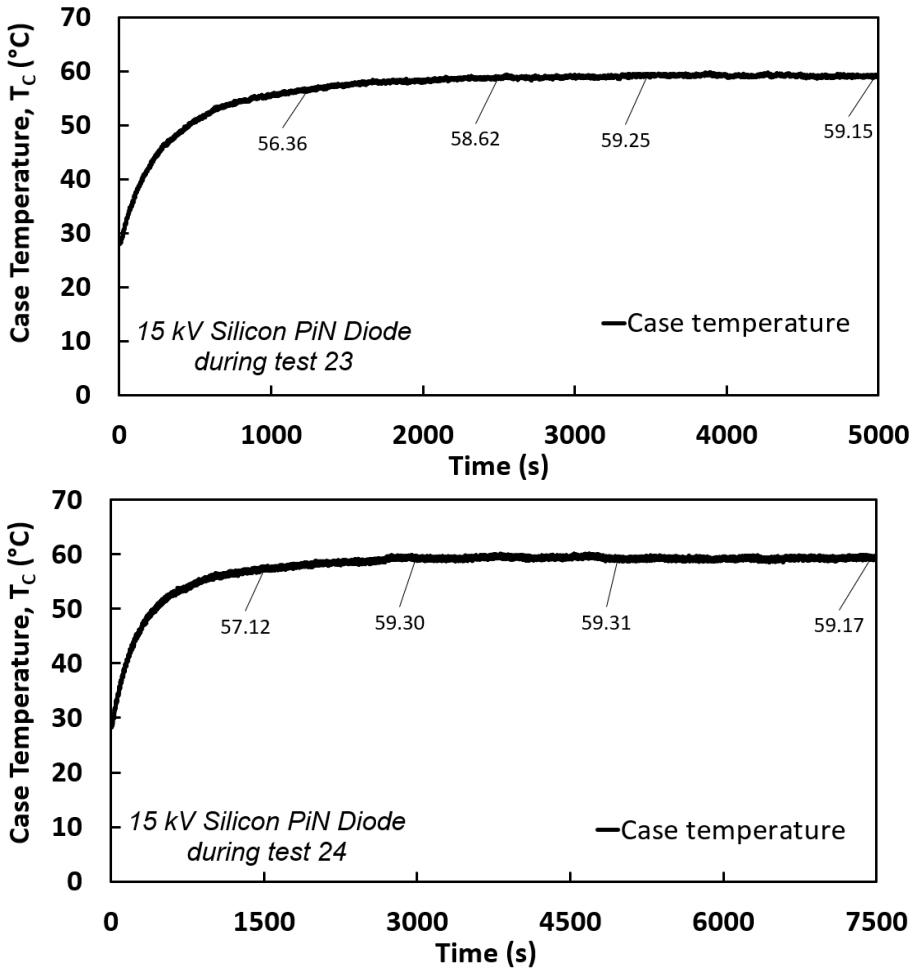

Figure 6.53: Case temperature of 15 kV Silicon PiN diode during test 23 and test 24.

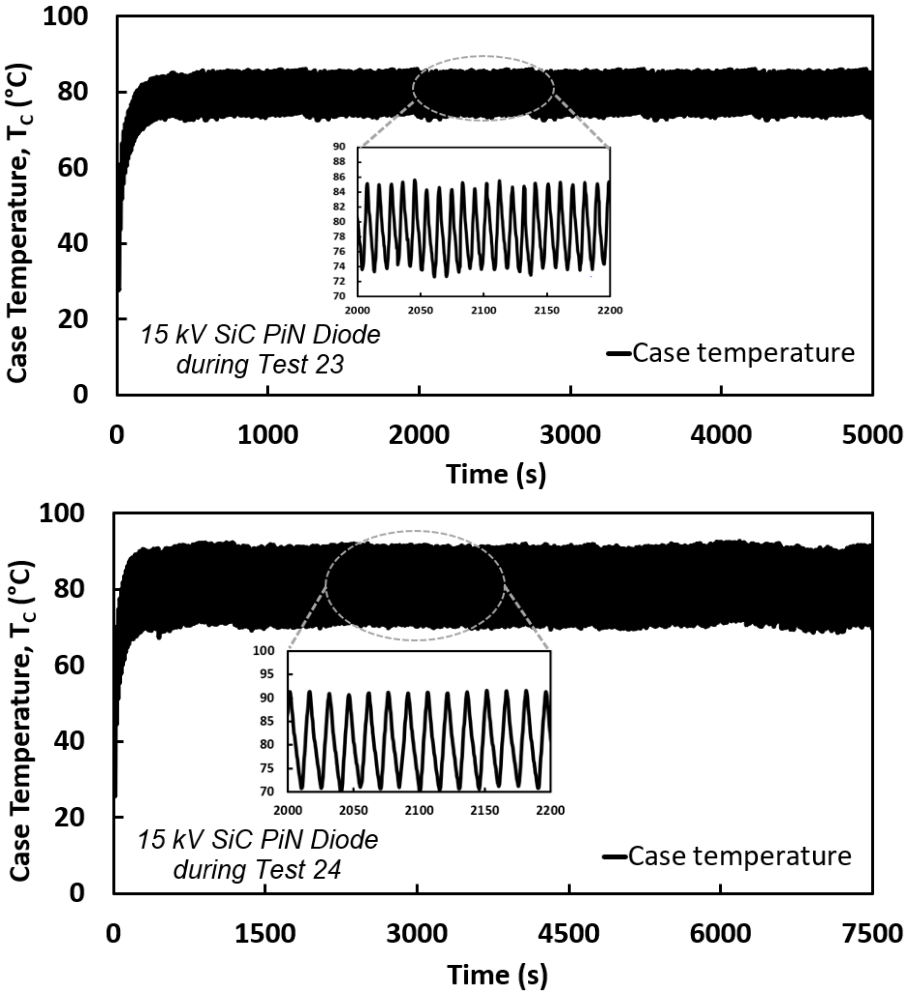

Figure 6.54: Case temperature of 15 kV SiC PiN diode during test 23 and test 24.

Fig. 6.53 and Fig. 6.54 shows the noticeable temperature swings in the 15 kV SiC PiN diode but not for the 15 kV Silicon PiN diode. To introduce more stresses material interfaces, the constant switching time strategy [115] is used to have case temperature swings of 60°C (35-95°C) within 1 cycle. Although this strategy requires the constant t_{on} and period, it cannot generate the same temperature swing for both 15 kV Silicon and SiC PiN diode because of the different capability of heat extraction. To solve this problem, the heating current is increased to 2 A for Silicon PiN diode by using ALR3206D power

supply to accelerate its heating process, while that for SiC PiN diode is reduced to 0.58 A alongside the smaller t_{on} to suppress its junction temperature. The detailed test plans are given in Table. 6.6.

Table 6.6: Same case temperature swing test as test 25 ($\Delta T_C = 60°C$ for both Silicon and SiC PiN diode).

Test	Current (A)	t_{on} (s)	Period (s)	Cycle number
Test 25 - Si	2	∼240	∼460	20
Test 25 - SiC	0.58	∼200	∼330	500

Fig. 6.56 and 6.57 show very minor degradation in 15 kV Silicon PiN diode from test 23 to test 25 while a minor drift of forward voltage in SiC PiN diode.

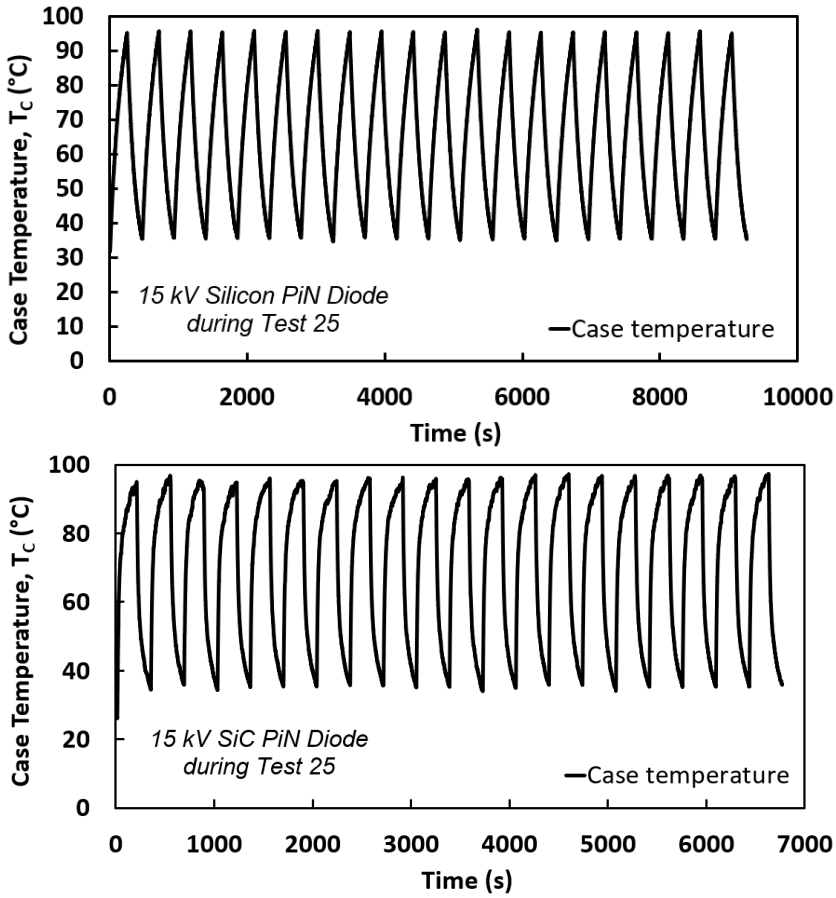

Figure 6.55: Case temperature during test 25 for 15 kV Silicon and SiC PiN diodes.

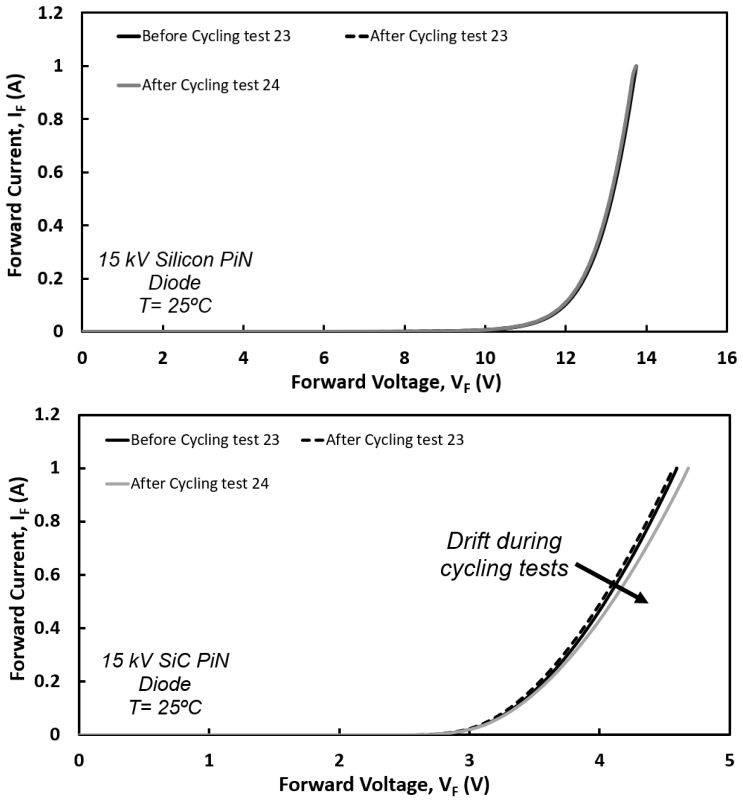

Figure 6.56: Forward I-V after test 23 and test 24 for 15 kV Silicon & SiC PiN diodes.

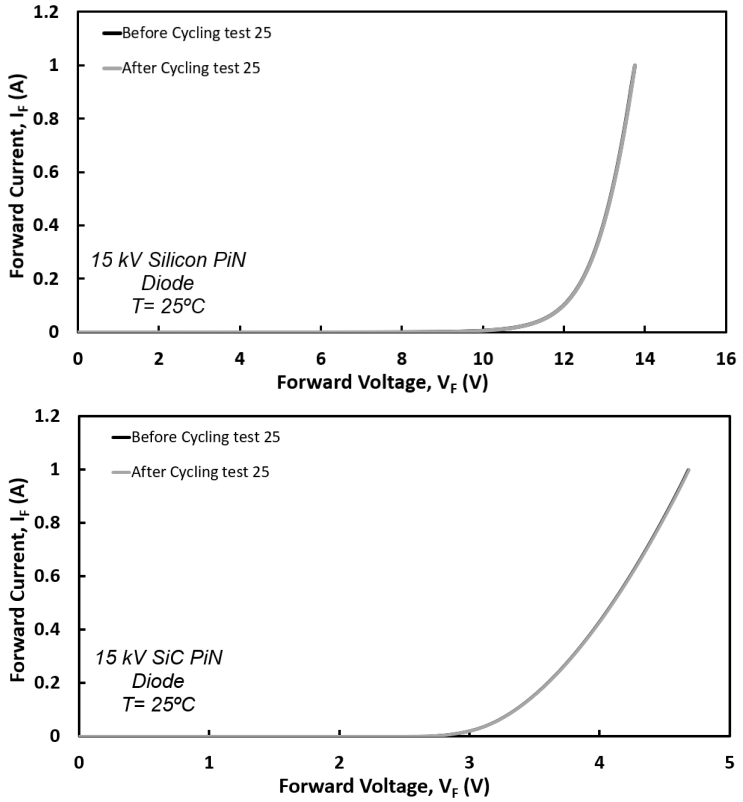

Figure 6.57: Forward I-V after test 25 for 15 kV Silicon & SiC PiN diodes.

6.4 Summary

This chapter explored the static and dynamic characteristics of the commercially available 15 kV SiC PiN diode, the long on-state reliability and the die-to-package lifetime by means of extensive power cycling tests as well as to compare with the 15 kV Silicon PiN diode rectifier. Static and dynamic characterizations show that the smaller die size in the SiC PiN diode gives rise to less reverse recovery charge and less on-resistance than the Silicon PiN diode. For the long-term power cycling tests, the junction temperature is estimated by referring to the temperature-dependent on-state voltage. The estimated junction temperature of the SiC PiN diode is found to be larger than that in the Silicon PiN diode for the same test duration because of the less forward voltage between each series-connected Silicon chip inside the Silicon diode rectifier and high thermal capacitance and thermal resistance from its packaging. Such high junction temperature and the crystal defects in the SiC PiN diode lead to the shift of the forward voltage referred to as Bipolar degradation, while no degradation has been observed from that in the less-defect Silicon PiN diode for the same equivalent junction temperature and high-temperature duration as in the case of SiC. To perform proper temperature swing tests, more power cycles as well as more server temperature swings need to be applied in the future to characterize the actual lifetime of 15 kV Silicon and SiC power PiN diode.

Chapter

7 Conclusion and Future Work

This chapter presents the key conclusions of the studies discussed in this thesis, followed by proposing future work to continue the research.

7.1 Conclusions

This thesis compared the static and dynamic switching characteristics and electrothermal reliability of the recently commercialized SiC bipolar devices including SiC BJT, SiC MPS diode and SiC PiN diode, with their closely rated Silicon counterparts primarily by means of experimental measurements, to deliver an improved understanding of the prospects and drawbacks of these SiC bipolar devices.

Chapter 3 firstly characterized the commercially available 4H-SiC BJT and Silicon BJT in terms of the switching characteristics and DC common-emitter current gain (β), together with simulation analysis verifying the experimental results. It has been shown that the voltage and current switching times in SiC BJTs are at least ten times faster than in Silicon BJTs due to the smaller widths in the base and drift regions. Both turn-on

and turn-off transitions are found to become faster at high collector currents while both switching transitions become slower at high temperatures. The turn-off delay in Silicon BJT plays a dominant role to inhibit its switching performance. The DC current gain in both BJTs improve with increasing temperature at low collector currents, but their temperature coefficient flips at higher collector currents due to the onset of the high-level injection (Webster effect) reducing the emitter injection efficiency. It is common practice to connect devices in parallel to increase the current-rating limits. The longer turn-off delay in Silicon BJTs is observed to incur a larger current mismatch between paralleled Silicon BJTs, and higher power dissipation which is also caused by a sudden current drop in a single SiC device and results in device failure. In contrast, the paralleling of two SiC BJTs with small base resistance mitigates the sudden current drop, as well as helping to avoid device failures. It is observed that the superior switching performance of SiC BJTs favor high-frequency applications.

Chapter 4 evaluates the on-state performance of Silicon and SiC power BJTs. At high temperatures, considerable base-emitter leakage current is observed in Silicon BJT whereas SiC BJTs exhibit minimal leakage current. It has been discovered that the larger base-emitter junction voltage of SiC BJTs leads to quasi-saturation mode of operation with low on-resistance, which also holds for Silicon BJTs at large base currents. Silicon BJTs need significant base current to initiate the modulation in the P region to reduce the resistance while this is significantly lower in SiC. The gain (β) is measured during the steady state operation as well the dynamics switchings, which shows negative temperature coefficient (NTC) of in SiC BJTs and positive coefficient (PTC) in Silicon BJTs which can potentially even leads to a lower current gain in SiC BJTs than Silicon BJTs at high temperatures. Analysis of measurements when devices are paralleled have shown to improve the on-state conductivity in SiC BJTs and promote both the conductivity and

current gain in Silicon BJTs.

Experimental results from Chapter 5 indicated that the switching performance of SiC MPS and SiC JBS diodes outperform the Silicon PiN diode due to the negligible reverse recovery charge and thus the much smaller switching power losses. However, the on-state voltage of Silicon diode is smaller than the SiC counterparts as a result of the high intrinsic carrier concentration in Silicon by the conductivity modulation effect that then leads to further reduction of on-resistance under high temperatures at high currents. This is while a larger on-state voltage can be observed in SiC JBS and MPS diode becoming worse at high currents under high temperatures. In terms of the UIS measurements, although the Silicon PiN diode exhibits the highest reverse voltage among these three similarly rated power devices, the avalanche ruggedness of SiC MPS & JBS diodes is superior to that of the closely rated Silicon PiN diode because of the wide-bandgap of SiC providing strong covalent bonds, enabling it to endure higher electric fields. The higher critical avalanche energy and thus the stronger avalanche ruggedness of SiC JBS diode than SiC MPS diode can be explained by that the avalanche current of SiC JBS diode is more evenly distributed in the device active region when compared with that of the SiC MPS diode. In terms of the surge current measurements, forward I-V characteristics and reverse leakage current are also captured to monitor degradation inside the diodes. All the devices can still conduct current at the on-state akin to a pure conductor even though the failure is identified in their reverse characteristics where the breakdown voltage can be reduced to a very low value. SiC MPS diode can withstand similar electrothermal stress to that in Silicon PiN diode due to the minor conductivity modulation effect and good thermal conductivity while SiC JBS diode failed at a lower stress.

Static and dynamic switching results of 15 kV PiN diodes in Chapter 6 reveal that the smaller device dimensions in the 15 kV SiC PiN diode results in less reverse recovery

charge and less on-resistance than the 15 kV Silicon PiN diode. When applying repetitive current pulses to evaluate the long-term reliability, the junction temperature is estimated by means of calibration for the temperature-dependent on-state voltage. Although the SiC PiN diode has a lower on-state power dissipation, it was discovered that its estimated junction temperature was higher than that in Silicon PiN diode for the same test duration. Such high junction temperature and the substrate defects in SiC PiN diode cause its forward voltage to drift, but no signs of aging was observed in the Silicon PiN diode for the same equivalent junction temperature and high-temperature duration as the SiC device.

In summary, this thesis showed that the newly commercialized SiC BJTs have superior on-state and switching performance to their Silicon counterparts at low temperatures but failed during the switching events at high temperatures, while its on-state performance is also observed to be worse than the Silicon BJTs at high temperatures. This reliability issue in SiC BJT can be suppressed by parallel connections. The conductivity modulation effect is not clearly evident in SiC MPS diodes while for similar device packaging technology, SiC MPS diode can compete with the Silicon PiN diode in terms of avalanche ruggedness and surge current robustness. As for the case of 15 kV PiN diodes, weaker long-term stability can be observed in the SiC device.

7.2 Future Work

To further investigate the dynamic performance of BJTs, the maximum collector current during double-pulse test needs to be increased to 15 A at room temperature to further study the impact of high-level injection (Webster effect) on the switching performance and dynamic current gain of both Silicon and SiC BJT. The difference in switching energy

between BJTs in parallel connection needs to be observed.

To continue the research on the static performance of BJTs, the measurements need to be repeated at higher collector bias to capture the maximum current gain of Silicon BJTs from the saturation mode of operation from the I-V curves. This requires using a power supply with a higher current & voltage rating. In a similar manner, the on-state resistance tests from section 4.4 can also be extended by increasing the collector current to about 15 A for both Silicon and SiC BJTs at room temperature. Additional sampling points, especially at low base currents, are needed to be added to explore the lowest base current at which the Silicon BJTs switch from the low-resistance regime to the high-resistance mode. Although the negative temperature dependence of current gain (or positive temperature of on-state resistance) in SiC BJT is expected to favor long-term operation, the long-term stability test previously performed for 15 kV SiC PiN diode in section 6.3.1 need to also be repeated for power BJTs, together with power cycling test. In doing so, the differences in the base current between Silicon and SiC BJTs must be taken into account.

In regard to the paralleled BJTs, improved stability of switching performance and the enhanced on-state performance is seen as well as negative temperature dependence of current gain in SiC BJT which is expected to favor long-term operation. This need to be verified by means of long-term stability and power cycling tests.

For UIS measurements, it is worth investigating the repetitive UIS events since the coupling of high dI/dt and the stray inductance may not cause enough avalanche energy to initiate the avalanche breakdown immediately in a single switching event, but device degradation could be seen after experiencing substantial UIS cycles [116, 117].

For surge current measurements, the impact of different device packages needs to be excluded by repeating the surge current test using diodes mentioned in Table 5.1. Based

upon what was observed in Fig. 5.27, the comparison of surge current capability among 1200 V power diodes can be further explored by adjusting the power loop resistance to allow similar surge current curves. The inductive load also needs to be included to emulate the surge current incidents that may happen in real converter topologies.

The double-pulse measurements of 15 kV SiC PiN need to be continued at multi-kilovolts (>4 kV) to further investigate the dynamic performance and evaluate possible reliability issues such as dynamic avalanche breakdown at turn-off transitions. The PCB for double pulse configuration needs to be redesigned to characterise the dynamic performance at higher voltages.

To complete the constant-switching-time power cycling tests for 15 kV PiN diodes, an automated timer circuit needs to be designed and set up to schedule the turn-on and turn-off periods of the forced air cooling fan and the power supply. Consequently, power supply switches on and the fan is turned off spontaneously during the heating phase while power supply switches off and the fan is turned on to accelerate the cooling phase.

Finally, to better understand the failure or degradation mechanisms, TCAD modelling and decapsulation of the failed devices together with CT-Scan and SEM analysis need to be performed.

Appendix

A Publications Titles

For the sake of future reference of the readers, the publications online access links along with their title pages are provided here, in order of presented chapters, respectively. The citation details of the papers are mentioned in the publication list on page ix and the full version of these publications are available on online databases accessible via the links provided here on [118–123].

I. Journal Papers

IEEE Open Journal of Power Electronics

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=9684981

Microelectronics Reliability

- https://www.sciencedirect.com/science/article/pii/S0026271422002104

Microelectronics Reliability

- Submitted - Under Review

IEEE Open Journal of the
Industrial Electronics Society

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Impact of Carriers Injection Level on Transients of Discrete and Paralleled Silicon and 4H-SiC NPN BJTs

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ABSTRACT The 4H-SiC vertical NPN BJTs are attractive power devices with potentials to be used as high power switching devices with high voltage ratings in range of 1.7 kV and high operating temperatures. In this paper, the advantages of the 4H-SiC NPN BJTs in terms of switching transients and current gain over their silicon counterparts is illustrated by means of extensive experimental measurements and modelling, including investigation of high level injection, as a common phenomenon in bipolar devices that influences the switching rates and DC current gain. The two device types have been tested at 800 V with maximum temperature of 175 °C and maximum collector current of 8 A. The turn-ON and turn-OFF transition in Silicon BJT is seen to be much slower than that of the SiC BJT while the transient duration will increase with increasing temperature and decreases with larger collector currents. The common-emitter current gain of SiC BJT is also found to be much higher than silicon counterparts, increasing with temperature in low injection levels but decreasing in higher injection levels in both devices. The rate of increase of current gain slows down toward stability as the collector current increases, known as the high-level injection. Current sharing imbalance among parallel connected devices is also investigated, which are shown to be evidently dependant on temperature and base resistance in Silicon BJT, while the current collapse in also seen in SiC BJT at high injection levels with high base resistance. The turn-OFF delay is seen to be temperature dependant in single and paralleled Silicon BJTs while almost non-existent in SiC device.

INDEX TERMS Bipolar junction transistor, DC gain, high level injection, silicon carbide, temperature.

NOMENCLATURE

D_n	Electrons Diffusion Constant (cm^2/s).
D_p	Hole Diffusion Constant (cm^2/s).
D_{nB}	Electrons Diffusion Constant in Base (cm^2/s).
J_W	Webster Current Density (A/cm^2).
J_C	Collector Current Density (A/cm^2).
J_B	Base Current Density (A/cm^2).
J_{BR}	Reverse Base Current Density (A/cm^2).
J_{SCR}	Recom. Cur. at Space-Charge Reg. (A/cm^2).
J_n	Electron Current Density (A/cm^2).
J_p	Hole Current Density (A/cm^2).
L_n	Diffusion Length (μm).
L_{s2}, L_{c2}	Inductance Between Paralleled Devices (nH).
L_{s1}, L_{Stray}	Parasitic Inductance on PCB Board (nH).
N_B	Doping Concentr. of Base Region (cm^{-3}).
N_D	Doping Concentr. of Drift Region (cm^{-3}).
n_i	Intrinsic Carrier Concentration (cm^{-3}).
n	Electron Concentration (cm^{-3}).
p	Hole Concentration (cm^{-3}).
Q_{SC}	Drift Region Minority Charge (As).

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FEM-based analysis of avalanche ruggedness of high voltage SiC Merged-PiN-Schottky and Junction-Barrier-Schottky diodes

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ABSTRACT

Through comprehensive experimental measurements and TCAD simulation, it is shown that the avalanche ruggedness of SiC MPS & JBS diodes outperforms that of closely rated Silicon PiN diodes taking advantage of the wide-bandgap properties of SiC which leads to a high ionization and activation energy given the strong covalent bonds. Although the MPS diode structure favours a high reverse blocking voltage with small leakage current and a high current conduction, the localise current crowding caused by the multiple P^+ implanted region leads to the avalanche breakdown at lower load currents than the SiC JBS diode. The results of Silvaco TCAD Finite Element modellings have a good agreement with the experimental measurements, indicating that SiC JBS diode can withstand the high junction temperature induced by avalanche in line with the calculated avalanche energy.

1. Introduction

Merged-PiN-Schottky (MPS) are bipolar SiC devices [1,2] that can be used for high frequency and medium voltage applications, for instance as output diodes in Power Factor Correction (PFC) circuit and as clamping diode in high voltage DC transmission. Clamping diodes can experience high voltages that they may lead to avalanche conduction and potentially failure, while undetected failures in grid-connected PFC circuits [3] may lead to overcurrent surges. Electrothermal ruggedness and avalanche ruggedness of SiC MPS diodes have been assessed [4–7] under Unclamped Inductive Switching (UIS) test, but with lack of comparison with other similarly rated power rectifiers. The intention of this work is to investigate the avalanche ruggedness of commercially available 4H- SiC MPS diodes through UIS tests in comparison with similarly rated Silicon PiN and SiC Junction Barrier Schottky (JBS) diode in Table 1 as in Fig. 1. Extensive experiments and Silvaco TCAD modelling are carried out to investigate the performance by UIS stressing, verifying the models by good matching.

2. UIS test measurements

The single event avalanche ruggedness of Silicon PiN, SiC JBS and SiC MPS diodes have been investigated through a wide range of UIS measurements. Table 1 includes the key parameters of the three diodes under test. All devices are fabricated in standard TO-220 packages. The UIS testing board is shown in Fig. 2 with a common, high voltage Silicon IGBT (IXBX55N300) acting as the power switch. The initial temperature of diodes before each UIS event is controlled from 25 °C to 175 °C via a temperature controller. A load inductor of 1.25 mH is charged to the peak avalanche current that is proportional to the length of the gate pulse (L_P), with pulse length of 80 μs & 160 μs, and proportional to the DC link voltage (V_{DC}) increased from 90 V to 360 V. When the IGBT switches off, the current flowing through the inductor starts to decrease while a counter Electromagnetic Force (EMF) will be induced to resist the abrupt change. The diode voltage rises to the breakdown voltage [7,8], triggering the avalanche current to flow through the diode. Unlike the power diodes which will suffer high electrothermal stress, the IGBT will stay in the safe region due to its much higher voltage/current ratings (3 kV & 55 A at 110 °C). The load current is initially set to a low value to ensure an initial avalanche energy lower than their failure limit. The pulse length and DC-link voltage are then gradually increased to apply more electrothermal stress on the device under test (DUT) until failure.

Figs. 3 and 4 show the UIS waveforms for diodes with different technologies with load current increased until device failure is achieved. Before the failure occurs, the avalanche duration increases with increase

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II. Conference Papers

PCIM 2021

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=9472239

PEMD 2022

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=9868626

EPE 2022

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=9907751

ECCE 2022

- http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=9948045

Analysis of Dynamic Transients of High Voltage Silicon and 4H-SiC NPN BJTs

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Abstract

4H-SiC vertical NPN BJTs are attractive power devices with potentials to be used as high power switching devices with high voltage ratings in range of 1.7 kV. Compared with silicon power BJTs, they particularly benefit from a large current gain to a factor of ten times higher than silicon counterparts which improves the efficiency of the gate driver. In this paper, the advantages of the 4H-SiC NPN BJTs in terms of switching transients over their silicon counterparts is illustrated by means of extensive experimental measurements and modelling. High level injection, as a common phenomenon among bipolar devices, determines the switching Speed between on-state and off-state. The two device types have been tested at 800 V with maximum temperature of 175°C and maximum collector current of 8 A. The turn-on and turn-off transition in Silicon BJT is seen to be much slower than that of the SiC BJT while the switching time will increase with increasing temperature and decreases with larger collector currents.

1 Introduction

Silicon Bipolar junction transistors (BJTs) has been used for half of the century. The low DC gain (β) in vertical Si BJTs makes it a not promising choice for applications in power electronics because complicated base drivers are needed for high base current. However, semi-insulating 4H-SiC BJTs can compete with power MOSFETs and other Substitutions of Si BJT, which have higher current density and gain [1].
In addition, BJTs have low on-state resistance due to the conductivity modulation for bipolar devices, while the gate channel used for current flow in the MOSEFT has serious ruggedness issues at high temperature application [2][3][4]. Despite thyristors are not suitable in the circuit control system, GTO thyristors made by SiC can also provide high operating temperatures, fast turn-off transients [5], etc. Furthermore, SiC BJTs have higher transconductance than SiC JFETs [2].

Thanks to the lower carrier lifetime, lower carrier mobility and much smaller width of the base & drift region, SiC BJT is predicted to have faster-switching transients [4]. At a low doped base region, especially the base and drift region of power BJT, the injected electron concentration is much higher than the base doping concentration when the high-density current injected from the collector side. This is referred to as high-level injection (HLI) in the base area. BJT undergoes large concentration of both electron and hole, which is also known as the conductivity modulation of the base region. It dramatically reduces the base resistance to allow a larger on-state current density and a lower on- state voltage drop, whereas the DC current gain and the switching characteristic are compromised [6][7]. For the dynamic transition, the variation of temperature and collector current play an important role. The dynamic switching transition can be divided into the turn-on transition and the turn-off transition which are determined by the temperature-dependent diffusion coefficient and carrier lifetime, while these two are also affected by the current level.

This paper demonstrates the performances of 4H-SiC BJTs in contrast to silicon BJTs, with analysis of Switching transients in a wide range of temperatures (25°C to 175°C) and collector current

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ANALYSIS OF ON-STATE STATIC AND DYNAMIC TRANSIENTS OF HIGH VOLTAGE 4H-SIC MERGED-PIN-SCHOTTKY DIODE

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Keywords: Silicon Carbide, Power Semiconductor Diodes, Junction Barrier Schottky, Merged-PiN-Schottky

Abstract

The 4H-SiC vertical Merged-PiN-Schottky (MPS) diodes are attractive power devices with potentials to be used in high-power DC-DC converter with high voltage ratings in the range of 1.7 kV and high operating temperatures, as an alternative to Junction Barrier Schottky (JBS) diodes. This paper reveals the dynamic switching performance and the static characteristics of the SiC MPS diode in comparison with the Silicon PiN diodes and SiC JBS diodes through a wide range of experimental measurements. It shows the superior switching performance of the SiC MPS and JBS diodes due to the absence of the reverse recovery charge. However, it is shown that this is at the cost of the large on state voltage especially at high currents and high temperatures and the increasing forward voltage during the conduction state. As the temperature dependence of forward voltage of Silicon PiN diodes is negative, they are prone to thermal runaway when connected in parallel. Such destructive consequence is also hold for single SiC MPS diode as it is shown that the lack of conductivity modulation leads to a surge of forward voltage in the on-state.

1 Introduction

SiC Schottky Barrier Diodes (SBDs), unlike the other SiC power devices like SiC MOSFETs and SiC JFETs, still suffer from a poor reverse blocking performance even though the critical electrical field of SiC is an order of magnitude larger than Silicon. This is because the leakage current of SiC SBD is much larger compared to the aforementioned SiC devices even at low reverse blocking voltage of about 300V before the onset of avalanche breakdown [1-3]. One of the reasons for this significant leakage currents are the presence of surface defects at the Schottky contact [4]. In addition, the Schottky barrier height is reduced by the image force [2] [4] when the electric field is applied at metal- semiconduction junction.

To solve this problem, 4H-SiC device manufactures moved towards the Merged PiN Schottky (MPS) diode which contains additional implanted P+ well located just below the Schottky contact, as can be seen in Fig.1. This effectively enables to become one of the few available bipolar SiC devices [5, 6] The space between P-N junctions in the MPS structure pinches off at small reverse bias voltage where a potential barrier is formed under the p+ region to protect the Schottky contact from the high electric field. The greatly reduction of electric field at Schottky contact suppress both the Schottky barrier lowering and the surge of energy states at Schottky contact, both achieves a further reduction of leakage current in SiC MPS than Silicon MPS as the absence of surface defects in the latter devices. Power Rectifiers are used for high frequency and medium voltage applications as output diodes in Power Factor Correction (PFC) circuit [7] and freewheeling diodes in the Variable Frequency Drive (VFD)control circuit [3].

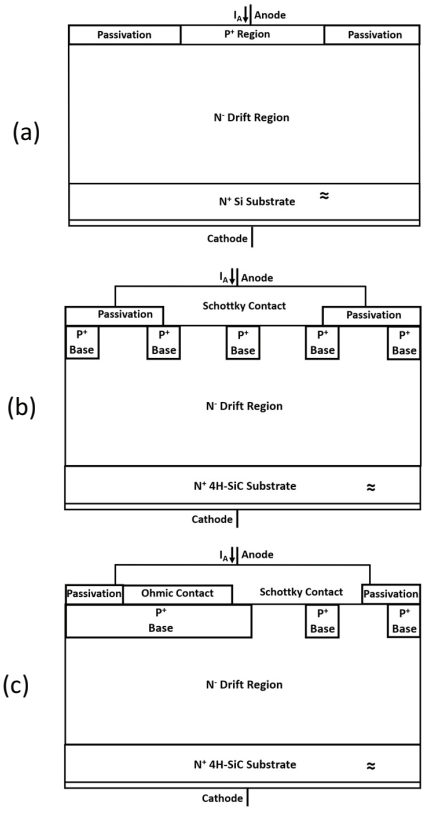

Fig. 1. Cross-sectional schematic of (a) Silicon PiN diode, (b) 4H-SiC JBS diode and (c) 4H-SiC MPS diode.

Investigation of the Static Performance and Avalanche Reliability of High Voltage 4H-SiC Merged-PiN-Schottky Diodes

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CT data were obtained at the XTM Facility, Palaeobiology Research Group, University of Bristol.

Keywords

≪Silicon Carbide≫, ≪Junction Barrier Schottky≫, ≪Merged-PiN-Schottky≫, ≪Schottky Diode≫

Abstract

A comprehensive range of static measurements and UIS tests have been conducted for Silicon PiN diodes, SiC JBS diodes and SiC MPS diodes with temperatures ranging to up to 175°C. The results shows that the forward voltage of Silicon PiN diode is lower at the on-state, even at high temperatures and at high currents. Higher forward voltage and positive temperature coefficient are observed for SiC devices during the static measurements, while they outperform the Silicon devices in terms of the electrothermal ruggedness, as validated by the UIS measurements and its subsequent calculated avalanche energy and die area as measured by means of CT-Scan imaging of the devices.

Introduction

Merged-PiN-Schottky (MPS) diode structure can be the compromise to exhibit the best attributes of both PiN and Schottky diode for power electronics applications [1]. This is because the significant reduction of electric field at Schottky contact suppress the leakage current [2] and carriers from the P^+ regions, as shown in Fig. 1, will be injected into the drift region [2, 3], allowing the occurrence of conductivity modulation to reduce the on-state voltage drop. A further reduction of leakage current is expected in SiC MPS diode as the peak electric field occurring at the SiC surface defects on Schottky contact [4] is reduced. In addition to performance metrics, reliability of power semiconductor devices and lifetime prediction has been a major topic of research in the last few decades [5, 6]. In some applications such as grid-level converters, power diodes can experience such high voltage transients that they may be led into the avalanche rating conduction, and potentially failure [7]. These diodes can also be used for high frequency and medium voltage applications as output diodes in Power Factor Correction (PFC) circuit and as clamping diode in high voltage DC transmission. Clamping diodes can experience such high voltage transients that they may be led into the avalanche rating conduction and potentially failure, while undetected grid failures in PFC circuit [8] may lead to overcurrent in output diodes. Previously, electrothermal ruggedness and avalanche robustness of SiC MPS diode have been assessed [9, 10, 11, 12] under Unclamped Inductive Switching (UIS) tests, though in absence of like-for-like comparison with

Electrothermal Ruggedness of High Voltage SiC Merged-PiN-Schottky Diodes Under Inductive Avalanche & Surge Current Stress

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***Abstract*—A comprehensive range of surge current measurements and UIS tests have been conducted for Silicon PiN diodes, SiC JBS diodes and SiC MPS diodes with temperatures ranging to up to 175°C. The results show that the SiC devices outperform the Silicon devices in terms of the avalanche ruggedness, while the SiC MPS diode can compete with the Silicon PiN diode in terms of the surge current performance. These results are validated by the experimental measurements and their subsequent calculated avalanche energy.**

***Index Terms*—Silicon Carbide (SiC), Junction Barrier Schottky, Merged PiN Schottky, Avalanche, Surge Current**

I. Introduction

Power diodes are key components in power electronics converters in automotive and renewable energy sectors [1]. Experimental [2] and simulation-based [3] of these devices have been at the center of power electronics research. Devices are either Unipolar, i.e. MOSFETs transistors and Schottky diodes, or Bipolar, i.e BJT transistors or PiN diodes [4]. Merged-PiN-Schottky (MPS) diode structure can be the compromise to exhibit the best attributes of both PiN and Schottky diode. This is because the additional implanted P+ well located just below the Schottky contact, as can be seen in Fig. 1, can reduce the electric field at Schottky contact and suppress the leakage current [5], while carriers from the P+ regions can be injected into the drift to trigger the conductivity modulation to reduce the on-state voltage drop. A further reduction of leakage current is expected in SiC MPS diode [6]. Surge Current ruggedness and Avalanche ruggedness of SiC MPS diode have been experimentally characterized in [7]–[12], but with the lack of comparison with other similar rated power rectifiers.

This paper explores the surge current ruggedness of commercially available 4H-SiC MPS diodes in contrast to Closely Rated Silicon PiN and 4H-SiC Junction Barrier Schottky (JBS) diode, the single event avalanche performance of these three devices is also evaluated by means of experimental measurements. Section II explains the mechanism of UIS tests and provides insights based on the experimental results while Section III provides the surge current performance analysis on three devices. Conclusions are provided in Section IV.

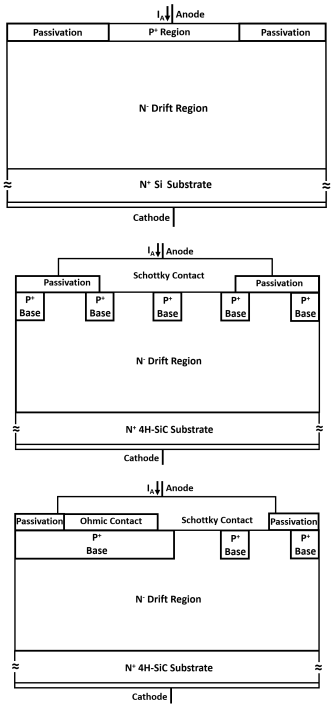


Fig. 1. The cross-sectional schematic of the Silicon PiN, SiC JBS diode and SiC MPS diode, respectively.

This work is supported by the UK EPSRC Supergen Energy Networks Hub under grant number EP/S00078X/2.

Appendix

B PCB Design Schematics

This section includes the printed circuit boards (PCB) designed by the author for different experimental measurements conducted in this thesis.

B.1 Gate Driver

For experimental measurements conducted in this thesis, a unipolar gate driver is designed as shown in Fig. B.1 to drive power semiconductor switches on PCB. This circuit requires an external voltage input of 5 volts to power up, followed by a DC-DC converter (MGJ2D052005SC) to increase this voltage to 24 volts. The output voltage of 15 volts from the adjustable voltage regulator (LM317T˙NOPB) is determined by the value of the resistors R1 and R2. For optimum performance, it is recommended that many capacitors need to be connected in parallel at the input and output of the LM317AT˙NOPB. To prevent the discharge of external capacitors through the low-impedance paths of the IC, the fast diode D1 (MUR160S˙R4) is included. The 5 V input voltage, the 15 V output voltage from LM317T˙NOPB and the control signal are sent to the gate driver integrated

circuit (1ED3124MU12HXUMA1) to drive power switch. J4 is a PCB Receptacle to house replaceable gate resistance to regulate the switching speed of power switches.

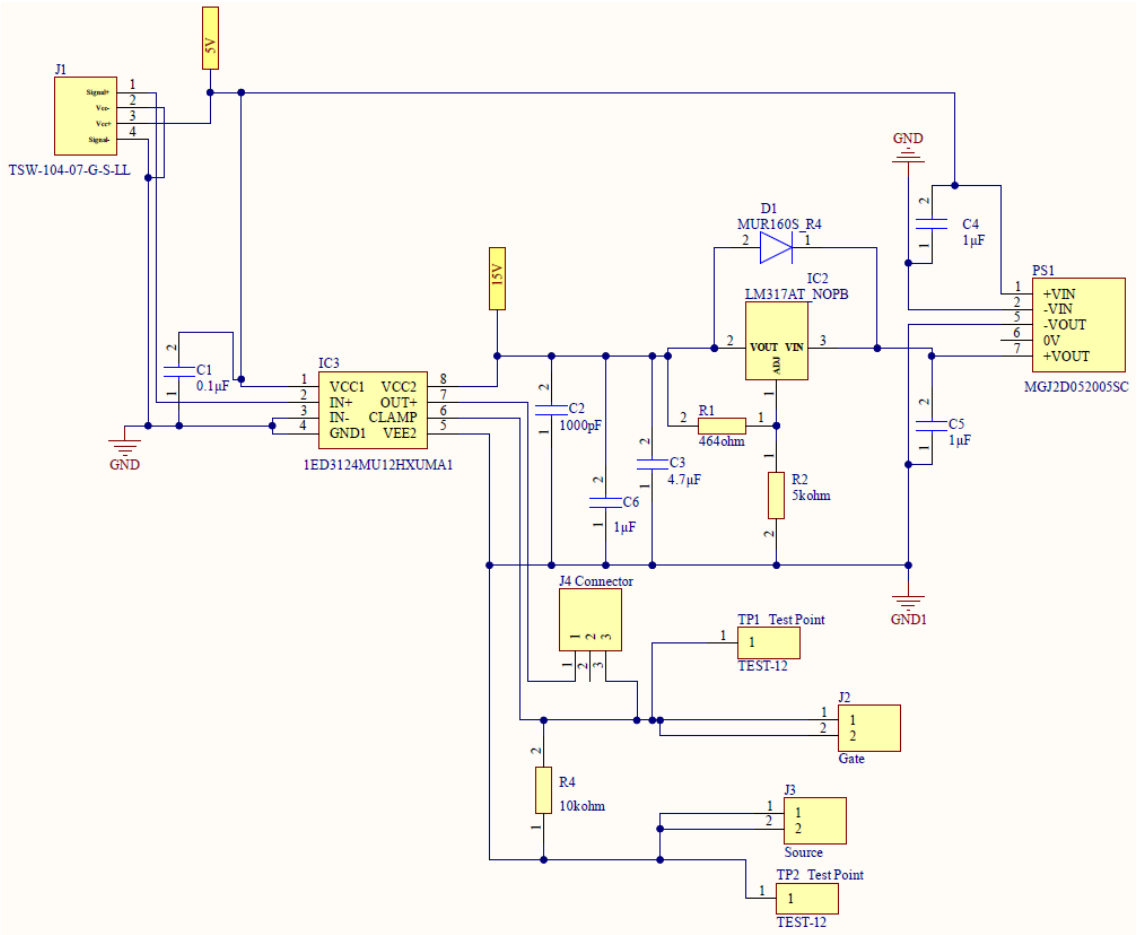


Figure B.1: Schematic diagram of the unipolar gate driver.

The PCB layout and 3D view of this unipolar gate driver are shown in Fig. B.2 and Fig. B.3, respectively. These diagrams show how components and footprints are placed on the gate driver board.

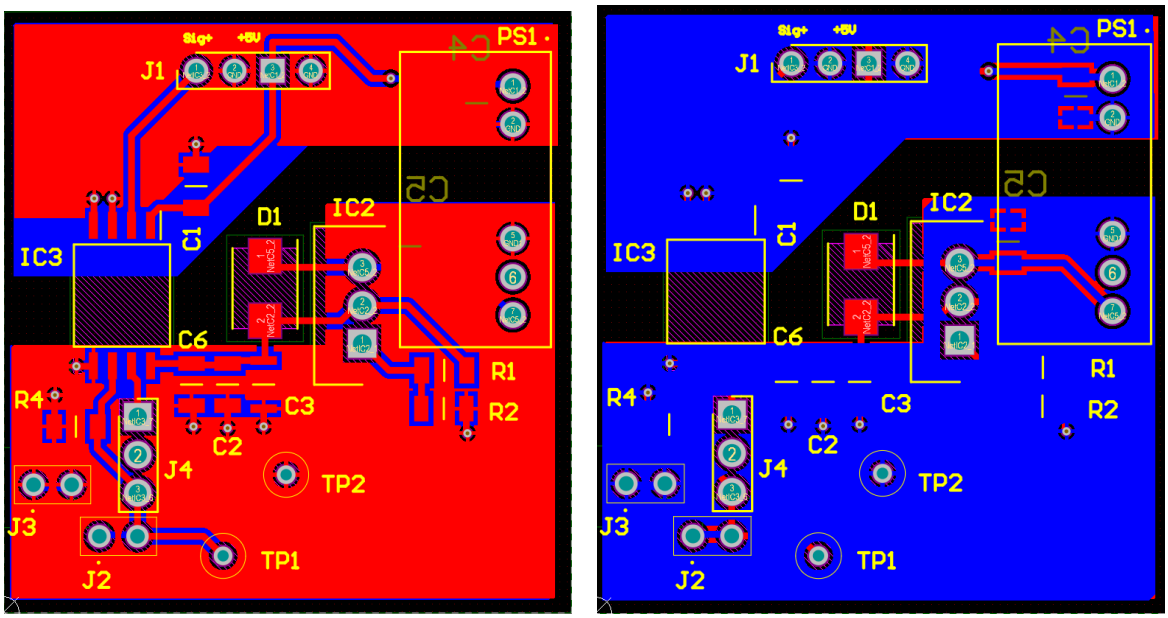


Figure B.2: (Left) The top view and (Right) the bottom view of PCB layout for the unipolar gate driver.

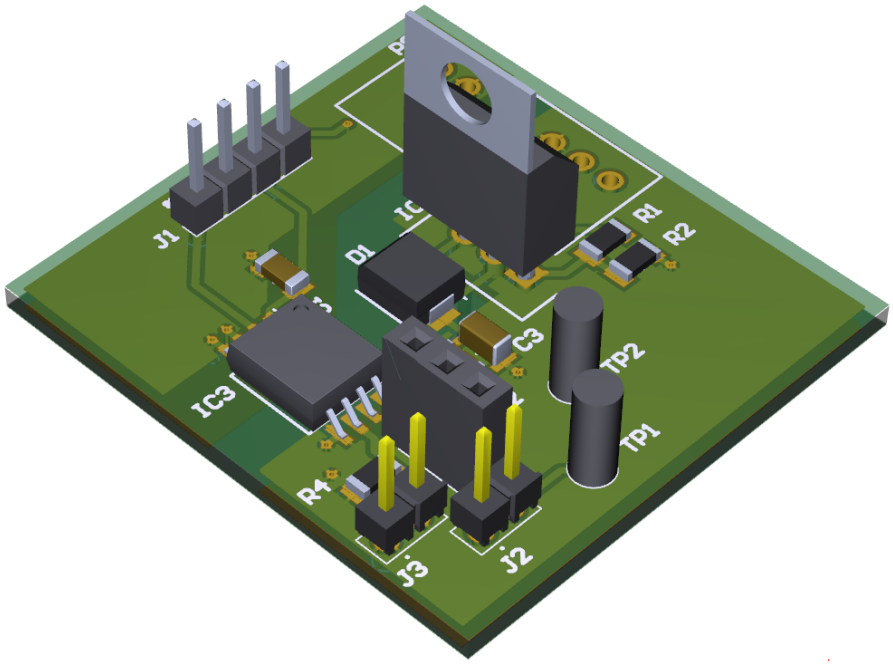


Figure B.3: The 3D view of PCB layout for the unipolar gate driver.

B.2 Double Pulse Test Board for 1200 V diodes

For double pulse measurements of 1200 V diodes, a double-pulse test board is designed as shown in Fig. B.4. The DC-link voltage is supplied from the MHV connector. The energy stored in the capacitor bank (C3-C10) is converted into load current during the first pulse. While these capacitors (R75PW44704030J) are connected in series to increase the voltage rating and connected in parallel to increase the total inductance. J1 and J2 are connected to the external load inductor. The input signal is provided via a signal connector at J3. Two blocking rectifiers (RHRP3060) are used to avoid severe overvoltage of the capacitor bank, and two 1 MΩ resistors are employed to provide an equal potential across the series-connected capacitors.

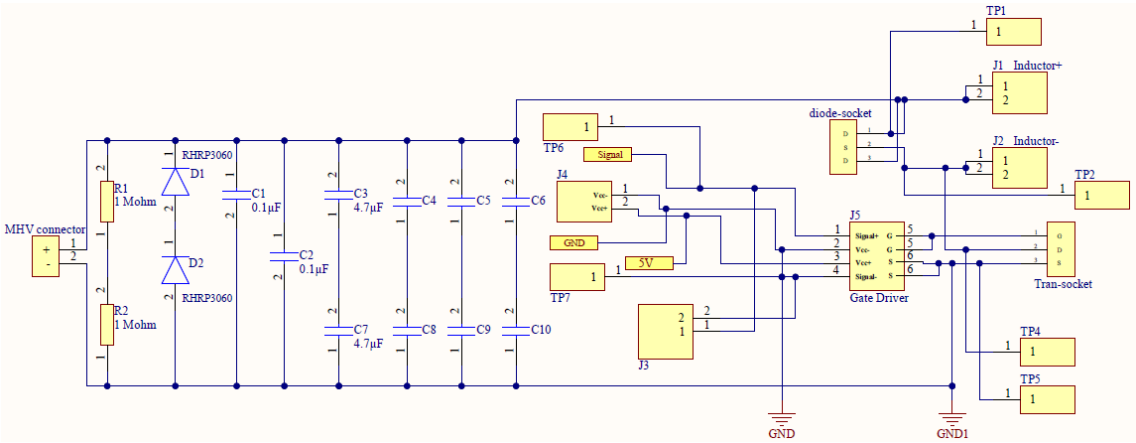


Figure B.4: Schematic diagram of the 1200 V double-pulse board.

The PCB layout and 3D view of this double pulse board are shown in Fig. B.5 and Fig. B.6, respectively. These diagrams show how components and footprints are placed on this board.

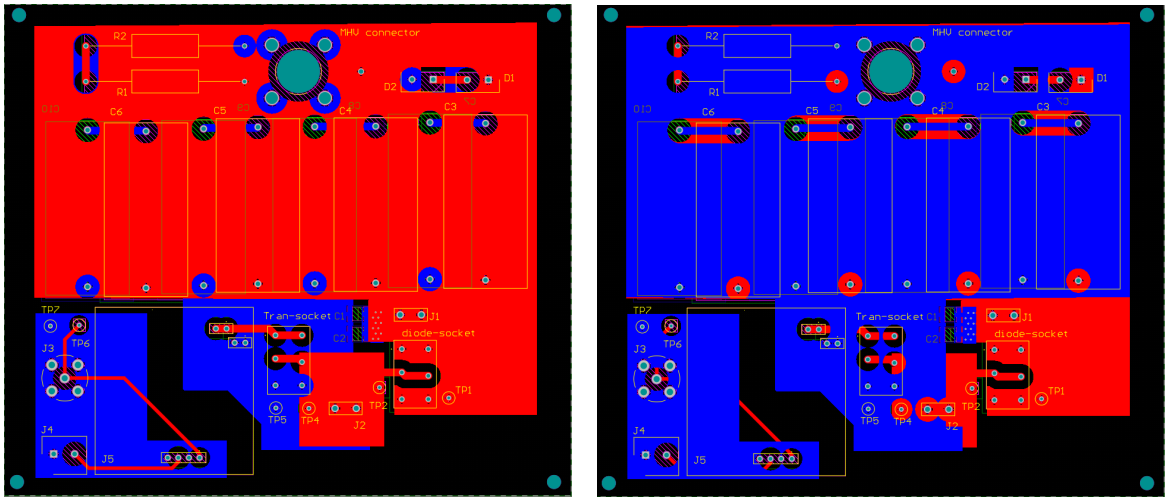


Figure B.5: (Left) The top view and (Right) the bottom view of PCB layout for the 1200 V double-pulse board.

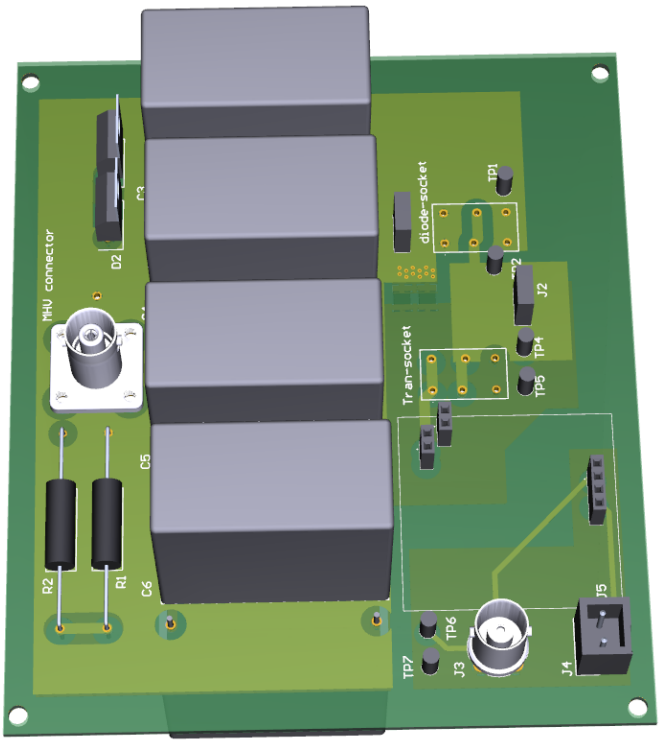


Figure B.6: The 3D view of PCB layout for the 1200 V double-pulse board.

B.3 UIS Test Board

The design of the UIS board is similar to the 1200 V double-pulse board. In this case, the diode under test is connected antiparallel to the high-voltage power switch as shown in Fig. B.7.

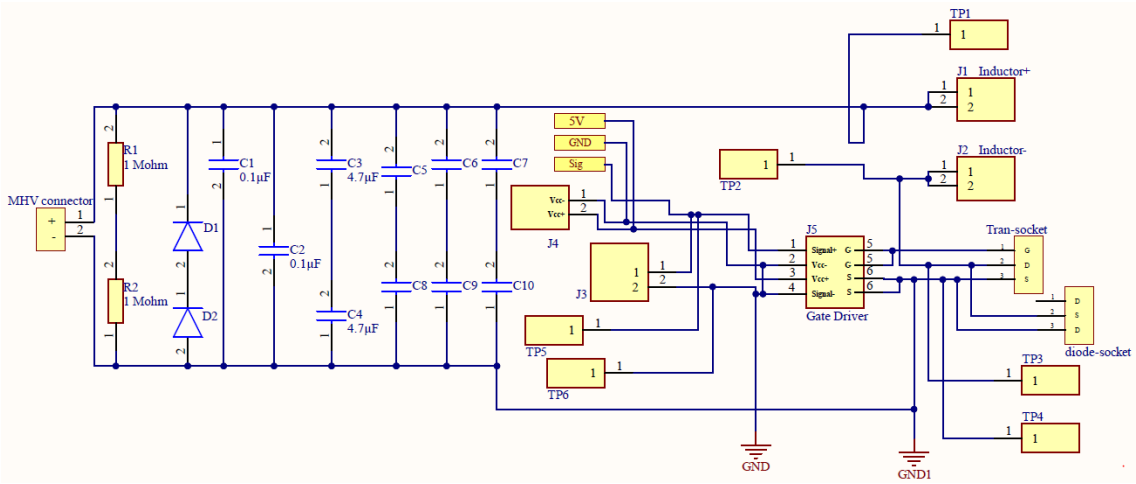


Figure B.7: Schematic diagram of the UIS test board.

The PCB layout and 3D view of this UIS board are shown in Fig. B.8 and Fig. B.9, respectively. These diagrams show how components and footprints are placed on this board.

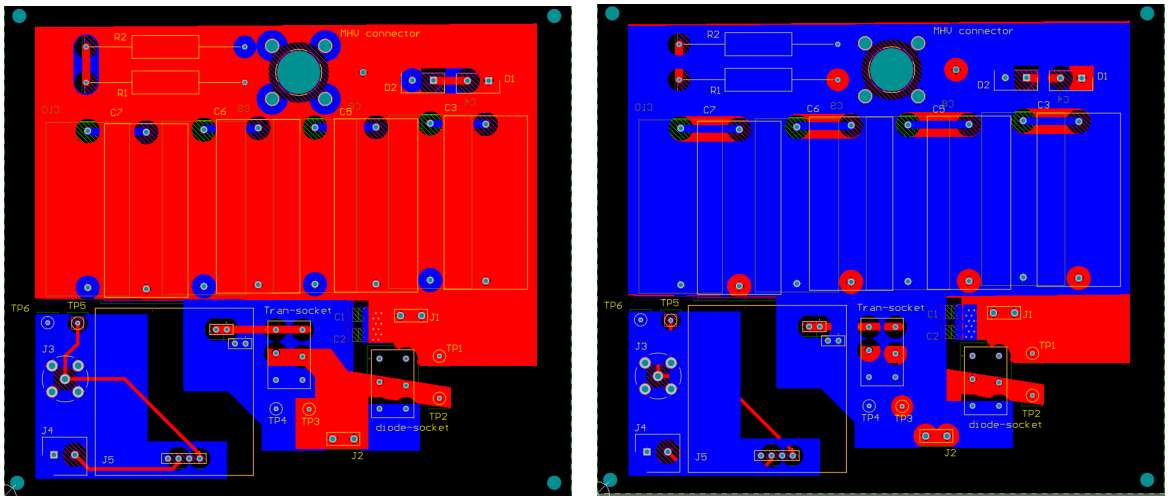


Figure B.8: (Left) The top view and (Right) the bottom view of PCB layout for the UIS test board.

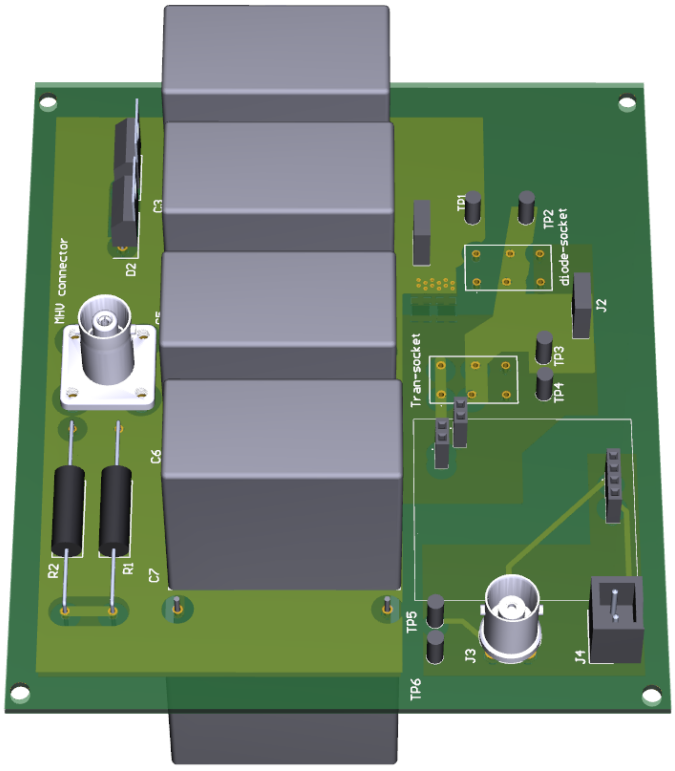


Figure B.9: The 3D view of PCB layout for the UIS test board.

B.4 Surge Current Test Board

Fig. B.10 shows the schematic diagram of the designed surge current board. The PCB layout of this board is shown in Fig. B.11. These diagrams show how components and footprints are placed on this board.

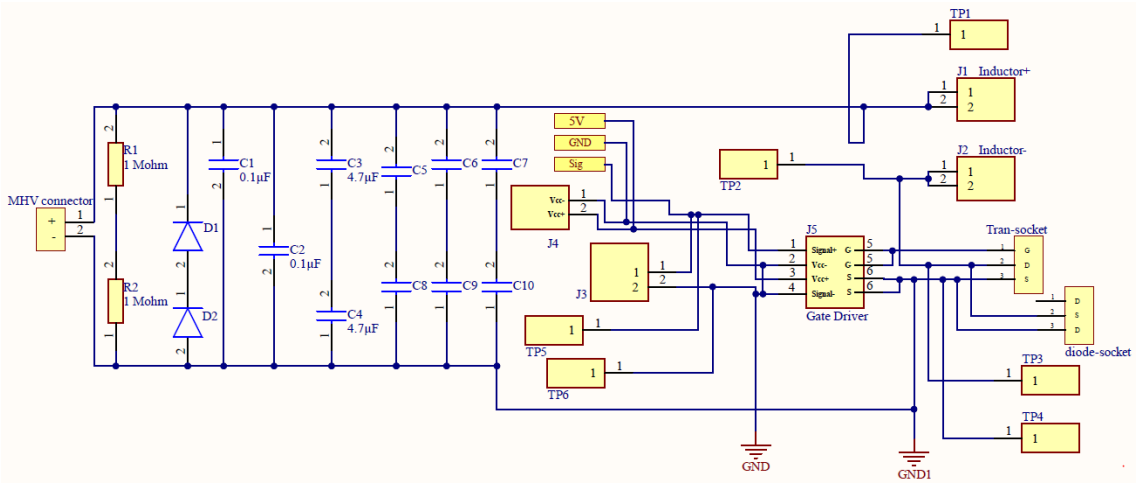


Figure B.10: Schematic diagram of the surge current test board.

Aluminium electrolytic capacitors are used to store sufficient energy to induce high surge currents. It is worth pointing out that only three electrolytic capacitors with the total capacitance of 2052 μF are used during the surge current to cause enough degradations on all power diodes. Two transistor connectors (TCC05DCSN-S1403) are used here to house parallel connected Silicon power IGBTs. The highlighted PCB cut-off is used to adopt T3RC3000-LF Rogowski Current Probe which can measure peak current up to 3000 A.

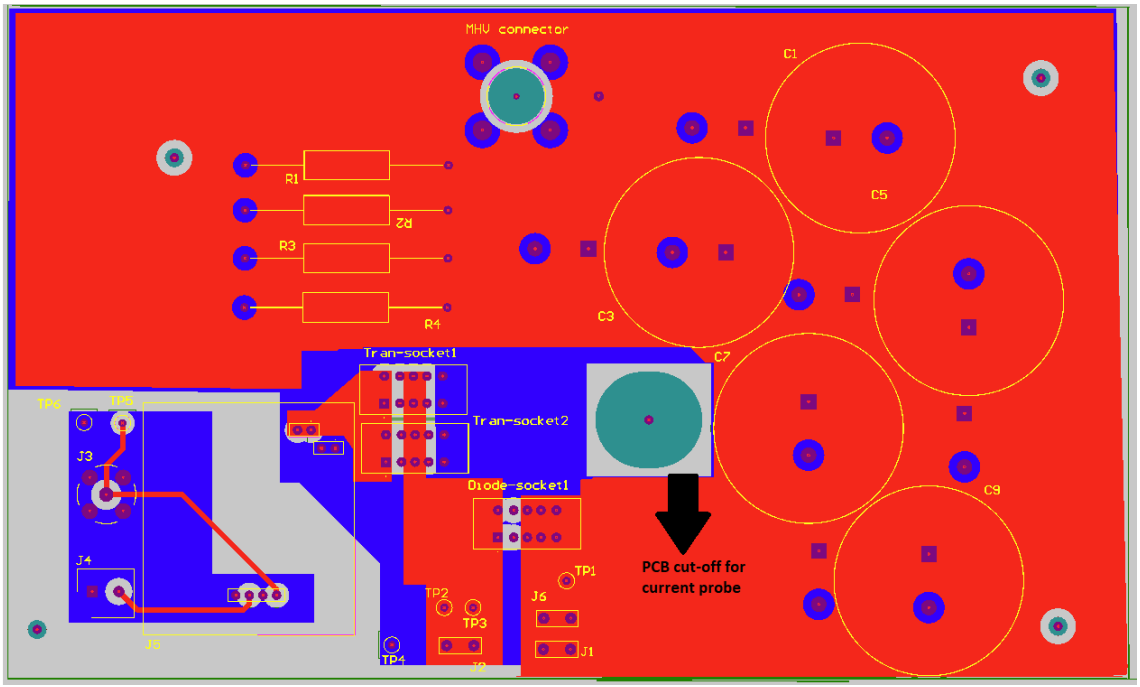


Figure B.11: PCB layout for the surge current test board.

B.5 3000 V Double Pulse Test Board

Fig. B.12 shows the designed double-pulse board to characterize power diodes with blocking voltages of up to 3000 V. Mini PCBs are also designed to displace commercial transistor connectors at J6, J7 and J8 because of the low voltage rating, mitigated by introducing air gaps in these newly designed connectors.

The PCB layout and 3D view of this double-pulse board are shown in Fig. B.13 and Fig. B.14, respectively. These diagrams show how components and footprints are placed on this board. More PCB cut-offs are included to introduce air gaps to improve the isolation voltage between areas with different voltage levels.

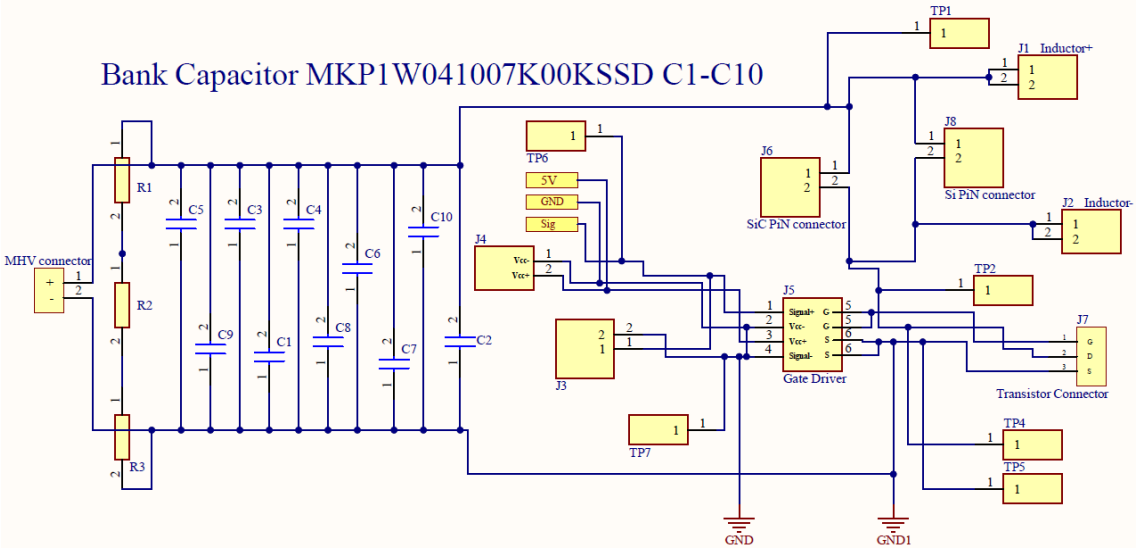


Figure B.12: Schematic diagram of the 3000 V double-pulse board.

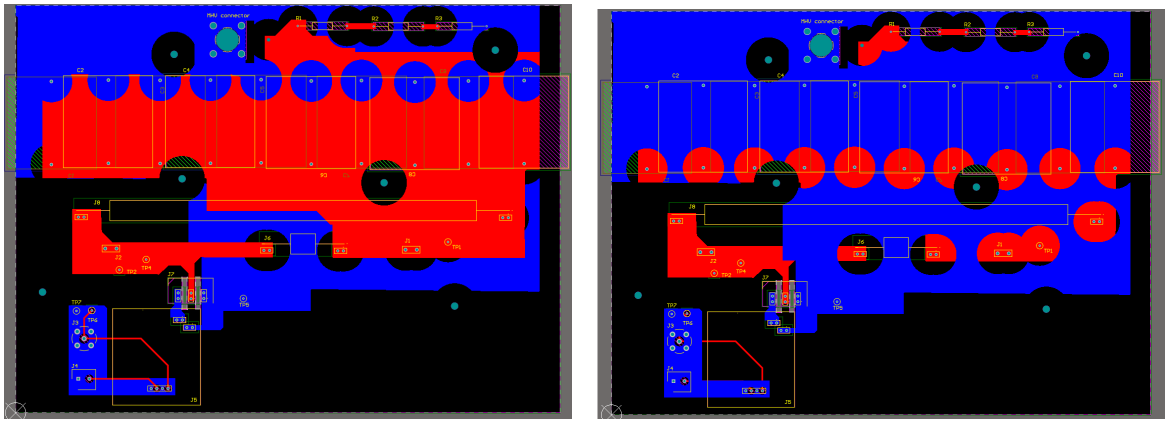


Figure B.13: (Left) The top view and (Right) the bottom view of PCB layout for the 3000 V double-pulse board.

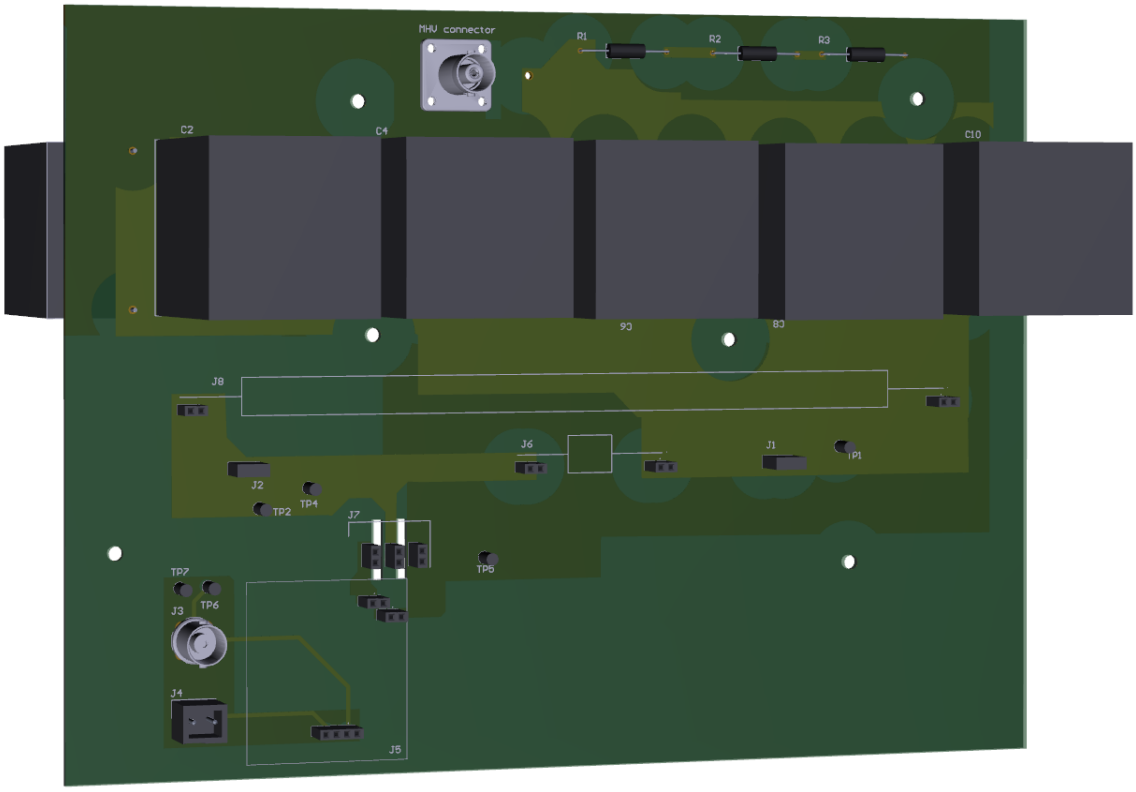


Figure B.14: The 3D view of PCB layout for the 3000 V double-pulse board.

Appendix

C Table of Equipments

This section includes a list of test equipment used in experimental measurements in this thesis to get accurate and reliable results. These features include output waveform accuracy, measurement resolution, bandwidth of test equipment, and other aspects.

Equipment	Specifications	Appearance
High Voltage Power Supply HTP-HPx40 757	Output Voltage: 0-4 kV Output Current: 0-750 mA Maximum Power: 3 kW Switching Frequency: 70-90 kHz Efficiency: Up to 93%	

Table C.1: Specifications of test equipments used for the experimental measurements.

ELC ALR3220 Bench Power Supply	Output Voltage: 0-32 V Output Current: 0-20 A Power Rating: 770 W Current Accuracy: 0.03% Efficiency: Up to 84%	
Agilent 33220A Function Arbitrary Waveform Generator	Frequency Resolution: 1 μHz Sample rate: 50 MSa/s Amplitude resolution: 14 bits Accuracy: $\pm$10 ppm Frequency Range: 1 μHz to 20 MHz	
Keysight B2902A Precision Source/Measure Unit (SMU)	Max Voltage Output: 210 V Max DC Current Output: 10.5 A Max Pulsed Current Output: 3.03 A Max Power Output: 31.8 W Min Voltage Resolution: 1 μV Min Current Resolution: 1 pA	

Table C.1: Specifications of test equipments used for the experimental measurements.

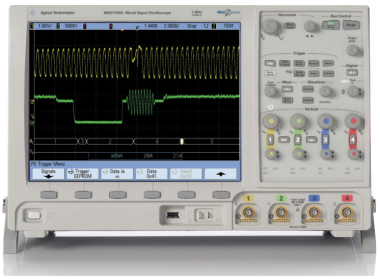
Keysight MSO7104A Mixed Signal Oscilloscope	Bandwidth: 1 GHz Sample Rate: 4 GSa/s Vertical Resolution: 8 bits DC Vertical Gain Accuracy: ±2%	
GW INSTEK Voltage Probe GDP-100	Voltage Rating: ±7000 V Bandwidth: 100 MHz Accuracy: ±2% Rise time: 3.5 ns	
PEM CWT Ultra-mini Rogowski Current Coil CW- TUM/1/B	Current Rating: 0-300 A Sensitivity: 20 mV/A Peak di/dt: 20 kA/μs Accuracy: ±2%	

Table C.1: Specifications of test equipments used for the experimental measurements.

Teledyne Rogowski Current Probe T3RC3000-LF	Current Rating: 0-3000 A Bandwidth: 0.11 Hz to 6.5 MHz Sensitivity: 2 mV/A Peak di/dt: 11 kA/μs Max Noise: 2.5 mV rms	
Tektronix Current Amplifier TCPA300 & Probe TCP312	Max DC (continuous) Current: 30 A High Current Sensitivity: 10 A/V Low Current Sensitivity Range: 1 A/V Rise Time: $\leq$ 3.5 ns Bandwidth: DC - 100 MHz Lowest Measurable Current: 1 mA	
Inkbird PID Temperature Controller ITC-100	Controlling Range: -50 to 1300°C Power Consumption: Approx 0.5 VA (100-240 VAC) Accuracy: 0.1°C Period of Sampling: 0.5 S	

Table C.1: Specifications of test equipments used for the experimental measurements.

FlIR Infrared Camera FLIR E5-XT	IR Resolution: 160×120 (19,200 pixels) Image frequency: 9 Hz Thermal Sensitivity: <0.10°C Temperature Range: −20°C to 400°C Accuracy: ±2% of the reading	
TAS LTCL600 Climatic Test Chamber	Temperature: −70°C to +180°C Rate of heating and cooling: 3°C/min Stability: ±0.3 to 1.0 K	

Appendix

D Devices Datasheets

For the sake of future reference of the readers, the main characteristics of the devices used in the measurements of this thesis are presented here by means of providing the main page of the datasheets. The full version of these datasheets are available online.

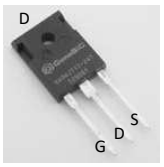
Normally – OFF Silicon Carbide Junction Transistor

V_{DS}	=	1700 V
$R_{DS(ON)}$	=	180 mΩ
$I_{D\ (Tc = 25°C)}$	=	15 A
$I_{D\ (Tc > 125°C)}$	=	5 A
$h_{FE\ (Tc = 25°C)}$	=	100

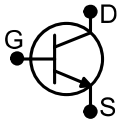
Features

- 175 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package



TO-247



Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1700	V	
Continuous Drain Current	I_D	T_C = 25°C	15	A	Fig. 17
Continuous Drain Current	I_D	T_C = 160°C	4	A	Fig. 17
Continuous Gate Current	I_G		0.25	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, Clamped Inductive Load	$I_{D,max}$ = 4 @ $V_{DS} \leq V_{DSmax}$	A	Fig. 19
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 0.2 A, V_{DS} = 1200 V, Non Repetitive	>20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_C = 25 °C / 160 °C, t_p > 100 ms	106 / 10	W	Fig. 16
Storage Temperature	T_{stg}		-55 to 175	°C	

FJL6920

High Voltage Color Display Horizontal Deflection Output

- High Collector-Base Breakdown Voltage : BV_{CBO} = 1700V
- Low Saturation Voltage : V_{CE}(sat) = 3V (Max.)
- For Color Monitor

TO-264

1.Base 2.Collector 3.Emitter

NPN Triple Diffused Planar Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Rating	Units
V_{CBO}	Collector-Base Voltage	1700	V
V_{CEO}	Collector-Emitter Voltage	800	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current (DC)	20	A
I_{CP}*	Collector Current (Pulse)	30	A
P_C	Collector Dissipation	200	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

* Pulse Test: PW=300μs, duty Cycle=2% Pulsed

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{CES}	Collector Cut-off Current	V_{CB}=1400V, R_{BE}=0			1	mA
I_{CBO}	Collector Cut-off Current	V_{CB}=800V, I_E=0			10	μA
I_{EBO}	Emitter Cut-off Current	V_{EB}=4V, I_C=0			1	mA
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=500μA, I_E=0	1700			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=5mA, I_B=0	800			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=500μA, I_C=0	6			V
h_{FE1} h_{FE2}	DC Current Gain	V_{CE}=5V, I_C=1A V_{CE}=5V, I_C=11A	8 5.5		 8.5	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C=11A, I_B=2.75A			3	V
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C=11A, I_B=2.75A			1.5	V
t_{STG}*	Storage Time	V_{CC}=200V, I_C=10A, R_L=20Ω I_{B1}=2.0A, I_{B2}= - 4.0A			3	μs
t_F*	Fall Time			0.15	0.2	μs

* Pulse Test: PW=20μs, duty Cycle=1% Pulsed

Thermal Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Typ	Max	Units
$R_{\theta jC}$	Thermal Resistance, Junction to Case		0.625	°C/W

Rev. A, May 2001

CREE

C4D10120H

Silicon Carbide Schottky Diode

Z-Rec® Rectifier

V_{RRM}	=	1200 V
I_F (T_C=135°C)	=	15 A
Q_c	=	52 nC

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F
- Increased Creepage/Clearance Distance

Package

TO-247-2

Halogen-Free

RoHS

Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

Part Number	Package	Marking
C4D10120H	TO-247-2	C4D10120

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Reverse Voltage	1200	V		
I_F	Continuous Forward Current	31.5 15 10	A	T_C=25°C T_C=135°C T_C=155°C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	46 30	A	T_C=25°C, t_p=10 ms, Half Sine Pulse T_C=110°C, t_p=10 ms, Half Sine Pulse	
I_{FSM}	Non-Repetitive Forward Surge Current	67 59	A	T_C=25°C, t_p=10 ms, Half Sine Pulse T_C=110°C, t_p=10 ms, Half Sine Pulse	Fig. 8
$I_{F,Max}$	Non-Repetitive Peak Forward Current	750 620	A	T_C=25°C, t_p=10 µs, Pulse T_C=110°C, t_p=10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation	153 66	W	T_C=25°C T_C=110°C	Fig. 4
dV/dt	Diode dV/dt ruggedness	200	V/ns	V_R=0-960V	
$\int i^2dt$	i^2t value	22.5 17.5	A^2s	T_C=25°C, t_p=10 ms T_C=110°C, t_p=10 ms	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C		
	TO-247 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

GC20MPS12-220
1200V 20A SiC Schottky MPS™ Diode

Silicon Carbide Schottky Diode

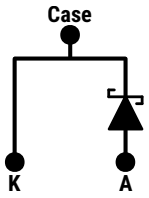
V_{RRM}	=	1200 V
$I_{F\,(T_C\,=\,154°C)}$	=	20 A
Q_C	=	107 nC

Features

- Low V_F for High Temperature Operation
- Enhanced Surge and Avalanche Robustness
- Superior Figure of Merit Q_C/I_F
- Low Thermal Resistance
- Low Reverse Leakage Current
- Temperature Independent Fast Switching
- Positive Temperature Coefficient of V_F
- High dV/dt Ruggedness

Package

TO-220-2



RoHS

REACH

Advantages

- Improved System Efficiency
- High System Reliability
- Optimal Price Performance
- Reduced Cooling Requirements
- Increased System Power Density
- Zero Reverse Recovery Current
- Easy to Parallel without Thermal Runaway
- Enables Extremely Fast Switching

Applications

- Power Factor Correction (PFC)
- Electric Vehicles and Battery Chargers
- Solar Inverters
- High Frequency Converters
- Switched Mode Power Supply (SMPS)
- Motor Drives
- Anti-Parallel / Free-Wheeling Diode
- Induction Heating & Welding

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Repetitive Peak Reverse Voltage	V_{RRM}		1200	V	
Continuous Forward Current	I_F	T_C = 100°C, D = 1 T_C = 135°C, D = 1 T_C = 154°C, D = 1	43 30 20	A	Fig. 4
Non-Repetitive Peak Forward Surge Current, Half Sine Wave	$I_{F,SM}$	T_C = 25°C, t_P = 10 ms T_C = 150°C, t_P = 10 ms	200 160	A	
Repetitive Peak Forward Surge Current, Half Sine Wave	$I_{F,RM}$	T_C = 25°C, t_P = 10 ms T_C = 150°C, t_P = 10 ms	120 84	A	
Non-Repetitive Peak Forward Surge Current	$I_{F,MAX}$	T_C = 25°C, t_P = 10 µs	1000	A	
i^2t Value	$\int i^2dt$	T_C = 25°C, t_P = 10 ms	200	A^2s	
Non-Repetitive Avalanche Energy	E_{AS}	L = 1.8 mH, I_{AS} = 20 A	360	mJ	
Diode Ruggedness	dV/dt	V_R = 0 ~ 960 V	200	V/ns	
Power Dissipation	P_{TOT}	T_C = 25°C	279	W	Fig. 3
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

C4D02120A

Silicon Carbide Schottky Diode

Z-Rec® Rectifier

V_{RRM}	=	1200 V
I_F (T_C=135˚C)	=	5 A
Q_c	=	11 nC

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

Package

TO-220-2

Halogen-Free

RoHS

Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

Part Number	Package	Marking
C4D02120A	TO-220-2	C4D02120

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Reverse Voltage	1200	V		
I_F	Continuous Forward Current	10 5 2	A	T_C=25˚C T_C=135˚C T_C=165˚C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	13 8.4	A	T_C=25˚C, t_P=10 ms, Half Sine Pulse T_C=110˚C, t_P=10 ms, Half Sine Pulse	
I_{FSM}	Non-Repetitive Forward Surge Current	19 16.5	A	T_C=25˚C, t_P=10 ms, Half Sine Pulse T_C=110˚C, t_P=10 ms, Half Sine Pulse	Fig. 8
$I_{F,Max}$	Non-Repetitive Peak Forward Current	200 160	A	T_C=25˚C, t_P=10 µs, Pulse T_C=110˚C, t_P=10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation	60 26	W	T_C=25˚C T_C=110˚C	Fig. 4
T_J	Operating Junction Range	-55 to +175	°C		
T_{stg}	Storage Temperature Range	-55 to +135	°C		
	TO-220 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

CREE

C4D20120H

Silicon Carbide Schottky Diode

Z-REC® RECTIFIER

V_{RRM}	=	1200 V
I_F (T_C=135°C)	=	26 A
Q_c	=	99 nC

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F
- Increased Creepage/Clearance Distance

Package

TO-247-2

Halogen-Free

RoHS

Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

Part Number	Package	Marking
C4D20120H	TO-247-2	C4D20120

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Reverse Voltage	1200	V		
I_F	Continuous Forward Current	54 26 20	A	T_C=25°C T_C=135°C T_C=156°C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	86 56	A	T_C=25°C, t_p=10 ms, Half Sine Pulse T_C=110°C, t_p=10 ms, Half Sine Pulse	
I_{FSM}	Non-Repetitive Forward Surge Current	130 104	A	T_C=25°C, t_p=10 ms, Half Sine Pulse T_C=110°C, t_p=10 ms, Half Sine Pulse	Fig. 8
$I_{F,Max}$	Non-Repetitive Peak Forward Current	1150 950	A	T_C=25°C, t_p=10 µs, Pulse T_C=110°C, t_p=10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation	246 106.5	W	T_C=25°C T_C=110°C	Fig. 4
dV/dt	Diode dV/dt ruggedness	200	V/ns	V_R=0-960V	
$\int i^2dt$	i^2t value	84.5 54	A^2s	T_C=25°C, t_p=10 ms T_C=110°C, t_p=10 ms	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C		
	TO-247 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

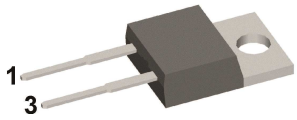
Standard Rectifier

V_{RRM}	=	1200 V
I_{FAV}	=	30 A
V_F	=	1.25 V

Single Diode

Part number

DSI30-12A



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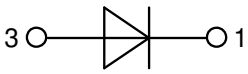


Features / Advantages:

- Planar passivated chips
- Very low leakage current
- Very low forward voltage drop
- Improved thermal behaviour

Applications:

- Diode for main rectification
- For single and three phase bridge configurations

Package: TO-220

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

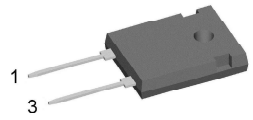
HiPerFRED

V_{RRM}	=	1200 V
I_{FAV}	=	30 A
t_{rr}	=	35 ns

High Performance Fast Recovery Diode
Low Loss and Soft Recovery
Single Diode

Part number

DSEP30-12B



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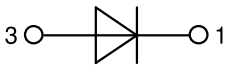


Features / **Advantages:**

- Planar passivated chips
- Very low leakage current
- Very short recovery time
- Improved thermal behaviour
- Very low Irm-values
- Very soft recovery behaviour
- Avalanche voltage rated for reliable operation
- Soft reverse recovery for low EMI/RFI
- Low Irm reduces:
  - Power dissipation within the diode
  - Turn-on loss in the commutating switch

Applications:

- Antiparallel diode for high frequency switching devices
- Antisaturation diode
- Snubber diode
- Free wheeling diode
- Rectifiers in switch mode power supplies (SMPS)
- Uninterruptible power supplies (UPS)

Package: TO-247

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

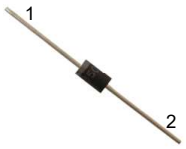
Silicon Carbide PiN Diode

V_{RRM}	=	15.0 kV
$I_{F\ (Tc=25°C)}$	=	1 A

Features

- 15 kV blocking
- 175 °C operating temperature
- Fast turn off characteristics
- Soft reverse recovery characteristics
- Ultra-Fast high temperature switching

Package



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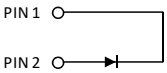

Advantages

- Highest voltage rectifier commercially available
- Reduced stacking
- Reduced system complexity/Increased reliability

Applications

- Voltage Multiplier
- Ignition/Trigger Circuits
- Oil/Downhole
- Lighting
- Defense

Maximum Ratings at T_j = 175 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values	Unit
Repetitive peak reverse voltage	V_{RRM}		15	kV
Continuous forward current	I_F		1	A
RMS forward current	$I_{F(RMS)}$		0.5	A
Operating and storage temperature	T_j , T_{stg}		-55 to 175	°C

Electrical Characteristics at T_j = 175 °C, unless otherwise specified

Parameter	Symbol	Conditions		Values min.	Values typ.	Values max.	Unit
Diode forward voltage	V_F	I_F = 1 A, T_j = 25 °C I_F = 1 A, T_j = 175 °C			6.4 4.7		V
Reverse current	I_R	V_R = 8 kV, T_j = 25 °C V_R = 8 kV, T_j = 175 °C			1	20 100	µA
Total reverse recovery charge	Q_{rr}	$I_F \le I_{F,MAX}$ dI_F/dt = 70 A/µs T_j = 175 °C	V_R = 1000 V I_F = 1.5 A		558		nC
Switching time	t_s		V_R = 1000 V I_F = 1.5 A		< 236		ns
Total capacitance	C	V_R = 1 V, f = 1 MHz, T_j = 25 °C V_R = 400 V, f = 1 MHz, T_j = 25 °C V_R = 1000 V, f = 1 MHz, T_j = 25 °C			22 4 3		pF
Total capacitive charge	Q_C	V_R = 1000 V, f = 1 MHz, T_j = 25 °C			4.5		nC

January 8, 1998

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- Low forward voltage drop
- High thermal shock resistance
- Corona free construction
- Low distributed capacitance

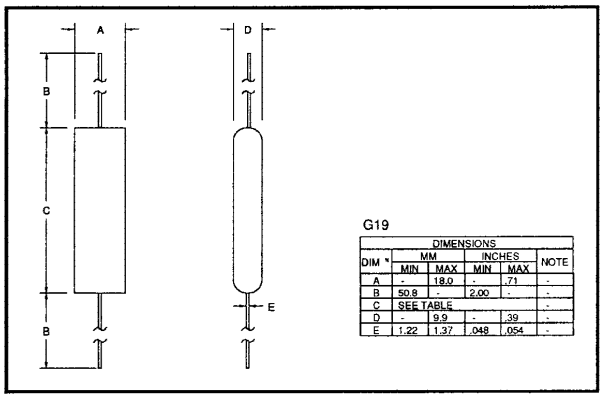
QUICK REFERENCE DATA

- V_R = 2500V - 15000V
- I_F = 2.0A
- I_R = 1.0 µA
- I_{FSM} = 80A

ABSOLUTE MAXIMUM RATINGS

Device Type	Working Reverse Voltage V_{RWM}	Average Rectified Current $I_{F(AV)}$				1 Cycle Surge Current I_{FSM} t_p = 8.3mS @ $T_{j\ MAX}$	I^2t t_p = 8.3mS @ $T_{j\ MAX}$	Repetitive Surge Current @ 25°C	Case Length dim. C Max
		@ 55 °C	@ 100 °C	Forced air 600CFM, 25°C	in still oil @ 55 °C				
	Volts	Amps	Amps	Amps	Amps	Amps	A^2S	Amps	Inches
SCHS2500	2500	2.0	1.2	2.0	4.0	80	26	31	1.53
SCHS5000	5000								2.53
SCHS7500	7500								3.53
SCHS10000	10000								4.53
SCHS12500	12500								5.53
SCHS15000	15000								6.53

MECHANICAL



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