# Design of Quantum Dot Electroabsorption Modulators for Next-Generation Data and Telecommunications

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I, Joe Mahoney, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the work.

# Abstract

The work presented in this thesis investigates the characterisation and optimisation of InAs quantum dots for the purpose of electro-absorption modulators. The modulator is a crucial component of the next generation of integrated circuits using photonics for lower power-consumption and faster data transfer speeds.

Initial studies measuring the quantum confined Stark effect in undoped and p-modulation doped InAs QD stacks highlighted an enhanced red-shift and increase in ground state absorption strength in the p-doped structure due to carrier blocking effects. The potential modulation performance was quantified with a standard figure of merit. The figure of merit, defined as the change in absorption for a given voltage swing over the absorption at $1V$ showed that the p-doped QD stacks had an improvement of as much as four times that of the undoped QD when applying a $9V$ swing between 21 to $100\,^{\circ}C$. The same level of improvement was observed in the p-doped sample using a $4V$ swing at $-73\,^{\circ}C$. This suggests the suitability of p-doped QDs for modulation in high or low temperature environments.

Further optimisation of the QD electro-absorption modulator was carried out using various simulation techniques. Schrodinger-Poisson models were used to get initial agreements between the model and the aforementioned measurement results. This model was then used to adjust various aspects of the QD stack to determine the optimum configuration for the modulator. The optimal configuration was found to use 7 QD layers, with a stepped doping profile within the p and n-cladding. This configuration led to an estimated 20% improvement in RC-bandwidth whilst having a negligible effect on the QCSE of the stack. This will enable high performance, low power consumption modulators for next generation data-communications. A

brief study into using total-internal reflection (TIR) mirrors to couple light from the QD III-V stacks to Silicon waveguides was carried out. The work showed potential for efficient, compact coupling of the light. Simulations produced using 3D FDTD found that the optimised system involved using $45^\circ$ angled reflectors for both the active and passive sections. The effect misalignment of the TIR's in both the x and y-axis on coupling performance showed a reasonable degree of tolerance when considering accuracy of typical fabrication techniques to both the overlap and relative confinement within the QD core compared to the expected TE mode profile.

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# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

## 1.1 Thesis rationale

Silicon is a key component of the electronics industry, which itself has become the backbone of today's technological advancements, with applications such as streaming, social media and banking relying heavily on the operation of data centres to run smoothly. One of the main issues currently facing the future of data and telecommunications is that electronic interconnects are requiring the use of ever-increasing amounts of energy to keep up with today's data demands [1; 2]. On top of this, with the potential end of Moore's law using microelectronics fast approaching as feature sizes on chips approach the size of individual atoms [3], new approaches to overcome the hard quantum limit of conventional transistors is needed.

Although transistor size has continued to decrease over the years in the data-communication sector, other factors within the larger electrical integrated circuit have become big issues in terms of performance and energy consumption. At the forefront of these issues as already stated is the interconnect. In standard integrated circuits these interconnects are typically very thin metal wires that are used to enable the input and output of information signals of the transistor and overall microprocessor. As transistor size decreases so too must the interconnect; so why is this such an issue? To understand this we need only use simple electrical analysis; with the requirement of smaller metal interconnects, the resistance of said interconnect increases. In conjunction with this, the required increased transistor

density in state-of-the-art integrated circuits requires these smaller interconnects to be packaged more closely together. This tighter packaging of interconnects inherently creates a larger capacitance between them. This is nicely illustrated in Fig. 1.1 and highlights how as the interconnect becomes smaller in size (primarily as both H and $L_s$ decrease) both capacitance and resistance increase.

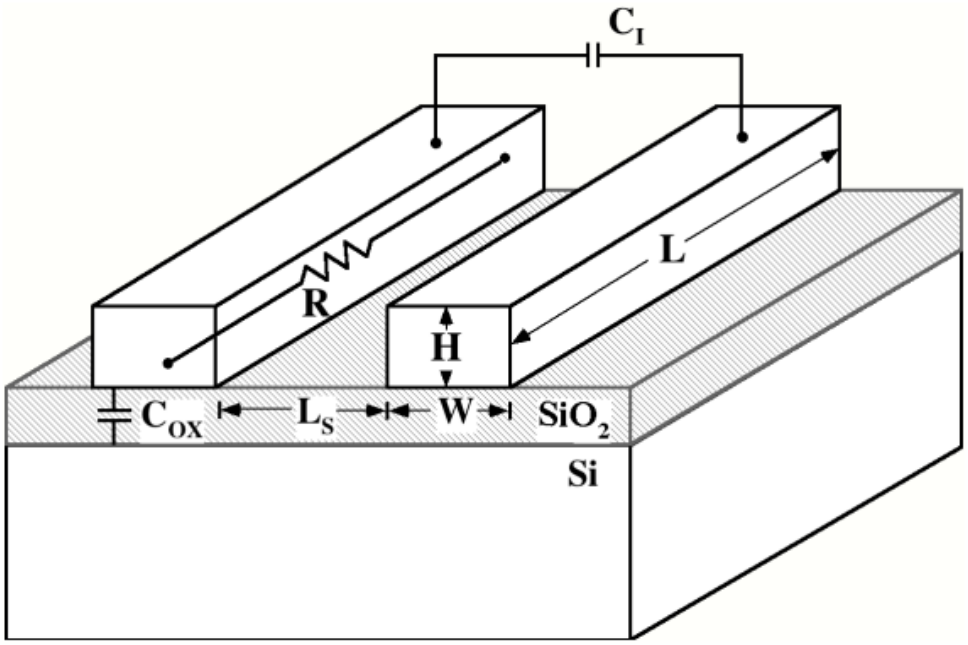


**Figure 1.1:** Figure adapted from [4; 5] showcasing where the resistance and capacitance of smaller and smaller electrical interconnects can become an increasingly important issue in the development of integrated circuit technology.

The main issue this increase in both resistance and capacitance initially causes is an increase in interconnect delay time sending or receiving signals to/from other areas of the integrated circuit. This becomes a problem when the interconnect delay is larger than the transistor gate delay. This issue is highlighted in [6] and is shown in Fig. 1.2. The Figure indicates that the interconnect delay will dominate the total delay time of the integrated circuit once the transistor becomes small enough. This dominance of the interconnect delay means any further benefits to the raw transistor performance become completely negated by the interconnect bottleneck.

The delay time is an important issue, but in conjunction with this the energy dissipation due to resistive heating under forward bias in the metal interconnect

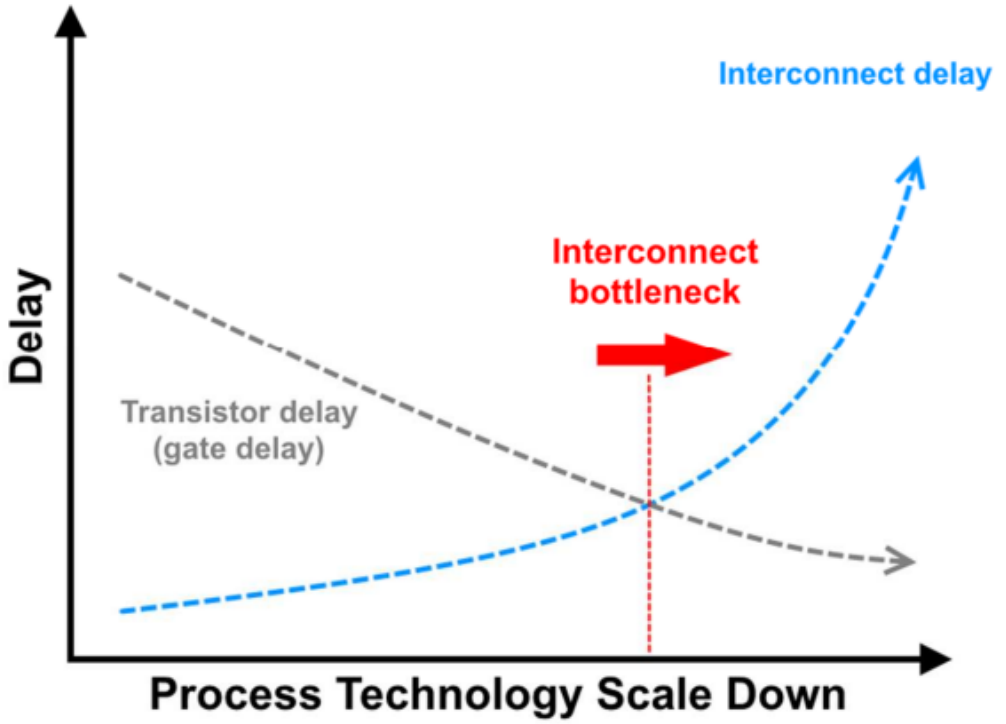


**Figure 1.2:** Figure taken from [6] highlighting the interconnect bottleneck issue. As transistor size decreases, improving transistor gate delay times, so the interconnect delay increases as they too become smaller. Once the interconnect delay is larger than the gate delay, any benefits in scale are mitigated.

becomes an ever more troubling issue with increased scaling of electrical integrated circuits [1]. Additionally capacitive discharge of the signal lines themselves [7] poses another significant contribution to the overall power budget of the chip. All of this leads to the real possibility of reduced rate of growth in processing performance (Moore's law) whilst also increasing power consumption on a huge scale. Data centres play a key role in enabling modern technologies, and various studies have been conducted trying to forecast the growth in power consumption data centres will require to continue to operate. Such work has predicted, as shown in Fig. 1.3, that annual global data centre power consumption could rise to as much as 750TWh by 2030 if Moore's Law is not upheld and there is a rise in internet of things (IoT) applications [8]. This is predicted to be over 2% of the available global electricity. Both from a financial but crucially an environmental standpoint, approaches must be considered to try and overcome this issue.

Photonics is widely seen as the next logical evolution to combat these increas-

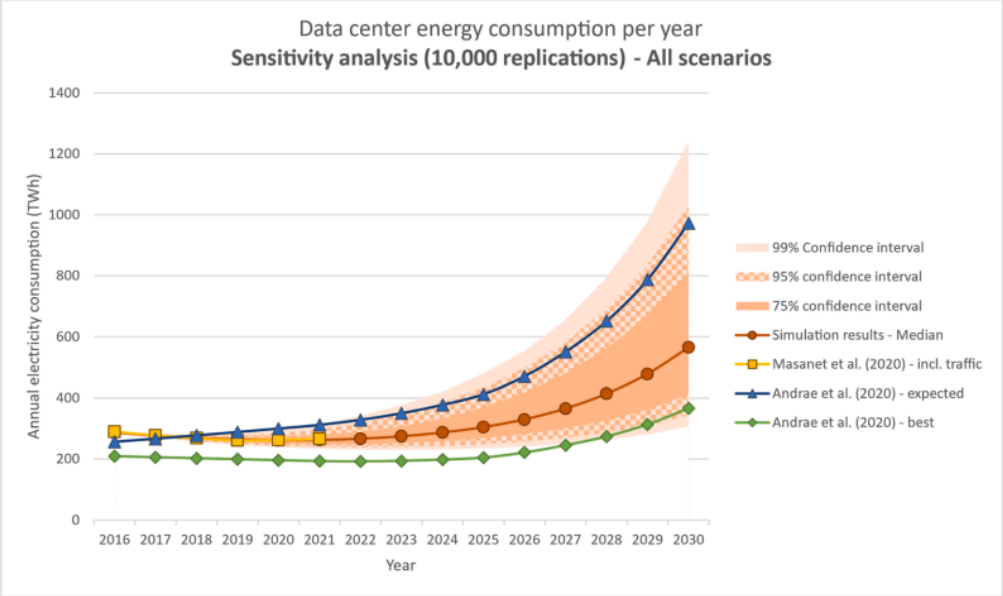


**Figure 1.3:** Figure taken from [8] highlighting the potential effect on data centre energy consumption if Moore's law fails to be upheld and the Internet of Things continues to rise in scale.

ing energy demands and improve data communication speeds. The bottle necking of delay times in optical interconnects is not an issue as they do not have resistive loss [9]. This lack of a resistive component to the optical interconnect also reduces energy dissipation, improving overall energy efficiency. Finally optical interconnects can be made to have far larger data transfer rates compared to electrical equivalents as they use photons to send and transmit information bits, which inherently travel far faster that electrons in a traditional electrical integrated circuit. In order to ensure that this photonic solution is feasible, the main drive in research is to use silicon as the basis of these photonic components, hence the term Silicon Photonics (SiPh) has been universally adopted for this area of research. As silicon is widely realised to be an inefficient active photonic material, the fundamental idea of this research area is to design photonic devices that combine III-V materials, which are generally efficient at emitting and interacting with light, with silicon in such a way that the device performance is comparable to photonic devices grown on native substrates. In addition to this it is crucial the design is compatible with complementary metal oxide semiconductor (CMOS) techniques that have been greatly developed in the

electronics industry. By being compatible with current fabrication techniques used in electronics means that these photonic devices can be produced on larger scales, improving scalability and lowering device cost. It is noted however that given that the De Broglie wavelength of electrons is significantly smaller that the wavelength used in photonic integrated circuits (PICs), any photon interconnects will typically require larger devices to ensure significant signal loss is not incurred.

However, there are various defects that commonly occur when integrating III-V materials with silicon (Si). These defects include issues such as threading dislocations as well as the potential development of anti-phase boundaries at atomic steps in the silicon lattice [10]. Such defects form non-radiative recombination centres and ultimately degrade both the performance and lifetime of such devices. It has been proposed that the use of quantum dots (QD) as the active region of these photonic devices could lead to improved performance due to their greater tolerance to such defects. Subsequently the designs put forward in this thesis will use QD active layers.

The work carried out over this PhD is on designing and optimising a key optical interconnect required for a PIC, the modulator. Although producing devices grown on silicon is imperative if feasible PICs are to be developed for next generation data and telecommunication technologies, it is also crucial that the overall physics of the active stack is understood and optimised. As a result, the work carried out in this thesis will look into aiding the development of the optimised QD stack for the purposes of electroabsorption modulation. It is therefore important that no obvious defects are present in the device to ensure the differences between any sets of measurements can be attributed to the changes made to the stack, and not variations in defects caused by the substrate. Although ideally devices would remain on native substrates, various processes such as the metallisation used to form electrical contacts on GaAs are not CMOS compatible. As such moving to a Silicon substrate base is paramount.

In principle, moving to a silicon substrate does pose some problems to potential device performance. Therefore, optimising on native substrates enables a clear

and efficient way to determine the best parameters required to achieve the highest device performance, without having to be concerned that the aforementioned issues associated with silicon are obscuring the clear observation of what improves, or hinders, the most efficient possible performance. Generally then, moving this optimised stack to a silicon substrate can then be done once the optimisation of the active region has been achieved. As a result, all measurements in this thesis were carried out on native substrates. Another point to consider is ensuring the III-V material operates at wavelengths which enable low-loss propagation within passive Silicon waveguides within the larger PIC. This is typically in the region of 1.3-1.5μm [11]. Within this thesis modulator performance in the O-band typically around 1310nm is considered.

## 1.2 Thesis outline

The focus of this thesis will be on the measurement and subsequent optimization and design of QD modulators for data and telecommunication applications. Chapter 2 will start with introducing the key areas of physics that will be exploited in succeeding chapters. Namely, a review of the quantum confined Stark effect (QCSE) as a means to achieve modulation is given and is compared with other modulation techniques to qualitatively define their advantages and disadvantages with respect to each other. Key QD properties are discussed that can be beneficial for active devices in the SiPh platform, and how their use has advantages for the QCSE as well.

Chapter 3 focuses on explaining the main measurement techniques and simulation model to be used in chapter 4 and 5 respectively. This description outlines the key aspects to ensure accurate results as well as the modifications made to the setup or model to further improve accuracy and efficiency of the results.

Chapter 4 will focus on the measurement work carried out on InAs QD segmented contact devices. A thorough examination of the QCSE in p-type modulation doped and unintentionally doped InAs QDs that are otherwise nominally identical is conducted using the segmented contact method [12]. Measurements of the QCSE in

both samples is carried out over a wide temperature and applicable voltage range. Quantitative figure of merits commonly used to understand prospective modulator performance are used to determine the benefits, if any, with p-type modulation doped the InAs QDs. Processing of PICs can require multiple rounds epitaxy and lithography to define all the different required devices. This complexity comes at the cost of increased processing time and cost. To enable the possibility of using the same epistructure to perform different tasks within the PIC is therefore an interesting prospect. As a result, this chapter also looks at the feasibility of using a common epistructure for two separate active functions; namely the QD modulator and laser. Optimal performance for both operations is carried out over a wide temperature range to see if sufficient performance can concurrently be extracted from both devices at the same operational wavelengths.

Chapter 5 looks into using simulations to aid in the further optimization of the QD modulator design. An investigation into aspects of the device such as optimizing the overlap between modal and static electric fields in the QD core is studied. A large part of this chapter looks into determining the intrinsic capacitance from both the measured and modified InAs QD stacks. This section of chapter 5 ends with a look into the optimised QD stack based on capacitance simulations to determine the effect on the QCSE. Initial simulations are compared with measurement to validate the model. With the QD models accuracy confirmed, a detailed analysis of the optimised stacks' QCSE is carried out and compared with the initial QD stacks for using both P-doping and unintentionally doped stacks.

This chapter also briefly looks at the prospect of using total internal reflection as a means to couple light to and from the QD modulator to a silicon waveguide. Different reflection angles are studied, as well as a study on device alignment, to determine the best configuration to achieve optimal coupling.

The final chapter gives an overview of the main results of this thesis. Additionally, thought is given to the potential future work that can be carried out building off what has been presented here, as well as the potential impact this work could have on future photonic devices within the Silicon Photonics platform.

# Chapter 2

# Theory and background

## 2.1 Introduction

To design and optimise next-generation modulators for the silicon photonics platform, there needs to be a clear understanding of the larger problem established. For example, being able to understand the issues of implementing III-V semiconductors on silicon through heteroepitaxial growth can lead to more efficient development of robust devices. In addition, having a fundamental understanding of the various main techniques utilised to achieve modulation is equally important. This not only involves understanding the physical phenomena that can be implemented to achieve modulation, but understanding their respective advantages and disadvantages for the desired applications.

This chapter will briefly look into the main issues involved with growing III-V on silicon. Subsequently a review of QDs and their potential robustness against these defects is presented. Different modulation techniques will be discussed, with a focus on the quantum confined Stark effect.

## 2.2 Difficulties of growing III-V on Si

The aim of this research is to develop optical interconnects for the main purpose of development for the SiPh platform. This last part is vital as it is only by utilising silicon as the basis of such devices can the cost and scalability be improved to such an extent that these devices become commonplace in future technologies. Unfortunately, due to silicon's indirect band gap the option to use it as the active regions

of these devices would drastically reduce performance and efficiency. Ultimately the direct epitaxial growth of direct-gap III-V materials on a silicon substrate is the most promising alternative, as there is the potential to achieve efficient performance whilst also capitalizing on silicon's cost effectiveness and scalability. However, this integration of III-V on silicon is not without its issues, the main of which will be discussed below.

### 2.2.1 Lattice mismatch

The first issue that will arise from this integration comes from the differences in lattice constant which will always be present between silicon and a III-V material. When growing III-V on silicon, the lattice constant mismatch will cause strain, which grows as more layers are added. Eventually after a certain number of growth layers the strain becomes so great that the system relaxes above a certain thickness [10]. This relaxation is caused via the generation of misfit dislocations. The formation of these misift dislocations is highlighted in Fig. 2.1. If these dislocations occur when growing on a large planar area (e.g. a substrate), these misfit dislocations will likely form threading dislocations (TD) [10]. TDs can create regions of non-radiative recombination, which will ultimately reduce the efficiency of a device. On top of this, the lifetime of the device is also degraded as these TDs become longer through a process called recombination enhanced dislocation climb [13; 14]. An image taken from [15] in Fig. 2.2 highlights the potential generation of TDs when growing III-V materials over silicon. One solution to try and mitigate this undesired effect is to implement a buffer region between the substrate and the active region. This method aims to ultimately 'trap' all the TDs within the buffer region so they have less of an effect on the active region, thus offering the potential of improved performance and lifetimes. An issue with this technique is that there may be reduced coupling efficiency between the device to a waveguide or other passive devices, as well as a greater density of thermal cracking due to the larger thickness with the inclusion of the buffer layer [16].

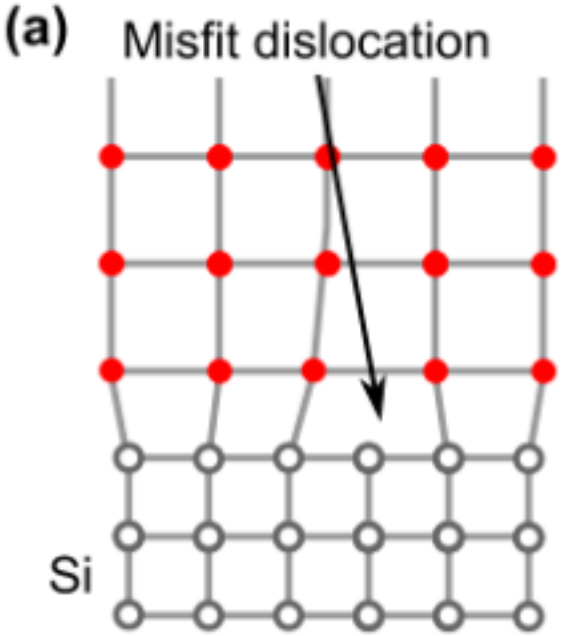


**Figure 2.1:** Diagram highlighting formation of misfit dislocation when materials of differing lattice constant is grown on top of another. Image taken from [17]

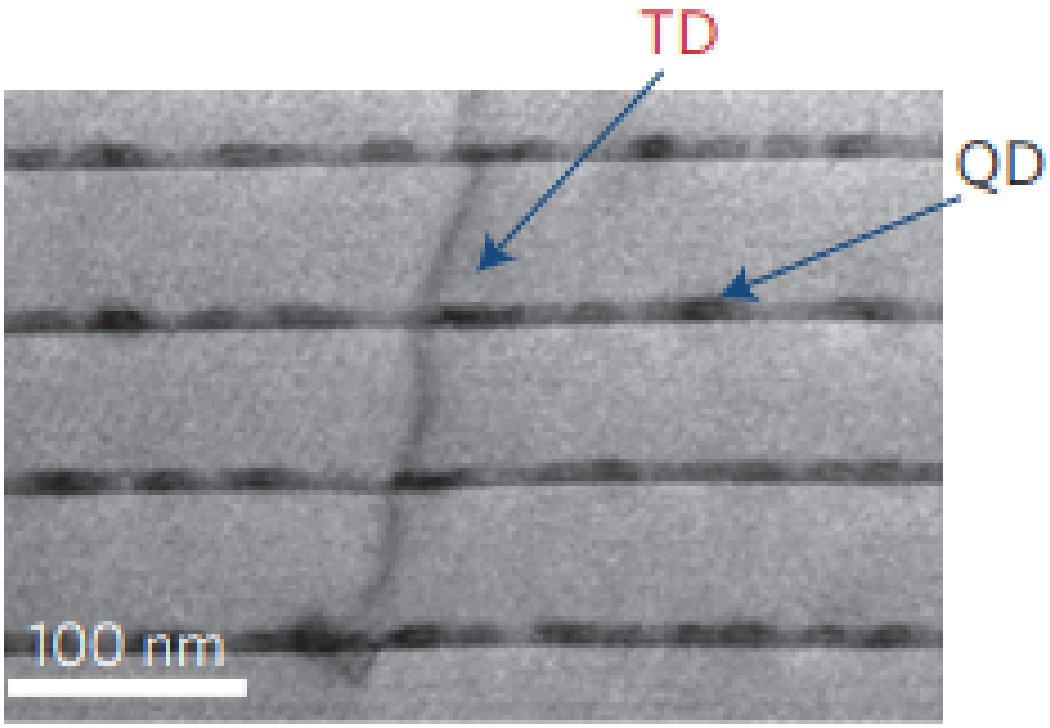


**Figure 2.2:** TEM image of interactions between TDs and QDs. Image taken from [15]

### 2.2.2 Coefficients of thermal expansion

The next major issue with epitaxially growing III-V's on silicon is that they have different coefficients of thermal expansion (CTE). This issue is most prevalent during the growth stage where temperatures can reach upwards of $600\,^{\circ}C$ during processes such as molecular beam epitaxy (MBE) or metallorganic chemical vapor deposition (MOCVD). The different CTE's in the materials means that when cooling down from these high temperatures to room temperature, there is the potential for cracks to form in the substrate, leading to the likelihood of losing a large proportion of the device yield [10]. Even if this were not to occur it is still likely that the strain caused from the changing rates of compression could lead to further encouragement of dislocations described above. It should be noted that typical temperatures sustained in the likes of data centres are around $80\,^{\circ}C$, and so the effects of CTE's in such an environment would be significantly less.

### 2.2.3 Anti-phase boundaries

Finally, because III-V materials are inherently polar (consisting of group III and V elements) and silicon is not, the epitaxial growth of III-V's on silicon can lead to the formation of anti-phase boundaries (APB), which can lead to the formation of anti-phase domains (APD). If the silicon substrate surface has single steps present in its bonding arrangement, the polar III-V material will grow on the substrate in such a way that two domains are created. The domains are separated by III-III or V-V boundaries, which are electrically charged and, like TDs, act as non-radiative recombination centres [18]. A diagram from [18] of how APBs are formed between III-V epilayer and silicon is shown in Fig. 2.3. This issue can be resolved by using miscut silicon as the substrate to introduce double atomic steps and the Si/III-V interface. The issue with doing this however, is that the use of miscut silicon means that the device design would not be compatible with current CMOS manufacturing techniques implemented in the electronics industry. Given that one of the main motivations for this research area is to produce low cost, highly scalable photonic devices the use of double atomic steps via miscuts is not feasible [10].

In spite of all these defects that can limit device performance, research into

developing devices that are more tolerant to these defects using QDs as the active material are being extensively studied, and will be discussed in the next section.

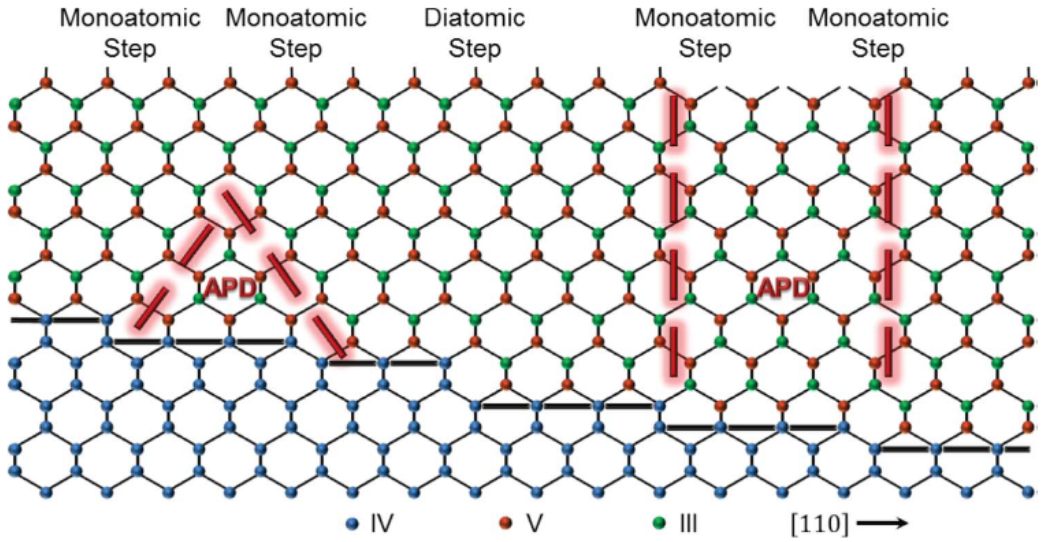


**Figure 2.3:** Illustration of development of APBs between a III-V epilayer and silicon Substrate. Image taken from [18]

## 2.3 Quantum dots

Quantum dots (QD) are nanometer-sized 3D structures where a narrower band gap material is buried in a wider band gap material. The dot sizes are at quantum length scales and lead to a discrete atom-like density of states. A comparison of the density of states found in bulk and QW materials with QD's is shown in Fig. 2.4. One of the main methods used to grow QD's is via a process called the Stranski-Krastanov method [19]. This method of growth is carried out typically using MBE or MOCVD and relies on the fact that the material used for the substrate and for the dots has some degree of lattice mismatch. As explained earlier this mismatch will cause strain on the growth layers. The strain on the growth material ultimately leads to the formation of self-assembled small islands. These formations are the more energetically favourable state as the strain is relieved from the material. These islands are the QDs which are typically then buried under a wider band gap material to produce the dot-well (DWELL) structure [19].

As the dots are self-assembled as a result of trying to relieve the strain, the dots

sizes are not identical, which can lead to inhomogeneous energy distributions for optical transitions. Despite this, QD's have the potential to offer numerous advantages for use in photonics over more thoroughly studied QW devices. For example, the small sizes of QD's means that there is less potential for them to interact with TDs. This reduced interactivity means that even if a small fraction of dots interact with such a defect, the rest of the QD's that do not interact with a TD will still be able to operate as expected [18]. This benefit is briefly demonstrated in Fig. 2.5. The strong strain field that is produced when growing QDs has also been attributed to the pinning or deflection of TDs away from QDs, offering even further tolerance to defects [15]. Furthermore, the reasons for QD tolerance to defects produced during growth also extend to externally-produced defects by events such as proton bombardment [20]. Such an event is common to occur in space and so a tolerance would prove beneficial for space applications or harsh environments in general.

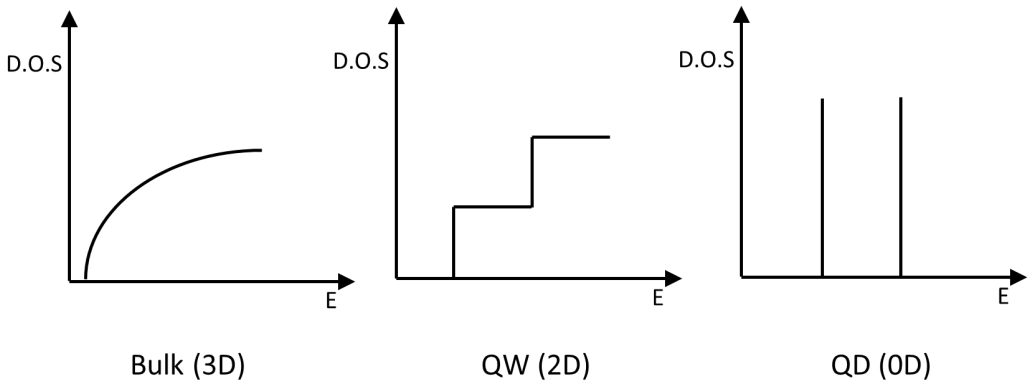


**Figure 2.4:** Plots of the density of states for bulk, QW, and QD materials.

In addition to their tolerance to TDs, QD active regions present the potential to offer far superior temperature tolerance than QW counterparts. This increased tolerance is a result of the fact that carriers are unable to thermally broaden into higher states. For example, InAs QD's have shown typical energy separations between the ground and 1st excited state of the conduction band of around 70meV, far higher than thermal energy at room temperature [10] which is approximately 26meV. The potential for greater temperature tolerance makes the use of QD's for high performance lasing over a range of temperatures an intriguing prospect.

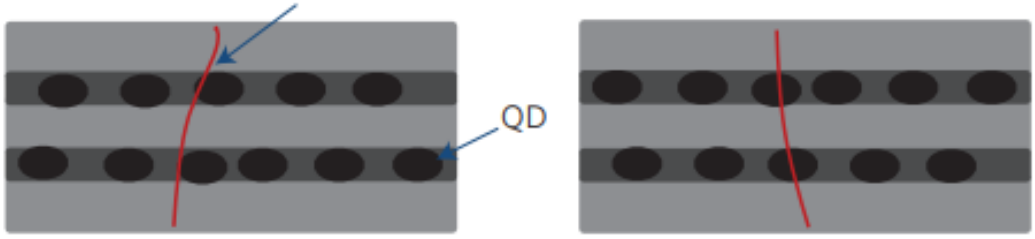


**Figure 2.5:** Illustration of lower likelihood of interaction between threading dislocations and QDs. Image taken from [15]

### 2.3.1 Confining carriers to device active region

In order to achieve a reliable active device, it is important to ensure that carriers are confined to the correct areas of the device in use. One of the more common means of achieving this is to confine the active region between thick layers of larger band-gap, heavily doped materials. This creates a p-i-n configuration that simultaneously achieves effective confinement and efficient means of biasing the device. The use of wider band-gap materials to confine carriers to a specific region can be used within the intrinsic region to create quantum-confined states. This is known as a separate confinement hetero-structure and is illustrated in Fig. 2.6. The figure highlights the p and n cladding regions and respective contacts, and shows the electron and hole Fermi levels under $0V$.

Fig. 2.6 shows a single valence band, however the electronic configuration of III-V materials typically produces three distinguishable valence bands. These are the heavy and light hole bands and the split-off band [19]. Typically the split-off band is far away in energy from the other two and so is typically neglected. The heavy and light hole bands in bulk materials are typically degenerate, differing only in their curvature in k-space. In quantum devices where there is significant strain present, degeneracy can be lifted between the heavy and light hole states and leads to one transition dominating at the ground state of the device. In typical InAs QD devices, it has been observed that this strain induced lifting of the degeneracy leads to heavy hole dominated transitions [19]. It has also been observed that heavy hole and light hole transitions are typically polarization sensitive, with heavy hole being predominantly related to TE light whilst light hole transitions generally having a

stronger TM composition [21].

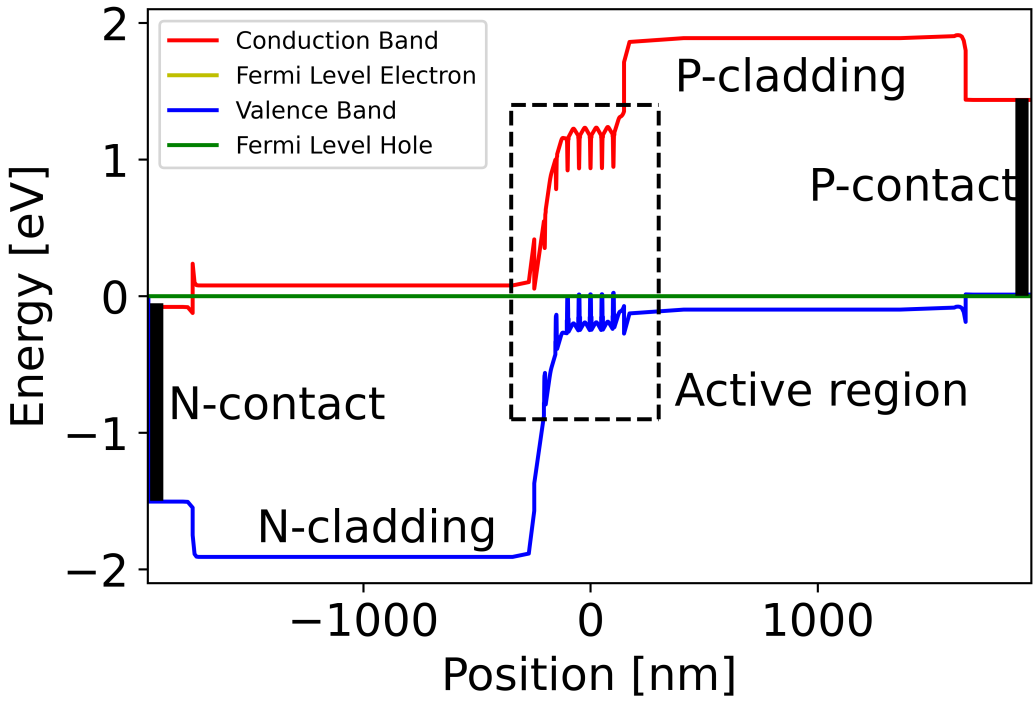


**Figure 2.6:** Band diagram of p-doped QD p-i-n structure under $0V$ highlighting p and n cladding regions and respective contacts along with QD active region.

### 2.3.2 Conduction-valence band transitions and Valence band asymmetry

As mentioned in the previous section, any transitions in most InAs QD devices are between the conduction and heavy hole states. The main transition mechanisms between these two states are spontaneous and stimulated recombination, stimulated absorption and non-radiative recombination [19]. In order to emit/absorb light efficiently, inter band transitions need to occur at the same k-vector. This can pose a problem in III-V materials where there is an asymmetry between the conduction and valence band due to differences in effective mass [22]. This difference generally leads to the conduction band having a smaller density of states compared to the valence band. This is an issue as this means there will inherently be many populated conduction states that lack empty valence states at the same k-vector. This will lead to a reduced maximum possible gain in III-V devices as the degree of population

inversion will be subsequently limited by the asymmetry [23].

### 2.3.3 P-type modulation doping

A well-established approach to try and reduce the valence asymmetry in III-V materials is to incorporate p-type modulation doping within the active region. The method has been used for QDs using GaAs [24] and Si [25] substrates to improve laser performance and has also been shown to be beneficial to QW devices [26]. The inclusion of a doped layer in InAs QDs has also been shown to lead to smaller reductions in luminescence intensity with temperature compared to undoped equivalents. This was attributed directly to the increased hole population in the ground state at higher temperatures [27]. The inclusion of a doped layer in close proximity to the dot layer allows an increased number of holes to be present within the valence states, which in turn lowers the quasi Fermi level. This helps to reduce the asymmetry, increasing likelihood of recombination events. The effect of including a doped layer close to the dots is shown in Fig. 2.7 and highlights the increased hole occupation in the ground valence states.

Modulation doping has also been used in QW modulators, where it has been suggested that the inclusion of the doping reduces the overall power consumption of the device by requiring a smaller operating voltage [28]. The effect of p-type modulation doping on the QD modulator has previously not been investigated. Given the already promising results of modulation doping for the QD laser, the demonstration of improved modulator performance using modulation doping in QD modulators may suggest the suitability of an optimised epistructure for both lasing and modulation. This would be a boon for any photonic application, as the ability to utilise a single epistructure for multiple functions would greatly reduce PIC fabrication complexity by requiring less processing steps.

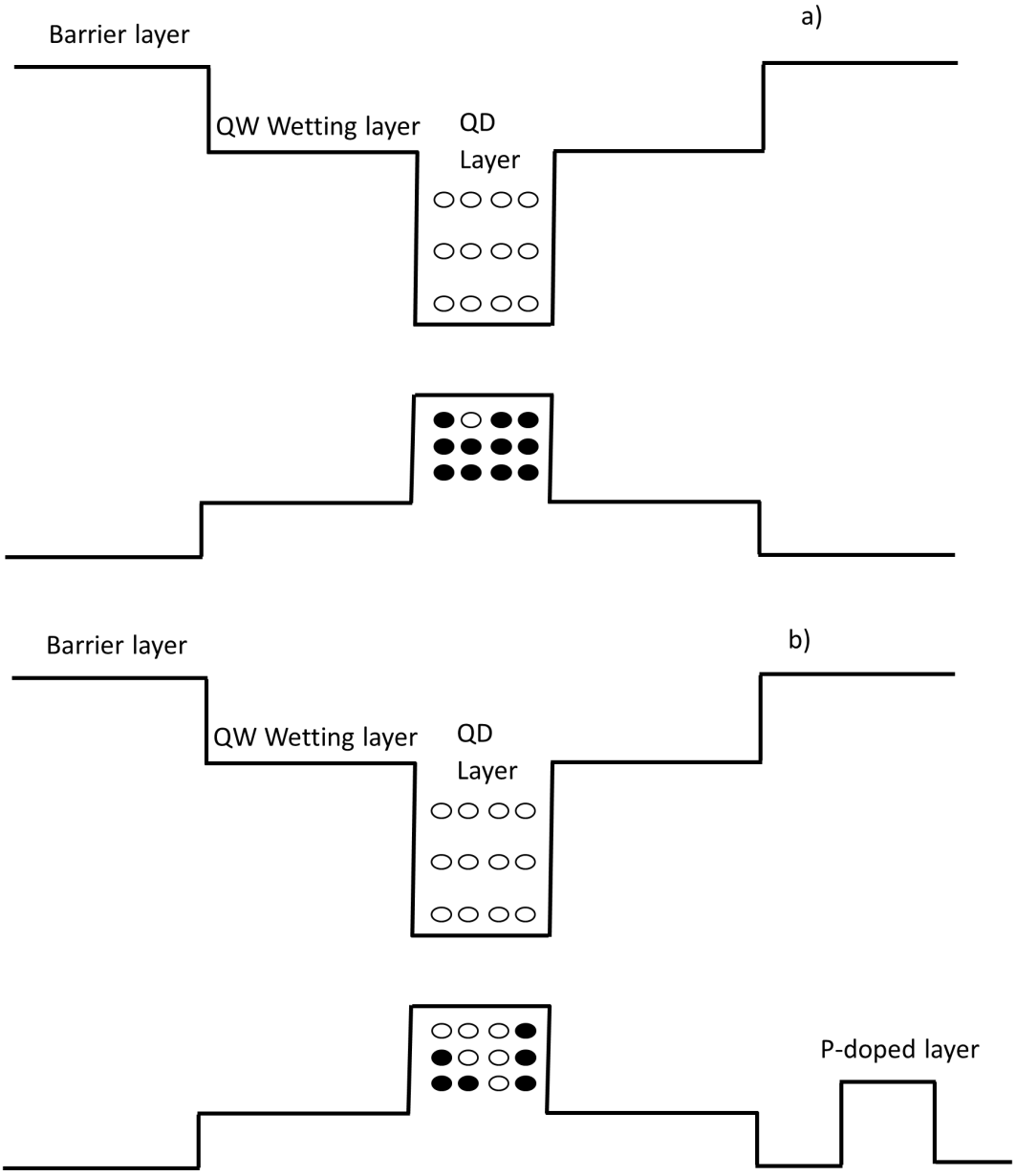


**Figure 2.7:** Diagram of band structure of a DWELL where barrier is a) undoped and b) has p-type modulation doping. Black circles are electrons and the white circles are holes.

## 2.4 Quantum confined Stark effect

The quantum confined Stark effect (QCSE) describes the change of the energy state separation of a quantum confined material under the influence of an external electric field. Typically, a QW or dot will have a discrete set of states of a certain energy that the electrons and holes occupy. When an electric field is applied these states

shift, thus affecting the frequencies at which the material can absorb/emit. On top of this the electric field will cause electrons and holes to move to opposite ends of the material (QW, QD etc.) which causes a reduction in the overlap integral of the electron and hole wavefunctions, leading to a reduction in recombination efficiency [29]. A simple diagram illustrating this is shown in Fig. 2.8. The QCSE is the main mechanism utilised for optical modulators today due to their strong absorption shifts and potential for high speed modulation [30].

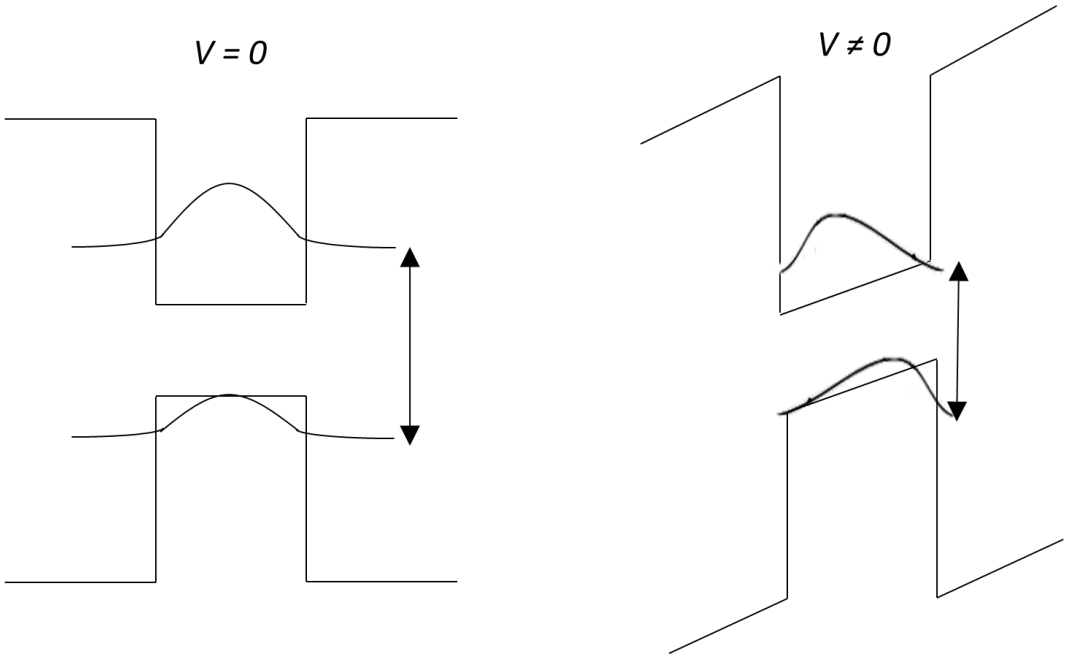


**Figure 2.8:** Simple diagram of the QCSE on band structure and wavefunction overlap of a material. When a voltage is applied, the band bends allowing lower energy transitions. Electrons and holes are pulled to opposite ends of dot material, reducing wavefunction overlap and subsequently absorption strength.

The expected shift from a particular applied bias can be approximated using perturbation theory [31] and should take into account excitonic effects. The presence of excitonic behaviour in QW's and, in particular, QD's is key to exploiting the QCSE. Due to the increased confinement of electrons and holes within the dot or well, even when large electric fields are applied, shifts in absorption spectra are still observed. This is not the case in bulk materials, where the excitons are not as confined. Subsequently, an increase in electric field would lead to reduced exciton lifetimes, ultimately limiting the degree the absorption spectra can be shifted [29].

Due to the three-dimensional confinement of carriers in QD's, it has been proposed that the stronger excitonic effect in QD's compared to QW's may lead to more efficient electroabsorption modulators (EAMs) [32]. This improved efficiency could allow for the ability to design smaller optical interconnects that have sufficient performance, which would lead to a greater density of components on a single chip.

## 2.5 Other types of modulation techniques

### 2.5.1 Franz-Keldysh effect

So far a discussion of the QCSE as a means to achieve absorption modulation has been presented. Here a brief description of the other possible means of modulation are discussed, with some discussion on their advantages and disadvantages. Along with the QCSE, the Franz-Keldysh effect is the other main physical phenomena that can be used to achieve absorption modulation. The Franz-Keldysh effect is similar to the QCSE, and can be thought of as the limit of the QCSE as quantum structures become larger and approach that of their bulk counterparts [33; 30].

The physical explanation of the Franz-Keldysh effect is as follows. When an electric field is applied, the energy band profile tilts along the direction of the electric field. The electron and hole wave functions then begin to leak through the band gap. Therefore, an absorption tail below the band gap exists allowing transitions at previously forbidden energies.

Although this effect can be useful, it is well established that the QCSE is the superior of the two approaches for absorption modulation. This superiority largely stems from the inability to achieve sharp absorption edges in the bulk materials when using the Franz-Keldysh effect, leading to weaker extinction ratios compared to quantum materials, where the modification to the density of states enables both sharper absorption edges, and larger electric fields to be applied due to the enhanced exciton binding energy found in quantum materials. Additionally, the push towards greater integration of optical devices in future PIC's means that using bulk material modulators that utilise the Franz-Keldysh effect makes integration with other, quantum based devices like the laser and photodetector more difficult. Clearly then,

when it comes to developing future absorption modulators, the QCSE is superior to the Franz-Keldysh effect.

### 2.5.2 Electro-refraction modulators

Apart from EAM's, the other main form of modulation used in optical interconnects is Electro-refraction. Simply put, this involves the change in the real part of the refractive index of the modulator material through the application of some external effect. This fact is in opposition to EAM's where it is the imaginary part of the refractive index that is changing under the application of an external electric field. The change in refractive index that occurs in electro-refraction modulators (ERM's) causes a change in the phase of the light propagating through the effected medium. Modulation can then occur by interfering this new wave with the original, unperturbed wave by using resonators or a Mach-Zender configuration. Fig. 2.9 shows a typical Mach-Zender ERM device. Subsequently, provided the phase difference between the original and new wave is different, the final output power from the device can be varied.

There are different means to achieve ERM's. A simple method is to vary the temperature of the device. The temperature change will induce a change in refractive index that can create the phase difference between two separate sources in order to achieve modulation. There are various issues with this approach to optical modulation. First and foremost, the requirement to change the temperature in order to achieve modulation is a slow process, and ultimately limits this approach of modulation to a small number of applications. In addition, for small devices that use this effect, temperature control over the whole system can become difficult, which can effect the extent of the phase difference between neighbouring waveguide arms. Despite these drawbacks, thermo-optic modulators are still actively being researched for applications that do not require GHz speeds such as LiDAR, with promising results indicating small-size, low-loss, low-power modulators in recent works [34]

Analogous to EAM's, an external electric field can be applied to change the real part of the refractive index to realise ERM's. Typically the effect seen in most applicable materials is called the Kerr effect. Often in modulator devices the Kerr

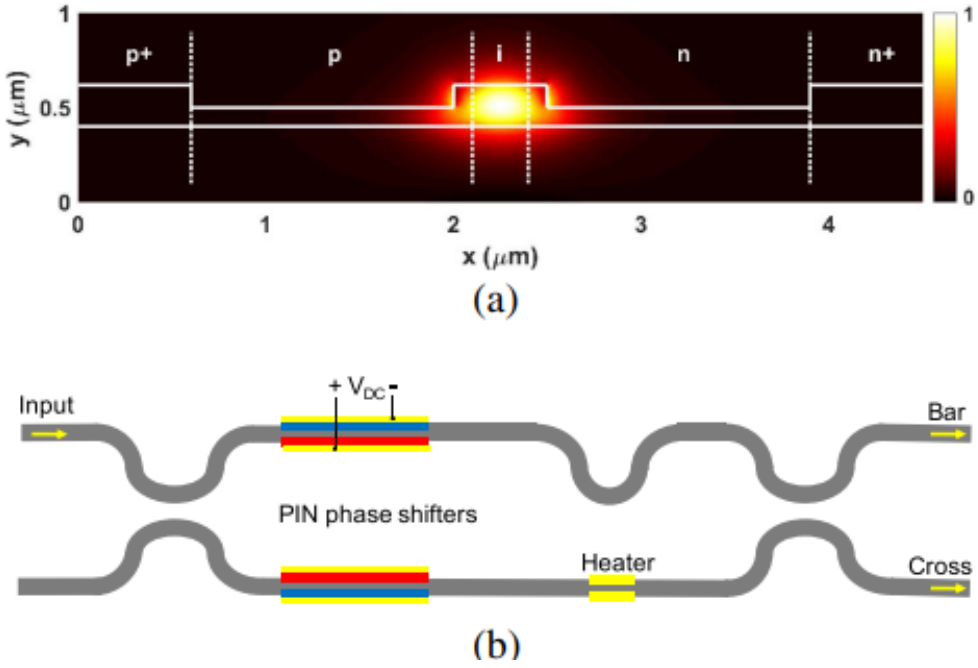


**Figure 2.9:** a) Typical PiN diode structure that can be used to create ERM's. b) Mach-Zender configuration often used to create phase difference that enables modulation. PiN phase shifters are incorporated in each arm to allow independent control of the phase. Bottom arm also incorporates a thermo-optic section for additional phase control. Image taken from [35]

effect is combined with the plasma dispersion effect in an additive fashion to enhance modulation characteristics of the device [35; 36]. The plasma dispersion effect involves the change of the material refractive index through a change in carrier density. Like with the Kerr effect, this most readily occurs when an external field is applied, hence why both effects can be present in an ERM concurrently. Although reasonable modulation performance can be achieved by implementing this type of ERM, the need to use interferometers to induce modulation can often require larger device footprints [37]. This is generally not an issue with the QCSE and more broadly speaking EAM's, where in principle compact devices are possible owing to the strong absorption changes that can be induced [30]. The Kerr effect in materials like Silicon and GaAs is generally quite weak [38; 39] requiring large fields to induce small changes in both refractive index and subsequently change in absorption. As such when using such materials this approach is not usually considered suitable for modulators.

### 2.5.3 Directly-modulated lasers

All of the above means of modulation require a dedicated device in order to modulate the light to produce the encoded signal. Of course another means of achieving modulation is to control the output of the laser directly. This simply means turning the laser on and off to create the desired signal. The main advantage of such a technique is that compared to using external modulators, directly modulated lasers are cheaper and simpler in design. However, the main disadvantages of using a directly modulated approach is that high modulation bandwidth is difficult to achieve as it is largely carrier limited [30] and chirp is more significant compared to using external modulators. Chirp is where the wavelength of the light emitted varies throughout duration of the emitted pulse [19]. This occurs due to the small variation in the laser material's refractive index when varying the electrical current to the device. This leads to dispersion which can obscure the encoded signal, leading to higher error rates in the generated signal.

## 2.6 Work on QD EAM's

When considering the design of EAM's, there are three main performance criteria that must be primarily optimised. These are the extinction ratio (ER), modulation bandwidth and voltage swing of the modulator. The extinction ratio is simply a means of quantifying the ratio between maximum and minimum operational light output of the modulator, and is given by equation 2.1.

$$ER = \frac{P_{through}(V = V_o)}{P_{through}(V = V_{shift})} = \frac{e^{-\alpha(V_o)L}}{e^{-\alpha(V_{shift})L}} \tag{2.1}$$

Where $\alpha(V)$ refers to the material absorption under an applied voltage $V$, $L$ is the device length and $P_{through}$ is the transmitted power through the device under an applied bias. The modulation bandwidth is a measure of how fast the modulator can be switched between "on" and "off" without significant loss in signal quality. The voltage swing gives an indication of the energy consumption of the modulator, and is given by equation 2.2 where $C$ and $V$ are the capacitance and operational voltage

swing of the modulator [40]

$$E_{bit} = \frac{CV^2}{4}. \tag{2.2}$$

The factor of $1/4$ out front comes specifically from using non-return to zero modulation. In such a scheme, the combination of adjacent signals (0 or 1) are 00,01,10,11. For a given data stream, there is one complete charging and discharging every four pairs of signal generation. As such the total energy per bit is therefore a quarter the enrgy to charge and discharge the device.

There has been limited research into the QCSE in QD's, but the work carried out thus far has been promising. For example, in [41] an EAM using InAs QD's ER of 10dB under a reverse bias of 10V at 1328nm. The transmitted power as a function of reverse bias that shows this is found in Fig. 2.10. The modulator in this work had a strain reducing layer of $In_{0.15}Ga_{0.85}As$ above the InAs QD's. This layer was included as InAs QD's typically emit between 1.1-1.2μm, and so the strain reducing layer was added to extend the emission wavelength to the more favorable wavelength of 1.3μm often used in communication technologies. However, the introduction of this layer led to the heavy hole wavefunction movement under reverse bias being suppressed by the potential barrier created by the $In_{0.15}Ga_{0.85}As$. This feature meant that only once a large enough electric field (bias) was applied (around 70kV/cm) where the barrier overcome, was there a significant decrease in electron and heavy hole wavefunction overlap to see a significant change in photon absorption. It was also observed that the full-width half-maximum of the QD spectra increased with increasing bias. This is a common occurrence when measuring the QCSE in QW's and QD's and is attributed to the effect of field ionization at larger applied fields [42]. Like in the Franz-Keldysh effect, where this occurs more prominently, widening of the spectra at larger fields leads to diminished performance.

Although [41] showed promise for QD's using the QCSE for electroabsorption modulators, no direct modulation was measured. This issue was not the case in [32] where 12 layers of $In_{0.75}Ga_{0.25}As$ QD's with an $In_{0.1}Ga_{0.9}As$ strain reducing layer

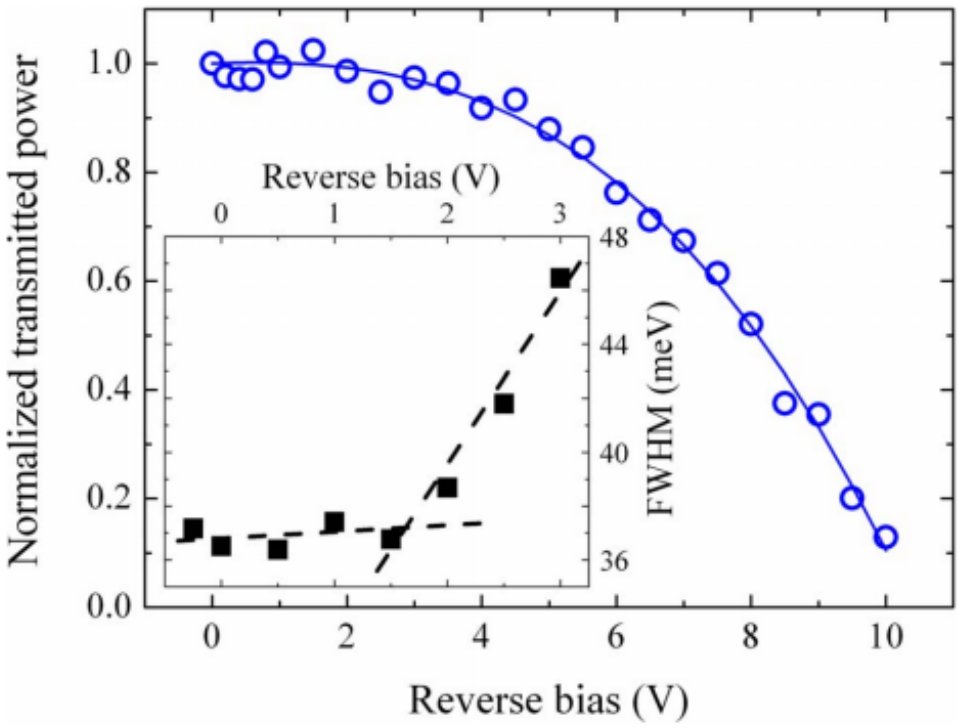


**Figure 2.10:** Normalised power transmitted in InAs QD modulator design from [41]. Inset highlights change in FWHM of absorption spectra.

was implemented. The device was 300μm in length and demonstrated an extinction ratio of 5dB by applying a reverse bias of 6V at 1310nm. This result was compared with a QW electroabsorption modulator of the same length and was found to achieve the same order of magnitude in extinction ratio in spite of the fact that the QD device had a lower density of states. This demonstrated the potential for stronger QCSE in QD's compared to QW's. The -3dB bandwidth of the device was measured and found to be 3.3GHz. This bandwidth is shown in Fig. 2.11. It was proposed that the main limitation on this value was caused by the lack of optimisation of the capacitance characteristics of the device. In addition to this, it was also suggested that as the design of this QD structure was based off a previous QW counterpart, that through device optimisation the modulation performance could be further improved.

A more recent work [43] used InAs QDs to determine the feasibility of achieving negative chirp modulation devices. Such a device would require signal amplification, but would enable a lower signal degradation through decreased chromatic

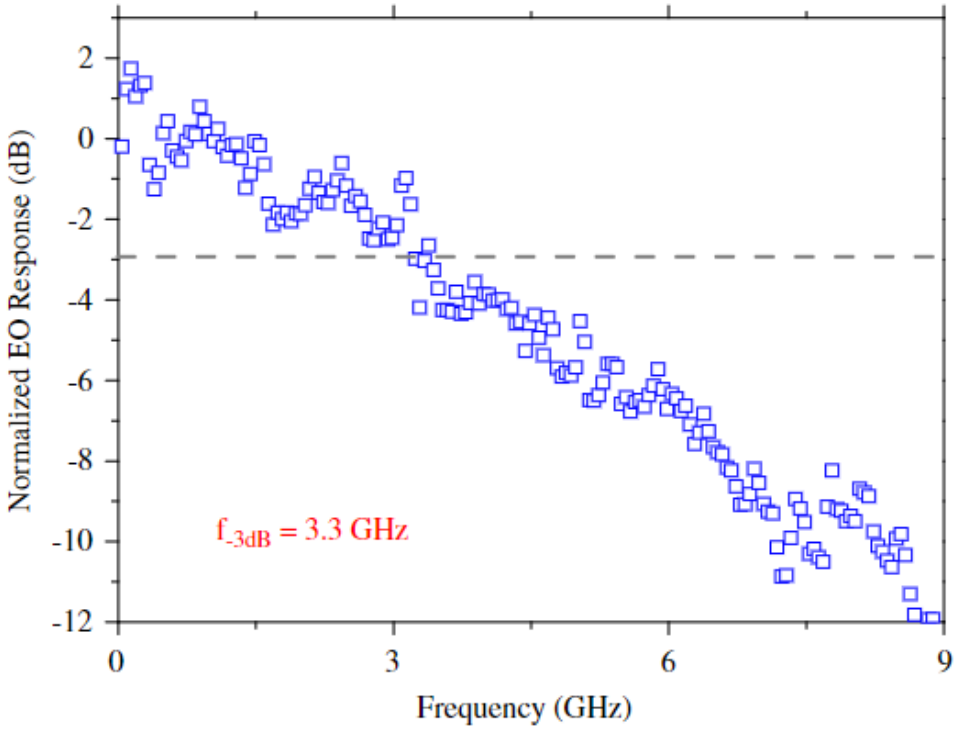


**Figure 2.11:** Elecro-optic response of InAs QD modulator, highlighting 3.3GHz operational speed at -3dB loss. Image from [32].

dispersion. This feature would ultimately enable longer transmission distances within the fibre. Fig. 2.12 shows the ER and insertion loss (IL) of the InAs QD devices for different detunings as a function of device length. The detuning refers to where above the band edge the device is considered to be "on" or "off". Blue detuning refers to using the low-voltage regime as the "off" state, relying on the reduction in absorption between the ground and first excited state that is present due to the modified density of states found in QDs. This reduction means an ER can be achieved when a reverse bias is applied to the devcie. Red-detuning is the more conventional approach where the low-loss band edge at low voltage is used as the "on" state, relying on the red-shift of the ground state absorption peak due to the QCSE under a larger bias to create a sufficient ER. Although reasonable ER can be obtained for the negative (blue) chirp regime, there is significant loss. This loss is why optical amplifiers are required in a practical device if this approach were to be realised in real-life applications.

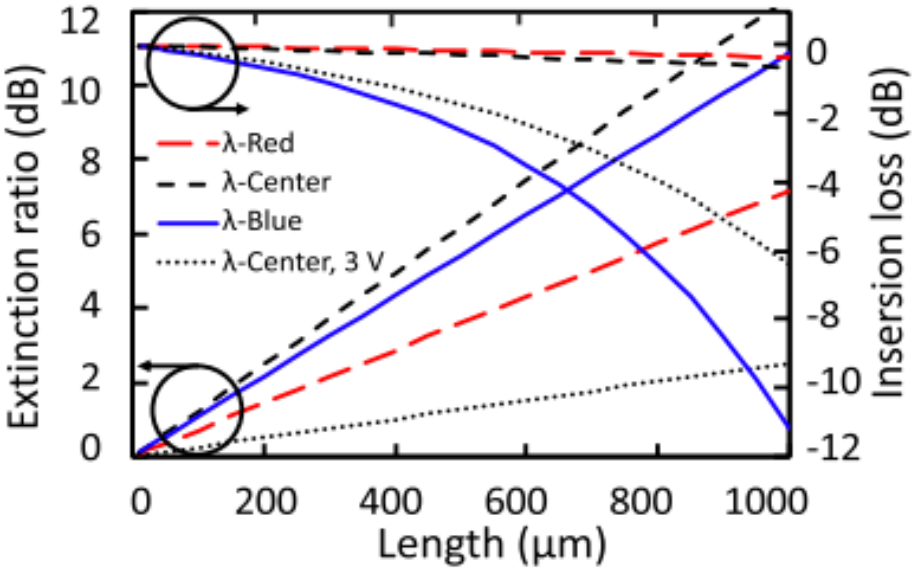


**Figure 2.12:** Extinction ratio and insertion loss as a function of length for different detuning modulation schemes. Image from [43].

Finally, as mentioned previously, it is crucial that for these optical components to be commercially viable, they must be compatible with silicon CMOS circuitry. The potential of using silicon as the substrate for a QD EAM was evaluated [44]. The modulator used five InAs /$In_{0.15}Ga_{0.85}As$ dot-in-well active layers each separated by a layer of GaAs. The device was 500μm long and used a 1200nm buffer layer of GaAs above the silicon substrate to try and capture any threading dislocations before they propagated up into the active region to try and mitigate any degradation in performance. At a reverse bias of 20V, extinction ratios of 5.1 and 21.6 dB were produced at 1310 and 1355nm respectively, which is shown in Fig. 2.13. This voltage swing is clearly is not as efficient as the devices described above grown on native substrates, but does indicate that through suitable optimisation of attributes such as the dot growth and device fabrication, using III-V QD's grown on silicon substrates is a viable method of achieving next generation optical modulators.

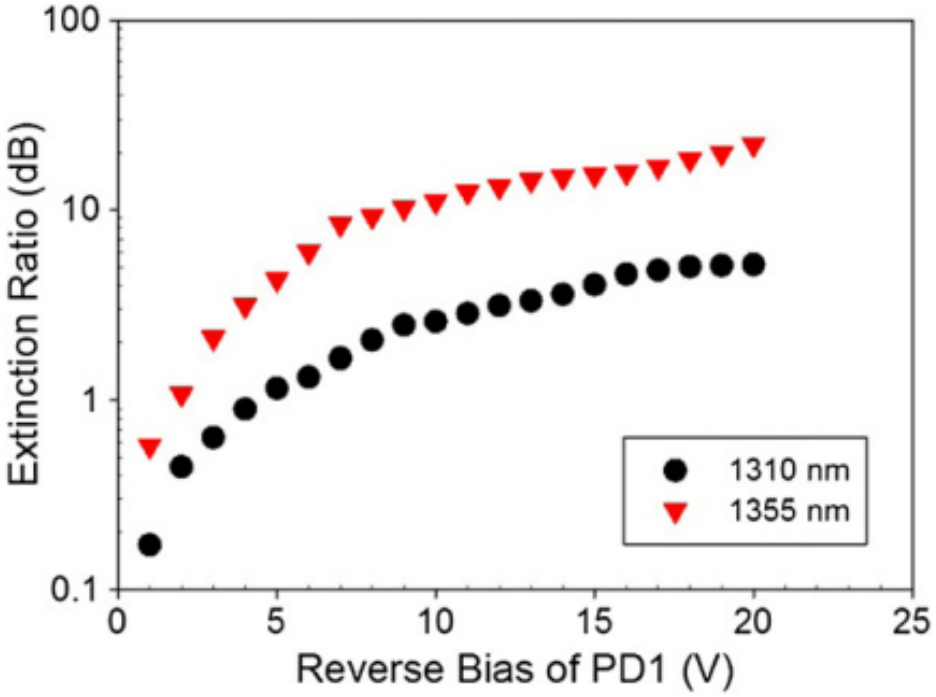


**Figure 2.13:** Extinction ratio obtained using InAs QDs on silicon multisection device as a function of reverse bias. PD1 refers to the section of the device where voltage is applied, and where absorption takes place (i.e. PD2 produces light and is adjacent to PD1, light from PD2 passes through PD1 which has an applied reverse bias, such that the transmission through PD1 is effected by the bias-dependent QCSE). Image from [44].

## 2.7 Coupling and integration techniques

Although achieving efficient active devices like the laser and modulator are important milestones, there is also a need to be able to effectively integrate such devices with passive waveguides. Being able to achieve such integration is imperative if feasible photonic integrated circuits (PICs) are to be achieved. In order to combine both the active and passive components of a PIC, light needs to be efficiently coupled from one to the other. Another caveat that needs to be considered is the desire to achieve efficient coupling and subsequent integration of active and passive devices using silicon substrates. As well as offering the incentive of lower material cost compared to using native substrates, it is widely known that being able to use silicon as the substrate presents the opportunity to leverage the superior economy of scale already present in the vastly more mature field of microelectronics. In addi-

tion to the economic benefits the tight confinement enabled by silicon-on-insulator (SOI) substrates offers superior performance for passive waveguide designs. There are numerous potential approaches that can be utilised to try and achieve efficient coupling to such waveguides.

Ideally the simplest approach to couple light between active and passive materials would be to evanescently couple the light between them, typically in the vertical direction. The major issue here is that in order to compensate for the severe mismatch in lattice constant, thick buffer layers are usually placed between the silicon and III-V layers to aid in reducing defect density in the active region. Although this in principle has been shown to improve active devices performance over silicon substrates [45], the increased distance between the active and passive regions greatly impedes the maximum coupling efficiency [16]. The following sections will investigate the other proposed options that have been put forward to evanescently couple light into the silicon waveguide.

### 2.7.1 Heterogeneous bonding of III-V and Silicon

Approaches to coupling to and from the silicon waveguide typically involve coupling the light from the III-V to the silicon waveguide either in the downwards direction or by horizontally butt-coupling to the silicon waveguide. Upward evanescent coupling can also be achieved by using amorphous silicon [46] or by bonding a silicon wafer on top of the active III-V material. After integration of the wafer from above, the silicon can then be processed into waveguides. A similar but far more widely implemented technique to couple light from the active to passive regions is to heterogeneously bond both sections together. In this approach both the active and passive sections are independently grown and processed and bonded together [47]. There are many obvious and immediate advantages to heterogeneously bonding the passive and active sections. First, provided both active and passive devices are grown over silicon substrates, the inherent scale and economic benefits of using silicon are retained. In addition to this, any buffer layers required when growing the III-V over silicon does not directly impede on the prospective coupling efficiency into the silicon waveguide.

Again however, there are some issues with this approach to achieving efficient coupling. First, there is of course the additional step of bonding the two sections together compared to some of the other common integration methods which only comprise of a single growth from start to finish. This extra step does add a degree of complexity to the procedure. In addition, there are inherent issues with the bonding itself, such as ensuring accurate alignment of both regions as well as the inherently high thermal resistance brought on the III-V to silicon bonding layer. At least in the context of the micro-ring laser, this increased thermal resistance has been shown to reduce maximum operating temperature when compared to monolithically integrated equivalents [48].

### 2.7.2 All III-V active/passive systems

The approaches to achieve coupling between active and passive components thus far have used a silicon waveguide as the passive material. Although using silicon does offer multiple advantages in terms of confinement and dimension, it is also completely possible to use III-V materials as both the active and passive segments, simply using the silicon as a substrate to drive down overall device cost. This approach can negate thermal resistance caused by the III-V/Si interface, offering the potential of higher temperature operation. In this all III-V system, the intrinsic region of the created p-i-n junction will house both the active and passive components. The active region will be shifted away from the center of the intrinsic region and can be confined there by creating sufficient mode-mismatch with the passive section in the remainder of the intrinsic region. Through tapering, the light can be efficiently coupled into and out of the III-V waveguide. Such a system was demonstrated in [49], where an InAs QD active region was used for lasing, with the output light being sufficiently coupled into a GaAs waveguide below. A diagram of the stack used in this work is shown below in Fig. 2.14.

Although there are clear advantages to implementing this approach to coupling the light effectively, there may be some drawbacks when looked at from the point of view of the modulator. In principle the thicker overall intrinsic region could lead to reduced device capacitance, which in turn would lead to improved bandwidth

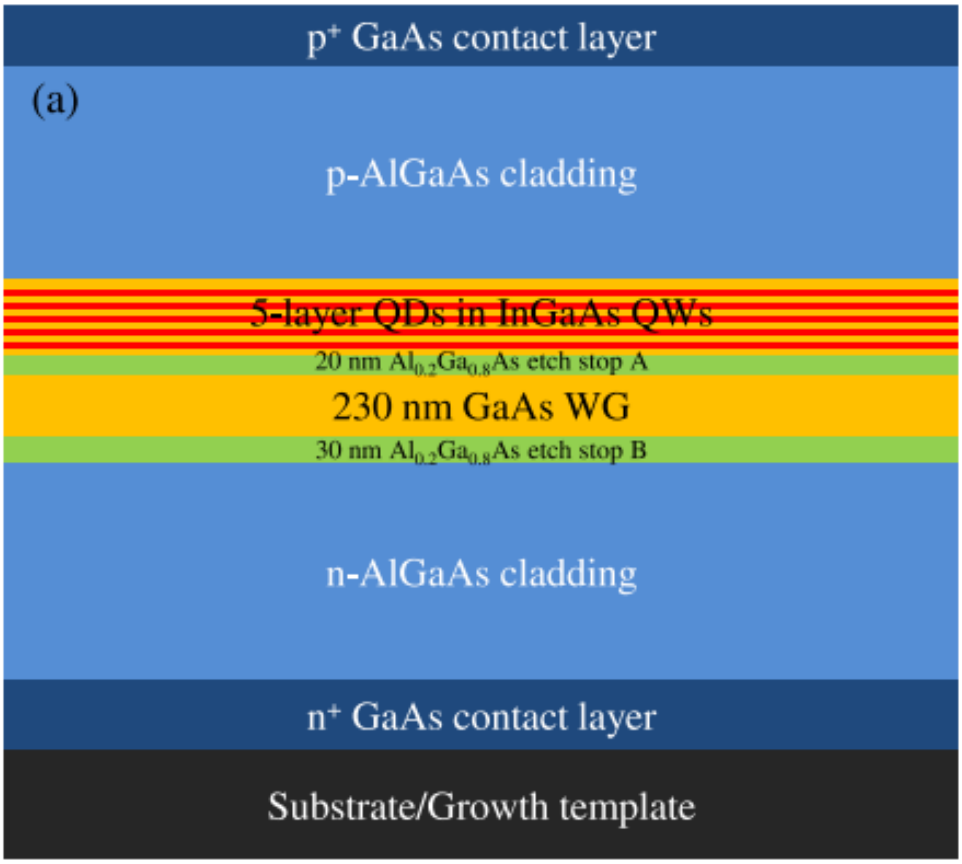


**Figure 2.14:** Device stack used in [49] using III-V materials as both active and passive components in the intrinsic region

performance in an RC-limited device. However, this increase in intrinsic region thickness would also affect the required voltage swing to achieve a sufficient extinction ratio, leading to increased power consumption to maintain a certain level of performance.

There are other ways to achieve active and passive components using all III-V materials without necessarily needing to use tapers. Analogous to using silicon, by implementing an additional re-growth step, one could achieve a butt-coupled active-passive system using a GaAs waveguide and QD active region. The key to using an all III-V system is to ensure there is a sufficient band-gap difference between active and passive components. In principle one could use intermixed QDs as the passive medium. Here, through ion implantation and a selective annealing process [50; 51], the passive bandgap can be blue-shifted to the extent that losses at

operational wavelengths can be drastically reduced. Despite demonstrations of such blue-shifting occurring in QD systems, there has been little work into the possibility of using such a technique to achieve efficient active-passive QD integration.

## 2.8 Chapter summary

This chapter has focused on providing a background to relevant and key theory that will be considered and implemented throughout the rest of this work. First the main issues faced when growing III-V over silicon were briefly discussed. This was then followed with a description of QDs and their potential to exhibit a far greater robustness to these issues than their QW counterparts. The benefits of QDs to the QCSE were also presented, along with an overall review of the physics behind the QCSE. To gain an appreciation of the relevance of the QCSE as a means to achieve modulation, other modulation techniques were presented. This looked at reviewing the fundamentals of the Franz-Keldysh effect as well as electro-refractive modulation approaches. Despite the different advantages and disadvantages each technique possess, the superior extinction ratios and modulation speeds present in the QCSE set it up as a front runner to be the strongest candidate for next-generation optical modulators.

# Chapter 3

# Experimental techniques and simulation model

## 3.1 Introduction

Being able to perform low noise measurements on samples is the most direct and reliable means of furthering our understanding of photonic devices. Ensuring the experimental setup is optimised to perform the desired measurements is therefore the paramount prerequisite before conducting a full characterisation of the QD structures used in this thesis. This chapter will therefore be dedicated to describing the main measurement techniques and software used throughout the subsequent chapters. Analysis of key modifications to some of the equipment and measurement setup are presented, with emphasis on the benefits attained through these modifications to the desired measurement outputs that will be analysed throughout this work.

## 3.2 Segmented contact method

To measure absorption and gain spectra data from samples studied in this thesis a technique known as the segmented contact method (SCM) has been used. The technique relies on measuring the amplified spontaneous emission (ASE) of the semiconductor material, which is then used to calculate optical modal gain and absorption spectra [12; 52]. A diagram of the multi-section device structure used in these measurements is shown in Fig. 3.1. The structure largely resembles an edge

emitting laser, with the notable difference of having gaps in the p-side metal contact. These devices have contacts placed on a 300µm pitch, with each contact 292µm in length meaning the contacts are separated by 8µm. This 8µm gap is then etched to remove the highly conductive p-type GaAs contact layer to reduce any leakage current whilst ensuring uniform pumping between any two adjacently-pumped sections. Having multiple metal contacts allows for sections to be pumped separately which is crucial for the technique to be successfully carried out. Separate pumping of sections is required as this enables direct calculations of gain and absorption spectra, which will be discussed in more detail shortly. Typically, only the two front sections are driven during the measurement, and the remaining sections are grounded, leaving them to act as passive absorbers. These grounded sections allow for the suppression of any round-trip amplification, meaning any light emitted from the front facet is a result of a net single pass gain. As well as using the rear sections to suppress round-trip gain, it can often be desirable to roughen the rear facet. When the light interacts with this damaged facet it is then scattered, leaving a small fraction to be reflected back into the device.

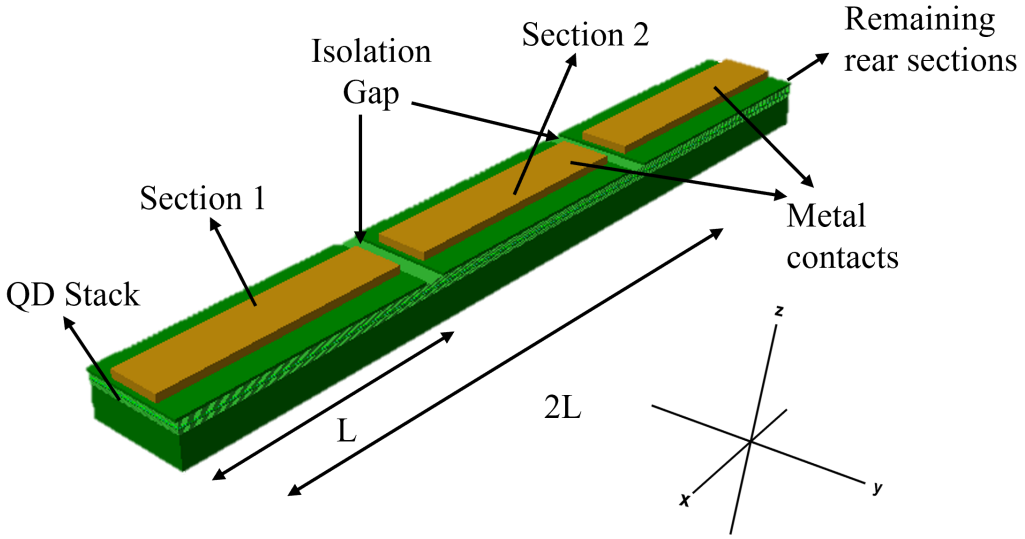


**Figure 3.1:** Diagram of typical Multisection device showing contacts and adjacent sections of equal length *L*.

Fig. 3.1 can be used to help to understand how the gain and absorption spectra are calculated from the measured ASE. As can be seen in the figure, light propagates along the $x$-axis in the device, with the plane and normal of the active region in the y and z-directions respectively. When the multi-section device is pumped, there will be multiple spontaneous emission events which occur in the $x-y$ plane of the active region. One can denote the rate of emission into a particular polarisation as $I_{sp}$. This rate has units of per second, per unit energy and per unit area. The light within the active region will undergo some amplification, with the intensity in the $x$-direction I($x$), subject to a net gain $G-\alpha_i$ originating from an infinitesimal point of thickness d$x$ and travelling a distance $x$, being given by

$$I(x) = \beta I_{sp} \exp[(G-\alpha_i)x]dx, \tag{3.1}$$

where the coefficient $\beta$ represents the fraction of spontaneous emission that is coupled into the waveguide in the $x$-direction and $\alpha_i$ is the internal optical loss. The subsequent ASE that is emitted from the front facet of the device after propagating a length $L$ is determined by integrating the above equation to obtain

$$\int \beta I_{sp} \exp[(G-\alpha_i)x)]dx = \frac{\beta I_{sp}(\exp[(G-\alpha_i)L]-1)}{G-\alpha_i}. \tag{3.2}$$

To obtain the gain spectra, two measurements are required. First, the ASE emitted from the front two sections together $I_{1+2}(2L)$ is measured, followed by pumping the front section alone, $I_1(L)$. By manipulating $I_1(L)$ and $I_{1+2}(2L)$, the net modal gain, $G-\alpha_i$, is subsequently given by

$$G-\alpha_i = \frac{1}{L}\ln\left(\frac{I_{1+2}(2L)}{I_1(L)}-1\right). \tag{3.3}$$

To calculate the net modal absorption spectrum, given by the modal absorption

$A(\lambda)$ plus the internal optical loss, a similar routine is carried out as above, however now the ASE is measured pumping section 1 and 2 separately, giving

$$A + \alpha_i = \frac{1}{L} \ln \left( \frac{I_1(L)}{I_2(L)} \right). \tag{3.4}$$

The basis of this approach to measuring the absorption spectra relies on sections 1 and 2 being the same length as well as being pumped at equal current densities [12]. If this is the case, then the ASE leaving section 2 and going into section 1 is equal to that of the ASE from section 1 at the facet. Subsequently, the ASE from section 2 when section 1 is unpumped gets passively absorbed by section 1, so by comparing the ASE from section 1 and 2 the absorption can be measured, giving the equation above. It was mentioned above how rear sections are grounded to supress round-trip amplification. It is also necessary to ground the sections that are not being pumped during a particular measurement (i.e. ground section 1 when measuring ASE from section 2 during the absorption run). Grounding any unpumped sections ensures that if any carriers leak into the adjacent section, they are swept to ground. This sweeping helps to avoid any recombination in that section, which would lead to false gain and/or absorption spectra being obtained.

The net gain or absorption spectra that are calculated from the SCM comprises of the modal gain/absorption and the internal optical loss, $\alpha_i$. For wavelengths above the absorption edge the net gain and absorption spectra converge to the internal optical loss of the material. The value of the internal optical loss can be effected by issues such as scattering by defects or rough interfaces. As a result, the value for $\alpha_i$ can reflect the overall quality of the material being measured. Fig 3.2 shows the convergence of the net gain and absorption spectra for a multi-section device using QD's and has an internal optical loss value of $\alpha_i \sim 1.4 cm^{-1}$.

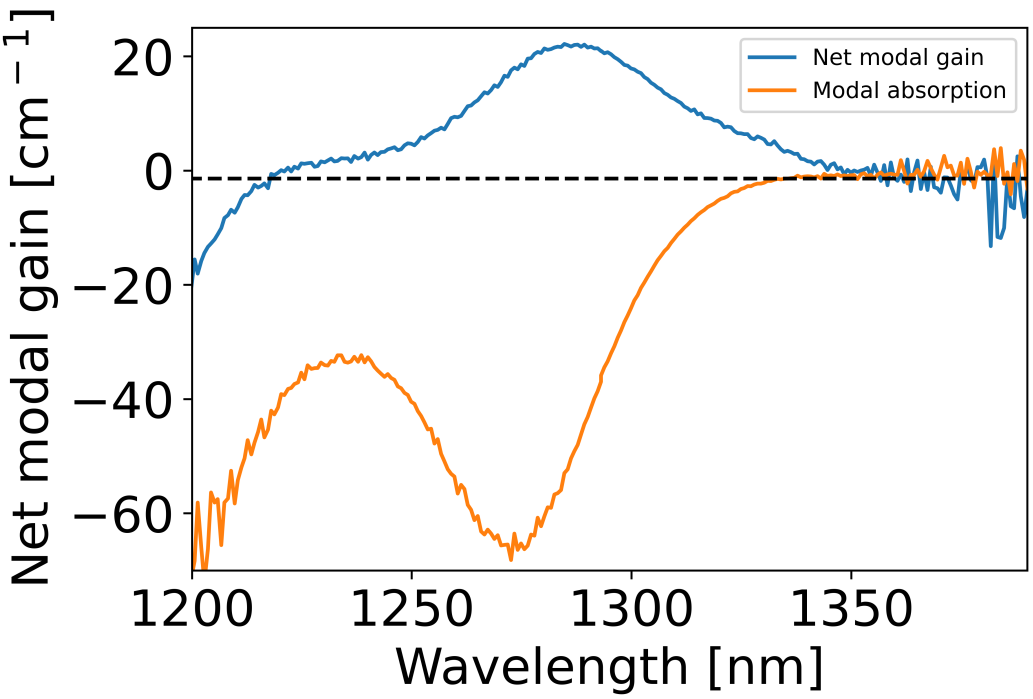


**Figure 3.2:** Plot of net modal gain and absorption spectra highlighting convergence to $\alpha_i$ at the band edge. Modal absorption plotted as negative gain.

### 3.2.1 Experimental technique

Fig. 3.3 shows a schematic of the experimental setup used to perform the segmented contact method on the QD devices used in this thesis. The QD multisection device is mounted to a stand or a microstat depending on if low temperature measurement runs are required. The stand has a heating element that can be set to a certain temperature using a Thorlabs TC200 temperature controller. A pair of in-house pulse generators are used to electrically pump the different sections of the device. The pulse generators are set to have a repetition rate of 5kHz with a 0.5% duty cycle. The pulse generators are also connected to a switch box to enable dynamic control of what sections are being pumped at a given time.

It is crucial that the multisection device is accurately aligned with the spectrometer to ensure that only light that has propagated the whole length of the stripe is being detected by the charge-coupled device (CCD) camera. Any stray light emanating from the multisection device that is collected by the camera will lead to incorrect ASE spectra, and subsequent incorrect gain and absorption spectra. There

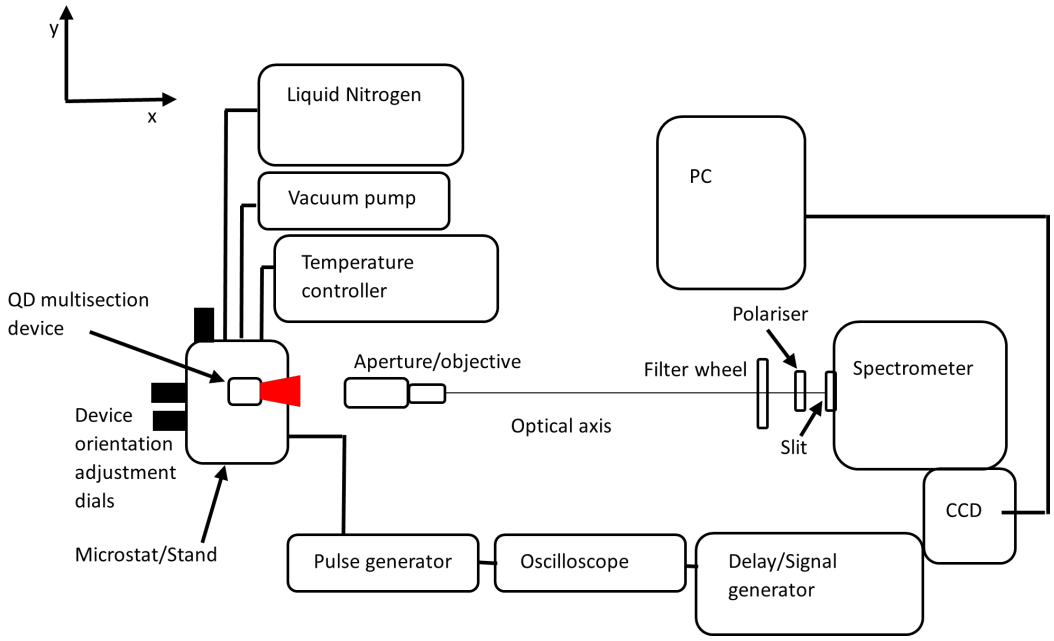


**Figure 3.3:** Schematic of experimental configuration used to perform segmented contact measurement on multisection device.

are several aspects of the measurement setup that are in place to try and ensure no such light is detected.

The first aspect that aids in correctly aligning the device is a positioning stage that has orientation adjustment dials that can adjust the position of the stand, and by extension the device, enabling up to six degrees of freedom. The dials can be used to focus the ASE beam with respect to the objective along the lights optical path. The objective also has a shutter that can be used to define a narrow aperture for the beam to pass through. Ensuring this aperture is as small as possible whilst still maintaining a sufficient beam intensity helps to reduce any diverging light from entering the spectrometer. The final aspect to aid in alignment is the use of an adjustable slit placed just before the light enters the spectrometer. Much like the shutter, ensuring this slit is as small as possible helps reduce the likelihood of diverging light entering the spectrometer. All of these aspects to alignment can be monitored and adjusted in real time by viewing the readout of the CCD camera. Additionally, just before light enters the slits, it passes through a polariser which is configured to only allow TE light into the spectrometer.

Once the ASE from the device facet is focused and aligned such that the shut-

ter and slits have been minimised, the ASE enters the spectrometer and undergoes dispersion such that the CCD displays the wavelength and near-field of the ASE on the x and y-axis respectively. To ensure the light entering is not too intense for the CCD camera (i.e. saturation or beyond linear operation of the camera), a filter wheel (and other filter windows if required) is used to reduce the incoming intensity to a manageable amount for the camera. During alignment the integration time of the camera is set to 500 milliseconds to allow for rapid adjustment of the stage to reduce alignment time. Then when the measurement is being taken the integration time of the camera is increased to 20 seconds to help produce an ASE with a higher SNR.

### 3.2.2 Further requirements for accurate measurements using SCM

As mentioned above, it is important that there is no round-trip amplification, which is limited by having unpumped sections grounded at the back of the device and roughening the rear facet. In addition it is important that the current injected into the sections produces a consistent current density over the entire pumped length. This can be checked by inspecting the I-V characteristics of adjacent sections. If they are shown to be the same, there can be confidence that an equal amount of current is delivered to each section when driven together by a single pulse generator. The near-field profile can also be used to determine the current spreading of each section. The near-fields should therefore be the same for any measured sections, and can also be used to calculate the current density applied to each section.

As was discussed in the previous section, the measured ASE should ideally have travelled parallel to the x-axis in Fig. 3.1. To check that the device is aligned with the optical axis, initial test runs measuring gain and absorption are carried out. If the sections are electrically identical, and the system is aligned, one would expect the internal loss of both the gain and absorption spectra to converge at low energy, as can be seen in Fig. 3.2. If this does not occur then it suggests that further adjustment to the position of the device is required to ensure light from the pumped sections is only being collected which has travelled the section length $L$.

It is also crucial that inter-contact resistance is high (typically inter-contact resistance of more than 200Ω) so that any current spreading only reaches pumped sections, and not unpumped sections. Nevertheless, any remaining current leakage must be compensated for in order to obtain the correct ASE spectra and hence gain and absorption data.

### 3.2.3 Current compensation

The previous section briefly mentioned the need to compensate for any leakage current in order to ensure the correct ASE spectra is obtained, and subsequently the gain and absorption of the measured material is accurately produced. A large inter-contact resistance between sections, along with grounding any sections that are not pumped should significantly reduce any leakage current. Nevertheless, trying to compensate for any remaining leakage increases accuracy.

To find the leakage current, I-V characteristics of the multisection device need to be measured. Fig. 3.4 shows the I-V characteristics of such a QD multisection device. The leakage current can then be found from the gradient before diode turn-on, shown in equation 3.5

$$I_{leak} = m_{leak}V + c_{leak}, \tag{3.5}$$

where $V$ is the voltage dropped, $m_{leak}$ and $c_{leak}$ are the respective gradient and intercept of the turn-on region.

With this information, the current actually contributing to the ASE is then the injected current minus the leakage current. The gradient and intercept of the diode's on-region of the I-V trace can also be found using a similar expression given by

$$I_{on} = m_{on}V + c_{on}, \tag{3.6}$$

where $m_{on}$ and $c_{on}$ are the respective gradient and intercept of the diodes on-region.

By realising the desired current to produce the ASE is $I_{on}$ - $I_{leak}$, the compensated current $I_{comp}$ can be found by using the expression given by 3.7, where $I_{want}$ is the desired current wanted within the device contributing towards the ASE.

$$I_{comp} = m_{leak}\frac{I_{want} + c_{leak} - c_{on}}{m_{on} - m_{leak}} + c_{leak} + I_{want} \tag{3.7}$$

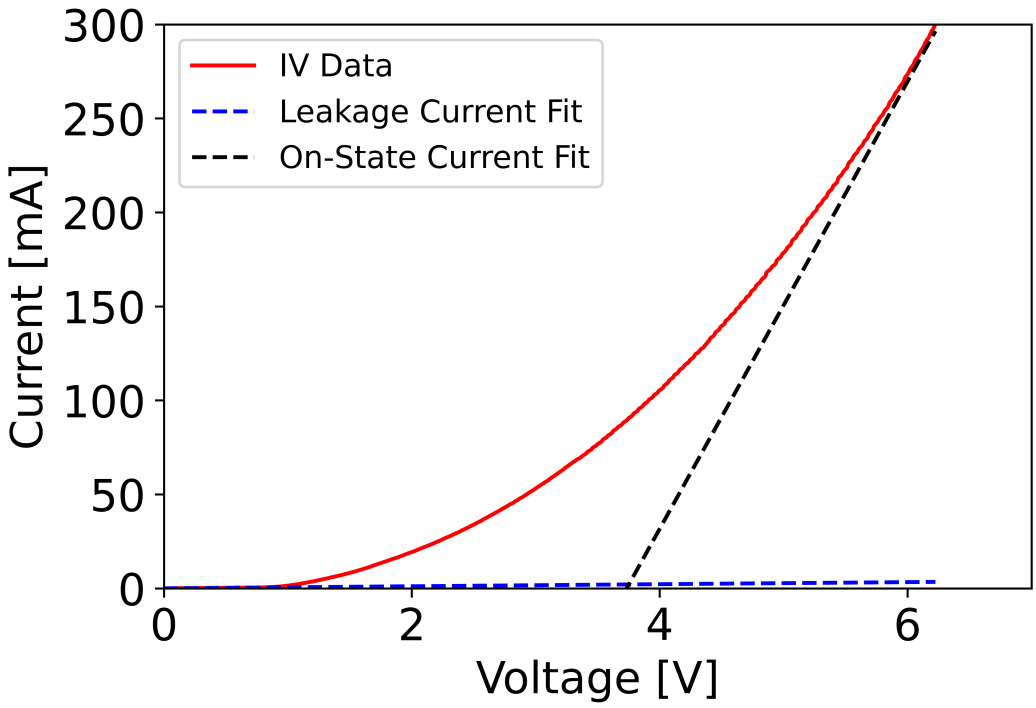


**Figure 3.4:** Plot of I-V characteristics for an InAs QD material. Leakage current is calculated from the gradient of the turn-on region of the plot. This leakage current can then be used to more accurately determine the current that is flowing in each section, and therefore ensure accurate ASE spectra is obtained. Adjacent section is grounded when pumping (i.e section 2 grounded when pumping section 1 and vice versa).

## 3.3 Modifications to SCM setup

### 3.3.1 IV measurement on SCM setup

The first of the two modifications made to the experimental setup that the segmented contact method is carried out on regards adding the capability to do basic current-voltage measurements. As mentioned in the previous section it is important to be

able to compensate for any current leakage in the device. To understand how 'leaky' a device may be I-V measurements are carried out on each section and pair of sections (typically section 1,2,3,1+2 and 2+3). Up until recently in the lab this has been done on a separate oscilloscope and pulse generator not connected to the segmented contact measurement equipment. Although this setup of doing I-V measurements on a separate kit is useful as it allows two users to work concurrently (one on longwave kit doing SCM and other doing I-V's on a different device), there are some issues with not having I-V capability on the SCM experimental setup. The main issue is that the kit currently used to measure I-V's for the multisection devices is not set up to perform the measurement at high temperatures or with any sections reverse biased. This is an issue if it is desired to measure gain and absorption spectra at high temperatures or under reverse bias to observe the QCSE, as leakage is likely to change under these different scenarios, and so must be correctly compensated for if the measurement is to be as accurate as possible.

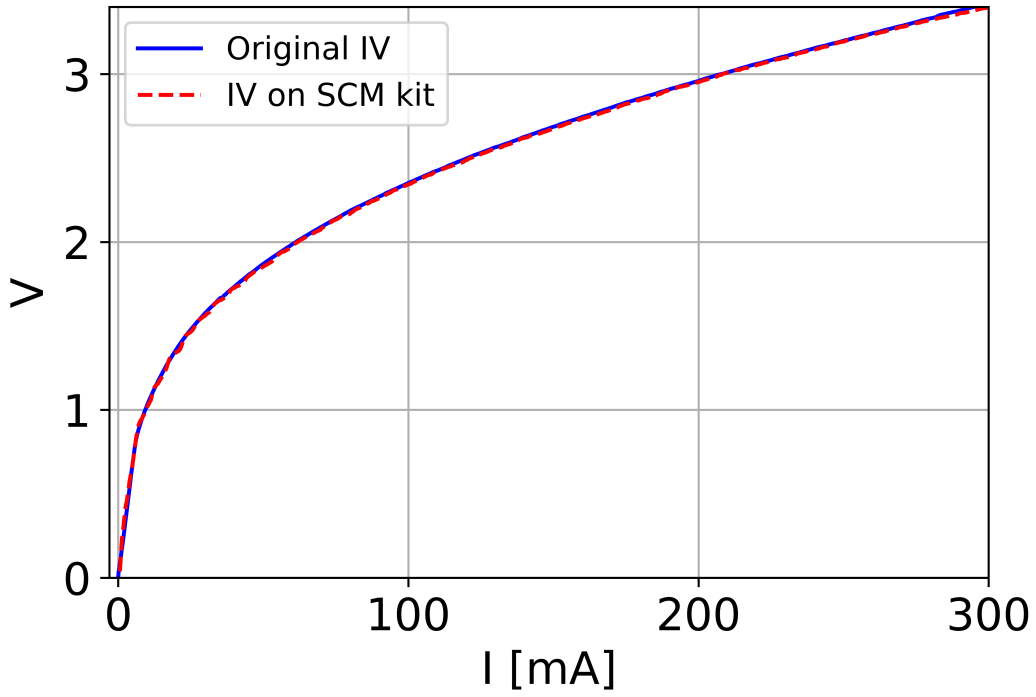


**Figure 3.5:** Comparison of I-V measurement of InAs QD test multisection device using original kit and modification to SCM experimental setup.

To measure I-V's on the longwave kit a modification was made to the MatLab

code currently used to perform the SCM that added a new tab to the user interface to enable this measurement. The tab allows the user to set a current and voltage limit to the measurement, along with the ability to choose what sections will be forward biased, reverse biased or grounded. To determine if the modification was measuring the I-V relationship correctly, a previously measured sample on the original I-V kit was re-measured using the modification to see if they matched, which is shown in Fig. 3.5. The figure demonstrates how the modification has successfully been implemented as the I-V characteristics are almost identical between the two kits.

### 3.3.2 Absorption-only mode implementation to SCM setup

The second modification made to the SCM experimental setup was to enable an 'absorption only' SCM run on devices. As mentioned in section 3.2, to measure gain one needs ASE spectra from section 1 and section 1+2, and for the absorption spectra one needs ASE spectra from section 1 and section 2. The standard setup on the SCM experimental setup is to measure all the above combinations such that both the gain and absorption spectra can be calculated from one measurement run. The issue in doing this is that prior to starting the measurement, the device must be set up such that the ASE is not saturating the camera to ensure the measurements are reliable and do not damage the camera itself. This fact means that usually during alignment section 1+2 are pumped together, as this combination will produce the greatest intensity.

Providing that section 1+2 intensity does not reach the non-linear range or saturate the camera, the ASE from section 1 or 2 in isolation will not either. This is fine for measuring gain as the signal is as strong as it could be, thus meaning the gain spectra should have a good signal to noise ratio (SNR). However, in the case of measuring the absorption spectra, the SNR could actually be improved by not measuring the ASE from sections 1+2 together. This would mean aligning the device while pumping only section 1 so the intensity from either section 1 or 2 is as large as it can be without saturating the camera. The goal of allowing for an absorption only mode then is to improve the SNR and ultimately the accuracy of the absorption spectra obtained. In Fig. 3.6 absorption spectra from the same device are

shown using the standard SCM routine of measuring every combination of section pumping as well as the spectra from the absorption only modification.

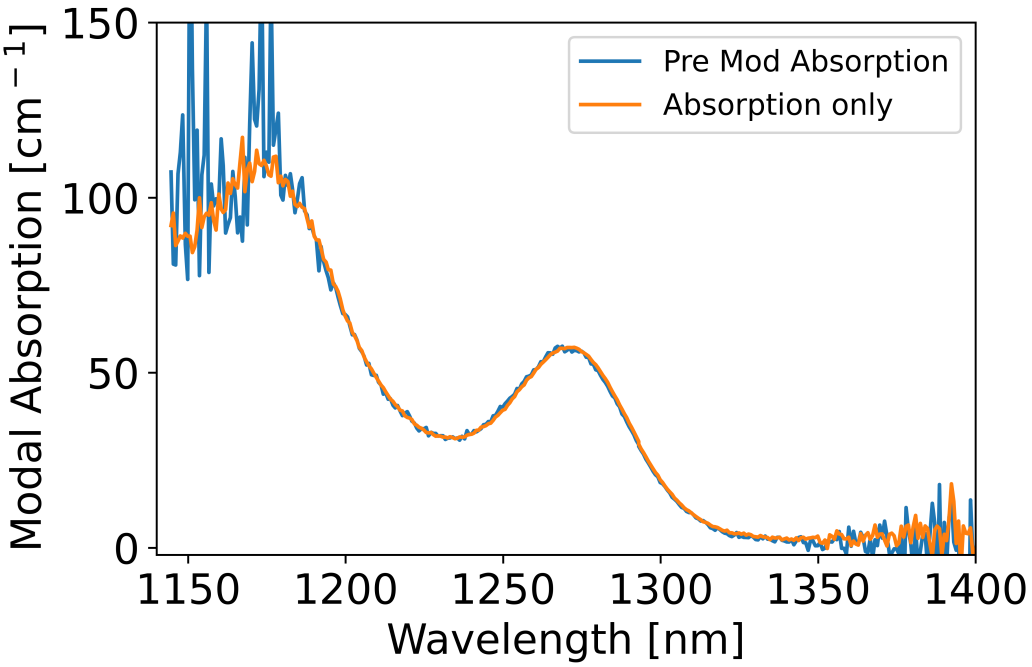


**Figure 3.6:** Average Absorption of InAs QD test sample 2 using standard SCM routine and absorption only modification.

Between 1250 to 1400nm both spectra are almost identical. Given that the absorption is not particularly large here any improvement in SNR would not have an effect on the overall result. However, the improvement to SNR in this region is very useful when comparing different sets of absorption data, particularly when dividing one set by another, as will be required in later chapters when considering modulator figure of merits. The improvement to the SNR reduces the issue of the absorption crossing over zero at the absorption edge tail, which can cause unwanted sharp steps when dividing two sets of absorption data together. For wavelengths below 1200nm it is clear the improved SNR has allowed for a more accurate absorption spectra to be calculated from the ASE from section 1 and 2. The modification now produces a far clearer 1st excited state absorption peak. This extra information is useful as it allows fitting schemes to work on a wider range of data, which in the case of looking at QD structures, can offer greater insight into the potential bimodal dot size distribution in the material [53].

### 3.3.3 Study of ASE intensity effect on maximum net gain

As explained previously in this chapter, the gain and absorption are calculated from the ASE spectra of various combinations of pumped sections. The camera that measures the ASE intensity needs to operate over a certain intensity range where the camera remains linear in responsivity. An investigation into whether a wider intensity range of the camera could be utilised was carried out with the aim of trying to increase the maximum possible net gain that could be reliably measured. By analysing Eq. 3.3 it is clear that if the difference between ASE(S1+S2) and ASE(S1) is increased then the net gain is subsequently larger.

The maximum net gain can be found by making ASE(S1+S2) and ASE(S1) equivalent to the maximum and minimum intensity values with which the camera remains linear. To obtain these maximum and minimum intensities, gain and absorption measurements were taken at a fixed current density, with the only change between each measurement being the amount of filtering of the ASE. This allowed different intensities to be picked up by the camera.

From this point on two values for intensity will be used to describe the ASE. First, the intensity of the ASE when doing routine alignment (at an integration time of 500 milliseconds) will be referred to as the filter intensity. This is because it is at the alignment stage that the filter wheel is adjusted to a certain intensity value to allow the measurement to start. The second intensity will be referred to as the measured intensity. This is the intensity of the ASE during measurement where the integration time is now much longer at 20 seconds.

Fig. 3.7 shows plots of the various ASE spectra obtained at different filter intensities for pumping of sections 1 and 2 separately. To determine the range of the camera, the ASE from sections 1 and 2 can be compared at a range of filter intensities. Fig. 3.8 shows the ratios between the two ASE spectra at each filter intensity at specific points at each spectrum. The ratios shown are between the ground state peaks of section 1 and 2, the ground and excited state peaks of section 1, and the ground state peak and the minimum of section 1. The ratios are quite constant throughout the filter intensity range, with the exception of the lowest filter intensity

of 400 counts where there is a constant deviation from the typical ratio. This indicates that the linearity of the camera being used ranges from filter intensities of approximately 450 to 700 counts. The kit prior to investigation typically operated at a filter intensity of 500, corresponding to a peak ASE measured intensity of roughly 1400 counts for an integration time of 20 seconds. The result suggests the potential of using a larger filter intensity whilst remaining within the linear range of the camera.

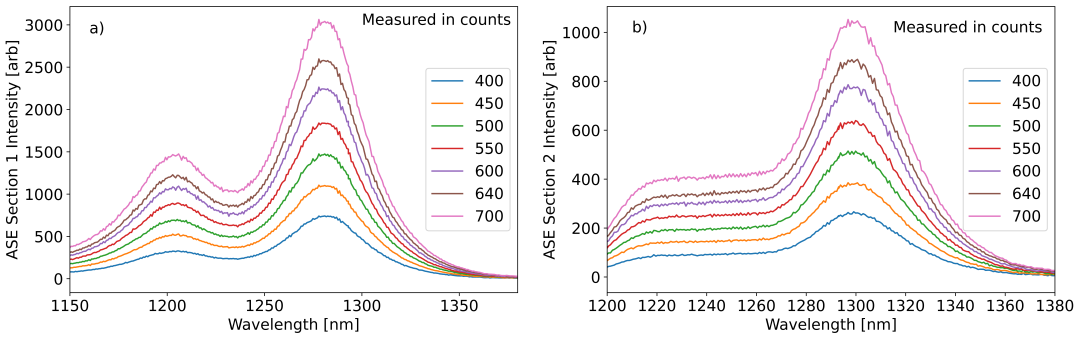


**Figure 3.7:** Plots of ASE spectra for different filter intensities for section 1 (a) and 2 (b). Intensity is measured in counts.

To ensure that the camera does not become saturated, which could lead to damaging the camera, a filter intensity of 620 counts was chosen to allow for a maximum ASE measured intensity of roughly 2500 counts. Using this new filter intensity, net gain spectra were taken at various currents on a device that had previously been characterised at a filter intensity of 500. The graph in Fig. 3.9 shows the comparison between the net gain spectra obtained at both filter intensities. At the lowest current there is almost no difference between the spectra, as the net gain is not near the reliable limit of either of the filter intensities.

At the next current there is a slight difference in peak gain between the two spectra, with the peak from the higher filter intensity being larger. Although this difference may be attributed to a small variation in alignment of the device, it is quite clear that at the largest current there is a noticeable difference between the net peak gain of the two filter intensities. For this particular current value, the net gain is close to the max reliable net gain value for a filter intensity of 500. As a result,

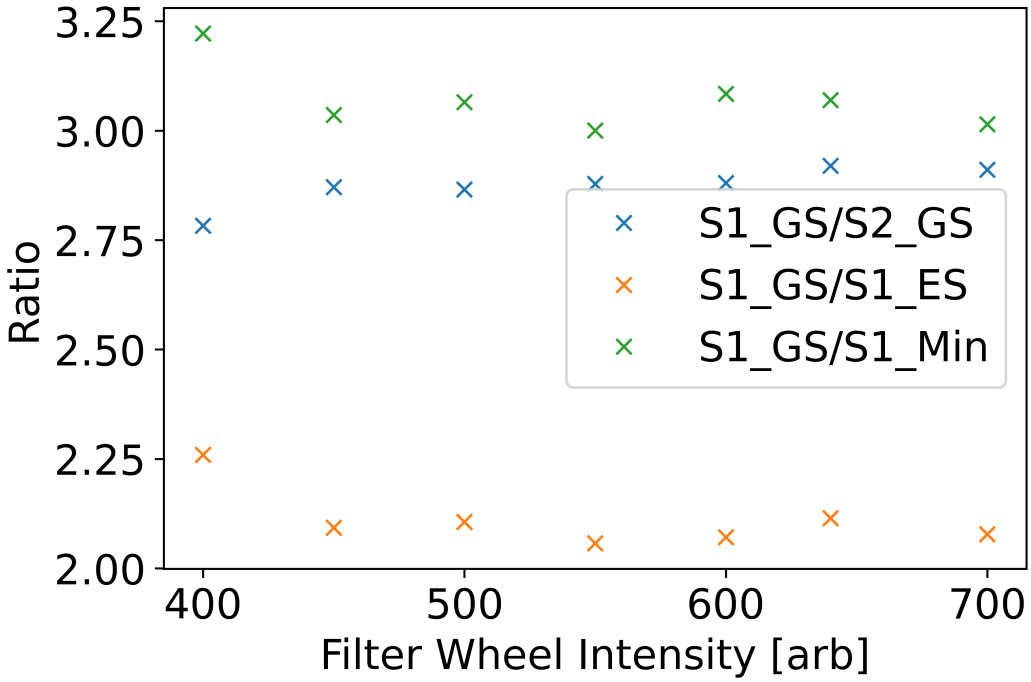


**Figure 3.8:** Ratios of various points between ASE of section 1 and 2. Ratios taken between ground state and excited state maximum of section 1, ground state maxima of section 1 and 2, and ground state maxima and minima of section 1.

there may have been some suppression of the measured net gain in the lower filter intensity measurement, which has then been resolved by increasing the maximum ASE count allowing for a more accurate net gain measurement to be made.

Despite the change in peak net gain at the largest measured current, the internal optical loss between both sets of measurements are similar and agree within 1-sigma error, along with the transparency point which is approximately at a wavelength of 1216nm for both measurement runs.

Additionally, and perhaps more important to the work of this thesis, the higher filter intensity can be used in conjunction with the absorption only mode to produce even better SNR absorption spectra. A development of Fig. 3.6 now showing absorption only mode spectra using a filter intensity of 600 counts is shown in Fig. 3.10. It can be seen that using the higher filter intensity has further reduced noise at the extremities of the spectra, with less fluctuation in the first excited peak and absorption edge. The combined use of the absorption only mode and higher filter intensity is therefore considered the optimal approach to measuring the absorption

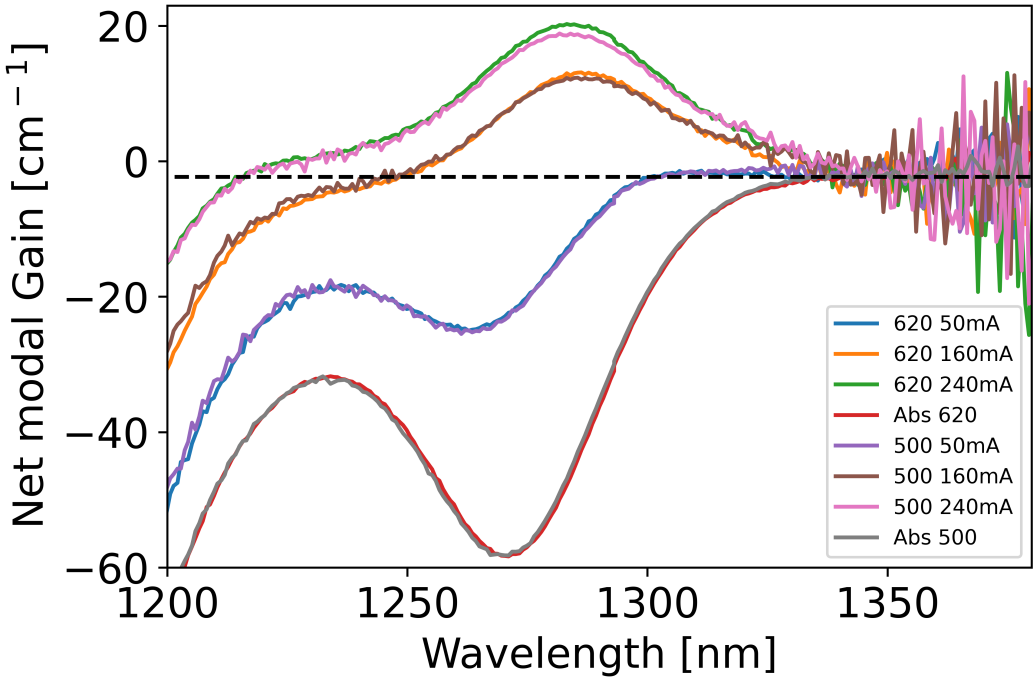


**Figure 3.9:** Comparison of gain spectra of same InAs QD device using filter intensities of 500 and 620 over a range of applied currents. Absorption shown as negative gain.

spectra in this work, and therefore has been used in the proceeding chapter to study the QCSE of the QD devices.

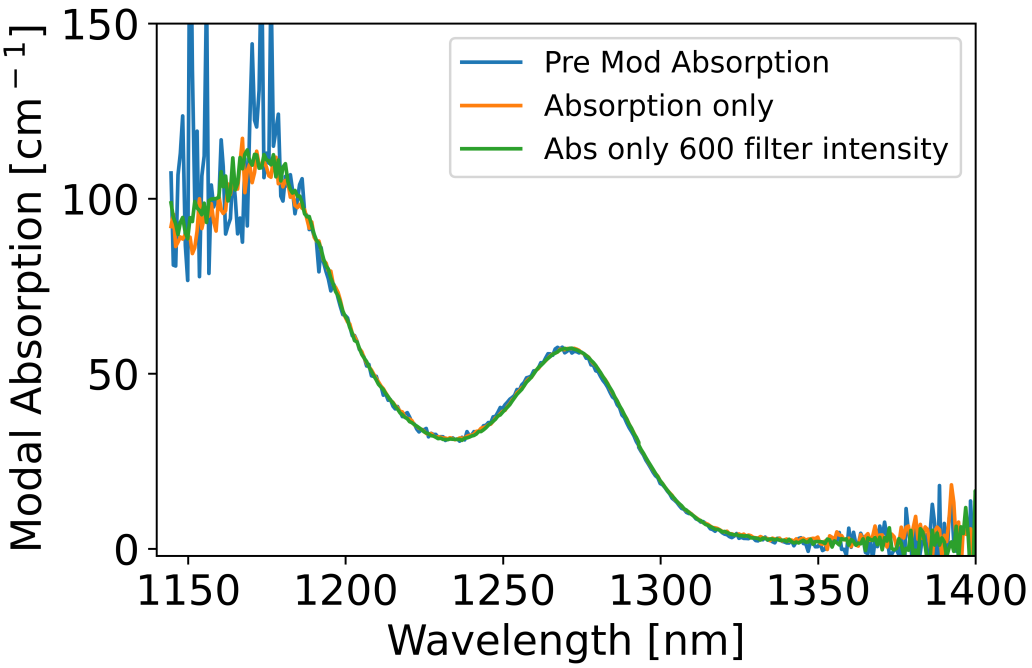


**Figure 3.10:** Development of Fig. 3.6 now showing absorption only mode spectra using a filter intensity of 600 counts.

## 3.4 Quantum dot model implementation

Although measurements are a crucial aspect of understanding device level physics, being able to have a simulation-based model enables the opportunity to further modify a structure to understand better potential changes that can be made to improve the device performance. To do this, confidence in the model's accuracy is first required. This will be carried out by comparing simulation with measured results to determine if there is good agreement between the two.

To perform the simulations self-consistent Schrödinger-Poisson solvers are implemented using NextNano software [54]. Generally speaking this involves solving Poisson's equation from an initially-input charge distribution, which outputs an electrostatic potential. This potential can then be used in the Schrödinger equation, which in turn effects and updates the charge distribution. This process is iterated on until the discrepancy between neighbouring iterative steps falls below a predetermined error threshold.

Before any comparisons can be made between simulation and measurement,

modifications to the QD materials to be used need to be carried out. In order to maintain efficiency, 1D simulations will be used. Ideally 3D simulations would be carried out for QD devices, given their unique confinement properties. However, such simulations would be exceedingly computationally expensive and so approximations using 1D must be implemented. To try and achieve QD-like behaviour in the 1D simulations, approaches from the work of Benjamin Maglio [55] are implemented and adapted. First, it has been observed that InAs QDs have very small heavy-hole state separation, on the order of 10meV [56], as well as conduction state separation up to 80meV. To achieve this, modifications to the effective mass tensor in NextNano are made. The 1D simulation effectively treats the materials like a 1D QW. As such the required modified effective mass for a given energy level separation can be approximated using a rearranged solution to the infinite square well, given by equation

$$\Delta E = \frac{\Delta(n^2)\pi^2\hbar^2}{2m^*L^2}, \tag{3.8}$$

where $\Delta E$ is the predetermined or desired energy state separation, $\Delta(n^2)$ represents the difference in the square of energy states, $L$ is the "width" or equivalently height of the well, $\hbar$ is Planck's constant and $m^*$ is the effective mass of the electron or hole.

Additionally, the dot density can be approximated using a similar approach. The carrier density can be determined by integrating the product of the density of states of the well with the Fermi distribution [19]. For the case of the QW this gives equation

$$p = \frac{m^*k_BT}{\pi\hbar^2} ln\left(1+\exp(\frac{E_{Fv}-E_v}{k_BT})\right), \tag{3.9}$$

where $p$ is the hole carrier density, $E_{Fv}$ is the quasi valence Fermi level, and $E_v$ is the valence state energy.

The band-structure of the InAs QD is shown in Fig. 3.11, where the afore-

mentioned state separations in the dot have been achieved using the effective mass modifications above. Additionally, it can be seen that the dots have a parabolic-like shape. This has been achieved by parabolically changing the material from InGaAs to InAs in the dot. This emphasises the diffusion of the InGaAs wetting layer into the InAs QD, but also encourages roughly consistent state separations in both conduction and valence bands, which has been observed in InAs QD structures [19]. To further verify whether the modifications to the 1D model are appropriate, direct comparison to experimental data is required. This comparison is conducted in chapter 5.

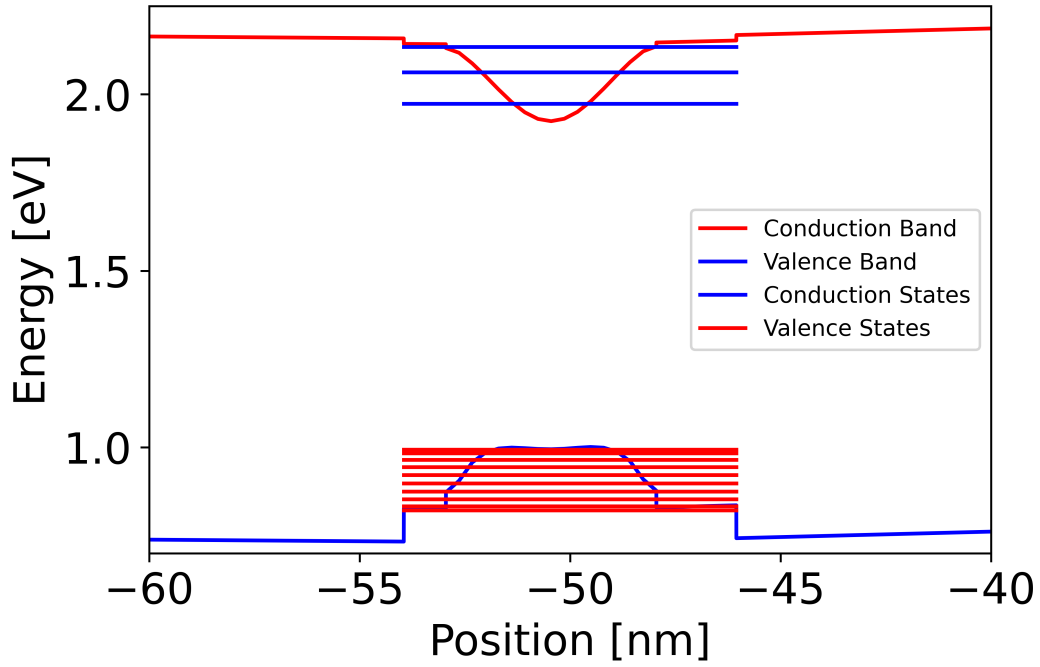


**Figure 3.11:** Band structure of InAs QD material in NextNano. Conduction and valence states are also shown to highlight the effect of modifying effective mass of QD material.

## 3.5 Chapter summary

This chapter focused on the measurement techniques and simulation software that will be mainly used in the remainder of this work. A detailed outline of the segmented contact method was presented. This involved the overall measurement procedure, along with highlighting the key areas of the measurement that need to be

carefully considered to help ensure accurate results. A review of the fundamental modifications to the segmented contact measurement setup were presented. This looked into enabling an absorption-only measurement regime to enable higher SNR QCSE spectra to be calculated, the ability to measure I-V traces directly on the measurement setup to enable both a swifter measurement process as well as allow for I-V traces to be measured under reverse bias. The optimum camera intensity was also determined to ensure as high a SNR was achieved for both gain and absorption measurements using the segmented contact method whilst ensuring the camera was still within its linear response range.

Finally, an overview of the simulation model that was implemented in NextNano was discussed. The 1D implementation of the QD p-i-n diodes meant certain approximations had to be made. To encourage QD-like behaviour in the simulations, parabolic potentials were induced in the dot regions to encourage equal spacing of energy levels. Additionally, modifications to the effective mass tensors were implemented to ensure correct state spacing and carrier density compared to previously measured InAs QD stacks. As with previous iterations of such a model, the modifications showed good agreement with expected state spacing.

# Chapter 4

# Measurement of quantum confined Stark effect in InAs quantum dots

## 4.1 Introduction

The quantum-confined Stark effect (QCSE) is widely used in several electro-absorption modulators (EAMs) and it is present in QD systems. There are numerous advantages to utilizing this effect, including greater bandwidth when compared to the plasma dispersion effect [30] exploited in current silicon modulators. Additionally, the QCSE allows a shorter modulator length and reduced electrical power consumption [57]. A more complete description of the QCSE can be found in section 2.4 in chapter 2.

The QCSE is present in both QWs and QDs [32; 43; 58; 41; 28; 44; 42; 59; 60]. One of the commonly accepted advantages of QD devices, as discussed in chapter 2, is that they are more resilient than QW devices when growing them over silicon as the QWs are more strongly effected by defects arising from the material lattice mismatch and different thermal expansion coefficients. In the case of modulator devices specifically, defects in the semiconductor materials lead to uneven static electric fields across QW active regions through the onset of leakage current as demonstrated in [61; 62]. Furthermore, the non-uniform static electric field leads to a non-uniform Stark shift, broadening the QCSE excitonic peak and reducing the maximum absorption, leading to smaller extinction ratios (ERs) [61; 62].

On the other hand, QDs offer the prospect of significant electro-optic coefficients and steeper absorption edges due to their confined nature [10]. For example, the work in [32] demonstrated that the QCSE in QDs can achieve comparable ERs to QWs despite having a lower density of states by two orders of magnitude. This result is possible due to the modified density of states in dots. In principle the delta-function density of states in dots would lead to very sharp ERs compared to QWs. Homogeneous and inhomogeneous broadening in dots will of course lead to smaller ERs than the assumption of a delta-function-like spectra, but the results suggested here nevertheless show the benefits of using dots are still present. This result suggests the potential for high-performance EAMs using QDs.

Despite several recent measurements of the QCSE in QDs [32; 43; 41; 42], the QD stacks used in those works are very similar or identical to the QD laser, and the stacks were not optimized to improve the QCSE for modulation.

Given the vastly more mature research into QW stacks, this is generally not the case for QW modulators, which have been heavily optimized to improve the QCSE for modulation. One successful method is the incorporation of barrier doping as shown in [28]. The study suggested that incorporating a modulation-doped superlattice in a multi-QW structure can lead to equivalent ERs while reducing the applied voltage by almost half. The enhancement was attributed to the modification of the potential by the doping profile to create higher polarizability of the electron and hole wavefunctions. This improvement would lead to more efficient QW modulators with reduced power consumption [40].

The same technique has been applied to the QD laser by doping the QD barriers and offering better performance as described in [63]. Nevertheless, the method has not been investigated for modulation and, to the best of our knowledge, there has been no report on the influence of QD barrier doping on the QCSE.

In this chapter, the influence of p-doping the QD barriers on the QCSE and comparing it with unintentionally doped (UID) barriers with temperatures between $-73$ to $100\,^{\circ}C$ is investigated. Gain measurements are also carried out on the stacks to determine the plausibility of utilising the same epistructure to achieve an in-

tegrated laser-modulator device. In order to quantify the performance of the QD stacks as prospective modulators, there are three main performance metrics usually considered. These are the operating voltage swing required, the change in absorption (extinction ratio) for the given voltage swing, and the modulation bandwidth. This chapter will focus on looking at the voltage swing as well as the extinction ratio (ER) performance of the stacks. From the measurements of the QCSE the stacks were compared for modulation using the industry-standard figure of merit (*FoM*), defined as the ratio of the change in absorption ($\Delta\alpha$) to the loss at $1V$ ($\alpha(1V)$), *FoM* = $\Delta\alpha/\alpha(1V)$. The measurements show that the p-doping in the QD barriers offers up to 3x larger maximum *FoM* over the spectrum between $-73$ to $100\,^{\circ}C$.

## 4.2 QCSE using p-doped and unintentionally doped quantum dot barriers

This work measured the QCSE in the stacks shown in Table 4.1 and compared as potential modulators. The only difference between the stacks is that the QD barrier is P-doped (PD) or left UID; the barrier is highlighted in bold in Table 4.1. Additionally, we compared the performance from $-73$ to $100\,^{\circ}C$ by using a heater and a heat sink, or a microstat for the low temperature measurements.

The stacks in Table 4.1 were grown using molecular beam epitaxy by UCL on an n-doped GaAs substrate. The p-doping concentration in the QD barrier of $5 \cdot 10^{17}\,cm^{-3}$ is equivalent to 10 holes per dot. In both stacks, the InAs QD areal density is $5 \cdot 10^{10}\,cm^{-2}$). The QD active region stack consists of 7 dot-in-a-well layers with a total core thickness of 350 nm. Finally, the waveguide core has an $Al_{0.4}Ga_{0.6}As$ cladding layer above and below with a thickness of 1400 nm. The structure contains a top highly doped GaAs layer and bottom GaAs for making electrical contacts. To handle strain between GaAs and $Al_{0.4}Ga_{0.6}As$ and reduce device voltage through limiting the effect of band bending, there are 10 repetitions of 5 nm GaAs/$Al_{0.4}Ga_{0.6}As$.

The QCSE was measured using the segmented contact method [12] using the structure shown in Fig. 4.1. Two identical structures were fabricated with the stacks

shown in Table 4.1. Each section of the multisection devices have dimensions of $100\mu m \times 300\ \mu m$. The top layer in the stack is doped over $1 \cdot 10^{19}\, cm^{-3}$ to guarantee Ohmic contacts with gold. In order to observe the QCSE from the measurements, the front section of the multisection device has a reverse bias applied to it when the adjacent section is pumped. As explained in section 3.2 of chapter 3, the absorption of the front section can be calculated from equation 3.4. As the front section has a reverse bias applied to it, the absorption spectra should shift due to the QCSE.

**Table 4.1:** Layer structure for QD stacks. The only difference between the stacks is the QD barrier doping highlighted in bold, which is PD ($5 \cdot 10^{17}\, cm^{-3}$) or left UID. P stands for PD, and N for n-doped. The column Repetitions represents the number of times a set of layers is repeated in the stack, e.g., there are $7\times$ repetitions of the QD active region [64].

| Material | Thickness | Type | Repetitions |
|---|---|---|---|
| GaAs | $300\,nm$ | P($1 \cdot 10^{19}\, cm^{-3}$) | – |
| GaAs/AlGaAs | $5\,nm$ | P($5 \cdot 10^{17}\, cm^{-3}$) | $\times 10$ |
| AlGaAs | $1400\,nm$ | P($2 \cdot 10^{17}\, cm^{-3}$) | – |
| AlGaAs | $30\,nm$ | UID | – |
| GaAs/AlGaAs | $2\,nm$ | UID | $\times 12$ |
| **GaAs** | $17.5\,nm$ | UID | |
| **GaAs** | $10\,nm$ | **P($5 \cdot 10^{17}\, cm^{-3}$)/UID** | |
| **GaAs** | $10\,nm$ | UID | |
| **GaAs** | $5\,nm$ | UID | |
| **InGaAs** | $5\,nm$ | UID | |
| **InAs QD** | $3\,ML$ | UID | $\times 7$ |
| **InGaAs** | $2\,nm$ | UID | |
| GaAs | $42.5\,nm$ | UID | – |
| GaAs/AlGaAs | $2\,nm$ | UID | $\times 12$ |
| AlGaAs | $30\,nm$ | UID | – |
| AlGaAs | $1400\,nm$ | N($2 \cdot 10^{18}\, cm^{-3}$) | – |
| GaAs/AlGaAs | $5\,nm$ | N($2 \cdot 10^{18}\, cm^{-3}$) | $\times 10$ |
| GaAs | $200\,nm$ | N($2 \cdot 10^{18}\, cm^{-3}$) | – |

Gaps of $8\mu m$ in length and 700 nm in depth were etched in the top layers to isolate the contacts electrically. During the measurement, the leakage current was compensated as the resistance between contacts and the leakage current change with temperature from $-73$ to $100\,^{\circ}C$. Inter-contact resistance was typically found to be around $150 - 300\Omega$, with the PD samples generally having large leakge current.

The measurements of the QCSE using the segmented contact method are shown in Fig. 4.2(a) for the stack with PD QD barriers and Fig. 4.2(b) for the stack with UID QD barriers. The ground state absorption peak of the PD stack increases slightly with increasing temperature, as shown in Fig. 4.2(a). This be-

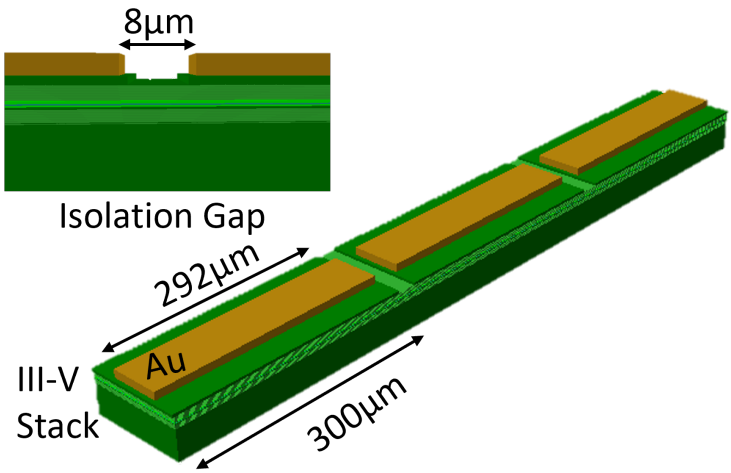


**Figure 4.1:** Schematic of multisection device used to measure the QD in the stacks of Table 4.1.

haviour is attributed to the redistribution of carriers in the ground valence states as the temperature increases. The redistribution leads to a greater occupancy probability for electrons in the ground QD valence states, which increases photon absorption at the ground state transition energy. Conversely, the ground state absorption peak of the stack with UID barriers in Fig. 4.2(b) decreases with increasing temperature as expected. The same trend was measured in [65].

Regarding the absorption spectra shown in Fig. 4.2(a), the PD QD stack exhibits a quenched absorption peak at the QD ground-state wavelength. The ground-state absorption peak suppression is attributed to the injection of holes in the QD ground valence state from the PD barrier. The holes inhibit the excitation of electrons from the ground valence state to the ground conduction state and therefore inhibit photon absorption. In contrast, the stack with UID barriers has the expected ground-state absorption peak, as shown in Fig. 4.2(b).

Fig. 4.3(a) and Fig. 4.3(b) show the change in absorption $\Delta\alpha$ for a reverse bias voltage swing of 9V and the absorption $\alpha(1V)$ at a reverse bias of 1V for 21 $^{\circ}C$, 50 $^{\circ}C$, 75 $^{\circ}C$, and 100 $^{\circ}C$ for PD and UID QDs respectively. The pre-biased value of 1V is used to mitigate the modulator's capacitance penalty as in [43].

When comparing the $\Delta\alpha$ of both stacks in Fig. 4.3(a) and (b), there is only a slight decrease in $\Delta\alpha$ with temperature. This will lead to a modulator with a

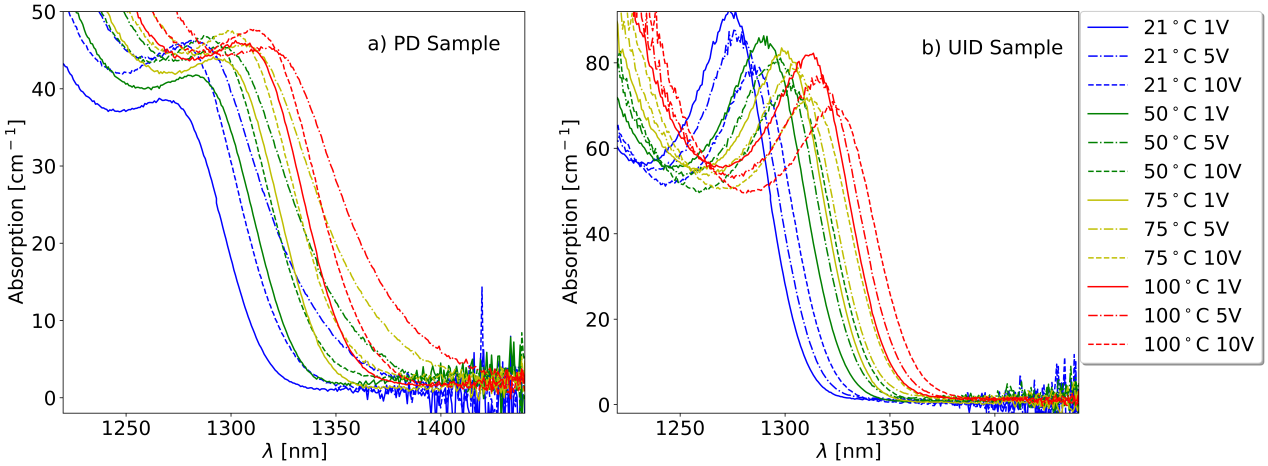


**Figure 4.2:** Measured absorption spectra for PD (a) and UID (b) multi-section devices vs temperature.

stable ER from 21 $°C$ to 100 $°C$ for both stacks. Additionally, the stack with UID QD barriers has the largest $\Delta\alpha$ value of around 12 $dBmm^{-1}$, which will lead to a larger ER. Nevertheless, it also has a larger material absorption $\alpha(1V)$ at the same wavelength, which will lead to a larger insertion loss (IL).

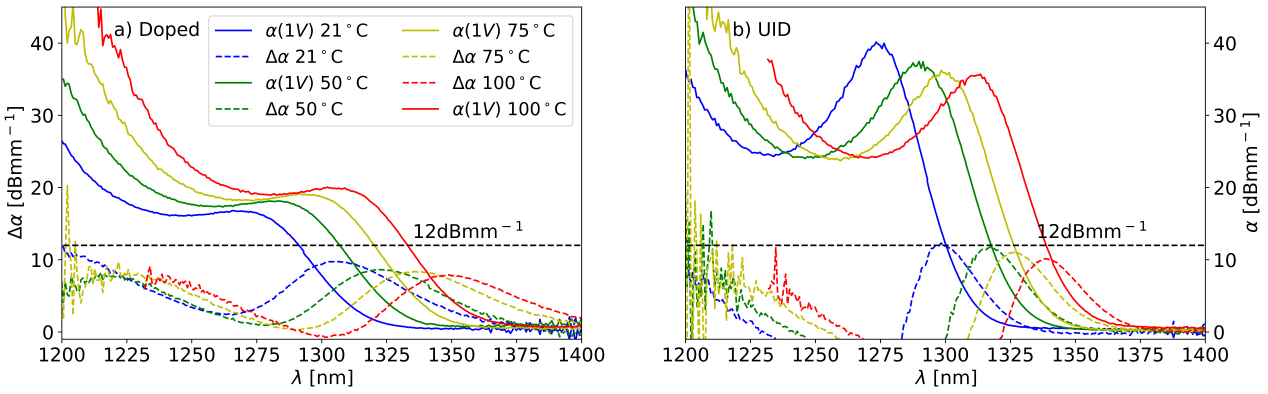


**Figure 4.3:** $\Delta\alpha$ (dotted lines) and $\alpha(1V)$ (solid lines) for PD (a) and UID (b) multi-section devices vs temperature.$\Delta\alpha$ corresponds to a change in absorption between $10V$ and $1V$.

To investigate the trends further, the QCSE ground-state absorption peak for the stack with PD and UID QD barriers as a function of reverse bias was studied in Fig. 4.4(a) for three temperatures $-73\,°C$, $21\,°C$, and $100\,°C$. Additionally, the absorption peak wavelength shift is represented in Fig. 4.4(b). The ground-state absorption peak wavelength is the transition wavelength at the peak of the

absorption spectra before approaching the band edge.

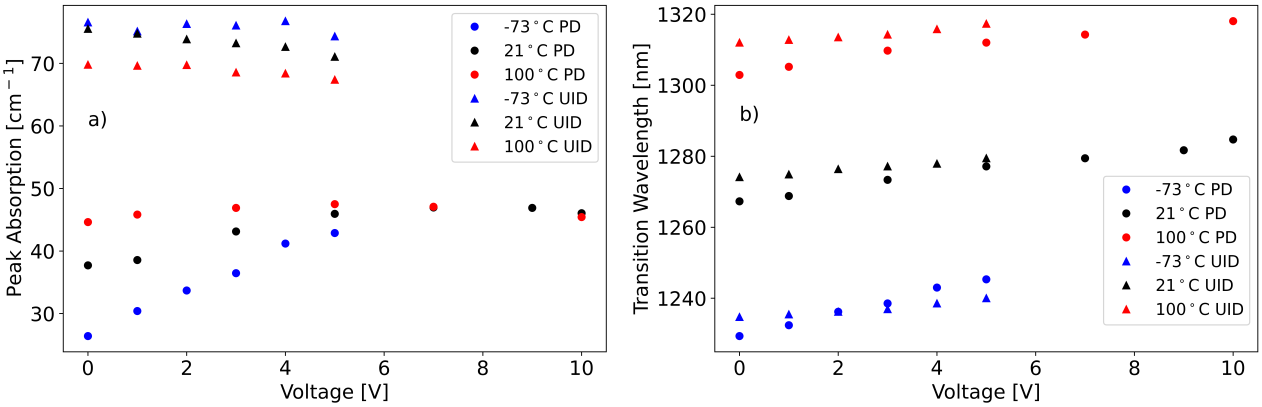


**Figure 4.4:** The change in ground state absorption peak (a) and wavelength (b) between $-73\,^{\circ}C$ and $100\,^{\circ}C$ for the doped and UID layers.

As shown in Fig. 4.4(a), the stack with UID ground-state absorption peak generally decreases with increasing reverse bias at $-73\,^{\circ}C$, $21\,^{\circ}C$, and $100\,^{\circ}C$. As the reverse bias increases, the increased static electric field pulls the electrons and holes in opposite directions inside the QDs. This phenomenon leads to a reduction in the overlap between the carriers' wavefunctions and contributes to reducing the photon absorption [66].

However, the stack with PD QD barriers has different behaviour. Below moderate reverse bias (less than 5.5V), the holes in the ground valence state inhibit the photon absorption. As the reverse bias increases, the built-in static electric field starts to deplete the holes from the ground valence state, allowing photons to be absorbed and excite electrons from the valence ground-state to the bottom of the conduction ground-state, thus increasing absorption at the ground state transition [67]. For voltages below 4V, the ground-state absorption peak is smaller at $-73\,^{\circ}C$ rather than at $100\,^{\circ}C$ due to more electrons being thermally excited to the valence ground-state at higher temperatures. A simple band diagram illustrating the thermal redistribution of carriers in the valence states is given in Fig. 4.5. The figure illustrates the distributions of holes at low (zero) temperature and at a temperature $T > 0K$. Given that in InAs QDs the energy separation between valence states is typically found to be on the order of $10meV$ [56], thermal energy present will have a significant effect on carrier redistribution once at higher ambient temperatures. For

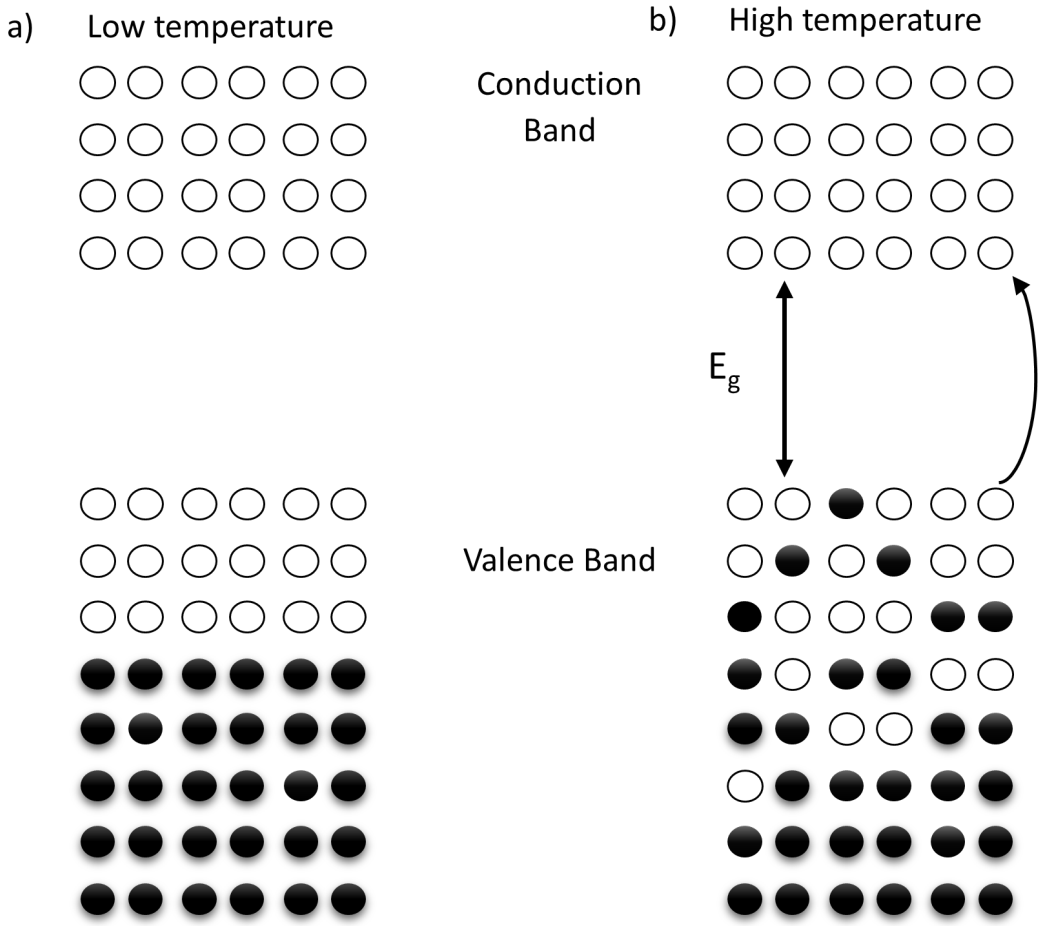


**Figure 4.5:** Simple band diagram highlighting effect of thermal redistribution of electrons in the valence band at low (a) and high (b) temperatures. At low temperatures, the top valence states are filled with holes (white circles). As a reverse bias voltage is applied so the holes in these states are depleted, leading to a more pronounced carrier-blocking effect. At higher temperatures, the thermal energy is enough such that electrons (black circles) can be excited to higher valence states. Subsequently, as a reverse bias is applied, the carrier-blocking effect is weakened due to the increased electron population in the top valence states as a result of the thermal redistribution.

this reason, the rate of change in ground-state absorption peak at $-73\,^{\circ}C$ is more significant between 0V and 5.5V than at $100\,^{\circ}C$.

The ground-state absorption peak will increase with a reverse bias for all temperatures until all holes are entirely depleted from the valence ground-state. As shown in Fig. 4.4(a), all holes are depleted around 5.5V, and the absorption peak starts to decrease beyond 5.5V for the same reason as the stack with UID barriers. The built-in static electric field pulls the carriers in opposite directions reducing the

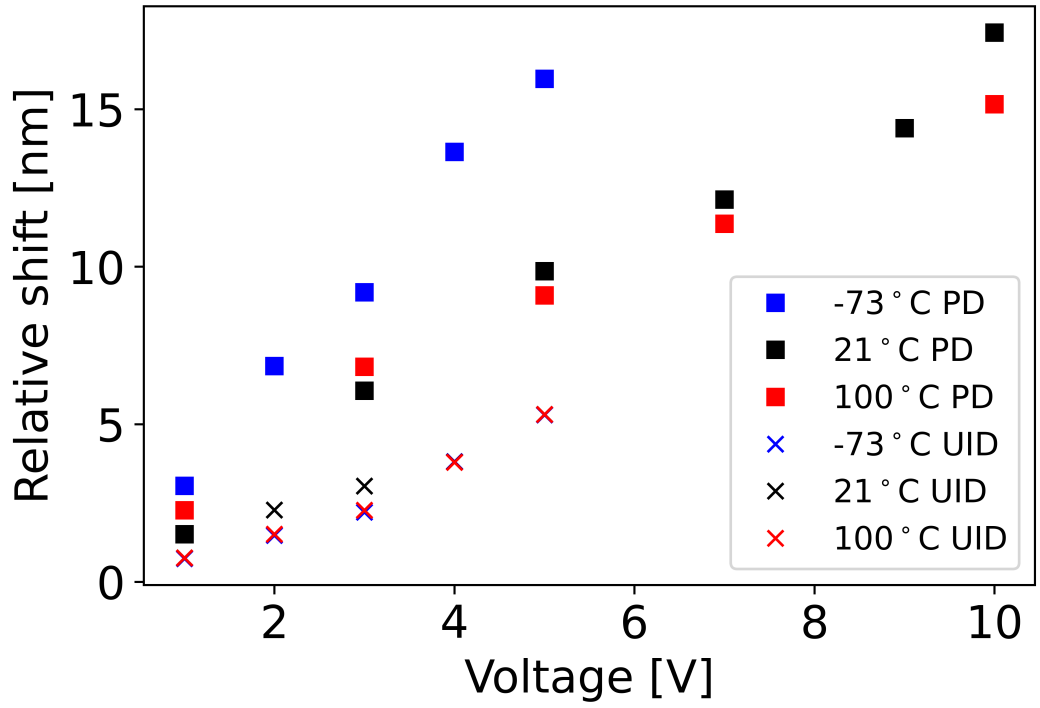


**Figure 4.6:** Relative shift of the PD (squares) and UID (crosses) with respect to the ground state wavelength at $1V$ at $-73\,^{\circ}C$ (blue), $21\,^{\circ}C$ (black) and $100\,^{\circ}C$ (red)].

carrier's wavefunction overlap and the photon absorption.

The wavelength shift of the ground-state absorption peak is shown in Fig. 4.4(b). The stack with doped barriers shows a more significant shift than the stack with UID barriers. For reverse biases between 1V and 5V, red-shifts at $-73\,^{\circ}C$ are 13nm for the stack with doped barriers and 5nm for the stack with UID barriers. The shift difference is more considerable at $-73\,^{\circ}C$, and it decreases with increasing temperature. This is clearly illustrated in Fig. 4.6 which highlights the relative shift of the PD and UID with respect to the ground state wavelength at $0V$ at $-73\,^{\circ}C$, $21\,^{\circ}C$ and $100\,^{\circ}C$. The figure shows the rate of change of red-shift decreases from approximately $3\text{nm}V^{-1}$ to $1.4\text{nm}V^{-1}$ for the PD stack between $-73\,^{\circ}C$ and $100\,^{\circ}C$. On the other hand, the UID stack's rate of change remains largely the same at all temperatures, at a value of approximately $1.1\text{nm}V^{-1}$.

Both stacks show the Stark shift present in the QCSE. Nevertheless, the stack with doped barriers has additional contributions to the red-shift. One comes from the QD layers having a larger static electric field strength when compared with the

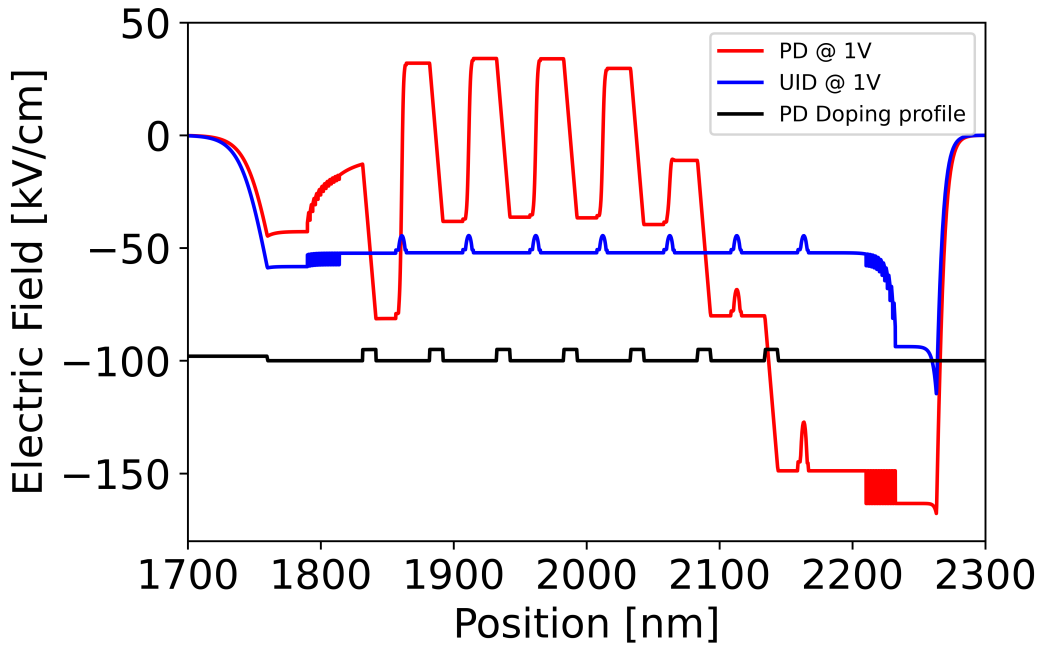


**Figure 4.7:** Static electric field distribution across the QD active region for the stacks with doped (red line) and UID (blue line) barriers for a 1V reverse bias at 21 °*C*. The black line shows the position of the doped barriers, and the QDs are between them. The static electric field was numerically calculated using NextNano [54].

stack with UID barriers. The larger static electric field is due to the QD layers being surrounded by doped GaAs layers. The static electric field distribution across the QD active region for both stacks is shown in Fig. 4.7 and it was calculated using NextNano [54]. The black line at the bottom of the figure indicates the position of the doped barriers with respect to the dot layers. Figure 4.7 highlights the significantly stronger field across the QDs of the stack with doped barriers. Therefore, the larger applied electric field would cause a more substantial red-shift.

The other shift contribution originates from the removal of holes from the highest valence states as the static electric field increases with reverse bias. As holes are depleted from the top of the valence states, longer wavelength (lower energy) transitions are allowed. Subsequently, as the temperature increases, thermal redistribution of carriers within the valence states would weaken this effect. This is considered the main reason as to why the rate of red-shift with voltage decreases with temperature as shown in Fig. 4.6.

In order to determine which stack design is better for modulation, the stacks

were compared using the $FoM = \Delta\alpha/\alpha(1V)$. The $FoM$ maximises $\Delta\alpha$ to have a large ER and minimises $\alpha(1V)$ to reduce the IL. The $FoM$ is shown in Fig. 4.8(a) for a 4V-swing and in Fig. 4.8(b) for a 9V-swing. As shown in Fig. 4.8, the stack with PD QD barriers outperforms the stack with UID barriers offering up to $3\times$ enhancement in the $FoM$ from $-73\,^{\circ}C$ to $100\,^{\circ}C$.

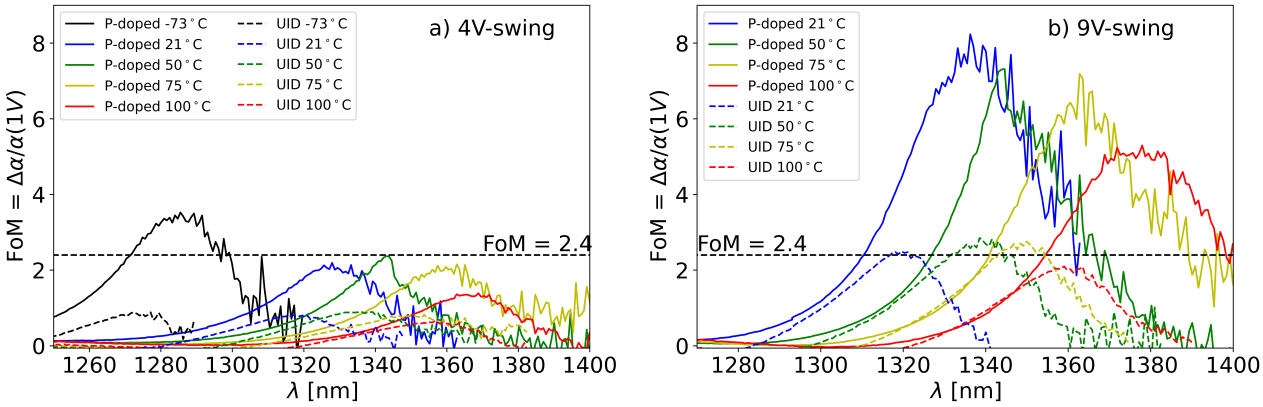


**Figure 4.8:** $FoM$ for a $4V$-swing (a) and $9V$-swing (b) for both doped and UID QD barrier vs temperature.

Several factors explain the better performance of the stack with doped QD barriers. As shown in Fig. 4.3, the $\Delta\alpha$ of the stack with UID barriers is around $12\,dBmm^{-1}$, and it is slightly larger than the stack with doped barriers. Nevertheless, the $\alpha(1V)$ is more significant in the stack with UID barriers at the same wavelength. In this comparison, only the material absorption contribution to the insertion loss (IL) is considered. As both PD and UID have similar internal optical losses at the band edge of approximately $1\,cm^{-1}$, the IL difference between the PD and UID will come down to the shape of the respective absorption tails.

Additionally, the extra red-shift in the stack with doped barriers shifts away the maximum $\Delta\alpha$ from the absorbing edge of the absorption spectrum $\alpha(1V)$ represented in Fig. 4.3(a) offering a better trade-off $\Delta\alpha/\alpha(1V)$). Overall, the $FoM$ is better for the stack with doped barriers when considering all factors.

To explain the results in Fig. 4.8(a) further, the $FoM$ of the stack with UID barriers is below $\sim 0.8$ from $-73\,^{\circ}C$ to $100\,^{\circ}C$ for a 4 V-swing. In contrast to this, the $FoM$ of the stack with doped barriers is $\sim 4$ at $-73\,^{\circ}C$ and it is around $\sim 2.4$ from $21\,^{\circ}C$ to $100\,^{\circ}C$. Consequently, for a 4V-swing the $FoM$ of the stack with

doped barriers is $\sim 3\times$ larger than the stack with UID barriers.

Considering the results for a 9V-swing shown in Fig. 4.8(b), the maximum *FoM* of the stack with UID barriers is around 2.4 from 21 °*C* to 100 °*C*. However, the maximum *FoM* for the stack with doped barriers starts at $\sim 8$ at 21 °*C* and degrades to $\sim 5$ at 100 °*C*. Consequently, the *FoM* of the stack with doped barriers is at least $\sim 3\times$ (at 100 °*C*) larger than the stack with UID barriers. Finally, the *FoM* = 2.4 of the stack with UID barriers at 9V-swing is approximately the same as the stack with doped barriers with a 4V-swing. This result implies that a modulator using the stack with doped barriers may need 5V less driving voltage which would significantly reduce power consumption.

### 4.2.1 Prospective device lengths based on *FoM* values

**Table 4.2:** PD and UID Modulator Lengths based off *FoM*

| PD | Voltage Swing [V] | ER [dB $mm^{-1}$] | IL [dB $mm^{-1}$] | Length [mm] | Wavelength [nm] |
|---|---|---|---|---|---|
| 21 °*C* | 9 | 8.94 | 2.54 | 2.23 | 1315.8 |
| | 6[1] | 6.48 | 3.17 | 3.08 | 1312.8 |
| | 4[1] | 2.89 | 1.54 | 6.9 | 1321 |
| 50 °*C* | 9 | 8.04 | 2.34 | 2.48 | 1331.7 |
| | 6[1] | 5.31 | 2.68 | 3.76 | 1330.2 |
| | 4[1] | 2.8 | 1.47 | 7.1 | 1337 |
| 75 °*C* | 9 | 7.65 | 2.33 | 2.62 | 1345.3 |
| | 6[1] | 4.84 | 2.49 | 4.13 | 1343.8 |
| | 4[1] | 2.64 | 1.31 | 7.59 | 1351.4 |
| 100 °*C* | 9 | 7.09 | 2.17 | 2.82 | 1359.8 |
| | 6[1] | 4.3 | 2.17 | 4.65 | 1359.8 |
| | 4[1] | – | – | – | – |
| −73 °*C* | 4[2] | 6.98 | 2.45 | 2.86 | 1274.9 |
| UID | | | | | |
| 21 °*C* | 9[1] | 7.55 | 3.9 | 2.65 | 1311.2 |
| 50 °*C* | 9[1] | 7.81 | 4.08 | 2.56 | 1328.7 |
| 75 °*C* | 9[1] | 7.28 | 3.76 | 2.75 | 1338.5 |
| 100 °*C* | 9[1] | 4.97 | 2.54 | 4 | 1355.2 |

[1] Values found for ER/IL = 20dB/10dB. [2] Value found for ER/IL = 20dB/7dB

Although the *FoM* by itself gives a clear indication of the potential performance of the QD material as EAM's, further insight is required in order to better

determine performance of a fully realised device. In order to ensure as high an integration density as possible in a prospective PIC, device length should be minimised. In table 4.2, such values are given for the PD QD measurements for various temperatures and voltage swings. In order to determine the length of a prospective device, an ER and IL need to be set such that the device achieves a sufficiently large ER and low IL. Performance of approximately 20dB ER and 6 dB IL has been considered for the PD stack. These values would be equivalent to a *FoM* of roughly 3, which has been demonstrated to be readily achievable for larger voltage swings in the PD samples, as shown in Fig. 4.8.

Despite the performance benchmark defined above being attainable in the PD sample, quick inspection and comparison between Fig. 4.8 and Fig. 4.3 indicate that using peak *FoM* device performance would lead to lengths that are very long. This is because at the peak *FoM*, the values for both $\Delta\alpha$ and $\alpha(1V)$ are small. Therefore, an "optimum" *FoM* is found that maximises the *FoM* whilst keeping overall device length as short as possible. This optimum *FoM* is taken to at the wavelength that first achieves a *FoM* equivalent to 20dB ER over 6 dB IL. The subsequent lengths for the PD sample shown in Table 4.2 highlight that, using a $9V$-swing (between 10V and 1V) the desired ratio of 20dB/6dB could be achieved whilst remaining below a device length of 3mm.

To determine the drop-off in performance in the PD sample for lower voltage swings, Table 4.2 also includes equivalent analysis at $6V$-swing and $4V$-swings. As noted in the table, performance of 20dB/6dB is not actually attainable at these voltage swings, and has been adjusted to 20dB/10dB to enable some comparison. The results clearly show the significantly longer devices that would be required to hit the specified performance benchmark, and therefore the need to use larger voltage swings in real applications.

Although the use of higher voltage swings are not currently achievable in CMOS circuitry, the results do indicate the potential performance that can be achieved, provided the stack is optimised for lower voltage swing-operation. Such optmisations could be achieved through reducing the overall stack thickness by re-

ducing thickness of buffer layers in the active region. Nevertheless, low-temperature operation in PD stacks is far more readily attainable even at lower voltage swings. Results at $-73\,^{\circ}C$ indicate that even using a $4V$-swing, almost equivalent performance is attained to higher temperature $9V$-swing results whilst maintaining a device length below 3mm. This is another clear demonstration of the carrier-blocking effect being more clearly present at lower temperatures.

Finally despite the fact that the UID sample, even at $9V$-swing, does not produce the desired ER/IL of roughly 3, it is included for the same performance parameters used for $6V$-swing and $4V$-swing PD measurements. Unlike the lower voltage-swing PD results, the UID can produce sub-3mm lengths at least up to $75\,^{\circ}C$. The values for optimum *FoM* in Table 4.2 are considered to give a clearer reflection of real device performance compared to simply looking at the raw maximum *FoM*, as the device length is taken into account in the former metric. Nevertheless, as with looking at raw *FoM* performance, the PD sample clearly outperforms the UID sample, achieving better "optimum" *FoM* values whilst requiring shorter devices to achieve said performance.

## 4.3 Comparison with state of the art

The QCSE was measured in QDs in slightly different stacks. Using different stack configurations can lead to changes in the QCSE which will produce modulators with various performances.

All the papers measuring the QCSE in QDs or modulator applications are summarized in Table 4.3. This comparison only considers the material loss contribution to the IL and all ER and IL were calculated assuming a QD modulator length of 1 mm.

The work presented in [42] reported the second-largest bandwidth around 2 GHz but the 3.5 dB ER for a 8 V-swing is significantly lower than the one presented in this work. The bandwidths generally reported here are significantly lower than what is currently considered sufficient for prospective PICs, with current expectations around $40GHz$ [70]. Nevertheless, optimisation of the capacitance and

**Table 4.3:** State-of-the-art comparison

| | Cambridge (2007) [42] | NTU (2009) [41] | NSYSU (2011) [32] | Glasgow (2019) [43] | Current Work [UID[1]] | Current Work [PD[1]] | CNET (1993) [68] | KTH (2003) [69] | UCSB[3] (2012) [59] |
|---|---|---|---|---|---|---|---|---|---|
| ER | 3.5dB | 10dB | ∼10dB[2] | ∼12dB | 7.55dB | 8.94dB | 12dB | 10dB | 20dB |
| IL | – | – | – | ∼3dB | 3.9dB | 2.54dB | 3dB | 6dB | 5dB |
| V | 8 | 10 | 5 | 11 | 9 | 9 | 1.2 | 3 | 5 |
| B.W [GHz] | 2 | – | 3.3 | – | – | – | 20 | 50 | 67 |
| $\lambda\,[nm]$ | 1300 | 1328 | 1300 | ∼1310 | 1311 | 1316 | 1550 | 1530 | 1300 |

[1] The values are estimated at 21 $^{\circ}C$. [2] ER taken from 1V in Fig. 4 [32] to be consistent with the rest of the papers. [3] Approximated from Fig.4 at 1300nm [59].

resistance of these devices was not considered, which will play a major role in improving modulation bandwidth. On the other hand, the ER achieved in [41] and [32] are around 10 dB which is a similar value to the one presented in this work. However, the stacks have 10 ([41]) and 12 ([32]) QD layers. The additional QD layers absorb additional light due to more overlap between the absorbing QDs and the optical mode. Nevertheless, the bandwidth of such a stack may be smaller owing to increased transit time [71].

The work presented in [43] offers similar performance to this work. Nevertheless, it requires a larger driving voltage of around 11V-swing, and the stack has a higher QD density around $5.9 \cdot 10^{10}\,cm^{-2}$ and 8 QD layers.

Finally, comparing to QW modulators, our PD *FoM* is quite competive. Various works in the literature [68; 69; 59] have achieved a *FoM* of between roughly 2 and 4. The main advantages these QW devices currently hold over not only this work but QD modulators in general is that generally lower voltage swings are required to achieve a desired level of performance. Additionally, the larger density of states in QWs typically means shorter devices can be achieved. The former issue may prove difficult in overcoming, though reducing the spacer region thickness between QD layers has been suggested to reduce the required voltage swing [72]. Increasing the dot density will help improve reducing device lengths even further to that of QW equivalents.

To conclude, the stack with UID barriers offers similar performance to the

state-of-the-art shown in Table 2. Nevertheless, when the barriers are doped, the efficiency of the QCSE for modulation is boosted, offering better performance than the state-of-the-art in terms of *FoM*, driving voltage, electrical power consumption, and operational temperature from $-73\,^{\circ}C$ to $100\,^{\circ}C$.

## 4.4 Feasibility of same epistructure for integrated laser-modulator device

Very few in depth studies have been carried out working towards the integration of different QD devices. Two such devices that would benefit from being integrated together are the QD laser and QD modulator. This combination has already been explored using QW active regions with different strategies; intermixing [73], selective area growth [74], butt-coupling [75] and using the same QWs [76].

The use of the same epistructure and processing steps for multiple functions adds requirements on the active region material such as the complexity of having reasonably similar optimal wavelengths for the laser and the modulator. Any significant differences between the laser and the modulator would lead to a reduction in overall efficiency. Significant potential advantages of a combined functionality were suggested in [43],where the use of a QD DFB laser and modulator were shown to produce a negatively chirped pulse as a solution to the positive chirp introduced in fibre transmission systems.

Based on the superior PD *FoM* results obtained compared to the UID samples in the previous section of this chapter, the focus in this section will be on the PD QD samples. In this section, the maximum heat sink temperature the PD stack can operate at as both a laser and modulator in isolation without signs of significant degradation in performance is determined. The implications for the combined performance is then studied. To study the behaviour, the net modal gain and the net modal loss of the active region were measured using the segmented contact method [12].

The temperature behaviour of: 1) Peak net modal gain and optimal wavelength and 2) the QCSE in In(Ga)As/GaAs QDs in the active region of the modulator

were measured from 21 $^{\circ}C$ to 100 $^{\circ}C$. It was found that: the QD active region studied can be used in isolation for lasing and modulating up to 100 $^{\circ}C$ without signs of significant degradation in performance, particularly as a modulator. The optimal operational wavelength for both lasing and modulating shifts with heat sink temperature by 0.6 and 0.54 nm$^{\circ}C^{-1}$ respectively.

In reality for most systems a DFB laser would be used, where a desired operating wavelength, a high side mode suppression ratio and relatively narrow linewidth is achieved by controlling the lasing wavelength with the in-built grating. In this case the lasing wavelength tunes with the temperature dependence of the refractive index (typically below 0.1nm/K [77]). Such devices can be made where wavelength tuning is possible over a much wider range [78] and any wavelength with sufficient optical gain can be selected. In this case operating at the optimum modulator wavelength becomes a question of the modal gain available at this wavelength.

### 4.4.1 Gain performance of InAs Stacks

In Fig. 4.9, the net modal gain spectra at 21 $^{\circ}C$ for different bias current's are presented for the PD sample. Measurements were done pulsed to avoid self-heating effects. The ground state (GS) gain increases steeply and begins to saturate at high current densities. Current densities were calculated taking into account current spreading, determined from nearfield measurements. There is a slight spread in internal optical loss values at the absorption edge, particularly at low current densities (below 400A$cm^{-2}$) which is attributed mainly to noise error of the measurement. It can also be seen that the PD sample has a largely suppressed absorption peak. This is due to the presence of holes in the top valence states preventing absorption events as explained previously.

The peak net modal gain at all bias currents measured for the PD stack is plotted in Fig. 4.10 for different temperatures. Generally PD samples will produce significantly larger threshold current densities when compared to UID samples. This larger current density requirement is common in such devices and is attributed to the increase in internal loss through intervalence band absorption and increased nonradiative recombination [79]. However, p-modulation doping has been shown

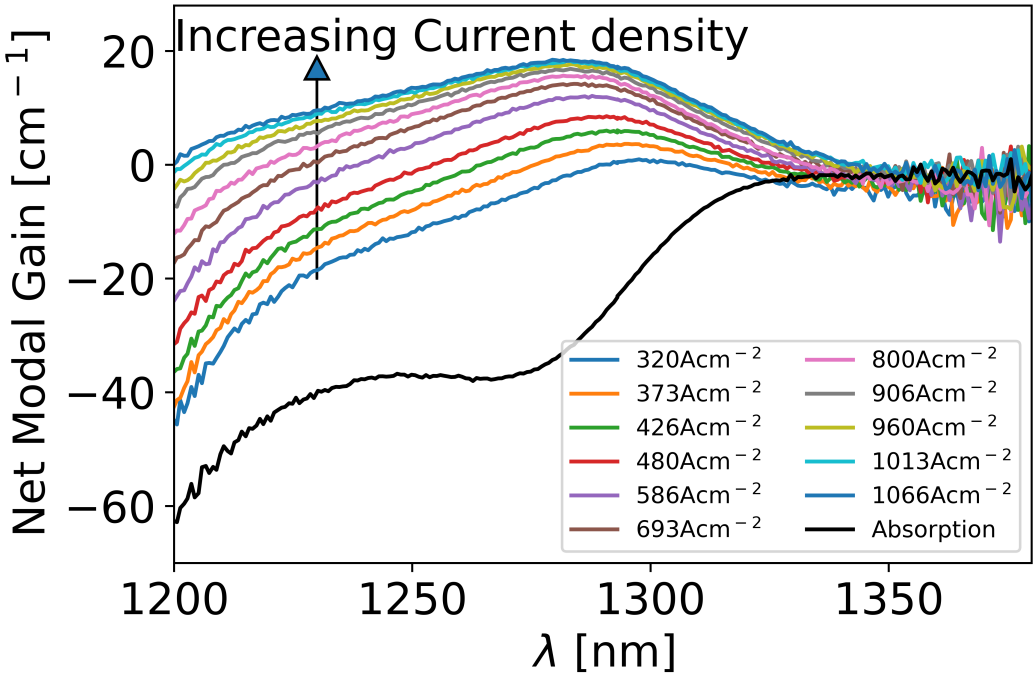


**Figure 4.9:** Gain Spectra at 21 °$C$ for the PD QD sample with increasing current density. Absorption shown as negative gain.

to actually enable lower threshold current densities at high temperatures and using short cavity length, and has a higher characteristic temperature compared to both undoped and n-doped QD lasers [80].

The peak net modal gain decreases with increasing heat sink temperature as shown in Fig. 4.11, reducing to 8 $cm^{-1}$ at 1066 A$\,cm^{-2}$ and 100 °$C$ for the PD sample. A fundamental issue when looking at device performance over a temperature range is that the bandgap of the semiconductor will change with temperature, resulting in a shift of the wavelength of the peak gain and of the overall spectrum. Fig. 4.11 also shows the wavelength at peak net modal gain of the segmented contact devices as a function of heat sink temperature for a fixed current density of 1066A$\,cm^{-2}$ for the PD device. As explained in chapter 3, the current density is found by using the measured device length and the device width, which is derived from the near-field profile, taking into account the effect of current spreading. The wavelength of the peak net gain was found to shift with heat sink temperature at a rate of approximately 0.6nm°$C^{-1}$. The figure also re-emphasises how the saturated

gain values decrease approximately linearly with heat sink temperature indicating a decay rate of 0.14 $cm^{-1}{}^{\circ}C^{-1}$.

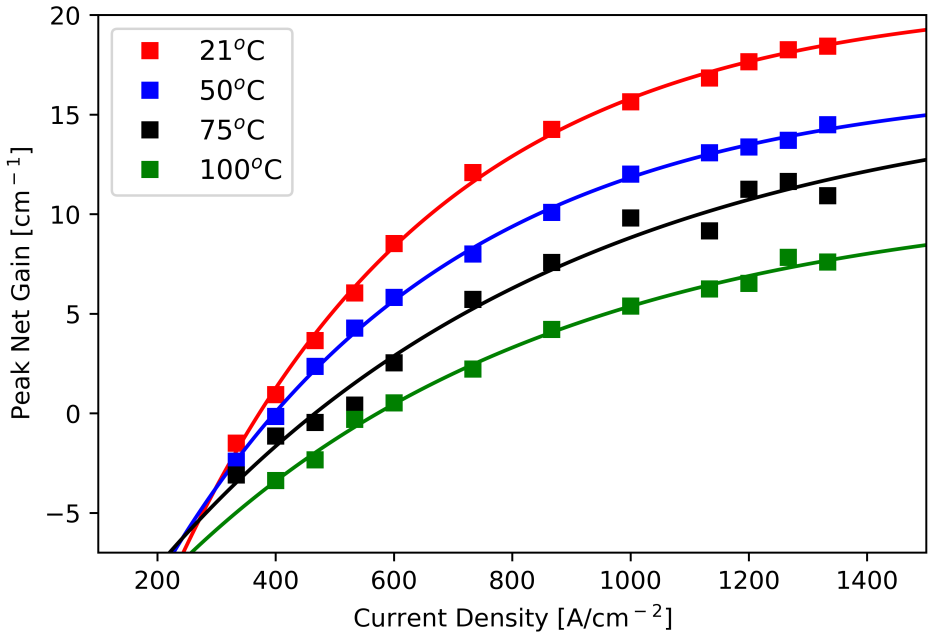


**Figure 4.10:** Peak Net Modal Gain between temperature's of 21 °*C* to 100 °*C* for the PD sample.

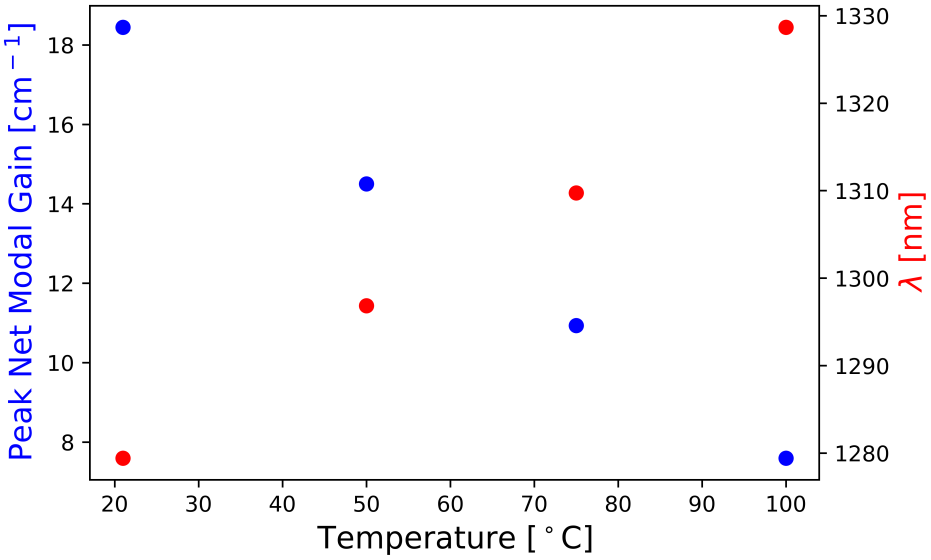


**Figure 4.11:** Peak Net Modal Gain between temperatures of 21 °*C* to 100 °*C* for the PD sample and corresponding wavelengths.

### 4.4.2 *FoM* performance for QD devices

The *FoM* performance for the QD devices was analysed in detail in the previous section 4.2, but will be briefly revisited here to consider the performance in context with gain data of the same devices. Fig. 4.12a shows the *FoM* spectra for both PD sample between 21 $^{\circ}C$ to 100 $^{\circ}C$. The maximum *FoM* is roughly 8 for the PD stack and degrades with temperature to roughly 5 at 100 $^{\circ}C$. The reduced rate of red-shift and increase in absorption peak are the main causes of the observed decrease with temperature.

Similar to that of Fig. 4.11, the peak FoM and corresponding wavelength are plotted in Fig. 4.12b. Similar to the laser, the optimal wavelength for the modulator is the result of optimizing $FoM = \Delta\alpha/\alpha(1V)$. The rate of change of optimal wavelength with temperature is very similar to the gain data, shifting at a rate of 0.54nm$^{\circ}C^{-1}$ for the PD sample.

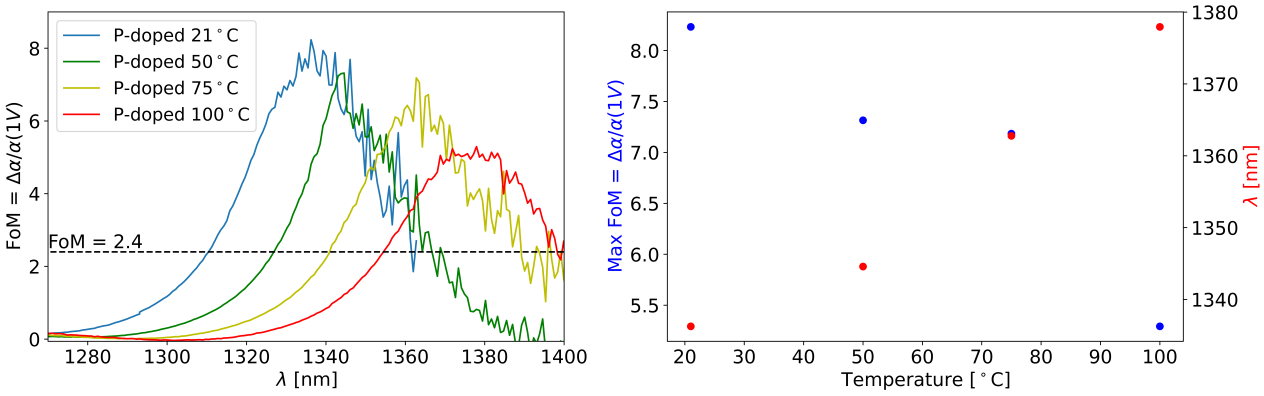


**Figure 4.12:** *FoM* for a 9V-swing for the PD QD barrier vs temperature (left). Evolution of maximum *FoM* and corresponding wavelength versus temperature for the PD sample (right).

## 4.5 Integration of laser and modulator with same QD active region

In this section, the integration of the QD laser and modulator using the same QD active region is discussed. From the previous section it is clear that the rate of change of optimal wavelength of both modulator and laser for both samples shifts by similar amounts. Although this agreement in spectral shift with temperature is useful,

closer inspection highlights that the difference between optimum wavelengths of the laser and the modulator is at least 50nm at all temperatures between 21 °$C$ to 100 °$C$ for the PD sample. This is highlighted more clearly again in Fig. 4.13.

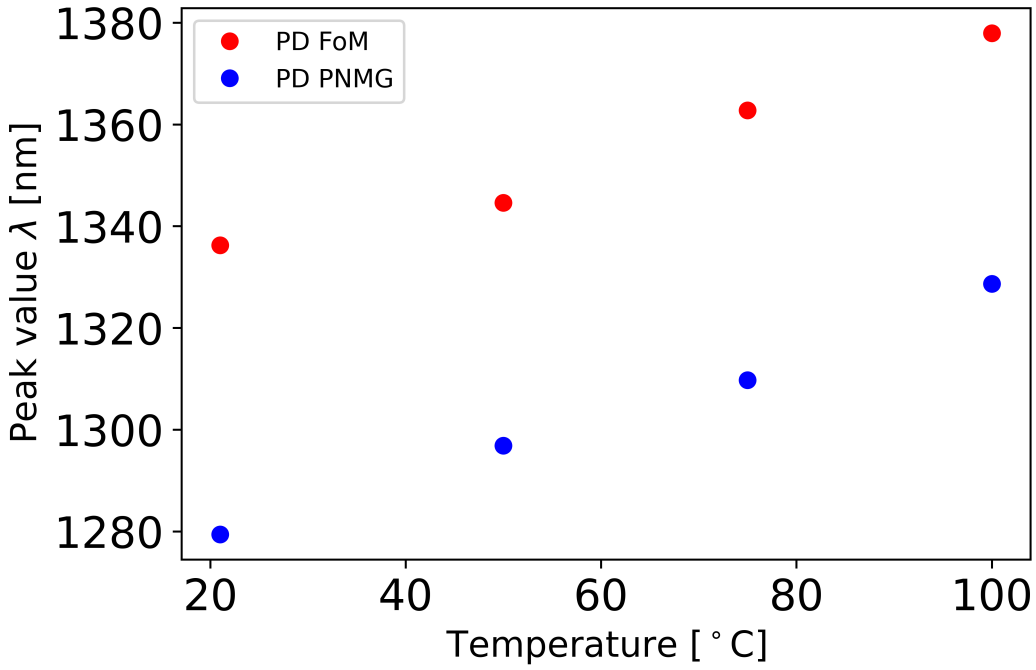


**Figure 4.13:** Peak wavelength values of both *FoM* (red) and gain (blue) for the PD sample.

One possible solution to reduce this difference is to use a DFB laser and tune its wavelength. The wavelength shift of a DFB laser, which is controlled by the temperature dependence of the refractive index is typically around 0.1 nm°$C^{-1}$ [81] which is lower than the PD stack measured in this work. To access the full temperature range it is necessary to utilise a DFB that can be tuned over a much wider temperature range [78]. In this case the DFB could be operated at the optimum modulator wavelength providing the available gain is sufficient.

In order to determine if this is feasible, first the desired modulator performance needs to be selected. It is not enough to simply choose the wavelength where the FoM is maximum. This is because although at the maximum you are in principle achieving the greatest contrast between ER (considered here as $\Delta\alpha$ from the measurements) and IL ($\alpha(1V)$ from the measurements), it is likely at the expense of requiring very long devices to achieve desired contrast ratios. Subsequently, and as

has already been shown in section 4.2.2, the optimal *FoM* for the PD sample has been selected based on attaining shortest device possible whilst maximising *FoM* performance.

Fig. 4.14 shows the gain and *FoM* spectra at 21 $^{\circ}C$ and 100 $^{\circ}C$ for the PD sample. Despite the peak values of both the gain and *FoM* of the PD sample not occurring at the same wavelength, there is still significant overlap between the two spectra, giving an early suggestion for the potential for integrated operation.

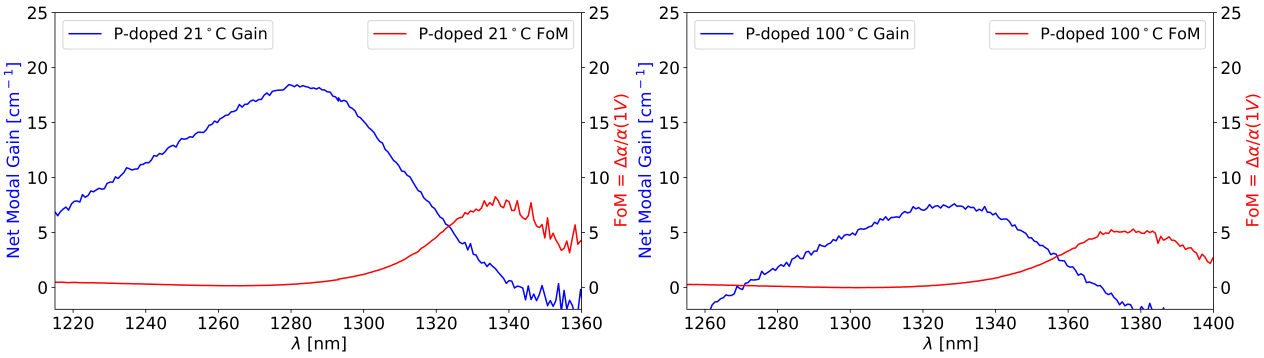


**Figure 4.14:** Net gain and FoM spectra for PD and UID samples at 21 $^{\circ}C$ (left) and 100 $^{\circ}C$(right) at 1066 A $cm^{-2}$.

To get a clearer picture of the integrated performance at the new optimal modulator wavelengths the achievable gain as well as modulator FoM are plotted in Fig. 4.15. Here for a threshold gain requirement (mirror loss) of roughly 2 $cm^{-1}$ for a 3mm laser with un-coated facets, operation up to 100 $^{\circ}C$ would be possible for the PD sample. Although not shown here, the PD sample was capable of maintaining similar performance at $-73$ $^{\circ}C$ whilst only requiring a 4V -swing.

In addition to this, as the measurements here were done pulsed, in practice the self heating that would arise from CW operation would lead to a red-shift in the wavelength of the peak net modal gain, potentially offering an improvement in lasing performance at the optimal modulator wavelengths. Other approaches such as laser annealing [82] or ion implantation followed by rapid thermal annealing [83; 84; 85] to tune their bandgap can also be used to alter optimum wavelengths with the penalty of greater fabrication complexity.

The results suggests that, taking into account mirror loss, sufficient gain can be

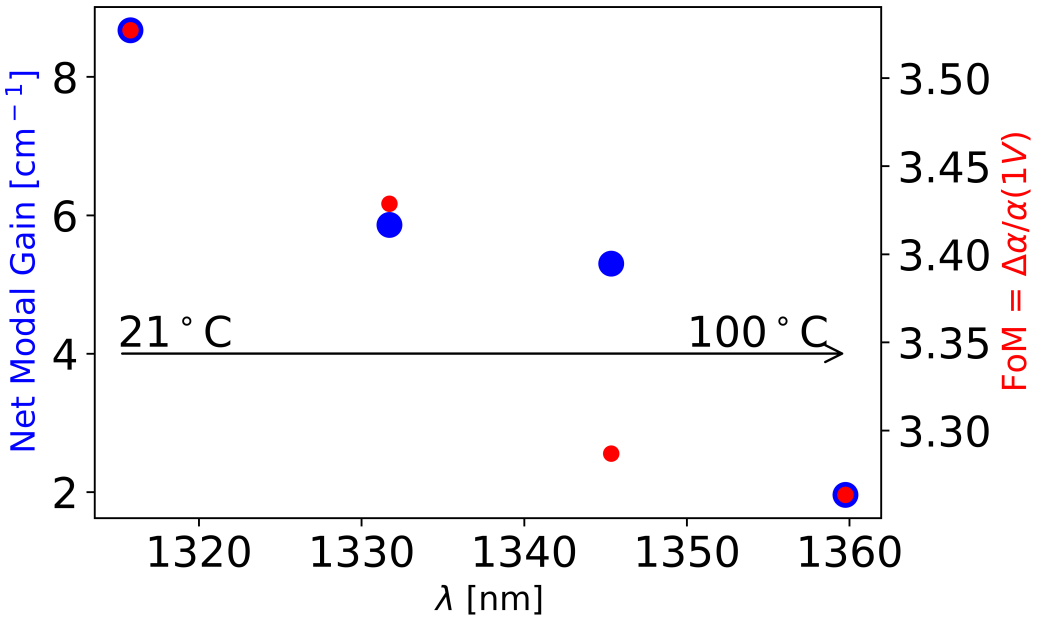


**Figure 4.15:** Evolution of optimal *FoM* and corresponding net modal gain with temperature versus optimal wavelength for PD sample.

achieved at optimal modulator wavelengths up to 100 °*C* for the PD sample. Similar results were achieved with the UID device, achieving sufficient gain up to 100 °*C* at the UID optimal modulator wavelengths. However, and as previously mentioned, the UID had markedly worse optimal *FoM* compared to the PD QD device. Nevertheless for either device improved gain performance and/or higher temperature operation at the optimal modulator wavelength may be possible providing the redshift produced in the laser due to self-heating effects when operated CW is large enough, the increased temperature does not significantly reduce available gain and the modulator/laser are thermally decoupled. If this is the case the significant improvement in modulation performance of the doped sample opens up the possibility of using a single epistructure for integrating a laser and modulator using such a QD active region. Such a device can be operated over a wide range of temperatures without significant compromise in overall device performance. This opens the possibility of using the devices in harsh environment applications on a GaAs substrate or build the QD III-V devices over a Si substrate to bring the laser and a more efficient modulator to the Silicon Photonics platform [10].

## 4.6 Chapter summary

This chapter has looked into the experimental measurement of the QCSE in InAs QD stacks. The focus of the study looked at comparing the QCSE behaviour in nominally identical stacks, except where p-modulation doping was introduced in the barrier layers above the QDs. Using the segmented contact method, low-noise absorption spectra were obtained when applying a range of reverse biases to the devices between temperatures of $-73\,^{\circ}C$ and $100\,^{\circ}C$.

Measurement of the QCSE in both QD stacks led to the observation of both an enhanced red-shift and non-trivial increase in absorption strength with applied reverse bias in PD samples. This behaviour was attributed to the carrier-blocking effect present in the PD QD's as a direct result of the increased presence of holes on the QD valence states. At low reverse bias, absorption at ground state transitions were quenched, leading to higher energy absorption and decreased ground state absorption peak. Then, as the reverse bias is applied, holes are removed from the valence states increasing the electron occupation for more significant ground state absorption.

The *FoM*, defined as the ratio of the change in absorption for a given voltage swing to the absorption at $1V$, indicated significantly increased performance in the PD sample at all temperatures. The degree of improvement in PD samples was observed to decrease with temperature, which was attributed to the thermal redistribution of holes within the valence states of the PD stack, weakening enhancements due to the carrier-blocking effect.

Gain measurements were also carried out on the same InAs stacks to determine the feasibility of an integrated laser-modulator epistructure. Gain performance was characterised for the PD sample. Despite similar temperature trends between the rate of change in optimal gain and *FoM* performance wavelength, specific peak wavelengths were considerably far apart. Sacrificing peak gain performance for optimal *FoM* led to the potential for a prospective laser-modulator device using PD QDs, where threshold gain including mirror loss was still attainable up to $100\,^{\circ}C$.

# Chapter 5

# Optimisation of QD EAM Design

## 5.1 Introduction

There are various factors that can help indicate potential performance of modulators. This chapter will look into determining suitable parameters to further optimise the QD EAM studied in Chapter 4. Parameters such as overlap between modal and static electric field in the core, intrinsic capacitance and resistances as well as the QCSE of the optimised structure will be explored. To carry out this investigation, eigenmode expansion simulations and Schröedinger-Poisson models will be used in conjunction with one another to ensure an accurate approximation of device physics is achieved.

## 5.2 Overlap between modal and electric fields of QD stacks

The first parameter to be investigated for optimisation is the overlap integral between the optical mode of the device and the static electric field in the active region. The overlap between these two parameters helps determine how strong the QCSE will be, which will effect the achievable $ER$ of the device. The larger the overlap integral the better the $ER$ of the modulator will be. Subsequently by varying geometrical parameters such as the waveguide width and etch depth of the modulator the overlap integral between the applied electric field and the optical mode of the device can be maximised, in turn maximising the QCSE-induced electro-absorption

and thus increasing the *ER* and efficiency of the EAM. As the active region is where the absorption and modulation process should occur, to maximise the overlap, and therefore the potential performance, both fields need to be as tightly confined to the active layers as possible. Here eigenmode expansion method simulations within Lumerical (Lumerical Inc. 2021, MODE) varying the width and etch-depth of the waveguide device are investigated for both samples with undoped and p-modulation doped active layers to determine optimal overlap integral conditions.

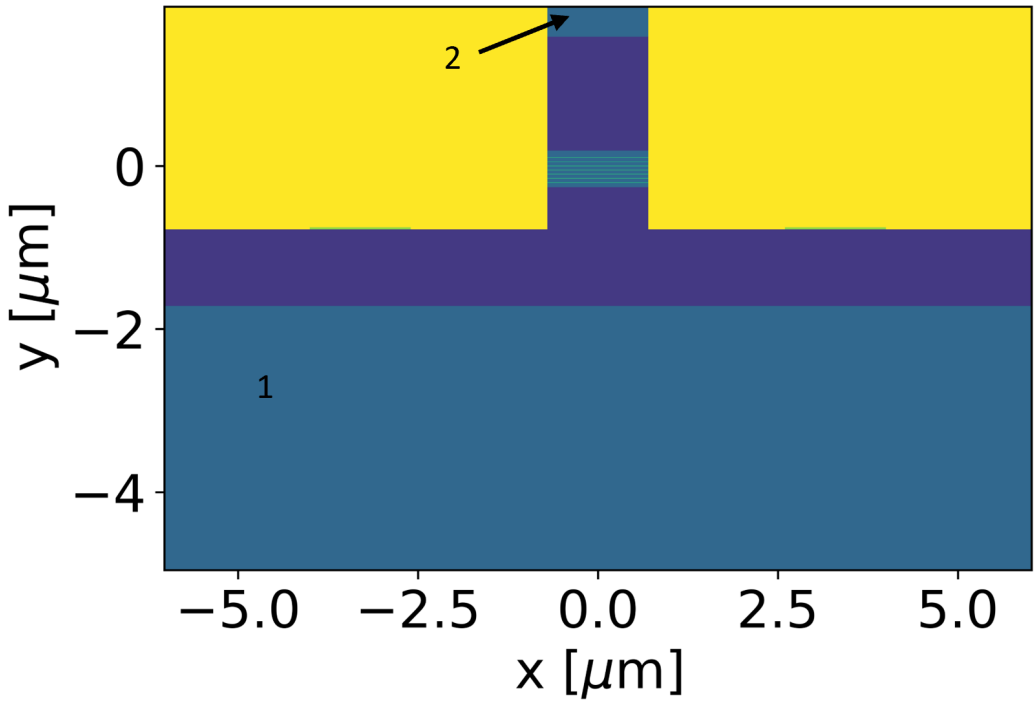


**Figure 5.1:** Diagram of QD waveguide device showing a 1.2 μm width and 2.25μm etch depth. Dark blue areas represent the upper and lower cladding of the waveguide. The region between the two claddings is the active region with the QD layers included. The lighter blue areas labelled 1 and 2 are the substrate and P-contact respectively, both comprising of GaAs. Yellow is a low refractive index material that acts at a dielectric passivated surface.

### 5.2.1 Single-mode operation

First the waveguide width is looked at for optimisation. Here a 2D cross section of the proposed QD waveguide device is simulated, varying the width of the waveguide between 2.4 μm and 0.9 μm in steps of 0.1 μm. An example of such a simulated device can be seen in Fig. 5.1. Before trying to calculate the overlap integral the

simulations are used to first find the single mode cut off point. This is the point at which the device only supports the fundamental TE and TM modes, as all higher order modes are no longer supported within the waveguide. Having the device as small as possible can enable higher integration densities on a PIC, and having single mode-operation further aids in improving coupling efficiencies to other components such as fibres in longer distance communications [72]. Fig. 5.2 shows the results of the simulation. It can be seen that the single mode cut off point occurs at around 1.5 µm. This essentially puts an upper limit on the waveguide width of the modulator device. With this limit now set the overlap integral as a function of waveguide width can be looked at up to a value of W = 1.4 µm to ensure single-mode operation is achieved for any subsequent device consideration.

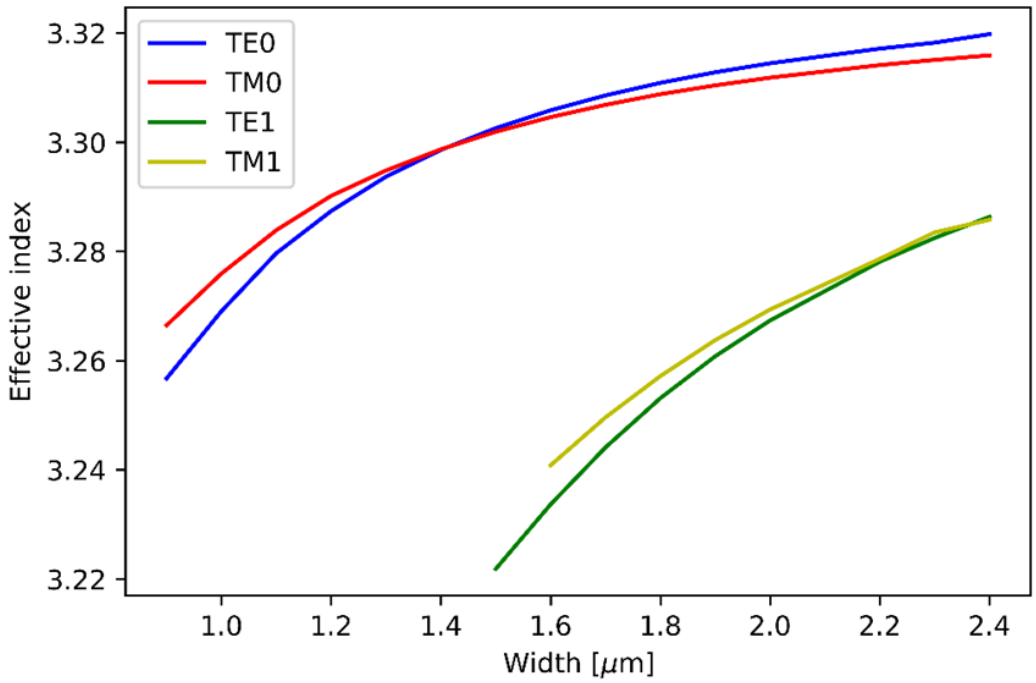


**Figure 5.2:** Effective index variation vs. waveguide width at etch depth of 2.25µm

### 5.2.2 Overlap vs waveguide width and etch depth

With an upper limit set on the waveguide width for single mode operation, the same waveguide structure, with and without doping in the QD barrier layers, were simulated in NextNano [54] to determine the electric field variation across the structure in order to determine the relationship between the overlap integral and waveguide

width. In order to ensure that single mode operation is obtained and devices are not too lossy, simulations are only carried out between 1 µm and 1.4 µm. Figure 5.3 shows the fundamental TE mode profile and electric field profile under an applied bias of 0V for a waveguide width of 1.2 µm and etch depth of 2.25 µm. The calculation of the overlap considers only the induced electric field in the region of the active layers. The general equation used to calculate the overlap integral is given by equation 5.1

$$Overlap = \frac{(\int E_{mode} \times E_{static}\, dA)^2}{\int E_{mode}^2\, dA \int E_{static}^2\, dA}, \tag{5.1}$$

where $E_{mode}$ and $E_{static}$ are the modal and static electric fields respectively.

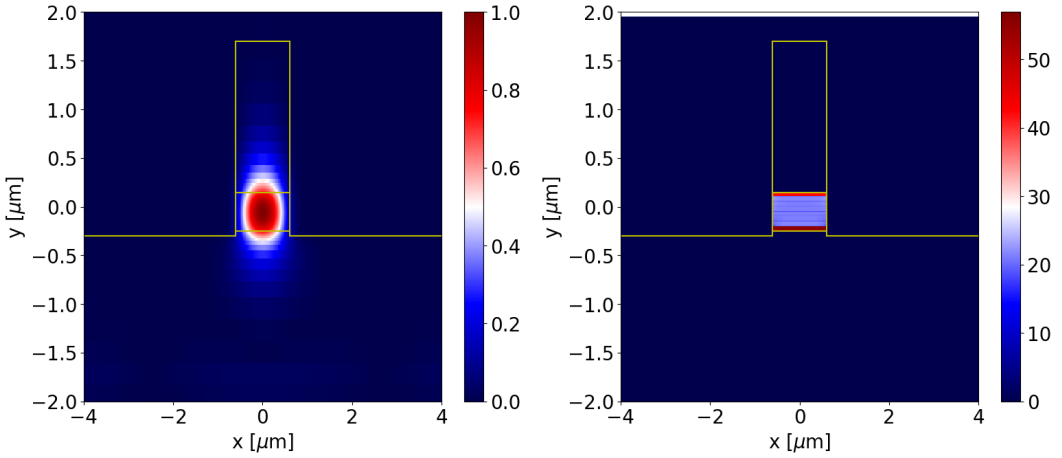


**Figure 5.3:** Modal (left) and undoped electric field at 0V (right) for waveguide structure using an example width of 1.2 µm and depth of 2.25 µm. Colour bar for the undoped electric field shows strength of electric field in units of kV/cm.

The variation with overlap for both the undoped and p-modulation doped structures are shown in Fig. 5.4 and Fig. 5.5 respectively. It is clear that in both structures the overlap integral increases with waveguide width. This observation is reasonable as the increase in width simply leads to less sidewall leakage of the mode, thus causing the value of the integral to increase. It is also clear from the figure that the undoped sample consistently has a larger overlap value compared to the p-doped sample. The optical fields for both structures are almost identical, implying any

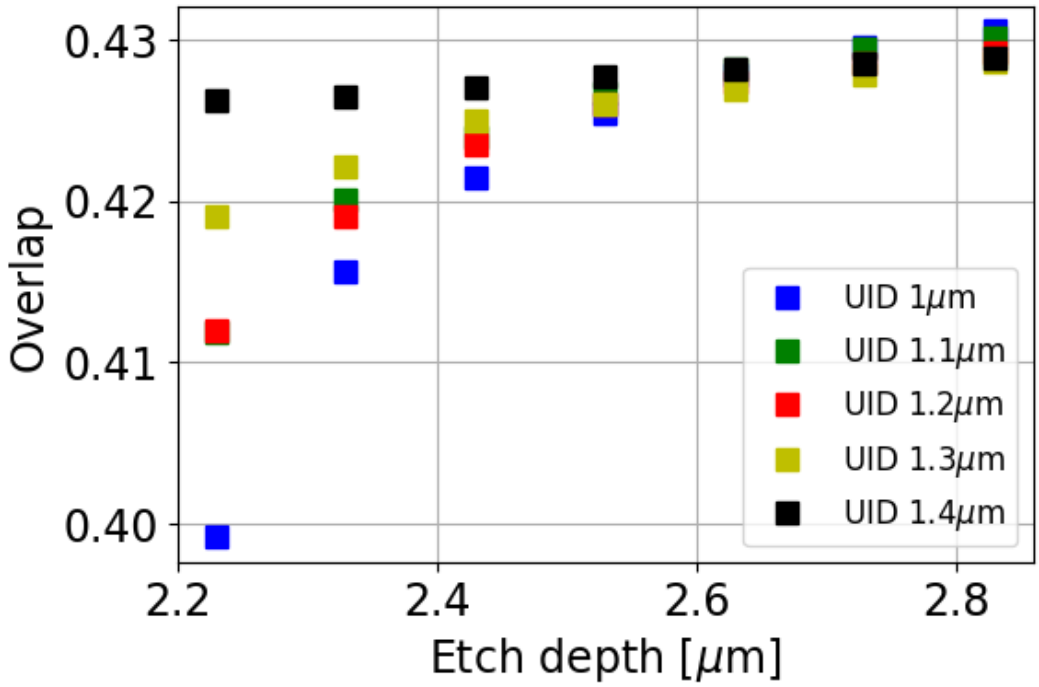


**Figure 5.4:** Evolution of the modal field overlap with the built-in static electric field for the undoped waveguide.

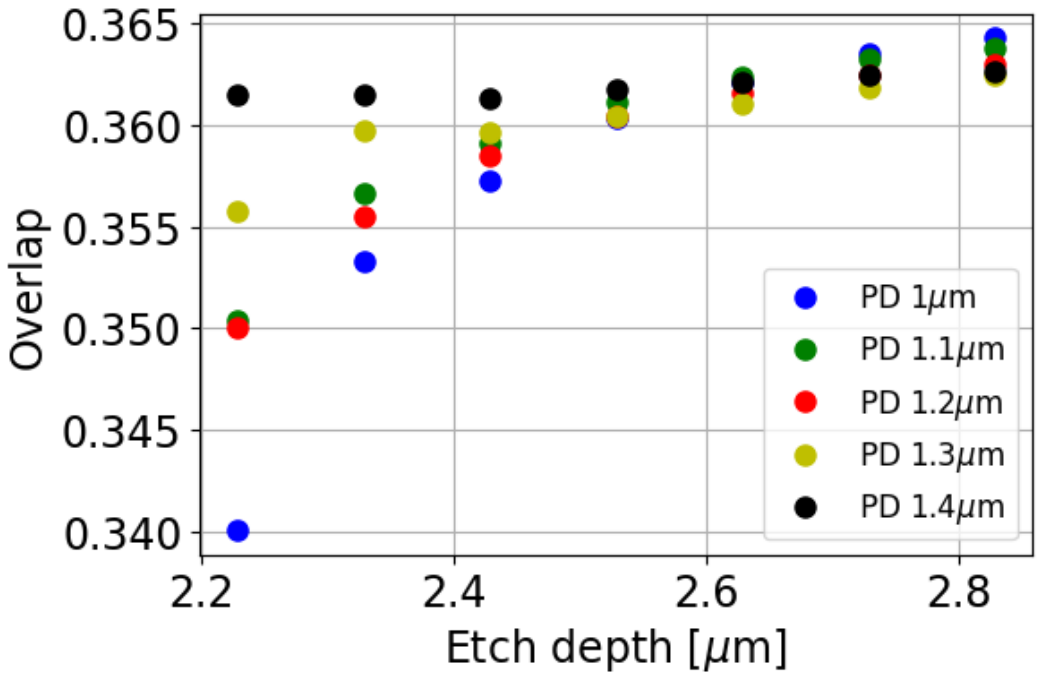


**Figure 5.5:** Evolution of the modal field overlap with the built-in static electric field for the p-doped waveguide.

differences in overlap originate with the variation in the electric field distribution. Comparing both electric field distributions of the two samples, shown in Fig. 5.6, it is clear the reduction in overlap is due to the reduced area in the active region where there is a strong field present. The figure highlights how in the undoped distribution, the electric field is consistent across the whole active region. In the p-doped case the field is only really present at the bottom of the active region towards the n-doped cladding. This can be explained as follows; the doping in the barrier layers above

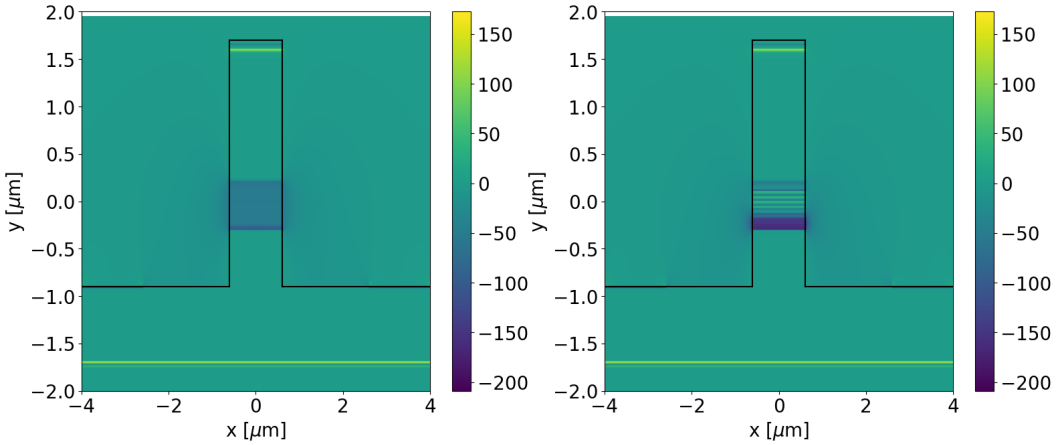


**Figure 5.6:** Built-in static electric field for the undoped (left) and p-doped (right) devices. Scale is in kV/cm

the dots leads to an artificial extension of the p-doped region of the p-i-n diode into the intrinsic region. As a result, only the dot layers closest to the n-doped cladding have been depleted, and so in this region there is some re-establishment of the electric field induced by the junction [86]. This smaller region in the active region where an electric field is established will subsequently lead to a smaller overlap with the modal field.

Fig. 5.4 and 5.5 also shows the evolution of the overlap using etch depths between 2.25 µm to 2.85 µm. It can be seen that increasing the etch depth leads to an increase in the overlap integral. The main reason for this behaviour is that etching further down into the cladding reduces the mode leakage underneath the active region, thus leading to the mode being more confined producing a larger overlap value.

In Figs.5.4 and 5.5, it can also be seen that the overlap begins to plateau the

deeper the etch is taken into the cladding. This trend is related to the previous point as despite etching reducing the leakage into the cladding, eventually the confinement of the mode is limited to leakage through the sides of the waveguide and the areas immediately above and below the active region. This plateauing of the overlap suggests significant fabrication tolerance with respect to the desired overlap, achieving nearly constant overlap values over an etch depth variation on the order of 100's nm. Finally, Figs.5.4 and 5.5 illustrate how the increase in waveguide width eventually reaches a limit in overlap, with slight reductions in overlap observed at 1.3 and 1.4 μm. The modal confinement in the active region for each waveguide width as a function of etch depth was also investigated. It was seen that the modal confinement generally follows the same trend as in Fig. 5.4, but with values for 1.3 and 1.4 μm producing a more uniform confinement across all etch depths. This trend is highlighted in Fig. 5.7.

The reason that the overlap subsequently decreases slightly at 1.3 and 1.4 μm is that despite the small increase in modal confinement, it is not sufficient enough to compensate for the increased area of the static electric field at these wider waveguide widths. As a result the overlap starts to gradually decrease with waveguide width. The results shown here suggest that the optimal structure to maximise the overlap would be using a waveguide width between 1.1 and 1.2μm with an etch depth between 2.65 and 2.85μm.

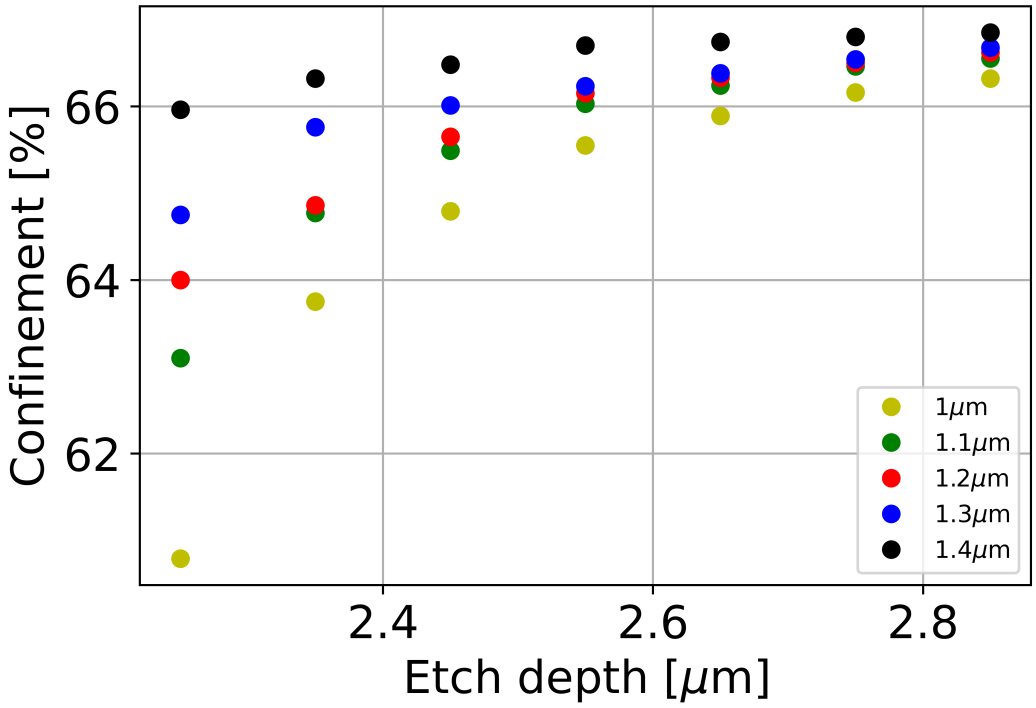


**Figure 5.7:** Plot of modal confinement in active region vs etch depth using waveguide widths between 1 and 1.4μm.

## 5.3 Capacitance and resistance considerations

Another important characteristic of any modulator is its capacitance. In an RC limited system, the capacitance is incredibly important to the devices maximum operational speed. In addition, the capacitance is also an important parameter in determining the energy consumption of a modulator. For a modulator that has a capacitance C, resistance R and operates with a voltage swing V, the RC limited bandwidth and energy consumption per bit are given by equation 5.2 and equation 2.2 respectively.

$$f_{RC} = \frac{1}{2\pi RC} \tag{5.2}$$

Clearly then when trying to optimise the modulator, having an understanding of the devices capacitance is an important component in trying to characterise the modulators potential performance. To determine the capacitance of the measured

structures from chapter 4, the PD and UID QD stacks are recreated in 1D using NextNano software [54]. The structures were initially simulated with reverse bias values ranging between 0 and 3.5V in steps of 0.25V. At each voltage step the carrier density across the material was determined. The materials simulated are essentially p-i-n diodes, and so the intrinsic region carrier density was integrated to produce the carrier density in units of $cm^{-2}$

The well known expression that relates capacitance, charge and voltage, given by the change in charge for a given change in voltage was used to obtain the capacitance per square cm, given by equation 5.3

$$C = \frac{dQ}{dV}. \tag{5.3}$$

This parameter then allows us to determine the total capacitance of the structure for any given waveguide width and length.

As explained above, the first stage of determining the capacitance in these two structures is finding the change in carrier density as a function of reverse bias. The evolution of the hole and electron density in the intrinsic region for both the PD and UID structures was investigated and is shown in Fig. 5.8. The most obvious difference between the carrier densities of the PD and UID samples was the increased hole density in the dot layers in the PD structure. In addition to this, the UID structure at 0V is almost depleted in the intrinsic region, with only the dot layers closest to the p and n boundaries with any holes or electrons present respectively. By an applied reverse bias of 6V, the intrinsic region is largely depleted. A similar process occurs in the PD structure, though the larger initial carrier density present has meant that there were still some dot layers with significant carrier densities even at 6V.

When calculating the capacitance from the integrated carrier density, the optimised waveguide width of 1.2μm found from the overlap section was used. In this way, the capacitance can be found for a waveguide configuration that maximises the overlap between the modal and electric field within the core.

The plot in Fig. 5.9 shows the calculated capacitance for both the PD and UID

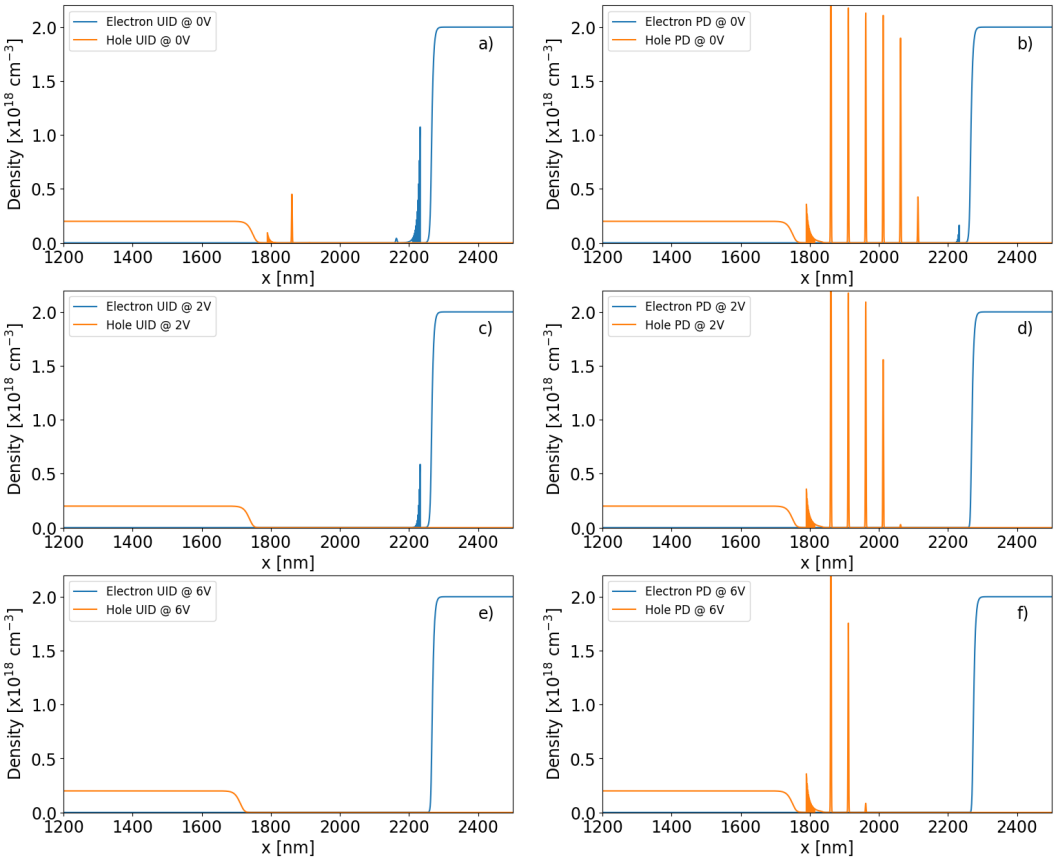


**Figure 5.8:** Carrier densities for UID and PD material at 0 (a,b), 2 (c,d) and 6V (e,f).

structures in units of picofarads per cm between temperature range of $-73\,^{\circ}C$ and $100\,^{\circ}C$. It is clear that the PD structure produces a noticeably larger capacitance per cm than the UID equivalent. At a reverse bias of 1V the PD capacitance is roughly 6.3pF/cm, as opposed to the UID value of roughly 3pF/cm at $21\,^{\circ}C$.

Although both structures see their capacitance decrease with reverse bias, due to the depletion of carriers out of the intrinsic region, the value at 1V is important as under operation this is the value that will limit bandwidth and subsequent energy consumption, assuming the voltage swing is taken from this value, as was done in previous work [64].

The increase in capacitance in the PD structure comes from the increased carrier density in the intrinsic region. At large reverse bias values the UID capacitance is dominated by the change in carrier density in the p/n cladding boundaries. In the PD structure slight plateaus can be observed at certain voltage swings. These

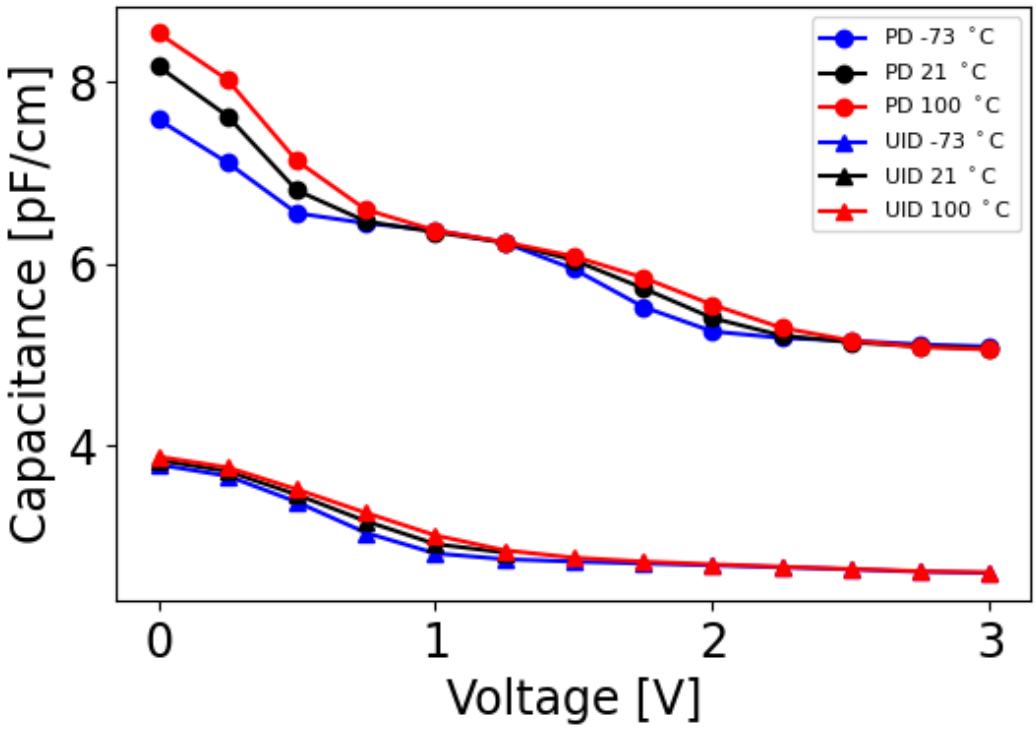


**Figure 5.9:** Capacitance for both UID and PD structures at $-73\,°C$, $21\,°C$ and $100\,°C$

features correspond to the depletion of carriers in a given dot layer and has been observed in various QD devices in the literature [87; 88; 89]. In the UID structure these plateaus are not observed to the same extent due to the dot layers being largely depleted even at 0V, thus the C-V curve has more of a resemblance to that of a bulk device. It can be seen in Fig. 5.9 that there is very little change in the profiles with temperature, with any changes due to the slight thermal redistribution of carriers within the intrinsic region.

Work carried out in [90] studied the effect of mesa area on the capacitance of similar InAs QD photodiodes. The study determined a parasitic capacitance of approximately 520fF. Parasitic capacitance due to unavoidable characteristics such as wire bonding [91] are not accounted for in the current simulations. Given that the devices in [90] are similar to those simulated here, accounting for the parasitic capacitance suggests the values obtained from the simulations are reasonable. Furthermore, the parasitic capacitance being of the same order of magnitude as the junction capacitance further reinforces the need to minimise the junction capaci-

tance of the device.

As explained above, it is also useful to have an idea of the resistance within the structure to try and get some understanding of bandwidth performance. The regions labeled A-E in Fig. 5.10 highlight key resistive parts of the prospective modulator device. Again based on of the results from section 5.2, to maximise the overlap between the electric and modal fields the structure uses a 1.2 µm waveguide width and etch depth of 2.85 µm.

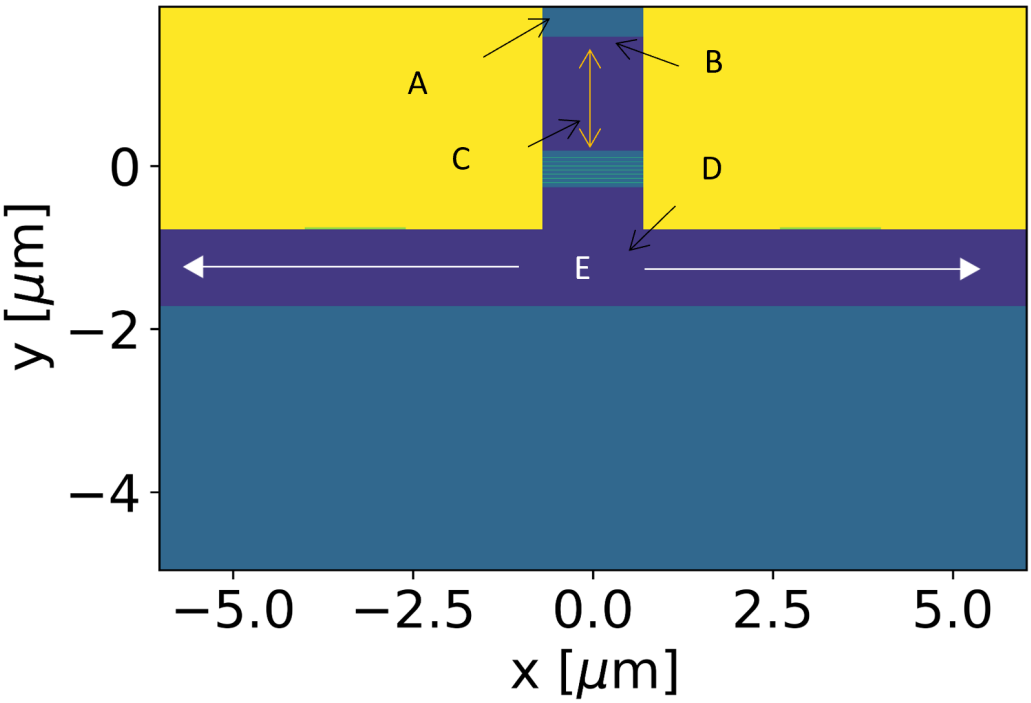


**Figure 5.10:** Diagram of QD waveguide device.
A-E represent key resistive regions. A - highly PD contact layer, B and C are PD GaAs/AlGaAs layers and AlGaAs cladding respectively, D and E are n-doped equivalents.

To calculate the resistance in the structure, the mobility was calculated, taking into account the effect of aluminium percentage and doping concentration in the AlGaAs cladding layers. In order to do this, a simple empirical expression that has formerly been developed has been used to take into account the effect of aluminium content and doping on the hole mobility when doped with Carbon [92]. Despite using beryllium as the dopant atom in the current samples, the formula agrees well with previous experimental work. This is due to the fact that for the doping values

used in the current samples, the mobility is largely unaffected by the dopant atom [93]. The material resistivity is then found using the calculated mobility. To determine the resistance from the resistivity $\rho$, the general relation is used using the length L and cross sectional area A of each region given by equation 5.4

$$R = \frac{\rho L}{A}. \tag{5.4}$$

The values of length and area used in this thesis will depend on where specifically the resistance in the structure is being calculated. Table 5.3 below shows the resistance for each of the regions shown in Fig. 5.10.

**Table 5.1:** Resistance contribution from each section highlighted in Fig. 5.10

| Region | Resistance [$m\Omega$cm] |
|---|---|
| A | 2.8 |
| B | 6.3 |
| C | 402 |
| D | 3.9 |
| E | 13 |

In each instance the value for modulator length is on the denominator for resistances at each point A-E. This feature allows for the calculation of potential bandwidths for the PD and UID structures without having to worry about device length, as it cancels with the capacitance. It should also be noted that the values in the table are identical for both structures, and so the intrinsic bandwidth is entirely dependent on the capacitance of the specific structure. Using the capacitance values for both structures at a reverse bias of 1V, the intrinsic bandwidth is calculated and given to be roughly 120 and 60GHz for the UID and PD devices respectively.

The above calculated bandwidths are likely to be overestimates of the real device performance. Nevertheless, purely from intrinsic resistance and capacitance considerations, it is clear that the UID device has a larger potential intrinsic bandwidth. The larger UID bandwidth ultimately means that although there is a higher FoM in the PD sample, as shown in chapter 4, in terms of maximum operational speed the UID structure is the superior active material. However, and as mentioned

above, there are other factors that need to be considered when considering these QD active regions for real devices. There are other resistive components that have not been considered here, such as the interface resistance at the electrodes. This parasitic resistance will likely be of the same order of magnitude as the intrinsic resistance [90; 94]. Additionally such resistances would be considered about the same whether using a PD or UID device. Taking into account parasitic capacitance which would also be considered the same irrespective of whether the device was PD or UID, and the discrepancy between PD and UID bandwidth could actually be smaller than calculated above. This scenario will depend on factors like desired extinction ratio and insertion loss, and the subsequent lengths needed to achieve them. All of this depends on the fine balance of many parameters, and the situation the device is used in, where restrictions on parameters like maximum voltage swing may not be an issue.

### 5.3.1 Capacitance under optimal *FoM* conditions

As alluded to in the previous section, although the intrinsic capacitance and resistance have no length dependence when it comes to the prospective bandwidth calculations, other factors can effect such metrics to the extent where device length becomes a relevant parameter to consider. In this scenario, minimising length to subsequently minimise capacitance to reduce energy consumption and improve bandwidth becomes a key goal. As in the previous chapter, to determine the length of a modulator device, a targeted performance of approximately 20dB ER and 6 dB IL has been considered for the PD samples and 10dB of IL for UID samples. This pins the length and subsequent capacitance to ensure optimal *FoM* performance.

Starting with the PD samples, it can be seen in Table 5.2 that capacitance increases slightly with temperature and at lower voltage swings. The result against temperature is expected and is attributed to the decrease in carrier-blocking effect at higher temperatures. Likewise larger capacitance at lower voltages is simply due to the lower ER produced and subsequent longer lengths required to achieve the desired level of performance. It should also be noted that capacitance per unit length is taken at a reverse bias of $1V$, as this would be the limiting operational capacitance

**Table 5.2:** PD and UID Modulator Lengths based on *FoM* inlcuding capacitance

| PD | Voltage Swing [V] | ER [dB $mm^{-1}$] | IL [dB $mm^{-1}$] | Length [mm] | Wavelength [nm] | Capacitance [pF] |
|---|---|---|---|---|---|---|
| | 9 | 8.94 | 2.54 | 2.23 | 1315.8 | 1.42 |
| 21 °C | 6[1] | 6.48 | 3.17 | 3.08 | 1312.8 | 1.95 |
| | 4[1] | 2.89 | 1.54 | 6.9 | 1321 | 4.38 |
| | 9 | 8.04 | 2.34 | 2.48 | 1331.7 | 1.57 |
| 50 °C | 6[1] | 5.31 | 2.68 | 3.76 | 1330.2 | 2.38 |
| | 4[1] | 2.8 | 1.47 | 7.1 | 1337 | 4.51 |
| | 9 | 7.65 | 2.33 | 2.62 | 1345.3 | 1.66 |
| 75 °C | 6[1] | 4.84 | 2.49 | 4.13 | 1343.8 | 2.62 |
| | 4[1] | 2.64 | 1.31 | 7.59 | 1351.4 | 4.82 |
| | 9 | 7.09 | 2.17 | 2.82 | 1359.8 | 1.79 |
| 100 °C | 6[1] | 4.3 | 2.17 | 4.65 | 1359.8 | 2.95 |
| | 4[1] | – | – | – | – | – |
| −73 °C | 4[2] | 6.98 | 2.45 | 2.86 | 1274.9 | 1.82 |
| UID | | | | | | |
| 21 °C | 9[1] | 7.55 | 3.9 | 2.65 | 1311.2 | 0.8 |
| 50 °C | 9[1] | 7.81 | 4.08 | 2.56 | 1328.7 | 0.77 |
| 75 °C | 9[1] | 7.28 | 3.76 | 2.75 | 1338.5 | 0.83 |
| 100 °C | 9[1] | 4.97 | 2.54 | 4 | 1355.2 | 1.2 |

[1] Values found for ER/IL = 20dB/10dB. [2] Value found for ER/IL = 20dB/7dB

of the device when considering different voltage swings. Fig. 5.9 indicates that the capacitance at $1V$ does not change significantly with temperature, and so does not have a significant effect on the observed trend with temperature.

Under real operation, the device length would not change with temperature, and so a fixed length must be chosen to ensure the prospective modulator would perform under all temperatures to the desired level. To achieve this at a voltage swing of $9V$, a device length of 2.82mm would be used for the PD stack. Although this produces the maximum capacitance of 1.79pF, it is only slightly larger than the lowest achievable value for the PD device (1.42pF) at $21\,°C$. In addition, the slightly longer length means for temperatures below $100\,°C$, performance superior to the criteria used here is in principle possible. If lower temperature operation is required, from the results in table 5.2, it can be suggested that provided a voltage swing slightly larger than $4V$ is applied at $-73\,°C$, the device length of 2.82mm

would more than suffice to achieve the desired ER/IL ratio for all temperatures measured.

The UID data in the table, as mentioned in chapter 4.3.2, relies on worse performance when extracting device lengths from an ER/IL of 20dB/10dB even when using a $9V$ swing. Despite the similar device lengths up to $75\,^{\circ}C$ compared to the PD stack, the reduced capacitance per unit length does mean that between each temperature the UID has a lower intrinsic capacitance.

Although initially this may seem like an advantage for the UID sample, there are various issues that should be considered. Modulation performance is worse compared to the PD stack, but additionally it can be seen that at $100\,^{\circ}C$, the UID modulator length exceeds 3mm, at 4mm. This is over 40% larger than the longest PD length, and would certainly impact integration density when considered in a larger PIC. In addition, if one were to pin the length of the UID to 4mm in a similar fashion to what was done with the PD stack above, it can be seen that the subsequent capacitance of 1.2pF is closer to the PD value of 1.8pF than when simply looking at capacitance per unit length in Fig. 5.9. As a whole then, even with slightly worse capacitance performance, the PD stack offers better performance over a far wider temperature range whilst improving potential integration density.

### 5.3.2 Optimising QD stacks for capacitance and resistance

The capacitance values calculated in Fig. 5.9 were found using the original measured stacks. However, using NextNano, variations to the stack could be made to see how potential RC properties were effected. This section will look at modifying the QD stack to determine if a more optimal configuration for capacitance and resistance can be produced. The first set of plots in Fig. 5.11a and b shows how the capacitance only increases slightly with increasing aluminium content in the AlGaAs cladding. The capacitance doesn't change significantly here as it is mainly the active (intrinsic) region materials that will govern the capacitance, which is unchanged between simulation runs. Nevertheless this would be detrimental to the potential bandwidth performance of the modulator. Additionally, it should be noted that changing the Al content in the cladding also effects the intrinsic resistance of

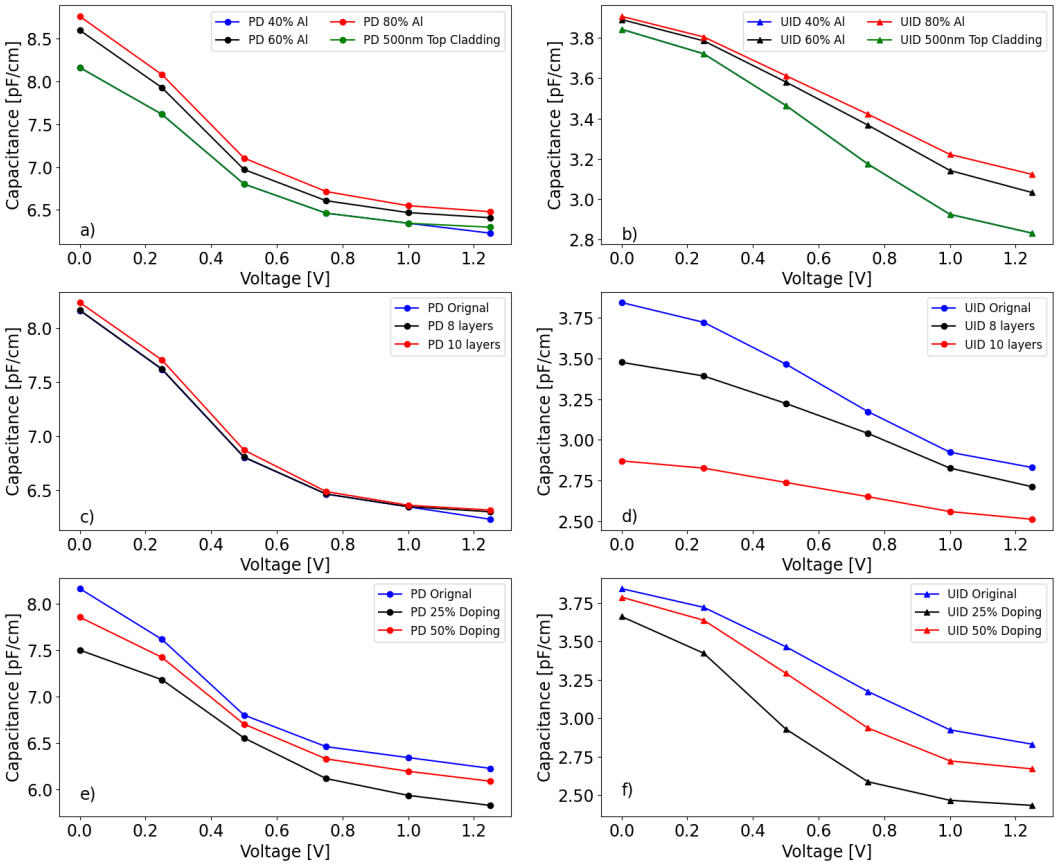


**Figure 5.11:** Capacitance for both PD (a) and UID (b) structures where aluminium percentage in the cladding is varied. The effect on capacitance by changing the number of QD layers is also looked at for PD (c) and UID (d). Variation in capacitance by using stepped doping profile in the cladding is also shown for PD (e) and UID (f)

the device. This will be discussed shortly below.

In Fig. 5.11c and Fig. 5.11d different trends are seen in the capacitance when increasing the number of QD layers. In Fig. 5.11d, it can clearly be seen that as the number of QD layers in the UID sample are increased, so the capacitance of the device decreases. This is not surprising as given that the overall materials are identical between simulation runs, the additional QD layers will create a wider intrinsic region. This increase in width is fundamentally what causes the reduction in capacitance. However, it can be seen when studying Fig. 5.11c that increasing the number of QD layers in the PD sample produces almost no change in the capacitance. This highlights the significance the doping layers are having on the overall capacitance of the device. Despite increasing the number of QD layers, the depletion region cre-

ated between the dot layers and the n-cladding does not change significantly enough to effect the device capacitance. In principle reducing the number of layers would also not have an effect on the capacitance in the PD structure, at least up to the situation where the number of QD layers that are depleted at $0V$ in the pin structure are equal to the total number of QD layers. However, reducing the number of dot layers in the PD structure would impact the extent in which the absorption peak increases under reverse bias. As this was considered to be a contributing factor in increasing the *FoM* in chapter 4, reducing the number of QD layers in the PD structure is not considered to present any immediate benefit.

Finally, the set of plots in Fig. 5.11e and Fig. 5.11f show a decrease in capacitance for both PD and UID structures as the doping density in the vicinity of the intrinsic region is reduced by incorporating a stepped doping profile in the cladding. This fundamentally occurs simply due to the smaller amount of charge in the system. Once again, as with the variation in Al content in the cladding, intrinsic resistances of the devices will be effected, and will be considered in the next section.

### 5.3.3 Resistances of different device designs

As previously mentioned, adjusting parameters like Al content and doping density in the cladding is going to have effects on the resistance as well as the capacitance. As before, the intrinsic resistance of the structures in Fig. 5.11 are calculated to determine if they could in fact produce better bandwidth performance for the modulator. The total intrinsic resistance for the top four plots in Fig. 5.11 are shown in table 5.3.

**Table 5.3:** Total series resistance for original structure along with top two plots of Fig. 5.11

| Structure type | Resistance [Ωcm] |
|---|---|
| Original | 0.43 |
| 60% AlGaAs | 0.52 |
| 80% AlGaAs | 0.62 |
| 50% Cladding Doping | 0.37 |
| 25% Cladding Doping | 0.68 |

It can be seen that the resistance has increased by almost 60% as the Al percentage is increased compared to the original stack design. This is simply due to

the decrease in mobility that occurs as the AlGaAs cladding has more aluminium present. Fundamentally then, given that both the capacitance and resistance increase with increasing aluminium content, it may not be worthwhile designing a modulator with increased Al content in the AlGaAs cladding.

At half the original doping level for the cladding, a decrease in the total intrinsic resistance is observed. Reducing the doping further leads to an increase in the resistance. This trend is due to the balance between the decrease in carrier density with the increase in mobility as doping is reduced to produce an optimum resistance value for the cladding. The results here suggest that introducing a stepped doping profile to the cladding, and halving the doping in the vicinity of the intrinsic region can lead to further reductions to both the intrinsic capacitance and resistance of the prospective modulator.

It is important to note that in addition to improving the RC characteristics, the proposed doping profile in the cladding may also lead to reduced internal losses within the device due to free carrier absorption. Furthermore, the extent at which the doping has been changed in the vicinity of the QD core, although beneficial to its RC characteristics, will have a negligible effect on the modal confinement within the core. This is due to the small variation in real refractive index with doping [95].

The combined improvement to the intrinsic resistance and capacitance would increase the RC-limited bandwidth of the doped modulator by almost 20% over the original design. Finally, the main contribution to the intrinsic resistance comes from the top p-cladding. A simple approach that could drastically reduce the cladding's resistance would be to make the region thinner. It can be seen in Fig. 5.11a that using a 500$nm$ thick top cladding has no effect on the device capacitance. Checking the affect on the modal profile only illustrated a slight decrease in confinement within the QD's, which is supported by [96], where it was shown in MQW devices that the thickness on the upper cladding had significantly less impact on the losses within the device compared to reducing the lower cladding thickness. Taking this into account, the proposed optimised modulator device would incorporate a thinner p-cladding with a graded doping profile. Such an optimised stack is proposed in

Table. 5.4

**Table 5.4:** Layer structure for proposed optimised QD stack.

| Material | Thickness | Type | Repetitions |
|---|---|---|---|
| GaAs | 300 *nm* | P($1 \cdot 10^{19}\, cm^{-3}$) | – |
| GaAs/AlGaAs | 5 *nm* | P($5 \cdot 10^{17}\, cm^{-3}$) | ×10 |
| AlGaAs | 300 *nm* | P($5 \cdot 10^{17}\, cm^{-3}$) | – |
| AlGaAs | 200 *nm* | P($1 \cdot 10^{17}\, cm^{-3}$) | – |
| AlGaAs | 30 *nm* | UID | – |
| GaAs/AlGaAs | 2 *nm* | UID | ×12 |
| **GaAs** | 17.5 *nm* | UID | |
| **GaAs** | 10 *nm* | **P**($5 \cdot 10^{17}\, cm^{-3}$) | |
| **GaAs** | 10 *nm* | UID | |
| **GaAs** | 5 *nm* | UID | |
| **InGaAs** | 5 *nm* | UID | |
| **InAs QD** | 3 *ML* | UID | ×7 |
| **InGaAs** | 2 *nm* | UID | |
| GaAs | 42.5 *nm* | UID | – |
| GaAs/AlGaAs | 2 *nm* | UID | ×12 |
| AlGaAs | 30 *nm* | UID | – |
| AlGaAs | 200 *nm* | N($1 \cdot 10^{18}\, cm^{-3}$) | – |
| AlGaAs | 400 *nm* | N($1.3 \cdot 10^{18}\, cm^{-3}$) | – |
| AlGaAs | 400 *nm* | N($1.7 \cdot 10^{18}\, cm^{-3}$) | – |
| AlGaAs | 400 *nm* | N($2 \cdot 10^{18}\, cm^{-3}$) | – |
| GaAs/AlGaAs | 5 *nm* | N($2 \cdot 10^{18}\, cm^{-3}$) | ×10 |
| GaAs | 200 *nm* | N($2 \cdot 10^{18}\, cm^{-3}$) | – |

## 5.4 Simulating QCSE in InAs QDs

### 5.4.1 Simulation of measured InAs stacks

Up to this point, simulation work has been carried out to optimise the waveguide structure of the modulator. Using the optimised waveguide structure an investigation was then carried out looking into optimising the intrinsic capacitance and resistance of the overall device. Simulations of the carrier density for both measured and altered InAs QD stacks suggest the use of a stepped doping profile in the vicinity of the QD active core. Although this configuration offers a 20% improvement in intrinsic RC-limited bandwidth, it is currently unclear how this modified doping profile in the cladding will affect the QCSE of the device.

In order to see the effect this new doping profile has on the modified device, simulations can be carried out on the stack of interest, and the QCSE shift with voltage observed. However, before this can be carried out there must be some initial investigation to ensure that the model being used to simulate the QCSE in the InAs

QD stacks is reasonable. To do this, a modelling scheme implemented in NextNano by Benjamin Maglio [55; 97] has been adapted here to look at initially simulating the InAs QD stacks measured in chapter 4. Further details on aspects of the model can be found in chapter 3 or for a complete discussion within the aforementioned references.

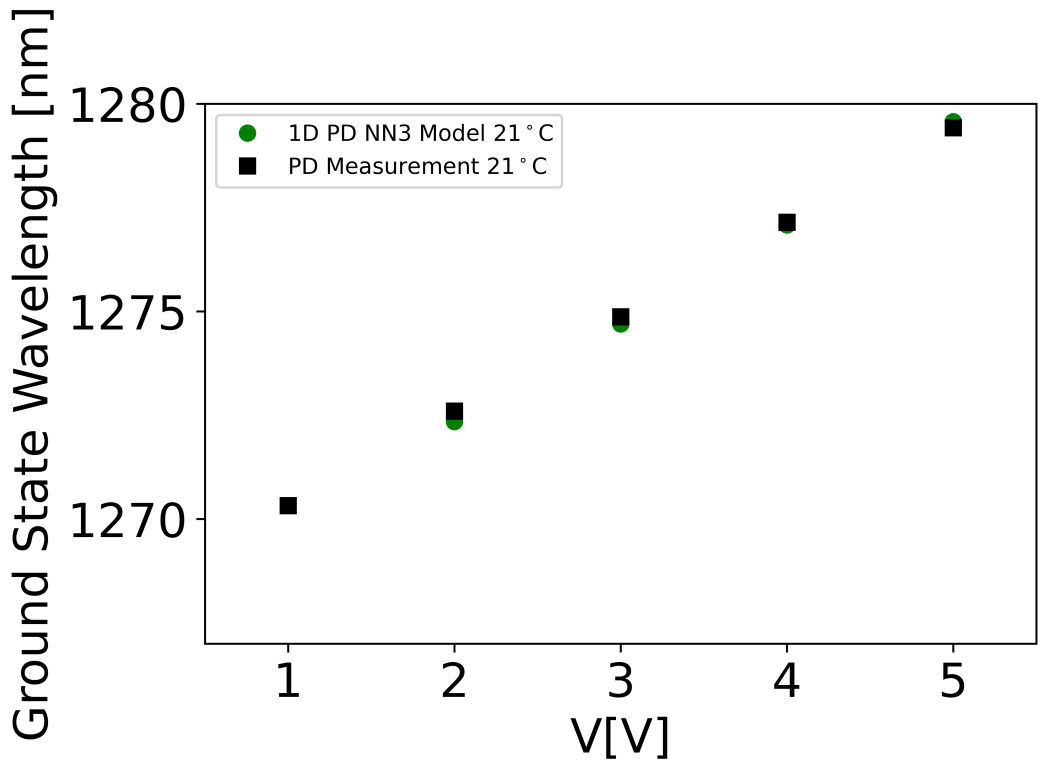


**Figure 5.12:** QCSE shift at room temperature for the measured PD InAs QD stack compared with the QD model implemented in NextNano.

In the simulations of the PD measured stacks, adjustments were made to the 1D simulation space to ensure correct valence and conduction band state separations, as well as ensure the dot density in the doped QD layers corresponded to roughly $5 \cdot 10^{10}\, cm^{-2}$. Comparison between measurement and simulation for the PD QD sample is shown in Fig. 5.12. It is clear that there is very close agreement between the measurement and the simulation up to $5V$. In order to attain this agreement, the carrier blocking effect produced in the simulation had to be taken into account. The carrier blocking effect, as already explained in chapter 4, is essentially the inability of absorption events to occur due to the high probability that the valence state is

filled with a hole. To take this into account in the simulation of the QCSE shift, the QD layer shift is weighted by its corresponding Fermi occupation probability. Additionally, using expressions for QD absorption adapted from [31], the absorption spectra can be approximated from the NextNano simulations and compared to measurements from Chapter 4. Several parameters including the state energy separation and Fermi occupation probability are directly input from NextNano into calculating the absorption spectra. However, broadening parameters due to both homogeneous and in-homogeneous sources are determined by fitting Gaussian profiles directly to measurements and adapting the results for the simulated absorption calculation.

This calculated absorption is shown in Fig. 5.13 for the PD sample and highlights the good agreement between measurement and simulation at $1V$ and $5V$ at the absorption edge. At higher energies than the absorption edge, potential bimodal contributions between the ground state and excited states not accounted for in the simulation may lead to the observed discrepancies between the measurements and simulations. Such bimodal distributions are often observed under high growth temperatures in InAs QDs [98]. Nevertheless, for the QCSE the absorption edge is the most important aspect of the spectra to observe, as this is what directly quantifies the devices modulation potential.

Although the PD InAs QD stack has proven to achieve better *FoM* performance, capacitance calculations in this chapter indicate that UID QDs clearly offer superior bandwidth performance. As a result it is worthwhile simulating the UID QD stack here to not only ensure the model agrees with both the PD and UID QD measurements, but also to enable a clearer understanding of how the PD and UID compare, and if there is any change in the QCSE between the two optimised structures. In Fig. 5.14, the comparison between measured and simulated UID QDs can be seen. As with the PD simulations in Fig. 5.12, there is excellent agreement between the two sets of data. Unlike with the PD simulations, no carrier blocking is present, and so no weighting of each QD layers contribution using Fermi statistics is required. The simulation of the UID QDs validates the model to be used to determine the effect simple modifications to the UID stack has on the QCSE. Much

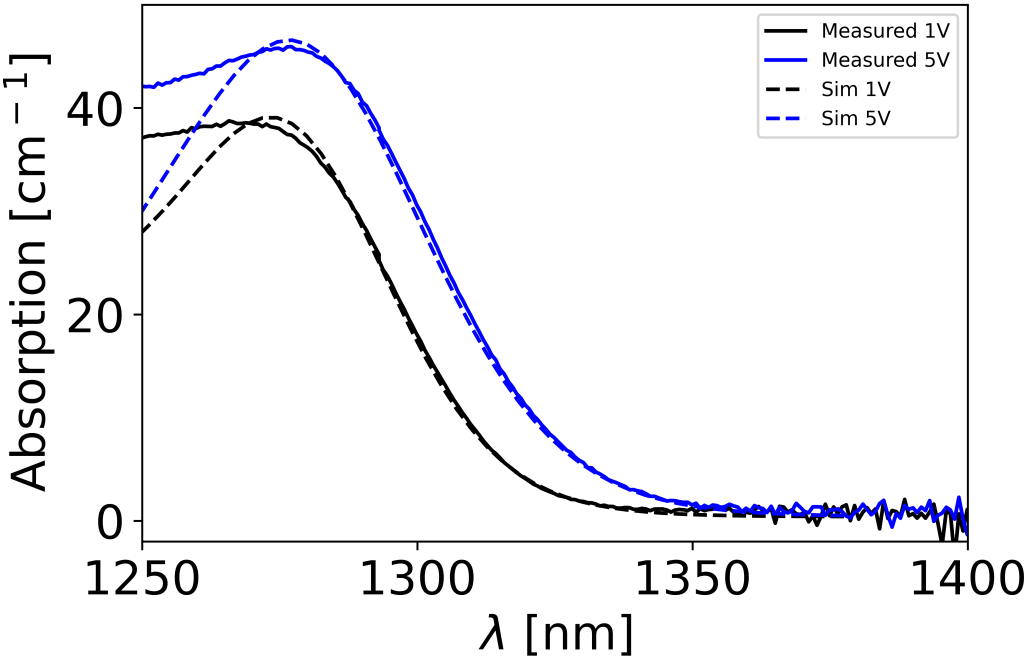


**Figure 5.13:** Measured and simulated QCSE at room temperature for the PD InAs QD stack at $1V$ and $5V$.

like with the PD simulations, approximate calculations of the UID absorption spectra can be obtained, and are shown in Fig. 5.15. The figure highlights the excellent agreement between the measurements of chapter 4 and the simulation at $1V$ and $5V$. It is also noted that for the UID simulations, there is a better fit to the measurement at shorter wavelengths. This is likely due to the difference in bimodal distribution in UID QDs compared to PD QDs.

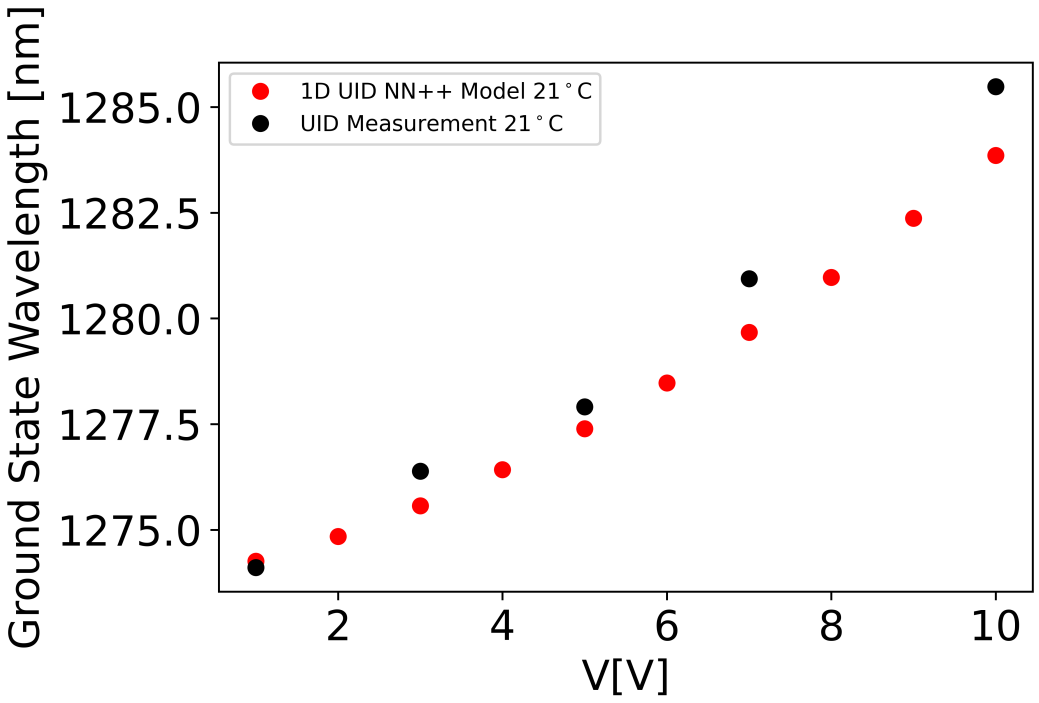


**Figure 5.14:** QCSE shift at room temperature for the measured UID InAs QD stack compared with the QD model implemented in NextNano.

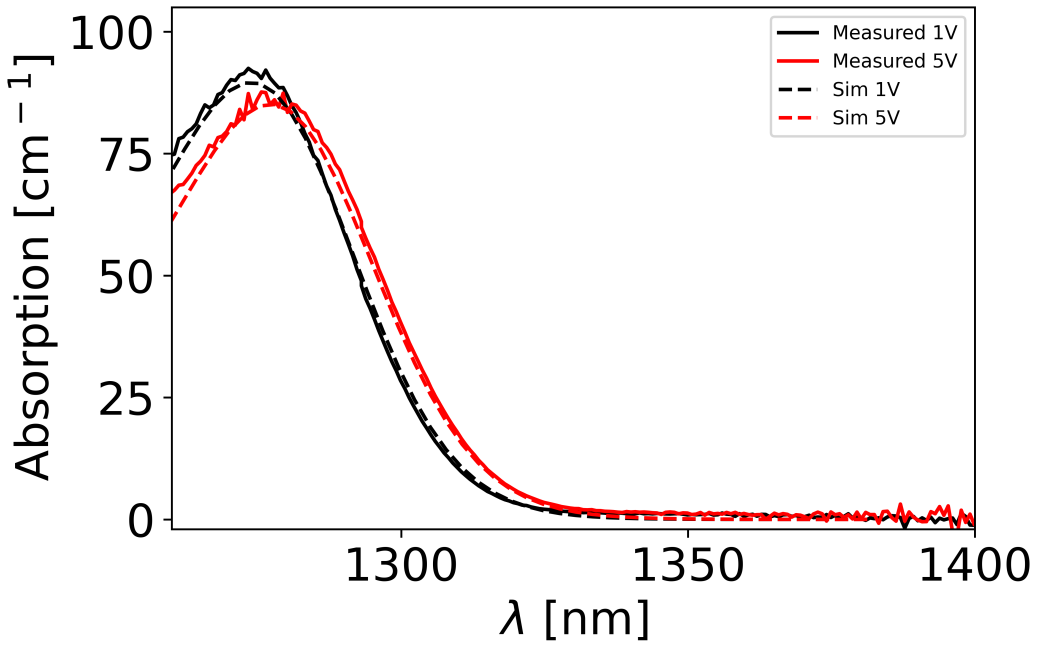


**Figure 5.15:** Measured and simulated QCSE at room temperature for the UID InAs QD stack at $1V$ and $10V$.

### 5.4.2 Simulation of optimised structure QCSE

With initial tests of the QD model in NextNano completed and agreeing well with measurement results, it is possible to start adjusting certain aspects of the stack to see the effect on the QCSE. To help ensure that the model can be deemed as an appropriate approximation of the potential measured QCSE of such a stack, no modifications will be carried out directly to the QD core. The fundamental reason for this is that any modification to the QD core in a fabricated device would directly impact aspects of dot growth and strain. This in turn could effect the QCSE significantly within the core and so may not be approximated in this current model correctly. Thus, this section will concentrate specifically on varying the doping within the cladding of the stack. Capacitance and resistance considerations in earlier sections deemed that reducing the doping in the vicinity of the active core by half yielded the optimum results. Subsequently, such a doping profile will be incorporated into the following PD and UID simulations. This way no changes to the QD core are implemented and so the model's accuracy of the QCSE should be acceptable.

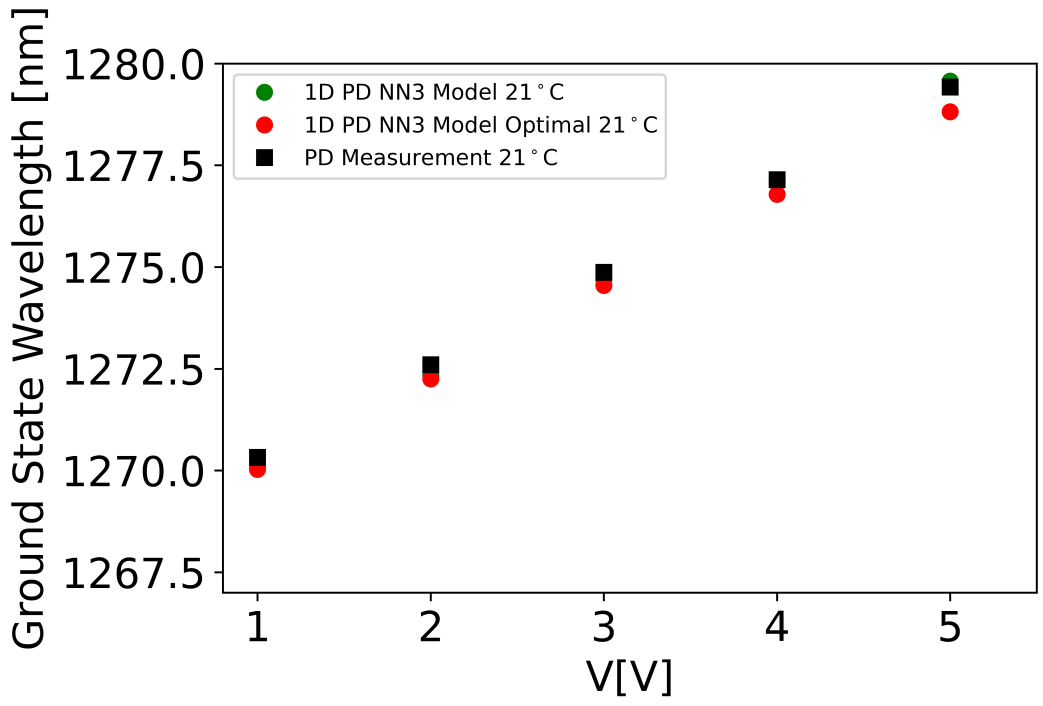


**Figure 5.16:** QCSE shift at room temperature for the optimised PD InAs QD stack using the QD model implemented in NextNano.

First the optimised doping within the cladding is implemented with the PD QD stack. The QCSE of this is seen in Fig. 5.16. The original measured stack and corresponding simulation are also shown in the figure, and, at least at first glance, indicate only a slight reduction in the QCSE shift over a 5$V$ range. To get a clearer picture of the change to the red-shift in the optimised structure, the relative difference in red-shift between the simulated measured and simulated optimised structures are shown in Fig. 5.17. It can be seen that the difference between original and optimised stack increases at higher reverse bias, with the optimised stack having a smaller red-shift at each voltage.

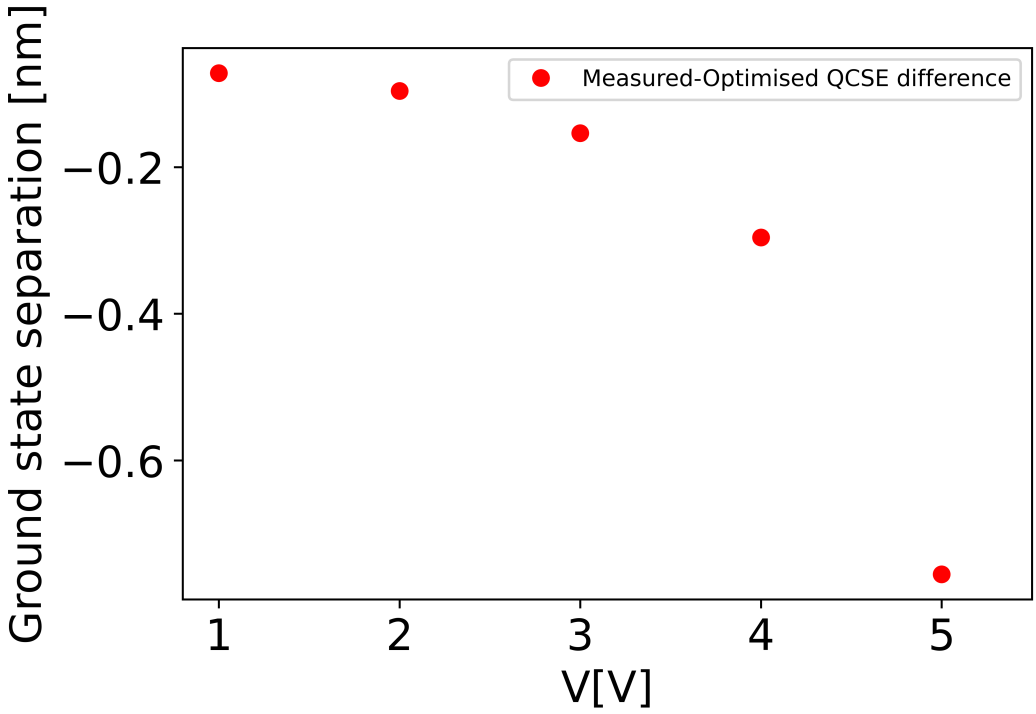


**Figure 5.17:** Relative change in QCSE-induced red-shift between simulated measured and simulated optimised PD InAs QD stacks.

To determine where this decreased red-shift with applied reverse bias comes from, analysis of the valence ground state electron occupation differences between both simulations has been carried out. The Fermi occupation probability for each QD layer for both sets of simulations are shown as a function of reverse bias in Fig. 5.18. It can be seen that the differences between both sets of occupations in the ground valence state are negligible for almost all layers and applied reverse bias.

This suggests that the extent of the shift due to carrier blocking is not significantly different between both stacks. Therefore the difference comes almost entirely from the decreased induced electric field across the optimised stack. This lower electric field is a direct result of the lower doping concentration around the active core, leading to a smaller initial built-in field across the stack.

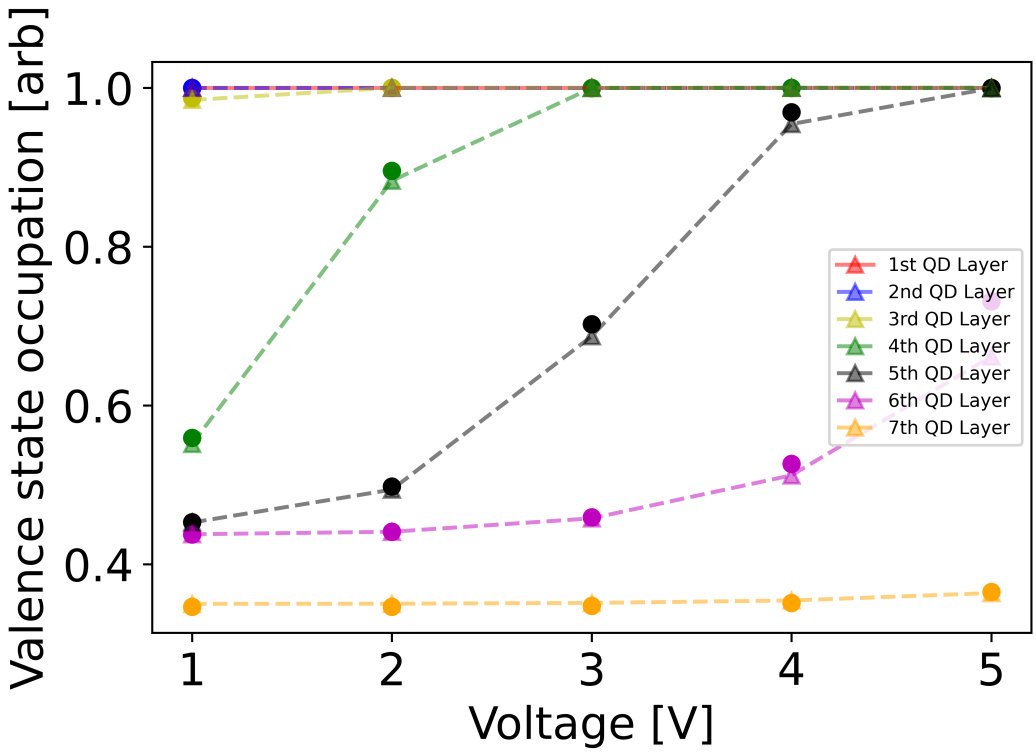


**Figure 5.18:** Comparison of the ground valence state Fermi occupation probability of electrons using the QD model implemented in NextNano. Circles show Fermi occupation for original structure, triangles represent new occupation in optimised structure.

Similar to Fig 5.16, a plot of the differences between the measured and optimised UID simulations are shown in Fig. 5.19. In a similar way it is clear that the shift in the optimised structure is smaller than the original measured stack. This is again shown more clearly in Fig. 5.20. It can be seen that the extent of the change between the measured and optimised structures when UID is greater than the PD equivalent. This is a result of the PD screening that lessens the effect of the reduced built-in static electric field created from the modified doping in the cladding. The results suggest that if modifications are to be made to the QD stack, using PD QDs

will result in smaller impacts on the red-shift whilst still being able to observe the desired benefits in RC-characteristics.

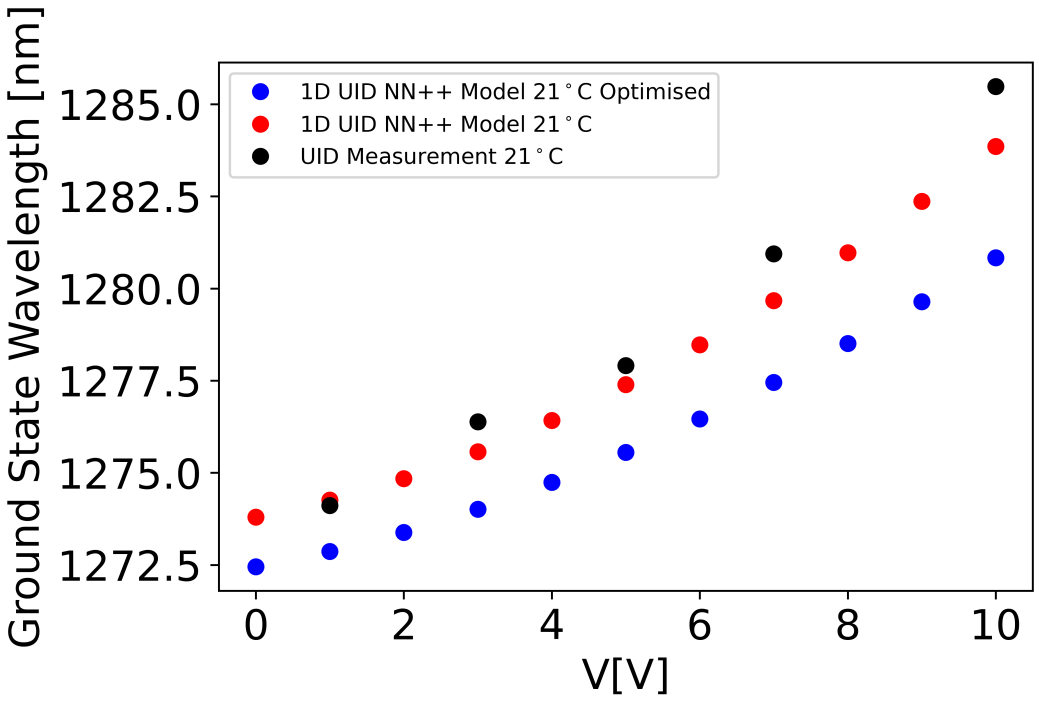


**Figure 5.19:** QCSE shift at room temperature for the optimised UID InAs QD stack using the QD model implemented in NextNano.

Having now calculated the expected C-V characteristics, determined the intrinsic resistance and simulated the QCSE shift of the stepped-doping cladding stack, the results indicate that although the intrinsic capacitance and resistance are in principle significantly lower, the same reasons that cause this improvement lead to a slightly weaker overall QCSE red-shift with applied reverse bias. Although this is the case for both the PD and UID stacks, it should be noted that the effect on the shift is small, decreasing by less than $1nm$ at $5V$ for the optimised PD sample compared to the original measured stack. This is still a larger shift than what is possible in the nominally identical UID stack, and so would still produce markedly larger *FoM* performance. To emphasise this, the measured PD *FoM* is compared against both the original simulated structure as well as the optimised configuration, shown in Fig. 5.21. The figure highlights the good agreement between measurement and simulation, as suspected from Fig. 5.13. It also shows only a small reduction in

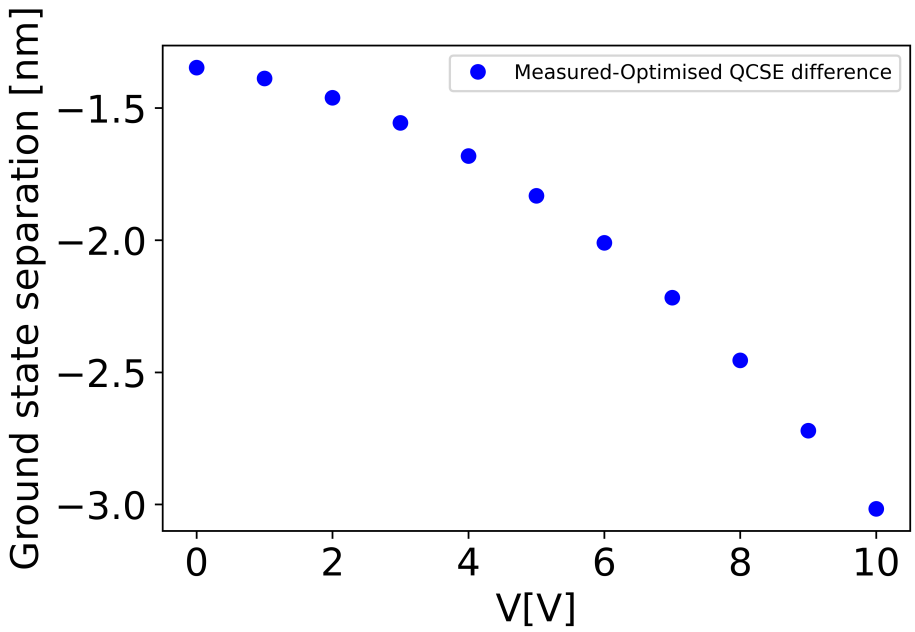


**Figure 5.20:** Relative change in QCSE-induced red-shift between simulated measured and optimised UID InAs QD stacks.

peak *FoM* in the optimised structure. However, as explained previously in chapter 4, the optimal *FoM* that would be used in practice is unlikely to be the peak value, and so in principle the discrepancy in performance between the measured and optimised structure would be even smaller. Subsequently, the use of reduced doping in the vicinity of the active cladding, as done here, can lead to an optimised QD modulator with improved RC characteristics without jeopardising the raw modulation performance.

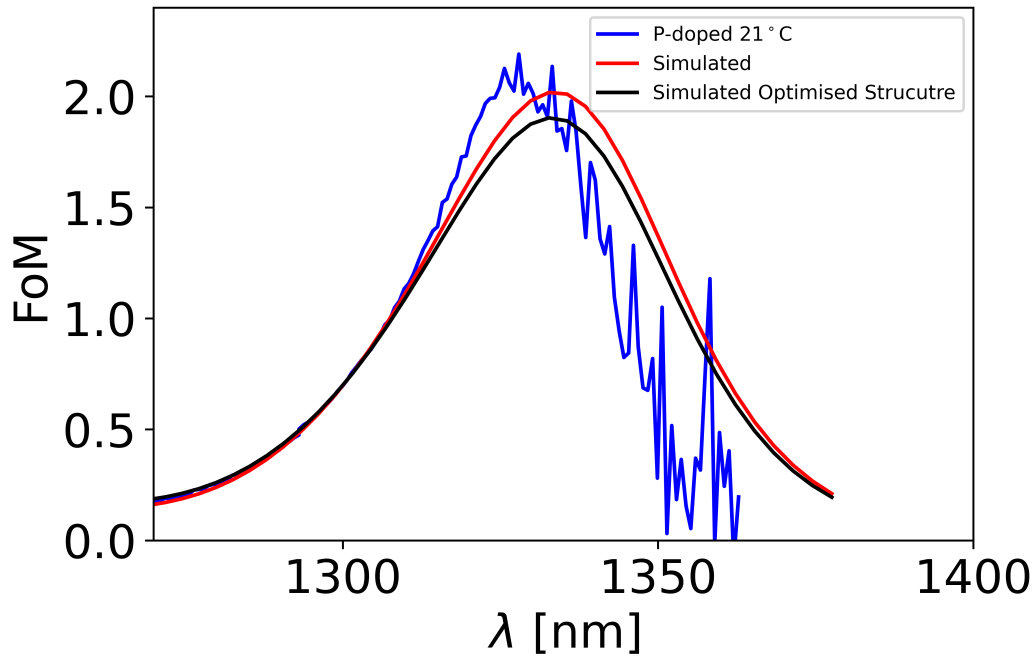


**Figure 5.21:** *FoM* of measured PD QD stack (blue) compared with simulated equivalent (red) and optimised structure (black) at 21 °*C*

## 5.5 Total internal reflection coupling simulations

Up to now the discussion has focused on different ways to optimise the active core of the QD modulator. In this section an approach to coupling the light will be investigated. In pariticular, we will use total internal reflection (TIR) technique to couple the light vertically from the passive waveguide below to the active region above it over a short distance. A simple illustration of the structure is shown in Fig. 5.22. The design is based on a concept from VTT [99].

The silicon waveguide used here will be a strip waveguide of $2 \times 3\ \mu m^2$ dimensions. Although this is larger than the nanoscale waveguides typically sought after, it has been shown that using such a design can offer numerous benefits. Although strip waveguides of such dimensions are not typically single mode operation, it has been shown through the use of tapering down from rib to strip waveguides that there is very limited excitation of higher modes in the process [100; 101]. This feature essentially creates the opportunity to use strip waveguides under strictly single mode operation.

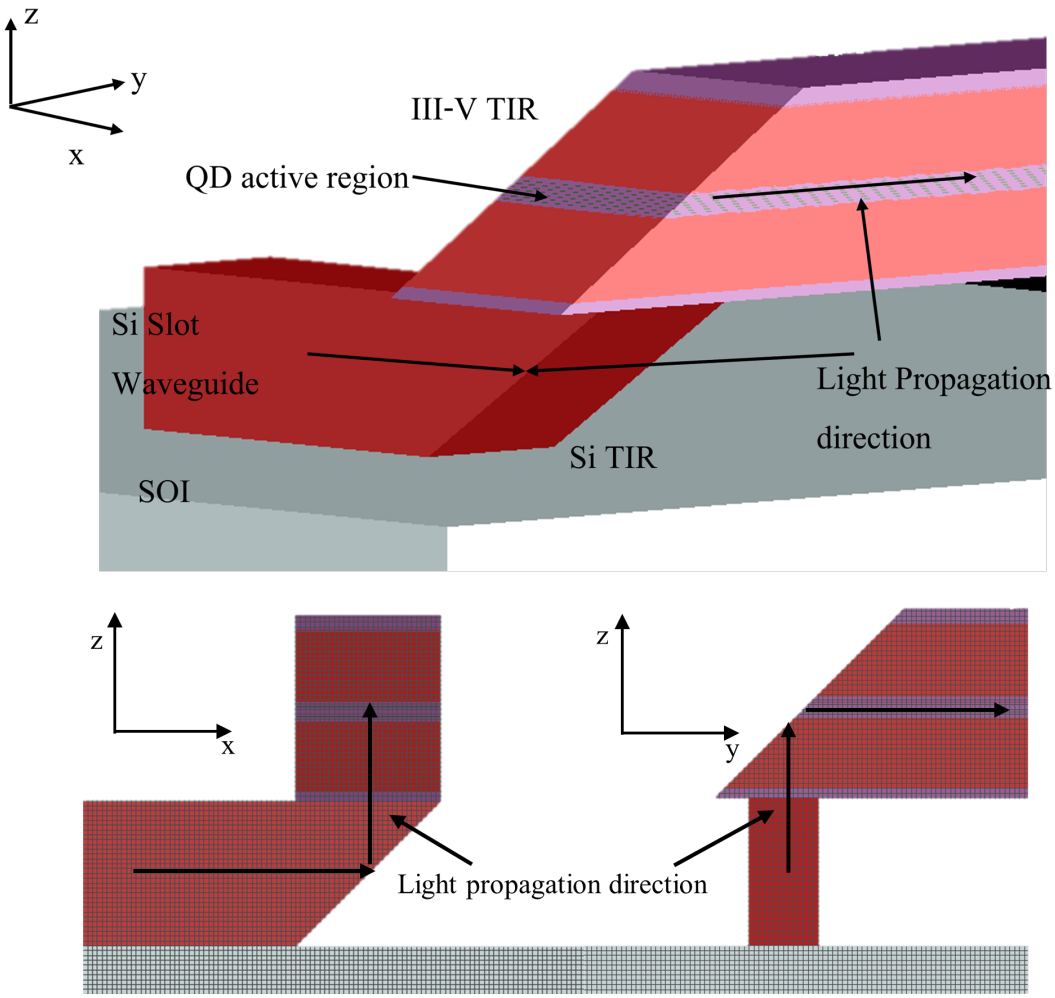


**Figure 5.22:** (Top) Perspective view of device design for coupling technique using total internal reflection mirrors. (Bottom left) cross-section of device in x-z plane with corresponding direction of light propagation. (Bottom right) cross-section of device in y-z plane with corresponding direction of light propagation.

The single mode operation in rib waveguides stems from the radiation of higher order modes into the Si slab below and to the sides of the rib. This radiative loss does not occur in strip waveguides, which enables the potential of much greater levels of integration density. In addition to the lower radiative loss, rib waveguides offer single mode operation over a very large wavelength range, covering the entire communication wavelength band. This large bandwidth of operation opens up strong possibilities to enable significant wavelength division multiplexing. As well as the large operation bandwidth, the larger dimensions used for these waveguides

enables significantly reduced losses compared to nanoscale equivalents due to the almost total confinement of the mode in the waveguide core. This section will consider the prospect of possible passive-active coupling using TIR mirrors. The active III-V device and Si waveguide are considered to be directly bonded together, through a process such as $O_2$ plasma bonding. The Si TIR mirror will use a $45^o$ angle to achieve right angled changes in direction. This is fairly readily achievable in such materials [102]. The active TIR will also in the first instance use an angle of $45^o$. Although not as readily achievable, it has been demonstrated to be repeatedly produced [103] using dry-etching techniques. Finally, a different crystal orientation to produce a plane angle of $55^o$ to the horizontal for the active TIR is investigated to see the effect on coupling efficiency. This angle is studied as it is generally easier to etch in AlGaAs. In all instances, the active section has a width of 3μm. Simulations are carried out using a full 3D finite-difference time-domain method (FDTD) model using Lumerical software.

### 5.5.1 $45^o$ III-V TIR

First the coupling into the active region using purely $45^o$ TIR for both waveguides is investigated using a bonding approach for passive-active integration. Fig. 5.23 shows the modal overlap between the TE III-V mode expected in the active region with the mode that gets coupled into the core after coming from the Si waveguide and passing through the TIR's. The plot shows the variation in the overlap as a function of the edge of the active TIR in the y-axis direction with respect to the centre of the Si TIR waveguide. For each variation looked at in Fig. 5.23, the position of the active TIR effects the potential modal overlap of the final coupled mode. This observation is due to the fact that the mode will get reflected at different points along the TIR by $90^o$ depending on how much the active TIR is offset in the y-axis. It can be seen that for all the variations in the figure, optimal overlap is achieved with a lateral shift of the active TIR edge by approximately 1.7μm from the centre of the Si waveguide.

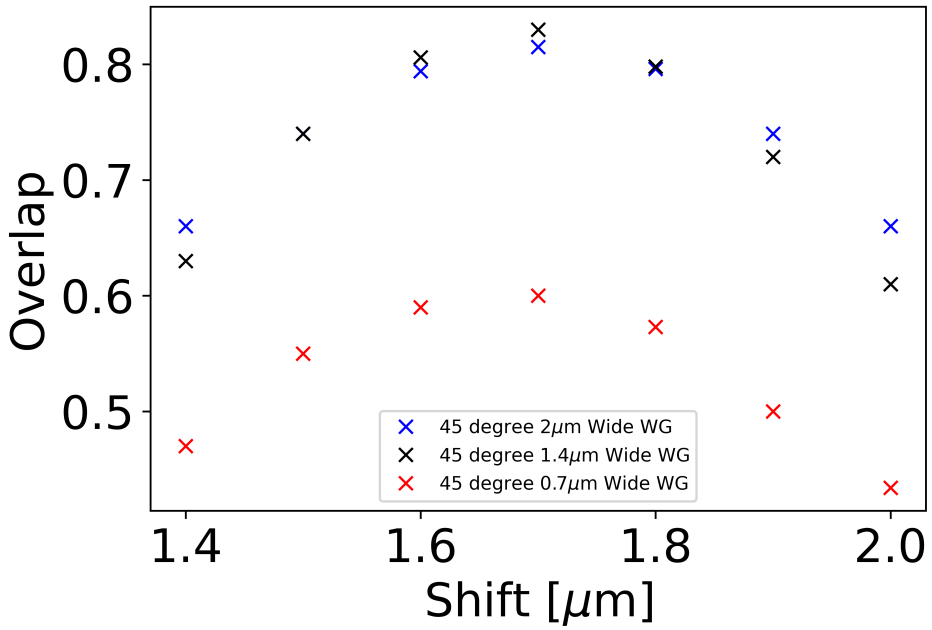


**Figure 5.23:** Overlap between coupled and III-V TE mode expected via the 45° TIR as a function of active TIR position in the y-axis.

There are different maximum values for the overlap depending on the width of the Si waveguide. Given the size of the strip Si waveguide used, achieving an exactly matching effective index with the active core is not readily achievable. Although minimizing this difference is important, the modal spot size is also an important factor to consider. The width of 3µm in the active region has been used to match the size of the Si TIR, which is dictated by the Si waveguides thickness. However, the Si waveguide width has the potential to be adjusted more freely. In principle to match the spot size of the desired active mode, the Si waveguide would need to be in the order of 100's of nm wide, as the QD active region is approximately 400nm thick. It can be seen however, when using a 700nm wide Si waveguide, the overlap decreases quite significantly compared to other variations. When looking further into the simulation it was found that upon entering the active TIR, the mode diffracts considerably, which is what has caused the observed reduction. However, in principle the need to reduce the mismatch in modal spot size is illustrated when looking at the overlap of the 1.4µm wide Si waveguide. It can be seen that the maximum overlap is achieved for this structure configuration.

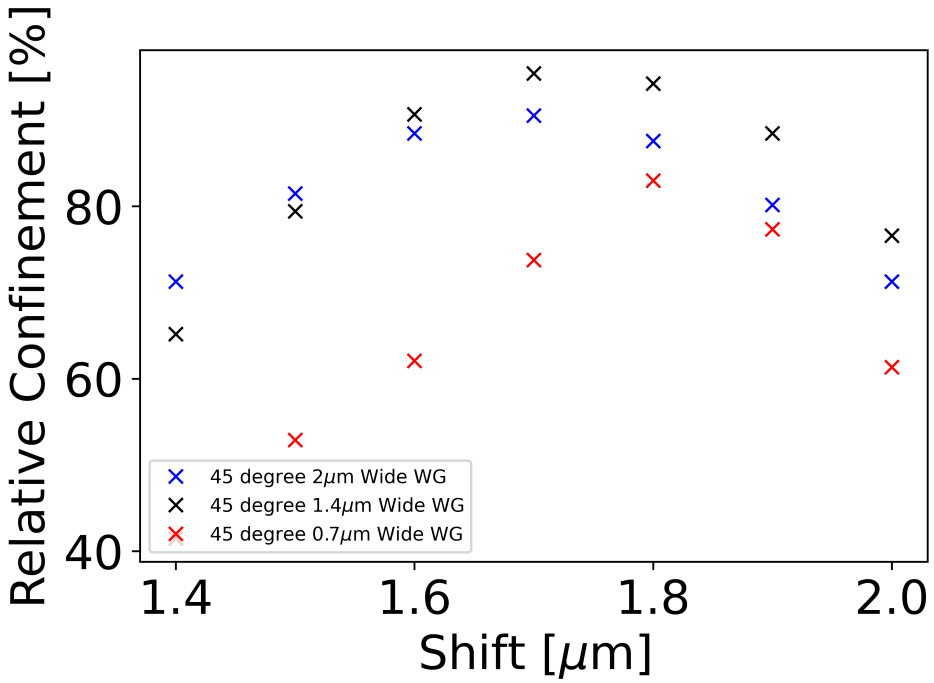


**Figure 5.24:** Proportion of power coupled to the active region via the 45° TIR relative to the simulated maximum active region power as a function of active TIR position in the y-axis.

The simulations also output the power within key sections of the design, including the final couple power into the QD core. Fig. 5.24 shows the relative power coupled to the active core with respect to the simulated maximum confinement of the exact mode of the core for the same parameters. For the 1.4µm width variation, up to 95% of the potential power has been confined to the active core of the modulator at a shift of 1.7µm from the centre of the Si waveguide. From Fig. 5.23 and Fig. 5.24 it can be seen that for the 1.4µm width variation, the exact position of the active core in the y-axis has some degree of freedom, as both the overlap and power remain above 70% and 80% respectively over an approximately 500nm range in y-axis shift of the active TIR.

### 5.5.2 55° III-V TIR

The next variation looked at here uses the (111) crystal plane angle with respect to the (100) plane of roughly 55° for the TIR. It is clear from the results in Fig. 5.25 that the overlap, and by extension the coupled power into the active core as seen

in Fig. 5.26, are severely diminished. This is fundamentally due to the fact that the active TIR is now reflecting at an angle of 110$^{o}$ as opposed to 90$^{o}$. This means the light coupled into the QD modulator is naturally not completely parallel to the plane of the active core. As a result of this, the coupled mode when using a 55$^{o}$ TIR dispersed over a larger area of the waveguide. This is shown more clearly in Fig. 5.27, where it can be seen that the coupled mode into the III-V waveguide is spread significantly over both the n and p-cladding's when using a 55$^{o}$ TIR. Despite the improving the spot size mismatch improving the overlap as in Fig. 5.23, the overlap with the desired TE mode within the III-V stack is still roughly eight times smaller than the bonded integration using 45$^{o}$ TIR's.

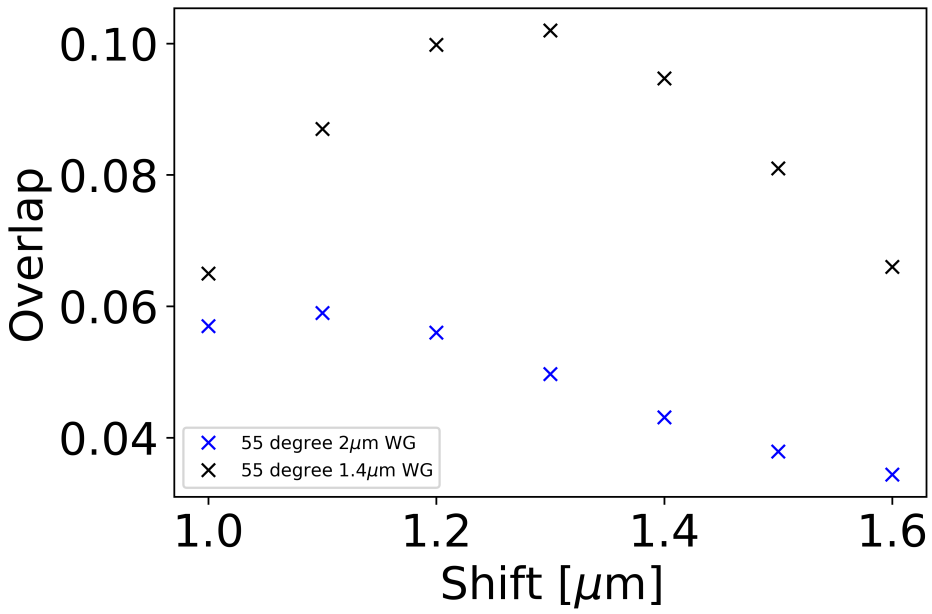


**Figure 5.25:** Overlap between coupled and III-V TE mode expected via the 55$^{o}$ TIR as a function of active TIR position in the y-axis.

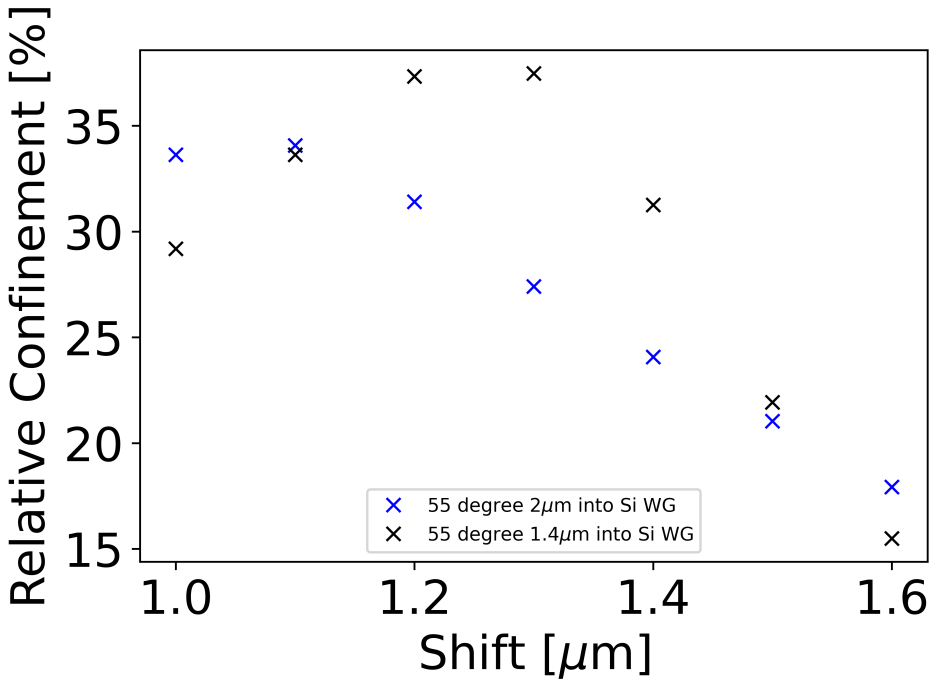


**Figure 5.26:** Proportion of power coupled to the active region via the 55° TIR relative to the simulated maximum active region power as a function of active TIR position in the y-axis.

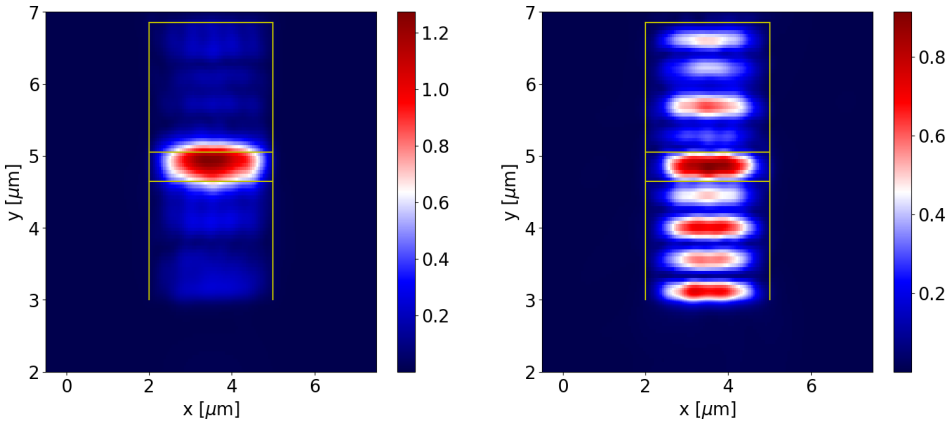


**Figure 5.27:** Coupled mode profile using 45° TIR with 1.4µm width Si waveguide (left) and mode profile of 55° TIR (right). Yellow outline indicates relative position of III-V waveguide.

### 5.5.3 Effect of TIR alignment on optimal coupler configuration

Having looked at both 45° and 55° TIR coupling prospects, it is clear that using 45° TIR mirrors offers superior coupling efficiency. Although previous sections looked into the effect of the position of the active TIR in the y-direction with respect to the

centre of the Si waveguide, no dependence on the shift in x-axis was considered. Here a more in-depth study of the tolerance to misalignment is investigated for the 45° TIR using a 1.4µm width Si waveguide.

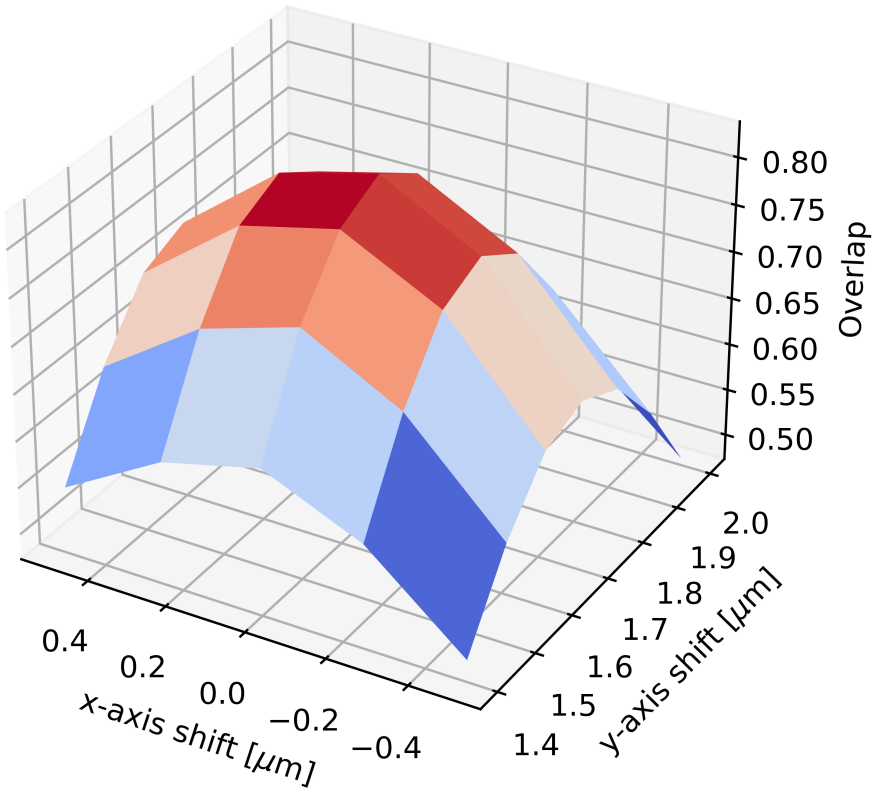


**Figure 5.28:** Variation in overlap of the coupled TE mode compared to the expected III-V TE mode profile using 45° TIR with 1.4µm width Si waveguide as a function of both shift in x and y axes.

The variation of the overlap between the coupled TE mode and expected III-V TE mode profile as a function of both x and y-axis shift is presented in Fig. 5.28. It can be seen that the overlap value does not vary as much with respect to x-axis shift compared to the change with y-axis shift, remaining fairly unchanged with shifts of plus or minus 500nm. The maximum variation in overlap for a particular shift was found to be around 15% from the maximum value at x = 0µm. In a similar fashion, the relative confinement of the TE mode within the QD core is shown in Fig. 5.29 and follows a similar pattern, with a maximum variation of around 5%.

The results here suggest that an alignment tolerance of around $\pm 250nm$ in the y-axis and $\pm 300nm$ in the x-axis without the relative confinement of the TE mode within the QD core or overlap dropping below 80% and $\sim$ 70% respectively. Using more sophisticated photo lithography tools, such tolerances are readily attainable in such a device.

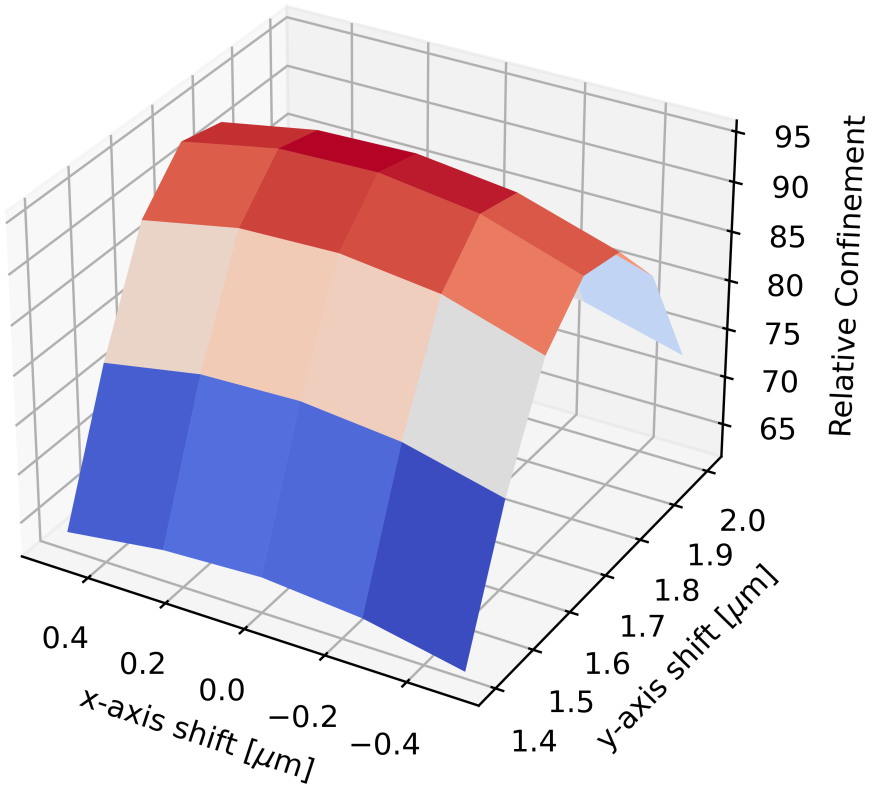


**Figure 5.29:** Variation in relative confinement of the TE mode within the active QD core using 45° TIR with 1.4μm width Si waveguide as a function of both shift in x and y axes.

### 5.5.4 Coupling from III-V to Si waveguide

The final part of this analysis will briefly look into the prospect of reversing the coupling direction i.e. coupling the light from the III-V active core to the Si waveguide underneath. This will be needed if for example the modulator and laser are integrated together as suggested in chapter 4. As the light goes through two right-angled turns in different directions, the coupled light into the Si waveguide would

be TM if modulated light from the III-V active material is TE polarised. The overlap and relative confinement of the coupled TM Si mode compared to the expected TM mode profile using 45° TIR with 1.4µm width Si waveguide as a function of shift in y-axis position is shown in Figs. 5.30 and 5.31 respectively. The trend seen in both graphs are very similar to that shown in section 5.5.1. However it is noted that both the overlap and relative confinement within the Si waveguide are generally larger over the whole shift range in the y-axis. This is attributed to Si waveguides superior refractive index contrast. The greater refractive index contrast offers better modal confinement. Additionally, unlike in previous sections where the desired active mode is confined within a small QD core, here the coupled mode is coupled into the whole Si waveguide which is much larger in area. This helps enable a greater tolerance in coupling efficiency over the whole range of shifts in the active TIR. Subsequently then the use of TIR mirrors is considered a potentially viable approach to efficiently coupling light to or from the QD stack.

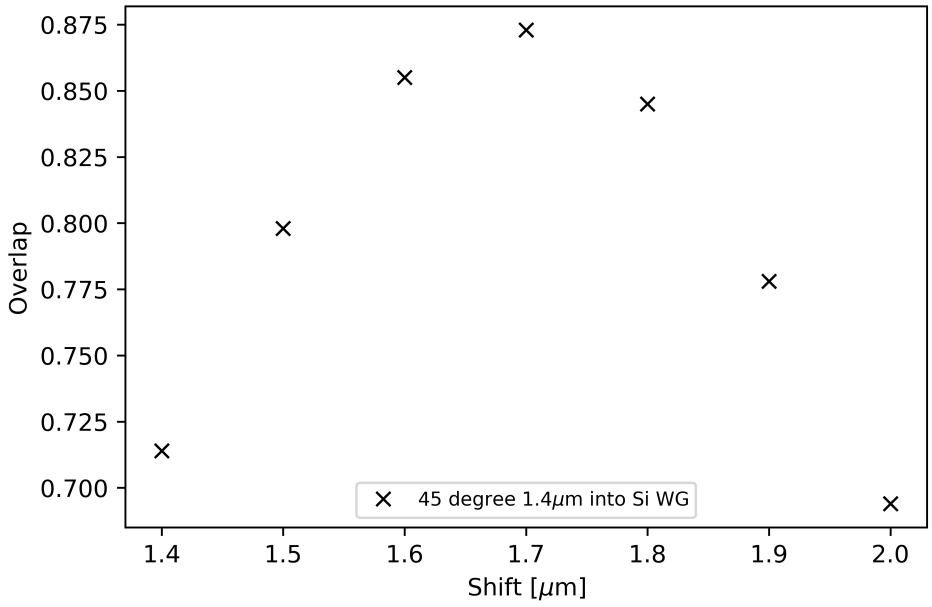


**Figure 5.30:** Variation in overlap of the coupled TM Si mode compared to expected TM mode profile using 45° TIR with 1.4µm width Si waveguide as a function of y-axis shift.

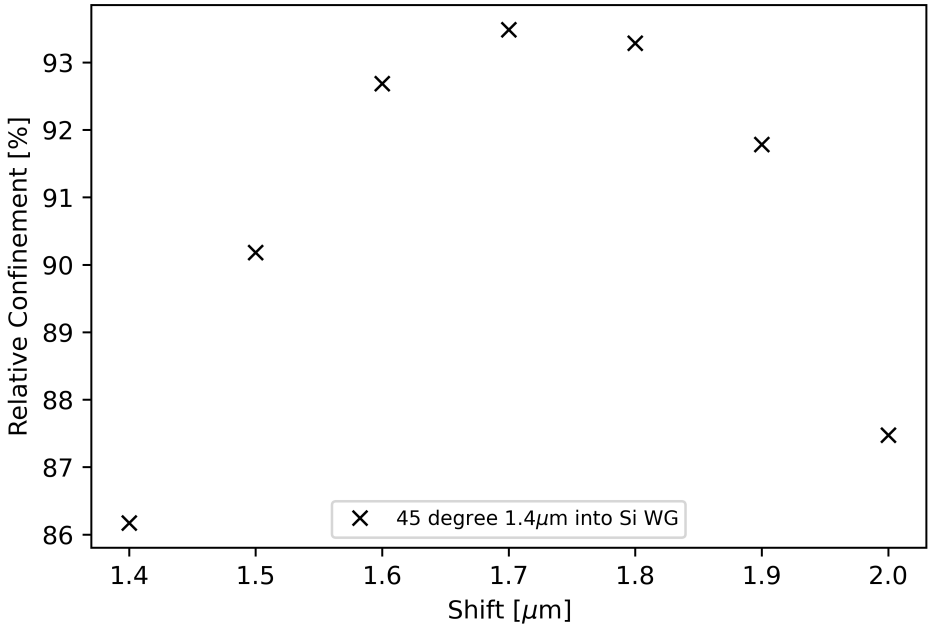


**Figure 5.31:** Variation in relative confinement of the coupled TM Si mode compared to expected profile using 45° TIR with 1.4µm width Si waveguide as a function of y-axis shift.

## 5.6 Chapter summary

The work presented in this chapter has focused on using various simulation techniques to try and further optimise the QD structure in Chapter 4. As the device measured in that chapter was not laterally waveguided, work in this chapter sought to determine both the single-mode waveguide regime as well as look to optimise the overlap integral between the modal field and the induced electric field in the QD active region. Single-mode operation was obtained using waveguide widths of less than 1.4µm. Using this as the upper width limit of the waveguide, overlap between modal and electric fields were found between 1µm and 1.4µm. In order to optimise the overlap integral, a deep etch waveguide design was chosen to inhibit mode leakage below the QD active region.

Once a waveguide width and etch depth were chosen, simulations using NextNano software were implemented to determine the capacitance of the prospective modulator devices using p-doped and undoped stacks. Carrier densities were calculated and used to determine the intrinsic capacitance as a function of reverse

bias. Due to the increased carrier density and subsequent narrower intrinsic region in the p-doped samples, the capacitance was over twice as large in p-doped results compared to undoped with temperature. If parasitic capacitance caused by elements such as wire bonding are considered, there was good agreement between the results here and similar measured QD stacks in the literature. In addition, intrinsic resistance was determined using an empirical formula, that produces accurate mobility values compared to the literature. The p-doped cladding was found to be the main contributor towards intrinsic resistance, though even this contribution would be reasonably small compared to external electrode resistance in a real device.

With capacitance and resistance determined for the original measured stacks, simulations of the p-doped and undoped active regions were carried out varying aspects such as the cladding doping, cladding aluminium content as well as the number of QD layers to get an understanding of the effect on both capacitance and resistance. Increasing the aluminium content in the cladding layers had very little effect on the capacitance of the device, though did increase the resistance of the modulator by a noticeable amount. Decreasing the doping in the cladding near the active region by 50% led to reductions in both capacitance and resistance. However any further reduction only improved capacitance, with resistance of the device beginning to rise again due to the balance between carrier density and mobility. For the undoped sample, when increasing the number of QD layers the capacitance reduced as expected. However in the p-doped case the capacitance did not change with number of QD layers, highlighting the significant contribution the modulation doping was having on the increased capacitance of the material.

With the simulations of capacitance using a graded doping profile in the cladding suggesting optimal RC characteristics, an understanding of the effect such changes would have on the QCSE was required. Simulations of the QCSE for the PD and UID optimised cladding suggested that the red-shift was slightly reduced when using graded doping profiles. Despite this, it was demonstrated that the reduced red-shift in PD QD simulations had a negligible effect on the *FoM* performance. On balance the results suggest the use of a graded doping profile in the

cladding can lead to enhanced RC characteristics without jeopardising raw modulation performance.

The work into coupling light from a passive Si waveguide into the active III-V material utilised total internal reflection mirrors to allow for efficient, compact coupling of the light. Simulations produced using 3D FDTD found that the optimised system involved using 45 $^\circ$ angled TIR's for both the active and passive sections. An investigation into the effect misalignment of the TIR's in both the x and y-axis on coupling performance showed a reasonable degree of tolerance to both the overlap and relative confinement within the QD core compared to the expected mode profile. Using the (111) crystal plane of the active material to produce a TIR angle of 55 $^\circ$ led to severe decreases in both final coupled power and modal overlap with the desired output mode. The large drop off in coupling efficiency highlights the importance of ensuring correct crystal orientation is used to achieve the desired 45 $^\circ$ TIR's.

# Chapter 6

# Conclusions and future work

## 6.1 Conclusions

This work has focused on the development and optimisation of quantum dot electroabsorption modulators. With the continuing need to find the technology capable of handling future data and telecommunication demands, the ability to determine the most feasible route in reaching these goals is paramount. QD lasers have shown remarkable and rapid results over the years; to achieve as high an integration density as possible in any prospective photonic integrated circuit, the logical idea would be to use common QDs for other active components within the PIC. This idea is a key reason why this work was established, to allow a clearer understanding of the feasibility of using QDs as a viable EAM.

To achieve modulation in the prospective devices, the QCSE was studied. In order to measure the QCSE in the QD stacks, the segmented contact technique was utilised. Various aspects of the measurement setup were optimised prior to measuring the stacks to ensure as low a SNR as possible was achieved. These modifications involved ensuring the maximum intensity range was utilised from the camera whilst remaining in its linear range, as well as adding an absorption-only mode to the kit to maximise signal strength of the ASE when measuring the QD stacks for absorption only. These modifications are outlined in chapter 3 but aided in obtaining the results found within chapter 4.

Chapter 4 focused on measurement characterisation of InAs QD devices. The

study investigated the difference in QCSE performance in two sets of nominally identical InAs QD stacks. The only difference between both sets was that one was left unintentionally doped, whilst the other set had p-modulation doping within the QD barriers. The doping concentration in the PD QD sample was approximately given to be 10 holes per dot.

Measurements of the red-shift under reverse bias for the UID and PD QD stacks showed that, irrespective of temperature and voltage swing, the PD stack consistently had a larger shift in absorption edge than the UID equivalent. In addition to this, it was observed that the PD absorption peak, which was initially significantly smaller than the UID equivalent, increased with reverse bias. This observation was in opposition with the UID absorption peak, which decreased in an expected fashion with reverse bias due to the reduction in electron and hole wavefunction overlap.

These observations stem from the inherent carrier blocking effect present in the PD QD stacks. With the top valence states occupied by holes, the absorption peak is initially quenched when compared to the UID equivalent. As the reverse bias is applied, so holes are swept from the valence states, enabling more absorption events to occur, thus increasing the absorption strength despite the reduction in wavefunction overlap that is inherently present due to the QCSE.

Likewise the enhanced red-shift in the PD samples also come from carrier blocking effects. As the holes are swept out of the valence states, so lower energy transitions become more prevalent, adding to the observed red-shift already present due to the QCSE. In addition the QCSE itself is also stronger in the PD sample due to carrier blocking effects. Within the larger p-i-n diode, the majority of QD layers in the PD stack are initially flat band. Any QD layers within the inherently thinner depletion region naturally have a significantly larger electric field across them. This larger initial field leads to a stronger QCSE at subsequent reverse biases.

As the enhancements found in the PD stack are almost exclusively due to the carrier-blocking effect, one would expect temperature dependence on the strength of its contribution toward the enhancements due to the inherently small level separation of heavy holes within the QDs. This is observed in the measurements, where the

rate of red-shift and increase in absorption strength are weaker at higher temperatures, and much more obvious at lower temperatures. Although the PD outperforms the UID at all temperatures measured, the clear enhancement at low temperature strongly suggest the potential for such PD QD EAMs to be used in applications where there could be low ambient temperatures such as in aerospace applications.

The enhanced red-shift and increase in absorption strength with reverse bias led to a significant improvement in the industry-standard *FoM* compared to the UID QD stack. This *FoM* in the PD QD stack actually went beyond the current literature state-of-the-art, strongly suggesting the potential for PD QDs to be used in next-generation PICs.

The final section of chapter 4 looked into the prospect of using the same epistructure for both lasing and modulation. Using the measurements of the QCSE, and comparing the gain characteristics of the same PD QD stack, it was shown that, providing the QD DFB laser can be tuned appropriately, optimum modulator performance can be achieved in the QD stack whilst simultaneously achieving enough gain to overcome threshold, including any mirror loss for a 3mm laser. This result opens up the opportunity to enable increased integration density of photonic devices on next-generation PICs.

Whilst chapter 4 looked into measuring InAs QD stacks for modulation purposes, chapter 5 aimed at further optimising the QD stack in other key performance parameters. To start, the single-mode operation regime was established for a waveguided device. From there, a study into optimising waveguide geometry was carried out by investigating the overlap integral between the TE modal field and static electric field induced in the QD core. By having deep etched waveguides, mode leakage into the lower cladding could be greatly reduced, enabling stronger overlap between the two fields. Having a high overlap is important to ensure that the QCSE in the QD core is as strong as possible for modulation.

A large part of chapter 5 looked at the capacitance and resistance characteristics of the QD stacks. Initial simulations of the carrier densities in the measured PD and UID QD stacks were carried out. Output capacitance was found to agree

with similar measured QD stacks in the literature accounting for parasitic contributions. The PD QD stack exhibited a larger intrinsic capacitance than the UID stack due to the reduced depletion region width brought on by the carrier blocking effect, the same main reason why the PD stack was better in terms of *FoM* in the previous chapter. Despite a larger capacitance, in principle, leading to lower modulation bandwidth and increased energy consumption, the enhanced *FoM* performance in PD meant that, when considering device length, the shorter device lengths needed for the PD modulator would decrease the discrepancy between it and the UID equivalent. Resistance was determined using a previously developed phenomenological model to take into account doping in the cladding layers. As both stacks were identical in this regard, the resistance was the same for both PD and UID stacks.

Various modifications were made to the QD stacks to determine if the intrinsic resistance and capacitance could be reduced. Increasing Al content in the p and n-claddings led to increased intrinsic capacitance and more substantial increase in resistance. Likewise increasing the number of QD layers, at least in the UID stack, would lead to wider depletion regions and lower capacitance. Although desirable, this would lead to larger voltage swings required in practice and so would take them further away from actually becoming viable as a practical device. In the PD stack increasing the number of QD layers had little impact on capacitance. This was a direct result of the impact the doping layers had on the initial depletion region width. Finally a stepped doping profile within the cladding layers was proposed, that demonstrated that both intrinsic capacitance and resistance could be reduced by as much as 20% if doping close to the active core was reduced by a factor of half compared to the original measured stacks to a value of $1 \cdot 10^{17}\, cm^{-3}$. The intrinsic resistance could actually be reduced even further by making the p-cladding thinner, as this was the component that had the most significant impact on the total resistance. Provided the cladding layer thickness is not reduced too greatly, this would have a negligible effect on the modal confinement within the QD core, and so would have little direct effect on the potential QCSE of the optimised device.

The next stage of the optimisation was to see how the stepped doping profile

would effect the QCSE of the modulator, as although such a structure improved RC characteristics, it was unclear how the QCSE would be effected. Initial simulations of the measured stacks were carried out to determine the feasibility of the QD model simulation. For both UID and PD QD stacks good agreement was found between the simulations and measurements. In the PD case, the Fermi occupation of valence state electrons was used as a weighting for each QD layer to allow the carrier-blocking effect to be accounted for in the simulated shift. Using the QD model to simulate the stepped doping structure, it was found that there was a slight decrease in red-shift compared to the original stack. In the PD sample an in-depth comparison was carried out to determine the origins of this difference. As the carrier blocking contributions from both sets of simulations were almost identical, the difference in red-shift was deemed to be solely from the QCSE. This difference in QCSE shift stems from the weaker electric field induced across the QD core as a direct result of the slightly lower doping in the vicinity of the core. The decrease in red-shift in the PD graded-cladding QD stack however was not large enough to discredit the use of such a structure, and was therefore deemed optimal in comparison to the original stack.

## 6.2 Future Work

There are various possible avenues for investigation that can be explored from this work. Chapter 4 showed the benefits of p-modulation doping for both a laser and a modulator, as well as the prospect of integrating two such devices together without heavily compromising performance. The development of an electroabsorption-modulated-laser using a simplified fabrication process can be carried out to directly measure the potential performance in a practical situation. As mentioned in chapter 4, CW operation of the laser could actually lead to less of a trade-off between the laser and modulator performance. Fabricating such a structure would lead to the further verification of the viability QDs can have on increased integration in next-generation PIC's.

Work carried out looking into co-doping QDs using p-type modulation dop-

ing and n-doping has recently shown promising results for lower threshold current densities and improved temperature sensitivity compared to undoped laser performance [104]. An interesting avenue that could be explored would be to determine the QCSE and by extension *FoM* of such a co-doped QD device. In a similar vein to that shown in chapter 4, the feasibility of using a co-doped epistructure for both lasing and modulation could be investigated. A similar study using only n-doped QDs could also be explored, as n-doping in isolation has also shown benefits for QD laser performance [80], though no investigation of its effect on the QCSE has been presented. It is envisaged that the carrier blocking benefits observed in the p-doped devices of this work would also be present to some extent in n-doped equivalents.

Chapter 5 focused on the optimization of the QD stack and overall waveguide design through simulation work. Although all the initial simulation work on the QCSE and capacitance were either verified by comparing to measurements in the preceding chapter, or by similar devices in the literature respectively, the final proposed optimised design was not fabricated to be tested both on native and Si substrates. Fabrication of such a device would be the next logical step to test the practical performance, and to further verify the simulation results in this thesis. Variations on this optimised sample could also be made and measured; reducing the p-cladding thickness to reduce the intrinsic resistance, as well as adjusting the QD layer thicknesses. The latter would enable a better description of the QD model to be implemented for thinner buffer layers, which could be a key way of further improving modulation efficiency.

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