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Chapter

From Challenges to Solutions, Heteroepitaxy of GaAs-Based Materials on Si for Si Photonics

Junjie Yang, Huiwen Deng, Jae-Seong Park, Siming Chen, Mingchu Tang and Huiyun Liu

Abstract

Monolithic growth of III-V materials onto Si substrates is appealing for realizing practical on-chip light sources for Si-based photonic integrated circuits (PICs). Nevertheless, the material dissimilarities between III-V materials and Si substrates inevitably lead to the formation of crystalline defects, including antiphase domains (APBs), threading dislocations (TDs), and micro-cracks. These nontrivial defects lead to impaired device performance and must be suppressed to a sufficiently low value before propagating into the active region. In this chapter, we review current approaches to control the formation of defects and achieve high-quality GaAs monolithically grown on Si substrates. An APB-free GaAs on complementary-metal-oxide semiconductor (CMOS)-compatible Si (001) substrates grown by molecular beam epitaxy (MBE) only and a low TD density GaAs buffer layer with strained-layer superlattice (SLS) and asymmetric step-graded (ASG) InGaAs layers are demonstrated. Furthermore, recent advances in InAs/GaAs quantum dot (QD) lasers as efficient on-chip light sources grown on the patterned Si substrates for PICs are outlined.

Keywords: heteroepitaxy, III-V materials, Si, defects, integration

1. Introduction

Recently, InP and GaAs-based optical transceivers have been progressively replacing the traditional copper interconnect due to the unique properties of high transmission speed, larger bandwidth, and less cooling power required [1, 2]. Although great performances of III-V-based optoelectronic devices have been demonstrated, the cost and scalability limit the entry of their applications into the market of consumer electronics and massive production [3, 4]. In contrast, low-cost, high-bandwidth, and high-speed Si-based PICs and optoelectronic integrated circuits (OEIC) are ideal candidates to replace high-cost InP and GaAs-based PICs due to the large scalability and better thermal conductivity [3, 5–8].

However, as a critical component of PICs, a highly reliable and efficient Si-based laser is missing due to the indirect bandgap structure of Si and Ge bulk materials

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[9, 10]. Fortunately, most III-V materials have superior optical properties and are ideal to be used as a laser gain medium, but a suitable integration method is needed to combine III-V materials and Si platforms [11–18]. As one of the most mature techniques, wafer bonding has been commercially used in the Si optical transceivers but left a questionable yield and cost [19–23]. Even though the integration method of direct epitaxy of III-V materials on the Si platform could cause many types of crystal defects, which leads to a substantial deterioration in the device performance, it has great potential owing to various advantages of large-scale, high yield, low-cost, and dense integration [24].

The crystal defects generated at the III-V/Si interface will trap carriers and produce extra heat to the devices by forming nonradiative recombination centers [25, 26]. Hence, a proper strategy to reduce and eliminate these crystal defects becomes the most critical condition to realize high-performance Si-based III-V optoelectronic devices. In this chapter, we will introduce the generation of different types of crystal defects in terms of different physical dimensions, followed by their corresponding solution and recently demonstrated results. After that, recent advanced works of monolithic integration of III-V QD lasers on the Si platform along with optical waveguide are discussed.

2. Direct epitaxy of III-V materials on Si

Although the direct epitaxy of III-V material on Si offers substantial benefits, issues streaming from large material dissimilarities between these two materials lead to the generation of nontrivial defects. For instance, the different polarity, large mismatch of lattice constant, and incompatible thermal expansion coefficient (CTE) result in the formation of APBs, TDs, and micro-cracks, respectively. Extensive endeavors have been dedicated to advancing the growth techniques in the last decades to tackle these three main challenges in III-V/Si heteroepitaxy and realize high-performance III-V lasers integrated into Si. In this section, the mechanisms of defect formation and strategies to suppress the defects will be discussed.

2.1 Antiphase boundaries

A planar defect called APB is formed during the heteroepitaxy of polar III-V materials on nonpolar Si (001) substrates. Si (001) vicinal surface with a small offcut angle ($<1°$) exhibits terraces of alternating 1×2 and 2×1 dimerization, which are separated by Si single-atomic-height (S) steps [27–30]. These Si S steps are classified into two groups, that is, S_a and S_b, depending on the dimer orientation in the upper terrace [31]. The schematic diagram of alternating S steps on the Si (001) surface is shown in **Figure 1**, where the S_a steps are straight, and the S_b steps are meandering due to thermal fluctuation [28]. The terrace width between the adjacent S_a and S_b steps is defined as L. The relationship between terrace width L and the offcut angle of the Si substrate θ is defined as

$$a = L \times \tan \theta \tag{1}$$

where a is the height of a single Si S step, corresponding to 0.136 nm.

In most zinc-blend structures, for example, III-As and III-P materials, different atoms occupy the two face-centered-cubic (FCC) sublattices. By contrast, identical

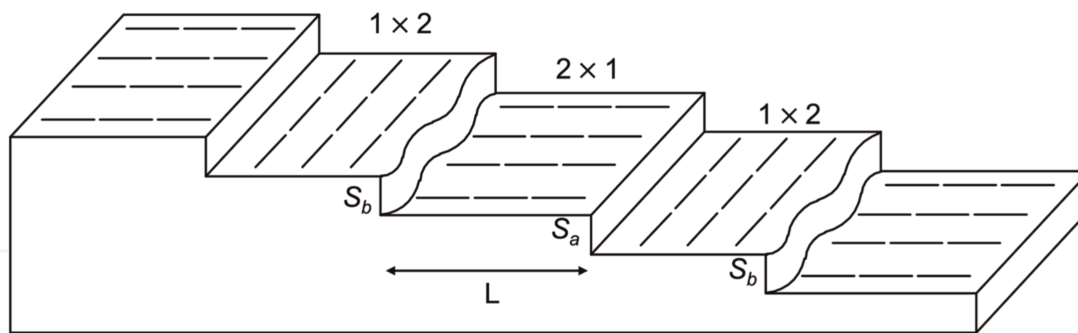

Figure 1.
Schematic diagram of Si (001) surface with S steps. Reprinted from reference [32] ©2021 the author under CC BY.

atoms occupy FCC sublattices in the diamond crystal structure of Si [33]. During the heteroepitaxy of III-V materials on Si (001) substrates, the orthogonal Si dimers in adjacent terraces lead to the formation of two domains with opposite sublattice allocation, that is, antiphase domains (APDs). The interface between two APDs is an APB consisting of homopolar bonds (Ga—Ga or As—As bonds) and is considered as electrically charged planar defect [34]. APBs propagate within the epilayers and act as nonradiative recombination centers and electrical leakage paths, severely degrading the optoelectronic properties of devices due to their relatively large area [34, 35]. In addition, the elastic strain associated with APBs will distort the crystal lattice and deform the DFLs. As a result, a high TD density (TDD) will be observed in the active region [32].

The presence of large-scale APBs can be characterized by using an atomic force microscope (AFM), electron scanning microscope (SEM), or transmission electron microscope (TEM). **Figure 2(a)** shows a typical AFM image of GaAs grown on Si (001) substrate with dense APBs, illustrated as curved boundaries. In practice, APBs emerge at the edge of Si *S* steps, and most of them propagate through {110} planes to the surface at low growth temperature as {110} APBs exhibit the lowest formation energy when compared with {112} and {111} APBs in both GaAs and GaP [36]. The kink of APBs into higher index planes, for instance, {111} and {112} planes, depends on the growth temperature of the epilayer. This process is crucial for the self-annihilation of APBs at the intersection [36, 37]. In stark contrast, the Si dimers are in the same orientation on the double-atomic-height (*D*) stepped Si surface. As a consequence, the nucleation of APBs is suppressed during the growth of III-V materials on Si *D* steps [25]. The APB nucleation and propagation under different circumstances are summarized in **Figure 2(b)**.

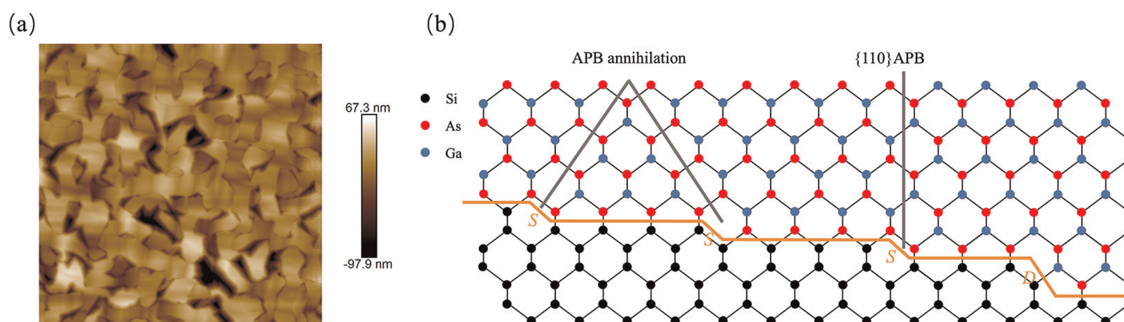

Figure 2.
(a) Top view AFM image shows dense APBs on the GaAs surface. (b) Schematic diagram of APB nucleation, propagation, and annihilation on Si steps.

A classic and common solution for suppressing APBs is to implement 4°–6° offcut Si substrates titled toward [110] direction, which preferentially forms *D* steps-dominated Si surface and thus inhibits the nucleation of APBs [28]. However, in order to be compatible with well-established CMOS processing technology, nominal Si (001) substrate with a misorientation of lower than 0.5° is required [38]. In the past decades, many techniques have been developed to achieve heteroepitaxy of APB-free III-V materials on on-axis Si (001) substrates, which will be introduced in the following contents.

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2.1.1 Selective area growth

Selective area growth (SAG) allows III-V heteroepitaxy on the prepatterned Si substrates and attracts intensive scientific interest as it provides efficient defect reduction, attributed to epitaxy necking effects and aspect ratio trapping (ART) [39–41]. SAG of III-V materials on the narrow trenches with patterned vertical dielectric sidewalls (normally SiO_2) ensures sufficient TD trapping if a high aspect ratio (AR) is defined. The AR is defined as the ratio of trench height h and width w:

$$AR = \frac{h}{w} \tag{2}$$

During the epitaxy of mismatched III-V on Si substrates, the misfit dislocation (MD) inevitably formed at the interface due to strain relaxation. Glissile 60° MDs tend to form segments that thread up as TDs, which propagate freely on the {111} planes in <110> directions and move upwards to the epilayer surface [42, 43]. As for the TDs propagating on the {111} planes perpendicular or parallel to the trench orientation, TDs will eventually hit the vertical dielectric sidewalls and are trapped if sufficient AR is applied, as illustrated in **Figure 3(a)** case (1) and (2). Since {111} planes form an incident angle of 54.7° with [1$\bar{1}$0] direction, a minimum AR of 1.41 is required to terminate the TDs within the trench. Unlike the TDs, however, the trench only traps the planer defects lying on the {111} planes parallel to the trench orientation, as indicated by case (3) and (4) in **Figure 3**. Furthermore, V-grooved Si (001) substrates with {111} facets, formed by using wet etching, were developed to prohibit the formation of APBs even with the presence of *S* steps [25, 44], as shown in **Figure 3(b)**.

Through V-grooved Si {111} surfaces via an ART process, Li et al. successfully demonstrated an APB-free GaAs-on-V-grooved Si (GoVS) template [45]. The Si (001) substrate patterned with [110] direction SiO_2 strips was etched by KOH solution to form V-grooved Si {111} facets as the etching rate of Si being the lowest in the (111) plane

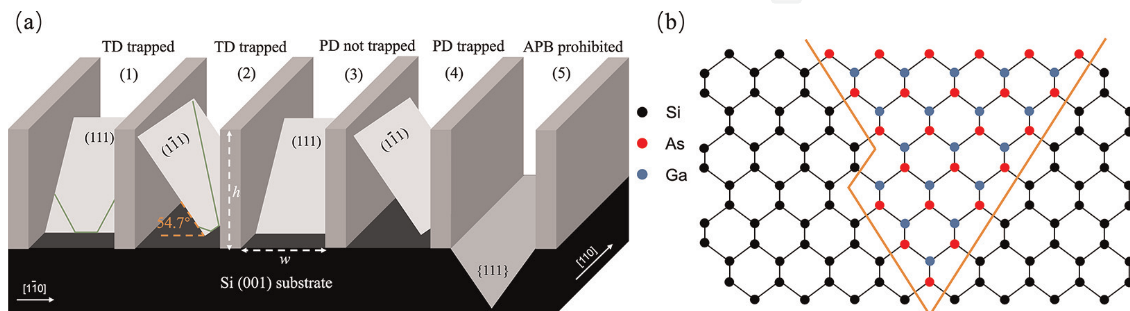

Figure 3.
(a) Schematic diagram showing TD and PD propagation within the narrow trenches with patterned vertical dielectric sidewalls. The APB nucleation is prohibited during the growth of III-V on V-grooved Si (001) substrate with {111} facets (b) even on a Si (111) S step.

[44]. SAG of GaAs nanowires was performed using a metalorganic chemical vapor deposition (MOCVD) system with a two-step growth method. **Figure 4(a)** shows the initial growth of GaAs on the V-grooved substrate, and planar GaAs nanowire is observed without APBs, thanks to the Si {111} facets. Interestingly, the unique "tiara"-like shape formed by Si undercut blocks the propagation of stacking faults through {111} planes, as shown in **Figure 4(b)**. After removing the SiO_2 strips by a buffered oxide etch, coalesced GaAs thin film was grown to finish the template. High-quality APB-free GaAs thin film was obtained after 300 nm GaAs overgrowth, as shown in **Figure 4(c)**.

In addition, Wei et al. proposed a novel way of forming Si {111} surfaces by homoepitaxy of Si on the U-shaped patterned Si (001) substrate. The U-shaped pattern along [110] direction is formed with a period of 360 nm, ridge width of 400 nm, and depth of around 500 nm by the deep ultraviolet photolithography (DUV) and subsequent dry etching, as shown in **Figure 5(a)** [46]. The U-shaped patterns will then be dipped in a diluted hydrofluoric acid to form a hydrogen-terminated surface and transferred into an IV molecular beam epitaxy (MBE) chamber for the deoxidation and subsequent homoepitaxy of 500 nm Si to form {111} facets, as shown in **Figure 5(b)**. Further deposition of Si to 550 nm leads to the merging of Si ridges and finally forms evolvement of (111)-faceted-sawtooth surface, which promotes the APB-free GaAs in the subsequent growth.

2.1.2 MOCVD/MOVPE grown APB-free GaAs/Si (001)

Although the pioneering works on SAG growth of APB-free III-V/Si (001) have been proved promising, the sophisticated processing and patterning of the Si surface

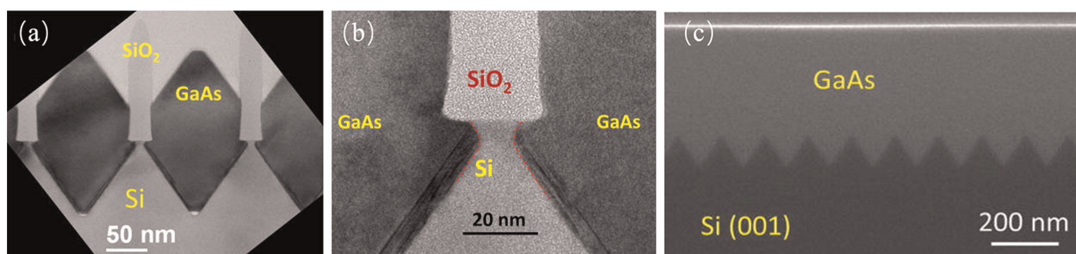

Figure 4.
(a) Cross-sectional TEM image showing the growth of GaAs on the V-grooved Si (001) substrates. (b) Defects are trapped by the "tiara"-like shape formed by Si undercut. (c)cross-sectional SEM of grown GaAs in the GoVS template. Reprinted with permission from [45] ©2015 AIP publishing.

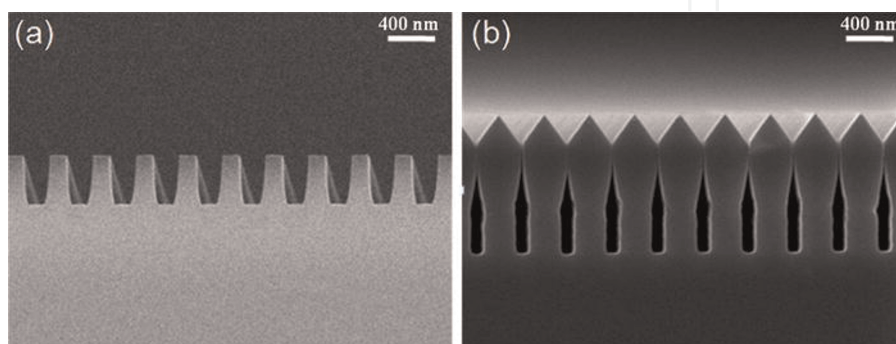

Figure 5.
(a) Cross-sectional SEM image showing a U-shaped patterned Si (001) substrate. (b) Si {111} facets formed by Si homoepitaxy. Reprinted with permission from [46] ©2015 AIP publishing.

are costly and time-consuming. Regarding the direct growth of III-V materials on planer Si (001) substrates, forming the *D* steps-dominated Si surface is the most straightforward idea to solve the APB issue. Thus, it has also been widely investigated. The Si *D* steps can be formed by high-temperature annealing of Si (001) substrates with proper hydrogen chemical potential, attributed to the preferential and selective etching of S_b steps by hydrogen [34]. This process is strongly related to the width of neighboring Si terraces. According to Eq. (1), a slightly large offcut angle of >0.1° is desired to erase S_b steps to a sufficiently low value and form the *D* steps-dominated Si surface.

Volz *et al.* achieved APB-free GaP on Si (001) substrate with an offcut angle of ~0.12° using metalorganic vapor phase epitaxy (MOVPE) [47–49]. A 500 nm Si buffer layer was first deposited, followed by postgrowth hydrogen annealing with the pressure of 950 mbar for 10 min at 975°C to obtain a *D* steps-dominated Si surface with an average terrace distance of ~120 nm. Nevertheless, *S* steps still appeared as a triangle-shaped form and existed between two neighboring *D* steps, covering ~15% of the surface area [37]. During the epitaxy of GaP on the Si buffer layer, APBs exist because of imperfect Si *D* steps. The distribution of APBs that resembles the underlying Si *S* steps is illustrated in **Figure 6(a)**, where the triangle-shaped *S* steps lead to the formation of APBs in two orthogonal directions [110] and [$\bar{1}$10]. The kinking and self-annihilation of APBs through energy favorable {112} is observed in the direction [110], which is perpendicular to the Si step orientation [36, 48]. The typical basal width of 180 nm for the *S* terrace yields a maximum height of 65 nm for APBs to be fully annihilated in GaP, as presented in **Figure 6(b)**. Since the triangle-shaped *S* steps become narrow along [110] direction, the decrease in basal length results in faster annihilation of APBs, which is confirmed by the TEM measurements in **Figure 6(c)**.

Based on this technique, a GaAs/GaP/Si (001) is developed as one of the most commercially successful templates for developing Si-based on-chip light sources. Many remarkable results have been reported based on this platform [50–52].

In contrast, Alcotte et al. selected a Si (001) substrate with a slightly larger miscut angle of 0.15° toward [110] direction to further enhance the etching of S_b steps. They demonstrated an APB-free GaAs grown on a Si (001) substrate by MOCVD without intermediate Si buffer layers [35]. Prior to growth, a Si wafer was first deoxidized in a SiConi™ chamber using an NF_3/NH_3 plasma. High-temperature hydrogen annealing at 850 to 950°C was then carried out to form Si *D* steps, as indicated in **Figure 7(b)**. A surface of GaAs grown on the un-optimized Si substrate is shown in **Figure 7(a)**,

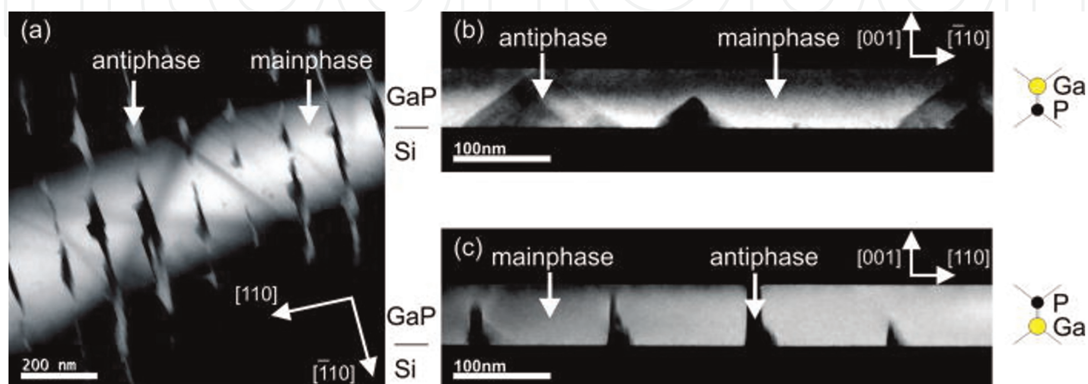

Figure 6.
(a) TEM plane view of GaP grown on pretreated Si buffer layer. Cross-sectional TEM measurement in (b) [110] and (c) [−110] cross-sections showing anisotropic APDs. Reprinted with permission from [48] ©2011 AIP publishing.

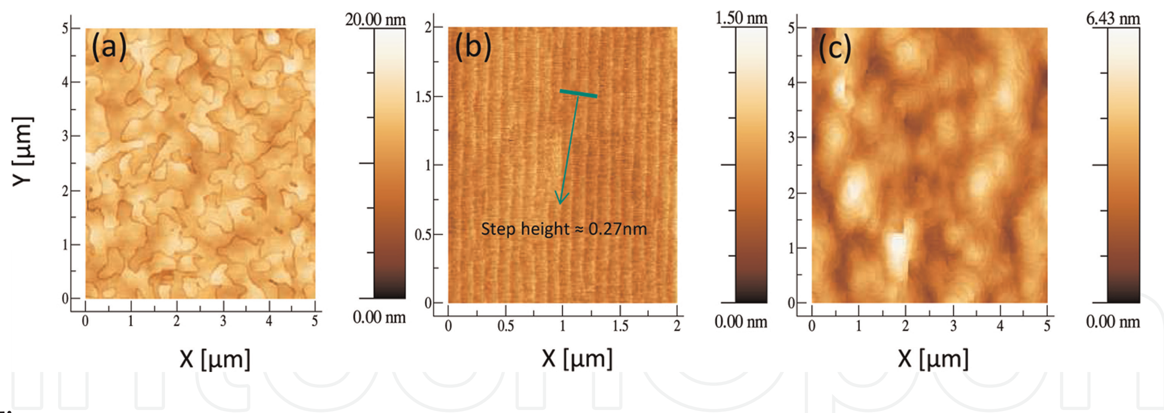

Figure 7.
(a) AFM image of GaAs grown on an un-optimized Si substrate showing high density of APBs. (b) Si D steps formed after annealing a Si substrate under optimized conditions. (c) AFM image of a 150 nm APB-free GaAs layer grown on Si (001). Reprinted from reference [35] ©2016 the authors under CC BY.

where a high density of APBs is visible. By utilizing an optimized Si substrate with the dominated Si *D* steps, a 150 nm APB-free GaAs epilayer was obtained with a low surface roughness of 0.8 nm for a $5 \times 5\ \mu m^2$ AFM scan, as presented in **Figure 7(c)**.

2.1.3 MBE grown APB-free GaAs/Si (001)

Indeed, the above-mentioned APB-free III-V templates grown by MOCVD/MOVPE have achieved great success in commercialization. Nevertheless, the requirement of a hydrogen source is unsuitable for migrating such methods into MBE systems. The MBE system has a unique advantage in obtaining high-quality QDs [53], which are insensitive to defects and have been regarded as one of the most promising gain media for high-performance Si-based on-chip laser sources [54]. Developing an APB-free III-V layer by a single system simplifies the growth process and is economical in the long term.

This need was first satisfied by Kwoen et al. who have successfully grown APB-free III-V lasers on on-axis Si (001) by MBE using a high-temperature $Al_{0.3}Ga_{0.7}As$ nucleation layer (NL). In the study, four samples with identical structures except for the composition of Al in the first 40 nm $Al_xGa_{1-x}As$ NL were grown and compared by SEM and photoluminescence (PL). It was concluded that $Al_{0.3}Ga_{0.7}As$ NL promoted self-annihilation of APBs and delivered the best GaAs quality. Based on this platform, InAs/GaAs-based QD lasers were developed with high operating temperature [55, 56].

Recently, Li and Yang et al. proposed a new method of using periodic Si *S* steps to redistribute the APB nucleation and promote the APB annihilation during optimized GaAs overlayer growth by a dual-MBE system [57, 58]. In their study, on-axis Si (100) substrates with unselected miscut angles of $0.15 \pm 0.1°$ toward <110> were deoxidized at 1200°C for 30 min in the group-IV MBE. A 100 nm Si buffer layer was first grown at 850°C by using a Si e-beam source. This was followed by five iterations of 20 nm thin Si grown at 850°C and annealed at 1200°C to reconstruct the surface and form periodic Si steps. The wafer was then transferred into the III-V chamber for subsequent growth. The schematic image showing the APB-free GaAs buffer layer structure is illustrated in **Figure 8(a)**, which started with a low temperature (LT) $Al_{0.4}Ga_{0.6}As$ NL grown at 330°C, and the growth rate was 0.1 monolayers per second (MLs^{-1}). A temperature ramping step with a ramp rate of 10°C Min^{-1} was applied afterward. At the same time of increasing temperature, GaAs was deposited

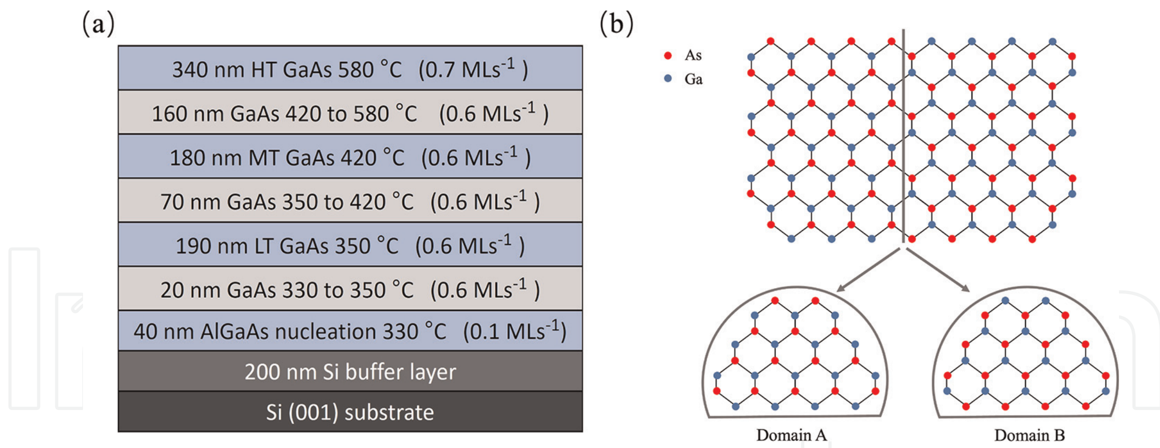

Figure 8.
(a) Schematic image of the APB-free GaAs buffer layer structure. (b) APB-MTE formed during high-temperature annealing. Reprinted from [58] © 2022 the authors, under CC BY.

simultaneously at a rate of 0.6 MLs^{-1}. This growth-during-ramp method was also applied in the following temperature ramping steps. Following the $Al_{0.4}Ga_{0.6}As$ NL, a three-step GaAs growth technique was implemented, consisting of 190 nm LT, 180 nm mid-temperature (MT), and 340 nm high-temperature (HT) GaAs grown at 350, 420, and 580°C respectively. The temperature ramping step was inserted between these GaAs layers, and the total GaAs buffer layer thickness was 1 μm.

In contrast to the growth parameter proposed by Kwoen et al. [59], the NL was grown at LT of 330°C in this study to avoid the formation of APB-modified thermodynamic equilibrium (APB-MTE). In APB-MTE, a (110) APB tends to enlarge, resulting in the formation of two APDs with opposite polarity, as shown in **Figure 8(b)** [58, 60]. Most recently, this growth strategy has been proved efficient by Gilbert et al. as it maintains the terrace-driven nature of APBs in initial nucleation rather than nucleation-driven, leading to controllable APB burying in the GaAs overgrowth [61]. Besides, the growth-during-ramping method helps to elongate the {110} APBs while preventing the APB-MTE. In addition, a suitable high growth temperature aids in the reconfiguration of the APBs into higher index planes, ultimately promoting the annihilation of APBs.

To examine the impact of the Si buffer layer on APB annihilation, a comparative analysis of the surface morphologies was conducted between Si substrates with and without an annealed Si buffer layer, as shown in **Figure 9**. For the deoxidized Si surface, the random distribution of Si atomic steps is observed in **Figure 9(a)**. These

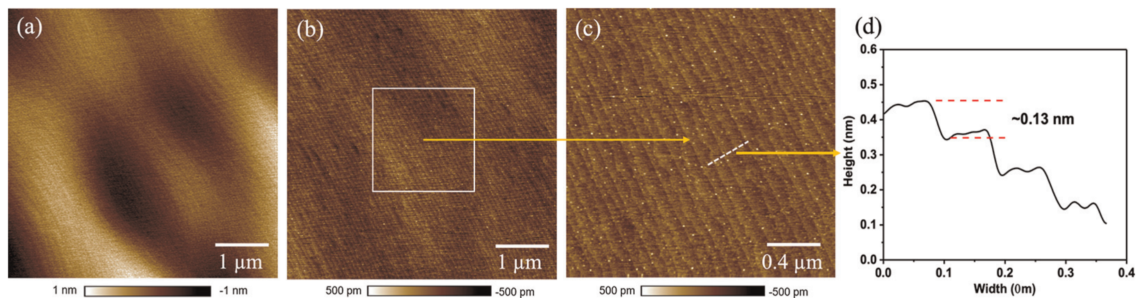

Figure 9.
5 ×5 μm² AFM image of (a) a deoxidized Si substrate and (b) a surface-reconstructed Si buffer layer. (c) 2 ×2 μm² AFM image of the Si buffer layer with periodic S steps. (d) Height measurement of Si steps, showing Si surface is mainly single-stepped. Reprinted from [57] © 2020 the authors, under CC BY.

undulating steps arise from the interaction between distinct stress domains on the Si surface, leading to the reduction in the overall elastic energy of the Si surface at a small offcut angle [62, 63]. In stark contrast, **Figure 9(b)** and **(c)** present the periodic *S* steps with a step height of ~0.13 nm, demonstrating only Si *S* steps instead of *D* presented on the Si surface after HT annealing [64, 65].

Two samples (sample A without Si buffer layer and sample B with Si buffer layer) with identical GaAs growth methods were grown and compared to test the impact of the Si *S* steps on APB annihilation. The cross-sectional TEM measurements are taken with a viewing direction of [$\bar{1}$10] for **Figure 10(a)–(d)** and [110] for (e) and (f). As shown in **Figure 10(a)–(d)**, APBs nucleate and propagate through the energy-favored {110} planes during LT GaAs growth. The APB propagation plane is configured to higher index planes in the high-temperature growth region, contributing to APB self-annihilation. The twisted patterns that demonstrate randomly distributed APB nucleation during GaAs/Si (001) (Sample A) are observed in **Figure 10(a)**. In contrast, periodic APBs occur when GaAs are grown on the Si buffer layer (Sample B), as illustrated in **Figure 10(c)**.

In both samples, APBs tend to intersect and annihilate with each other within the high-temperature growth region. However, in **Figure 10(a)**, the randomly distributed APBs shown in sample A propagate randomly within the GaAs, making them extremely difficult to eradicate effectively. The remaining APBs thus penetrate through the whole structure, as displayed in **Figure 10(b)**. In contrast, the well-organized APBs that nucleate on (S_a + S_b) resemble the underlying *S* steps and are closely spaced. The high growth temperature applied afterward sufficiently promotes the complete destruction of APBs within ~500 nm, as shown in **Figure 10(d)**.

Furthermore, the APBs that penetrate through the whole GaAs buffer layer in sample A are noticed from [110] viewing direction, as indicated in **Figure 10(e)**. By contrast, since the Si buffer layer is populated by *S* steps in [110] direction, the APBs that nucleate on these *S* steps resemble the step orientation, leaving no APB observed in [110] viewing direction, as shown in **Figure 10(f)**. This observation differs from the aforementioned APB-free GaP/Si growth, where triangle-island-shaped S_b steps

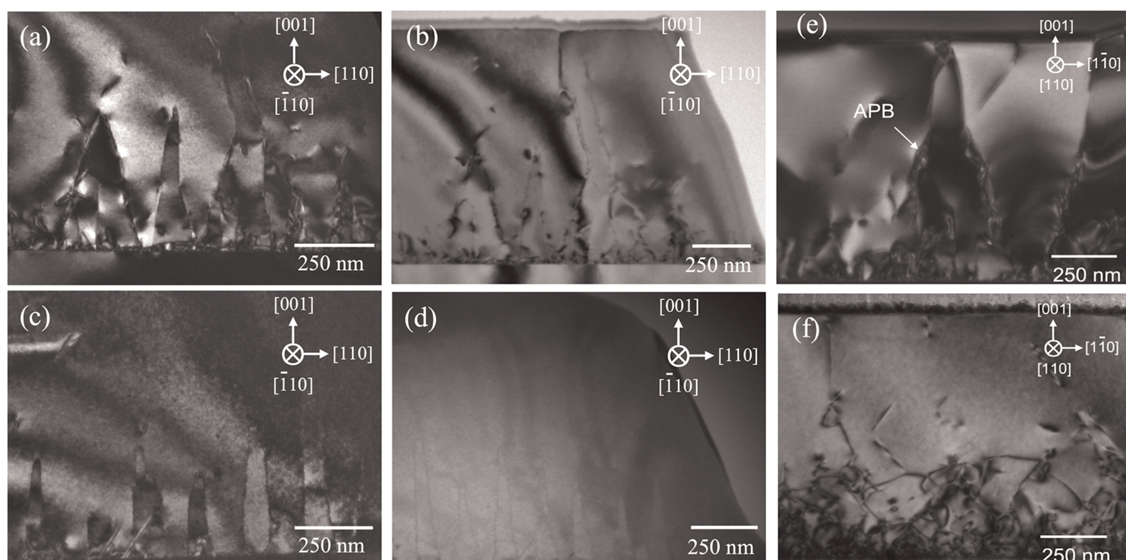

Figure 10.
Cross-sectional TEM images from [−110] viewing direction showing APB nucleation and self-annihilation for (a) regional and (b) 1 μ m range of sample a and (c) regional and (d) 1 μ m range of sample B. TEM images from [110] viewing direction for (e) sample a and (f) sample B. reprinted from [32] ©2021 the author under CC BY.

are left near the edge of the *D* steps. During subsequent growth of GaP on these *S* triangle islands, the APBs that resemble the underlying Si steps can be found in two orthogonal directions, that is, [110] and [$\bar{1}$10] [48, 49, 66].

The annihilation of APBs at HT is attributed to the difference in GaAs growth rate of the two domains. During the deposition of GaAs on Si, an Arsenic (As) prelayer is adopted to avoid Ga etching, and As resembles the underlying Si dimer orientation. Since Ga atoms diffuse mainly along the As dimer direction, GaAs deposited on the upper terrace of S_a are more likely to grow along the [110] direction (main phase), and GaAs deposited on the upper terrace of S_b will grow along [1$\bar{1}$0] direction (antiphase), as indicated in **Figure 11(a)** [67, 68]. The main-phase GaAs grow faster than antiphase GaAs in the [110] direction, forcing neighboring APBs to intersect toward each other during temperature increases. As a result, the annihilation of terrace-driven APDs is facilitated, as shown in **Figure 11(a)**.

Interestingly, it has been reported that {110} APBs help to reduce TDs during GaAs overgrowth [58]. {110} APBs trap {111} TDs to climb along it and promote the termination of TDs with opposite Burger vector signs. In addition, the trapped TDs can glide through other {111} planes and might be captured again by other {110} APBs. This process will recur until TDs are terminated or move beyond the APBs. Consequently, the TDD level reaches 8×10^8 cm^{-2} for GaAs grown on Si (001) substrate with periodic {110} APBs, which is half of GaAs grown on Si offcut substrate with identical growth structure. This result reveals the probability of controlling both APBs and TDs simultaneously and achieving a high-quality APB-free GaAs/Si (001) template by optimizing the GaAs growth technique in the future.

2.2 Dislocations

The second issue that hinders the direct epitaxy of III-V materials on Si is the formation of dislocations. Most III-V materials, except for GaP and aluminum phosphide (AlP), have a large lattice mismatch with Si. During the III-V-on-Si mismatched heteroepitaxy, the strain energy accumulated inside the epilayer is proportional to the epilayer thickness. Once the thickness of the strained layer exceeds a certain value, the so-called critical thickness, MDs, are formed at the interface to relax the accumulated strain. These MDs introduce missing or dangling bonds along the mismatched

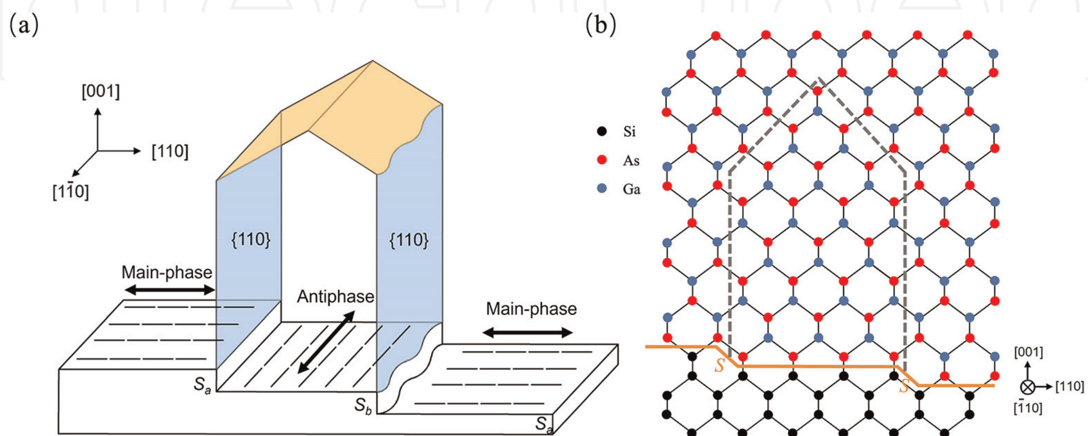

Figure 11.
(a) Schematic diagram of terrace-driven APB burying method. The area within the closed-loop APBs is considered as an antiphase, while the outside is the main phase. (b) Antiphase GaAs are buried by main-phase GaAs during the growth. Reprinted from [58]© 2022 the authors, under CC BY.

interface. The commonly occurred MDs can be classified into two types: (1) edge MDs with Burgers vector lying in the interface (001) plane and perpendicular to the line direction. This type of dislocation mainly originates from Si steps and is "sessile". (2) 60° MDs with Burgers vector of 60° to the dislocation line and 45° to the substrate, and this type of dislocation is termed "glissile". Since dislocations are one-dimensional defects and cannot terminate within a crystal, 60° MDs will move toward the edge of the crystal or form segments that thread up as TDs, which propagate freely along the {111} planes and penetrate through whole epi-layers. The TEM image of MD and TD are illustrated in **Figure 12**. TDs introduce deep states and act as nonrecombination centers for carriers, which leads to short carrier lifetime, low photon emission efficiency, and impaired device performance [43].

Several strategies were developed to control TDD in the past decades, aiming to reduce TDD to a low value of $\sim 10^{-6}$ and 10^{-5} cm^{-2}, which is close to the TDD on the native substrate. For instance, inserting a Ge intermediate or SiGe-graded buffer layer effectively bridges the lattice mismatch between Si substrates and III-V [69]. Besides, the three-step GaAs growth method is commonly utilized to control TDD within the GaAs buffer layer for the GaAs-on-Si system. A thin AlAs nucleation layer grown by migration-enhanced epitaxy is also adopted to suppress three-dimensional defects raised at the III-V/Si interface [70], which is followed by MT and HT GaAs to minimize the point defects during epitaxy [54]; Thermal cycle annealing (TCA) is another effective tool as it provides extra thermal stress to enhance the motion of TDs and promote higher probability for TD interaction [71].

In addition to the previously mentioned strategies, inserting SLSs serving as dislocation filter layers (DFLs) is another effective method that can sufficiently reduce the TDD. SLSs consist of periodic lattice-mismatched thin layers without strain relaxation. The unreleased strain tends to bend TDs at the SLSs interface and forces them to move laterally toward the edge of a crystal (parallel to the interface), enhancing the probability of intersection and termination of TDs, as shown in **Figure 13**. Besides, MD segments form at the SLSs interface as TD moves, relieving the misfit and reducing the net glide force of TDs to zero [43].

2.2.1 Optimization of SLSs and asymmetric step-graded filter structure

Optimizing SLSs to improve their filtering efficiency has been extensively explored. To design a proper SLS, the strain force must be first considered. A trade-off appears as a higher strain force strengthens the filtering ability, while an over-strain

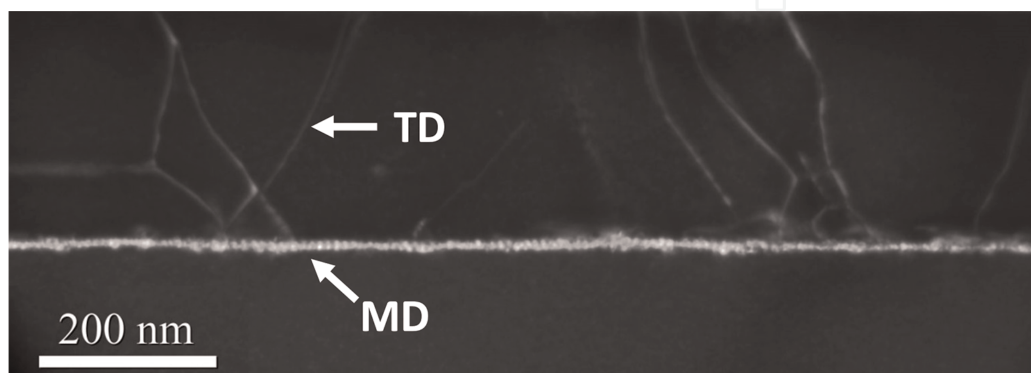

Figure 12.
Cross-sectional bright-field TEM image showing MDs and TDs.

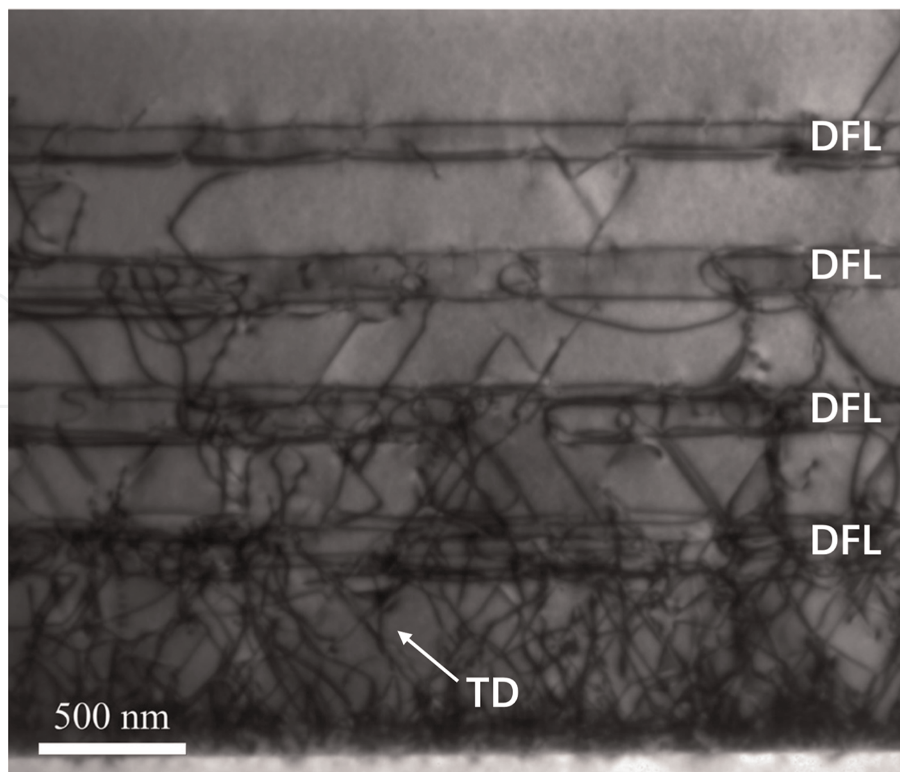

Figure 13.
Cross-sectional TEM image of GaAs grown on on-axis Si (001), showing TD propagation and annihilation within four sets of $In_{0.18}Ga_{0.82}As$/GaAs DFLs.

force leads to new defects. Thus, for the most commonly used InGaAs/GaAs system, the indium (In) composition and the thickness of GaAs space layers for $In_xGa_{1-x}As$/GaAs DFLs must be carefully designed. Tang et al. demonstrated that 18% of indium (among 16, 18, and 20%), along with a 300 nm GaAs space layer, delivered the best filter efficiency in the design of $In_xGa_{1-x}As$/GaAs DFLs [72]. Besides, *in situ* thermal annealing was applied for each set of DFLs when the growth was being pulsed in the reactor. This approach further reduced the TDD, as the motion of TDs was enhanced, and thus, a higher possibility for TD self-annihilation was achieved.

Shang et al. provided a comprehensive study of optimizing DFLs on GaAs/GaP/Si (001) templates, which formed the basis for the high-temperature InAs/GaAs QD laser with an extrapolated lifetime of over 22 years [51, 71]. In this study, $In_{0.15}Ga_{0.85}As$ (10 nm)/GaAs (x nm) × 20 SLSs as DFLs were grown and compared. X represents values 10, 7, 5, 2, 0. A decreasing trend of filter efficiency was observed when x became lower, attributed to a higher degree of relaxation for $In_{0.15}Ga_{0.85}As$. Based on this observation, 200 nm $In_xGa_{1-x}As$ were further analyzed with various indium (In) compositions (10, 15, 17.5, 20, and 25%). It was concluded that 15 and 17.5% In composition delivered the best filtering efficiency, and a clear blocking effect of TDs was observed for an In composition higher than 20%. Furthermore, Shang et al. developed novel filter layers with ASG filter structure, which helps to reduce blocking effects, as shown in **Figure 14(a)**. Ten minutes of annealing at 530°C was applied for each InGaAs layer to promote tensile relaxation. Finally, TDD of 2 $\times 10^6$ cm^{-2} was achieved based on this structure, as shown in **Figure 14(b)**. This is also proven by TEM results shown in **Figure 14(c)**. Almost all TDs are blocked by this ASG filter structure, leaving the top GaAs layer with ultra-low TDD.

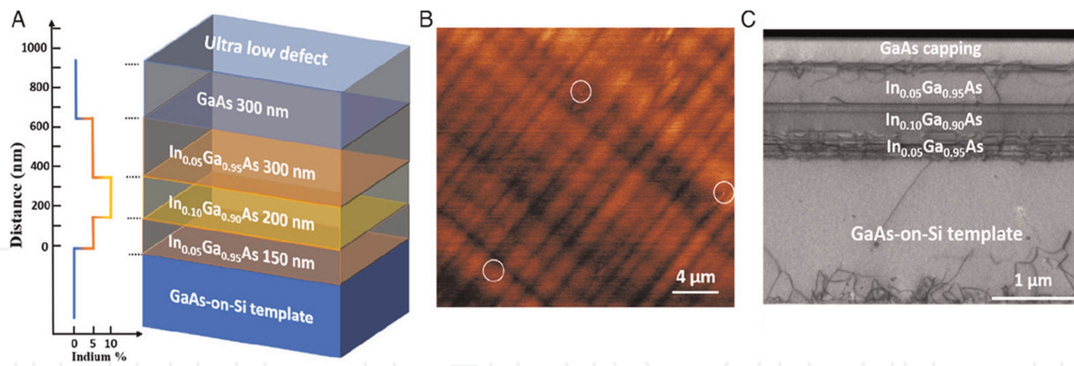

Figure 14.
(a) Schematic diagram of InGaAs ASG layers. (b) ECCI image showing TDD of 2 $\times 10^6$ cm^{-2}. (c) Cross-sectional TEM image of InGaAs ASG layers. Reprinted from [71] © 2020 the authors, under CC BY.

2.2.2 Trapping layer

During the postgrowth cooldown period, thermal stress-induced TD motion happens as a result of the large mismatch in CTE between III-V and Si. Once TDs encounter the In-contained DWELL structure, the mechanically hardened active region forces TDs to move laterally, leaving behind the MDs at the interface and severely degrading the optical properties of QDs. To solve this issue, Selvidge et al. inserted In-contained trapping layers (TL) to displace MDs above and below active region, which dramatically improved the optical prosperities of QDs [73]. The thickness of InGaAs TLs was kept below critical thickness (7 nm) without introducing extra MDs. As shown in **Figure 15**, inserting TLs does not contribute to TD reduction, but it displaces the MD formation below it rather than the active region to minimize the decremental impact brought by MDs. TLs were also applied in the laser structure to explore its efficiency, as illustrated in **Figure 16(a)**. 7 nm $In_{0.15}Ga_{0.15}As$ and $In_{0.15}Al_{0.15}As$ were placed 80 nm above and below the active region sandwiched by cladding layers to minimize the effect of the electrical barrier due to bandgap alignment. From **Figure 16(b)** and **(c)**, TLs were effective for displacing MDs along it rather than on DWELL. This observation is consistent with **Figure 16(c–f)**, where MDs lie on the DWELL when no TLs are inserted. Most MDs lie on the TLs, and further glide of TD segments does not introduce extra MDs in the QD lasers. It was

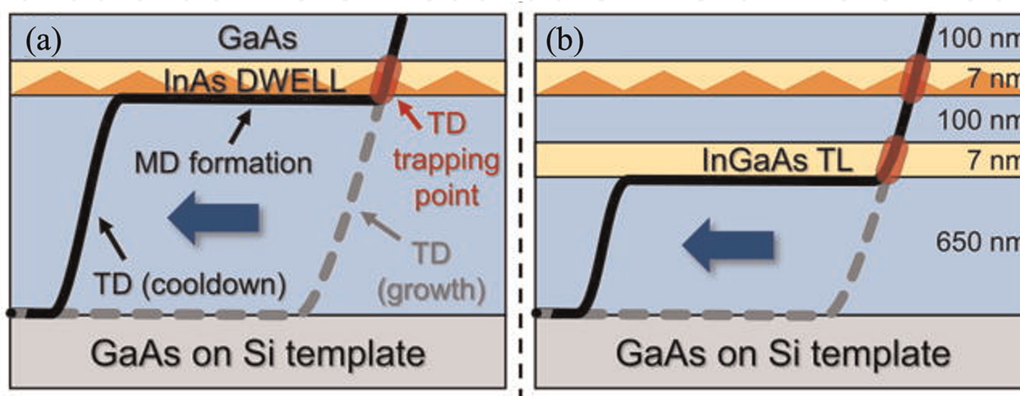

Figure 15.
Schematic diagrams showing MD formed (a) without and (b) with InGaAs TLs. Reprinted with permission from [73] ©2020 AIP publishing.

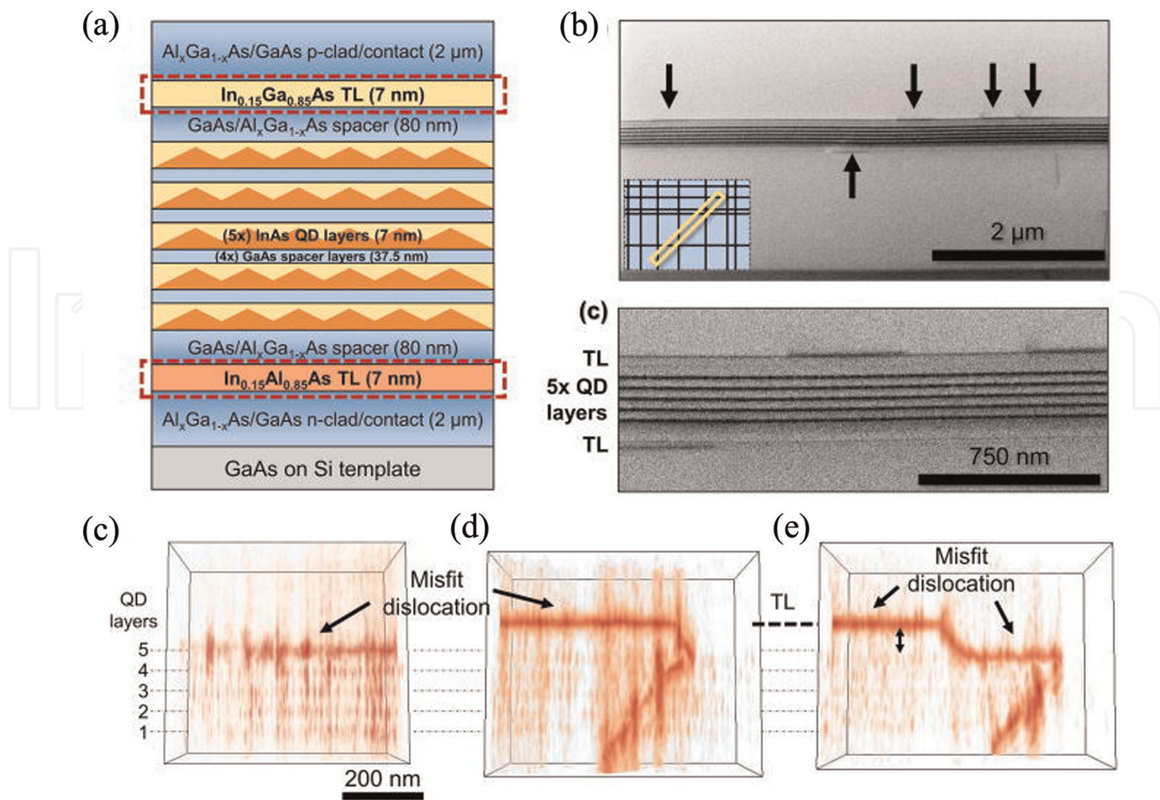

Figure 16.
(a) Schematic diagram of proposed laser structure with TLs. (b) Cross-sectional bright-field TEM image showing MD segments appear on TLs, as indicated by black arrows. (c) Zoom-in image of (b). Cross-sectional tomographic reconstruction showing (c) MDs lie on the 5th QDs in laser structure without TLs. (d) MDs lie on the TLs. (e) Part MDs lie on the TLs, and part lie on the 5th QD. Reprinted with permission from [73] ©2020 AIP publishing.

also demonstrated that the laser with TLs exhibited half of the threshold current (even lower than state-of-art lasers on Si when higher TDD is presented in this case), a 60% increase in slope efficiency, and ~ 3.4 times improvement in peak single facet output power, revealing the effectiveness of TLs. Such performance is comparable to Si-based QD lasers with one magnitude lower TDD. Compared with the structure consisting of thick DFLs, the insertion of thin TLs is more effective in improving laser performance without introducing a thick epilayer, which is beneficial for the yield and massive production of Si-based PICs in the long term.

Recent developments of reducing TDD in GaAs monolithically grown on Si (001) substrates by combining previously mentioned strategies are highlighted in **Table 1**.

2.3 Cracks

Controlling defect density to a sufficiently low value requires a thick buffer layer with several micrometers, which introduces the formation of micro-cracks. Because of the large mismatch in CTE between III-V materials and Si, for example, 5.73×10^{-6}°C^{-1} for GaAs and 2.6×10^{-6}°C^{-1} for Si, the accumulated thermal stress during the growth is relieved by forming micro-cracks and wafer warping when the epilayer cools down from high growth temperature to room temperature [79]. Theoretically, cracks form along the [110] and [1–10] directions when the elastic energy exceeds a critical value to generate two new surfaces, as shown in **Figure 17**. In addition, it is also proved that crack formation originates from other preexisting defects [80] and

Year	Substrate	Dislocation filter layer structure	Total buffer thickness (μm)	TDD (cm^{-2})	Ref
2021	V-grooved Si (001)	Two sets of five periods of $In_{0.15}Ga_{0.85}As$/GaAs SLSs and two sets of five periods of $In_{0.15}Al_{0.85}As$/GaAs SLSs	2.1	1.6×10^7	[74]
2020	GaP/Si (001)	$In_{0.05}Ga_{0.95}As$/ $In_{0.1}Ga_{0.9}As$/$In_{0.05}Ga_{0.95}As$ ASG	2.55	1.5×10^6	[71]
2020	Si (001)	Two sets of five periods of $In_{0.15}Ga_{0.85}As$/GaAs SLSs	2.6	3×10^7	[75]
2020	GaP/Si (001)	Single $In_{0.1}Ga_{0.9}As$ layer	2.3	7.3×10^6	[76]
2019	GaAs/Si (001)	Four sets of five periods of $In_{0.18}Ga_{0.82}As$/GaAs SLSs	2.3	5×10^7	[77]
2019	Si (001)	Three sets of five periods of $In_{0.15}Ga_{0.85}As$/GaAs SLSs	2	Below 10^8	[55]
2017	GaP/Si (001)	Ten periods of $In_{0.1}Ga_{0.9}As$/GaAs SLSs	3.1	8.4×10^6	[78]

Table 1.
Summary of recent optimization of DFL layers for GaAs monolithically grown on Si (001) substrates.

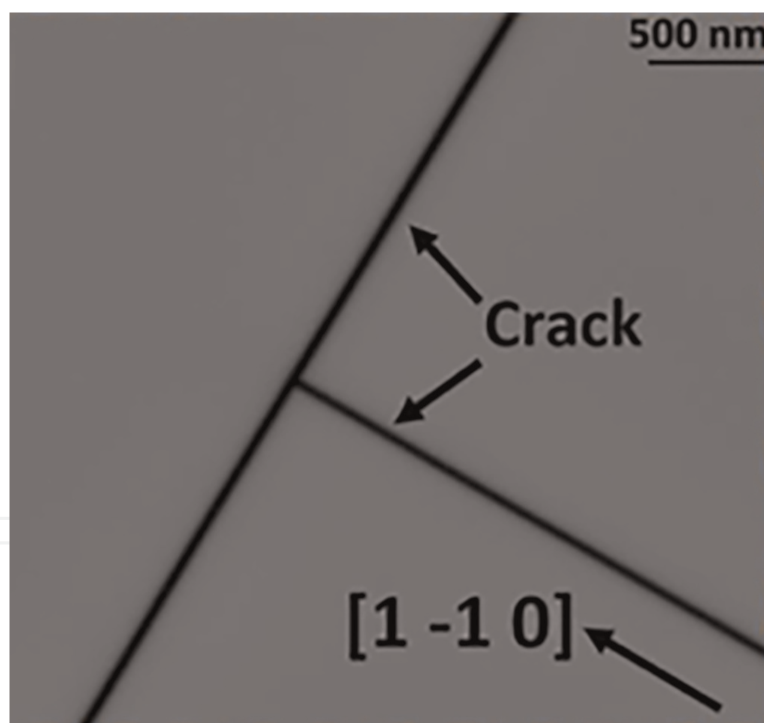

Figure 17.
SEM image of cracks in orthogonal directions. Reprinted from [79] © 2022 the authors, under CC BY.

layer thickness. For example, Yang et al. reported that the crack density increases sharply about three times when the thickness of the GaAs layer on Si increases from 5 to 6.7 μm [81]. Similar to other defects, micro-cracks are detrimental to the device's performance as they serve as scattering centers for light propagation and electrical leakage paths [81]. Additionally, the high density of micro-cracks will significantly reduce the total yield of devices [82]. Hence, controlling micro-crack is crucial for the mass production of Si-based PICs in the future.

A prolonged cooling down period with a slower cooling rate is suggested after growth to prevent the micro-cracks [79, 83]. Furthermore, SAG of III-V materials helps to prevent micro-cracks formation by alleviating thermal stress. However, dense defects, including TDs and stacking faults, will be generated near the pattern edge, degrading crystal quality. Moreover, in large patterned areas, micro-cracks remain on the sample surface [84]. Even though diverse techniques have been demonstrated, keeping the device thickness below the cracking threshold is the most economical and effective way [81].

As cracks are formed when the elastic energy exceeds a certain limitation, the thickness of the epilayers is the most prominent and essential reason for the crack formation. Yang et al. proposed the relationship between the critical cracking thickness and a dimensionless driving force number Z [85], which calculates the energy released per unit area for the crack:

$$G = \frac{Z\sigma^2 t}{\overline{E_f}} \tag{3}$$

where σ is the stress in the thin film, t is the thin film thickness and $\overline{E_f}$ denotes the biaxial modulus. In a typical system where the substrate and the epilayer have similar elastic moduli, the Z should be within 2 to 4. The stress in the thin film can be calculated as:

$$\sigma = \overline{E_f}\left(\alpha_f - \alpha_s\right)\Delta T \tag{4}$$

where α_f and α_s are the CTE of the thin film and the substrate, respectively. While the ΔT is the temperature difference between the growth temperature and the room temperature. The critical thickness for crack formation can be derived, provided that the fracture resistance Γ is twice the energy release rate G [85, 86]:

$$t_c = \frac{\Gamma \overline{E_f}}{Z\sigma^2} \tag{5}$$

Based on the mathematical model given above, the cracking threshold of GaAs is estimated as 3.9 μm when it is cooled down from the growth temperature of around 600°C to room temperature. However, for most growth of high-performance III-V compound semiconductor devices on Si, the structure was usually above 4 μm due to the utilization of a thick buffer layer to minimize the TD generated at the interface.

Furthermore, Shang et al. further improved the previous model and shed light on the relationship among dislocation density, film thickness, cooling rate, and crack formation [79]. It has been suggested that lower TDD induces higher equi-biaxial stress in the film during the cooling down period. The critical thickness is inversely proportional to the cool rate and TDD, as shown in **Figure 18**. It is suggested that with a low TDD of 1.0×10^6 cm^{-2} and a low cool rate of 1°C min^{-1}, the critical thickness of cracking is approximately 6 μm. Therefore, a thin epilayer with a low cooling rate is of pinnacle importance to prevent micro-cracks.

Recently, Yang et al. used an optimized 300 nm Ge buffer layer to replace part of the thick GaAs buffer layer in the laser structure while keeping the TDD unchanged [82, 87]. As a result, the total thickness of the laser structure can be reduced to approach the cracking threshold without bringing any negative effects. A comparison between TD propagation for GaAs deposited directly on a Si substrate and a Ge/Si

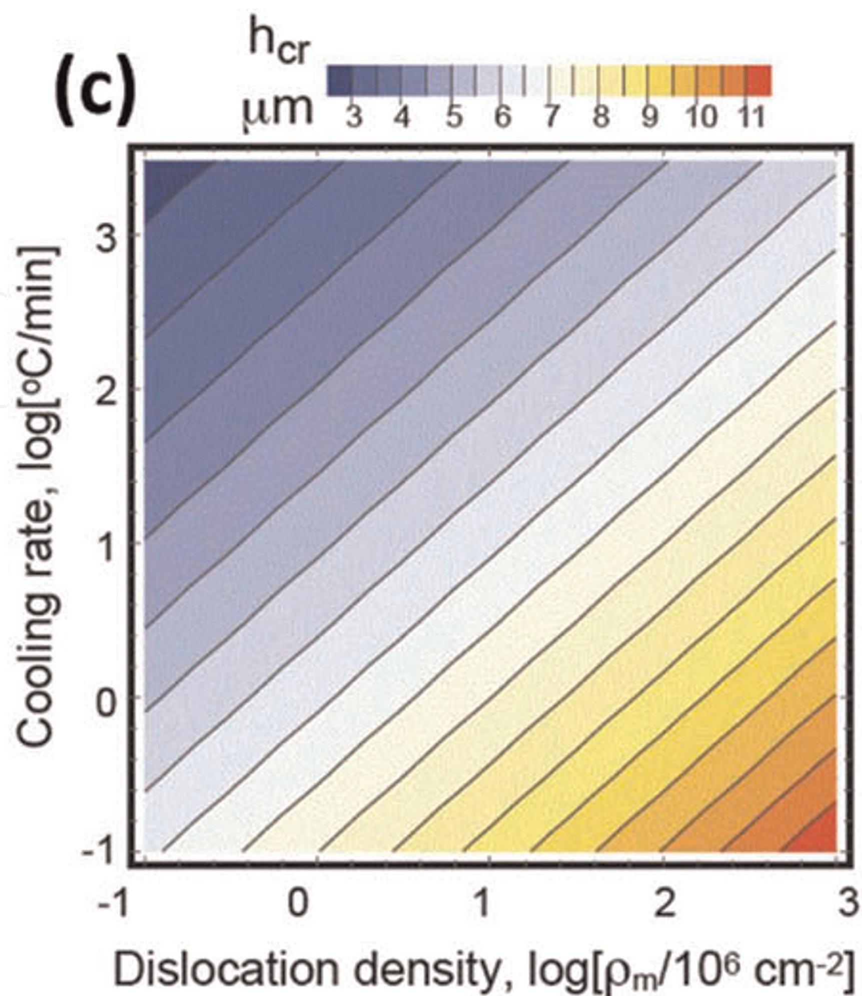

Figure 18.
Relationship among critical thickness, cooling rate, and TDD. Reprinted from [79] © 2022 the authors, under CC BY.

virtual substrate (VS) is demonstrated in **Figure 19**. As shown in **Figure 19(a)**, a high density of defects is generated at the GaAs/Si interface, and almost $\sim 10^9$ cm^{-2} TDD is observed underneath the first DFL [54]. In contrast, a much lower TDD of $\sim 6 \times 10^8$ cm^{-2} is obtained in the 300 nm Ge buffer layer attributed to the adoption of HT TCA between 600 and 900°C, as indicated in **Figure 19(b)**. This TDD is comparable to the 1.4 μm GaAs monolithically grown on Si with one set of DFL. In addition, MDs are barely introduced in the subsequent GaAs growth since the lattice constants of Ge and GaAs are almost identical. As a result, TDD reaches 4×10^6 cm^{-2} after applying four sets of DFLs. Based on this result, a high-quality InAs/GaAs QD laser was developed with high operation temperature, revealing the feasibility of using Ge/Si platform for reducing micro-cracks in the future.

2.4 Summary

Recent progress in controlling crystal defects during the heteroepitaxy of III-V materials on Si substrates has been reviewed in this section. Several newly developed techniques were applied for Si-based PICs, which will be discussed in the following contents.

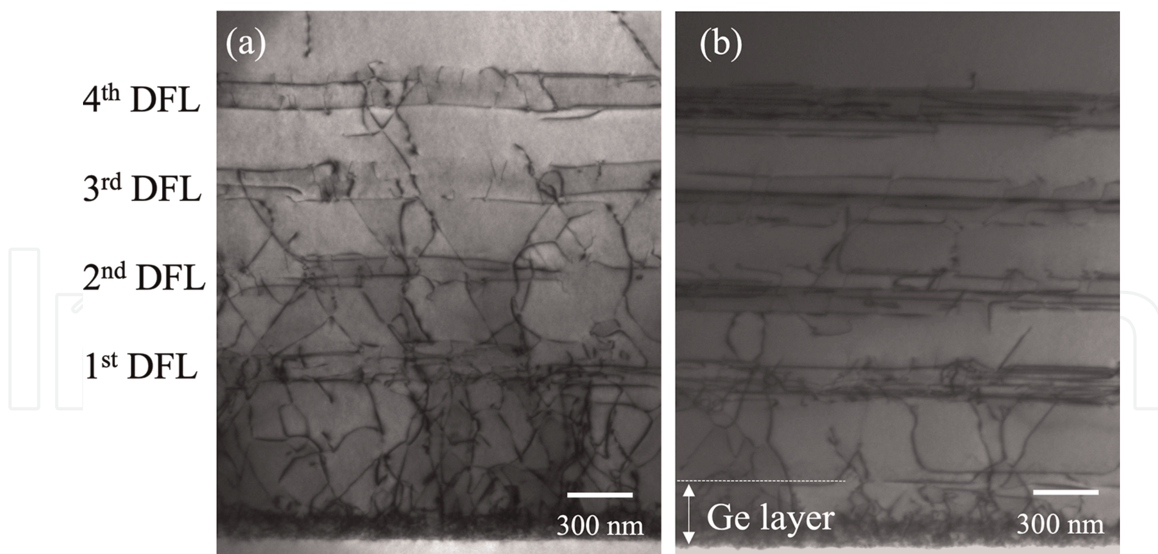

Figure 19.
Cross-sectional TEM images of GaAs buffer layer grown on (a) a Si substrate and (b) a Ge/Si VS. reprinted from [82] © 2021 the authors, under CC BY.

3. Photonic integrated circuits

The idea of using Si-based PICs in which all major photonic functions are monolithically integrated on a single Si or Si-on-insulator (SOI) substrate has emerged to promote rapid advances in quantum photonics, quantum computing, LiDAR, and artificial intelligence-powered nanophotonics [4, 88]. It contributes to the better life quality of consumers with low cost due to the low material cost and large wafer size of Si [4, 89, 90]. Over the past decades, an unprecedented boom of key components of Si photonics, including Si-based modulators [91], photodetectors [92], and waveguides [93], has been witnessed. Until now, an efficient, electrically pumped Si-based laser remains a missing piece and becomes the roadblock to the commercialization of Si-based PICs.

To circumvent the inherent limitations of Si, integrating direct-bandgap III-V materials onto Si has been regarded as an attractive approach for the Si-based on-chip light source in PICs. Such integration leverages the benefits of superior optical properties of III-V materials, along with large wafer sizes and the low-cost and mature processing technology of Si. Direct epitaxy of QD-based laser on Si substrates has achieved remarkable progress [51, 54, 94, 95]. Various novel laser structures were reported with superior performance, such as distributed feedback lasers [96], comb lasers [97], photonic crystal lasers [98], topological lasers [99], etc. All key optical components integrated on a single SOI substrate are highly desired as they offer high integration density and great compatibility with the current Si microelectronics platform. Until now, the integration of III-V gain regions on SOI substrates mainly relies on wafer bonding, in which light is evanescently coupled to underlying Si waveguides [9, 20]. However, from the commercialization perspective, direct epitaxy is economically favored in terms of cost, yield, and scalability. Considering the integration of on-chip laser sources, the thick, defective buffer layer adopted for direct epitaxy of III-V materials on Si hinders the evanescent coupling of light from gain regions to underlying Si waveguides. In this case, SAG growth of laser structure on a trenched substrate and butt-coupled to the embedded, prepatterned waveguide is promising for fulfilling the last missing piece of Si-based PICs. In addition, SAG helps to alleviate the

thermal stress of films, potentially preventing the formation of cracks [79]. On the other hand, such a method is nontrivial as it demands restricted design to minimize the alignment deviation between the central axis of the embedded Si waveguide and the InAs/GaAs QD active region and careful handle of polycrystal after the overgrowth of III-V on oxide.

Shang et al. recently reported the first electrically pumped continuous-wave (c.w.) InAs/GaAs QD lasers grown on a patterned 300 mm substrate [100]. In this study, the 200 nm GaP/Si template by NAsP $_{III/V}$ GmbH was adopted in trenches to prevent APBs [47, 66]. This was followed by a 1.6 μm GaAs buffer layer and InGaAs asymmetric graded dislocation filter layers to reduce TDD to around 1.5×10^7 cm^{-2}. The active region consists of five stacks of InAs/GaAs DWELL structure separated by 37.5 nm GaAs space layers. The QD nucleation temperature was precisely determined using indium as an ex situ "temperature gauge" in this template to ensure high-quality QDs. As a result, room temperature with a wavelength of 1300 nm and a full width at half maximum (FWHM) of 32 meV was achieved for QDs. The as-grown 300 mm wafer from IQE with an identical growth method is shown in **Figure 20(a)**. The milky wafer surface caused by the deposited polycrystalline III-V on the oxide brought challenging tasks for device fabrication. A wet etch process for nonselective polycrystal removal facilitates the following fabrication process, as shown in **Figure 20(b)**. The top-down view of the as-cleaved laser with probe metal and the cross-sectional SEM image of the fabricated laser with a ridge width of 3.5 μm in a 20 μm trench are demonstrated in **Figure 20(c)** and **(d)**, respectively.

Finally, an electrically pumped InAs/GaAs laser was demonstrated with c.w. lasing up to 60°C, a maximum double-side power of 126.6 mW, and a threshold current of 47.5 mA. However, this work only presents a demo of an in-trench laser without demonstrating butt coupling between the laser and the embedded waveguide.

In a parallel effort, Wei et al. took a step further to test the butt coupling efficiency between their embedded InAs/GaAs QD lasers and Si waveguides. **Figure 21(a)** shows a schematic diagram of butt coupling between a trenched laser and a patterned Si waveguide. The fabricated devices are displayed in **Figure 21(b)** and **(c)**. Prior to growth, laser trenches and Si waveguides are prepatterned in an eight-inch SOI wafer,

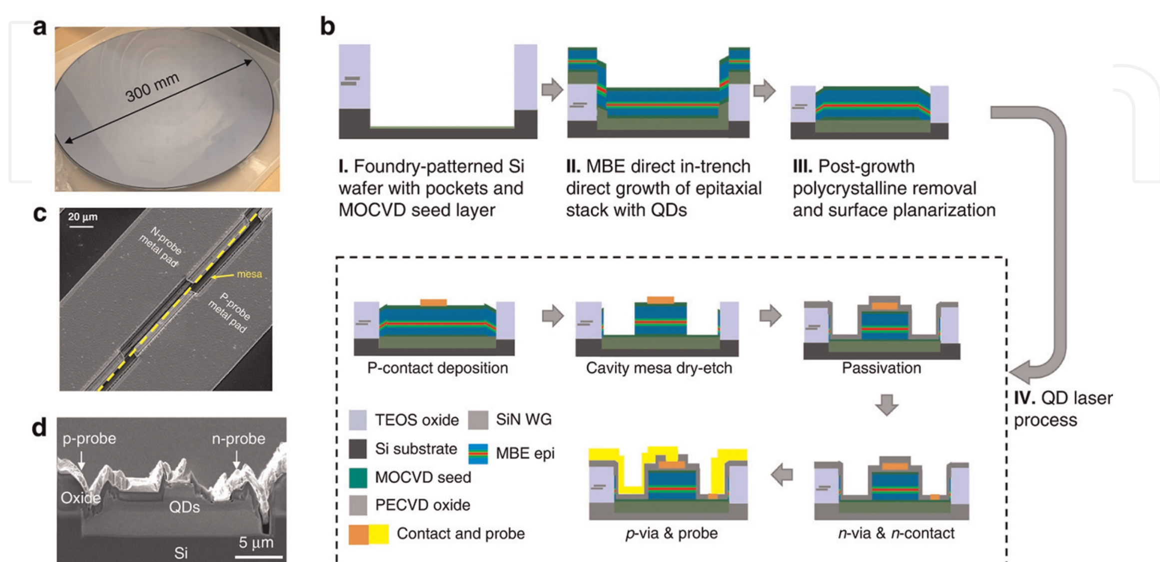

Figure 20.
(a) As-grown 300 mm wafer surface. (b) the fabrication process of the SAG laser. (c) As-cleaved laser with probe metal. (d) Cross-sectional SEM image of the fabricated laser in a 20 μm trench. ©2022 the authors under CC BY.

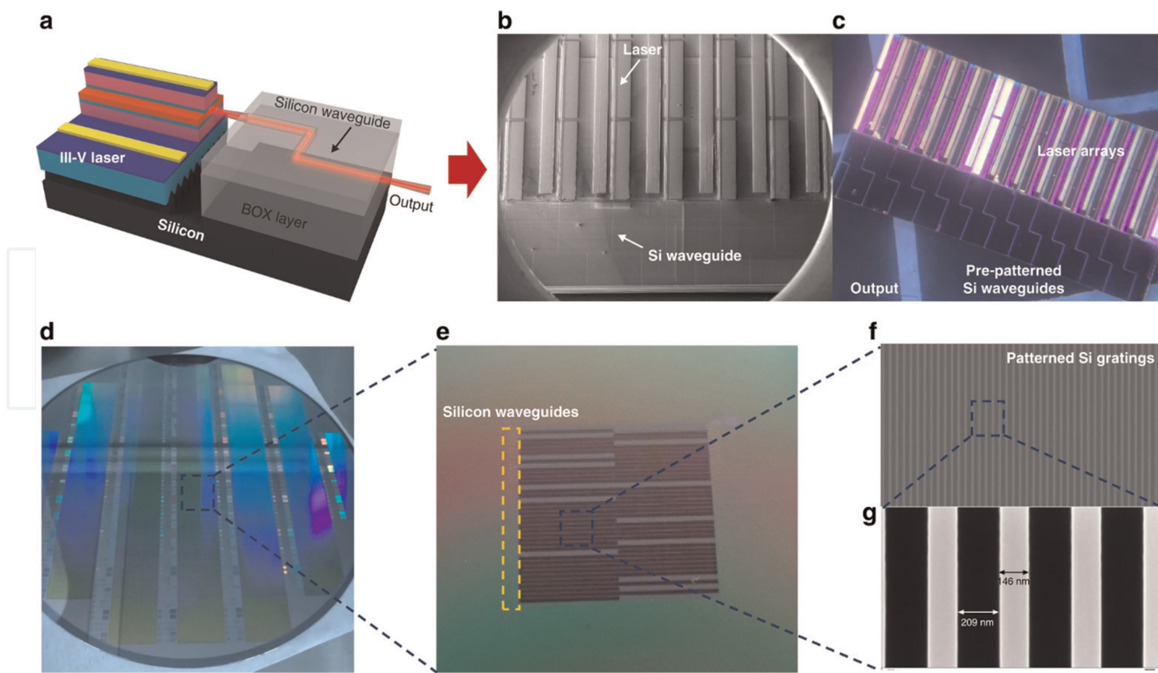

Figure 21.
(a) Schematic image of butt coupling between laser structure and Si waveguide. (b), (c) SEM and microscope images of trenched InAs/GaAs laser structure with prepatterned Si waveguide. (d)eight-inch wafer with predefined trenches and waveguides. (e) Microscope images of trenches for laser epitaxy and embedded Si waveguide. (f) and (d) patterned Si grating with 146 nm slab width and 209 nm gap for Si homoepitaxy and form Si {111} surfaces. *©2023 the authors under CC BY.*

and the periodic Si gratings are patterned inside the trench with 146 nm slab width and a 209 nm gap, as demonstrated in **Figure 21(d)** and **(e)**.

Instead of using a commercially available 200 nm GaP/Si template, Wei et al. adopted homoepitaxy of Si on the grating-patterned SOI trenches, which forms Si {111} facets to prevent the formation of APBs [46, 101]. The trenched laser is demonstrated in **Figure 22(a)**. A combination of a thin AlAs nucleation layer, a 2.1 μm GaAs

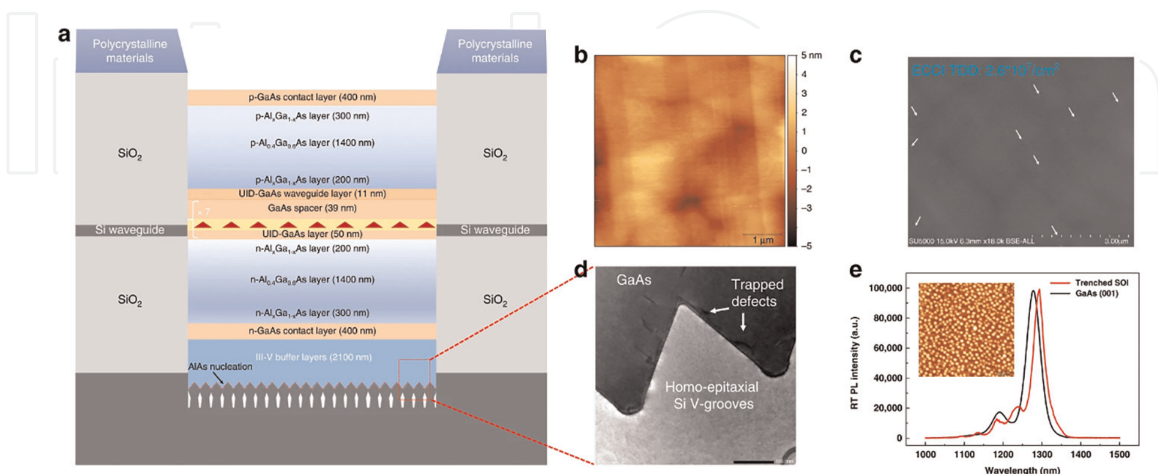

Figure 22.
(a) Schematic image of the trenched laser structure. (b) 5 × 5 μm² AFM image of 2.1 μm GaAs buffer layer. (c) TDD of 2.6 × 10⁷ cm⁻² is obtained for the GaAs buffer layer. (d) Cross-sectional TEM image of GaAs/Si (111) interface. (e) Comparison of PL measurement of trenched QD laser and blanket GaAs (001) laser with identical growth structure. Inset: Surface morphology of grown InAs/GaAs QDs of trenched laser. *©2023 the authors under CC BY.*

buffer layer consisting of InGaAs/GaAs DFLs, and GaAs/AlAs SLSs was adopted to reduce TDD to 2.6×10^7 cm^{-2} while maintaining low surface roughness of 0.8 nm in a 5×5 μm^2 AFM scan, as shown in **Figure 22(b)–(d)**. The active region consists of seven stacks of InAs/GaAs DWELL structure separated by 39 nm GaAs space layers, sandwiched by 400 nm GaAs contact layers and $Al_{0.4}Ga_{0.6}As$ cladding layers. A step-graded AlGaAs layers were also adopted to enhance the current injection efficiency. A comparison of PL measurements between a laser with an identical structure grown on a trench and a GaAs (001) is given in **Figure 22(e)**. A similar PL intensity with a narrow FWHM of 33 nm is observed for trenched laser, attributed to high density and high uniform QDs, as shown in the inset of **Figure 22(e)**.

In this study, H_3PO_4:H_2O_2:H_2O (1:2:20) wet etching was applied to remove unwanted polycrystalline III-V materials before fabrication. The trenched laser was processed with one-side cleaved and coated with a high-reflection coating. While the other side implements wet etch followed by two-step focused ion beam milling to produce high-quality facets. A High-performance trenched QD laser was fabricated with c.w. lasing up to 85°C, low threshold current of 50 mA and maximum output power of 37 mW at an injection current of 250 mA. Butt coupling efficiency between QD active region and Si waveguide was determined. A maximum power of 6.8 mW was measured at the end tip of the Si waveguide, indicating ~ -6.7db coupling efficiency. A further improvement in coupling efficiency can be achieved by using an advanced silicon spot-size converter with precise control of the gap between the facet and the waveguide. This laser offers a prospective technique for realizing an on-chip light source for Si-based PICs.

3.1 Summary

Demonstrating high-performance trenched QD lasers shapes the faith in realizing the monolithic integration of III-V lasers for Si-based PICs as on-chip sources. It paves the way toward large-scale, high-density, low-cost PICs for the forthcoming bloom of quantum and sensing technologies.

4. Conclusions

Heteroepitaxial growth of III-V materials onto Si substrates offers an appealing approach for achieving practical Si-based on-chip light sources. Because of the large lattice mismatch between III-V materials and Si, the formation of crystal defects, including TDs, APBs, and micro-cracks, is inevitable during the epitaxy. Over the past decades, great advances in growth techniques have been made to control these defects to a reasonably low value, and state-of-the-art techniques are reviewed in this chapter. Hence, the performance of InAs QD laser grown on Si substrates progresses rapidly in terms of threshold current, maximum working temperature, and reliability. A step further is urgent to migrate these techniques into Si-based PICs, which are primed to support the growing market of automotive, sensing techniques, and quantum technologies. In order to integrate the InAs/GaAs QD light source on Si-based PICs, SAG growth of laser structure on a trenched substrate and butt-coupled to the embedded, prepatterned waveguide is regarded as a promising candidate for realizing on-chip light sources. Though only a few reports have demonstrated a demo for coupling light from trenched InAs QDs active region into the waveguide, the initial results are promising, which shapes the faith of achieving monolithic integration of III-V lasers as

an on-chip light source. The realization of Si-based PICs will undoubtedly unleash the great potential of emerging technologies in the near future.

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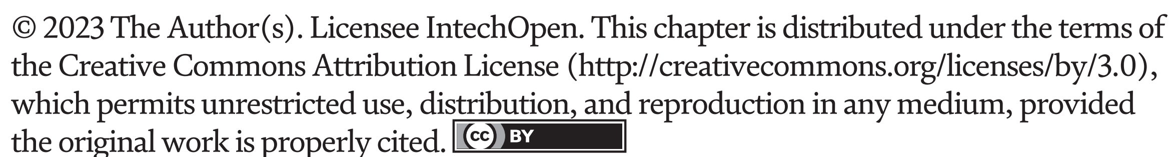
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