Chapter

Introductory Chapter: Computer Memory and Data Storage

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1. Introduction

Memory subsystems play a significant role in high-performance processors, occupying a considerable portion of the die area. Consequently, they have a profound impact on the overall energy, area, and performance of modern computing systems [1]. This necessitates the development of low-power, reliable, and high-performance memory solutions to cater to the needs of emerging applications.

Various solutions have been explored to address power consumption concerns. For instance, scaling complementary metal-oxide-semiconductor (CMOS) logic circuits offers improvements in power consumption, area utilization, and speed. However, aggressive voltage scaling increases the likelihood of memory failures. Thus, further reducing the supply voltage poses a risk to the accuracy of computations. Consequently, it is crucial to implement techniques that effectively handle reliability issues associated with low-power designs in such systems [2, 3].

Motivated by these challenges, this book focuses on memory designs and explores the techniques to minimize power consumption while enhancing performance and reliability. Readers will gain insights into recent advancements in computer memory and data storage through investigation and analysis. By engaging with this resource, they will stay updated on the latest developments in computer memory and data storage.

2. Balancing performance and energy efficiency in cache memory design: Voltage scaling and power management strategies

Cache design plays a critical role in optimizing memory access efficiency in modern processors [1]. One commonly used type of cache is SRAM (Static Random-Access Memory), which offers fast access times and is commonly employed in cache hierarchies. However, in the pursuit of low-power memory design, innovative techniques are being explored to reduce power consumption in SRAM-based caches. These techniques include voltage scaling, where the supply voltage to the SRAM cells is reduced, as well as adaptive power gating, which selectively shuts down portions of the cache when not in use [4]. By incorporating such low-power design methodologies, cache systems can achieve a balance between performance and energy efficiency, contributing to overall system power savings while maintaining satisfactory memory access speeds [5].

Voltage scaling is a popular approach employed to reduce power consumption in memory subsystems. Operating at lower voltages significantly decreases power

dissipation, leading to improved energy efficiency. However, voltage scaling brings challenges such as increased vulnerability to soft errors caused by radiation-induced particle strikes [2, 3]. To counter this, radiation hardening techniques are employed to enhance the resilience of SRAM cells against such errors. These techniques, such as redundant circuitry, error correction codes, and error detection and correction mechanisms, are employed to ensure reliable operation even in radiation-prone environments [6–10].

3. Reliable radiation-hardened memories: Design methodologies and techniques

Radiation hardening is a critical aspect of ensuring the reliability and robustness of electronic systems, particularly in demanding environments such as space applications. In space, electronic systems are exposed to high-energy particles that can cause significant damage and errors [3]. These particles can come from the sun, cosmic rays, and other sources, and they can cause single-event upsets (SEUs) or multiple-event upsets (MEUs) in electronic systems.

If a radiation strike impacts a node of an SRAM cell and modifies its stored data, it results in a phenomenon called Single Event Upset (SEU) [2]. This occurrence takes place when the charge delivered by the particle strike at the affected node exceeds the critical charge, known as Qcrit. Qcrit represents the minimum charge required to alter the data state stored within the SRAM cell [11]. If two or more neighboring nodes collectively receive and contribute to the deposited charge causing a state change, it is referred to as a Multi Event Upset (MEU) [11]. To address these challenges, radiation hardening techniques are employed in SRAM design.

Redundancy is a common approach wherein additional circuitry is incorporated to detect and correct errors. Error correction codes (ECC) are widely used to identify and correct bit errors, ensuring data integrity [7].

Moreover, techniques like triple modular redundancy (TMR) are employed to enhance system reliability [6]. TMR involves triplicating the circuitry and comparing the outputs to identify and correct errors. This redundancy adds an extra level of fault tolerance, ensuring reliable operation in the presence of radiation-induced errors.

Various techniques have been developed to mitigate Single Event Upset (SEU) issues in radiation-hardened memory cell designs [3]. Although conventional solutions such as ECC, DMR [8], and TMR have been used at the architectural level, they suffer from significant area overhead, power consumption, and increased system complexity, making them unsuitable for small memory blocks, particularly at low voltage levels [12]. In contrast, circuit-level techniques offer a more efficient approach by improving SEU immunity without architectural overhead, resulting in reduced area overhead, delay, and power consumption [3, 13–16].

However, previous designs exhibit various trade-offs in terms of SEU tolerance, critical charge, access time, area overhead, and recovery time. For example, some designs offer SEU tolerance but have a low critical charge (Qcrit) [15, 17] or high read access time [18]. Others address SEU tolerance but come with high area overhead [19], while some have limitations in SEU recovery and MEU immunity [14, 15]. Researchers continue to explore new techniques to develop memory cells that can offer improved radiation robustness while minimizing these trade-offs, especially for space applications and other scenarios requiring high reliability and efficiency.

4. Emerging non-volatile memory technologies: Overcoming limitations of existing technologies

Moore's law, which has significantly enhanced computing technology through technology scaling, has also brought about unintended consequences such as the heightened impact of radiation on SRAM cells. This is due to the increased susceptibility of transistors to noise at lower supply voltages and smaller feature sizes [2]. As a result, researchers are exploring alternative approaches to sustain continued scaling endeavors, leading to the emergence of non-volatile memory technologies.

These technologies, such as Flash memory, RRAM, and PCM, offer the advantage of data retention even when power is removed and are used in storage systems, solid-state drives, and embedded systems where persistent data storage is essential [20]. While non-volatile memories like Flash memory have been widely used in various applications, emerging non-volatile memory technologies such as MRAM, FeRAM, and STT-RAM are gaining attention due to their unique properties, such as non-volatility, high endurance, fast access times, high density, low power consumption, and fast write speeds [20, 21].

These emerging technologies have the potential to overcome some of the limitations of existing technologies. However, they also face challenges such as high production costs and scalability issues, which researchers are actively working to address and improve the performance and reliability of these technologies. Thus, the emergence of non-volatile memory technologies represents a promising alternative approach to sustain continued scaling endeavors and overcome the limitations of existing technologies [22].

5. Conclusion

In summary, the design of memory systems encompasses several key aspects, such as voltage scaling to reduce power consumption, radiation hardening to enhance resilience against soft errors, variation-aware design to address process variations, low-power cache design for improved energy efficiency, fault-tolerant memory design to ensure reliable operation, and the adoption of emerging technologies that have the potential to overcome limitations of existing technologies. By incorporating these techniques, memory systems can achieve high performance, low power consumption, resilience to radiation-induced errors, and robustness against various fault conditions, effectively meeting the demands of modern computing applications.

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References

[1] Hennessy JL, Patterson DA. Computer Architecture: A Quantitative Approach. 6th ed. Cambridge, MA, United States: Morgan Kaufmann; 2020

[2] Lin D, Xu Y, Liu X, Zhu W, Dai L, Zhang M, et al. A novel highly reliable and low-power radiation hardened SRAM bit-cell design. IEICE Electronics Express. 2018;**15**(3):20171129

[3] Seyedi A, Aunet S, Kjeldsberg PG. Nwise and Pwise: 10T radiation hardened SRAM cells for space applications with high reliability requirements. IEEE Access. 2022;**10**: 30624-30642

[4] Kaxiras S, Martonosi M. Computer Architecture Techniques for Power-Efficiency. San Rafael, CA, USA: Morgan and Claypool; 2008

[5] Seyedi A, Armejach A, Cristal A, Unsal OS, Valero M. Novel SRAM bias control circuits for a low power L1 data cache. In: Proceeding of NORCHIP. Copenhagen, Denmark; 2012. pp. 1-6

[6] Sterpone L, Violante M. Analysis of the robustness of the TMR architecture in SRAM-based FPGAs. IEEE Transactions on Nuclear Science. 2005; **52**(5):1545-1549

[7] Bajura MA, Boulghassoul Y, Naseer R, DasGupta S, Witulski AF, Sondeen J, Stansberry SD, Draper J, Massengill LW, Damoulakis JN. Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs. IEEE Transactions on Nuclear Science. 2007; **54**(4):935-945

[8] Teifel J. Self-voting dual-modular-redundancy circuits for single event-transient mitigation. IEEE Transactions on Nuclear Science. 2008;**55**(6):3435-3439

[9] Seyedi A, Yalcin G, Unsal O, Cristal A. Circuit design of a novel adaptable and reliable L1 data cache. In: Proceedings of the 23rd ACM International Conference on Great Lakes Symposium on VLSI (GLSVLSI). Paris, France. 2013. pp. 333-334

[10] Yalcin G, Seyedi A, Unsal O, Cristal A. Flexicache: Highly reliable and low power cache under supply voltage scaling. High Performance Computing. 2014;**1**:173-190

[11] Lin S, Kim Y, Lombardi F. Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset. IEEE Transaction on Device Materials Reliability. 2012;**12**(1):68-77

[12] Giterman R, Atias L, Teman A. Area and energy-efficient complementary dual-modular redundancy dynamic memory for space applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2017;**25**(2): 502-509

[13] Seyedi A, Aunet S, Kjeldsberg PG. Nwise: An area efficient and highly reliable radiation hardened memory cell designed for space applications. In: Proceeding of IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC). Helsinki, Finland; 2019. pp. 1-6

[14] Jahinuzzaman SM, Rennie DJ, Sachdev M. A soft error tolerant 10T SRAM bit-cell with differential read capability. IEEE Transaction on Nuclear Science. 2009;**56**(6):3768-3773

[15] Guo J, Zhu L, Sun Y, Cao H, Huang H, Wang T, et al. Design of area-efficient and highly reliable RHBD 10T

memory cell for aerospace applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2018;**26**(5): 991-994

[16] Jung I-S, Kim Y-B, Lombardi F. A novel sort error hardened 10T SRAM cells for low voltage operation. In: Proceeding of IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS). Boise, ID, USA. 2012. pp. 714-717

[17] Jiang J, Xu Y, Zhu W, Xiao J, Zou S. Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications. IEEE Transactions on Circuits and Systems I: Regular Papers. 2019;**66**(3): 967-977

[18] Calin T, Nicolaidis M, Velazco R. Upset hardened memory design for submicron CMOS technology. IEEE Transactions on Nuclear Science. 1996; **43**(6):2874-2878

[19] Pal S, Mohapatra S, Ki W-H, Islam A. Soft-error-immune read stability-improved SRAM for multi-node upset tolerance in space applications. IEEE Transactions on Circuits and Systems I: Regular Papers. 2021;**68**(8): 3317-3327

[20] Chen A. A review of emerging non-volatile memory (NVM) technologies and applications. Solid-State Electronics. 2016;**125**:25-38

[21] Meena JS, Sze SM, Chand U, Tseng T-Y. Overview of emerging nonvolatile memory technologies. Nanoscale Research Letters. Sep 25 2014; **9**(1). Article number: 526 (2014)

[22] Wong HS, Salahuddin S. Memory leads the way to better computing. Nature Nanotechnology. 2015;**10**: 191-194