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Investigation on Single and Split Output Gate Configurations Influence on the GaN-HEMTs Switching Behaviours

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***Index Terms*—Gallium Nitride (GaN), HEMTs, Intelligent gate driver, Parasitic elements, Switching losses.**

***Abstract*—This work investigates the power GaN-HEMTs switching behaviour differences resulted from usage of two gate driving configurations: single and split outputs. The analysis based on simulation and experimental results show that GaN-HEMTs could switch slower and cause higher switching losses when the split output configuration is used. This is because the output capacitance (C_{oss}) of MOSFETs inside gate driver will be charged during the turn-on process of GaN-HEMTs, and this charging process can reduce the charging speed of input capacitance (C_{iss}) of GaN-HEMTs. Moreover, the gate resistance and parasitic inductance are the main parameters selected for analysis, and their distribution can amplify this effect by increasing the impedance ratio of turn-on and turn-off loop. This research provides guiding suggestions for gate driver and high-efficiency GaN-HEMTs power module design.**

I. Introduction

Gallium nitride high-electron-mobility transistors (GaN-HEMTs) are attracting high interests in power electronics [1], [2]. As a result of the small relative permittivity of GaN material and the device dimension, the inter-electrode capacitance of power GaN-HEMTs can be low, giving rise to the fast switching speed and low switching losses, which is a desired property for high-frequency applications [3]. Therefore, the GaN-HEMTs are good candidates for high-power-density and high-efficiency power converters.

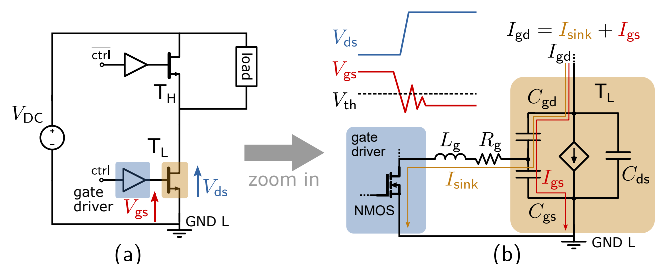

Fig. 1. Half-bridge (a) and false-turn-on principle (b)

However, the fast switching speed and low power losses of GaN-HEMTs are not without a price, which coexists with the negative threshold voltage (V_{th}) as the depletion-mode device [4]. Thanks to the p-GaN gate technology, the V_{th} of enhancement-mode GaN-HEMTs is elevated to around 1.5 V [5], [6], however, it is still low compared to the Silicon metal-oxide semiconductor field-effect transistors (Si-MOSFETs). Moreover, GaN-HEMTs suffer from V_{th} instability phenomena with voltage bias, and the V_{th} could be even lower after long V_{gs} bias time or during high V_{ds} bias [7]–[9]. Therefore, the device is easily to be turned on by the switching ringing [10]. For example, when GaN-HEMTs operating in the half-bridge circuit, the high-side (T_{H}) and low-side device (T_{L}) will turn on complementarily as shown in Fig. 1(a). When the T_{L} turns off, both of the drain to source capacitance (C_{ds}) and gate to drain capacitance (C_{gd}) will be charged by the load current. Among them the C_{gd} charging current I_{gd} is sunk by the on-state n-channel MOSFET (NMOS) in gate driver noted as I_{sink} or keeps charging gate to source capacitance (C_{gs})

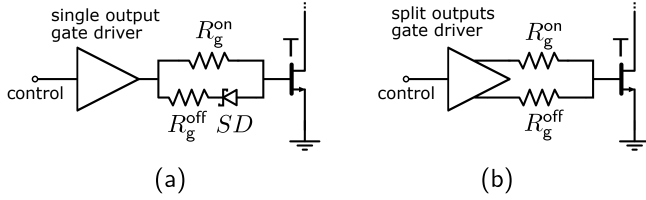

Fig. 2. Single output (a) and split output (b) gate configurations

forming I_{gs}, as shown in Fig. 1(b). However, the gate parasitic inductance (L_g) can limits the I_{sink} rising speed, inducing voltage drop, which further resonates with the GaN-HEMTs input capacitance ($C_{iss} = C_{gs} + C_{gd}$). This resonated switching ringing could make V_{gs} exceed V_{th}, leading to the false-turn-on of T_L. Just after a small dead time, the T_H is turned on, which can cause cross conduction of these two devices in half-bridge, resulting in high power losses or even device destruction. Moreover, applying negative gate sink voltage to prevent the false-turn-on is undesirable for GaN-HEMTs, as it increases the reverse on-state resistance, leading to higher reverse conduction losses [11].

The key to solving the false-turn-on and avoiding cross conduction in half-bridge is reducing the impedance of turn-off loop, for example, a smaller R_g^{off} can be applied as shown in Fig. 2(a). However, a Schottky diode has to be used to separate the turn-on and turn-off loop impedance, giving rise to around $0.2\,\text{V}$ forward voltage drop (V_{Diode}), which cannot be neglected when compared with the V_{th} ($1.5\,\text{V}$) of GaN-HEMTs. Therefore, the split output gate driver is suggested to drive the GaN-HEMTs [12], [13], as depicted in Fig. 2(b), since the Schottky diode in turn-off loop is not required. Consequently, not only the V_{Diode} can be eliminated but also the gate circuitry can become more compact to reducing the L_g, which design is ideal for the high-efficiency integrated power module [14].

Many works have focused on the active gate driver technologies [13], [15], [16] or gate loop optimization for small L_g [14], [17] to improve drive efficiency and fully release the fast switching performance of wide-bandgap power devices. However, only a small amount of studies have concentrated on the impact of gate driver topologies on device switching performance [18]–[21], although it is of high interests for gate driver selection and GaN-based high-efficiency power module design. In this work, the driving performance of the single and split output gate driver and their corresponding circuitry for GaN-HEMTs are investigated. The results suggest that the turn-on commutation speed of GaN-HEMTs could be reduced by using the split output gate configuration

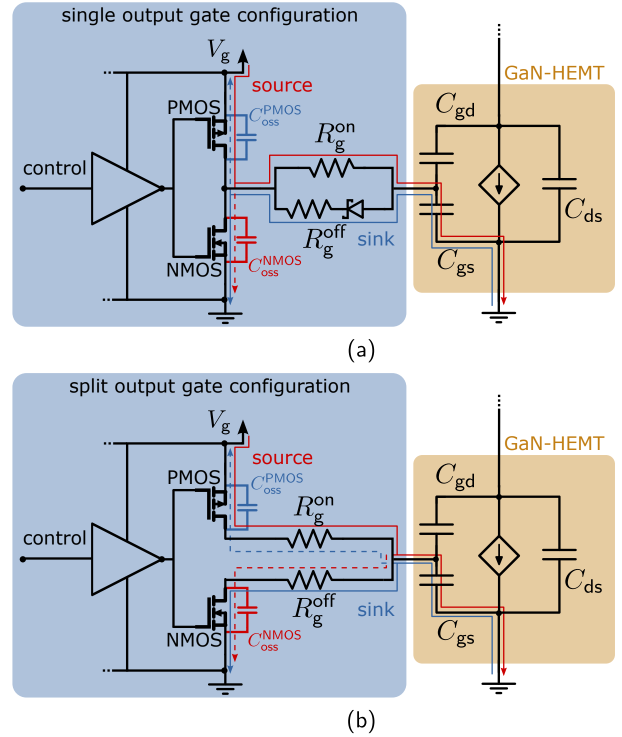

Fig. 3. Turn-on and turn-off (source and sink) loop of single (a) and split output (b) gate configurations for power GaN-HEMTs driving

compared to the single output configuration.

This paper is structured as follows: Section II illustrates the possibility and mechanism of the impact of different gate driver output topologies on the GaN-HEMTs switching behaviours by proposing the equivalent schematics. Afterward, the impact of gate loop resistance and parasitic inductance on this effect is analysed. In Section III, the SPICE simulation is applied to support the theoretical analysis and evaluate the switching losses caused by using different gate configurations. In Section IV, the double-pulse test (DPT) is implemented to verify the simulation results by modifying the commercial available gate driver output topologies. The conclusion is given in Section V.

II. Mechanism of Gate Configurations on GaN-HEMTs Charging Process

It is voltage across C_{gs} (V_{gs}) that turns on and off the GaN-HEMTs and the V_{gs} is sourced and sunk by gate drivers. This process is completed by switching on n-channel MOSFETs (NMOS) and p-channel MOSFETs (PMOS) complementarily in the gate driver as depicted in Fig. 3, where the source and sink loop are showed as solid arrow lines. During the turn-on transient of GaN-HEMTs, the PMOS in gate driver is turned on to allow gate voltage (V_g) to charge the C_{gs}. At this stage,

the NMOS is in off-state, and its output capacitance ($C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$) also get charged by the V_{g} as highlighted by the dashed red line in Fig. 3. Consequently, it provides a possibility that the charging process of C_{oss} in NMOS ($C_{\text{oss}}^{\text{NMOS}}$) could slow down the sourcing speed of C_{gs} of GaN-HEMTs, as the charging current is shunted. Dually, the sinking speed of C_{gs} can also be reduced by the charging process of C_{oss} of PMOS ($C_{\text{oss}}^{\text{PMOS}}$). Thus, the switching behaviour of GaN-HEMTs might be influenced.

The impact of the gate driver MOSFETs can be neglected when driving the Silicon (Si) or Silicon Carbide (SiC) power MOSFETs. Because the C_{iss} of these power MOSFETs can be up to several nano Farad [22], [23], which is far more larger than the C_{oss} of Si-MOSFETs in gate drivers [12]. However, the C_{iss} of power GaN-HEMTs ($C_{\text{iss}}^{\text{GaN}}$) has been reduced noticeably, which can be close to the C_{oss} of gate driver MOSFETs as compared in Table I and II. To be noted that the Si-MOSFETs in Table II are selected based on their V_{DS} and I_{D} values that are in the same range as maximum supply voltage (V_{DD}), sink (I_{sink}) and source current (I_{source}) of commercial gate drivers for GaN-HEMTs. The gate drivers supporting the previous mentioned GaN-HEMTs are given in Table III. To be noted, the I_{D} in Table II refers to continuous current, while the I_{sink} and I_{source} in Table III indicate pulsed current. Since the pulsed current is around 3 to 4 times higher than the continuous current, the Si-MOSFETs in Table II are in the same power range as the Si-MOSFETs in gate driver in Table III. Moreover, the $C_{\text{oss}}^{\text{NMOS}}$ of LM5114 and 1EDN7511B gate driver are measured in Section III, aligning with the C_{oss} range presented in Table II. As shown in Table I and II, some C_{oss} of the low power MOSFETs are even larger than the $C_{\text{iss}}^{\text{GaN}}$. This aspect could influence the GaN-HEMTs switching behaviours and as it represents an important part, which will be expanded below.

A. Mechanism of driving performance difference from single and split output gate configurations

In fact, when GaN-HEMTs are driven by the single output gate configuration, and if the L_{g} is neglected, the equivalent circuit of turn-on loop can be considered as a simple RC circuit, shown in Fig. 4(a). The charging loop of $C_{\text{oss}}^{\text{NMOS}}$ is omitted, since it gets charged very quickly, compared to the charging process of $C_{\text{iss}}^{\text{GaN}}$. By contrast, the split output gate configuration can be regarded as a two-stage cascade RC circuit as the $R_{\text{g}}^{\text{off}}$ in turn-off loop is included as depicted in Fig. 4(b). In this cascade topology, the $C_{\text{iss}}^{\text{GaN}}$ and $C_{\text{oss}}^{\text{NMOS}}$ will be charged to V_{g} simultaneously, interacting with each other during the charging process. Hence, the charging process of $C_{\text{iss}}^{\text{GaN}}$ can be influenced by the $C_{\text{oss}}^{\text{NMOS}}$ value and this mechanism can be illustrated by simulation. For simplification, linear capacitances are adopted as $C_{\text{oss}}^{\text{NMOS}}$, and the parasitic inductance L_{g} is neglected. A single pulse voltage source V_{g} with $2\,\text{ns}$ of rise time (t_{r}^{g}) is used as the output voltage of gate driver in the simulation. The rise time value is based on the power GaN-HEMTs gate driver [24]. The value of $C_{\text{oss}}^{\text{NMOS}}$ sweeps from 0 to $240\,\text{pF}$ in step of $60\,\text{pF}$ and these values

TABLE I
C_{iss} OF COMMERCIAL POWER GAN-HEMTS

Devices	Model	V_{DS} (V) / I_{D} (A)	C_{iss} (pF)
GaN-HEMTs	GS66502B	650 / 7.5	60
	GS66504B	650 / 15	120
	GS66508B/T	650 / 30	240
	IGLR60R340D1	600 / 8	87.7
	IGLR60R260D1	600 / 10	110
	IGO60R070D1	600 / 30	380
	SGT120R65AL	650 / 15	125
	SGT65R65AL	650 / 25	286

* Data in this table is from the manufacturer datasheet.
** C_{iss} is measured when V_{DS} is $400\,\text{V}$ and V_{GS} is $0\,\text{V}$.

TABLE II
C_{oss} OF COMMERCIAL LOW POWER SI-MOSFETS

Devices	Model	V_{DS} (V) / I_{D} (A)	C_{oss} (pF)
N-Chanel Si-MOSFETs	Si1050X	8 / 1.34	190
	CSD13381F4	12 / 2.1	47
	CSD13201W10	12 / 1.6	245
	PMXB40UNE	12 / 3.2	107
P-Chanel Si-MOSFETs	Si1499DH	-8 / -1.6	220
	RZF020P01	-12 / -2	75
	CSD13201W10	-12 / -1.6	73
	DMP1200UFR4	-12 / -2	131

* Data in this table is from the manufacturer datasheet.
** C_{oss} is measured under half of rated V_{DS} voltage and $0\,\text{V}$ of V_{GS}.

TABLE III
COMMERCIAL LOW-SIDE GATE DRIVERS FOR POWER GAN-HEMTS

Model	Max. V_{DD} (V)	I_{sink}(A) / I_{source} (A)	Output
LM5114	12.6	7.6 / 1.3	Split
UCC27511	18	8 / 4	Split
UCC27512	18	8 / 4	Single
1EDN7511B	10	8 / 4	Split
1EDN7512B	10	8 / 4	Single

* Data in this table is from the manufacturer datasheet.

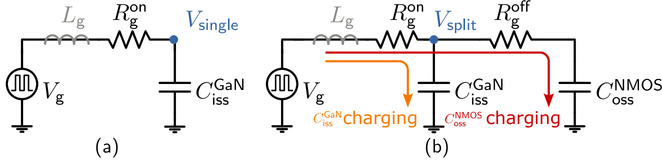

Fig. 4. Equivalent circuit of GaN-HEMTs charging process using single output (a) and split output (b) gate configurations

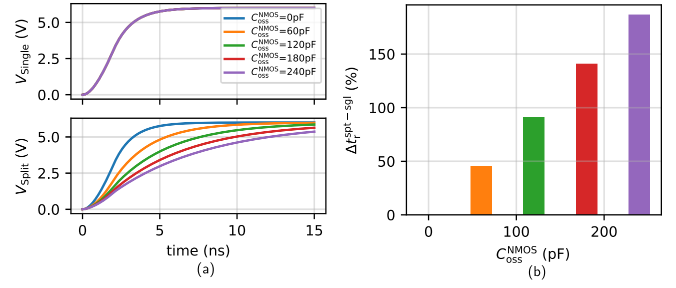

Fig. 5. Simulation charging waveforms (a) and $\Delta t_r^{\text{spt-sgl}}$ (b) of C_{iss}^{GaN} in single and split output configurations with various C_{oss}^{NMOS}

TABLE IV
SIMULATION PARAMETERS OF INVESTIGATING C_{oss}^{NMOS}

$R_g^{on} = 20\,\Omega$	$R_g^{off} = 2\,\Omega$	$C_{iss}^{GaN} = 60\,\text{pF}$	$V_g = 6\,\text{V}$	$L_g = 0\,\text{H}$

are in the same range of the C_{oss}^{NMOS} in commercial gate drivers. Other simulation parameters are listed in Table IV. The charging voltage of C_{iss}^{GaN} in these two different configurations (V_{single} and V_{split}) is shown in Fig. 5(a). The rise time of V_{split} is increased by C_{oss}^{NMOS} increasing, while the rise time of V_{single} remains constant. To quantify this differentiation, the rise time of V_{single} and V_{split} from 0 to 3.6 V (63 % of V_g) is respectively defined as t_r^{single} and t_r^{split}. Afterward, the relative change rate of t_r^{single} and t_r^{split} ($\Delta t_r^{\text{spt-sgl}}$) can be calculated:

$$\Delta t_r^{\text{spt-sgl}} = \frac{t_r^{split} - t_r^{single}}{t_r^{single}} \times 100\,\% \tag{1}$$

the $\Delta t_r^{\text{spt-sgl}}$ under different C_{oss}^{NMOS} is displayed in Fig. 5(b), which shows that the rising speed of V_{split} is slower than the V_{single} and this difference becomes prominent with the C_{oss}^{NMOS} increasing. The reason is that the impedance of C_{oss}^{NMOS} charging loop (R_g^{on}, R_g^{off} and C_{oss}^{NMOS}) becomes lower with C_{oss}^{NMOS} increasing, which shunts more current from the C_{iss}^{GaN} charging loop (R_g^{on}, C_{iss}^{GaN}), causing slowly V_{split} increasing.

Therefore, the $\Delta t_r^{\text{spt-sgl}}$ can become large with R_g^{off} decreasing or R_g^{on} increasing as well. This can be supported by sweeping the R_g^{on} and R_g^{off} respectively in Fig. 4. The results are displayed in Fig. 6, where 120 pF of C_{oss}^{NMOS} is selected and other parameters keep the same as shown in Table IV. For conciseness, the impact of C_{oss}^{NMOS} in split output gate configuration on C_{iss}^{GaN} charging process will be defined as split output gate configuration (SPOGC) effect further in this study. This effect can be quantified by $\Delta t_r^{\text{spt-sgl}}$ and the larger $\Delta t_r^{\text{spt-sgl}}$ the more notable SPOGC effect.

B. Impact of L_g and its distribution on SPOGC effect

The gate loop parasitic inductance L_g could also influence the SPOGC effect, as the impedance of C_{iss}^{GaN}

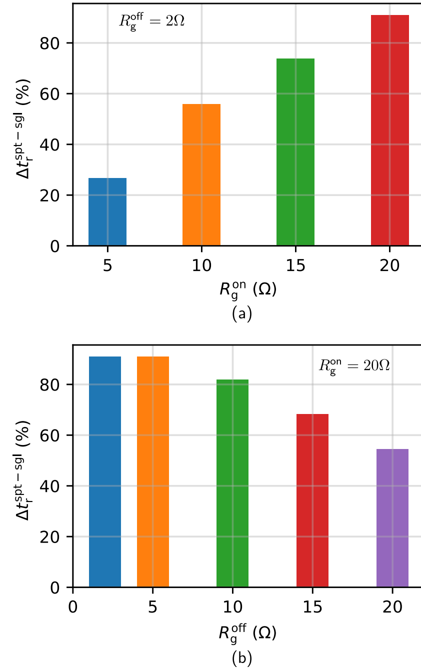

Fig. 6. Relative change rate of rise time (a) with different R_g^{on} at $R_g^{off} = 2\Omega$ and (b) different R_g^{off} at $R_g^{on} = 20\Omega$

charging loop (turn-on loop) and C_{oss}^{NMOS} charging loop (turn-off loop) is also related to the L_g distribution. It should be noted that the lumped L_g in Fig. 4 can not affect the SPOGC effect significantly, as it will not change the impedance ratio of turn-on to turn-off loop notably. This is evaluated by sweeping L_g from 0 nH to 20 nH in Fig. 4 with $C_{oss}^{NMOS} = 120\,\text{pF}$ and another parameters are the same as Table IV. The simulation result of $\Delta t_r^{\text{spt-sgl}}$ is shown in Fig. 7 and the small change of $\Delta t_r^{\text{spt-sgl}}$ can be neglected.

The actual L_g in gate circuitry is not lumped but unevenly distributed in turn-on and turn-off loop [14]. Thus, the impact of distributed L_g on SPOGC effect should be discussed and the cascade RC circuit is employed to evaluate this effect as shown in Fig. 8,

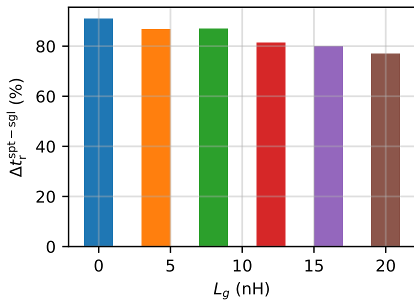

Fig. 7. Simulation result of $\Delta t_{\mathrm{r}}^{\mathrm{spt-sgl}}$ with lumped L_{g} increasing from $0\,\mathrm{nH}$ to $20\,\mathrm{nH}$

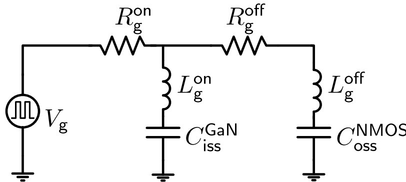

Fig. 8. Equivalent charging circuit of split output gate configuration considering distributed L_{g}

while the equivalent charging circuit of single output topology remains unchanged as shown in Fig. 4(a). The $L_{\mathrm{g}}^{\mathrm{off}}$ sweeps from $2\,\mathrm{nH}$ to $10\,\mathrm{nH}$ in step of $2\,\mathrm{nH}$ and other simulation parameters are listed in Table V. As the simulation results shown in Fig. 9(b), the $\Delta t_{\mathrm{r}}^{\mathrm{spt-sgl}}$ decreases with $L_{\mathrm{g}}^{\mathrm{off}}$ increasing due to the increased impedance in turn-off loop, which is similar to the results after increasing the $R_{\mathrm{g}}^{\mathrm{off}}$ as shown in Fig. 6(b). But the impact of $L_{\mathrm{g}}^{\mathrm{off}}$ on SPOGC effect is more complicated, because fluctuations exist in V_{split} waveforms when considering the L_{g} as shown in Fig. 9(a). In fact, the impact of L_{g} on SPOGC effect is highly related to the $R_{\mathrm{g}}^{\mathrm{on}}$ and $t_{\mathrm{r}}^{\mathrm{g}}$, as these two parameter changes rising speed (equivalent frequency) of $V_{\mathrm{iss}}^{\mathrm{GaN}}$ signal. And the inductive reactance of L_{g} is large with fast signal. Dually, the capacitance reactance of $C_{\mathrm{oss}}^{\mathrm{NMOS}}$ is small in fast charging process. Moreover, the $C_{\mathrm{iss}}^{\mathrm{GaN}}$ and $C_{\mathrm{oss}}^{\mathrm{NMOS}}$ are non-linear capacitance and there exist mutual inductive coupling between the gate and power loop, so the impact of L_{g} on SPOGC effect in different circuits can be different. But in short, the SPOGC effect becomes pronounced with the impedance ratio of turn-on to turn-off loop increasing.

III. SPOGC Effect on GaN-HEMTs Switching Behaviours and Losses in Half-Bridge Switching Simulation

It is of practical significance to investigate the impact of SPOGC effect on GaN-HEMTs switching behaviours considering the proper L_{g} distribution and non-linear

TABLE V
SIMULATION PARAMETERS OF INVESTIGATING L_{g} DISTRIBUTION

$R_{\mathrm{g}}^{\mathrm{on}} = 20\,\Omega$	$R_{\mathrm{g}}^{\mathrm{off}} = 2\,\Omega$	$C_{\mathrm{iss}}^{\mathrm{GaN}} = 60\,\mathrm{pF}$	$C_{\mathrm{oss}}^{\mathrm{NMOS}} = 120\,\mathrm{pF}$
$L_{\mathrm{g}}^{\mathrm{on}} = 5\,\mathrm{nH}$	$t_{\mathrm{r}}^{\mathrm{g}} = 2\,\mathrm{ns}$	$V_{\mathrm{g}} = 6\,\mathrm{V}$	

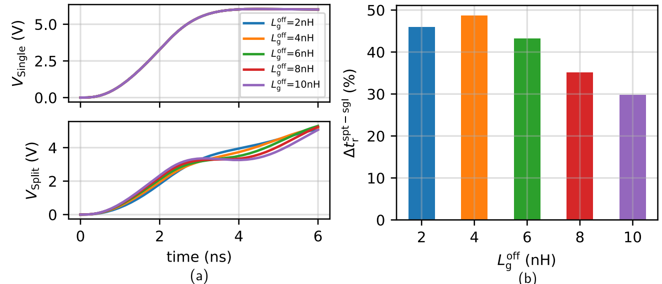

Fig. 9. Simulation charging waveforms (a) and $\Delta t_{\mathrm{r}}^{\mathrm{spt-sgl}}$ (b) of $C_{\mathrm{iss}}^{\mathrm{GaN}}$ in single and split output configurations with various $L_{\mathrm{g}}^{\mathrm{off}}$

$C_{\mathrm{iss}}^{\mathrm{GaN}}$ and $C_{\mathrm{oss}}^{\mathrm{NMOS}}$. Thus, a half-bridge based switching simulation is implemented and the schematic is shown in Fig. 10, where the low-side GaN-HEMT is driven by the customized gate driver model and the high-side device is an ideal freewheeling diode (D_{f}). Only the turn-on process is investigated, since the phenomenon in turn-off is repetitive. The GS66502B SPICE model from GaN Systems is used as the power transistors in this half-bridge. The gate driver model is implemented via ideal switches in parallel with capacitors, performing as the $C_{\mathrm{oss}}^{\mathrm{NMOS}}$ and $C_{\mathrm{oss}}^{\mathrm{PMOS}}$, and the whole ensemble acts as a push-pull gate driver. The reason for adopting ideal switches instead of MOSFET models is advantage to be able to adjust C_{oss} value of the gate driver MOSFETs. To obtain the non-linear C_{oss} of MOSFETs inside the gate driver, the $C_{\mathrm{oss}}^{\mathrm{NMOS}}$ of LM5114 are measured using impedance analyzer E4990A. Afterward, the measured C–V characteristics are modelled and imported to simulation, as shown in Fig. 11. The value of $C_{\mathrm{oss}}^{\mathrm{PMOS}}$ is set to $60\,\mathrm{pF}$, although it will not influence the charging process of $C_{\mathrm{iss}}^{\mathrm{GaN}}$. In addition, the simulation result from single output topology is compared and the non-linear C_{oss} of Schottky diode ($C_{\mathrm{oss}}^{\mathrm{SD}}$) is measured and modelled by the same method as $C_{\mathrm{oss}}^{\mathrm{NMOS}}$ of LM5114. At turn-on transient, the $C_{\mathrm{oss}}^{\mathrm{SD}}$ can allow the rising edge of gate driver output voltage flow through the $R_{\mathrm{g}}^{\mathrm{off}}$ branch due to the smaller impedance compared to the $R_{\mathrm{g}}^{\mathrm{on}}$ branch, accelerating the charging speed of $C_{\mathrm{iss}}^{\mathrm{GaN}}$. However, the Schottky diode is not required in the split output configuration, which means the impedance of turn-off loop in split output configuration is higher

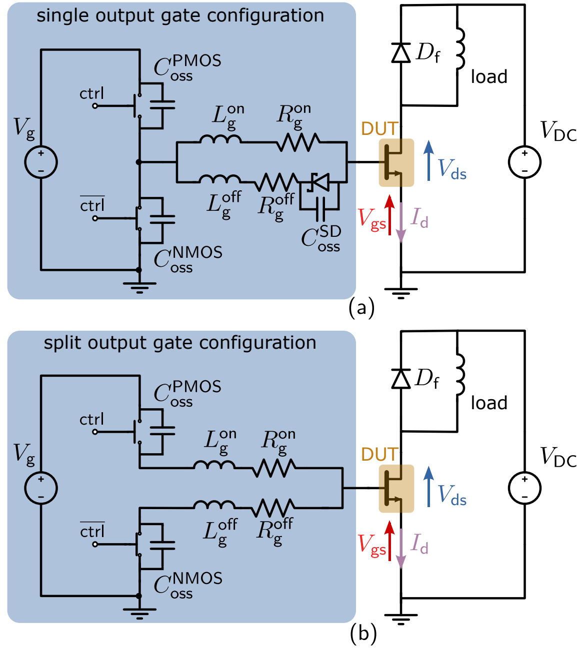

Fig. 10. Customized single (a) and split output (b) gate configurations and half-bridge schematics

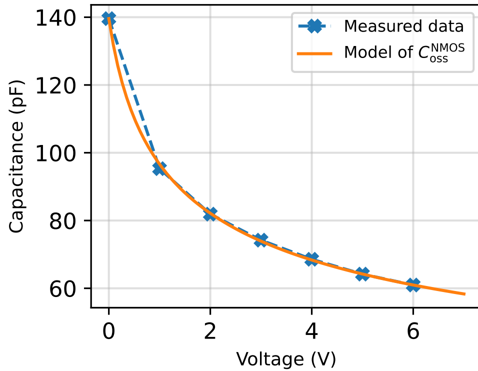

Fig. 11. Measurement and modelling results of C_{oss}^{NMOS} in LM5114 gate driver

than the single output configuration (for rising edge) with same L_g^{off} and R_g^{off}. Hence, the C_{oss} of Schottky diode can accelerate the C_{iss}^{GaN} charging speed in single output configuration, amplifying the difference caused by SPOGC effect. Other parameters are displayed in Table VI and these parameters consider the real gate circuitry, where the value of L_g is normally less than 10 nH [17], [25] and it can be as low as 2 nH in multi-layer PCB GaN-based power module using the split output gate configuration [14]. The simulation switching waveforms of GaN-HEMTs driven by single and split output gate configurations are depicted in Fig. 12. As analysed in section II, the V_{gs} rise speed is decreased

TABLE VI
SIMULATION PARAMETERS OF HALF-BRIDGE SWITCHING

$R_g^{on} = 20\,\Omega$	$R_g^{off} = 2\,\Omega$	$L_g^{on} = 6\,\text{nH}$	$L_g^{off} = 6\,\text{nH}$
$V_{DC} = 100\,\text{V}$	$t_r^g = 2\,\text{ns}$	$V_g = 6\,\text{V}$	$L_{load} = 40\,\text{uH}$

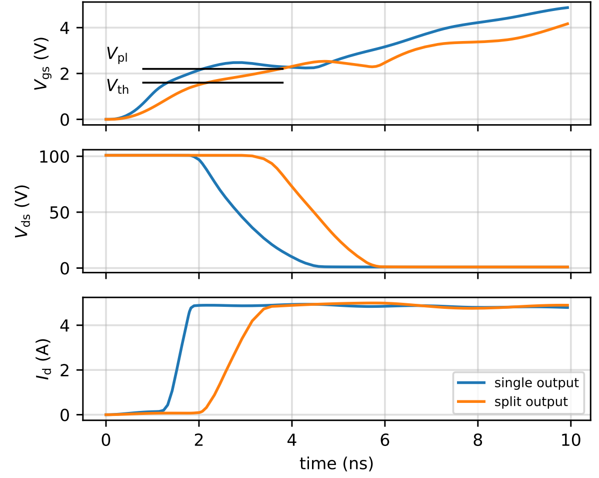

Fig. 12. Turn-on simulation waveforms of split and single output gate configurations in half-bridge

due to the SPOGC effect. Moreover, the I_d rising stage is dependent on the V_{gs} rising time from V_{th} to Miller plateau voltage (V_{pl}). As shown, the I_d commutation transient in the split output gate configuration is extended due to the slow V_{gs} waveform, which can increase the device switching losses. Considering the unknown actual parasitic inductance distribution in gate loop and power loop and their mutual inductive coupling, it is necessary to evaluate the SPOGC effect in experiment.

IV. Experiment Validation

To verify the SPOGC effect and affected switching behaviours, the double-pulse test (DPT) is implemented, adopting the same schematic in Fig. 10. Two GS66502B GaN-HEMTs are used as the freewheeling diode and the device under test (DUT) respectively. However, there is a challenge to choose the single and split output gate drivers with same output characteristics. For example, the C_{oss} of MOSFETs, the pull-down and pull-up resistance from different commercial gate drivers are various. These parameters could influence the source and sink behaviours of the gate driver. More importantly, the pins distribution of the single and split output gate drivers package are not matching, making challenging to drive the GaN-HEMTs under same L_g when using these two different gate configurations. To solve this problem, the source and sink pins of split output gate driver in this

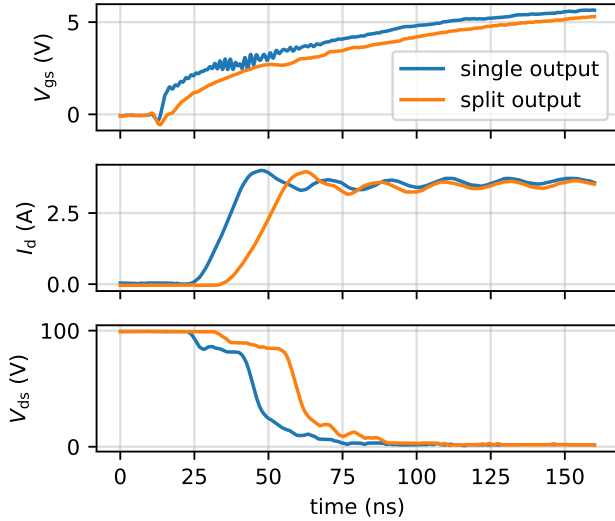

Fig. 13. Measured turn-on switching waveforms result of $R_g^{on} = 200\,\Omega$ with $R_g^{off} = 2\,\Omega$

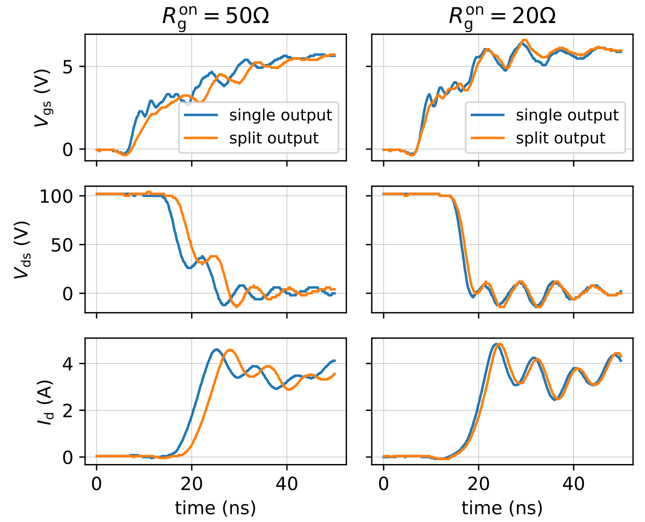

Fig. 14. Measured turn-on switching waveforms result of $R_g^{on} = 50\,\Omega$ and $R_g^{on} = 20\,\Omega$ with $R_g^{off} = 2\,\Omega$

study are connected together to replace the single output gate driver. For the single output gate circuitry, only a Schottky diode is required to be added as shown in Fig. 3. In this way, all parameters' values of the single and split output gate drivers and the L_g in these two gate circuitries can be as close as possible. To evaluate the width of shoot-through current spike (I_{peak}) of the NMOS and PMOS in the modified single output gate driver and avoid device breakdown, a current limiting resistor is necessary to be connected to the source and sink pins before implementing the test. The result shows that the maximum I_{peak} is 2.6 A for 30 ns when V_g is 6 V, which is below the breakdown condition of gate driver given in the datasheet.

The 1-GHz oscilloscope MSO58B is used to record the measured switching waveforms. A 1-GHz passive probe TPP1000 is used to measure the V_{gs}. A 200-MHz differential probe THDP0200 and a 120-MHz Hall-effect current probe TCP0030A are used to measure V_{ds} and I_d, respectively. To be noted, the DUT is biased for 5 minutes under the DC voltage (V_{DC}) at off-state before starting the test to avoid the influence of trapping effect on switching transients [8], [26], [27]. 100 V of V_{DC} is adopted for the DPT to avoid the common-source inductance induced V_{gs} switching ringing in single output configuration, because the gate driver LM5114 is not used in a recommended way (source and sink pins are connected together) and the Kelvin connection is not available in GS66502B device. In addition, the C_{iss}^{GaN} of GS66502B when V_{ds} is 100 V and 400 V are the same [28], [29], so 100 V of V_{DC} is enough to evaluate the SPOGC effect when the GaN-HEMT operating in rated voltage. A 200 Ω R_g^{on} is firstly used to evaluate the SPOGC effect. The turn-on switching waveforms are illustrated in Fig. 13. The V_{gs} rising time of the GaN-HEMT driven by the split output is reduced notably when compared to the single output configurations, especially in the initial rising stage. Correspondingly, the V_{ds} and I_d are slowed and delayed as the previous simulation results. The experiment results from different R_g^{on} are shown in Fig. 14.

The relative change of turn-on switching energy E_{on} of these two gate configurations can be used to outline the impact of SPOGC effect on device switching behaviours:

$$E_{on} = \int_{t_1}^{t_2} V_{ds}(t) I_d(t)\, dt \tag{2}$$

$$\text{Relative Change} = \frac{E_{on}^{split} - E_{on}^{single}}{E_{on}^{single}} \times 100\,\% \tag{3}$$

where the t_1 and t_2 are the time when I_d and V_{ds} are at 10 % of maximum value respectively. When $R_g^{on} = 200\,\Omega$, the SPOGC effect can cause about 22 % more E_{on}. When R_g^{on} is 50 Ω, the SPOGC effect is less preeminent compared with the large R_g^{on}, causing about 14 % more E_{on}. When R_g^{on} is 20 Ω, similar results are recorded, however, in a low scale, causing only around 4 % difference. These results support the analysis conclusion that SPOGC effect is pronounced with the impedance ratio of turn-on to turn-off loop increasing.

However, the measured SPOGC effect when $R_g^{on} = 20\,\Omega$ is less pronounced than that in simulation as shown

in Fig. 12. This difference could be explained by a number of factors:

1) The $t_{\mathsf{r}}^{\mathsf{g}}$ of the output voltage from LM5114 gate driver is around $10\,\mathrm{ns}$, which is larger than the $2\,\mathrm{ns}$ in simulation. Large $t_{\mathsf{r}}^{\mathsf{g}}$ means that the equivalent frequency of turn-on signal is low. So, the impedance of $C_{\mathsf{iss}}^{\mathsf{GaN}}$ and $C_{\mathsf{oss}}^{\mathsf{NMOS}}$ charging loop is more determined by resistance instead of reactance. Hence, the reactance of $C_{\mathsf{oss}}^{\mathsf{NMOS}}$ becomes higher in large $t_{\mathsf{r}}^{\mathsf{g}}$, leading to lower impedance ratio of $C_{\mathsf{iss}}^{\mathsf{GaN}}$ to $C_{\mathsf{oss}}^{\mathsf{NMOS}}$ charging loop and weak SPOGC effect.
2) The common-source inductance L_{cs}, power loop parasitic inductance L_{d}, and the distribution of L_{g} inside the turn-on and turn-off loop and their magnetic coupling are not considered in this study's simulation. And they might eliminate the SPOGC effect.
3) The V_{ds} and I_{d} switching waveforms are respectively measured by the 200-MHz and 120-MHz probes, providing a cut-off filter for the high-frequency signals. This is why much smaller $R_{\mathsf{g}}^{\mathsf{on}}$ is not used in the experiment.

In support with the above functioning observations, a different gate driver 1EDN7551B [30] is used in the same experimental setup as used for LM5114, which shows the similar result.

V. Conclusion

In this work, the driving performance of the single and split output gate configurations for the GaN-HEMTs is investigated via simulation and experimentation. Since the low value of C_{iss} encountered on the power GaN-HEMTs technology, the $C_{\mathsf{oss}}^{\mathsf{NMOS}}$ and $C_{\mathsf{oss}}^{\mathsf{PMOS}}$ in the split output gate configurations could influence the switching behaviour of the GaN-HEMTs, this could lead to higher switching losses, defining the SPOGC effect outlined by this study. As analysed, the impedance ratio of turn-on to turn-off loop in split output configuration mainly determines the SPOGC effect. Small $R_{\mathsf{g}}^{\mathsf{on}}$ contributed to eliminate the SPOGC effect, which is basically adopted by application engineers. However, small $t_{\mathsf{r}}^{\mathsf{g}}$ (less than $2\,\mathrm{ns}$) gate driver is expected for GaN-HEMTs driving in high-frequency application [24]. In this condition, the impact of gate parasitics inductance on SPOGC effect can be more pronounced. Hence, the SPOGC effect deserved to be noted in high-frequency application. On the other hand, MOSFETs with small C_{oss} are recommanded to choose to eliminate the SPOGC effect when designing the split output gate driver for power GaN-HEMTs.

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