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Integration of Superconducting Fault Current Limiter and DC Circuit Breaker for Electric Aircraft DC Network

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***Abstract*—Large-scale electric aircraft are a promising technology that could revolutionise air travel to reduce the environmental impact. Fault current limitation and interruption technology is crucial to realise the safety and reliability of the electric aircraft, in particular for large-scale electric aircraft using a DC distribution network. This paper proposes to integrate a resistive superconducting fault current limiter (SFCL) with a cryogenic DC solid-state circuit breaker (SSCB) so that the SFCL limits the fault current to acceptable levels in DC networks allowing the SSCB to operate quickly and reliably. A sub-cooled liquid nitrogen cryostat, which can be controlled from 65 K to 77 K, is designed and built for the integration of SFCL and DC SSCB. An SFCL and SSCB prototype is designed and experimentally tested at cryogenic temperatures, which successfully demonstrates the ability to limit and interrupt currents at cryogenic environment.**

***Index Terms*— Cryogenic, DC circuit breaker, sub-cooled liquid nitrogen, superconducting fault current limiter,**

I. Introduction

Aviation industry is seeking disruptive technologies to meet the increasing demand for air travel and to achieve zero carbon emission goals in "Flightpath 2050" [1]. Large-scale electric aircraft are attracting increasing interests due to their low carbon footprint, high efficiency and reduced noise.

Airbus launched the advanced superconducting and cryogenic experimental powertrain demonstrator (ASCEND) project in 2021 to develop a cryogenic electric aircraft propulsion system [2]. Feasibility of high-temperature superconducting and cryogenic technologies are investigated in this project. The ASCEND demonstrator system topology is shown in Fig. 1 and the DC voltage is below 500 V.

In a DC distribution network of large-scale electric aircraft, the impedance of the DC system is extremely low, which would result in a considerably high fault current (tens of kiloamperes) when a fault happens. It is crucial to limit the fault current and isolate the fault within a few milliseconds. To ensure the safety and reliability of the electric aircraft, fault current limitation as well as interruption technologies play a significant role in achieving this target. This paper proposes to integrate a superconducting fault current limiter (SFCL) and a DC circuit breaker (DCCB) in one cryostat to provide fault protection.

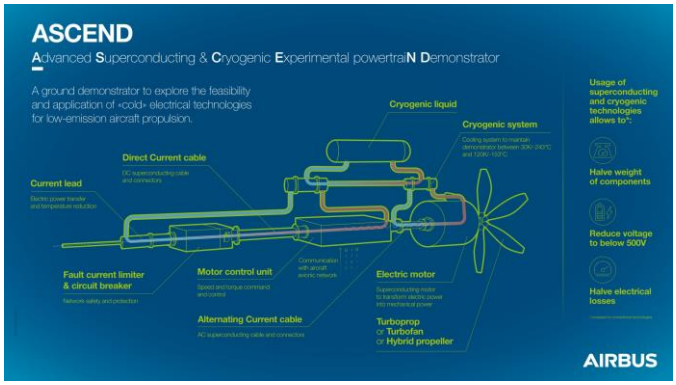

Fig. 1. Airbus ASCEND demonstrator [2].

SFCL and DCCB have been widely studied and developed as protection devices to protect DC networks. Resistive SFCL (R-SFCL) is a promising device to be used in DC systems because of its simple topology, compact structure, light weight and automatic triggering [3]. The performance of R-SFCL in different coolants has been studied, both liquid nitrogen (LN_2) and gaseous helium (GHe) can satisfy thermal requirements [4]. Many R-SFCL structures have been proposed and studied, mainly divided into the straight line type [5], pancake type [6-9] and solenoid type [10-12]. DC circuit breakers can be divided into mechanical circuit breakers, solid-state circuit breakers (SSCBs) [13, 14] and hybrid circuit breakers (HCBs) [15, 16]. SSCBs, using semiconductor devices to interrupt the fault current, have the fastest interruption speed to isolate faults in hundreds of microseconds [14, 17], which are desirable for protecting electric aircraft DC networks. However, the high on-state loss of SSCBs would reduce the system efficiency. The on-state loss of a Si MOSFET-based SSCB would be reduced at cryogenic temperatures as the temperature coefficient of Si MOSFETs on-state resistance is positive [18].

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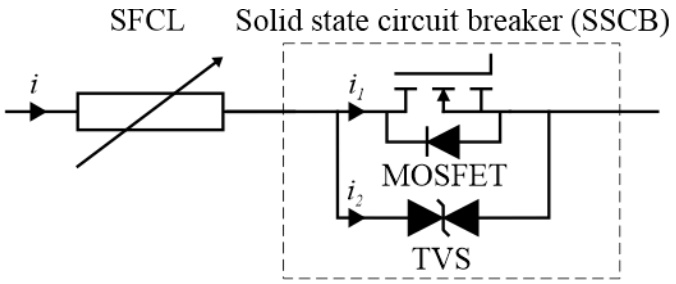

Fig. 2. Proposed topology of SFCL and DCCB

Integration of SFCL and DCCB has been proposed and investigated by several research groups [19-22]. However, none of them studies the current limiting and interruption behaviours when both SFCL and DCCB are at cryogenic temperatures. In this paper, the performance and characteristics of integration of SFCL and SSCB at cryogenic temperatures are studied for the first time. In section II, the operating principle, design of SFCL and cryogenic DC SSCB are introduced. Section III presents the sub-cooled liquid nitrogen cryogenic cooling system as well as DC fault current test platform. In Section IV, a prototype SFCL and DC circuit breaker is experimentally tested in a liquid nitrogen open bath and in a sub-cooled liquid nitrogen cryostat, respectively.

II. Design Of SFCL And Cryogenic DC Circuit Breaker

A. Operating Principle

Fig. 2 presents the proposed topology of SFCL and DCCB. A resistive SFCL is connected in series with a solid-state circuit breaker. The SSCB consists of multiple MOSFETs and transient voltage suppressor (TVS) diodes in parallel. Fig. 3 shows typical current and voltage waveforms. During normal operation, SFCL is in the superconducting state and MOSFET remains on, and the current flows through SFCL and MOSFETs. When a fault occurs at t_1, the current increases rapidly. Once the fault current exceeds the critical current of the SFCL, the SFCL transits from the superconducting state to the normal state and introduces resistance in the circuit to limit the fault current. When a fault current is detected, the SSCB starts to interrupt the current. MOSFETs are turned off at t_2, all the current is commutated from the MOSFET branch (i_1) to the TVS branch (i_2). The voltage across the SSCB is clamped by TVS to a designed level and all the residual energy is dissipated by TVS. After the instant when the current reduces to zero (t_3), the fault current has been successfully interrupted.

B. SFCL Prototype

A pancake SFCL coil prototype is designed and built as shown in Fig. 4. The parameters of the SFCL prototype are listed in Table I. The SFCL coil is wound onto a G10 former using a 12 mm wide YBCO high temperature superconducting (HTS) tape from Shanghai Superconductor Technology Co., Ltd [23]. Two copper terminals are placed at the symmetrical positions of the outermost circle of the coil and fixed onto the G10 former. An HTS tape is soldered to the copper terminals and two voltage taps are soldered at each end of the HTS tape. The resistance of the HTS tape at room temperature (RT) is 100 mΩ/m. The critical currents of the SFCL prototype at 77 K and 65 K are measured to be 533 A and 1023 A, respectively.

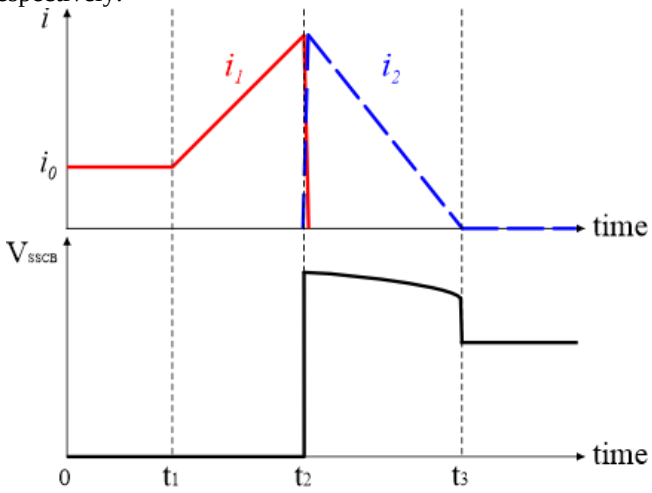

Fig. 3 Typical current and voltage waveforms for SFCL and DCCB

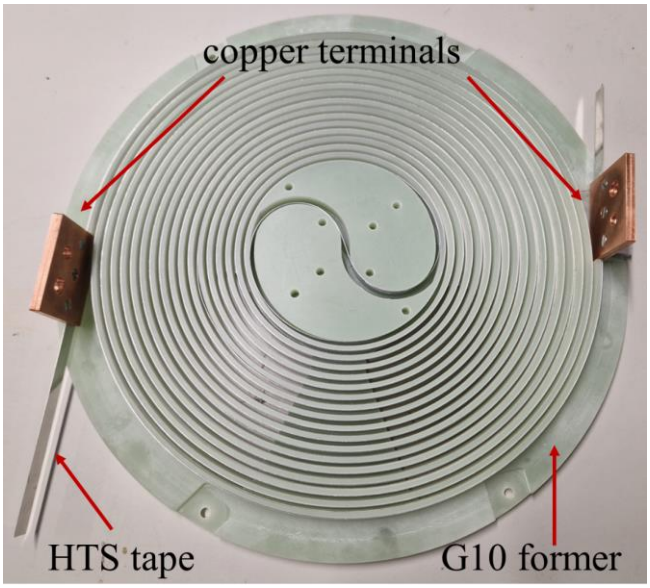

Fig. 4 SFCL pancake coil prototype

TABLE I
SFCL Prototype Parameters

Item	Value
Tape type	ST-12-L
Tape width	12 mm
Lamination	Stainless steel
Resistance @ RT	100 mΩ/m
Critical current @ 77K, self-field	533 A
Critical current @ 65K, self-field	1023 A
Tape length	11.6 m

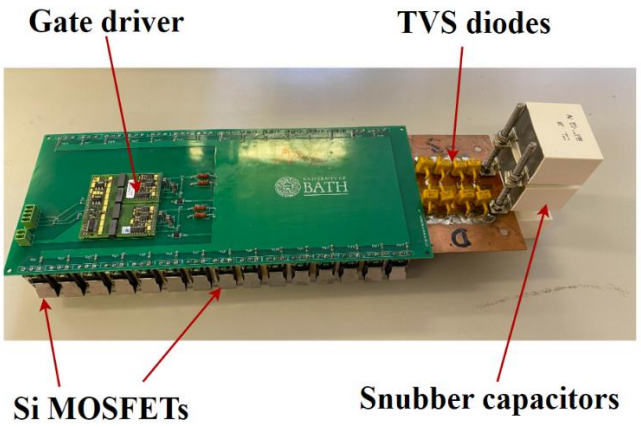

Fig. 5. Photo of the SSCB prototype

C. Cryogenic DC Circuit Breaker Prototype

A solid-state DC circuit breaker using multiple parallel connected power MOSFETs is designed to interrupt the DC fault current. Fig. 5 shows the photo of the SSCB prototype. Thirty Si MOSFETs are mounted on a cold plate and they are parallel connected through two copper busbars. Three snubber capacitors are connected to the MOSFET devices to limit the high voltage rate of rise (dv/dt) during the fault current interruption. Eight TVS diodes configurated with four parallel branches are used to clamp the overvoltage and absorb the residual energy in the system. Each branch contains two TVS diodes in series. The gate driver PCB board is assembled on the top of copper busbars. All components in the SSCB are selected to be suitable for cryogenic temperatures. A microcontroller board is designed to sense the fault current and send a turn-on or turn-off signal to the SSCB.

III. Experimental Setup

A. Cryogenic Cooling System

A cryogenic cooling system, including a sub-cooled liquid nitrogen cryostat, a water chiller, a cryocooler compressor, a vacuum pump and a temperature controller, is designed and built for the integration of the SFCL and the DC circuit breaker. The temperature of the cryostat can be controlled from 65 K to 77 K. A Lakeshore 336 temperature controller is used to monitor and control the temperature of the cryostat.

A two-tier G10 sample holder is manufactured to support the SFCL and the SSCB. The SFCL is placed on the lower tier, which is closer to the bottom of the cryostat bucket and coldhead. The SSCB is put on the upper tier. Six temperature sensors are attached on different positions of the SFCL and the SSCB to monitor the real-time temperatures during cooling down and testing. The entire sample is assembled into the cryostat.

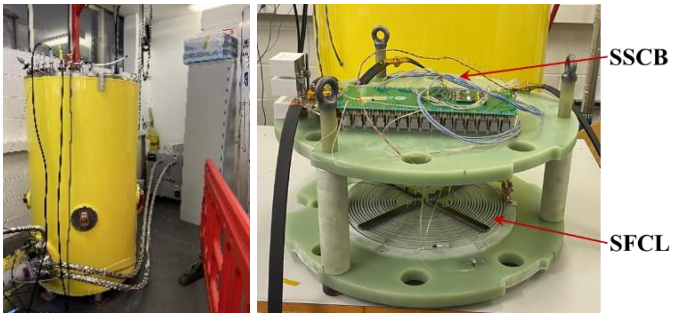

Fig. 6. Cryostat (left) and test sample holder with SFCL and SSCB (right)

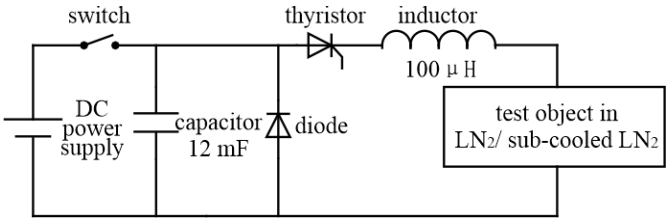

Fig. 7. Schematic circuit of DC fault current test circuit

B. DC Fault Current Test Platform

The schematic circuit of the DC fault current test platform is illustrated in Fig. 7. An LC resonant circuit using a 12 mF capacitor and a 100 μH inductor is utilized to generate DC fault currents. After pre-charging the capacitor to the voltage level from 50 V to 450 V through the DC power supply, a fault current of 0.4 kA to 3.8 kA can be achieved. The test object is connected in series in the test circuit. The fault current flows through the test object after triggering the thyristor. The freewheeling diode is used to bypass the capacitor to prevent reverse charging.

IV. Experimental Tests And Result Analysis

A. Current Limiting Performance Tests

During the tests, only the SFCL prototype was connected into the DC fault current test circuit. The current limiting performances of the SFCL prototype are investigated from 65 K to 77 K under different capacitor voltage levels. Experimental results under 300 V at 77 K are presented in Fig. 8 as an example. The red line with solid triangles shows the prospective values of fault currents without using the SFCL prototype. The red line with hollow triangles represents the fault current limited by the SFCL prototype, the blue line with hollow squares is the voltage drop across the SFCL coil, and the green line with hollow diamonds shows the SFCL impedance. As it can be seen in Fig. 8, the capacitor is pre-charged to 300 V. After triggering the thyristor at 0 ms, the fault current is generated and flows through the SFCL coil. The voltage across the SFCL coil starts to build up after the fault current is almost twice the critical current, reaching a maximum voltage of 202 V during the test. The maximum

quench resistance of the SFCL is 0.15 Ω, which is approximately 13% of the room temperature resistance value.

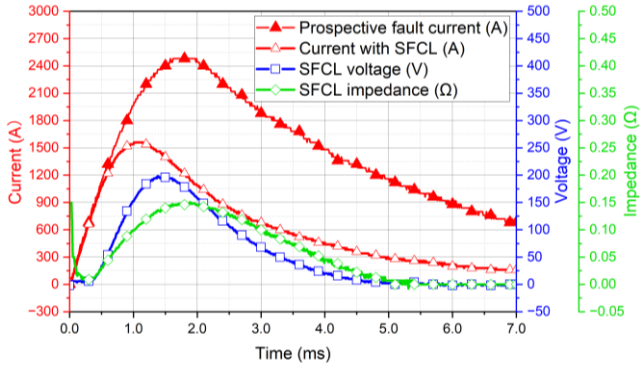

Fig. 8. Current liming performance under 300 V at 77 K

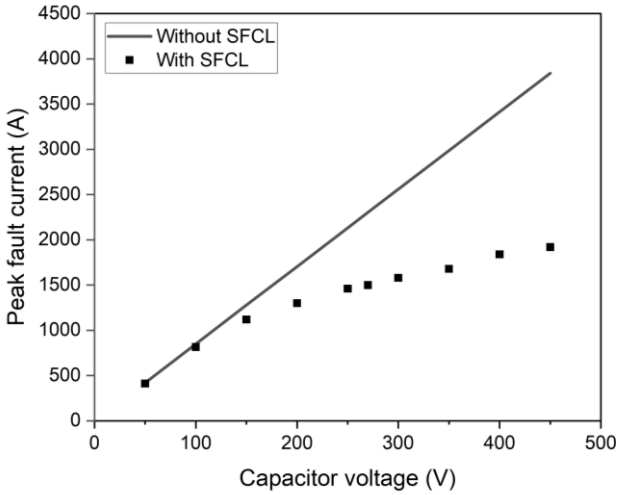

Fig. 9. Peak current values using different capacitor pre-charge voltage levels at 77 K.

Experimental results at 77 K with the capacitor voltage level up to 450 V are illustrated in Fig. 9. The SFCL prototype starts to perform the current limiting effect when the prospective fault current is over 1 kA. When the fault current exceeds twice the critical current of the SFCL coil, there is a significant current reduction as the capacitor voltage level increases. For example, the SFCL coil limits the prospective peak fault current from over 2.5 kA to 1.6 kA when the capacitor is pre-charged to 300 V.

Current liming performances from 65 K to 77 K with the pre-charged capacitor voltage of 300 V are demonstrated in Fig. 10. The critical currents (Ic) at different temperatures are listed in the legends. As the temperature decreases from 77 K to 65 K, the Ic of the SFCL coil is almost doubled. However, the peak fault current level after current limiting increases from 1.6 kA to 2.1 kA.

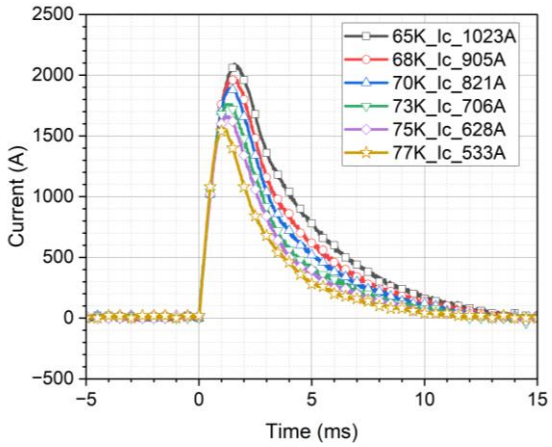

Fig. 10. Current liming performance under 300 V from 65 K to 77 K

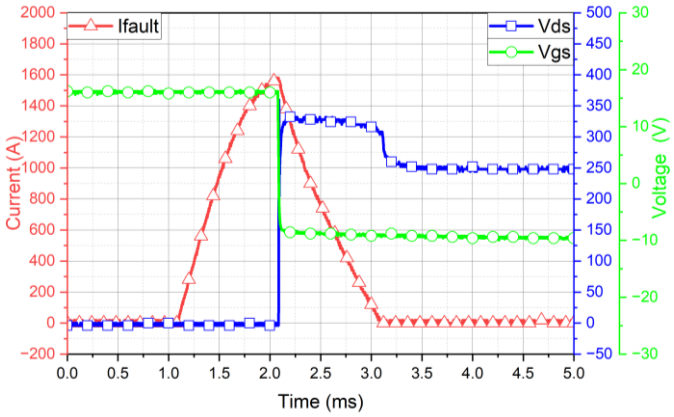

Fig. 11. SFCL and SSCB interruption in LN_2 open bath (77 K)

B. Current Limiting and Interruption Tests

The performance of integration of the SSCB and the SFCL is studied in this section. The SSCB prototype combined with the SFCL coil is connected to the DC fault current test circuit. The capacitor is pre-charged to 300 V and the SSCB is closed before a fault event is triggered by the thyristor.

Fig. 11 shows the current limiting and interruption waveforms when the SSCB prototype with the SFCL coil is submerged in a LN_2 open bath at 77 K. As it can be seen, the SFCL limits the current and then the SSCB prototype successfully interrupts the fault current at 1.58 kA while the voltage is clamped between 310 V and 330 V. In contrast, when the SSCB prototype with the SFCL coil is placed inside the sub-cooled LN_2 cryostat where the temperature is controlled at 73 K, the current limiting and interruption waveforms are displayed in Fig. 12. It demonstrates that the SSCB prototype interrupts the fault current at 1.74 kA while the voltage is clamped between 300 V and 330 V. The clamping voltage at cryogenic temperatures is lower than that at room temperature (380 V) [24], which is due to the reducing breakdown voltage of TVS diodes at lower temperatures.

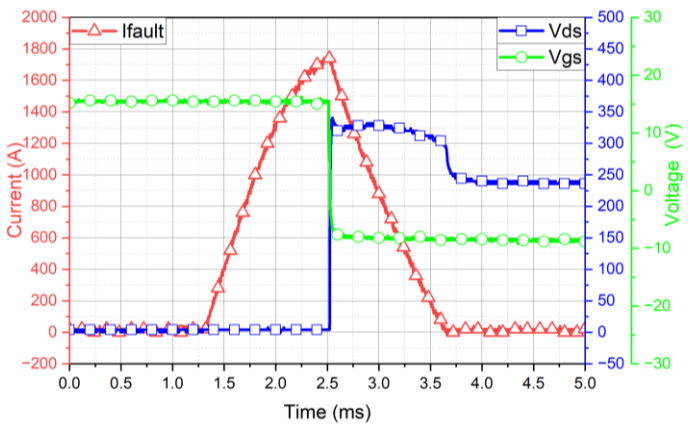

Fig. 12. SFCL and SSCB interruption in sub-cooled LN_2 cryostat (73 K)

V. Conclusion

An SFCL and SSCB prototype has been built and experimentally tested at cryogenic temperatures. A cryogenic cooling system is built to cool the prototype to the cryogenic temperatures of 65 K to 77 K.

The current limiting performances of the SFCL prototype are studied from 65 K to 77 K with the capacitor voltage level up to 450 V. As the temperature decreases, the critical current of the SFCL coil increases, which means the SFCL coil can carry more current during normal operation. The SFCL coil starts to perform a significant current limiting effect after the fault current exceeds twice the critical current. In addition, as the prospective fault current peak value increases, the current limiting effect becomes more significant. When limiting the same expected fault current, a SFCL coil with a lower critical current (at a higher temperature) can limit the fault current to a lower value. However, its current carrying capability during normal operation is reduced. In practical applications, an appropriate operating temperature should be selected for the design to obtain sufficient current carrying capacity and current limiting effect.

The interruption performances of the SFCL and SSCB prototype are investigated at 77 K and 73 K with the pre-charged capacitor voltage of 300 V. The prototype successfully demonstrates the ability to operate and interrupt currents at cryogenic environment. This paper shows the great potential and feasibility of using integrated SFCL and DC circuit breaker in cryogenic electric aircraft.

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