Enhanced Controller for grid-connected Modular Multilevel Converters in distorted Utility Grids

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Abstract: This paper is about the control of Modular multilevel converters, an innovative technology in the design of converters, which is beginning to be included in real installations. Papers about this topic include simulation models, circulating current reduction, voltage modulators, capacitor voltage balancing and control issues. The scheme for current source regulation used in this article includes all control loops, which are, from the outermost to innermost, DC bus voltage regulator, current regulator, voltage modulator, capacitor voltage balancing, and a PLL for the synchronization to the grid. Disposition-sinusoidal Pulse Width Modulation is used as the voltage modulator, and an enhanced control strategy in the stationary reference frame for 3-phase MMCs is used for the inner current control loops. Very detailed simulations of the complete control system have been performed for both the enhanced control strategy in the stationary reference frame, and the well-known control in the synchronous reference frame, as well as some experiments using the Hardware-in-the-Loop Simulation technique. The validation of these control strategies is made by a comparison of the capability of each one to compensate the harmonic distortions of the utility grid according to the grid code. The correct operation has been tested in the case of a strong/weak grid, unbalances and grid failures.

Keywords: Electric power transmission; modular multilevel converter (MMC); voltage-source converter (VSC); proportional-resonant (PR) controller; harmonic compensator (HC)

1. Introduction

The types of converters used for medium (MV) and high voltage (HV) AC/DC/AC conversion are line commutated converters (LCC) [1], voltage source converters (VSC) [2,3], and lately MMC, first used by Marquardt [4]. LCC and VSC are the classical topologies used for converters, but VSC multilevel topologies have also been used [5]. The LCC topology is built with thyristors, while the VSC topology can use IGBTs, IGCTs or GTOs featuring two, three or more than three levels.

Modular Multilevel Converters (MMC) is a new topology that has acquired great interest for researchers [6] and which has begun to be implemented in actual installations. The base is a switching

module (SM) composed by two bidirectional switches (IGBT + antiparallel diode) and a capacitor C (see Figure 1). The converter is built using several SMs and an inductance per arm, two arms per phase, and containing three phases (see Figure 1). The arm inductances L are used to couple the arm voltage to the DC bus voltage.

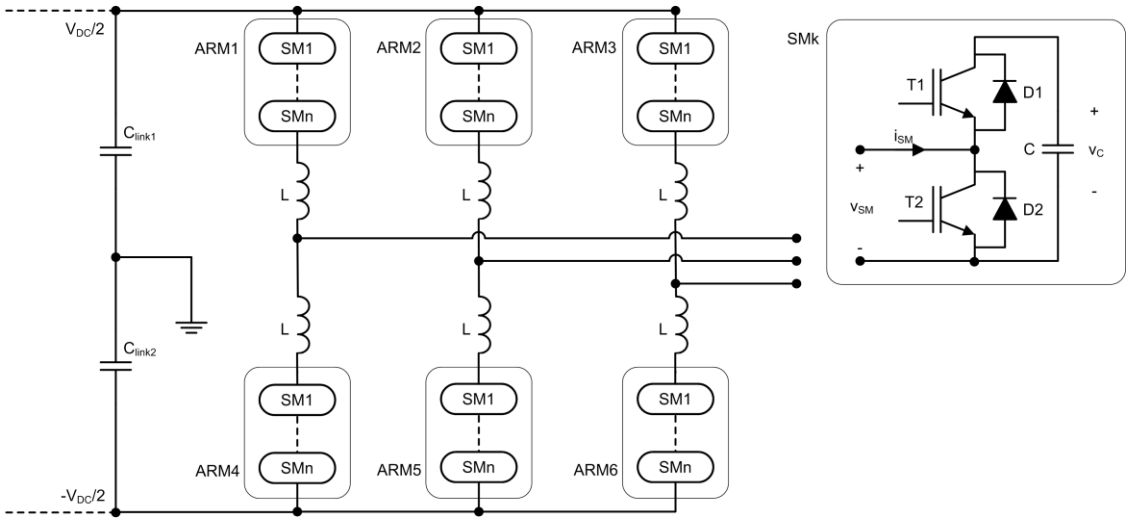


Figure 1. MMC scheme and SM structure.

An MMC converter with n SMs per arm can generate a phase to midpoint of the DC voltage with $n + 1$ levels. The number of AC output levels can be increased by increasing the number of SMs.

MMC has advantages and disadvantages regarding LCC and VSC [7]. The advantages include a reduction in the need for AC filtering, easy scalability, the distribution of the capacitive energy between several capacitors, and stress reduction in the semiconductor. The main disadvantage is the increased complexity: the number of modules and drivers, the number of signals to be handled, including module trigger and SM voltage feedback. Another disadvantage is the presence of the circulating three currents (one per phase) that circulate between each phase and the DC bus.

Studies about MMC tackle the analysis of semiconductor losses in comparison with other topologies, static and dynamic modeling, and control in balanced and unbalanced grids [8]. The SM capacitor voltage changes when current flows through it, and several techniques can be used to keep those capacitor voltages balanced: sorting algorithms [7,8], averaged and balanced control [9], predictive control [10], methods which do not require the sign of the arm current to be known [11] and methods to decrease the switching frequency [12].

Moreover, if the semiconductor models are very accurate, the simulation of the MMC can be extremely slow because of the very high number of semiconductors. Therefore, less accurate models are studied to obtain simulation with a sufficient degree of accuracy through averaged and approximated models [13-16].

For the AC voltage modulator, several possibilities are described, such as PD-SPWM, multilevel PWM and current source predictive control. PD-SPWM is a type of PWM where the reference is compared with n carriers to obtain the gate signals of the SMs [8,17]. Multilevel PWM calculates the average value of the voltage over a commutation period and generates the duty cycle necessary to obtain it [7]. Predictive control evaluates a cost function that includes several parameters and selects the best combination of ON/OFF states of the SMs [10].

The upper and lower arms of a phase leg have current simultaneously; the consequence is the existence of undesired currents, the circulating currents. Their equations are calculated in [18], their suppression in [17], and their reduction in unbalanced systems in [19].

Other aspects of MMC studied are: models and control systems in unbalanced grids [20,21], influence of the commutation frequency and the number of SMs in the harmonic content [22], DC bus protection using thyristors included in the SMs [23] and current source control [24].

Regarding the 3-phase grid-connected renewable systems, several vector control strategies are studied in the scientific literature. Hysteresis control [25], dead-beat predictive control [26,27], and dq control [28,29], among others, have been widely used for several years with acceptable results. The linear dq control approach is the cheapest strategy and uses the well-known PI regulators in synchronous reference frame, which allow a zero steady-state error when dc variables are used, as well as an easy digital implementation in commercial microcontrollers; its main drawbacks are a lower dynamic response and a non-zero steady-state error when sinusoidal variables are used. On the contrary, the dead-beat predictive control has a higher dynamic response, but it is necessary to measure or estimate some variables, which increases the cost of the system, and is very sensitive to model mismatches and parameters uncertainties. The hysteresis control is a non-linear strategy, having the fastest dynamic response, and being very easy to implement with analog devices, although enhanced more expensive signal conditioner circuits are needed due to the higher bandwidth of the measured line currents, which increases its overall cost; in addition, this strategy is almost insensitive to parameters uncertainties, and very robust to input and output disturbances, but a variable hysteresis band is mandatory [25] because its switching frequency is not constant, making the digital implementation very difficult.

The dq control strategy implemented in the synchronous reference frame [30] has been the preferable strategy for years and for this, the Park´s transformation [31,32] is applied to the 3-phase line currents. However, a trade-off between the advantages and disadvantages can be noticed: although its digital implementation is very easy, its main drawbacks deal when it is used in 3-phase distorted grid-connected systems, where the low-order harmonic distortions of the grid voltages must be compensated because they will appear in the line currents instead, reducing the power quality and the power factor of the connection. The feedforward of the dq components of the grid voltages and the cross-coupling terms can solve the situation, but a high bandwidth is mandatory in the open loop transfer function of the line currents in order to decrease the effect of delays [33,34], which firstly, increases the switching frequency and, in consequence the losses, and last but not least, a programmable device such as an FPGA must be used.

The reduction of the power quality and the power factor can make impossible the connection of the renewable system to the utility grid if the magnitude of the individual harmonic distortions and/or the total harmonic distortion of the line currents are higher than the limits imposed by the grid code [35,36]. For the fundamental frequency ω_1 of the 3-phase utility grid voltages with positive-sequence, the implementation of a harmonic compensation scheme in the synchronous reference frame can be done as in [37], but the interpretation of the Park´s transformation applied to the 5^{th}, 7^{th}, 11^{th}, 13^{th}, … harmonics must take into account the negative- sequence for the 5^{th} and the 11^{th}, as well as the positive- sequence of the 7^{th} and 13^{th} harmonics, and its transformation into the 6^{th} and 12^{th} harmonics, respectively, in the fundamental synchronous reference frame [33]. So, a conventional PI regulator can be employed for the fundamental frequency ω_1 because the d-q components of the line currents are constants and a zero steady-state error is ensured. However, the perturbation of the 6^{th}, the 12^{th}, … harmonics will not be cancel unless several synchronous reference frames rotating at $\pm 6n\omega_1$ (n=1,2,3,4,….) were applied. If so, the several constant d-q components of each synchronous reference frame will allow the use of integrators to reject the harmonic pollution of the 3-phase utility grid voltages by cascading its outputs to the output of the PI regulator of the fundamental synchronous reference frame. It is worth noting that special care must be taken with delays for high order harmonics.

Nowadays, an enhanced control strategy is being used to deal with distorted utility grids. Unlike the control described above, it is also possible to do it in the stationary reference frame [38] avoiding the use of several synchronous reference frames and reducing the computational burden. For this, the Clarke´s transformation is used [32,39], allowing its implementation with Proportional and Resonant (PR) regulators for the fundamental frequency, as well as several resonant controllers to compensate the low-order harmonics introduce by the utility grid voltages. In addition, PR regulators can deal with positive- or negative-sequence systems, as it will be explained in the next sections. Finally, the implementation of this strategy does not need a very high bandwidth of the open loop

transfer function of the line currents, and so, the switching frequency can be set at 10-20 KHz, allowing the use of commercial microcontrollers.

In this paper, a comparison of the behavior of the dq control strategy with the PR regulators plus the Harmonic Compensation (HC) structure has been made, mainly in their capability for the reduction of the harmonic distortions in the 3-phase utility grid currents. It is organized as follows: firstly, the basic structure and the main equations of the MMC are presented in Section 2, and an explanation of the fundamentals of the PR plus the HC structure, compared with the well-known dq control strategy with PI regulators, is presented in Section 3; in Section 4, the elements of the vector control for the 3-phase line currents (as the inner control loops) in the stationary reference frame, as well as the power balance exerted in the outer DC bus voltage control loop are analyzed, and the PLL, the sorting algorithm for the capacitor voltages, and the voltage modulator are also presented; in Section 5 the grid code used in this paper is presented. Secondly, some simulations and experiments are carried out in Sections 6 and 7, respectively, to validate the capability of each control strategy for the attenuation of the harmonic distortions of the 3-phase utility grid currents and the Fault-Ride-Through (FRT) operation. Finally, the conclusions are stated in Section 8.

2. Fundamentals of MMC

SMs are composed of two IGBTs, two diodes and a capacitor (Figure 1). The SM ON/OFF state and the SM current i_{SM} sign set the following parameters: the sign of the capacitor voltage increases Δv_C, the semiconductor through which current i_{SM} flows and the SM voltage v_{SM} (Table 1).

Table 1. Relations among elements and variables of the SM.

SM state	T_1 state	T_2 state	i_{SM}	Δv_C	i_{SM} flows through	v_{SM}
ON	ON	OFF	> 0	$+$	D_1	v_C
ON	ON	OFF	< 0	$-$	T_1	v_C
OFF	OFF	ON	> 0	0	T_2	0
OFF	OFF	ON	< 0	0	D_2	0

The sum of the number of SMs in the ON state in the upper n_{up} and lower n_{low} arms of each phase is equal to the number of SMs per arm n.

$$n_{up} + n_{low} = n \tag{1}$$

Regarding Figure 2, the grid-connected MMC can be fed by photovoltaic panels or wind turbines + AC/DC converter, where the input power will be proportional to the irradiance at a specific temperature or to the cube of the wind speed, respectively, whereas a large link capacitor C_{link} is used to transform this current into a voltage source at the input of the MMC converter. Therefore, at steady state regime each SM will have an average voltage $v_{SM} = \frac{V_{DC}}{n}$.

The first phase MMC voltage v_{oa} (Figure 2), is:

$$v_{oa} = \frac{V_{DC}}{2} - v_{upa} - L\frac{di_{upa}}{dt} \tag{2}$$

$$v_{oa} = -\frac{V_{DC}}{2} + v_{lowa} + L\frac{di_{lowa}}{dt} \tag{3}$$

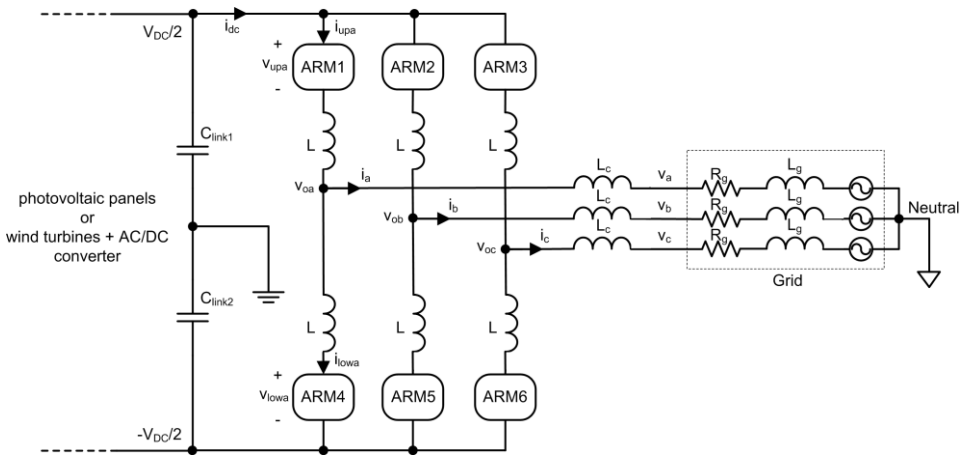


Figure 2. Scheme of the MMC connected to the grid.

If S_{upak} and S_{lowak} are the estate 1/0 of the first phase SMs, and v_{cupak} and v_{clowak} are the first phase capacitor voltages, then the upper and lower arm voltages are:

$$v_{upa} = \sum_{k=1}^{n} S_{upak}\, v_{Cupak} \tag{4}$$

$$v_{lowa} = \sum_{k=1}^{n} S_{lowak}\, v_{Clowak} \tag{5}$$

If i_{za} is the first phase circulating current, then the first phase arm currents are [8,14]:

$$i_{upa} = \frac{i_a}{2} + \frac{i_{dc}}{3} + i_{za} \tag{6}$$

$$i_{lowa} = -\frac{i_a}{2} + \frac{i_{dc}}{3} + i_{za} \tag{7}$$

Adding (6) and (7), the expression of the circulating current can be obtained:

$$i_{za} = \frac{i_{upa} + i_{lowa}}{2} - \frac{i_{dc}}{3} \tag{8}$$

The sum of the circulating current of the three phases is zero:

$$i_{za} + i_{zb} + i_{zc} = 0 \tag{9}$$

3. Fundamentals of the PR regulator plus the HC

The PR regulators, unlike the PI regulators, can be used in 1- or 3-phase systems because the former can track sinusoidal signals, meanwhile the latter is used for dc variables. For 3-phase signals, the Clarke´s transformation converts a 3-phase sinusoidal system (abc) into a 2-phase sinusoidal system in orthonormal ($\alpha\beta$) axes, also known as abc->$\alpha\beta$ transformation in the stationary reference frame; the inverse Clarke´s transformation ($\alpha\beta$->abc transformation) is also possible without losing information if the 3-phase variables have two degrees of freedom. For 1-phase systems, the ac sinusoidal signal is used as itself and no transformation is applied.

On the contrary, the PI regulator can only be used in 3-phase systems because the Park´s transformation converts the 3-phase sinusoidal variables into a 2-phase dc variables in orthonormal dq axes, also known as abc->dq transformation in the rotating synchronous reference frame. Again, the inverse operation (dq->abc transformation) is also possible without losing information if the 3-phase variables have two degrees of freedom.

In order to understand the advantages of the PR regulator plus the HC over the PI regulators, Figures 3 and 4 are depicted bellow. First, it must be said that the internal model principle (see Appendix C of [39] for a detailed explanation) states that the output of a closed control loop will track the input reference command and will reject the disturbance (zero steady-state error) if the denominators of any block of the open loop transfer function and the Laplace transform of both the input reference command and the disturbance are the same. Then, as the plant cannot be changed, it is clear that the denominator of the transfer function of the regulator must obey this principle.

When a PI regulator is employed, it can only track and reject dc variables, whose Laplace transform is 1/s, because the denominator of the transfer function of this regulator is s (see Figure 3). For example, in the case of 3-phase systems with a positive- sequence of the fundamental frequency of the 3-phase utility grid voltages, the PI regulator can only track and reject the dc variables of the Park´s transformation in d-q axes, corresponding to the fundamental frequency; conversely, the 5th negative- and 7th positive- sequence harmonics which are transformed into the 6th harmonic, and the 11th negative- and 13th positive-sequence harmonics which are transformed into the 12th harmonic [33,40], both in the same d-q axes, cannot be rejected by the PI regulator.

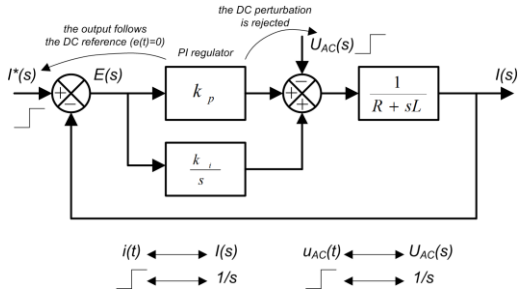


Figure 3. Block diagram of the line current closed loop using a PI regulator.

On the contrary, when a PR regulator is employed, it can only track and reject sinusoidal variables, whose Laplace transform are $\frac{\omega_o}{s^2+\omega_o{}^2}$ because the denominator of the transfer function of this regulator is $s^2+\omega^2_o$ (see Figure 4). In the case of 3-phase systems, the PR regulator can track and reject the sinusoidal variables of the Clarke´s transformation in α-β axes corresponding to the fundamental frequency, but what is more important, cascading several resonant filters tunned to the 5th, 7th, 11th, 13th, etc., the Harmonic Compensator (HC) structure is easily formed and these harmonics are rejected in the output α-β components of the 3-phase grid currents. In addition, it is worth noting that the PR regulator plus the HC can deal with positive- or negative-sequence systems because they always have a pair of conjugate poles in the complex plane for the fundamental frequency and its harmonics.

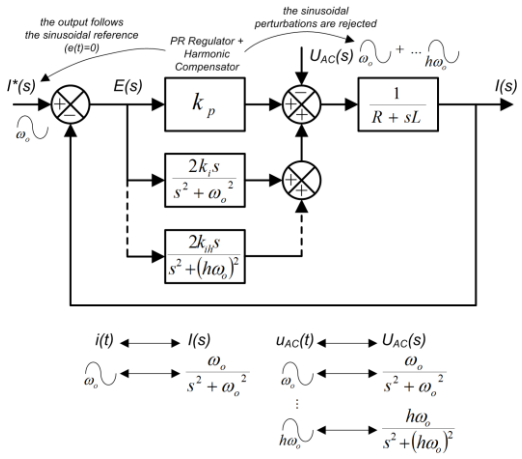


Figure 4. Block diagram of the line current closed loop with a PR regulator plus a HC structure.

4. Vector control

4.1. Current control loops

The vector equation that relates the converter voltage $\vec{v}_o$, the grid voltage $\vec{v}$, and the converter output current $\vec{\imath}$ is (Figure 2):

$$\vec{v} = \vec{v}_o - L_c \frac{d\vec{\imath}}{dt} \tag{10}$$

where L_c is the coupling inductance, and can be expressed by the following two equations in the $\alpha - \beta$ orthonormal axes [38]:

$$v_\alpha = v_{o\alpha} - L_c \frac{di_\alpha}{dt} \tag{11}$$

$$v_\beta = v_{o\beta} - L_c \frac{di_\beta}{dt} \tag{12}$$

Two identical Proportional-Resonant (PR) regulators are employed to control the $\alpha - \beta$ components of the 3-phase output currents, forming the inner loops of a cascade control structure together with the outer DC bus voltage regulator; they can be obtained from (11) and (12). As can be seen, unlike the PI regulators used for the vector control of the orthonormal $d - q$ components of the 3-phase output currents, these equations are not coupled and an easier implementation is achieved. In addition, a cascaded Harmonic Compensator (HC) structure can be added to both PR regulators, allowing the rejection of the harmonic pollution in the utility grid voltages (Figure 5) according to the internal model principle. The output of the PR regulators plus the harmonic compensators are the reference voltages of the converter $v_{o\alpha}{}^*$ and $v_{o\beta}{}^*$, being worth noting the absence of the feedforward utility grid voltages, commonly used in the dq control in the rotating synchronous reference frame.

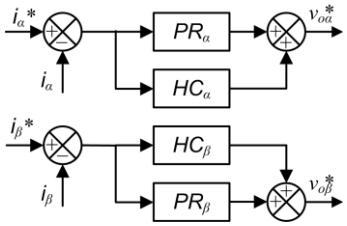


Figure 5. Proportional-Resonant (PR) regulators + Harmonic Compensators (HC) in $\alpha - \beta$ axes.

Definetly, the PR+HC structure are formed by a proportional regulator and a series of resonant filters tunned to the fundamental, the 5th, 7th, 11th,13th, …low order harmonics. Each resonant filter behaves as a Generalized Integrator [41] with a very high gain at its resonance frequency and a narrow bandwidth. Then, the proportional and the resonant filter tunned at the fundamental frequency can regulate sinusoidal reference signals: the proportional gain K_P sets the dynamic of the system (bandwidth, phase and gain margin), and the integral gain K_I guarantees a zero steady-state error, meanwhile the other resonant filters compensates (or reject) the harmonic distortion in the output currents due to the harmonic pollution of the 3-phase utility grid voltages.

The structure of the PR+HC shown in this paper is non-ideal, and a cut-off frequency ω_c is added to improve the stability problems and make the digital implementation easier [42]. The transfer functions of the PR and the HC are shown in (13) and (14) for the fundamental, 5th, 7th, 11,th, 13th harmonics, and the block diagram is depicted in Figure 6. An extension to other low order harmonics can be made by extrapolation, but special care must be taken with delays, mainly for high order harmonics distortion [34].

$$G_{PR}(s) = K_P + \frac{2K_I\omega_c s}{s^2 + 2\omega_c s + {\omega_o}^2} \tag{13}$$

$$G_h(s) = \sum_{h=5,7,11,13} \frac{2K_{Ih}\omega_c s}{s^2 + 2\omega_c s + (h\omega_o)^2} \tag{14}$$

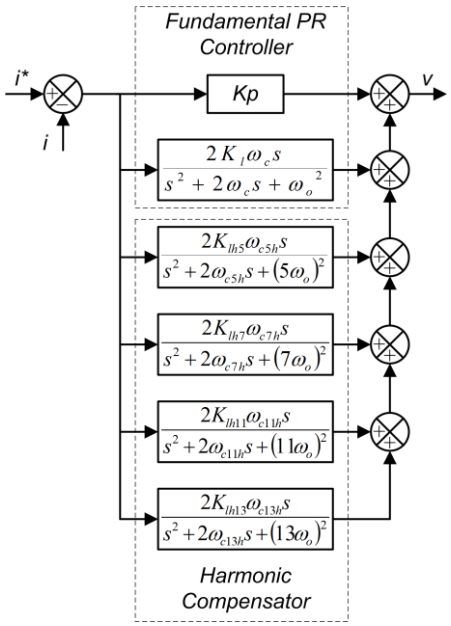


Figure 6. Detailed implementation of the PR Regulator + Harmonic Compensators (HC) structure for the fundamental, 5th, 7th, 11th, 13th harmonics.

4.2. DC bus voltage control loop

The DC bus voltage V_{DC} is regulated with the outer control loop of the converter [43], allowing the power balance between the incoming active power and the power delivered to the utility grid (Figure 7). The reference for the DC bus voltage V_{DC}^* is compared with the measured value of the DC voltage V_{DC}, and the error is fed to a PI regulator, which output is the d component of the reference line current i_d^* and is proportional to the maximum available power at the input; the q component of the reference line current i_q^* is set as an open loop signal and is capable to control the power factor of the MMC converter-grid connection. The inverse Clarke´s transformation is then applied to both components i_d^* and i_q^*, allowing the vector current control in the orthonormal $\alpha - \beta$ axes, explained above.

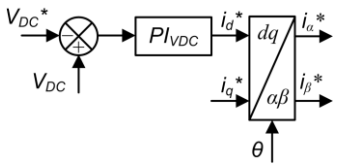


Figure 7. DC bus voltage control loop.

The instantaneous active and reactive powers can be calculated using the orthonormal $\alpha - \beta$ components of the 3-phase line currents and the utility grid voltages according to the instantaneous reactive power theory [44]:

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{15}$$

$$q = v_\beta i_\alpha - v_\alpha i_\beta \tag{16}$$

or with the orthonormal $d - q$ components [30,45]:

$$p = v_d i_d \tag{17}$$

$$q = -v_d i_q \tag{18}$$

when the utility grid voltage $\vec{v}$ is aligned with the d axis ($v_q = 0$), rotating at the fundamental angular frequency ω of the grid. The former is known as the stationary reference frame control, and the latter is known as rotating synchronous reference frame control, where p and q can be independently controlled by the currents i_d and i_q, respectively (Figure 8).

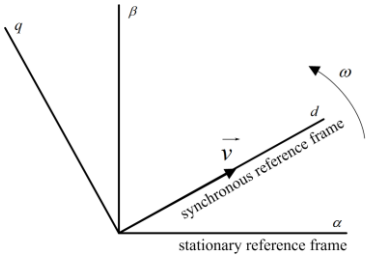


Figure 8. Stationary $\alpha - \beta$ and synchronous $d - q$ reference frames.

4.3. Phase-Locked Loop

For synchronization between the MMC converter and the grid, the angle θ of the grid voltage vector $\vec{v}$ must be known. A scheme for the synchronization PLL is found in Figure 9 [46]. It has a PI block whose input is the quadrature component of the grid voltage v_q. This block generates an output that tries to reduce the value of v_q to zero. The output of the PI block ω is the angular speed of the grid voltage $\vec{v}$; an initial value of the angular speed ω_{offset} is added to reduce the time to track the angle θ and improve the PLL stability. An integrator block is used to get the angle θ from the angular speed ω. For unbalanced systems, a Positive Sequence Detector (PSD) must be added to reject the negative sequence of the 3-phase utility grid voltages [40,47], but it must be pointed out that despite the presence of balanced 3-phase utility grid voltages, special care must be taken with the several errors produced at the output of the data acquisition electronic card, which can also introduce unbalances [48].

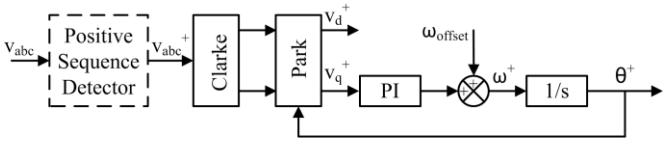


Figure 9. Block diagram of the PLL.

4.4. Sorting the capacitor voltages

There is a last block between the voltage source modulator and the hardware, which must ensure that the capacitor voltages of every SM throughout each arm remain balanced. To achieve this, the SMs of each arm must be selected to be switched ON or OFF to balance their voltages, depending on the sign of the arm current. The objective is to increase the lowest voltages and to reduce the highest voltages.

For example, if the number of modules per arm n is 5, the converter output voltage v_{oa} can take six values, listed in Table 2. Each phase has 10 SMs (2n), 5 SMs in the upper arm and 5 SMs in the lower arm. The voltage of each SM is approximately $\frac{V_{DC}}{5}$, so the number of SMs of each phase in the ON state is 5 in every switching time. For every value of the converter output voltage v_{oa}, the sum of the number of SMs in the ON state in the upper n_{up} and lower n_{low} arms is n (see Table 2).

Table 2. Levels of output voltage v_{oa}.

n_{up}	n_{low}	v_{oa}
5	0	$-\frac{V_{DC}}{2}+0\frac{V_{DC}}{5}$
4	1	$-\frac{V_{DC}}{2}+1\frac{V_{DC}}{5}$
3	2	$-\frac{V_{DC}}{2}+2\frac{V_{DC}}{5}$
2	3	$-\frac{V_{DC}}{2}+3\frac{V_{DC}}{5}$
1	4	$-\frac{V_{DC}}{2}+4\frac{V_{DC}}{5}$
0	5	$-\frac{V_{DC}}{2}+5\frac{V_{DC}}{5}$

To obtain a value of, for example, $v_{oa} = -\frac{V_{DC}}{2} + 2\frac{V_{DC}}{5}$, the number of SMs that must be switched ON in the upper n_{up} and lower n_{low} arms are, respectively, 3 and 2. The SMs to be switched ON must be selected to maintain the SM capacitor voltages balanced. When a SM is ON, its voltage increases or decreases depending on the positive or negative sign of the arm current (Table 1). If the SM is OFF, its voltage remains constant.

A sorting algorithm must be used to select the modules to be switched ON in an arm. The input to the algorithm is the number of SMs in the ON state, n_{up} for the upper arm and n_{low} for the lower arm. The algorithm's output are the SMs selected to be switched ON. When the arm current is positive, the SMs with the lowest voltages are selected, in order to increase their voltage by means of the arm current. When the arm current is negative, the SMs with the highest voltages are selected so as to reduce their voltage. The objective of the algorithm is to keep all the SM voltages around the value of $\frac{V_{DC}}{5}$. In Figure 10, an example of the sorting can be found for the cases of arm current i_{upa} positive and negative, and $V_{DC} = 5000V$.

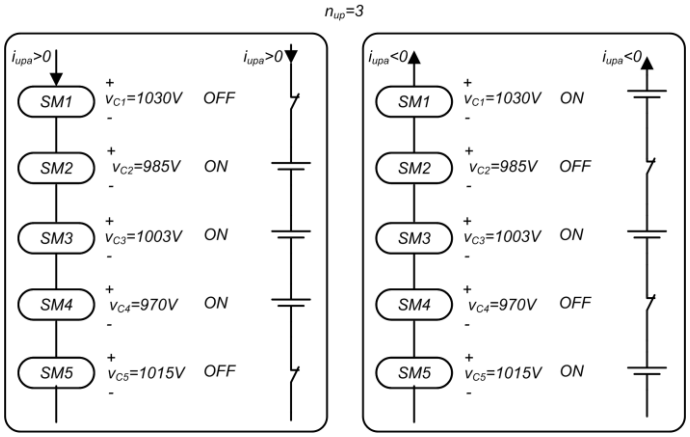


Figure 10. Example of SM voltage sorting for $n_{up} = 3$.

4.5. Voltage modulator

The current regulators set the references of the converter output voltages $v_{o\alpha}{}^*$ and $v_{o\beta}{}^*$ (Figure 5). Therefore, the voltage modulator is an inner loop to the current regulators.

Sinusoidal PWM (SPWM) has been used to control the output voltage of various types of multilevel converters, not only MMC. SPWM is based on a comparison of the modulating signal (supposedly sine wave) with some triangular carriers whose number depends on the number of voltage levels. According to the phase shift of the triangular signals, there are several types of SPWM [49]: Alternative Phase Opposition Disposition, Phase Disposition, Phase Opposition Disposition, Hybrid, Phase Shifted. Among them, Phase Disposition (PD) is a good choice in order to obtain low levels of harmonics. For PD, the phase difference among the triangular carriers is zero.

In this paper, the Phase Disposition-sinusoidal PWM (PD-SPWM) voltage modulator is used, and it is presented for the case of 5 SMs (n = 5) per arm, although a generalization for more or less SMs is straightforward; then, the converter output voltage of each phase v_{oabc} has six levels (n + 1). The relationship between this voltage and the number of ON modules in the lower arm n_{low} is:

$$v_o = -\frac{V_{DC}}{2} + n_{low} v_C \tag{19}$$

For the case of the six-level converter (Figure 11), the PD-SPWM [8] is based on the comparison of five high frequency triangular carriers and a low frequency sinusoidal modulating waveform. The converter output voltage can take the following values: $-\frac{V_{DC}}{2}, -\frac{V_{DC}}{2} + \frac{V_{DC}}{5}, -\frac{V_{DC}}{2} + \frac{2V_{DC}}{5}, -\frac{V_{DC}}{2} + \frac{3V_{DC}}{5}, -\frac{V_{DC}}{2} + \frac{4V_{DC}}{5}, \frac{V_{DC}}{2}$. Depending on the values of the output voltage reference $v_{oa}{}^*$ and the

triangular carriers, the converter output voltage v_{oa} is obtained by means of these equations (for the phase a):

$$v_{oa} = \begin{cases} \frac{V_{DC}}{2}, & (v_{tri5} < v_{oa}{}^{*}) \\ -\frac{V_{DC}}{2} + \frac{4V_{DC}}{5}, & (v_{tri4} < v_{oa}{}^{*} < v_{tri5}) \\ -\frac{V_{DC}}{2} + \frac{3V_{DC}}{5}, & (v_{tri3} < v_{oa}{}^{*} < v_{tri4}) \\ -\frac{V_{DC}}{2} + \frac{2V_{DC}}{5}, & (v_{tri2} < v_{oa}{}^{*} < v_{tri3}) \\ -\frac{V_{DC}}{2} + \frac{V_{DC}}{5}, & (v_{tri1} < v_{oa}{}^{*} < v_{tri2}) \\ -\frac{V_{DC}}{2}, & (v_{oa}{}^{*} < v_{tri1}) \end{cases} \quad (20)$$

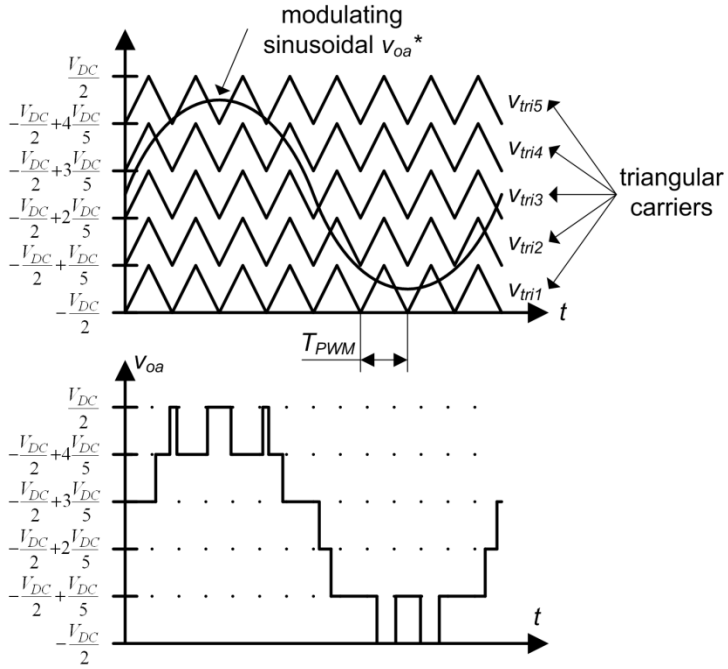


Figure 11. PD-SPWM control.

5. Grid code

On one hand, the limits of the harmonic distortion for the 3-phase utility grid medium voltages (MV) are established according to the IEC/TR 61000-3-6 Normative [35], where the allowed Total Harmonic Distortion (THD) is 6.5%, and the limits for each harmonic order is shown in Table 3.

Table 3. Regulation of harmonic voltage limits in MV power systems.

Odd harmonics non-multiple of 3	Harmonic voltage, MV (%)
5	5
7	4
11	3
13	2.5

On the other hand, the limits of the harmonic distortion for the 3-phase grid currents are established according to the IEEE Std. 519-1992 Normative [36]. The THD limit is established in 5%, meanwhile the limits for each harmonic order are lower, as it is indicated in Table 4.

Table 4. Regulation of harmonic current injection to the grid.

Odd harmonics	Maximum value (%)
3 – 9	4
11 – 15	2
17 – 21	1.5
23 – 33	0.6

In order to validate the outstanding features of the PR plus the HC control strategy compared with the conventional dq control one, some simulations and experiments are carried out for both, mainly doing an analysis of the capability of each one in the compensation of the low-order harmonics of the 3-phase utility grid voltages.

6. Simulations

The control scheme was explained in the previous sections divided into the main parts and the whole system is depicted in Figure 12. In this case, minor changes in the control system are made to allow the FRT operation. The reference line currents i_d^* and i_q^* are calculated applying (17) and (18) to the outputs Ref_P and Ref_Q, respectively. The former follows the available maximum power point (MPP) in normal operation, meanwhile the latter is set to q^* (zero for unity power factor operation). Unlike, when a fault is detected in the 3-phase utility grid voltages, the input Signal Fault is activated and the outputs Ref_P and Ref_Q will follow the non-MPP and q_{fault}, respectively. The simulation of the entire MMC control scheme is performed in MATLAB/SIMULINK, using the complete models of each SM and replacing the IGBT by ideal switches.

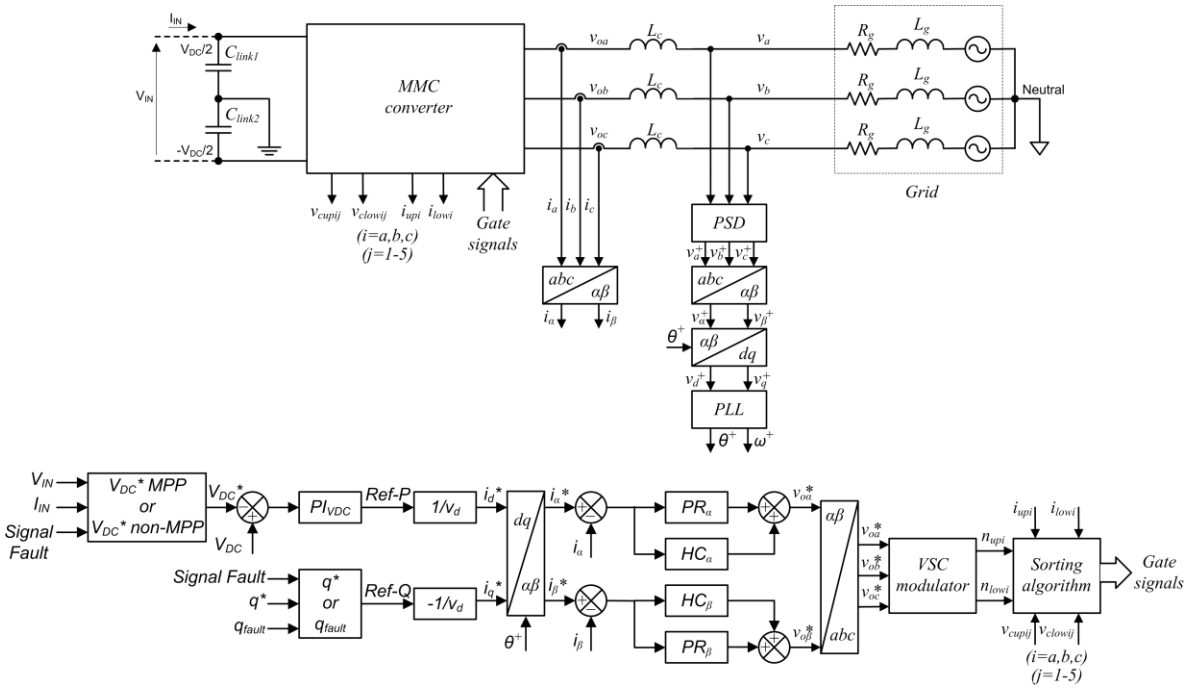


Figure 12. Complete control scheme.

The 3-phase grid voltages v_{abc} and the phase currents i_{abc} are measured and a PSD [47] is applied to the former. Then, v^+_{abc} and i_{abc} are transformed to the stationary reference frame $v^+_{\alpha\beta}$ (abc->αβ transformation), and $v^+_{\alpha\beta}$ is transformed to the rotating grid voltage reference frame v^+_{dq} (αβ → dq transformation). The positive sequence of the components of the grid voltages v^+_d and v^+_q are used by the PLL to obtain the phase angle θ^+ and the speed ω^+ of the rotating reference frame.

The main objective of the control system is to deliver the available maximum active power at the input of the MMC converter to the grid for normal operation with unity power factor, to reject the low-frequency harmonic distortions of the output currents produced by the utility grid voltages in order to improve the power quality of the installation, and to be able to deal with FRT operation. The actual values of the instantaneous active (p) and reactive (q) powers are calculated by means of (15) and (16).

The DC bus voltage regulator generates the active power reference Ref_P (proportional to the d component of the grid currents in the synchronous reference frame i^*_d), meanwhile the quadrature component Ref_Q (proportional to i^*_q) will depend on q^* in normal operation and on q_{fault} during a fault. The reference command of the DC voltage V^*_{DC} will vary according to the normal operation (V^*_{DC}MPP) or to the fault operation (V^*_{DC}non-MPP).

The current regulators generate the references of the direct and quadrature components of the converter output voltage in the stationary reference frame, $v^*_{o\alpha}$ and $v^*_{o\beta}$. The references $v^*_{o\alpha}$ and $v^*_{o\beta}$ are transformed into v^*_{oabc} by using the inverse Clarke´s transformation, which are the input of the PD-SPWM voltage modulator.

The modulator sets the semiconductors' switching frequency F_{PWM} and its output is the number of SMs to be set ON in each phase, n_{upi} and n_{lowi} $(i = a, b, c)$.

The last block of the control system is the sorting algorithm to balance the SMs voltages. This block uses the actual SMs voltages and the sign of the arm currents. Its output is the gate signals of the SMs.

The main goal of the PR controllers applied to the α-β components of the 3-phase grid currents is to attain a trade-off between the relative stability, the overshoot and the settling time of the 3-phase output currents. So, its proportional constants are computed as in a PI regulator [42] where its dynamics and stability are ensured by setting an adequate bandwidth (to reduce the voltage ripple due to the switching frequency of the MMC converter) together with the proper phase margin in the

open loop Bode plot. Moreover a zero steady-state error is ensured by selecting the proper integral constants guaranteeing the stability limits [30,50].

For the outermost DC voltage loop, a similar approach is suggested for the computation of its proportional and integral constants of the PI regulator, but a very low bandwidth is mandatory in order to avoid the influence of the AC grid voltages in the loop [30].

The constants of the PI regulator of the PLL will be a function of the settling time (T_{set}) and of the damping factor (ζ) [40]. It is worth noting that these constants need to be normalized with the peak value of the utility grid voltages in order to attain a proper behavior.

The Plant (MMC+Power system) is run at a rate of T_s seconds, meanwhile the Triggered Subsystem updates its outputs at a rate of T_{reg} seconds, simulating an interrupt event used in the microcontrollers for real-time control.

The simulation parameters of the power and control systems and their meaning are listed in Table 5. The constants of the regulators used in this work are highlighted in bold letters.

Table 5. Simulation parameters.

Number of Switching Modules SM	n	*5*
Active Power injected to the Grid	p^*=*Ref_P*	*300KW*
Reactive Power injected to the Grid	q^*=*Ref_Q*	*0*
DC bus voltage	V^*_{DC}	*5KV*
AC system	v_{abc}	- *Voltage level: 2165V(rms) line-to-line* - *Frequency: 50Hz* - *Harmonic Distortion: 5%,4%,3%,2.5% distortion for the magnitude of the 5th, 7ht, 11th, 13th harmonics, respectively* - *Strong Source: 6MVA of short circuit level (R_g=0.039Ω; L_g=2.48mH)* - *Weak Source: 1.5MVA of short circuit level (R_g=2.8Ω; L_g=4.44mH)*
Arm Inductance	L	*375μH*
The SM Capacitor	C	*30mF*
Coupling Inductance	L_c	*3mH*
Converter Gain	K_{PWM}	$\frac{2}{3}V^*_{DC}$
Switching Frequency	F_{PWM}	*6.104kHz*
Current Crossover frequency for open loop Bode (Bandwidth)	f_{cI}	*800Hz*
Current Phase Margin	PM_I	*60° aprox.*
Cut-off frequency for the resonant filter	ω_c	*1rad/s*

Proportional constant of the PR+HC controller	$k_{p,I\alpha I\beta}$	***0.0045***
Integral constant of the PR+HC controller	$k_{i,I\alpha I\beta}$	***3***
Voltage Crossover frequency for open loop Bode (Bandwidth)	f_{cV}	*12.208Hz*
Voltage Phase Margin	PM_V	*63.5°*
Proportional constant of the DC bus voltage regulator	$k_{p,Vcc}$	***0.1764***
Integral constant of the DC bus voltage regulator	$k_{i,Vcc}$	***6.745***
Settling time of the PLL	T_{set}	*20ms*
Damping factor of the PLL	ζ	$\frac{\sqrt{2}}{2}$
Proportional constant of the PI regulator of the PLL	$k_{p,PLL}$	***0.2602***
Integral constant of the PI regulator of the PLL	$k_{i,PLL}$	***59.8513***
Sample period of the Plant	T_s	*5.1196μs*
Sample period of the Triggered Subsystem (Controller)	T_{reg}	*40.957μs*

Figure 13 depicts the Bode plot for the PI and the PR+HC regulators, showing a stability behavior for both at the selected crossover frequencies and phase margins. It is worth noting that the HC structure does not affect the dynamics of the PR regulators because the peaks in the magnitude and phase will only appear around the resonance frequencies.

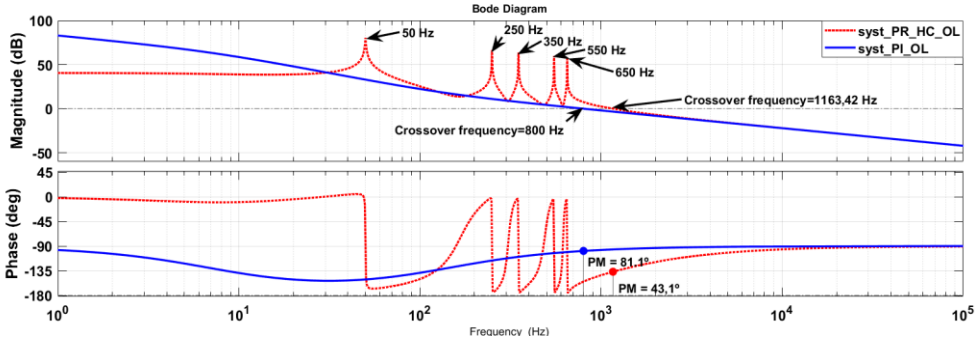


Figure 13. Open Loop Bode plot for the PI and PR+HC regulators applied to the inner current loop.

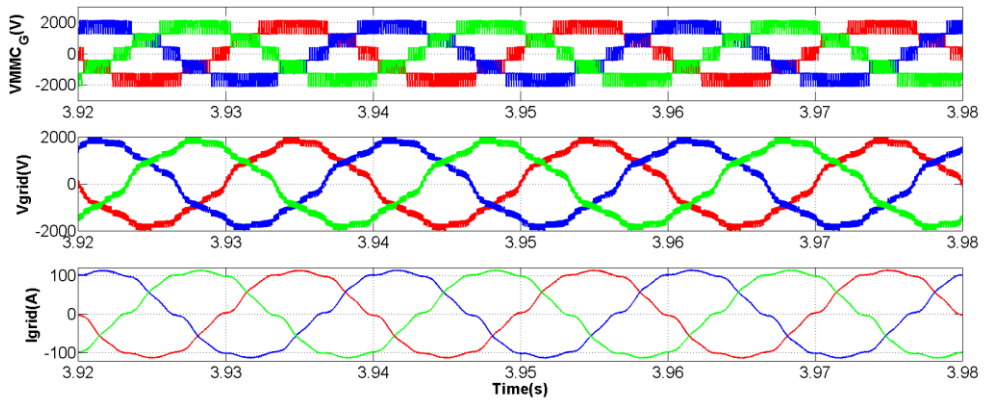
For the PD-SPWM, three modulators (one per phase) were implemented using five triangular carriers (see Figure 11). The modulators compare the references of the converter voltage v_{oabc}^* with the carriers to generate the number of SMs to be switched ON in each arm (Table 2), n_{up} and n_{low}, and therefore, the three converter voltages v_{oabc}.

Next, several test simulations will be carried out for a Strong Grid firstly, and then for a Weak Grid (see Table 5 for R_g and L_g values) in order to validate the control algorithms applied to the power system. For all the tests the nominal active power injected into the grid is 300kW with unity power factor in normal operation (no fault). Mainly, a comparison is made for the dq control algorithm in d-q axes and the PR+HC control in α-β axes.

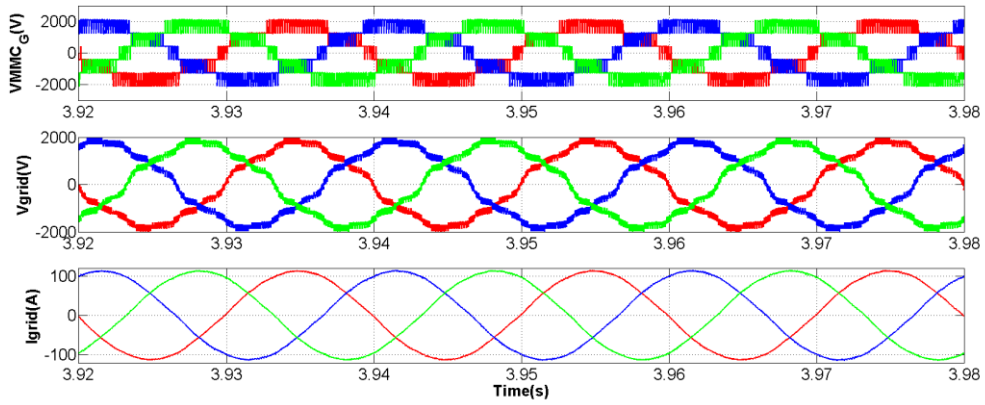
6.1 Strong Grid

Test 1. 5 SM, F_{PWM} = 6104Hz, $\boldsymbol{V_{DC}^{*}}$ **= 4200V**

Figures 14 depicts the time evolution of the 3-phase MMC voltages, utility grid voltages and the grid currents for the dq control strategy and the PR controller plus the HC structure. For both situations, the maximum and minimum amplitude of the MMC voltages are ±2100V and a remarkable attenuation in the magnitude of the low-order harmonics of the grid currents can be seen for the PR controller + HC compared with the harmonic contamination in the dq control strategy.



(a)



(b)

Figure 14. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.

(a) dq control.
(b) PR controller + HC.

Figure 15 shows the time evolution of the current error in d-q and α-β axes at steady- state. Although there is an average zero steady-state error for both situations, a low-frequency oscillation can be observed in in d-q axes due to the influence of the low-order harmonic distortions of the utility

grid voltages. However, there is no oscillation in α-β axes due to the compensation exerted by the HC structure.

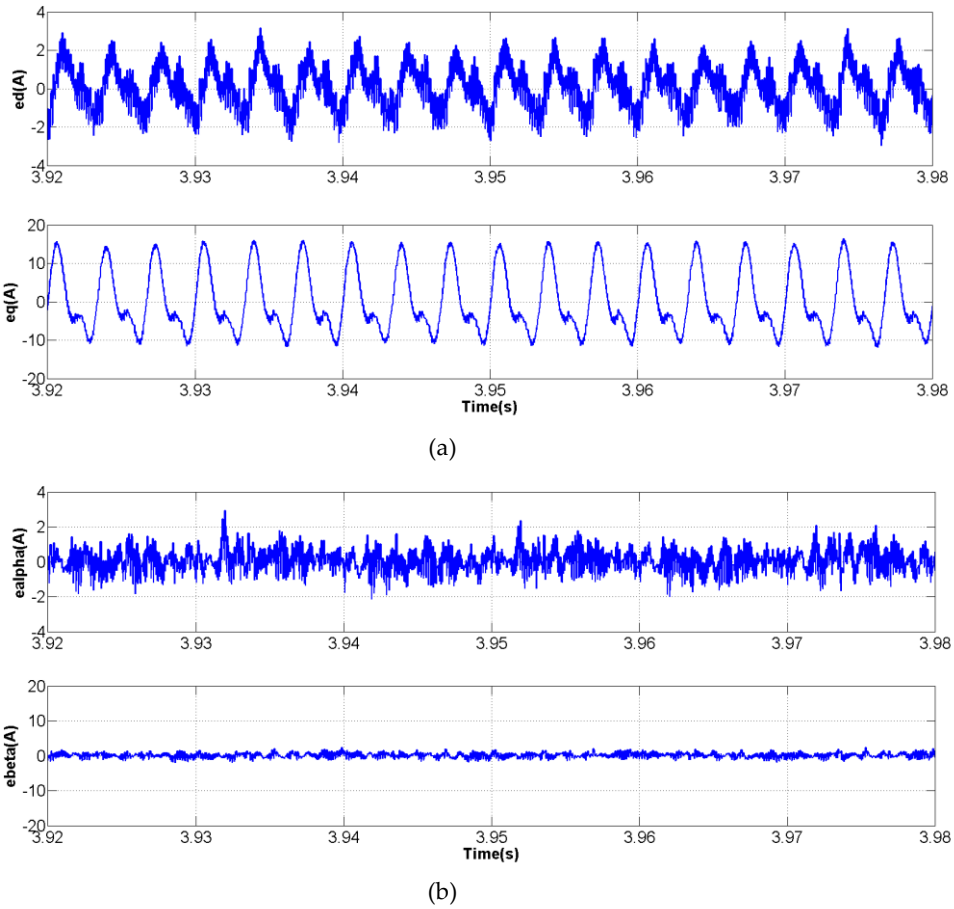
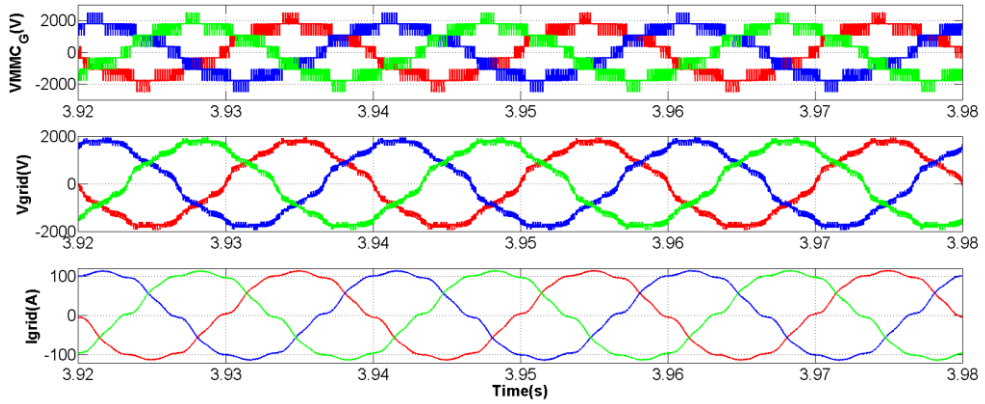


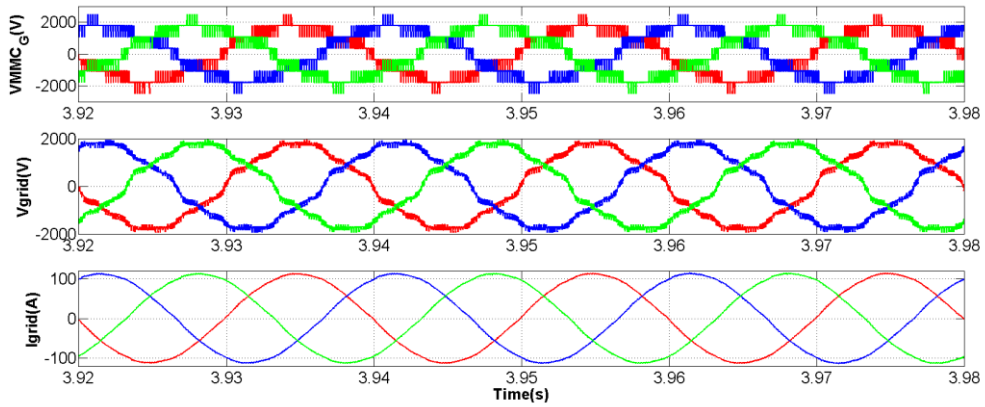
Figure 15. Time evolution of the current errors.
(a) d-q axes (dq control).
(b) α-β axes (PR controller + HC).

<u>Test 2.</u> 7 SM, F_{PWM} = 6104Hz, $\boldsymbol{V_{DC}^{*}}$ **= 5000V**

This test is similar to Test 1, but in this case 7 switching modules (7 SM) are employed and the DC bus voltage is increased to 5000V. Figure 16 depicts the time evolution of the 3-phase MMC voltages, utility grid voltages and the grid currents for both control strategies. Comparing with Figure 14, it is worth noting that the voltage levels has increased from 6 to 8 in the upper plot, whereas the maximum and minimum amplitude of the MMC voltages are ±2500V. Again, the harmonic distortion of the 3-phase grid currents is lower in the PR+HC control strategy.



(a)



(b)

Figure 16. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.

(a) dq control.

(b) PR controller + HC.

501

502 **<u>Test 3.</u> 5 SM, F_{PWM} = 7630 Hz,** V_{DC}^{*} = 5000V

503 In this test, 5 SM are used and the switching frequency F_{PWM} is set to 7630Hz, while the DC
504 bus voltage remains in 5000V. Figure 17 shows the time evolution of the 3-phase MMC voltages,
505 utility grid voltages and the grid currents for PR controller plus the HC structure. Again, the 3-
506 phase grid currents are almost sinusoidal with no distortions.

507

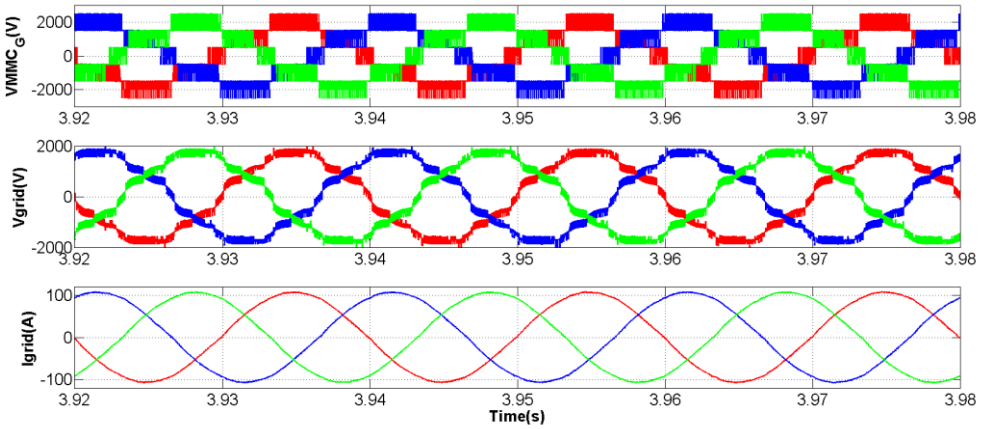


Figure 17. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively (PR controller + HC).

Test 4. 5 SM, $\boldsymbol{F_{PWM}}$ **= 9156Hz**, V_{DC}^{*}=5000V

In this case, the switching frequency F_{PWM} is increased to 9156Hz. Figure 18 shows the time evolution of the 3-phase MMC voltages, utility grid voltages and the grid currents for PR controller plus the HC structure with a similar behavior as Test 3.

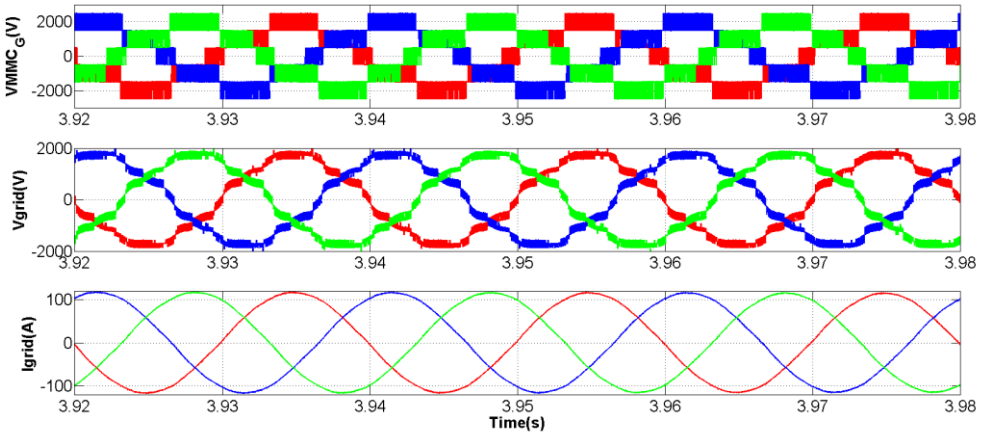


Figure 18. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively (PR controller + HC).

6.2 Weak Grid

Test 5. 5 SM, F_{PWM} = 7630Hz, V_{DC}^{*}=5000V

For a switching frequency F_{PWM} set to 7630Hz, Figure 19 depicts a similar behavior as Figure 17 (Test 3, Strong Grid), although the amplitude of the 3-phase grid currents is less for this case.

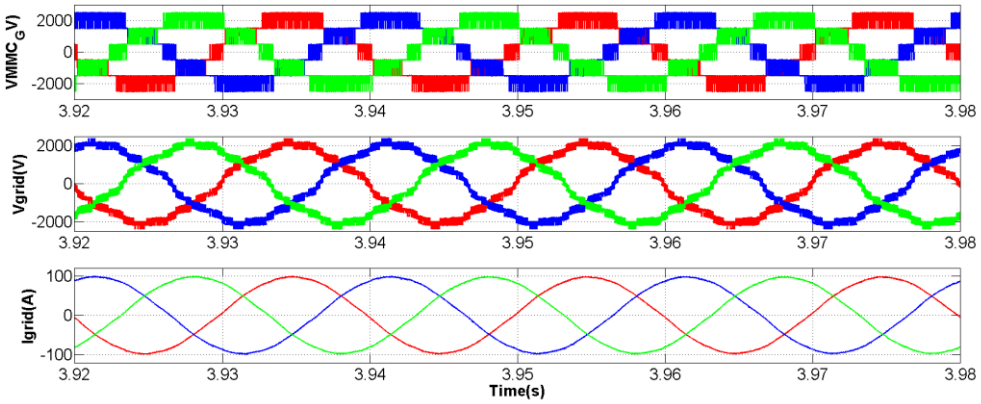


Figure 19. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively (PR controller + HC).

Test 6. 5 SM, F_{PWM} = 9156Hz, V_{DC}^{*}=5000V

In this case, the switching frequency F_{PWM} is set to 9156Hz and the time evolution of the 3-phase variables are depicted in Figure 20. Comparing this Figure with Figure 18 (Test 4, Strong Grid), the amplitude of the 3-phase grid currents is also less for this case.

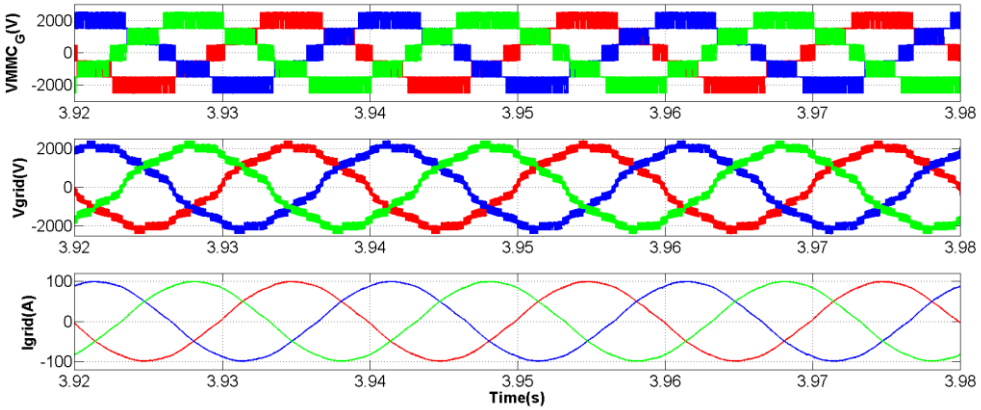


Figure 20. Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively (PR controller + HC).

6.3 Voltage Sags

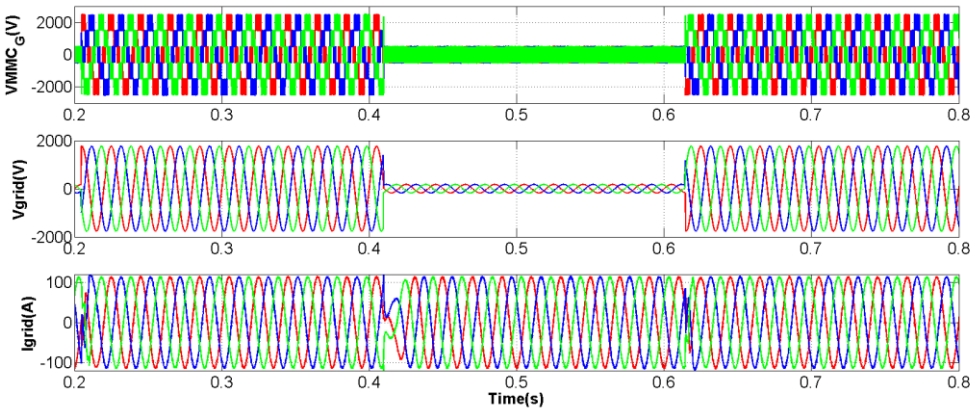
Next tests are intended to deal with voltage faults at the converter terminal. In general, grid codes [51,52] force the converter not only to remain connected even when severe faults occur, but also to inject a certain amount of reactive power according to the depth of the voltage sag, together with a limitation of the output grid currents to its nominal value, avoiding the automatic disconnection due to the overcurrent protection. This feature is known as Low-Voltage-Ride-Through (LVRT) or Fault-Ride-Through (FRT). In short, it must be pointed out that there will be two mode of operations: one mode is for normal operation with nominal values of the active (P) and reactive (Q) powers, meanwhile the second mode of operation will be activated when fault events occur.

For the next tests, there are 5 SM, the switching frequency is F_{PWM} = 6104Hz, and the DC bus voltage V_{DC}^{*}=5000V.

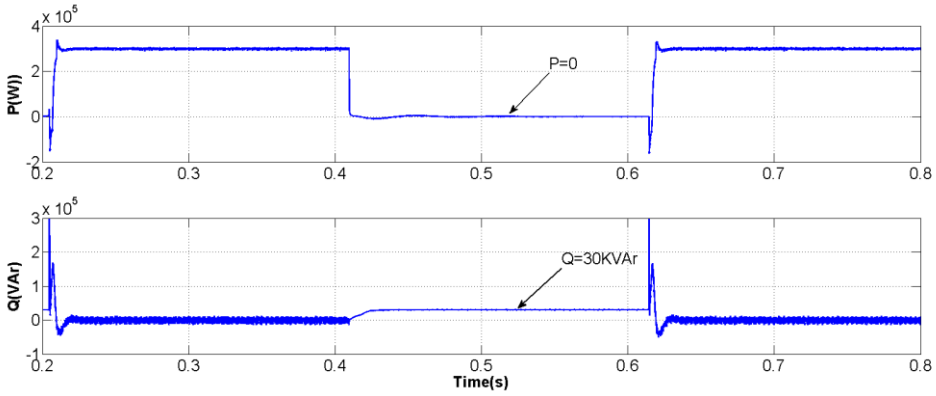
Test 7. 3-phase deep voltage sag (0.1(pu))

Figure 21 and 22 depict the response of the control algorithm to a 3-phase deep voltage sag (0.1 (pu)) for the dq control and the PR controller strategies, respectively. It can be observed that both strategies behave similar. The 3-phase fault event occurs at 0.42s approximately and, in the lower plot of (a) the time evolution of the 3-phase output grid currents indicates that there are no overcurrent during the event, meanwhile in (b) the plot indicates that the active power (P) is zero and the reactive power (Q) is 30KVAr. When the fault event finishes, the normal operation of the grid-connected MMC is established (P=300KW and Q=0).

Because of the similar behavior of both strategies when dealing with a 3-phase deep voltage sag together with the capability of the PR controller + HC structure to compensate the low-order harmonic distortions of the utility grid voltages, this control strategy will be evaluated in the next tests.



(a)



(b)

Figure 21. 3-phase deep voltage sag (0.1 (pu)) using the dq control strategy
(a) Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.
(b) Time evolution of the active (P) and reactive power (Q)

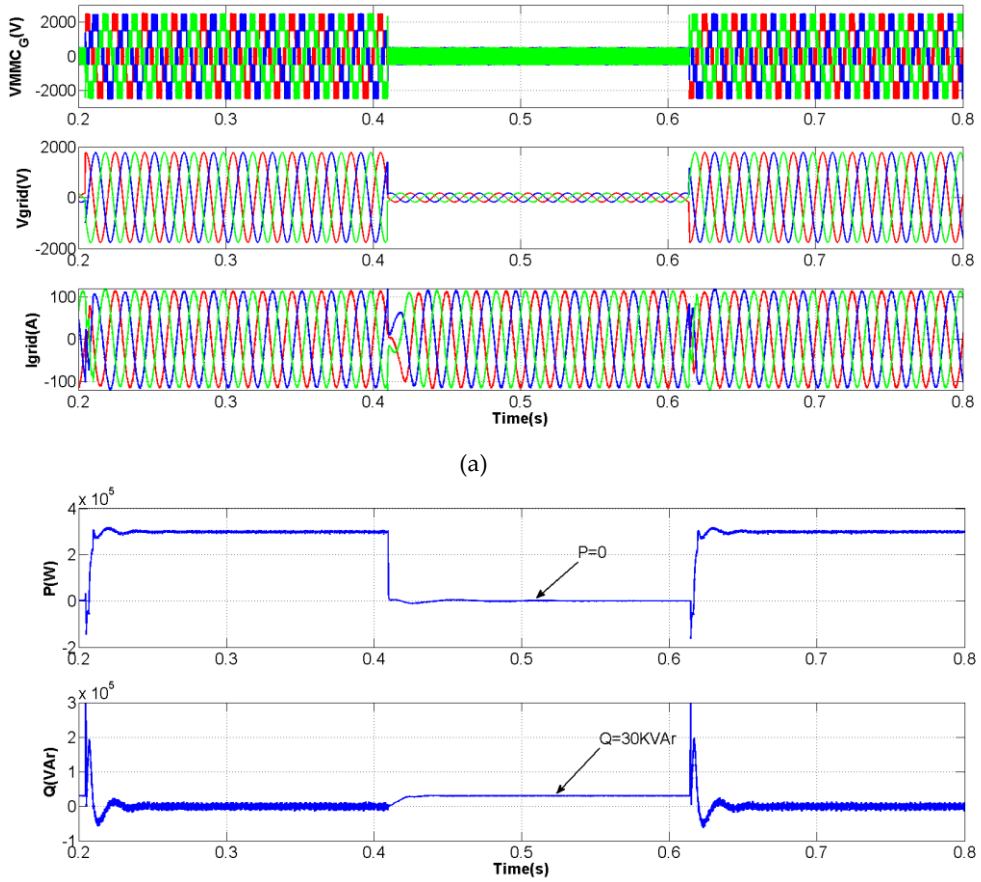
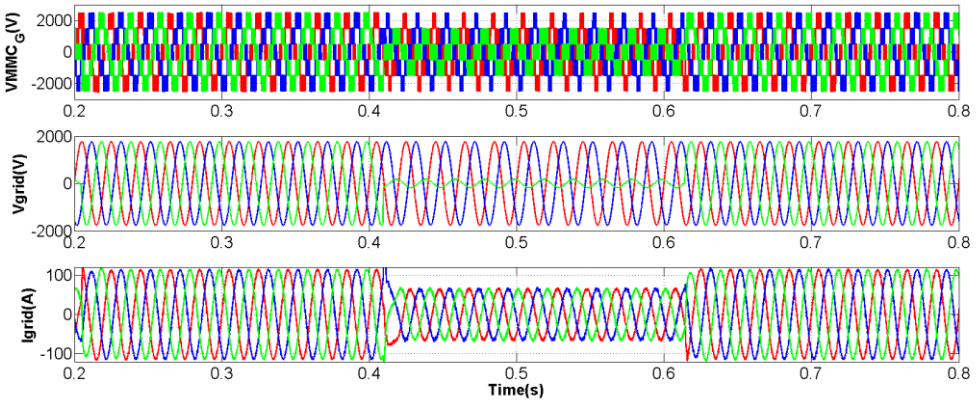


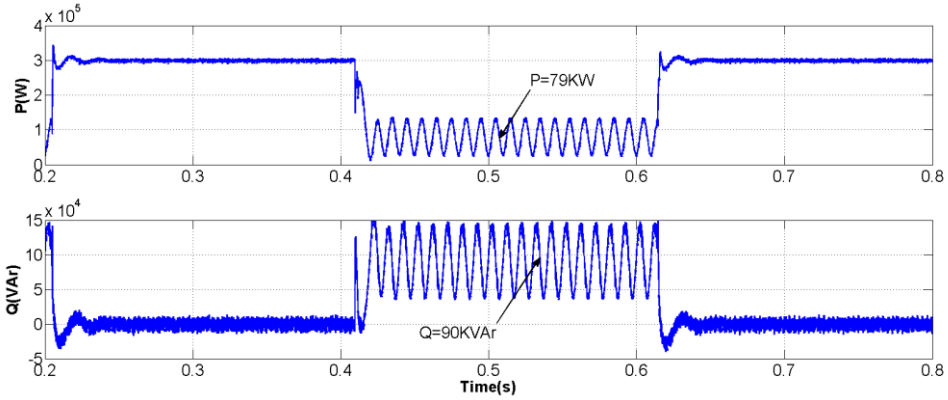
Figure 22. 3-phase deep voltage sag (0.1 (pu)) using the PR control strategy
(a) Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.
(b) Time evolution of the active (P) and reactive power (Q)

Test 8. Deep voltage sag in phase 3 (0.1(pu))

In this case, a deep voltage sag occurs at 0.42s approximately in phase 3 as shown in Fig. 23a. During the fault the 3-phase output currents are below its nominal value, meanwhile a certain amount of active power P=79KW and a reactive power Q=90KVAr are injected into the grid. The negative sequence component of the 3-phase utility grid voltages during the unbalanced fault (with angular speed ω^{-} in the rotating reference frame) together with its positive sequence produce the oscillating nature of the active and reactive powers at the second order harmonic of the fundamental frequency around their mean values. Also, the normal operation is attained when the fault event finishes.



(a)

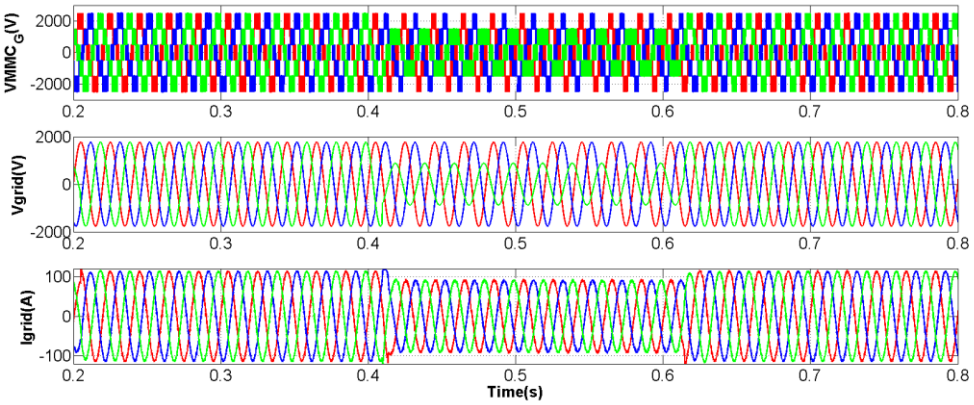


(b)

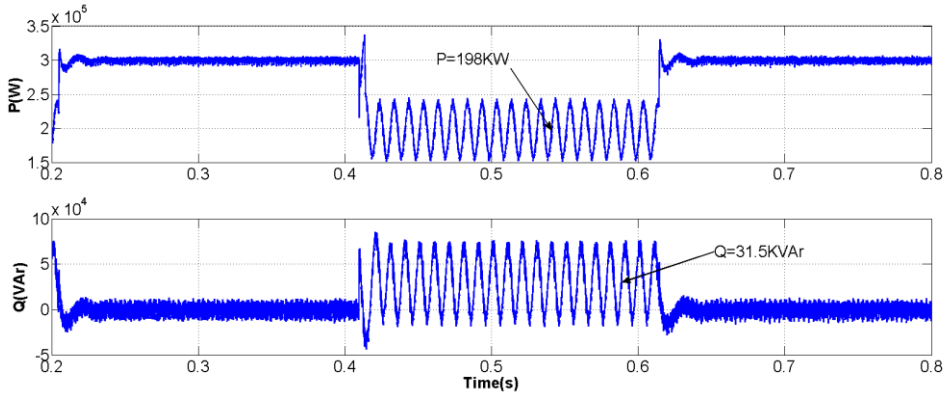
Figure 23. Deep voltage sag in phase 3(0.1 (pu)) using the PR control strategy
(a) Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.
(b) Time evolution of the active (P) and reactive power (Q)

Test 9. Moderate voltage sag in phase 3 (0.5(pu))

Figure 24 depicts a moderate voltage sag in phase 3 (0.5 (pu)). Again the output grid currents are below its nominal value and, in this case, a higher amount of active power is injected into the grid (P=198KW), and the reactive power Q=31.5KVAr. Again, the negative sequence of the 3-phase utility grid voltages produces the second order harmonic oscillations around the mean value of the active and reactive powers. When the fault ends, the normal operation is reached.



(a)



(b)

Figure 24. Moderate voltage sag in phase 3(0.5 (pu)) using the PR control strategy
(a) Time evolution of the 3-phase MMC voltages, utility grid voltages, and grid currents, respectively.
(b) Time evolution of the active (P) and reactive power (Q)

7. Experiments

Some experiments are shown in this paper to reinforce the validity of the control algorithm with Proportional Resonant controllers, and the Hardware-in-the-Loop (HIL) Simulation technique [53,54,55] is used for this. On one hand this technique uses a Real Time Digital Simulator (RTDS) with several I/O digital signals, as well as analog to digital and/or digital to analog converters (ADC and DAC blocks), in order to simulate in real time the behavior of any power system, including the power converter. On the other hand, an actual controller is connected to the input/output signals of the RTDS in order to exert a real time control. The actual controller ignores if the control is being exerted to a Simulator or to an actual power system, but the exchange of power is avoided and the safety of the installation is guaranteed, as well as the possibility to impose a series of critical tests to explore the response of the implemented control algorithms before the development of the prototype.

The RTDS platform used in this paper is built with the dSPACE DS1006 power processor, and the DS5202 Electric Motor HIL Solution boards with several I/O digital signals, and ADC and DAC blocks. The latter is the interface between the power processor and the controller prototype that is built with the dSPACE DS1104 card (see Figures 25 and 26). The model blocks of both the RTDS and the controller are built in MATLAB/SIMULINK in two Host PCs (Host PC 1: Windows 7 Professional (64 bits), 4GBytes of RAM, Intel Core i3 530@2.93GHz; Host PC 2: Windows XP SP3 (32 bits), 4GBytes of RAM, Intel Core 2 6300@1.86GHz), the C-code is generated automatically with Real Time workshop and downloaded into both targets.

For the RTDS platform, the range of analog voltage of the ANALOG OUT1-6 is ±10V (single-ended) and is used for the 3-phase grid voltages (v_{abc}) and currents (i_{abc}), meanwhile for the ANALOG OUT7 is +10V and is used for the DC bus voltage (V_{DC}). The range of the analog voltage of the ANALOG IN1-3 is ±15V (single-ended) and are fed by the duty cycles (d_{voabc}) sent by the controller card. For the controller prototype, the ADCs and DACs have an analog voltage range of ±10V (single-ended). For both, the RTDS platform and the controller prototype, all voltage ranges are expressed as peak values, and it is worth noting that according to these voltage levels, both electronic cards can be connected directly because dSPACE ensures the compatibility [56], although additional signal conditioner electronic circuits can be used to accommodate different levels of voltages and currents.

Finally, some measurements are displayed in an oscilloscope for monitoring purposes.

It must be pointed out that an average model for the MMC is used in the power system, and the 3-phase utility grid voltages are perturbed with the 5th, 7th, 11th, and 13th harmonics, with an amplitude of 5, 4, 3 and 2.5%, respectively, compared to the magnitude of the fundamental frequency of 50Hz. The time step is set to 13.65μs for the RTDS (T_s) and to 40.96μs for the controller (T_{reg}); the latter has a delay of $\frac{3}{2}T_{reg} = 61.44\mu s$ in the worst case. Furthermore, the discretization of any digital filter of the PSD block in the PLL, eg. the 90-degree phase-shift operator S90 [40,47], which not also reject the negative sequence of the 3-phase utility grid voltages, but also reduce the unbalances produced at the output of the data acquisition electronic card as said before [48], must obey the time step of the controller algorithm to avoid the degradation of the power factor. Firstly, the tests are carried out when the dq control strategy is used to regulate the 3-phase line currents; and secondly, the same tests are carried out when the PR controller and the HC structure are used.

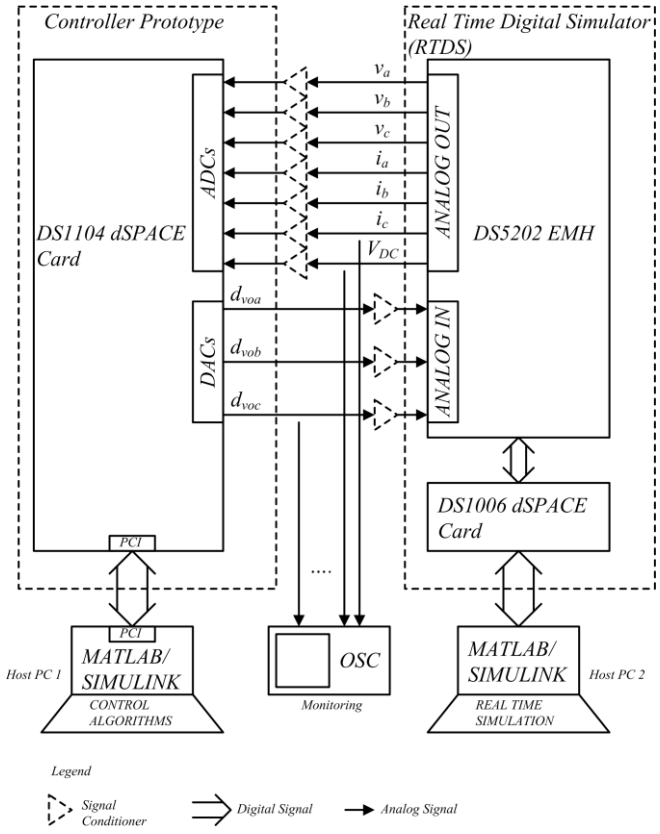


Figure 25. Block diagram of the HIL platform.

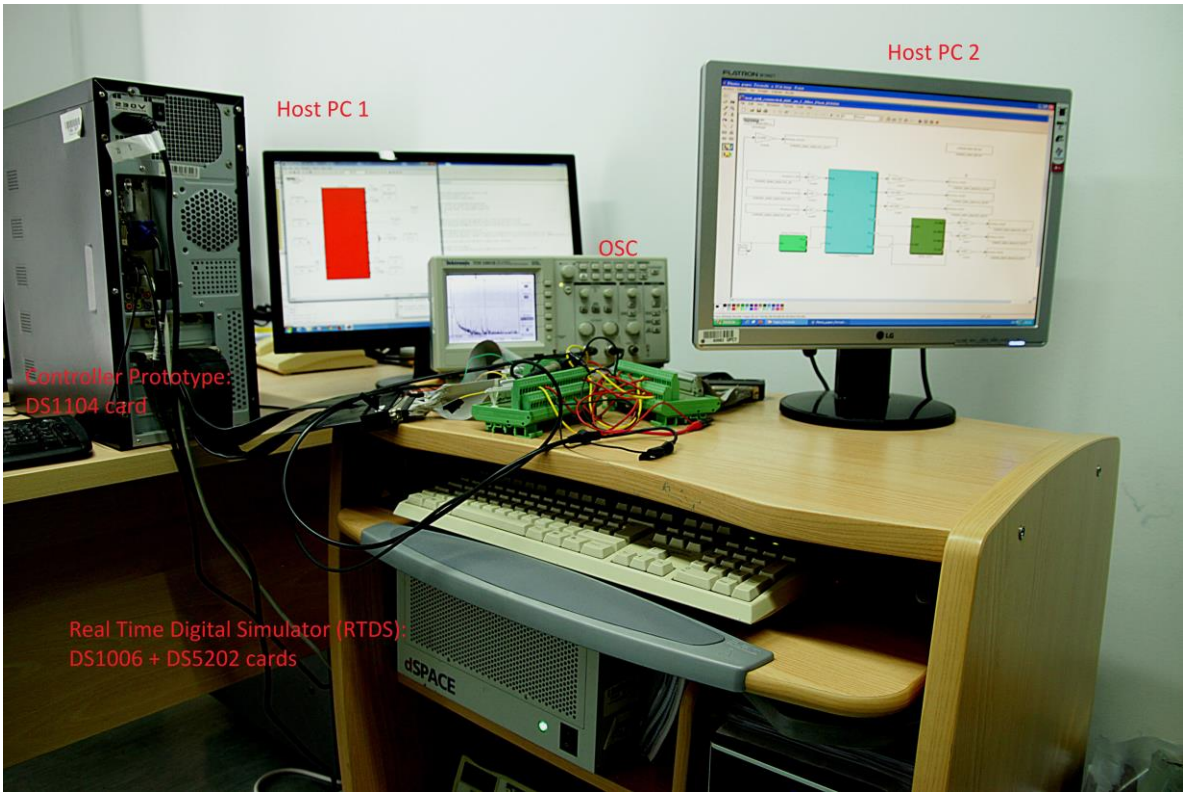


Figure 26. Photo of the HIL platform.

The time evolution of the grid voltage and current at phase 1 is depicted in Figure 27a, meanwhile the frequency spectrums of the grid current is depicted in Figure 27b for the dq control algorithm. In this case, the individual low-order harmonic distortions of the grid current exceeds the limits imposed by the Normative (see Table 4), except for the 11^{th} harmonic, and the THD also exceeds the limit of the Normative, as can be seen in Table 6. So, the dq control strategy will not be valid for the connection of the renewable system to the utility grid if the 3-phase utility grid voltages were disturbed by the maximum allowed magnitude distortions in the low-order harmonics.

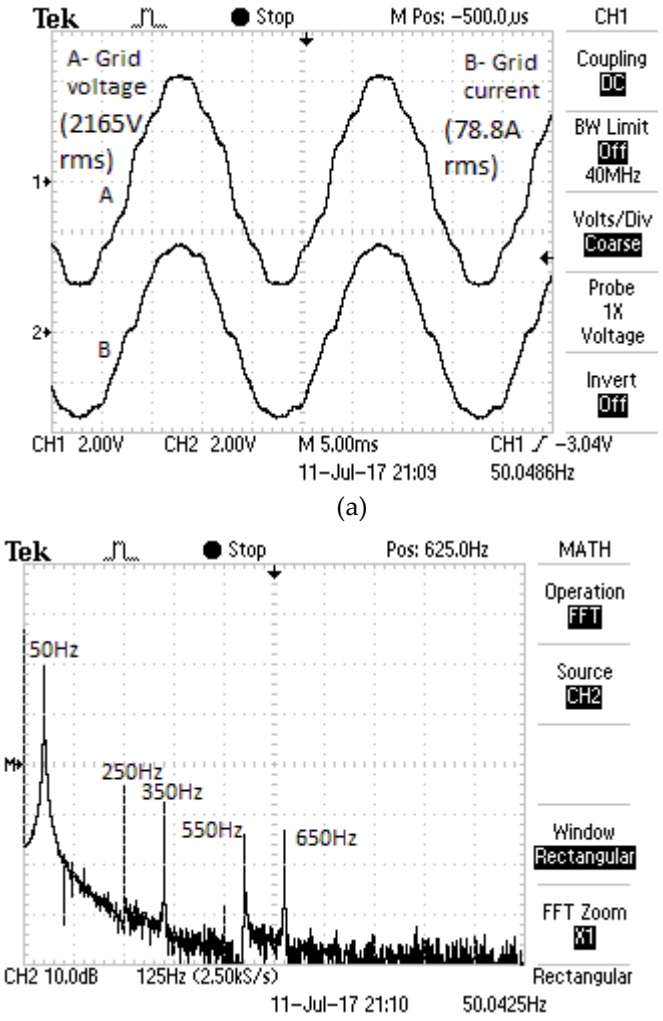


Figure 27. (a) Time evolution of utility grid voltage and current at phase 1 for dq control. **(b)** Frequency spectrum of the grid current at phase 1.

Table 6. Harmonic distortion for the grid current in phase 1 (**dq control**).

Harmonic	Measured value (%)		Maximum value (%)
5	6.3	>	4
7	4.47	>	4
11	2	=	2
13	2.24	>	2
THD	8.29	>	5

The same situation is shown in Figure 28a and 28b when the PR controller and the HC structure are used. In this case, both the individual harmonic distortions in the magnitude of the grid current, as well as its THD are lower than the limits imposed by the Normative, as can be seen in Table 7. So, the PR controller plus the HC are valid for the connection of the renewable system to the utility grid even for the maximum allowed distortion in the magnitude of the low-order harmonics of the 3-phase utility grid voltages.

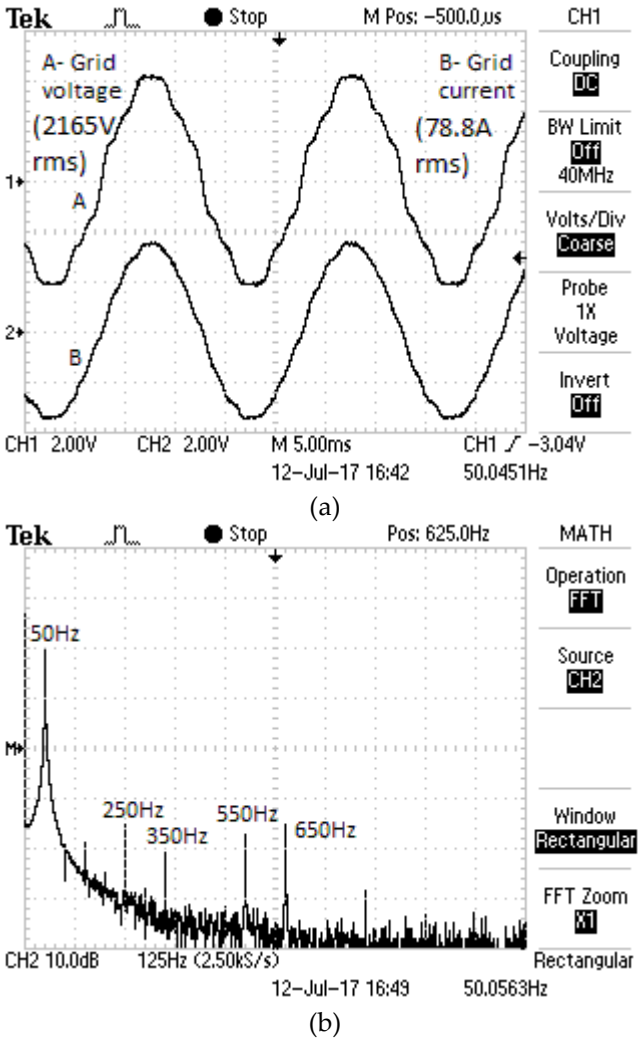


Figure 28. (a) Time evolution of utility grid voltage and current at phase 1 for the PR controller and the HC structure.

(b) Frequency spectrum of the grid current at phase 1.

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668 **Table 7.** Harmonic distortion for the grid current in phase 1 (**PR Control + HC**).

Harmonic	Measured value (%)		Maximum value (%)
5	1.78	<	4
7	0.94	<	4
11	1.41	<	2
13	1.78	<	2
THD	3.04	<	5

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8. Conclusions

This article presents a comprehensive and detailed study of an enhanced control of an MMC, mainly because a reduction in the need for AC filtering is achieved, reducing also the overall cost of the installation. Its easy scalability will be useful for those who want to integrate it into a larger application which may include two MMCs (one for the AC/DC conversion and one for DC/AC), or into an offshore wind application. However, the use of MMCs needs more sophisticated algorithms for balancing the voltages of the high number of modules, and modulators such as the PD-SPWM used in this paper to generate the multilevel output voltage, yielding to the use of more powerful microcontrollers.

The Proportional Resonant (PR) controllers and a Harmonic Compensator (HC) scheme, both in the stationary reference frame, are used as an enhanced controller in this paper for the inner current control loops, unlike the commonly used PI regulators in the synchronous reference frame. For both strategies, the power factor of the MMC-grid connection can be controlled in the same manner. The power balance is done with a PI regulator in the outer DC bus voltage control loop, guaranteeing the injection of the maximum available power, coming from the Renewable system at the input of the MMC, into the utility grid.

The simulations and experiments carried out validate the behavior of the enhanced controller. Regarding the experiments, it can be seen that the amplitude of the individual and total harmonic distortions of the 3-phase grid currents is below the limits imposed by the grid code when the PR plus the HC controller is used, improving the power quality and making possible the MMC-grid connection, meanwhile these distortions exceed the limits when the PI regulators are employed, which do not allow the connection.

The effects of single-phase and three-phase low voltage, single-phase and three-phase faults and grid unbalances have been simulated. In all cases, the converter remains connected, the grid current does not exceed the nominal value and neither active nor reactive power of the grid is demanded.

Finally, the PR plus the HC controller can be used in any other application that controls the currents in the inner loops of the power converter, i.e., Active Power Filters (APF), Voltage Source Converters (VSC) for renewables, stand-alone and grid-connected microgrids, etc. In addition, this control strategy can be applied in 1- or 3-phase systems.

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