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A Case Study in CMOS Design Scaling for Analog Applications: The Ringamp LDO

Steven Corum
University of Tennessee, Knoxville, scorum@vols.utk.edu

To the Graduate Council:

I am submitting herewith a thesis written by Steven Corum entitled "A Case Study in CMOS Design Scaling for Analog Applications: The Ringamp LDO." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this thesis and recommend its acceptance:

Nicole McFarlane, Garrett Rose

Accepted for the Council:
Dixie L. Thompson

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

A Case Study in CMOS Design Scaling for Analog Applications: The Ringamp LDO

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Degree

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Steven Bradley Corum

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This work is dedicated to the memories of my Father and Mother,

James Corum and Debbie Nicely.

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Abstract

As CMOS process nodes scale to smaller feature sizes, process optimizations are made to achieve improvements in digital circuit performance, such as increasing speed and memory, while decreasing power consumption. Unfortunately for analog design, these optimizations usually come at the expense of poorer transistor performance, such as reduced small signal output resistance and increased channel length modulation. The ring amplifier has been proposed as a digital solution to the analog scaling problem, by configuring digital inverters to function as analog amplifiers through deadzone biasing. As digital inverters naturally scale, the ring amplifier is a promising area of exploration for analog design. This work presents a ring amplifier scaling study by demonstration of scaling an output capacitor-less, ring amplifier based low-dropout voltage regulator designed in a standard 180 nm CMOS process down to a standard 90 nm CMOS process.

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Chapter 1

Introduction

In July 1958, Jack Kilby had recently joined Texas Instruments (TI) as a new employee. Since he hadn't yet accumulated vacation time, Kilby spent the July holidays at TI working alone, aiming to reduce the complexity of wiring between transistor devices. During this process, Kilby contemplated the concept of integrating multiple transistors on a single piece of silicon or germanium and connecting their terminals with wires. This innovative idea would later be known as the Integrated Circuit (IC) and would have a profound and lasting impact on the world's technological and economic development [1].

A year earlier Robert Noyce, alongside Gordon Moore, Jean Hoerni, and five others, departed William Shockley's (co-inventor of the transistor) lab to establish Fairchild Semiconductor. For this exodus, the group was labeled the "traitorous eight". At the same time that Kilby was working on the IC, Hoerni was addressing a different challenge. During that period, transistors were fabricated using a process by which a wax material was deposited onto germanium and later removed. Once the wax layer was removed, the transistors had a mesa-like appearance, referred to as "Mesa structures." Unfortunately, these structures were highly susceptible to impurities from the air. Hoerni's solution to this problem involved embedding the transistors into the germanium instead of fabricating them on top of it. Following Hoerni's groundbreaking "Planar Method" in manufacturing, Noyce recognized that instead of connecting transistor terminals with wires, metal lines could be directly deposited onto the semiconductor, similar to and an improvement upon Kilby's advancement, but with the added benefit of using planar transistors [1].

Back at TI, later in 1958, Jay Lathrop was solving another manufacturing problem. To make smaller transistors, smaller amounts of the wax material had to be deposited in smaller areas, which was starting to become a significant challenge. Lathrop had an idea based on the principle of how microscopes work. He considered that if a microscope uses lenses to make the image of something small appear large, lenses could also be used to make something large have a small image. This concept allowed for masks of the transistors to be more easily deposited by passing light through a large mask into a lens and focused onto a small area on a semiconductor on which photo-resist chemicals have already been deposited. The process is called "Photo Lithography." As minimum transistor gate lengths and other fabrication spacing requirements are largely established by the wavelength of light used in the photolithography process, the ability to scale this process for smaller wavelengths has significantly contributed to the massive device scaling that the world has seen over the last 65 years [1].

In 1965, Moore, who also co-founded Intel alongside Noyce, published a paper [2] in which he discussed an observed phenomenon that the number of components per chip approximately doubled year by year. This observation has since been famously named "Moore's Law" and characterizes the rapid pace of technological advancement. Moore's Law is more of a self-fulfilling prophecy driven by economic necessity and technological limitations than a fundamental law of nature. The primary method for achieving Moore's Law is by continually reducing transistor gate length through the introduction of new process node generations. This reduction in gate length leads to an increase in transistor density per chip and wafer yield, resulting in an overall decrease in fabrication cost per transistor, which is a highly advantageous outcome [3]

As CMOS technology advances to smaller process nodes, thanks to the innovations of Kilby, Hoerni, Noyce, Lathrop, Moore, and many others, digital circuit designs can readily adapt, benefiting from process optimizations tailored to digital circuits. This progress has resulted in significant enhancements in digital processing power, speed, memory, and more, as exemplified by the capabilities of the computer that is likely used to read this thesis. However, scaling poses a more complex challenge for analog circuit designs with each new process node generation [1, 2, 4, 5].

Analog circuit designers are routinely compelled to innovate circuit topologies merely to maintain functional performance in light of shrinking process nodes. A few illustrative examples are current matching and fractional error. When going from a long channel process to a short channel process, channel length modulation (λ) increases, resulting in poor current matching. Current matching is critical for establishing proper biasing within many analog circuits. Another analog design impact from scaled process nodes is reduced small-signal output resistance (r_o) which results in reduced terminal voltage gain (A_{vt}). A reduced A_{vt} results in an increased fractional error, which is the difference between the ideal and measured closed loop gains and has a direct impact on the total output error of the negative feedback amplifier [4, 5, 6, 7].

1.1 Motivation

In 2012, Benjamin Hershberg proposed the ring amplifier (ringamp) as a solution to the analog amplifier scaling challenge [8]. The ringamp can be viewed, at its simplest, as a ring oscillator that is modified for stability, making it suitable for use as a linear feedback amplifier. Since the ringamp, like the ring oscillator, consists of a chain of digital inverters, there is a promise of natural scalability, making ringamps an exciting prospect for analog CMOS amplifiers [8].

The fundamental structure of the ringamp is shown in Figure 1.1. To understand how the ringamp achieves stability, let's consider a simplified view of its operation during the sampling and amplification phases. In the sampling phase, the RST switches close, charging C_1 to V_{IN} minus the switch point (V_M) of the first inverter, typically V_M is at mid-rail. V_{DZ} charges C_2 to V_M minus $\frac{V_{DZ}}{2}$ and charges C_3 to V_M plus $\frac{V_{DZ}}{2}$. V_{DZ} is a systematic offset voltage used to "deadzone bias" the output inverter stage. It pulls the upper second stage inverter down to push the gate of M_{CP} near the cutoff region of operation, while M_{CN} is pulled down to a near cutoff region of operation [8].

During the amplification phase, the RST switches open. In steady state, C_1, C_2, and C_3 maintain the deadzone biasing established during the sampling phase. Assuming all NMOS devices are equally sized and all PMOS devices are equally sized for simplicity if all

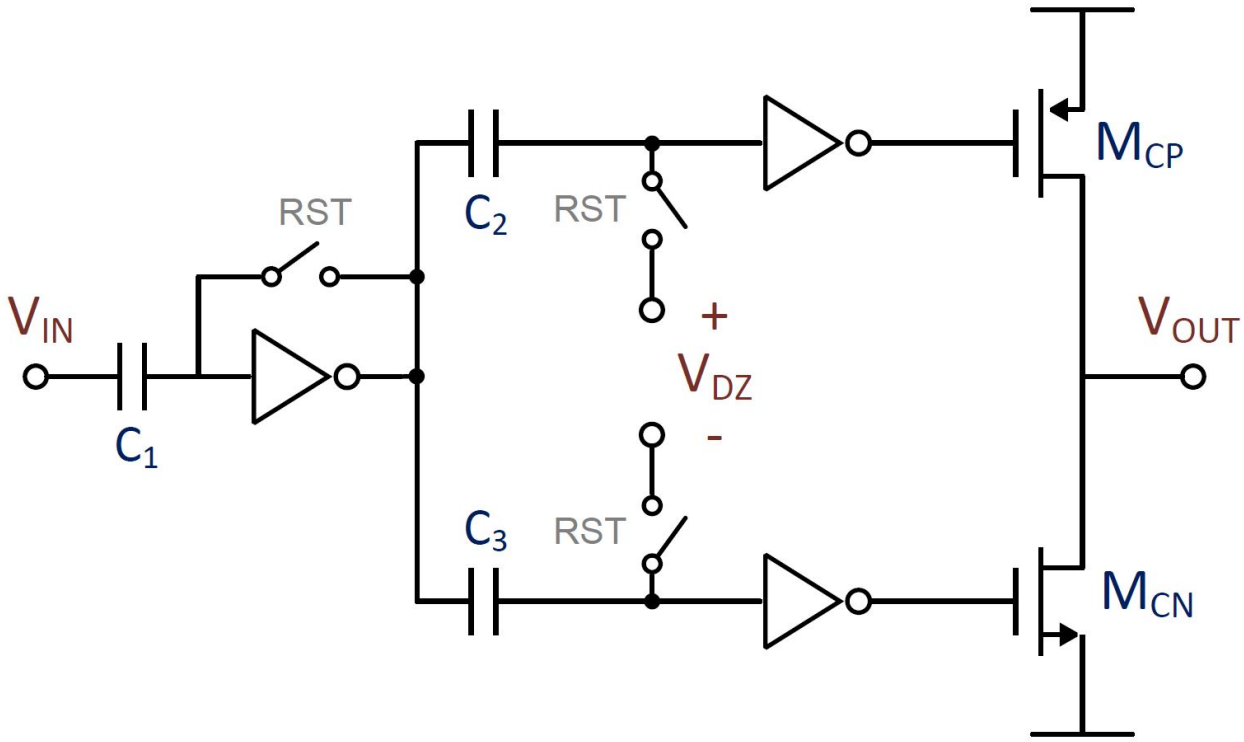

Figure 1.1: Fundamental ringamp structure schematic [8].

three inverters are biased similarly, the corresponding poles would also be similar, leading to positive feedback and instability. However, in this configuration, the bias current of the second-stage inverter is decreased, which increases its output resistance (r_o) and results in a decreased pole location. The output stage inverter's bias current is further reduced, resulting in a much lower output pole location, which becomes the dominant pole of the ring amplifier. By careful implementation of deadzone biasing, the pole locations of the three inverters can be shifted and a stable negative feedback amplifier can be achieved [8].

As ringamps are a relatively new technology with few implementations, it is challenging to assess the validity of the scalability claim. Most ringamp implementations have been within a flavor of pipeline analog-to-digital converters (ADCs) or successive-approximate-register (SAR) assisted pipeline ADCs. To date, there have also been four ringamp-based LDOs (RLDO), with the latest one providing the direct motivation for this work [9].

In 2022, Jordan Sangid proposed the first output capacitor-less (OCL) ringamp-assisted analog LDO (RLDOE), which he implemented using a standard 180 nm CMOS process [9]. Additionally, Sangid introduced an on-demand ringamp design guide that offers a simple and intuitive approach to designing and scaling Class B and AB ringamp topologies. The design guide provides Matlab® scripts to assist in determining the unit inverter sizing. As a study of the scalability of ringamps, this work will scale the ringamp loop of Sangid's RLDOE down to a standard 90 nm CMOS process [9].

1.2 Thesis Overview

This work documents the scaling of the RLDOE from a standard 180 nm CMOS process to a standard 90 nm CMOS process. Chapter 2 provides the reader with background information on LDO operation, the RLDOE, the ringamp design guide, and challenges associated with process scaling related to the reverse short channel effect (RSCE). Chapter 3 documents the design of the 90 nm Ringamp LDO (RLDO) and outlines the design scaling process for the ringamp unit inverter. Chapter 4 defines the evaluation setup required for testing the 90 nm RLDO and presents the experimental results, along with comparisons to the simulation results. This work is also directly compared to Sangid's 180 nm RLDOE. Chapter 5 provides

a summary of this work with a discussion of proposed future work including RLDO design improvements, enhancements to the ringamp design guide, and improvements for a multi-loop RLDO.

Chapter 2

Background

2.1 Low-Dropout Voltage Regulators

Linear voltage regulators (LVRs) are used to provide stable voltage sources for various applications while also offering buffering from the external supply. Low-dropout voltage regulators (LDOs) belong to a class of LVRs with a small voltage drop between the input voltage (V_{IN}) and the output voltage (V_{OUT}). LDOs provide a low-power approach to voltage regulation due to the small dropout voltage (V_{DO}), which offers clear benefits for battery-powered systems. There are many types of LDOs; however, the only topology discussed in this section is the analog operational transconductance amplifier (OTA) driven, PMOS pass device topology. This LDO topology, shown in Figure 2.1, is the fundamental structure for Sangid's RLDOE [9, 10].

2.1.1 LDO Operation

When the LDO load current (I_{LOAD}) increases, the stored charge on the load capacitance (C_{LOAD}) is dumped into I_{LOAD}. This charge dumping decreases V_{OUT}, which increases the V_{SD} of the pass device (M_{PASS}) and creates an error voltage (Δv_e) at the OTA input. The Δv_e causes the OTA to drive V_{SG} of M_{PASS}, allowing the new I_{LOAD} to be met at the original V_{SD} (V_{DO}). C_{LOAD} recharges, increasing V_{OUT} until the Δv_e is eliminated [10, 11, 12].

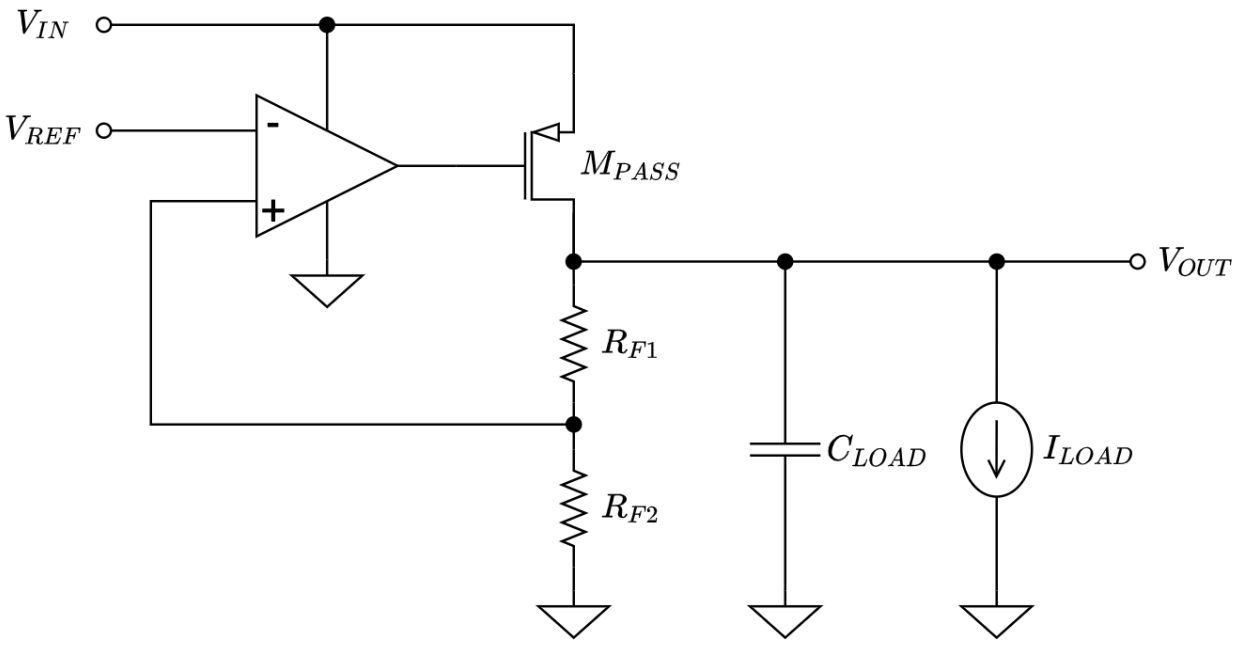

Figure 2.1: OTA error amplifier with PMOS pass device general LDO topology [9, 11]

Decreasing I_{LOAD} causes the excess current from M_{PASS} to add charge to C_{LOAD}, increasing V_{OUT} and driving M_{PASS} towards the linear operation region. This creates a Δv_e at the OTA input, lowering V_{SG} and allowing the new I_{LOAD} to be met by the original V_{SD}. C_{LOAD} discharges until the new I_{LOAD} is met and the Δv_e is eliminated [10, 11, 12].

The topology shown in Figure 2.1 shows a resistive divider to raise the output voltage above the reference voltage (V_{REF}). Removing these resistors for a non-inverting negative feedback configuration allows V_{OUT} to equal the V_{REF} [10, 11, 12].

2.1.2 Compensation

A common approach to ensuring the stability of an LDO is by placing a large C_{LOAD} at V_{OUT} to achieve the desired phase margin ($P.M.$). This compensation technique comes at the expense of a large off-chip capacitor and a reduced loop bandwidth, as the dominant pole is located at V_{OUT}. Fortunately, the topology shown in Figure 2.1 allows for internal frequency compensation, such as the Miller compensation technique [10, 11, 12].

With an internal frequency compensation approach, the node at the output of the OTA is designed to be the dominant pole of the LDO. Therefore, the dominant pole can be set with an added on-chip Miller capacitance (C_{Miller}) between the gate and drain of M_{PASS}. While on-chip capacitors usually take up a large chip area, the additional area required for C_{Miller} is negligible compared to that of an off-chip capacitor [10, 11, 12].

One challenge with internal frequency compensation is that the dominant pole is dependent on the terminal voltage gain (A_{vt}) of M_{PASS}, which is a function of I_{LOAD}. The input capacitance (C_{IN}) of M_{PASS} sets the dominant pole location and is given by Equation (2.1). As I_{LOAD} is variable, the $P.M.$ of the LDO (i.e., stability) is also variable. Therefore, the frequency compensation for the LDO must be designed to ensure stability under the extreme conditions of I_{LOAD}. When C_{Miller} is added to the circuit, another challenge to contend with is the right-half plane (RHP) zero created by the capacitor. A nulling resistor (R_{Null}) can be used in series with C_{Miller} to eliminate or move the zero to the left-half plane (LHP) [10, 11, 12].

$$C_{IN,PASS} = (C_{Miller} + C_{GD,PASS})(1 - A_{vt,PASS}) \tag{2.1}$$

2.1.3 Performance Metrics & Other Design Considerations

Static Metrics

The upper limit of V_{IN} is limited by the process, and the lower limit is limited by the requirements for keeping the OTA and M_{PASS} properly biased. The upper limit of V_{OUT} is limited by the $V_{SD_{SAT}}$ of M_{PASS}. The lower limit of V_{OUT} is limited by the lower limit of the OTA's input common-mode range (ICMR) or the system's power requirements. A larger than minimum V_{DO} corresponds to a lower power conversion efficiency (PCE) of the LDO and, therefore, a higher quiescent current (I_Q) [9, 10, 12].

The implication of the relationship between the upper limit of V_{OUT} and $V_{SD_{SAT}}$ is that the minimum V_{DO} is $V_{SD_{SAT}}$ and is dependent on I_{LOAD} and the size of M_{PASS}. At the maximum I_{LOAD}, M_{PASS} must be sized to source the required load without exceeding the desired V_{DO}. When the LDO is operating at a reduced I_{LOAD}, M_{PASS} will inherently stay in saturation, but the PCE will decrease. Therefore, when sizing M_{PASS}, the desired V_{DO}, I_{LOAD} range, I_Q, and active area must all be carefully considered [9, 10, 12].

Transient Metrics

When I_{LOAD} is changed, an undershoot or overshoot voltage (ΔV_{OUT}) occurs. This ΔV_{OUT} is a function of slew rate, loop bandwidth, $C_{GD,PASS}$, I_Q, and equivalent series resistance (ESR). Large slew rate and loop bandwidth correspond to a small ΔV_{OUT}. Large $C_{GD,PASS}$ and I_Q correspond to a larger ΔV_{OUT}. Thus, to minimize ΔV_{OUT}, a trade-off analysis is required for performance metric optimization [12].

After the ΔV_{OUT} has reached its maximum, the signal will settle to V_{OUT} in time T_{SETTLE}. T_{SETTLE} is a function of the slew rate, $P.M.$, bandwidth, and ESR. Higher slew rate, $P.M.$, bandwidth, or ESR correspond to a smaller T_{SETTLE}. For T_{SETTLE}, ESR is the only negative trade-off and is a minor contributor compared to the other factors. Therefore, there is justification to minimize ESR while designing for minimum T_{SETTLE} [12].

Thus, to minimize ΔV_{OUT}, a trade-off analysis is required for performance metric optimization [12].

Figures of Merit

There are two figures of merit (FOMs), FOM_1 and FOM_2, commonly used to evaluate LDOs, as shown in Equations (2.2) and (2.3) below. FOM_1 was developed by Peter Hazucha as a way to compare LDOs designed for different ΔV_{OUT} and is an indication of the LDO's speed. In FOM_1, C_{OUT} represents total capacitance, regardless of whether the capacitor is on or off-chip. It does not account for parasitic capacitances, such as from a pass device or a MOSCAP [13]. FOM_2 was developed by Jianping Guo to account for the time it takes for the load to change and is also an indication of speed [14]. FOM_1 is generally reported in femtoseconds or picoseconds, and FOM_2 is generally reported in volts or millivolts. For both FOMs, a smaller value indicates better performance.

$$FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \tag{2.2}$$

$$FOM_2 = \left(\frac{\Delta t_{edge}}{1\,\text{ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right) \tag{2.3}$$

2.2 The Output Capacitor-less, Ringamp-Assisted, Analog CMOS LDO

In Sangid's dissertation, he observed that digital-based LDOs (DLDOs) typically outperform analog-based LDOs (ALDOs) in scalability and chip area, but underperform in noise contribution and precision. With respect to the FOMs, ALDOs generally outperform DLDOs in FOM_1, while the opposite is true for FOM_2. RLDOs have not performed competitively with state-of-the-art DLDOs or ALDOs. The purpose of RLDOE is to provide an RLDO solution that improves the state-of-the-art for RLDOs and is competitive with DLDO and ALDO states-of-the-art. Sangid's work leverages RLDOs as a means for an LDO with "high precision, high power supply rejection (PSR), high current efficiency, dynamic voltage scaling (DVS), and process technology node scalability" [9].

Sangid accomplished this by creating an LDO with two independent loops as shown in Figure 2.2. This multi-loop LDO leverages the strengths of each loop's topology to mitigate

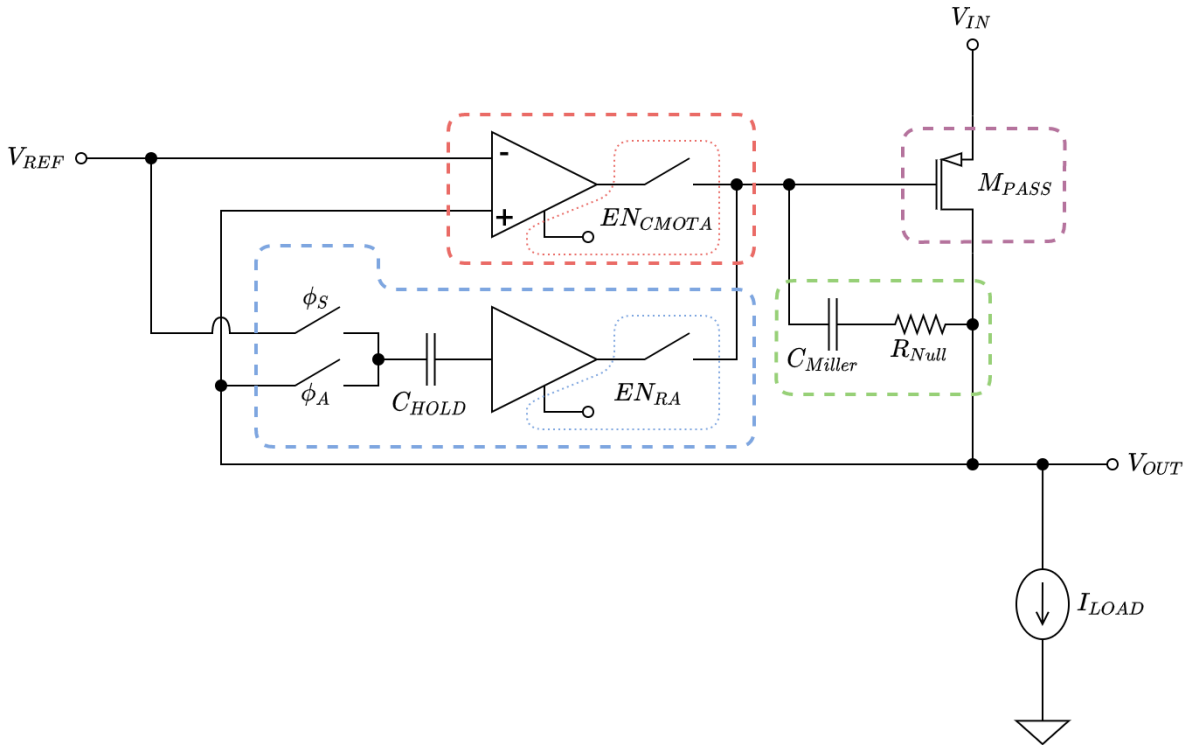

Figure 2.2: Output Capacitor-less, Ringamp-Assisted, Analog CMOS LDO block diagram [9]

the weaknesses of the other. The first loop is a high-efficiency loop that uses a current mirror operational transconductance amplifier (CMOTA) as its error amplifier. The second loop is a high-performance loop and uses a two-stage ringamp as its error amplifier. Both loops share a common pass device [9].

2.2.1 High Efficiency (CMOTA LDO) Loop

The CMOTA LDO loop, shown in Figure 2.3, is the primary loop for this LDO and is active when loads are at a steady state or when load changes are slow. This loop takes advantage of the minimally low I_Q (approximately 180 times lower than the RLDO loop), achieved by biasing the CMOTA in weak inversion. Another design advantage of the CMOTA is that the only high impedance node in the error amplifier is at the drains of M_{P4} and M_{N4} (*i.e.,* at the output of the CMOTA). This simplifies the stability design for this LDO loop, as the CMOTA is essentially a single-pole amplifier, and the pole is ideally located within the circuit for an internal frequency compensation approach [9].

2.2.2 High Performance (RLDO LDO) Loop

The RLDO loop, shown in Figure 2.4, is the secondary loop for this LDO and is only enabled during fast transient events. This loop takes advantage of the high loop bandwidth, loop gain, and slew rate of the RLDO for fast and accurate transient resolutions. After the transients are resolved, the RLDO is disabled, and the CMOTA LDO loop is re-enabled. It is worth noting that since the I_Q of the CMOTA is negligible, the CMOTA can be left on during fast transients for additional error correction [9].

Ringamp LDO Operation

During the sample phase (ϕ_S and ϕ_{AZ} switches are closed), the first-stage inverter is driven to its switching point (V_M) while V_{REF} charges the hold capacitor (C_{HOLD}) to V_{HOLD}, per Equation (2.4). Note that during the sample period, the feedback loop is broken, meaning that the LDO is unregulated. Therefore, the sample period should be as short as possible. Choosing the sample period is a relatively straightforward process by finding

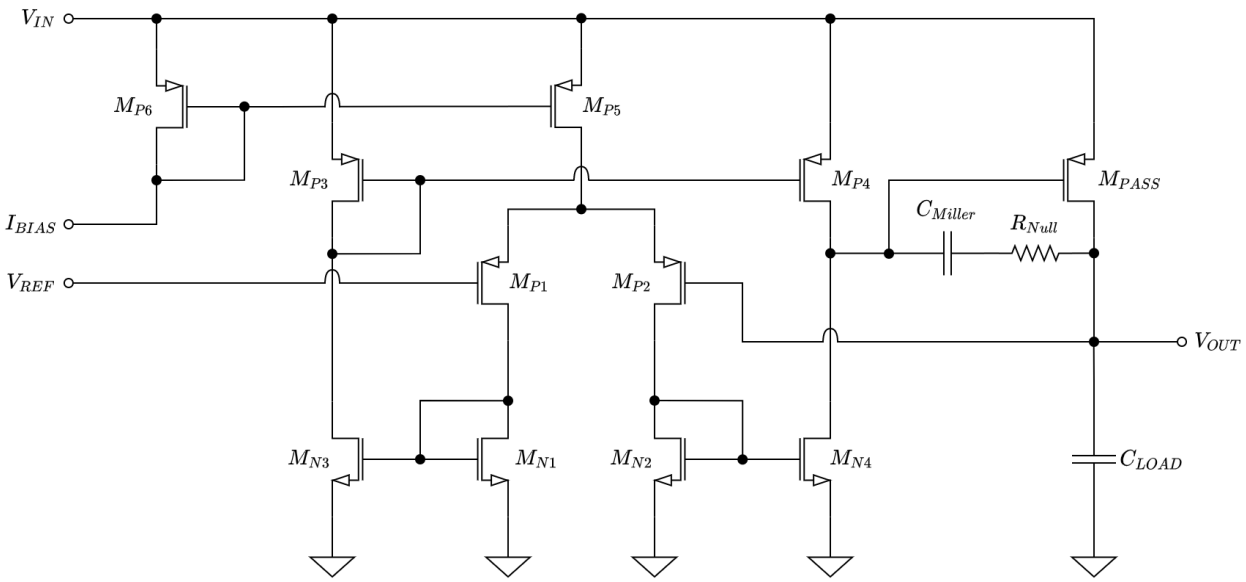

Figure 2.3: CMOTA LDO Loop simplified schematic [9]

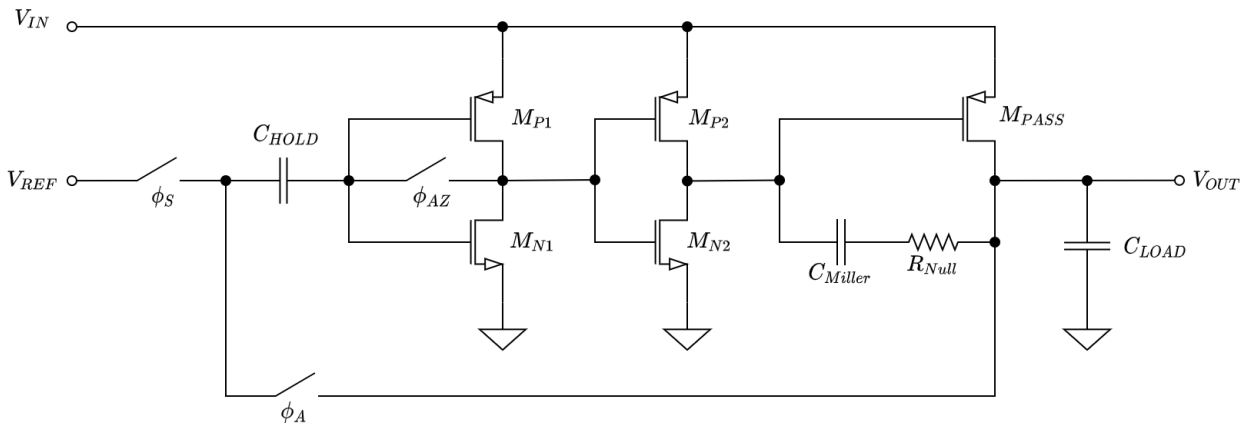

Figure 2.4: Ringamp LDO loop simplified schematic [9]

the time constant associated with C_{HOLD} (τ_{HOLD}) and then setting the sample period to at least 5 times τ_{HOLD}. The sample period should be long enough to charge C_{HOLD} to V_{HOLD}, but no longer. It is critical that the ratio of τ_{HOLD} to the time constant associated with M_{PASS} (τ_{PASS}) be as small as possible because ΔV_{OUT} during the sampling phase is directly proportional to this ratio [9].

$$V_{HOLD} = V_{REF} - V_{AZ} \tag{2.4}$$

During the amplify phase (ϕ_A switch is closed), C_{HOLD} is no longer connected to V_{REF} and is now connected to V_{OUT}. As I_{LOAD} changes, V_{OUT} changes due to the change of charge on C_{LOAD}. V_{HOLD} is maintained across C_{HOLD}, therefore the gate voltage of the first stage inverter moves in tandem with V_{OUT}. The ringamp error amplifier adjusts the drive strength to M_{PASS} to adjust for the change in I_{LOAD} until V_{OUT} is equal to V_{REF}. An important design note is that C_{HOLD} is both the input capacitor and the feedback capacitor in this topology, so matching is not a consideration [9].

2.2.3 Output Capacitor-less Stability

In Hershberg's original ringamp design (Figure 1.1), capacitors C_2 and C_3 are used to embed systematic offsets within the amplifier. These offsets are used to deadzone bias the output stage so that it only slightly conducts unless V_{OUT} is changing. Reducing the I_Q of the output stage allows the output pole location to decrease far below the other pole locations within the system to obtain stability [8]. For the RLDOE, to set the location of the dominant pole, C_{Miller} is added in parallel with $C_{GD,PASS}$. As mentioned in Section 2.1.2, implementing C_{Miller} creates an RHP zero. RHP zeros attenuate the like left half plane (LHP) zeros but have a phase response like LHP poles. A poorly located RHP zero can have devastating impacts on system stability. To compensate, R_{Null} is implemented to push the RHP zero into the LHP. The value of R_{Null} is chosen based on Equation (2.5) so that the LHP zero would most optimize the frequency response to maximize the P.M. of the LDO [9].

$$z_{Miller} \approx \begin{cases} +\frac{g_{mPass}}{C_{gd}+C_{Miller}} & \text{if } R_{Null} = 0; \\ -\frac{1}{(C_{gd}+C_{Miller})\left(\frac{1}{g_{mPass}}-R_{Null}\right)} & \text{if } R_{Null} > 0; \\ -\frac{g_{mPass}}{R_{Null}(C_{gd}+C_{Miller})} & \text{if } R_{Null} \gg {}^{1}/_{g_{mPass}}. \end{cases} \tag{2.5}$$

Another complexity of this LDO is that it has two LDO loops. To ensure the bandwidth requirements of the RLDO loop are met and that both loops have stability over the designed I_{LOAD} range, a nested Miller compensation (NMC) technique is implemented and split between the two LDO loops as shown in Figure 2.5. The output of the ringamp error amplifier is inherently dominant, so only a small C_{Miller} is required to ensure stability, meaning higher bandwidth. The output of the CMOTA requires a larger capacitance and uses both Miller networks in parallel. The CMOTA LDO loop is not intended for high-bandwidth applications, so the stability consideration is the primary design factor [9].

It should be noted that with the split Miller technique, the CMOTA error amplifier always has a signal path to V_{OUT}. To overcome this, R'_{Null} is chosen to be large for current limiting. When the CMOTA LDO loop and both Miller networks are active, the effective nulling resistance is $R_{Null}||R'_{Null}$, which is dominated by R_{Null}. Therefore, R'_{Null} is maximally large. The limitations of R'_{Null} are area and parasitic effects on LDO performance [9].

2.2.4 Pseudo-Differential Switch Driver

The pseudo-differential switch driver (PDSD), shown in Figure 2.6, takes a clock signal and generates two complementary overlapping clock signals. As the input to the PDSD changes state, the two complementary outputs simultaneously change states. This circuit enables the use of a single capacitor for the sampling and feedback capacitors of the RLDO loop. This circuit also acts as an output buffer for the clock signal, as the output is essentially an inverter [9, 15]. For optimum performance, the PDSD is designed so that the complementary signals overlap as close to $\frac{V_{DD}}{2}$ as possible. To ensure the PDSD does not introduce fast transients

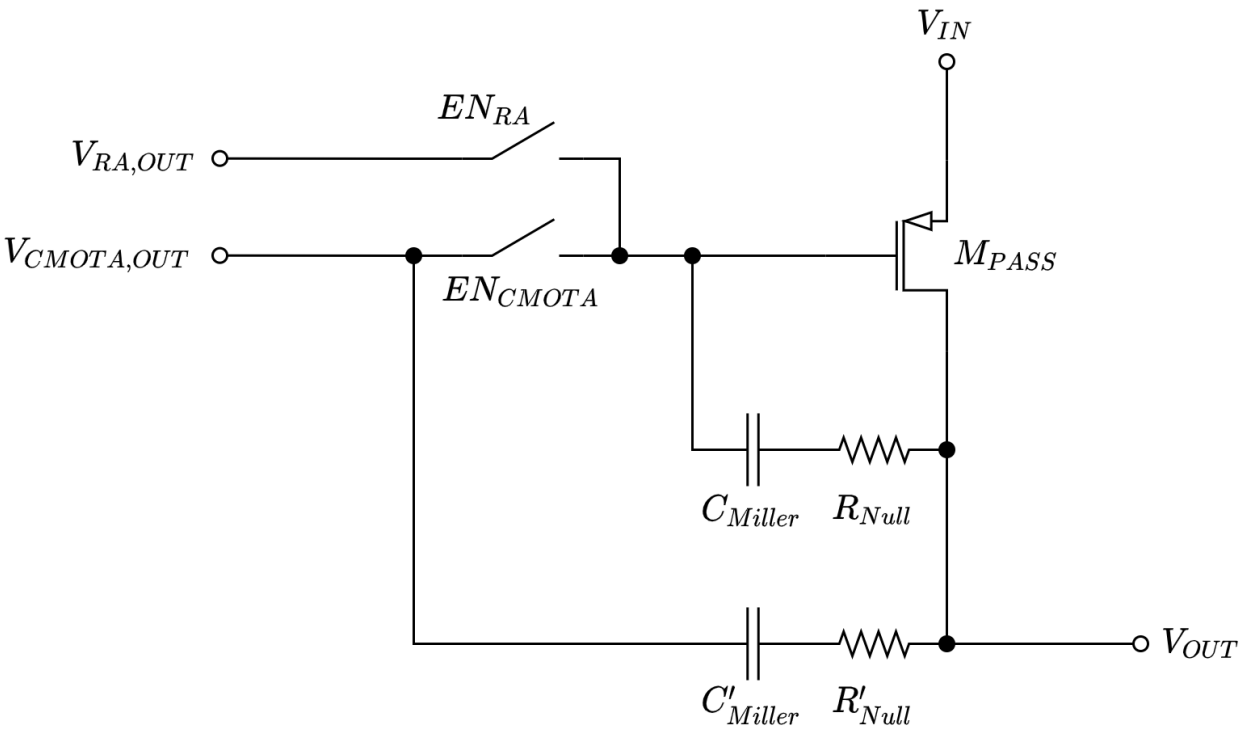

Figure 2.5: Split-Miller compensation technique for 180 nm RLDOE [9]

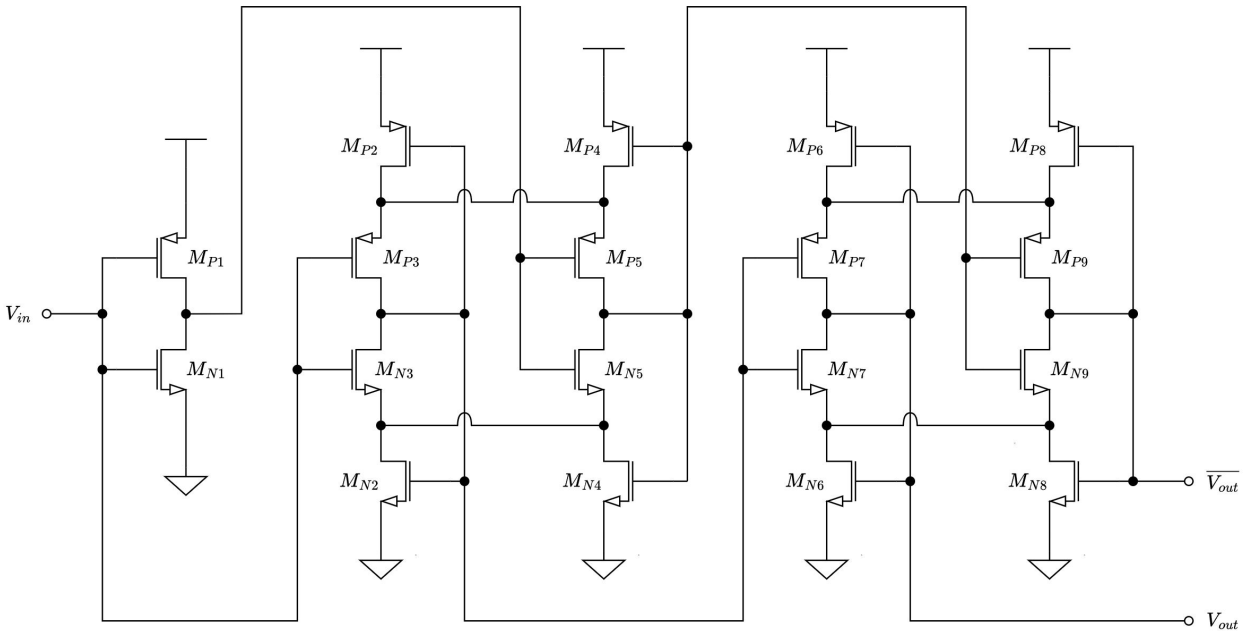

Figure 2.6: Pseudo-Differential Switch Driver schematic [9, 15]

into the signal through clock feed-through, a non-minimum L is used to slow the rising and falling edges of the output signal [9].

2.2.5 LDO Performance Comparisons

Tables 2.1 and 2.2, reported in [9], show the performance comparisons of the RLDOE with all known RLDOs and state-of-the-art ALDOs and DLDOs, respectively. As stated earlier in this section, the purpose of RLDOE is to make an LDO that performs well with respect to both FOMs. To validate this claim, Sangid developed the FOM graph shown in Figure 2.7. This log-log graph plots the inverse of an LDO's FOM_1 result along the x-axis and plots the inverse of its FOM_2 result along the y-axis. This FOM comparison plot makes it easy to compare LDO performances. The leading FOM_1-performing LDOs are located towards the right end of the graph, and the leading FOM_2-performing LDOs are located closer to the top of the graph [9].

As can be seen from Figure 2.7, the performance of the RLDOE exceeds the leading ALDO's performance with respect to FOM_2 and exceeds the leading DLDO's performance with respect to FOM_1 [9]. Additionally, this LDO's performance is comparable to the leading ALDO performances with respect to FOM_1, and it is reasonably competitive with the leading DLDO performances with respect to FOM_2. It should also be noted that the RLDOE is the highest-performing RLDO with respect to either FOM. Given the fact that Sangid's RLDOE is approaching the corner of the performance edge boundary, his claim of "bridging the gap" between ALDOs and DLDOs appears to be well-founded [9].

2.3 The Ring Amplifier Design Guide

Sangid's ring amplifier design guide provides the ringamp designer with a structured, methodical approach for designing the overdriven Class AB output stage ringamp topology, as shown in Figure 2.8, and the underdriven Class B output stage ringamp topology, as shown in Figure 2.9. The design guide is divided into three sections: pre-design tasks, design method, and final design considerations [9].

Table 2.1: Comparison of all known RLDOs vs. Sangid's Dual-Loop RLDO as reported in [9]

Parameters	**Unit**	**Yang and Mok [16]**	**Xiao *et al.* [17]**	**Park *et al.* [18]**	**Sangid [9]**
Year		2017	2019	2020	2022
Technology	[nm]	65	180	40	180
$\mathbf{V_{IN}}$	[V]	0.2-0.6	1.08-1.65	0.4-1.2	0.9-1.8
$\mathbf{V_{OUT}}$	[V]	0.05-0.55	1	0.2-1.18	0.6-1.7
$\mathbf{I_{OUT}}$	[mA]	0.1-50	40	400	200
$\mathbf{I_Q}$	[µA]	0.41-32	6.5	4.4-1280	0.354-72
$\mathbf{V_{DO}}$	[mV]	20	90	50	100
$\mathbf{C_{TOTAL}}$	[pF]	40	50	90	23.3
$\mathbf{\Delta t_{edge}}$	[ns]	10,000-150	100	10	15
$\mathbf{\Delta V_{OUT}}$	[mV]	133.9	46-163	78-45	146
$\mathbf{T_{SETTLE}}$	[ns]		234-700	500-25	125
PSR at 100 kHz	[dB]	20	~ 18	~ 30	42
$\mathbf{FOM_1}$ *	[fs]	228,300-1700	1505-8	28,600-55	0.0301
$\mathbf{FOM_2}$ †	[V]	0.165	0.748	0.00858	0.00388
Active Area	[mm^2]	1.379	0.1	0.12	0.068

* $FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right)$ [13] † $FOM_2 = \left(\frac{\Delta t_{edge}}{1\,\text{ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right)$ [14]

Table 2.2: Comparison of State-of-the-Art LDOs vs. Sangid's Dual-Loop RLDO as reported in [9]

Parameters	**Unit**	**Huang *et al.*** [19]	**Huang *et al.*** [20]	**Ma *et al.*** [21]	**Zhao *et al.*** [22]	**Han and Lee** [23]	**Sangid** [9]
Year		2016	2018	2020	2021	2021	2022
Technology	[nm]	65	65	28	65	180	180
Control		DLDO w/ Coarse-Fine-Tuning and Burst-Mode	Tri-Loop DLDO w/ Analog Assist	DLDO w/ NAND-based Analog Assist	Current-Controlled Oscillator	Active Capacitor	Analog Multi-loop w/ RLDOE
$\mathbf{V_{IN}}$	[V]	0.6-1.1	0.5-1	0.4-0.55	0.5-1.2	1.2-1.4	0.9-1.8
$\mathbf{V_{OUT}}$	[V]	0.4-1	0.45-0.95	0.35-0.5	0.45-1.15	1.0-1.2	0.6-1.7
$\mathbf{I_{OUT}}$	[mA]	100	10	40	50	80	200
$\mathbf{I_Q}$	[µA]	82	3.2	0.85	0.31-0.5	0.34	0.354-72
$\mathbf{V_{DO}}$	[mV]	100	50	50	50	200	100
$\mathbf{C_{TOTAL}}$	[pF]	1000	100	59	15	3	23.3
$\mathbf{\Delta t_{edge}}$	[ns]	20	1	0.1	15	100	15
$\mathbf{\Delta V_{OUT}}$	[mV]	55	105	113	150	120	146
$\mathbf{T_{SETTLE}}$	[ns]	700			300	110	125
PSR at 100 kHz	[dB]			~ 2		34	42
$\mathbf{FOM_1}$ *	[fs]	430	230	26	3	0.02	0.0301
$\mathbf{FOM_2}$ †	[V]	0.902	0.0336	0.00024	0.0225	0.051	0.00388
Active Area	[mm^2]	0.01	0.034	0.0134	0.118	0.04	0.068

* $FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right)$ [13]

† $FOM_2 = \left(\frac{\Delta t_{edge}}{1\,\text{ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right)$ [14]

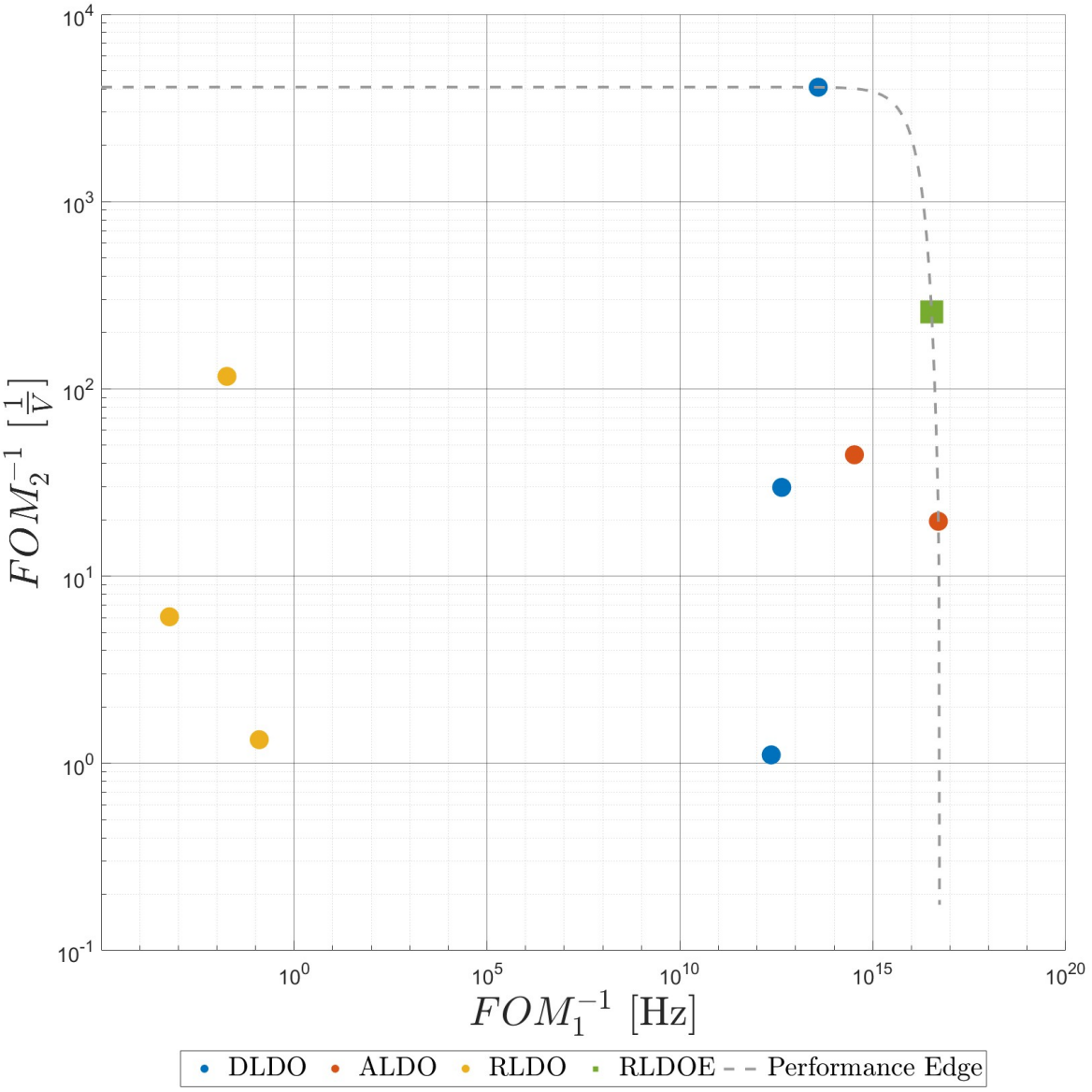

Figure 2.7: FOM comparison graph of Sangid's Dual-Loop RLDO, State-of-the-Art LDOs, and all known RLDOs [9]

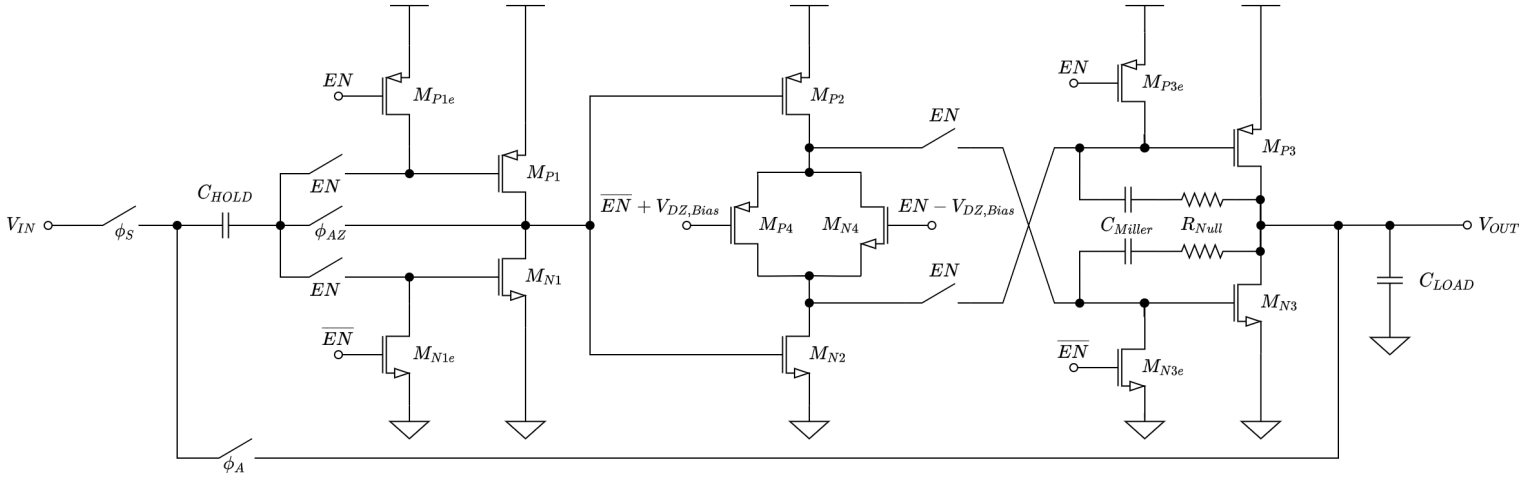

Figure 2.8: On-demand ringamp with over-driven Class AB output stage [9]

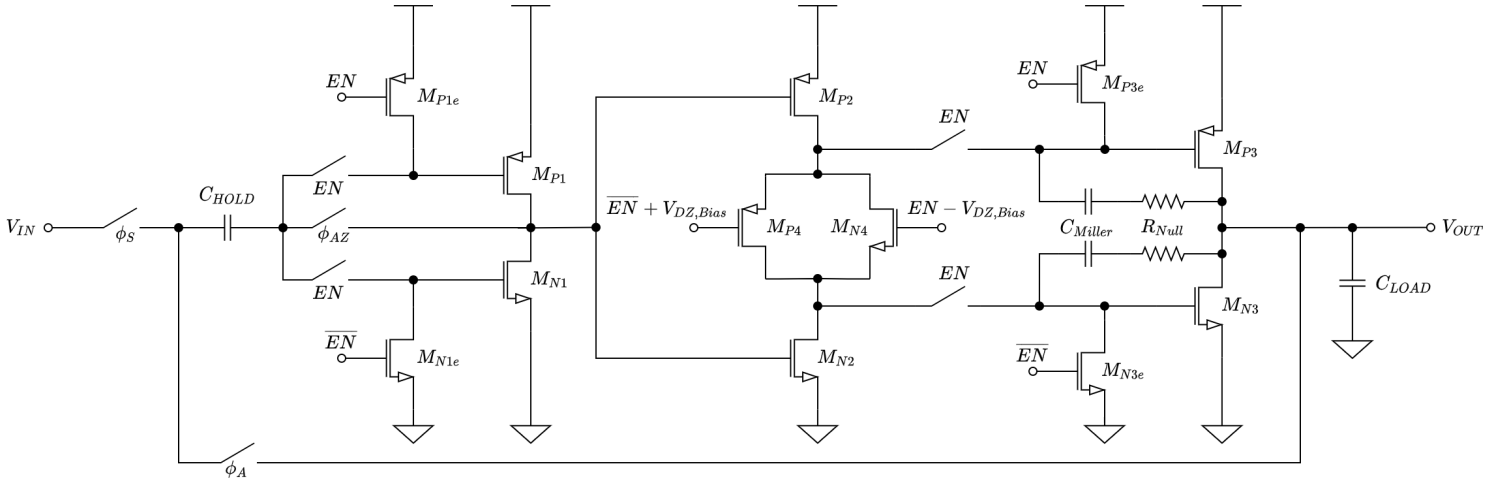

Figure 2.9: On-demand ringamp with under-driven Class B output stage [9]

The pre-design tasks involve the designer using the design automation script to create the ringamp's unit inverter that is tailored to the requirements of the designer's application. The designer begins by evaluating the amplifier's needs and determining the current budget, target gain, and target bandwidth. For ringamp designs, bandwidth typically takes precedence when designing the unit inverter since high bandwidth is inherently available in an inverter, and sacrificing it often offers little advantage [9].

Once the pre-design tasks are complete, the designer proceeds to work through the design method. An easy-to-follow flowchart is provided within the ringamp design guide, as shown in Figure 2.10. This flowchart offers general guidance for designing aspects such as gain, bandwidth, stability, and slew rate. The design guide also provides users with guidance on additional considerations, such as internal versus external frequency compensation, class B versus class AB output stages, and scaling between stages [9].

2.3.1 90 nm Unit Inverter Scaling Demonstration

This section presents a demonstration of the ringamp design assistance script for a standard 90 nm CMOS process. To use the script, IV curves are collected for the NMOS and PMOS devices. Maximizing loop bandwidth is the top priority, so L is set to the process minimum. Device widths are also set to the process minimum. The data is then organized into an Excel spreadsheet following the design guide's instructions. After entering user input into the MATLAB® script, the code is executed [9].

Design Assistance Script Results & Evaluation

The results from running the design assistance script and the subsequent evaluation are provided in Table 2.3. The script results are assumed to not be reasonable since the width of the PMOS device (W_P) is approximately 17 times larger than the width of the NMOS (W_N). To validate this assumption, two simulations are performed. The first simulation sweeps the gate voltage to generate the inverter transfer curve at the output, allowing V_M to be determined. The second simulation fixes the DC voltage at the gate to the simulated V_M and then an AC sweep is performed. This provides the A_{vt}, cutoff frequency (f_{-3dB}), and

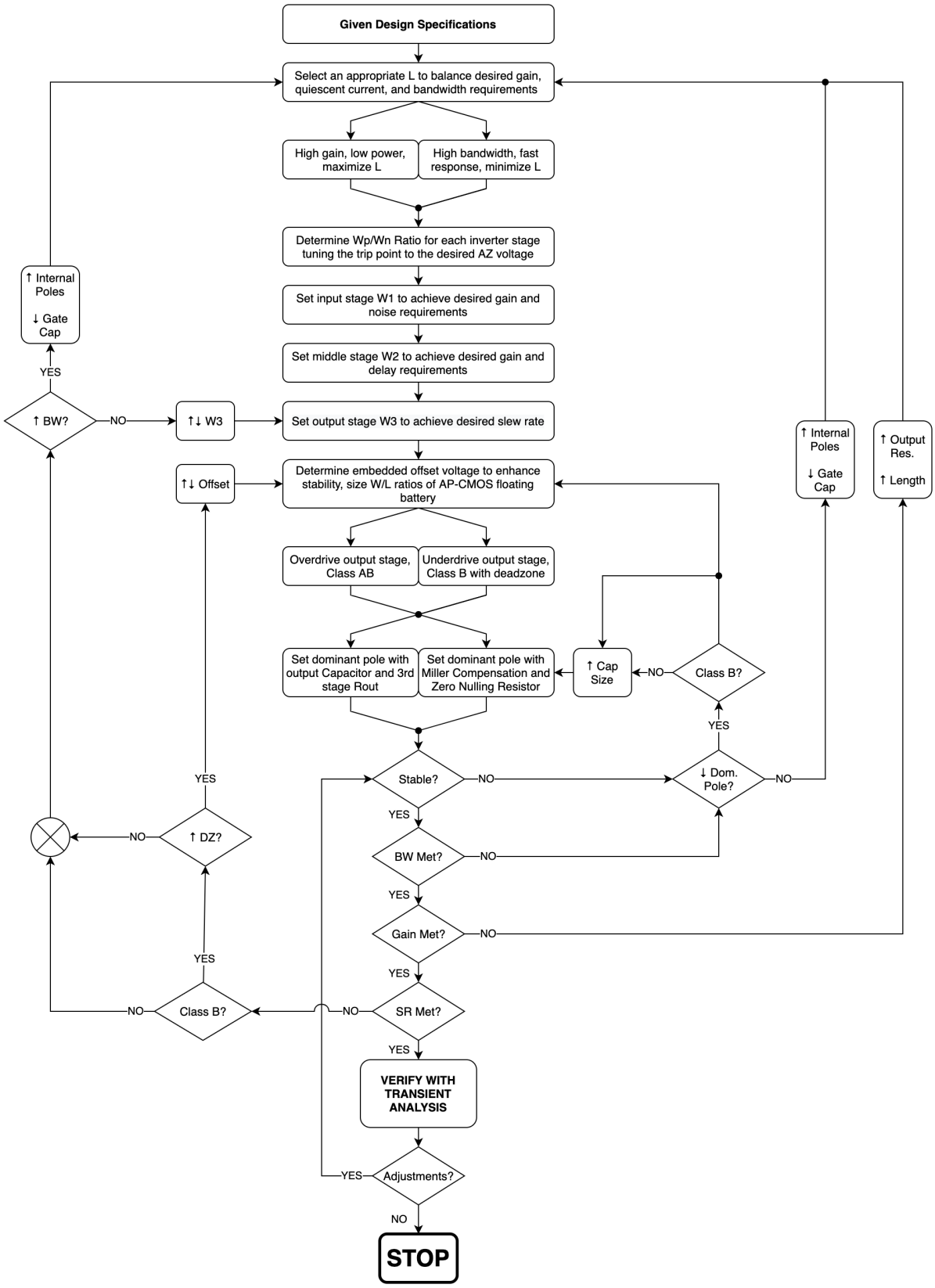

Figure 2.10: Design flowchart for class B and AB ring amplifiers [9]

Table 2.3: Design assistance script results and evaluations for a 90 nm CMOS process

Parameter	**Value**	**Unit**
W_N	W_{Min}	[nm]
W_P	$17.1(W_{Min})$	[nm]
L	L_{Min}	[nm]
V_M	723	[mV]
I_Q	14.0	[µA]
A_{vt}	20.3	[dB]
f_{-3dB}	1.41	[GHz]
UGF	15.8	[GHz]

unity gain frequency (UGF) for the inverter. While A_{vt}, f_{-3dB}, and UGF are all reasonable, though less than desired, the V_M for the inverter is far from the ideal mid-rail value. This will lead to decreased ICMR and linearity [9].

Based on these results and further investigation, it became apparent that this 90 nm CMOS process experiences an effect beyond the expected short channel effects (SCE) called the reverse short channel effect (RSCE). The RSCE impacts investigated in Section 2.4 explain why the design assistance script is unable to generate a reasonable inverter size for this 90 nm process.

2.4 Reverse Short Channel Effect

2.4.1 Halo Doping

Halo doping is a fabrication process implemented in some deep-submicron processes to mitigate short channel effects (SCE), primarily drain induced barrier lowering (DIBL). Figure 2.11 shows a comparison between a conventional NMOS structure and halo doped NMOS structures. The halo doped structures include a p^+ halo around the source and drain n^+ diffusion extensions. MOSFETs fabricated in a halo doped process experience RSCE, which causes the threshold voltages (V_{TH}) to decrease as the channel length (L) is increased, as illustrated in Figure 2.12.

Extreme variations in V_{TH} over L can imply additional variations in drain current (I_D), transconductance (g_m), and small signal output resistance (r_o) trends over L. The following four subsections compare the variations of V_{TH}, I_D, g_m, and r_o over L between the 180 nm CMOS process used in Sangid's original dual-loop ringamp-assisted LDO and the 90 nm CMOS process used in this work. Additional simulations provide a comparison of λ over V_{GS}. This provides critical insights into the challenges and benefits of designing in a halo-doped process with significant RSCE [24, 25].

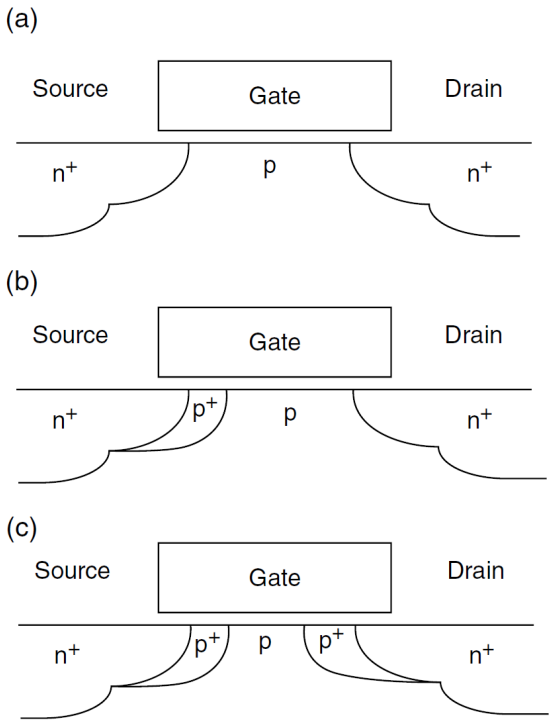

Figure 2.11: NMOS channel structures for (a) the conventional NMOS structure, (b) an NMOS structure with single-halo doping, and (c) an NMOS structure with double-halo doping [24]

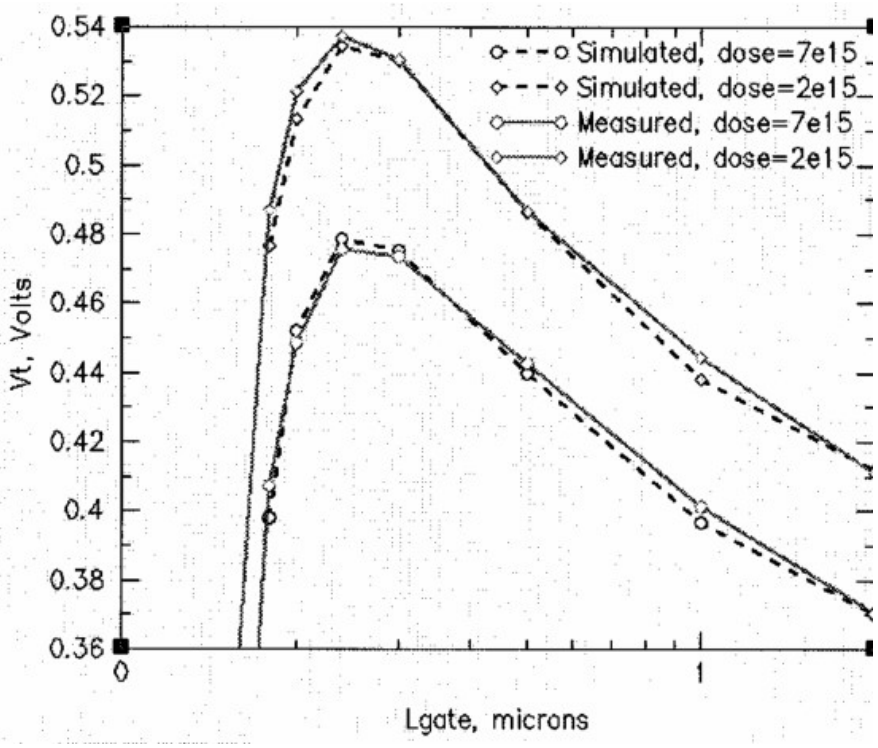

Figure 2.12: Example of V_{TH} vs. L in a process with RSCE [25]

2.4.2 Threshold Voltage Variation Over Length

Figure 2.13 shows the simulation results for V_{TH} vs. L in the 90 nm and 180 nm processes. The simulations cover a range from the minimum L to 20 times the minimum L. V_{TH} is normalized with respect to the ideal V_M for each process. V_{DS} and V_{GS} are set to $\frac{V_{DD}}{2}$, device widths are fixed to the process minimum, L is stepped as mentioned above, and V_{TH} is collected for each L step. L is plotted on a log scale to better highlight the results near the minimum L. This simulation test bench, shown in Figure 2.14, is used to collect data for all remaining simulations in this section.

The trends show that both processes experience RSCE, with threshold voltages decreasing as L increases. The RSCE in the 90 nm process is much more pronounced than in the 180 nm process, particularly for the NMOS device. At minimum L, V_{TH} is much closer to V_M in the 90 nm process compared to the 180 nm process. At maximum L, V_{TH} dropped significantly in the 90 nm process. Comparatively, V_{TH} for the 180 nm process is reasonably consistent over L. With V_{TH} so close to V_M at minimum L for the 90 nm NMOS device, the device is likely in moderate or weak inversion. Therefore, it is easy to see how sizing an inverter in this process for a symmetrical and linear amplification region is not intuitive.

Despite these challenges, there are some promising implications of RSCE. The general inverter transfer curve is shown in Figure 2.15. Regions 1, 2, and 3 on this plot represent where only the PMOS transistor ($M2$) is on, where both transistors are on, and where only the NMOS transistor ($M1$) is on, respectively. These regions are largely dictated by the threshold voltages of the transistors. As V_{TH} approaches $\frac{V_{DD}}{2}$, the A_{vt}, given by $\frac{\partial V_{in}}{\partial V_{out}}$, increases [26]. Since ringamp inverters are typically designed with a minimum L to maximize bandwidth, the improved A_{vt} becomes a possible benefit of designing in an RSCE process. Other implications are discussed in the succeeding subsections.

2.4.3 Drain Current Variation Over Length

The design assistance script is modeled on the square law equations, as shown in Equations (2.6) and (2.7). For designing circuits using this model, increasing L provides a means for decreasing the design current. Conversely, since ringamp inverters are generally

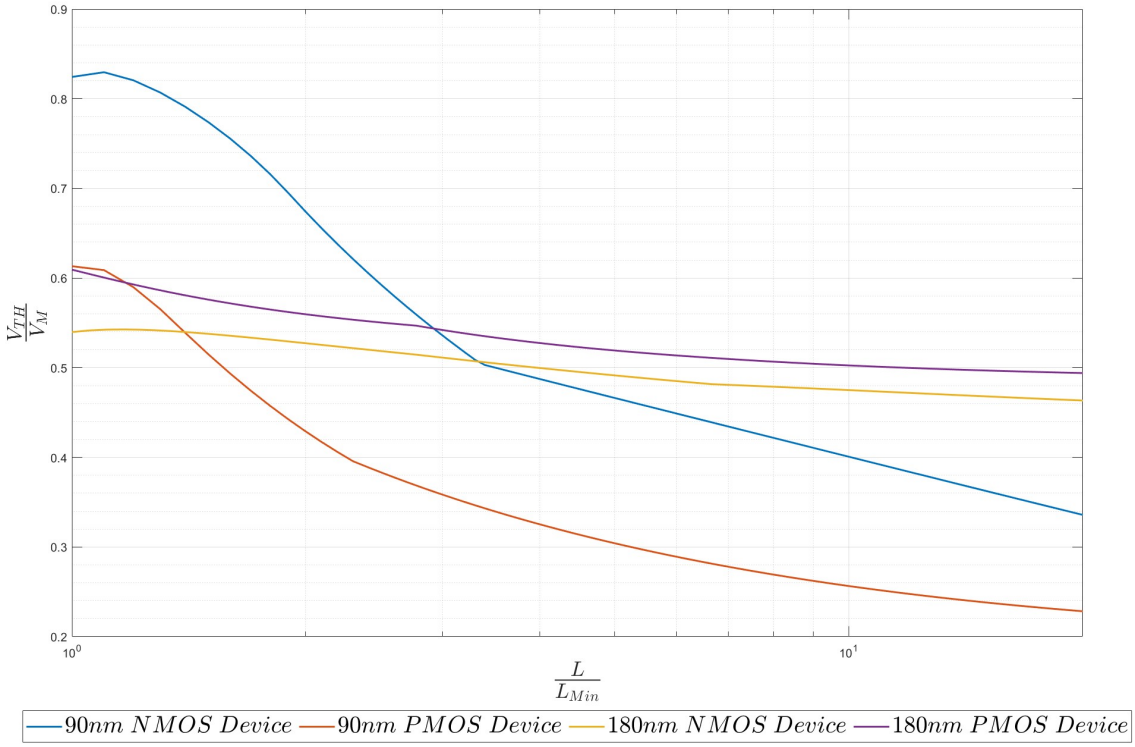

Figure 2.13: Simulation results if V_{TH} vs. L for 90 nm and 180 nm processes

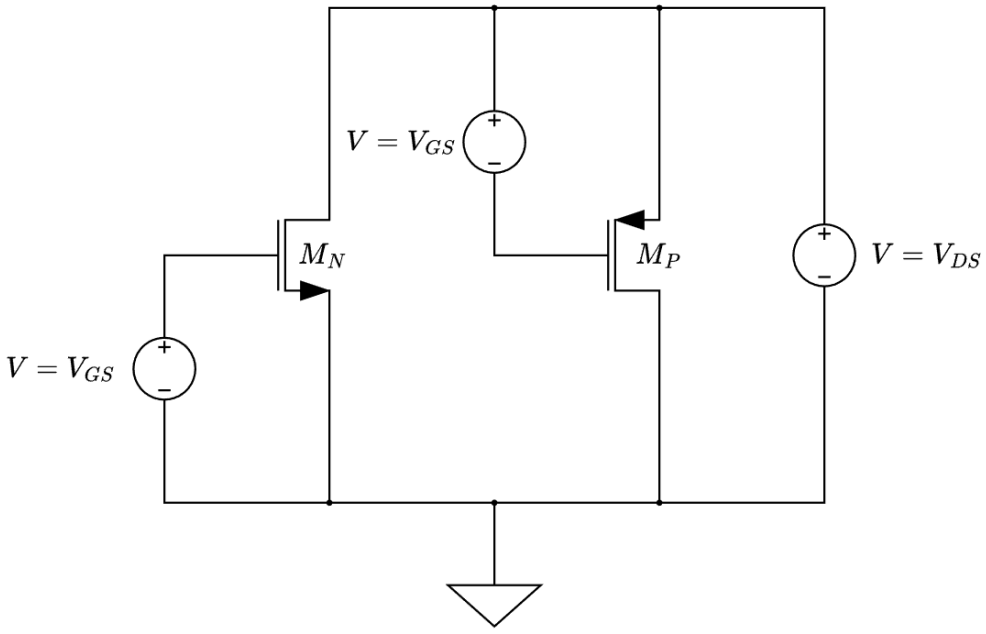

Figure 2.14: The I-V curve simulation test bench

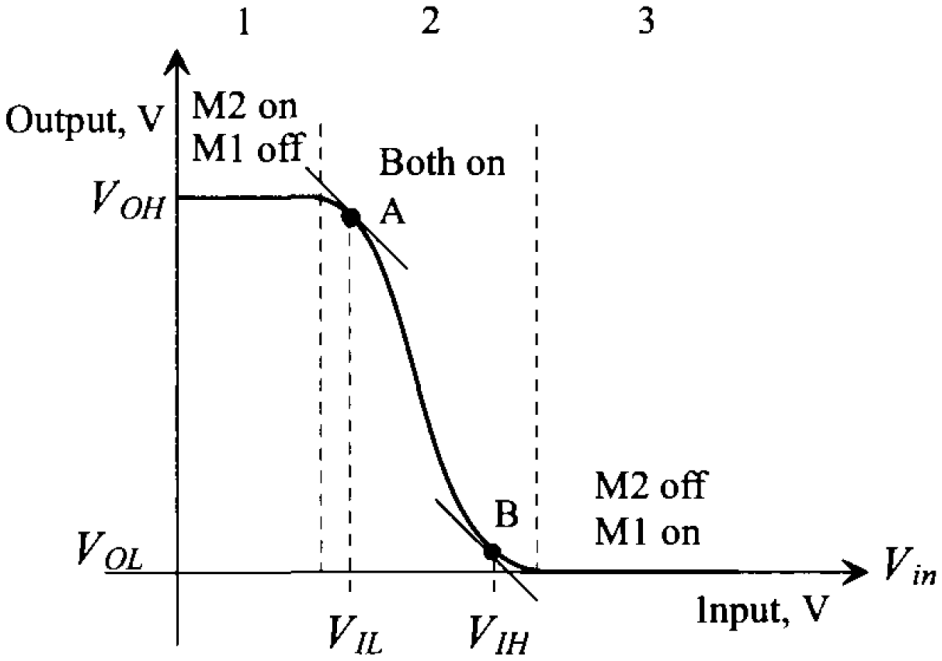

Figure 2.15: The general CMOS inverter transfer curve [26]

designed with minimum L, the inverters typically have large I_Q. Considering the 90 nm process V_{TH} plot from Figure 2.13, it is reasonable to expect that this may not necessarily be the case in processes with extreme RSCE near the minimum L.

Substituting V_M for V_{GS} and V_{DS}, as in Equations (2.8) and (2.9), it becomes clear that, at near minimum L but after V_{TH} peaks, an increase in L can result in a decrease in V_{TH} so large that the $(V_M - V_{TH})^2$ term (i.e., V_{DSat}^2) can dominate over the $\frac{1}{L}$ term. This is especially true if V_{DSat} is small at minimum L. This leaves a possibility for a region of L where an increase in L causes current to increase instead of decrease. However, a more important point to consider is that the square law equation assumes strong inversion-saturation. If V_{TH} is near $\frac{V_{DD}}{2}$ and V_M is approximately $\frac{V_{DD}}{2}$, then V_{DSAT} is approaching 0 V, which means the inverter is operating in moderate or weak inversion, as mentioned above, and the wrong model is being applied for the process [27].

$$I_D = K_n^{'} \frac{W}{2L} (V_{GS} - V_{TH_n})^2 [1 + \lambda_n V_{DS}] \tag{2.6}$$

$$I_D = K_p^{'} \frac{W}{2L} (V_{SG} - |V_{TH_p}|)^2 [1 + \lambda_p (V_{SD})] \tag{2.7}$$

$$I_D = K_n^{'} \frac{W_n}{2L} (V_M - V_{TH_n})^2 [1 + \lambda_n V_M] \tag{2.8}$$

$$I_D = K_p^{'} \frac{W_p}{2L} (V_M - |V_{TH_p}|)^2 [1 + \lambda_p V_M] \tag{2.9}$$

As a further demonstration of the impacts of designing in a process with significant RSCE, simulation results are provided below comparing the variation of I_D over L between the two processes. The results are shown in Figure 2.16. The 180 nm process simulation results appear to be close to the ideal plot one would assume based on the square law equation. The 90 nm process results are quite different, with the RSCE being more prominent in the NMOS device than in the PMOS device. This is similar to what is observed in the V_{TH} vs. L simulations. Instead of I_D decreasing with L, after an initial increase in L, I_D begins to increase before finally decreasing towards the minimum value. One major insight from

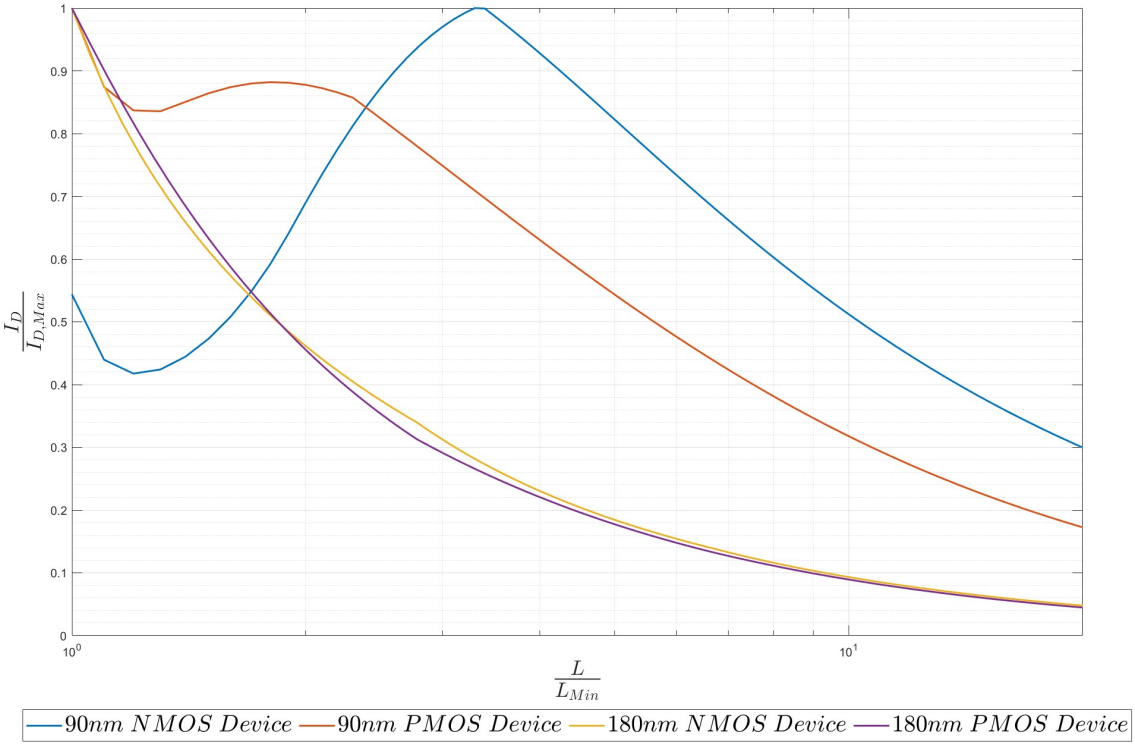

Figure 2.16: Simulation results of I_D vs. L for 90 nm and 180 nm processes

this plot is that L has to become more than 10 times the minimum before I_D decreases below the minima. This means that the minimum, or near-minimum, L corresponds to a near-minimum I_D. This simulation uses the same setup as described in Section 2.4.2 with the change that V_{DS} is set to V_{DD}.

2.4.4 Transconductance and Drain-Source Resistance Over Length

A final set of L variation demonstrations are provided by simulating the variation in g_m and r_o over L for the two processes. The results are shown in Figures 2.17 and 2.18. As with the previous simulations, the results for the 180 nm process align with square law expectations while the 90 nm process PMOS device shows moderate variation, and the 90 nm process NMOS device shows more extreme variation from the expected.

Looking at the 90 nm NMOS device, the trend of g_m is similar to I_D, but less extreme. This means that g_m is comparatively large for a long range of L. The PMOS device does not experience this same benefit, but the rate of g_m decline is much less extreme than for either 180 nm device. The trend of r_o also shows improvements at lower L, with the 90 nm NMOS device seeing a spike in r_o between the minimum and twice the minimum L.

2.4.5 Channel Length Modulation Variation over Inversion Length

DIBL causes V_{TH} to change with a dependence on V_{GS}. This makes the device easier to saturate at larger V_{GS} resulting in increased current. The $p+$ halo regions added around the $n+$ diffusion extensions ensure the device requires more V_{GS} to create a channel, therefore helping to mitigate DIBL. When thinking about halo doping in this way, the plot in Figure 2.12, the 90 nm plots in Figure 2.13, and RSCE becomes intuitive to understand. At minimum L, the halo doped region will have a large impact on V_{TH} as the ratio of the halo doped region to total L is large, so V_{TH} is naturally at a maximum. However, when L is increased, the consequences of the halo doped region are minimized because the ratio becomes small, so V_{TH} is naturally at a minimum [24, 25, 28].

However, a consequence of halo doping is that at small gate lengths, the pinch off region (X_D) is highly dependent on V_{DS} and now V_{GS}. When V_{GS} is small, the $p+$ region is not yet

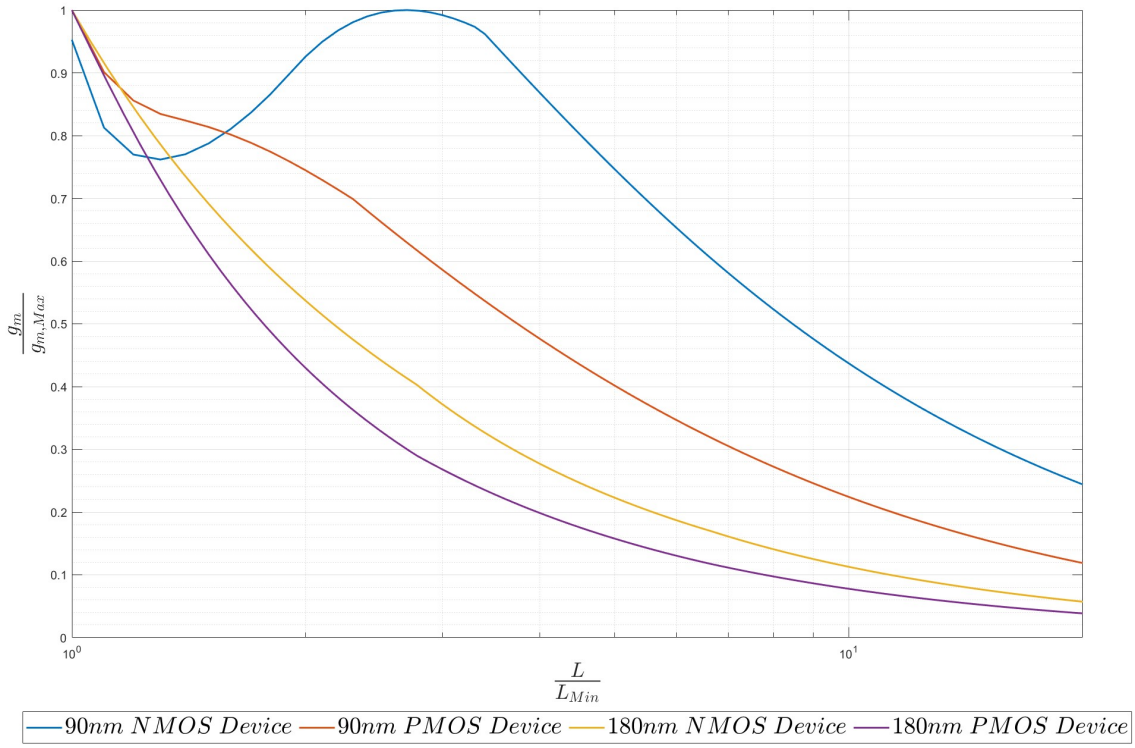

Figure 2.17: Simulation results of g_m vs. L for 90 nm and 180 nm processes

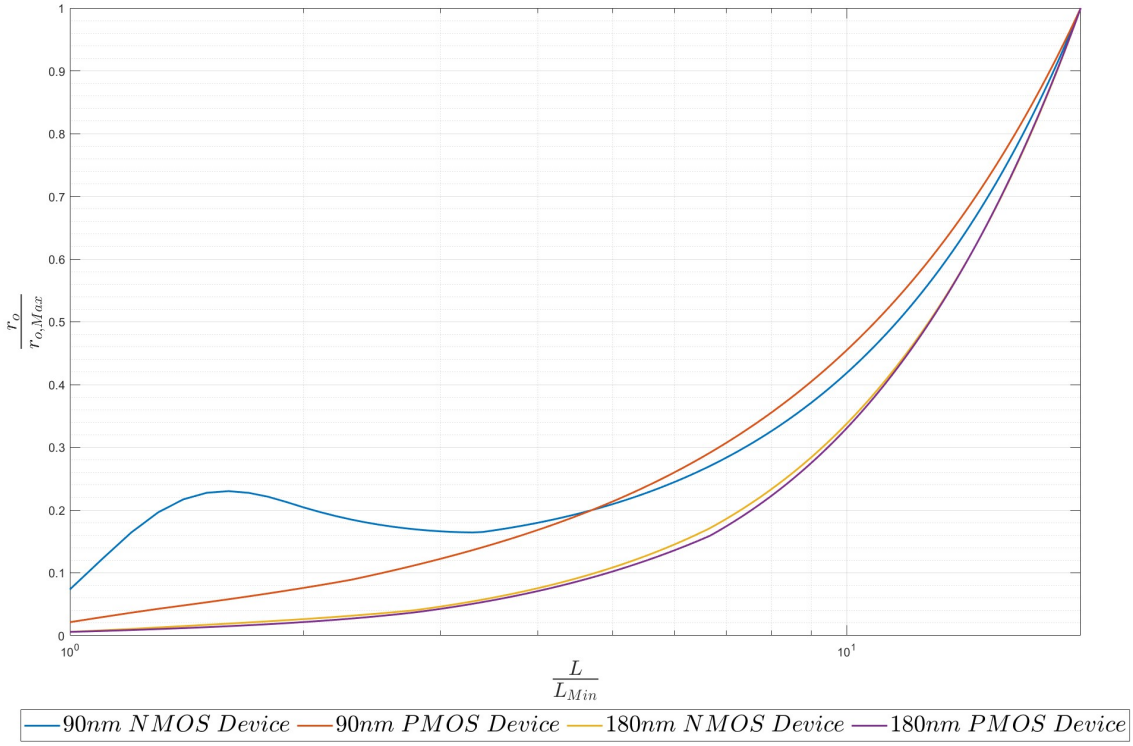

Figure 2.18: Simulation results of r_o vs. L for 90 nm and 180 nm processes

inverted and therefore contributes heavily to X_D making the effective channel length (L_{EFF}) small, as given by Equation (2.10). As V_{GS} increases, the $p+$ region begins to invert, and X_D decreases. Equation (2.11) shows that λ decreases as L_{EFF} increases and X_D decreases. Therefore, λ decreases as the level of inversion increases. A demonstration of this is shown in Figures 2.19 and 2.20, which shows the 90 nm and 180 nm processes λ and I_D plots versus V_{GS} for NMOS and PMOS devices, respectively. λ and I_D are normalized with respect to their minimum values and V_{GS} is normalized with respect to V_{DD}. This simulation uses the same setup as described in the previous section with the change that L is now fixed to the minimum and V_{GS} is swept [28, 27].

$$L_{EFF} = L - X_D \tag{2.10}$$

$$\lambda = \frac{1}{L_{EFF}} \frac{dX_d}{dv_{DS}} \tag{2.11}$$

I_D versus V_{GS} is provided on the plot for a comparison reference to a known parameter with a dependence on level of inversion. For the 90 nm process it can be observed that λ starts at a maximum value and begins to decrease as the inversion layer is forming. The 180 nm devices behave similarly, but do not have a peak λ at $V_{GS} = 0$. As observed in the Section 2.4.2, the 180 nm process devices experience a level of RSCE, however not as extreme as with the 90 nm process devices.

This leads to why the design assistance script does not provide reasonable values for the 90 nm demonstration. The script calculates λ for multiple steps of V_{GS} and takes the average value. This is the value of λ used for its sizing calculations. For small to moderate values of λ, this approximation is good enough, even with a moderate level of RSCE. However, if λ values are large, using the average value is likely to produce extreme errors between the simulation and the calculation. Additionally, with a strong RSCE presence, the average value of λ becomes heavily weighted towards the maximum value which amplifies the error.

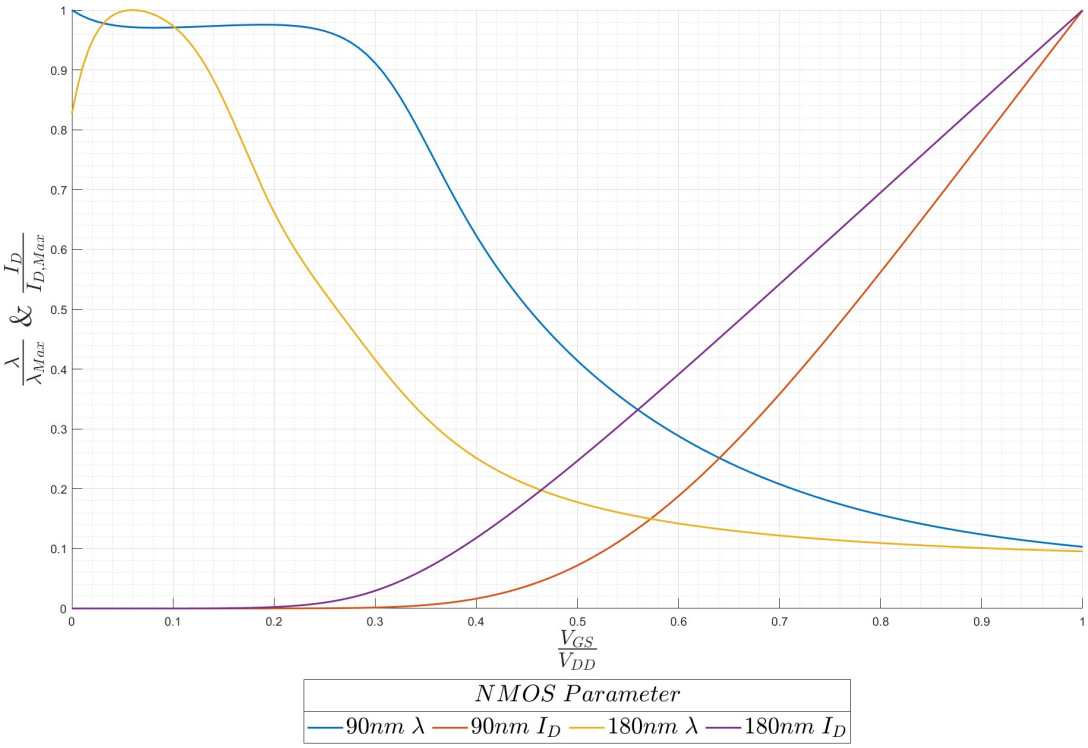

Figure 2.19: NMOS simulation results of λ and I_D vs. V_{SG} for 90 nm and 180 nm processes

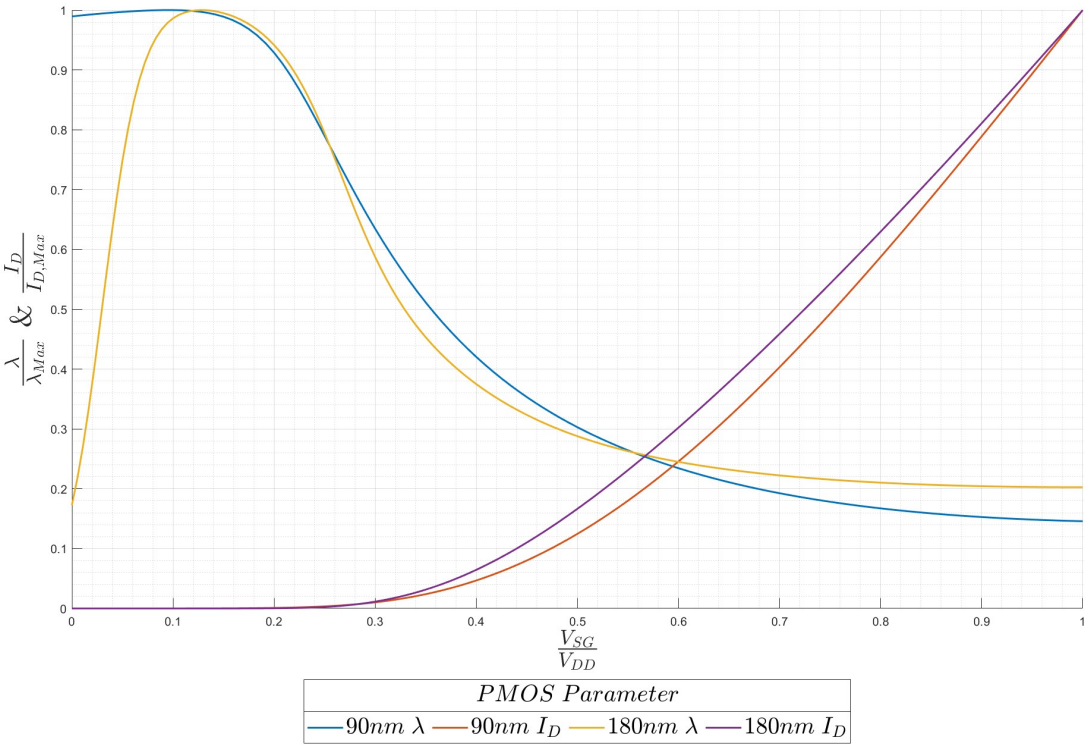

Figure 2.20: PMOS simulation results of λ and I_D vs. V_{SG} for 90 nm and 180 nm processes

2.4.6 RSCE impacts to the Ringamp Design Guide

The ringamp design guide and design assistance scripts provide a terrific resource for ringamp designers working in processes without significant RSCE and with low to moderate values for λ. Sangid provided a 65 nm simulation example, in his dissertation, supporting this point [9]. Despite this, modifications to the design guide and design assistance script are required for designing in processes with significant RSCE and/or large values for λ.

Chapter 3

90nm Ringamp LDO Design

This work is a case study of the scalability of ring amplifiers. In this study, a scaling demonstration is provided by scaling the RLDO loop of Sangid's RLDOE from a 180 nm CMOS process to a 90 nm CMOS process. The RLDOE's multi-loop functionality is not incorporated in this work. Limiting the scaling demonstration to the RLDO loop keeps the focus on ring amplifiers. As shown in Section 2.4, the impacts from RSCE made designing the 90 nm unit inverter not possible using only the ringamp design assistance script. Therefore, this chapter begins with a different design approach for the unit inverter. Subsequently, the designs for the transmission gates (T-Gate), PDSD, pass device, and stability are presented.

3.1 Unit Inverter Design

To design the unit inverter, highest considerations are given to f_{-3dB}, A_{vt}, and I_Q. As mentioned in Section 2.3, ringamp unit inverters, similar to their digital siblings, are designed with a minimum L to maximize speed. To maximize efficiency and performance metrics, a low I_Q amplifier is desirable. Additionally, to maximize loop gain and loop bandwidth of the LDO, it is desirable for A_{vt} and f_{-3dB} to be large. Therefore, a trade-off analysis is performed to determine the transistor's L and W sizes [10, 9, 7].

The trade-off analysis is initiated by inspection of the RSCE plots from Section 2.4. From this analysis, it becomes apparent that there is likely a "*sweet spot*" between the minimum and twice minimum L, where the NMOS I_D decreases to near its minimum value and its r_o

increases significantly. This narrows down design choices to a small range of L. The PMOS device sees a similar, but less extreme trend.

For inverters, a lower I_Q corresponds to reduced bandwidth due to an increase in output capacitance and r_o. So caution should be implemented when increasing the unit inverter's L. Since the Miller capacitance sets the LDO's dominant pole at the gate of the pass device (P_{ra}) and the pass device sets the next largest pole at the LDO's output (P_{out}), the f_{-3dB} of the unit inverter is only required to be sufficiently large that it does not have significant interactions with P_{out}. This means that a reduction in the inverter's f_{-3dB} (P_1 of the LDO) may not have significant impacts on the overall performance of the LDO. However, if the f_{-3dB} of the inverter falls too much, it would be easy for the RLDO to fall into instability.

A DC sweep simulation must be performed to determine the device width values that allow $V_M \approx \frac{V_{DD}}{2}$, for the initial L evaluation. To simplify the process of calculating the required device widths, W_n is set to the minimum value, $\frac{K_n^{'}}{K_p^{'}}$ is assumed to be 4, and Equation (3.1) is used to calculate W_p. For the initial DC sweep, the device widths require tuning to achieve the desired V_M. Once the W_n and W_p values are determined for the first L, the data from the RSCE study is used to estimate the ratio, $\frac{K_n^{'}}{K_p^{'}}$, by rearranging Equation (3.1). From here, the ratio $\frac{W_n}{W_p}$ can be estimated, for each subsequent L of interest. This method proved reasonable for determining the optimum device width values for each L via hand analysis, however, some tuning is required upon simulation verification.

$$\frac{W_p}{W_n} = \frac{K_n^{'}(V_M - V_{TH_n})^2[1 + \lambda_n V_M]}{K_p^{'}(V_M - |V_{TH_p}|)^2[1 + \lambda_p V_M]} \tag{3.1}$$

From here a DC operating point analysis, a DC sweep, and an AC sweep are performed on the inverter test bench for each L under consideration. Figure 3.1 and Table 3.1 show the unit inverter's open-loop response and other design and performance parameters. The designed inverter sizing is chosen to maximize A_{vt}, which is 5 dB higher than for the minimum L inverter. The f_{-3dB} is reduced by about half, though is still quite large at 1.8 GHz. I_Q experienced a 200 nA increase over the minimum sized inverter.

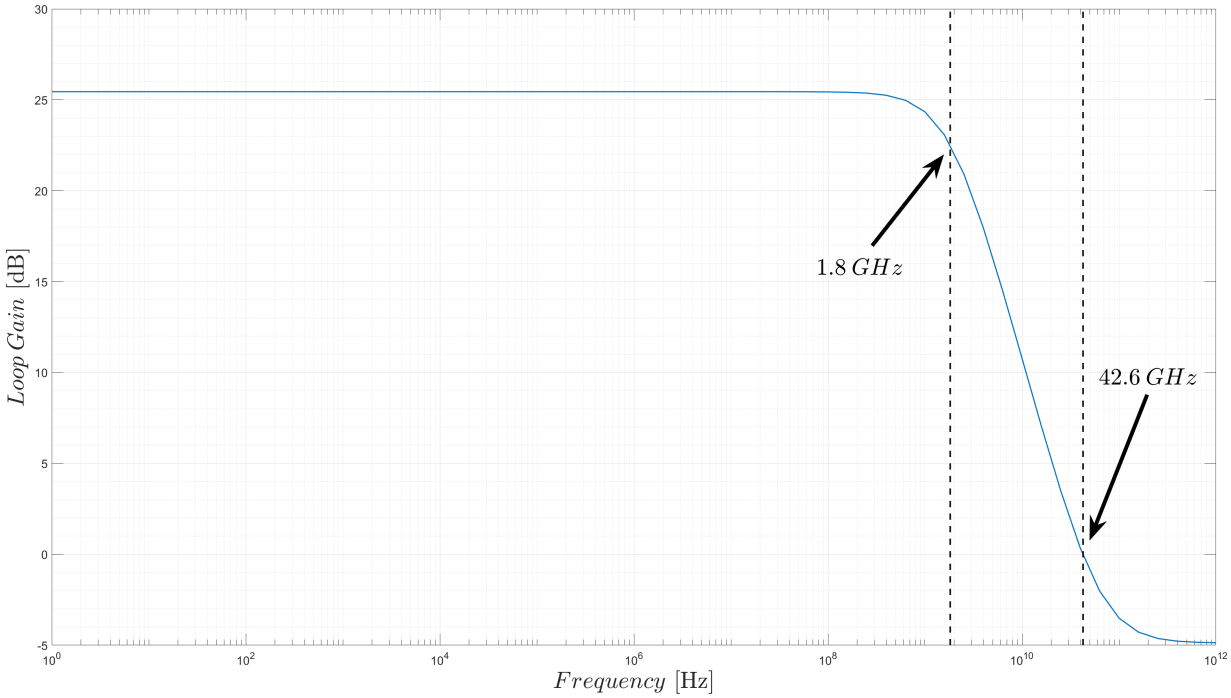

Figure 3.1: Open-loop frequency response of 90 nm RLDO unit inverter

Table 3.1: 90 nm unit inverter sizing results

Parameter	**Minimum L Value**	**Designed Value**	**Unit**
W_N	$1.2(W_{Min})$	W_{Min}	[nm]
W_P	W_{Min}	W_{Min}	[nm]
L	L_{Min}	$1.6(L_{Min})$	[nm]
V_M	602	602	[mV]
I_Q	5.15	5.35	[µA]
A_{vt}	20.4	25.4	[dB]
f_{-3dB}	3.7	1.8	[GHz]
UGF	42.2	42.6	[GHz]

3.2 RLDO Loop Design

This section presents the remaining design for the 90 nm RLDO. The RLDO is designed for an I_{LOAD} range of 2 mA to 100 mA. V_{DD} is 1.2 V for this process. Additional design objectives include an average T_{SETTLE} of less than 500 ns and total capacitance less than 50 pF. The design objectives are based on Sangid's RLDOE design objectives, but modified for the single loop design and process scaling. The schematic for the proposed RLDO is shown in Figure 3.2 [9].

3.2.1 T-Gate Design

The process for designing the T-gates is similar to that of the inverter. Equation (3.2) shows the equation for the drain to source resistance (R_{ds}) of the T-gate at a given input voltage (V_{in}). The T-gates used for sampling (Φ_S), amplifying (Φ_A), and for autozeroing (Φ_{AZ}) are designed for high impedance. This helps to mitigate charge leakage from C_{HOLD} and to reduce the size and parasitics. One drawback to a larger impedance is that it increases the C_{HOLD} time constant and the corresponding sample time. The T-gates used for enabling have a reduced impedance for faster gate charging. However, the reduced impedance T-gates are near minimally sized to minimize parasitics, which negatively impact loop bandwidth. Figure 3.3 shows the schematic for the T-gate and Figures 3.4 and 3.5 show the simulation results for drain to source resistance. Post-layout parasitic extraction (PEX) simulation results are included within the plots [9].

$$R_{ds} = \frac{L_n}{k_n W_n (V_{DD} - V_{in} - V_{THN})} || \frac{L_p}{k_p W_p (V_{in} - |V_{THP}|)} \tag{3.2}$$

3.2.2 Pseudo-Differential Switch Driver Design

The complementary outputs of the PDSD circuit, which is shown in Figure 2.6, enable the use of T-gates to simultaneously change the states of Φ_S, Φ_A, and Φ_{AZ}. Therefore, the switching point for the PDSD is ideally $\frac{V_{DD}}{2}$. This is similar to the inverter design so a similar approach is used for this circuit. As mentioned in Section 2.2.4, one difference in the design approach is that an increased L is desirable to decrease the output signal rise and fall

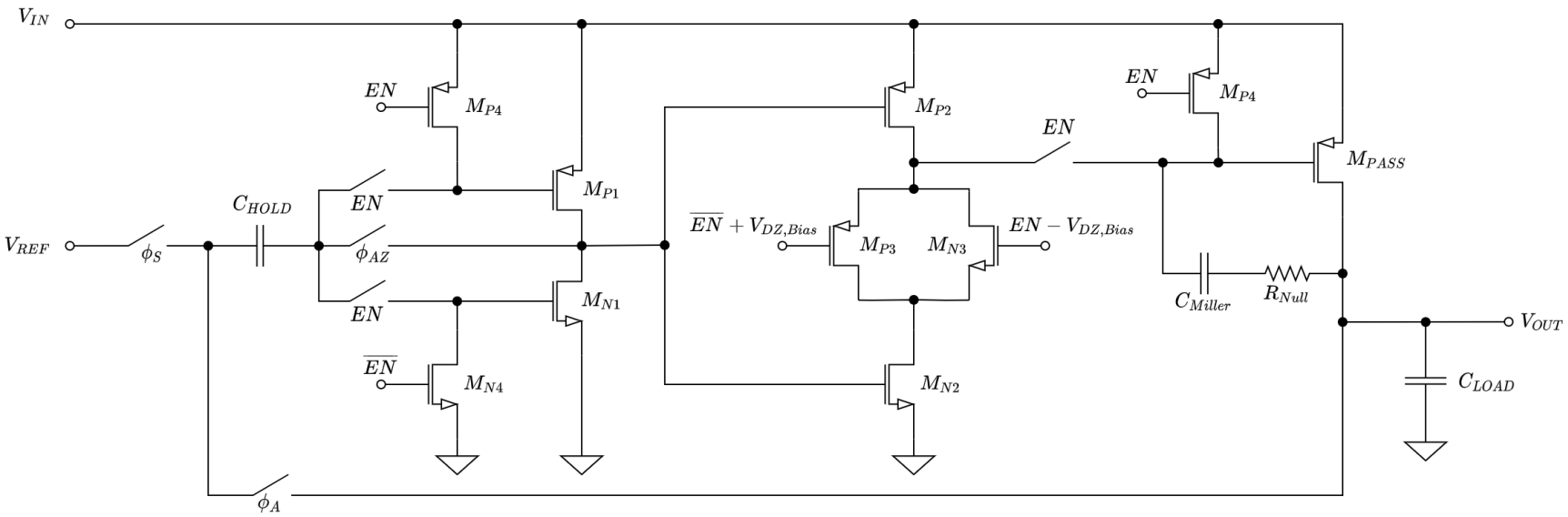

Figure 3.2: Schematic of RLDO with internal dominant-pole compensation and shutdown/enable control [9]

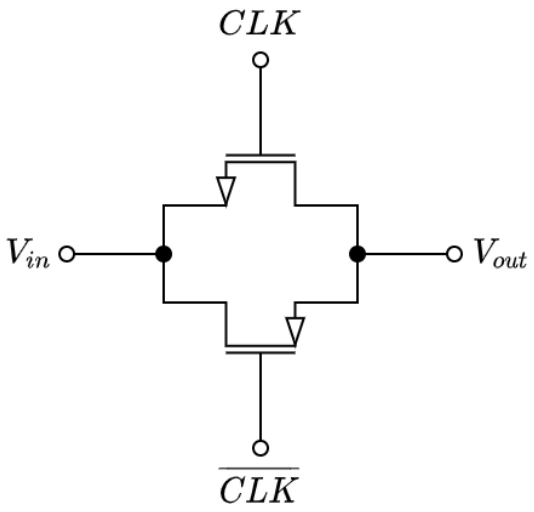

Figure 3.3: Transmission gate schematic [9]

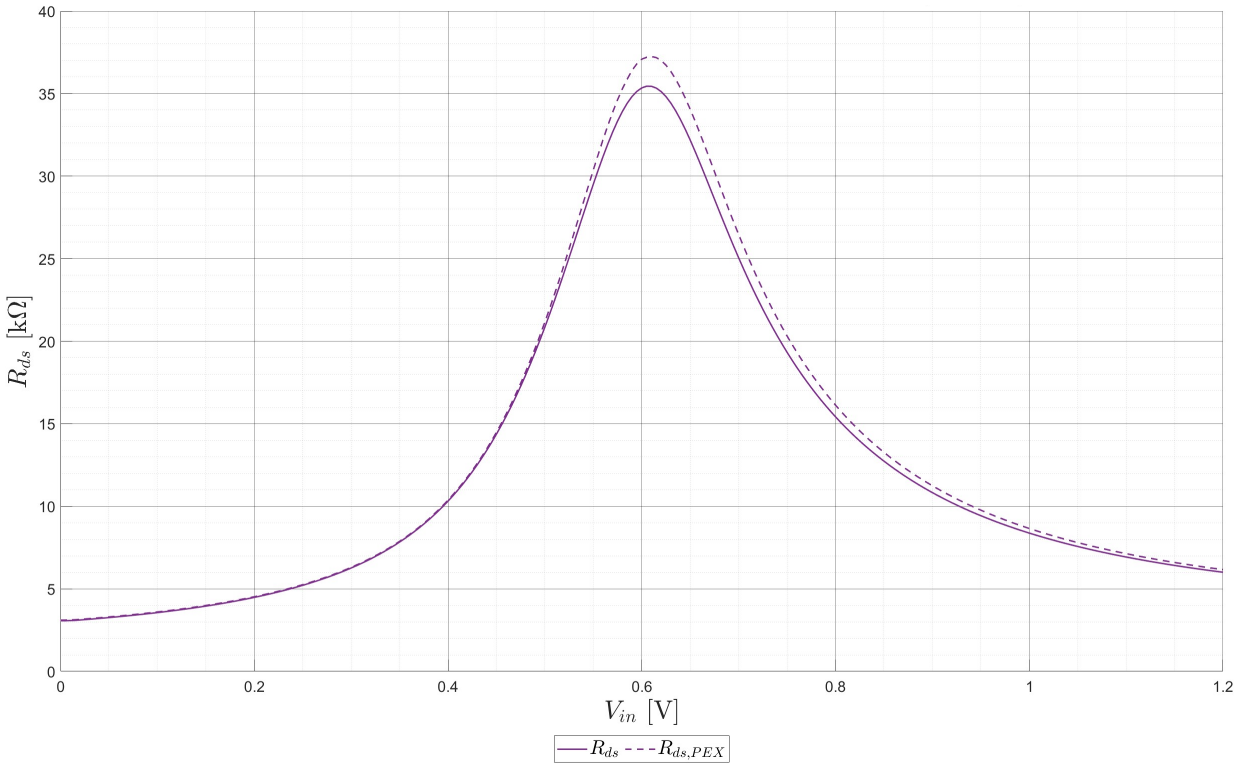

Figure 3.4: 90 nm high impedance transmission gate drain to source resistance simulation including PEX

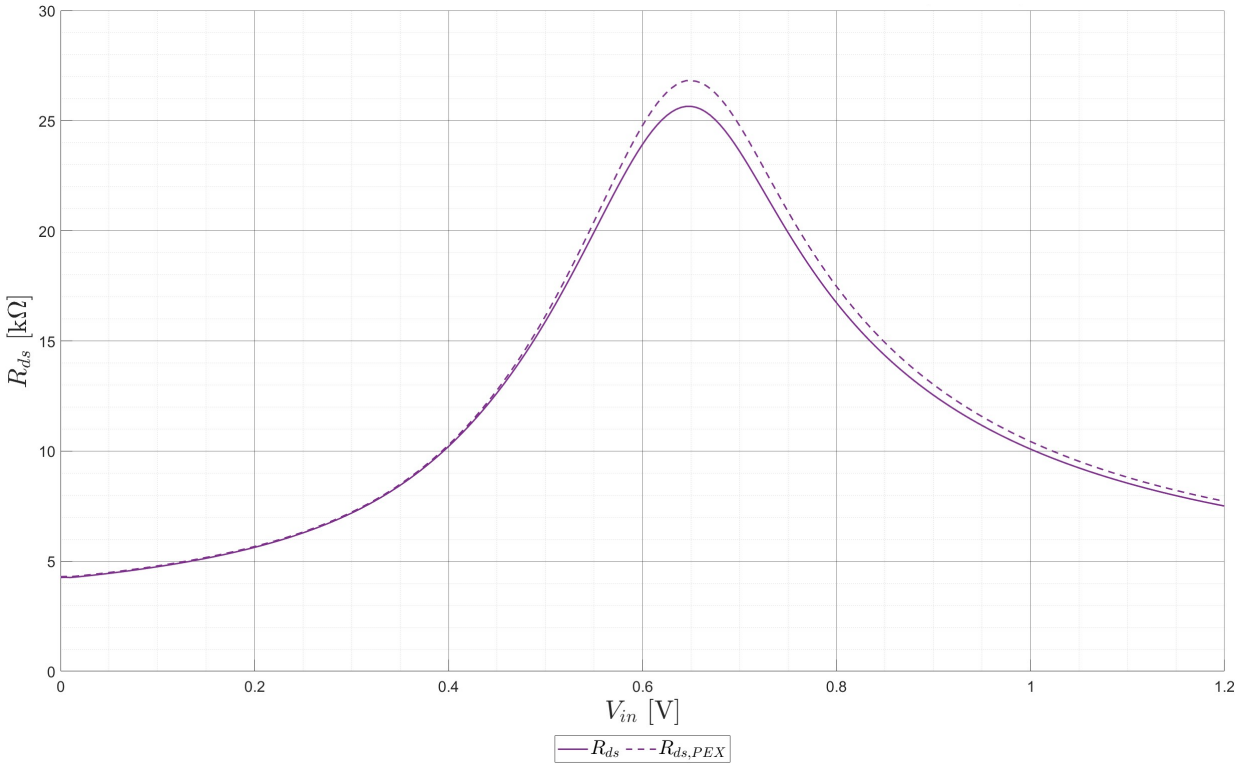

Figure 3.5: 90 nm reduced impedance transmission gate drain to source resistance simulation including PEX

times, with respect to the input signal. This helps to reduce high-frequency noise injection into the system. The PDSD contributes approximately 450 nA to the RLDO's total current draw. The simulated transient signals are shown in Figure 3.6 [9, 15].

3.2.3 Pass Device Design

For peak efficiency, M_{PASS} can be designed for triode operation, which allows V_{DO} to be less than $V_{SD_{SAT}}$. For this design, to effectively optimize the pass transistor (M_{PASS}) for transient performance, it needs to be sized such that it remains in saturation at the extreme conditions of I_{LOAD}. Fortunately, due to the negative feedback action, V_{SD} can be viewed as a fixed voltage, with respect to biasing. This means that if a transistor is in saturation at the maximum I_{LOAD}, then the transistor will inherently be in saturation at the minimum I_{LOAD}, due to there being a lower V_{SG} with a fixed V_{SD}. V_{DO} must be greater than the transistor's $V_{SD_{SAT}}$, as shown in Equation (3.3). If designing to the minimum possible V_{DO}, Equation (2.7) can be simplified to replace the overdrive voltage and V_{SD} terms with V_{DO}. However, it is desirable to build in margin to ensure the transistor is fully saturated which requires replacing the overdrive voltage term with $V_{SD_{SAT}}$ instead of V_{DO} as shown in Equation (3.5) [10, 12].

$$V_{DO} = V_{DD} - V_{OUT} \geq V_{SD_{SAT}} \tag{3.3}$$

$$I_{L_{MAX}} = K_p^{'} \frac{W}{2L} (V_{DO})^2 [1 + \lambda_p (V_{DO})] \tag{3.4}$$

$$I_{L_{MAX}} = K_p^{'} \frac{W}{2L} (V_{SD_{SAT}})^2 [1 + \lambda_p (V_{DO})] \tag{3.5}$$

The maximum desired I_{LOAD} for the proposed RLDO is 100 mA with a V_{DO} of 250 mV. The resulting effective width is 7200 µm with an estimated maximum $C_{GD,PASS}$ and $C_{GS,PASS}$ values of 11.84 pF and 19.70 pF, respectively. In comparison to Sangid's 180 nm pass transistor with equivalent maximum I_{LOAD}, the 90 nm device saw an effective width increase of 80 % with a larger V_{DO} and a maximum C_{GD} increase of 90 %. These results align with the

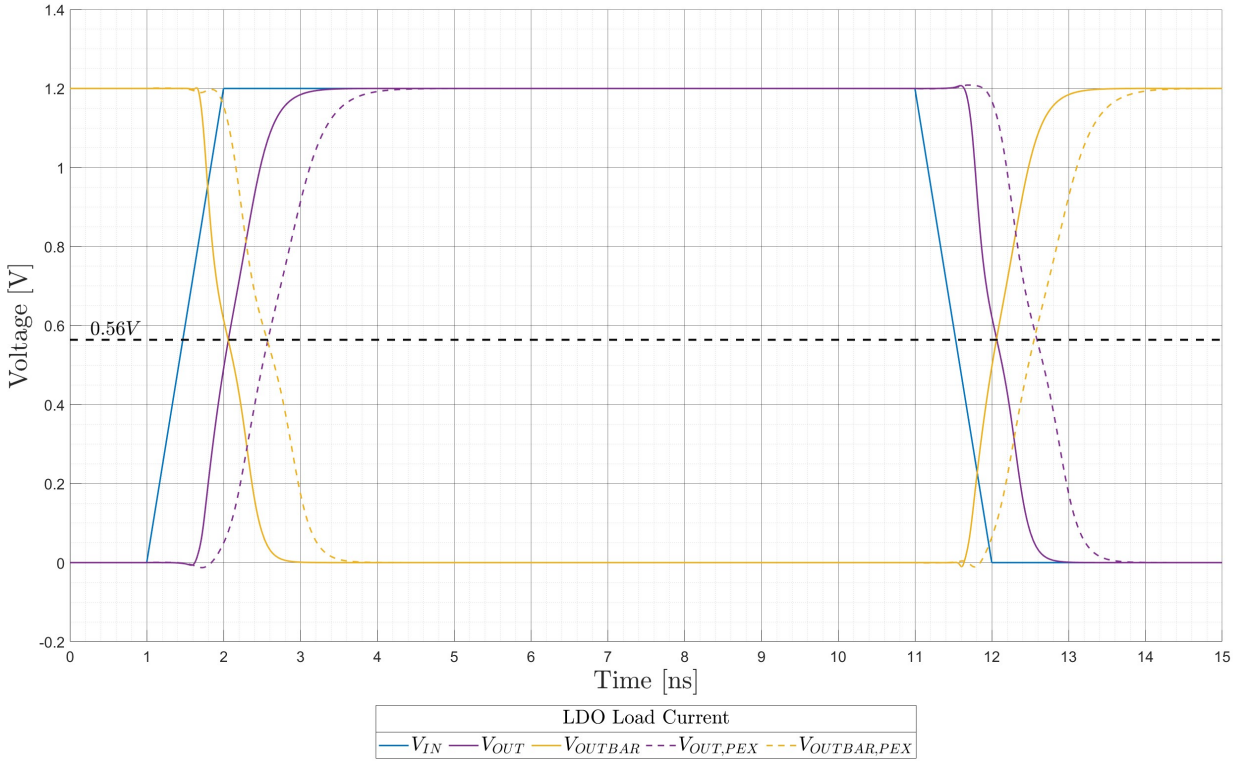

Figure 3.6: 90 nm pseudo-differential switch driver transient simulation results including PEX

expected results for constant field scaling occurring between the 180 nm and 90 nm processes [9, 29].

3.2.4 Stability Design & Analysis

To ensure the stability of the RLDO, the critical poles and zeros of the system must be analyzed to determine the required amount of compensation. The critical poles of this system are the pole at the output of the first stage inverter, P_1, the pole at the output of the ringamp error amplifier, P_{ra}, and the pole at the output of the RLDO, P_{out}. Additionally, there is a RHP zero associated with the pass devices gate to drain capacitance. The poles and zero locations are estimated by using Equations (3.6) to (3.9).

$$C_{ra} = (C_{GD,PASS} + C_{Miller})(1 - A_{vt,PASS}) + C_{GS,PASS} \tag{3.6}$$

$$P_{ra} = \frac{1}{(R_{ra} + R_{EN})C_{ra}} \tag{3.7}$$

$$z_{ra} = \frac{g_{m_{PASS}}}{C_{GD_{PASS}}} \tag{3.8}$$

$$P_{out} = \frac{1}{(R_{OUT})(C_{GD_{PASS}}(1 - \frac{1}{A_{vt_{PASS}}}) + C_L)} \tag{3.9}$$

From the previous design analysis of the first stage inverter in Section 3.1, the associated pole, P_1 is located at approximately 1.8 GHz. P_{ra}, which is the dominant pole for the RLDO, is approximately located at 11.6 kHz for a 2 mA load and at 12.8 kHz for a 100 mA load. The approximate location of z_{ra} is 3.87 GHz for a 2 mA load and 5.86 GHz for a 100 mA load condition. Finally, P_{out} is approximately located at 333.0 MHz for a 2 mA load and at 356.3 MHz for a 100 mA load condition.

For these results, the RLDO achieves a loop bandwidth between 30.3 MHz and 35.0 MHz, while maintaining a phase margin greater than 80.0 deg. This is primarily due to P_{ra} and P_{out} having very little variation over I_{LOAD}. At both extremes, P_{out} is approximately a decade beyond the crossover frequency, and since P_1 and z_{ra} are far enough beyond the crossover

frequency that the interaction with P_{out} is minimal a large phase margin is achieved. Because of these results, and due to the large $C_{GD,PASS}$, the RLDO can achieve stability without requiring a Miller compensation capacitor which would increase the area and reduce the loop bandwidth.

Figure 3.7 show the simulated loop gain and loop phase plots for the RLDO, including PEX results, for 2 mA, 50 mA, and 100 mA load conditions. Tables 3.2 to 3.4 show a comparison between simulation and PEX results. It should be noted that the PEX results include pad parasitics. From these results, it's clear that P_1 and P_{out} locations are reduced due to the added layout and pad parasitics. However, the reduction does allow the RLDO to remain stable between an I_{LOAD} range of 2 mA to 100 mA with a reduced loop bandwidth range of 20.0 MHz to 22.5 MHz. z_{ra} does not influence the results. The revised proposed RLDO schematic is shown in Figure 3.8.

3.3 Physical Implementation

The RLDO was fabricated using a standard 90 nm CMOS process. The full chip layout is shown in Figure 3.9, with the RLDO highlighted as LDO 1. The RLDO is configured to have two off-chip power supplies for the ringamp error amplifier and the pass device. This allows for precise current monitoring through a source measurement unit (SMU). The RLDO is also configured for the sample and amplify clock signal and required reference voltages (V_{REF}, EN, etc.) to be supplied off-chip. The pads include ESD protection and the pass device pads are designed for high current capacity to mitigate ESR when I_{LOAD} is large.

The active area of the ringamp error amplifier and the associated T-gate controls is 0.026 mm^2, and the active area of the pass device is 0.005 mm^2. Since the RLDO required no compensation capacitance, the total RLDO active area is 0.031 mm^2, which is 45.6 % of the total area of the 180 nm RLDOE. It should be noted that this area comparison does not account for the CMOTA and additional support circuitry required for the 180 nm RLDOE, which is not included within this 90 nm RLDO. However, as these additional circuits are relatively small, the comparison remains reasonable. Layouts for the PDSD, ringamp error amplifier, T-gates, and pass device are included in the Appendix.

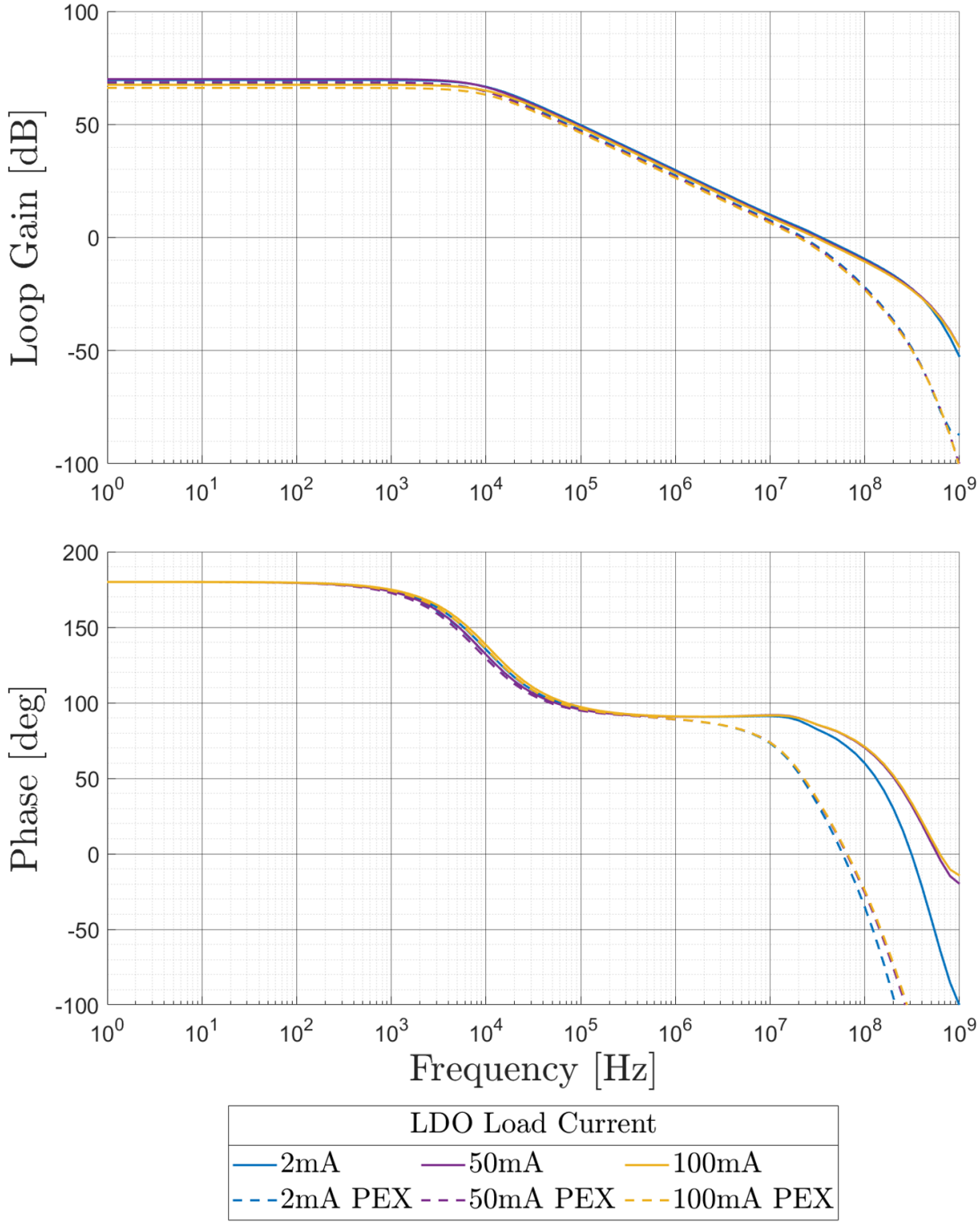

Figure 3.7: 90 nm RLDO loop gain and phase simulation results including PEX

Table 3.2: RLDO AC analysis summary for simulation vs. PEX at 2 mA load

Parameter	Simulation	PEX Simulation	Unit
A_o	69.6	68.4	[dB]
f_c	35.0	22.5	[MHz]
$P.M.$	81.1	48.7	[deg]

Table 3.3: RLDO AC analysis summary for simulation vs. PEX at 50 mA load

Parameter	Simulation	PEX Simulation	Unit
A_o	70.0	68.15	[dB]
f_c	32.1	21.1	[MHz]
$P.M.$	85.3	52.9	[deg]

Table 3.4: RLDO AC analysis summary for simulation vs. PEX at 100 mA load

Parameter	Simulation	PEX Simulation	Unit
A_o	67.5	66.1	[dB]
f_c	30.3	20.0	[MHz]
$P.M.$	86.0	55.2	[deg]

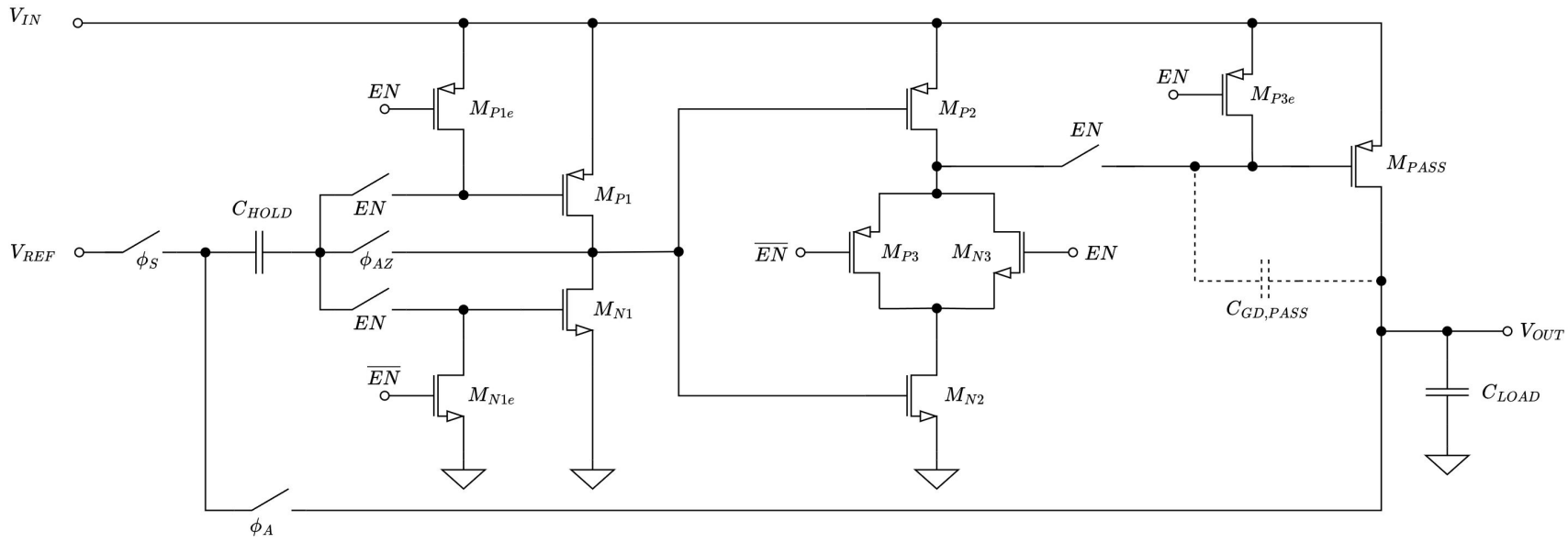

Figure 3.8: Schematic of RLDO with inherent dominant-pole compensation and shutdown/enable control [9]

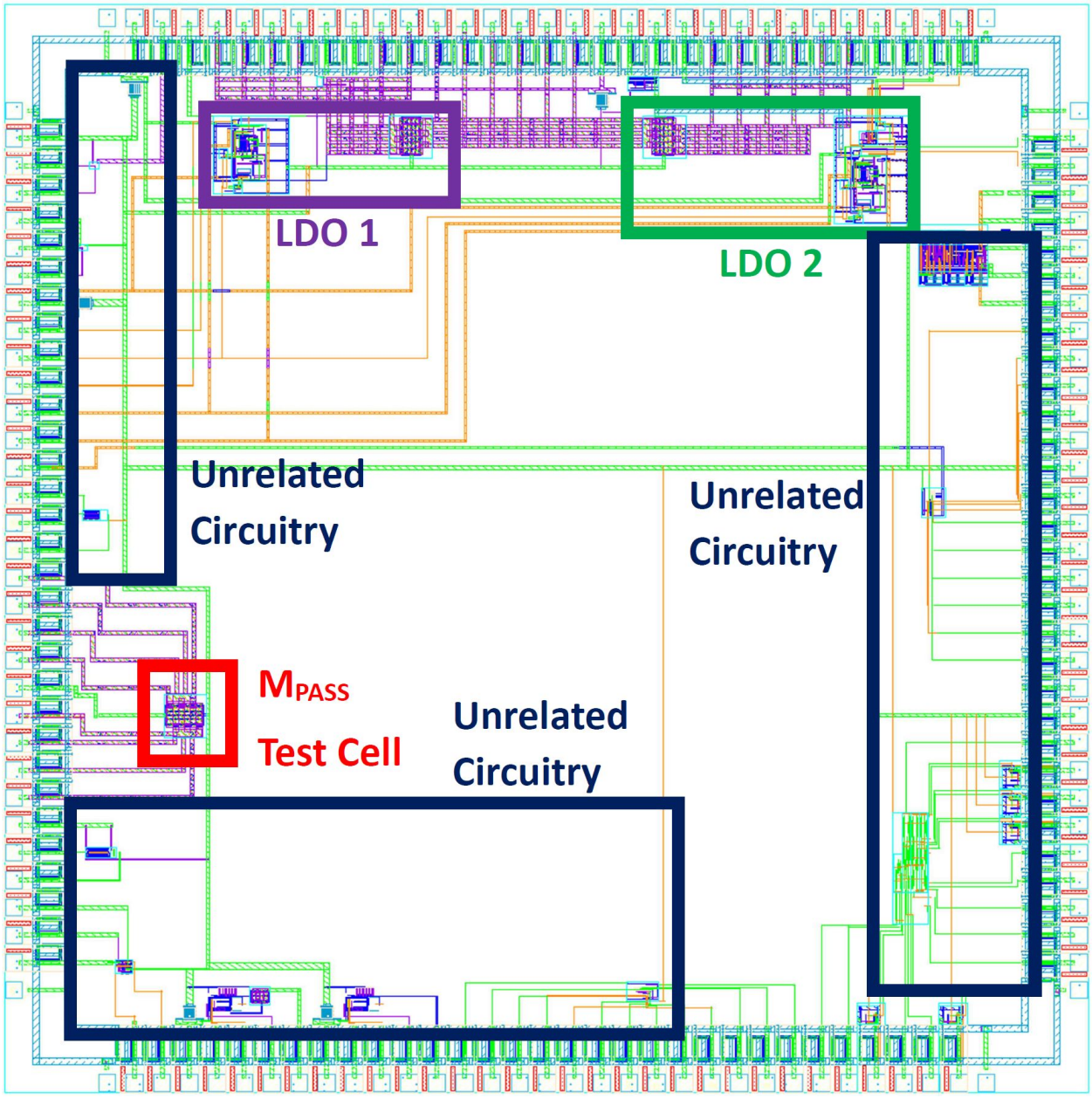

Figure 3.9: Full chip Cadence® layout image with relevant circuits highlighted (3 mm x 3 mm)

Chapter 4

Evaluations & Comparisons

4.1 Test Board & Equipment

4.1.1 Test Board Modifications

In lieu of designing a new test board for this chip, it is advantageous to appropriate Sangid's Teucer evaluation board and modify it for a 1.2 V supply. Great care is required during the chip design phase to ensure the pinout of the RLDO on the 90 nm chip is aligned with the pinout of the RLDOE on the 180 nm chip [9] to facilitate using the Teucer evaluation board. Additional design considerations included using the same package (QFN80) and making small redesigns to the evaluation board to accommodate reduced supply voltages. The redesign is accomplished by building out a blank test board and swapping out the components that are incompatible with this chip (*e.g.,* discrete LVRs). Doing this not only allows for the best possible direct comparison between the LDOs, as the test conditions are as similar as possible, but it also leverages the well thought out design features of the Teucer evaluation board and greatly saves on design time and board fabrication costs. Additional Teucer evaluation board background and the board's schematics, bill of materials, and assembly drawings can be found in [9]. The completed board assembled for evaluation of the 90 nm RLDO is shown in Figure 4.1.

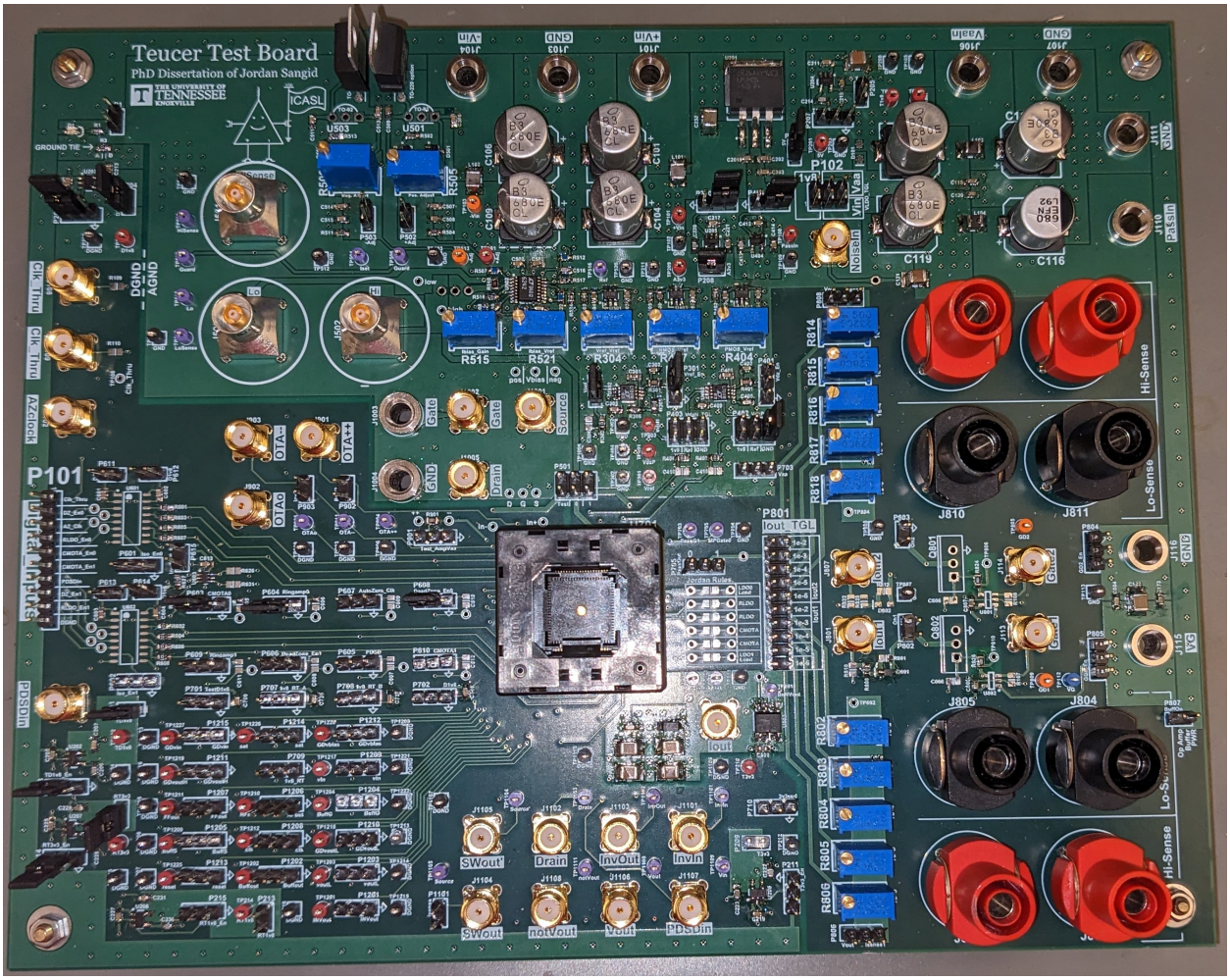

Figure 4.1: The modified Teucer test board for experimental evaluations of the 90 nm RLDO [9]

4.1.2 Test Equipment

The evaluations performed in this study include Line-to-Load regulation DC sweeps, transient current load steps, and power supply rejection (PSR). This section discusses the required equipment and the critical equipment functionality. A function generator is required for the RLDO sample and amplify clock. The signal has an edge of 5 ns and has a pulse width of 30 ns. A second function generator is required for stepping the load current. This signal has an edge 80 ns and carries up to 100 mA the function generator is required to sync. These two signals must be synchronized to prevent clock slippage. A DC source is required to supply power to the evaluation board. An SMU is required to provide supply voltages to the RLDO while taking precise current measurements. An oscilloscope is required for capturing signal waveforms. The test equipment used for evaluations of the 90 nm RLDO are:

- Keithley 2231A-30-3 DC Power Supply
- Agilent 33250A 80 MHz Function Generator
- Keysight 33500B 20 MHz Function Generator
- Keysight InfiniiVision MSOX4024A Mixed Signal Oscilloscope
- Keithley 2636B System SourceMeter

4.2 LDO Evaluations

A modified version of Sangid's RLDOE test configuration is shown in Figure 4.2. Since this RLDO is a single loop LDO, the DAQ and PC are not required to manage the transition of the RLDO and CMOTA loops and are therefore eliminated from the test configuration. Data from the evaluations are recorded via the oscilloscope's USB output. The sample and amplify clock is set to a period of 10 µs, a pulse width of 30 ns, a clock edge of 5 ns, and has a swing from 0 V to V_{DD}.

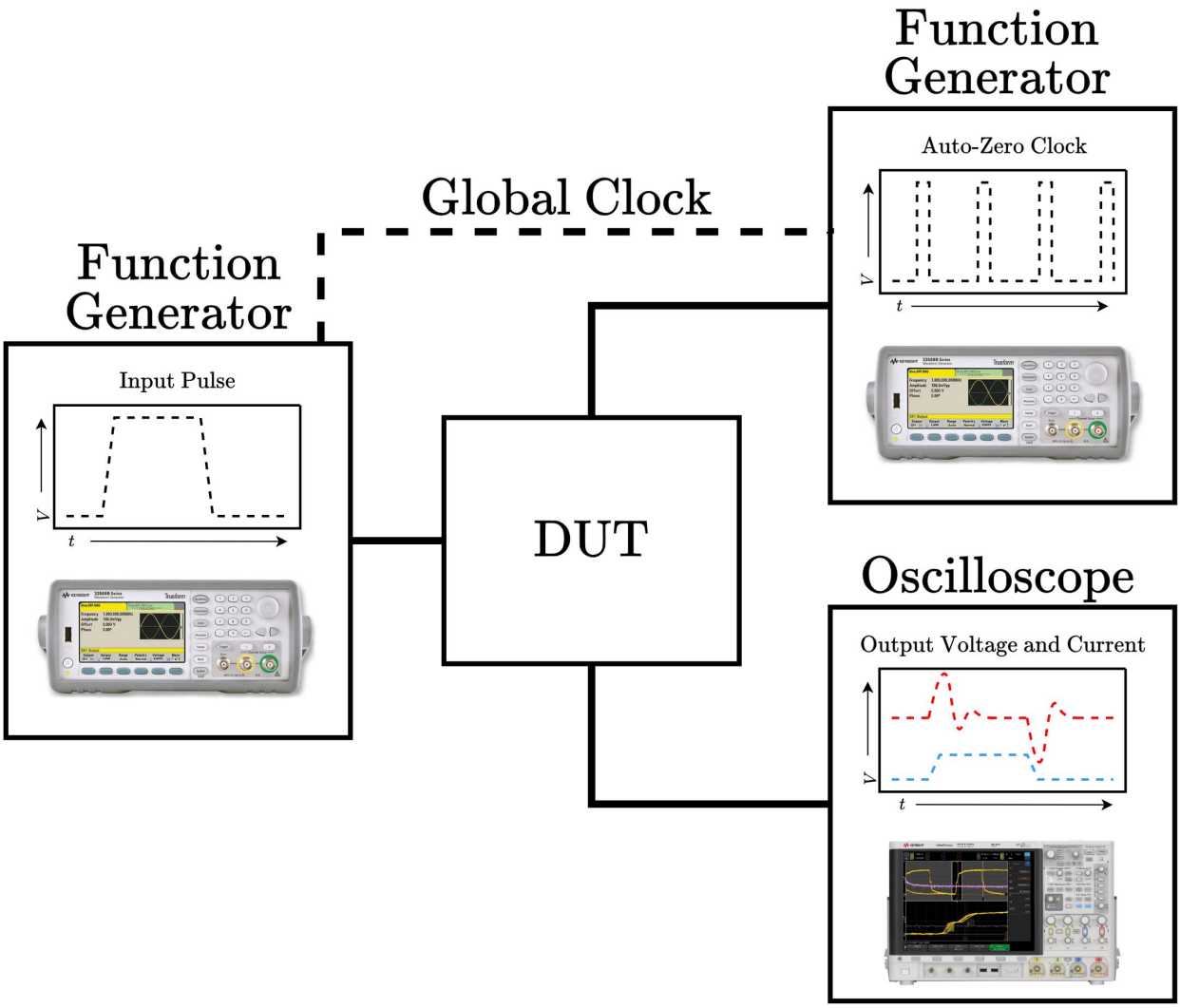

Figure 4.2: Experimental transient current load step response test configuration [9]

4.2.1 Line-to-Load Regulation

The Line-to-Load regulation evaluation is used to determine the minimum V_{DO} and the operating range of the RLDO. A reference voltage V_{REF} is set to a fixed voltage, and V_{IN} is swept from V_{DD} down. V_{REF} is then stepped down and the sweep is repeated. A fixed load current of $I_{LOAD} = 100\,\text{mA}$ is set over the full range of V_{IN} and V_{REF}. The evaluation results are shown in Figure 4.3.

As V_{IN} is swept, V_{OUT} initially is flat and strongly regulated for most values of V_{REF}. This region represents the operating region of the RLDO where the RLDO has high loop gain. As V_{IN} drops to the region where the LDO has low loop gain, V_{OUT} begins to slope downward linearly. The V_{OUT} slope increases further when V_{IN} falls into the region where the RLDO has no loop gain and V_{OUT} reaches 0 V when the RLDO has no voltage headroom. These results indicate an approximate minimum V_{DO} of 110 mV.

4.2.2 Transient Current Load Step

The transient current load step evaluation is used to directly determine the T_{SETTLE} and the ΔV_{OUT} of the RLDO for a given load step. Additional performance metrics such as loop bandwidth, loop gain, slew rate, phase margin, etc. can be indirectly determined or inferred from these results. To perform the evaluation, a function generator, that is synced with the sample and amplify clock, is used to establish the current load steps. This signal has a period of 10 µs with a 50 % duty cycle and an 80 ns clock edge.

The Teucer evaluation board has two independent resistor arrays for configuring an I_{LOAD} from 1.9 µA to 95 mA, where the maximum I_{LOAD} is set with a precision 0.05 % 10 Ω resistor between V_{OUT} and a node connected to a jumper that can be tied to ground. During a transient step, one array will have this node tied to ground setting a constant minimum load. This node on the other array is brought down to ground via a function generator to supply the load step. However, this configuration does not enable the required I_{LOAD} of 100 mA, therefore another testing modification is required from Sangid's evaluation setup.

Thanks to Sangid's well-planned evaluation board, there is a high-speed Schottky diode located at the end of the resistor array. The function generator is used to forward bias the

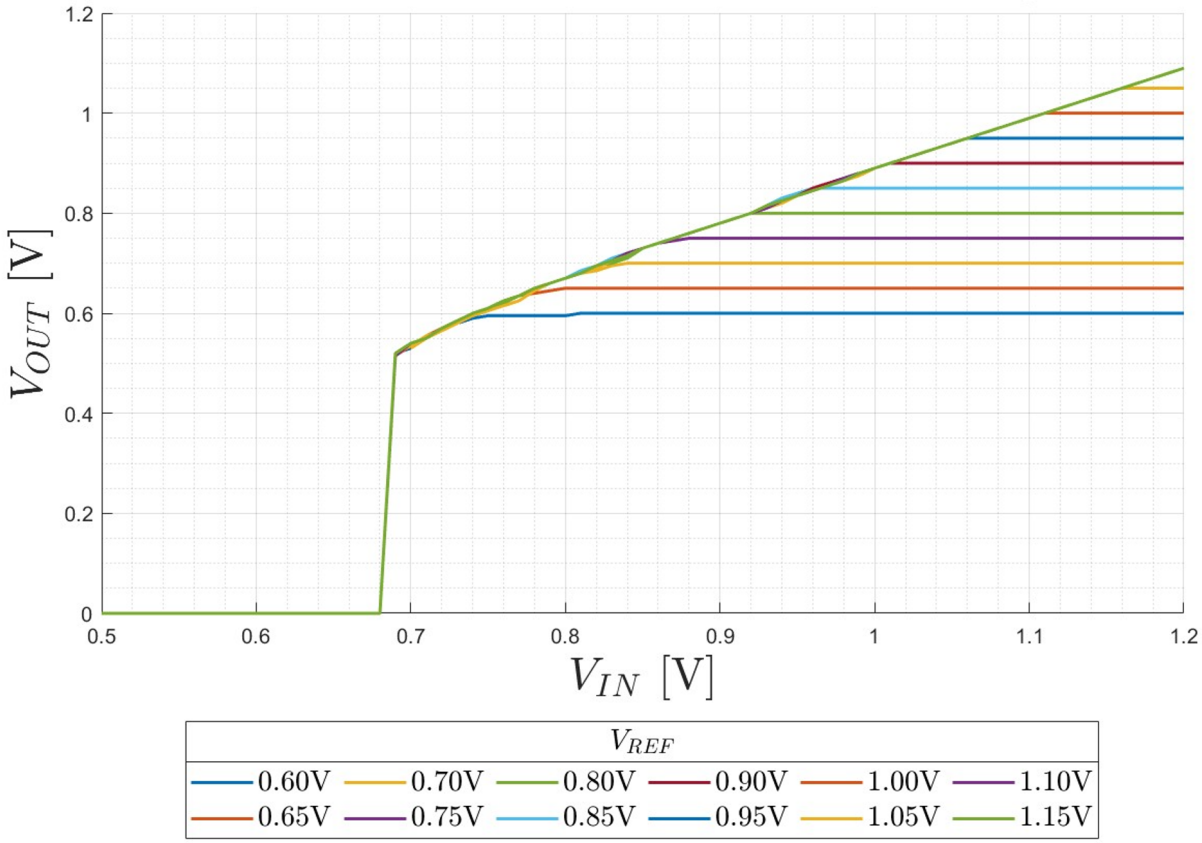

Figure 4.3: 90 nm RLDO experimental Line-to-Load DC sweep test results

Schottky diode enough to draw the required 100 mA. There is a capacitive loading penalty for this option, which results in slightly more ringing at 2 mA loads than anticipated based on the simulation and PEX results. There is also a penalty with respect to clock edge. On the load steps from 2 mA to 20 mA and 50 mA, the clock edge slowed by $10-30\%$. However, the impact to the 2 mA to 100 mA clock edge is not measurable.

Table 4.1 shows the results summary for the load steps from 2 mA to 100 mA and 50 mA with a V_{DD} of 1.2 V. Table 4.2 shows the results summary for the load step from 2 mA to 20 mA with a reduced V_{DD} of 0.9 V. The experimental performance is comparable to the simulation and PEX results demonstrating the successful fabrication and scaling of the 90 nm RLDO from the 180 nm RLDOE. See the Appendix for experimental load step plots.

4.2.3 Power Supply Rejection

The PSR evaluation is intended to quantify the LDO's effectiveness at power supply noise rejection onto the load across frequency. In a simulation environment, this evaluation is performed by applying a small signal frequency sweep on the V_{IN} supply. On the lab bench, the setup is not as simple. An AC test signal from a function generator must be summed with the DC supply voltage supplied applied to V_{IN} from the SMU. If the SMU and function generator are directly connected to a common node, the AC test signal is filtered out by the SMU. To sum these two signals, a DC blocking capacitor (C_{ZDC}) and an AC blocking inductor (L_{ZAC}) are implemented as shown in Figure 4.4. At DC, C_{ZDC} acts as a high-impedance path, and L_{ZAC} acts as a low-impedance path. This allows the DC supply current to pass into the RLDO without current being diverted by the low impedance output of the function generator. At high frequencies, relatively speaking, C_{ZDC} acts as a low-impedance path, and L_{ZAC} acts as a high-impedance path. This allows the AC test signal to pass onto V_{IN}, DC shifted by the supply voltage, without being filtered by the SMU.

This setup is a replication of Sangid's PSR evaluation setup, which is based on [30]. The critical resonance frequency (f_c) is set by Equation (4.1) below. One change to the setup is to increase the values of C_{ZDC} and L_{ZAC} to decrease f_c. For Sangid's setup, he is only able to evaluate down to 30 kHz. This is sufficient to measure PSR of the RLDO loop of the RLDOE, where the dominant pole is estimated to be 300 kHz, but is insufficient to evaluate

Table 4.1: 90 nm RLDO current load step results for $V_{DD} = 1.2\,\mathrm{V}$

Evaluation	**Parameters**	**Unit**	**Simulated**		**Experimental**			
			Initial	PEX	Min.	Mean	Max.	$\sigma_{n=4}$
$V_{DD} = 1.2\,\mathrm{V}$	I_Q	[µA]	15.4		13.7	14.8	15.9	1.0
Current Load Step 2 mA to 100 mA $V_{DD} = 1.2\,\mathrm{V}$ $V_{REF} = 0.95\,\mathrm{V}$ $t_{\Delta edge} = 80\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	250	252	249	252	254	2.6
	V_{OS}	[mV]	244	244	144	147	150	3.0
	$T_{OS,SETTLE}$	[ns]	142	168	253	255	258	2.4
	V_{US}	[mV]	94	117	170	180	193	11.1
	$T_{US,SETTLE}$	[ns]	80	82	112	114	115	1.3
Current Load Step 2 mA to 50 mA $V_{DD} = 1.2\,\mathrm{V}$ $V_{REF} = 0.95\,\mathrm{V}$ $t_{\Delta edge} = 80\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	250	250	247	249	251	2.2
	V_{OS}	[mV]	103	130	122	111	132	2.5
	$T_{OS,SETTLE}$	[ns]	117	135	145	223	426	11.6
	V_{US}	[mV]	47	67	139	88	152	7.0
	$T_{US,SETTLE}$	[ns]	49	82	51	104	132	4.1

Table 4.2: 90 nm RLDO current load step results for $V_{DD} = 0.9\,\mathrm{V}$

Evaluation	**Parameters**	**Unit**	**Simulated**		**Experimental**			
			Initial	PEX	Min.	Mean	Max.	$\sigma_{n=4}$
$V_{DD} = 0.9\,\mathrm{V}$	I_Q	[µA]	5.0		3.3	3.8	4.2	0.4
Current Load Step 2 mA to 20 mA $V_{DD} = 0.9\,\mathrm{V}$ $V_{REF} = 0.85\,\mathrm{V}$ $t_{\Delta edge} = 80\,\mathrm{ns}$	$V_{DO(RMS)}$	[mV]	50	50	46	47	49	1.6
	V_{OS}	[mV]	40	43	30	31	32	1.0
	$T_{OS,SETTLE}$	[ns]	170	214	245	291	325	33.4
	V_{US}	[mV]	36	58	46	50	52	2.9
	$T_{US,SETTLE}$	[ns]	96	118	148	159	168	8.3

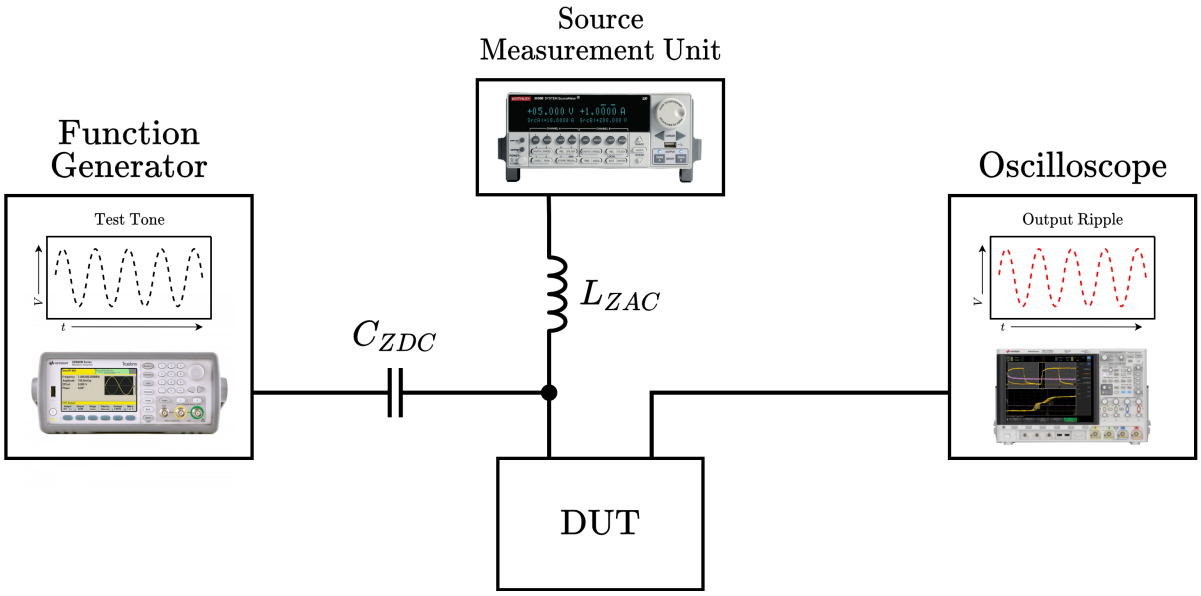

Figure 4.4: Experimental power supply rejection test configuration [9]

the CMOTA loop PSR which has a dominant pole located at an estimated 1 kHz. For the analysis in Chapter 3, the dominant pole for this work's RLDO is estimated to be located at 12.8 kHz, therefore limiting evaluations to frequencies of 30 kHz and above for this work would be insufficient. C_{ZDC} and L_{ZAC} values are chosen to support measurements down to frequencies of 5 kHz to account for this work's decreased dominant pole.

$$f_c = \frac{1}{2\pi\sqrt{L_{ZAC}C_{ZDC}}} \tag{4.1}$$

To measure the PSR, a load is applied to the output of the LDO, and a sinusoidal waveform is applied as the test signal input. The peak-to-peak amplitude of the test signal and LDO output signal are measured. PSR is calculated using Equation (4.2) below. This measurement is repeated across the applicable frequency range where measurements are valid. A load of 100 mA is chosen for this evaluation since the upper range of an LDO's allowable load current represents a worst-case for PSR. The PSR evaluation results are shown in Figure 4.5 which includes a curve fit of PSR.

From the Figure 4.5 plot, the dominant pole is observed to be at approximately 200 kHz, which is a decade higher than estimated. However, a 20 $\frac{\text{dB}}{\text{Dec}}$ slope is observed between the dominant pole and the 0 dB frequency of 10 MHz. This implies a single low-frequency pole and a crossover frequency of approximately 10 MHz, which aligns reasonably well with the AC analysis from Section 3.2.4. The difference between the simulated and measured dominant pole frequency can be explained by the limitations of the PSR test setup with respect to establishing a sufficiently low f_c. Higher frequency poles and the RHP zero are not visible due to being located beyond the measured frequency range of this experiment, which also aligns with Section 3.2.4. The peak PSR is observed to be approximately -25.9 dB.

$$PSR = 20\log\left(\frac{v_{out-pp}}{v_{test-pp}}\right) \tag{4.2}$$

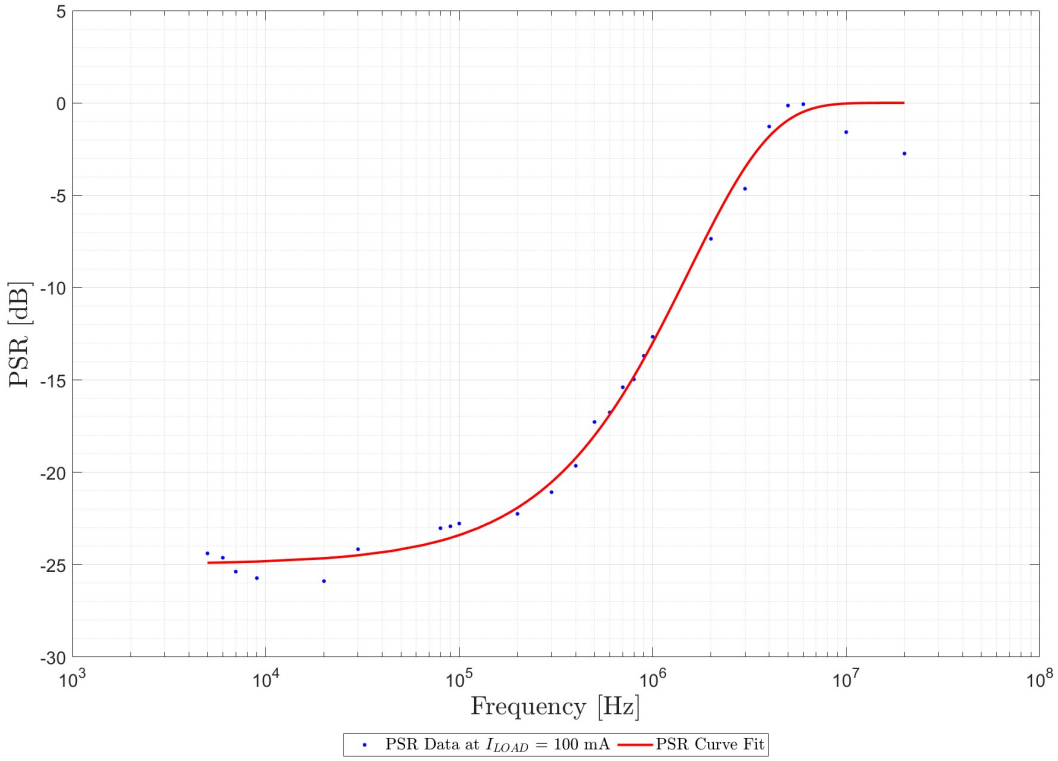

Figure 4.5: 90 nm RLDO experimental and curve fit power supply rejection test results

4.3 Results Summary

Table 4.3 shows the experimental result summaries comparison between the 180 nm RLDOE and the scaled 90 nm RLDO. Figure 4.6 shows the scaled 90 nm RLDO's FOMs plotted on the graph from Section 2.2.5. From these comparisons, it's clear that though the 90 nm RLDO does not exceed the performance of the 180 nm RLDOE and the RLDO is below the state-of-the-art with respect to FOM_2. However, it is also clear that the RLDO is highly competitive with the RLDOE and state-of-the-art ALDOs with respect to FOM_1, largely due to the elimination of the Miller capacitor.

Table 4.3: 180 nm RLDOE and 90 nm RLDO experimental result summaries comparison [9]

Parameters	**Unit**	**Sangid [9]**	**This Work**
Year		2022	2023
Technology	[nm]	180	90
$\mathbf{V_{IN}}$	[V]	0.9-1.8	0.9-1.2
$\mathbf{V_{OUT}}$	[V]	0.6-1.7	0.85-0.95
$\mathbf{I_{OUT}}$	[mA]	200	100
$\mathbf{I_Q}$	[µA]	0.354-72	14.83
$\mathbf{V_{DO}}$	[mV]	100	250
$\mathbf{C_{TOTAL}}$	[pF]	23.3	0.4
$\mathbf{\Delta t_{edge}}$	[ns]	15	80
$\mathbf{\Delta V_{OUT}}$	[mV]	146	180.25
$\mathbf{T_{SETTLE}}$	[ns]	125	113.5
PSR at 100 kHz	[dB]	42	25.9
$\mathbf{FOM_1}$ *	[fs]	0.0301	0.107
$\mathbf{FOM_2}$ †	[V]	0.00388	2.14
Active Area	[mm^2]	0.068	0.031

$$* \; FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \text{ [13]}$$

$$\dagger \; FOM_2 = \left(\frac{\Delta t_{edge}}{1\,\text{ps}}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right) \text{ [14]}$$

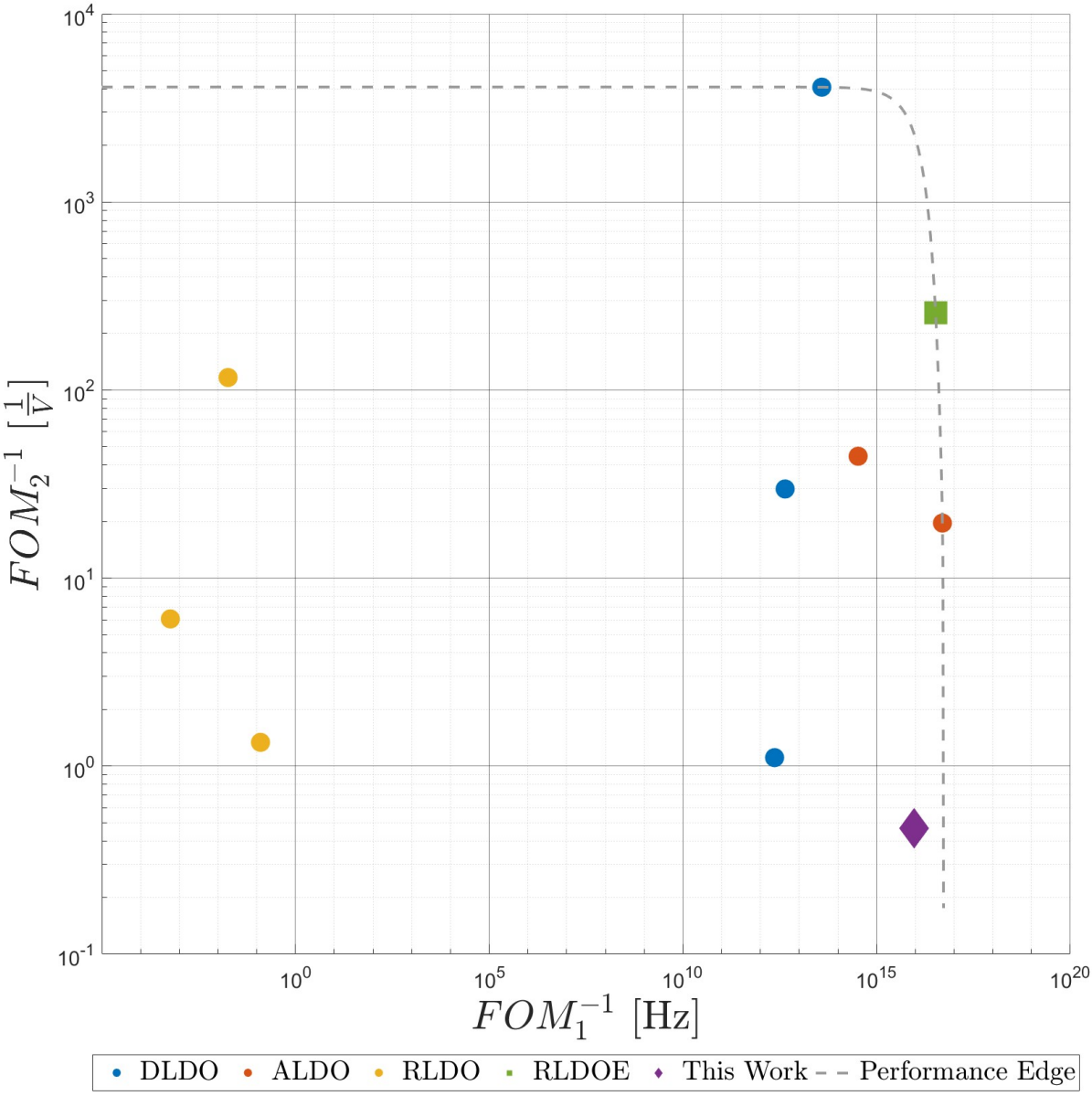

Figure 4.6: FOM comparison graph with this work plotted against State-of-the-Art LDOs [9]

Chapter 5

Conclusions and Proposed Future Work

5.1 Conclusions

This work has demonstrated a successful scaling of the RLDO loop of the 180 nm RLDOE down to a 90 nm process. The fabricated 90 nm RLDO is able to supply up to 100 mA with strong voltage regulation on fast transient events, implying high loop gain and bandwidth. This RLDO is also shown to be competitive with state-of-the-art LDOs with respect to FOM_1. This RLDO would work well as an on-chip supply for systems with moderate to heavy current demands that require fast transient response.

The largest challenge experienced during this design scaling demonstration was in understanding RSCE. As shown in Section 2.4, at near minimum L, devices with extreme RSCE do not share the same trends as devices with moderate to no RSCE. After the RSCE trends are understood, designing in this 90 nm process becomes a matter of using the device's advantages and disadvantages to optimize circuit performance.

5.2 Proposed Future Work

5.2.1 Improvements to the RLDO

One concern with the RLDO is the small I_{LOAD} range of stability. To reduce the minimum load required for stability, three design changes are recommended for consideration to improve this range. The first consideration is implementing a minimum L unit inverter. There is some advantage to the additional A_{vt} achieved by increasing the L of the unit inverter, however, the reduced pole location becomes a limiting factor with respect to stability. Minimizing L would push the unit inverter pole at least a decade beyond the crossover frequency. This change will increase the dominant pole of LDO, so a trade-off analysis is required [8, 9].

Resizing the pass device for a smaller maximum I_{LOAD} should also be a considered design change. Decreasing the pass device would reduce its parasitic capacitances, increasing P_{out}. However, this change will increase P_{ra} more than P_{out}, due to the Miller multiplication of $C_{GD,PASS}$. C_{Miller} would likely now be required and would partially negate the reduced pass device parasitics, but the increase in P_{ra} and P_{out} will result in an increased loop bandwidth. Additionally, adding R_{Null} in series with C_{Miller}, the RHP zero can be turned into an LHP zero which could be strategically located to ensure stability, partially negating P_{out}. Again, additional trade-off analysis is required to make this change [9].

The final design change consideration is the implementation of layout approaches to further reduce parasitics. The primary source for layout-associated parasitics in this design is the metal array connecting the source and drain of the pass device to pads. To mitigate the electromigration and ESR concerns, the pass device metal array has wide metal traces with generous amounts of vias. Optimization of these traces could be considered to maintain electromigration and ESR mitigation and reduce the associated parasitic capacitances. In addition to this, implementing a compact layout design for all other components would further reduce layout-associated parasitics.

5.2.2 Improvements to Design Guide for RSCE

As mentioned in Section 2.4, the ringamp design guide is not accurate for processes with significant RSCE, because the devices do not follow typical short channel trends at near minimum L and the extreme variations in λ over V_{GS}. The ringamp design guide and design assistance scripts provide a strong resource for ringamp designers working in processes without significant RSCE. Sangid provided a 65 nm simulation example, in his dissertation, to support this point [9]. Despite this, modifications to the design guide and design assistance script are required for designing in a process with significant RSCE. Therefore, a proposed future scope of work would be to expand upon the ringamp design guide and design assistance scripts to address RSCE concerns. The revision to the design guide would ideally maintain the original flow chart and design guidance, as it stands up well when RSCE is non-existent or minimal. However, a step to check for RSCE should be added at the beginning and then direct the reader to alternate guidance for designing ringamps in RSCE processes.

5.2.3 Improvements to Multi-Loop RLDO

There are several challenges associated with the RLDOE that are not yet solved. For instance, there is no control for starting the RLDO loop upon detection of a fast transient load event, which would need to be at least as fast as the fastest expected transient. If fast transient load events are predictable, this could be implemented with a clocked control scheme. However, if the events occur randomly, then a control scheme is much more complex. Additionally, the RLDOE requires an on-chip current reference for the CMOTA and a clock generator that is capable of generating the highly asymmetrical sample and amplify clock signals. These required circuits will likely cause a non-trivial reduction in both FOMs, due to the increase in I_Q.

Another approach to a multi-loop ringamp-based LDO is a time-interleaved RLDO, similar to [18]. This approach requires an additional first-stage inverter, with respect to the RLDO loop shown in Figure 3.2. This LDO would always have an active amplifier with high loop gain, high loop bandwidth, and high slew rate. Also, this LDO does not have a period where the output is unregulated, as it is always sampling and always amplifying, except

momentarily when switching between the two RLDO loops. An on-chip clock generator is required, but the clock can now be symmetrical, which is a simpler circuit. The additional first-stage inverter and clock generator are the only components that would impact the I_Q. This increase in I_Q is also non-trivial, but it could be justified due to the overall performance boost and the design simplicity.

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Appendix

Appendix A

Cadence Layout Figures

The fabricated 90 nm RLDO Cadence® layouts are shown in Figures A.1 to A.5.

- Figure A.1 – Ringamp error amplifier
- Figure A.2 – Pseudo-Differential Switch Driver
- Figure A.3 – High Impedance Transmission Gate
- Figure A.4 – Reduced Impedance Transmission Gate
- Figure A.5 – Pass device

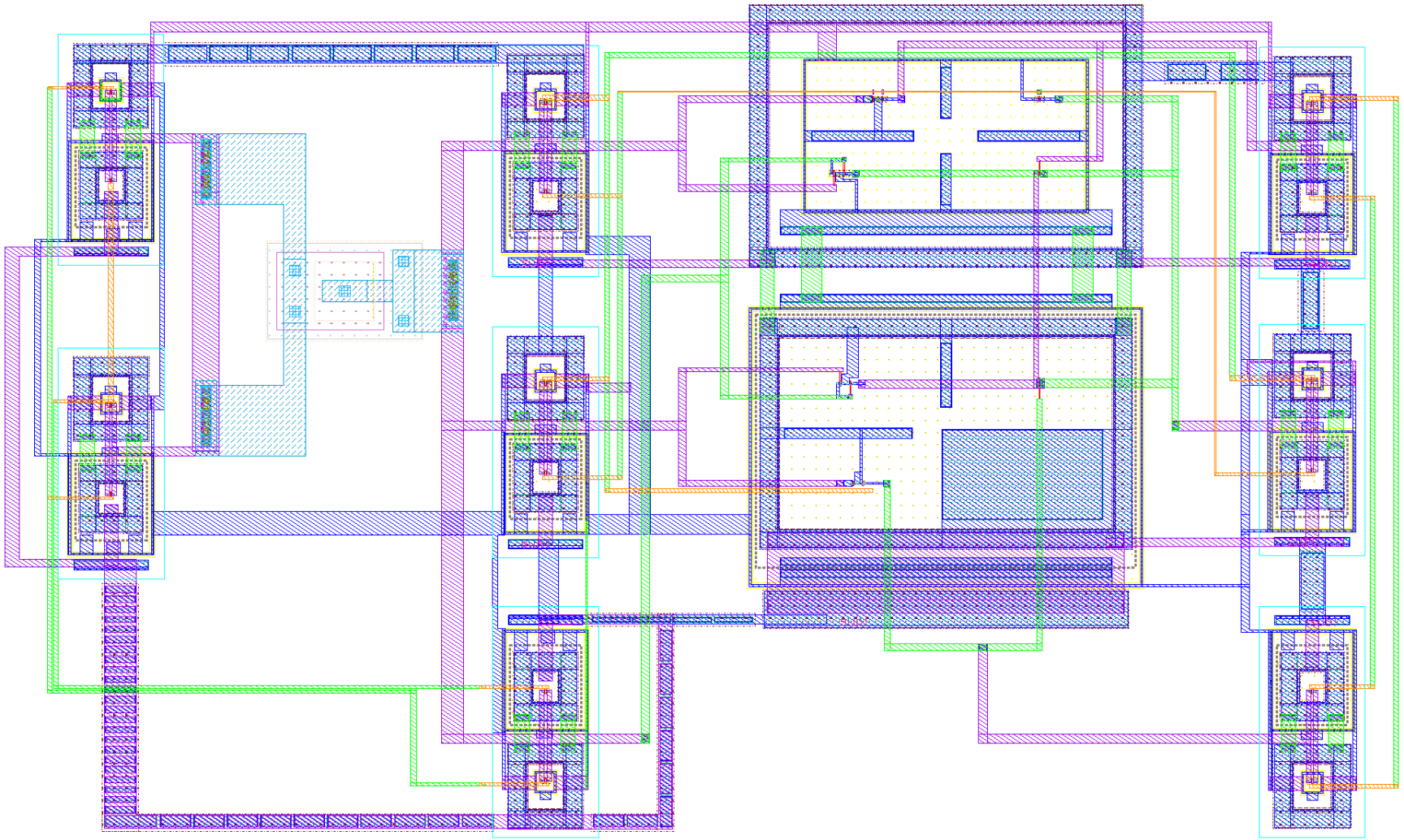

Figure A.1: 90 nm ringamp error amplifier Cadence® layout image (141.7 µm x 90.8 µm)

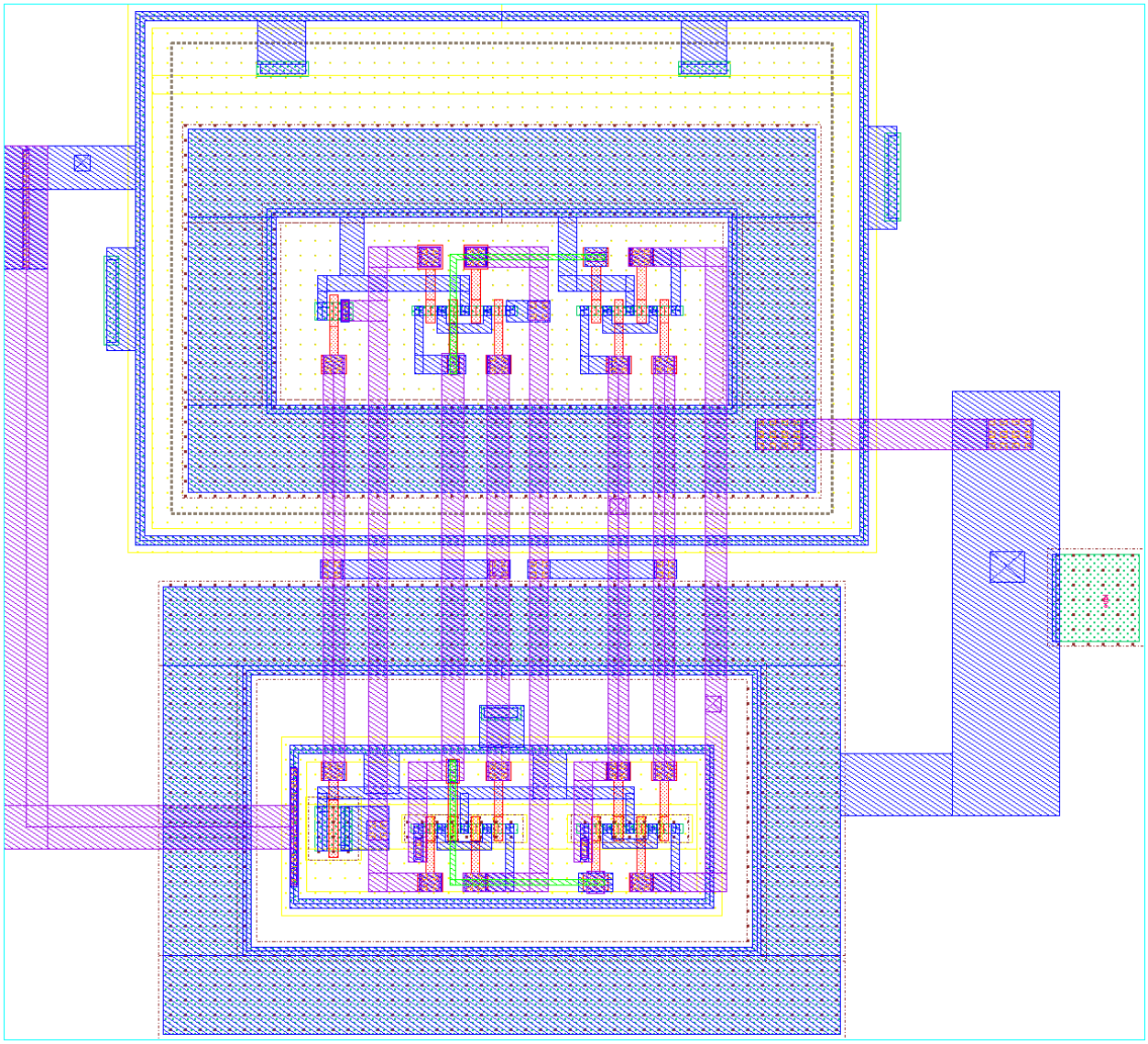

Figure A.2: 90 nm pseudo-differential switch driver Cadence® layout image (23.8 µm x 23.6 µm)

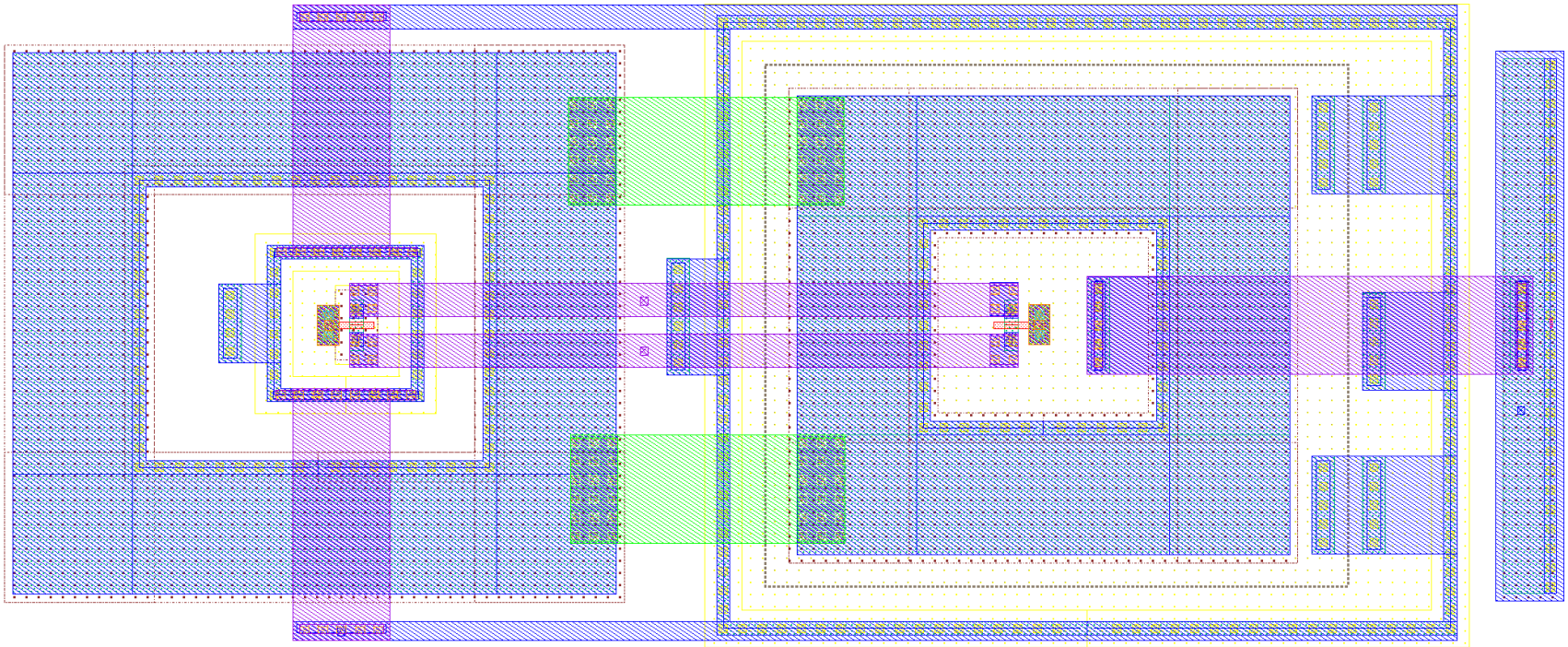

Figure A.3: 90 nm high impedance transmission gate Cadence® layout image (23.4 µm x 9.62 µm)

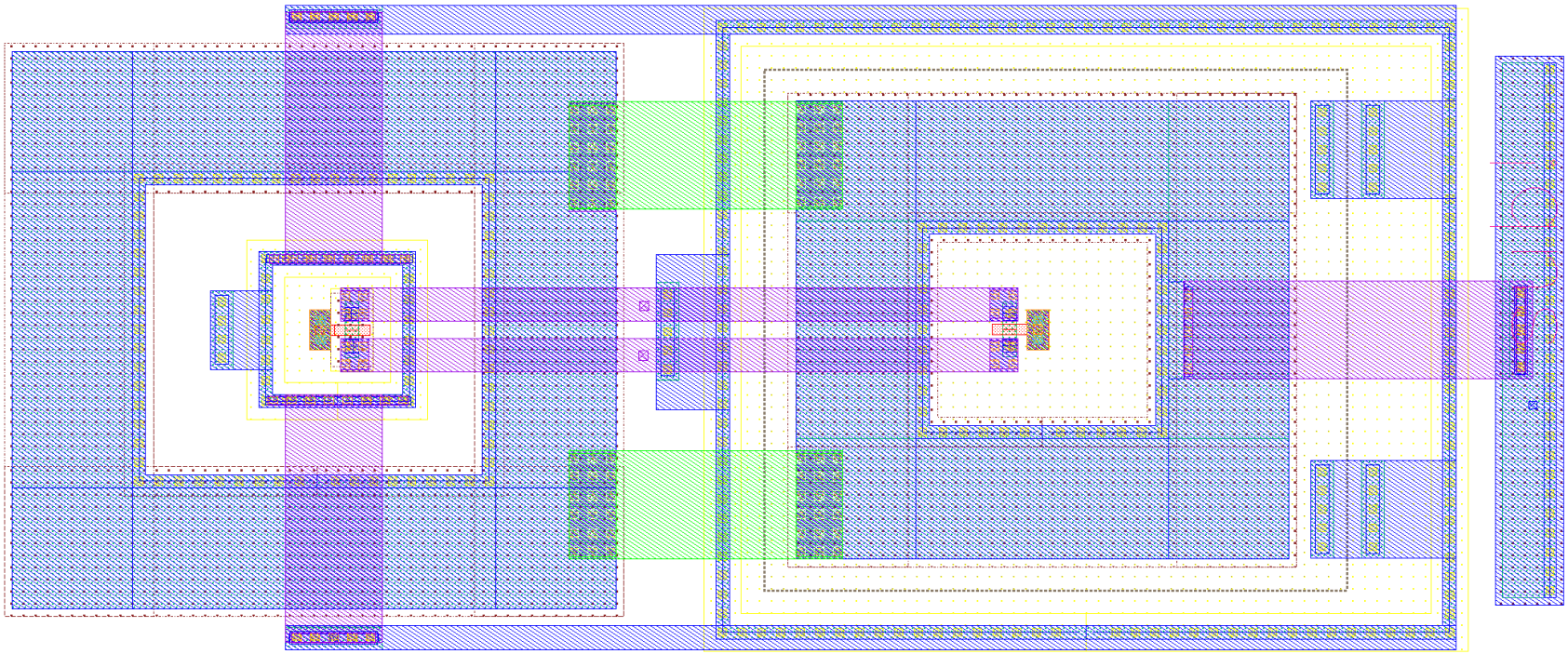

Figure A.4: 90 nm reduced impedance transmission gate Cadence® layout image (23.4 µm x 9.68 µm)

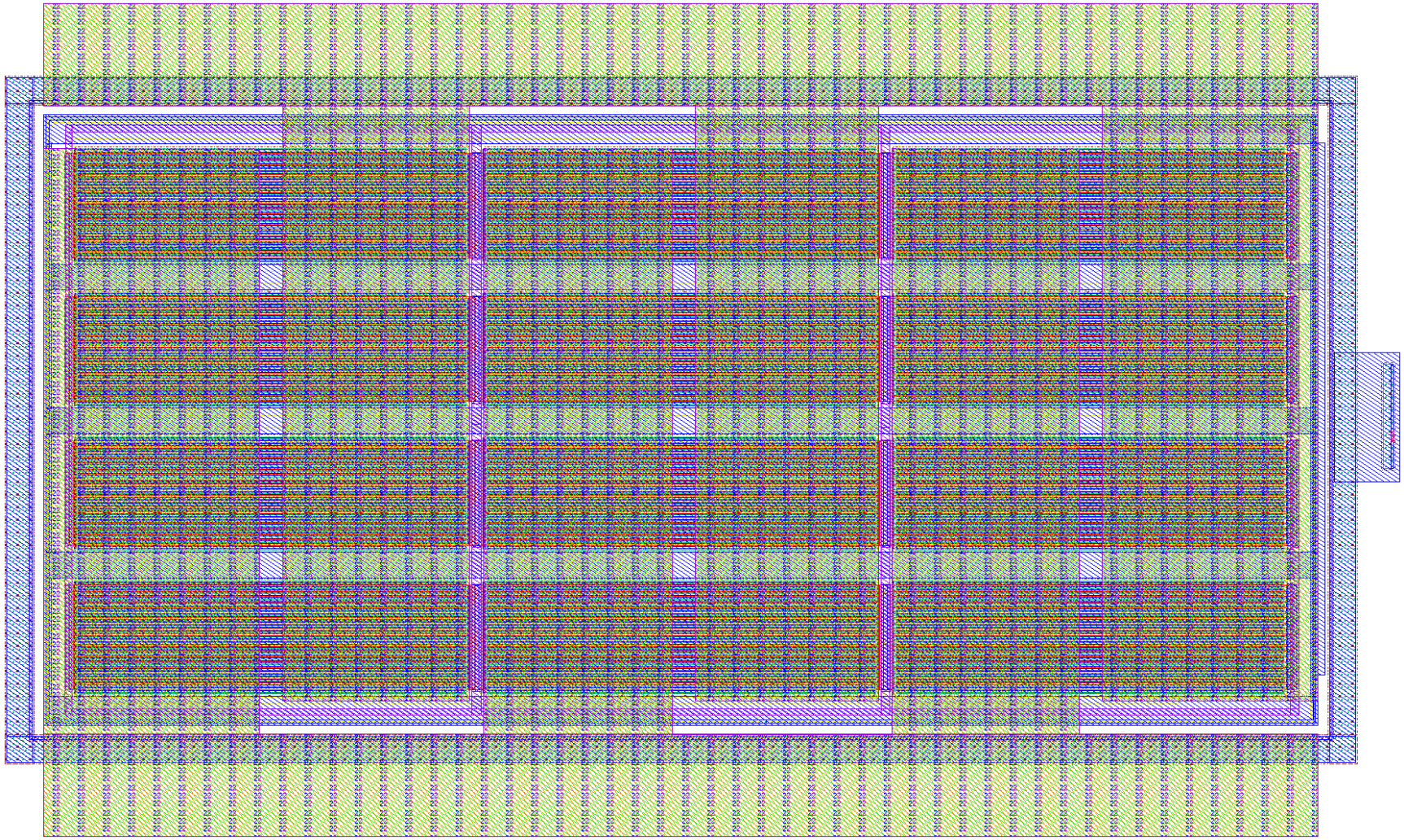

Figure A.5: Pass Device Cadence® layout image (107.3 µm x 47.0 µm)

Appendix B

Additional Simulation Figures

Additional simulation and PEX results are shown in Figures B.1 to B.4.

- Figure B.1 – Transient current load step results from 2 mA to 100 mA
- Figure B.2 – Transient current load step results from 2 mA to 50 mA
- Figure B.3 – Transient current load step results from 2 mA to 50 mA
- Figure B.4 – Power supply rejection results

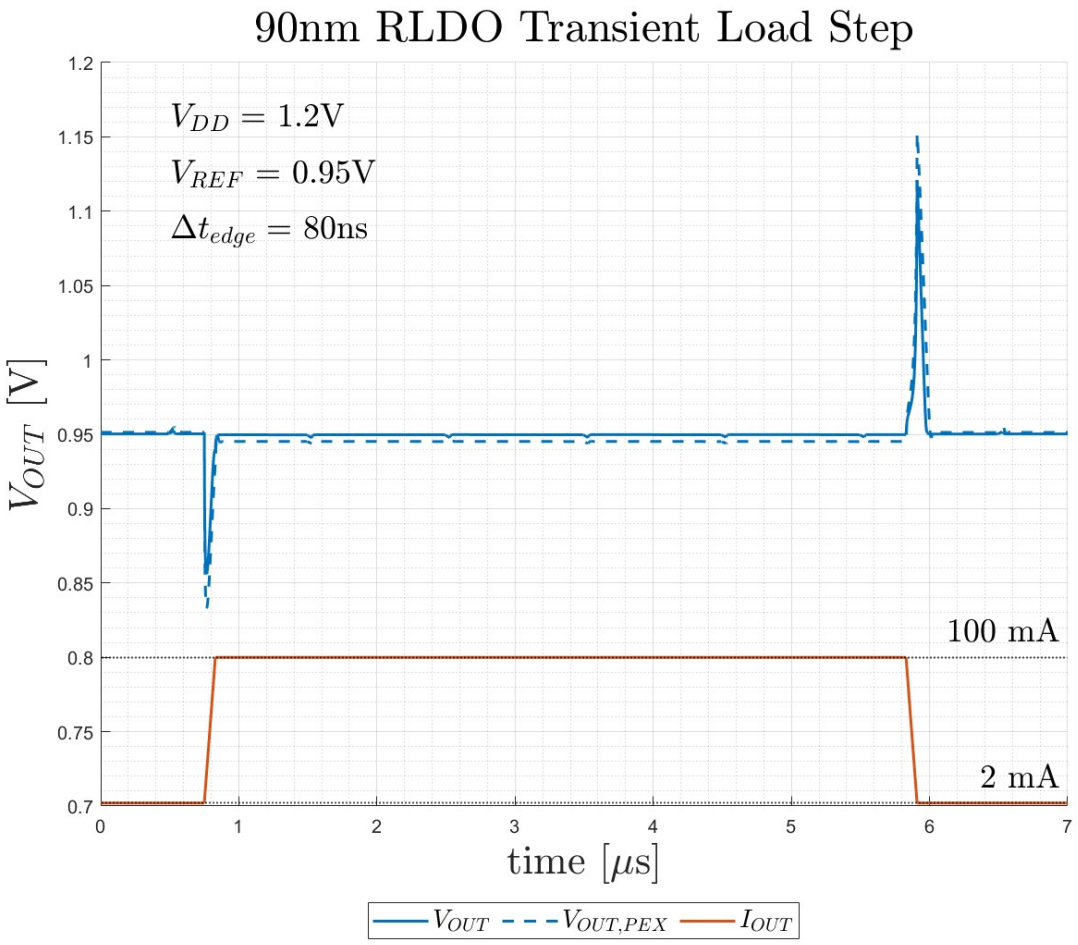

Figure B.1: 90 nm RLDO simulated transient current load step results from 2 mA to 100 mA with PEX

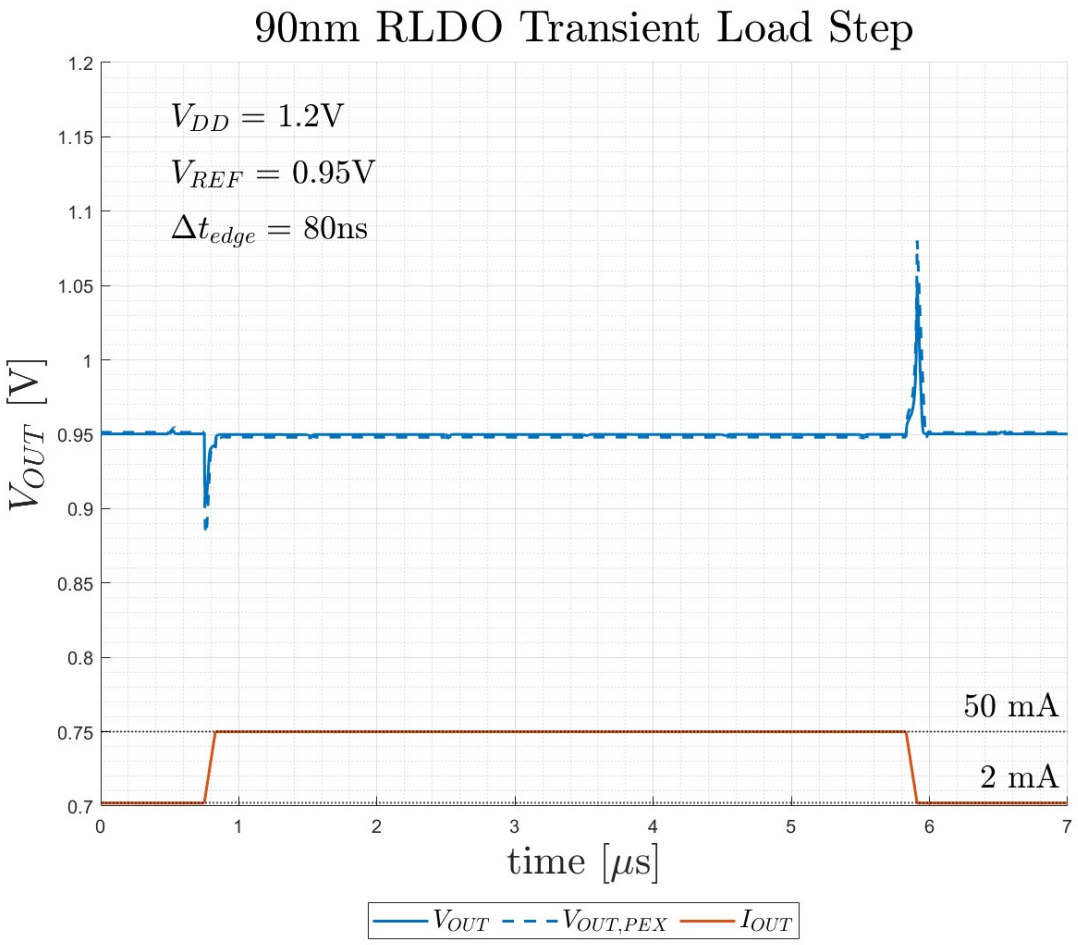

Figure B.2: 90 nm RLDO simulated transient current load step results from 2 mA to 50 mA with PEX

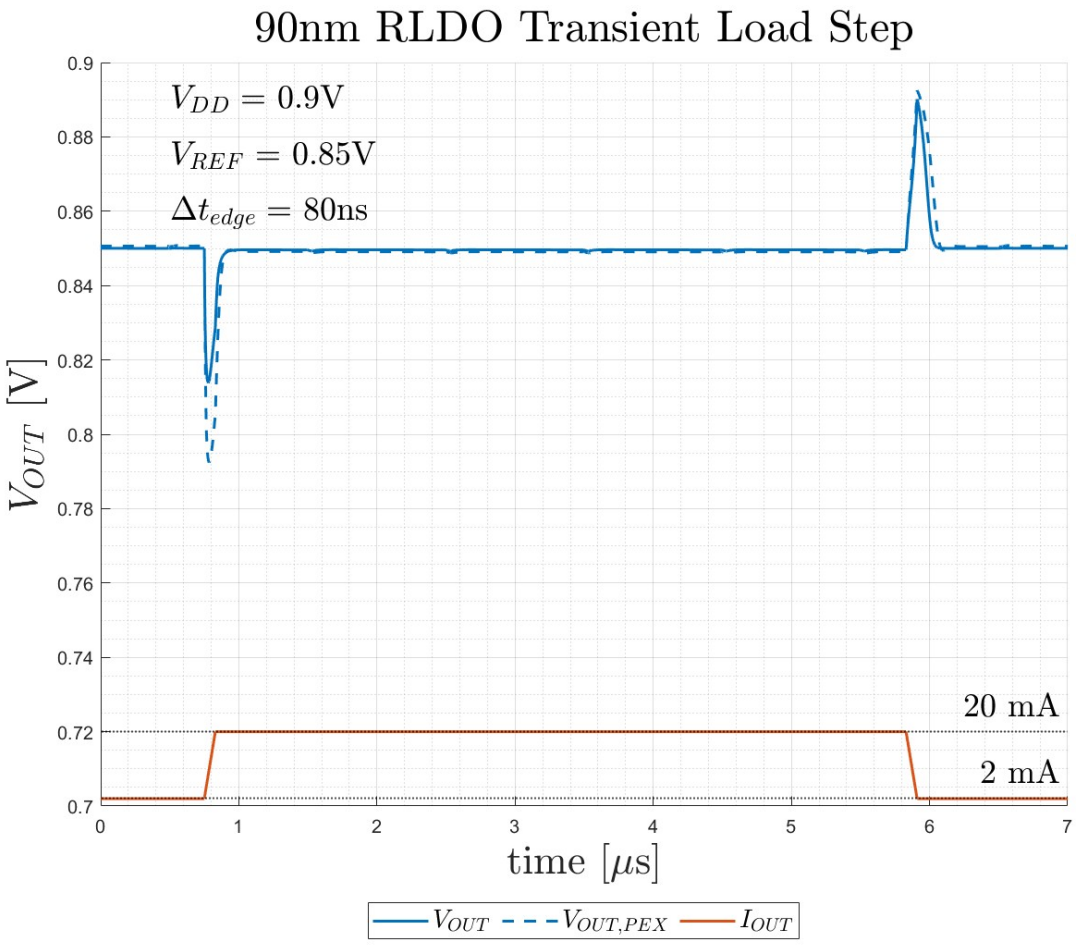

Figure B.3: 90 nm RLDO simulated transient current load step results from 2 mA to 20 mA with PEX and a reduced V_{DD}

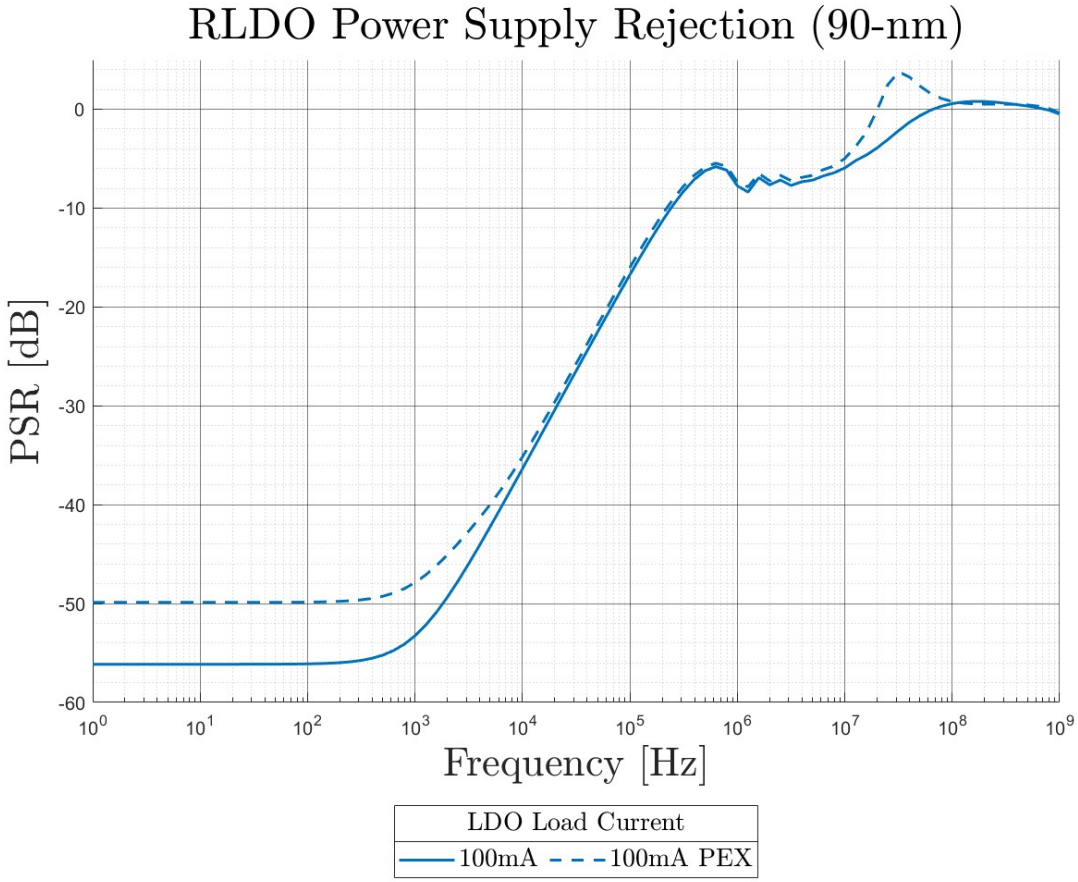

Figure B.4: 90 nm RLDO simulated power supply rejection results with PEX at $I_{LOAD} = 100\,\text{mA}$

Appendix C

90 nm RLDO Experimental Transient Load Step Figures

The RLDO experimental transient current load step results are shown in Figures C.1 to C.12.

- Figure C.1 – Transient current load step results from 2 mA to 100 mA for Chip A
- Figure C.2 – Transient current load step results from 2 mA to 100 mA for Chip B
- Figure C.3 – Transient current load step results from 2 mA to 100 mA for Chip C
- Figure C.4 – Transient current load step results from 2 mA to 100 mA for Chip D
- Figure C.5 – Transient current load step results from 2 mA to 50 mA for Chip A
- Figure C.6 – Transient current load step results from 2 mA to 50 mA for Chip B
- Figure C.7 – Transient current load step results from 2 mA to 50 mA for Chip C
- Figure C.8 – Transient current load step results from 2 mA to 50 mA for Chip D
- Figure C.9 – Transient current load step results from 2 mA to 20 mA for Chip A
- Figure C.10 – Transient current load step results from 2 mA to 20 mA for Chip B
- Figure C.11 – Transient current load step results from 2 mA to 20 mA for Chip C
- Figure C.12 – Transient current load step results from 2 mA to 20 mA for Chip D

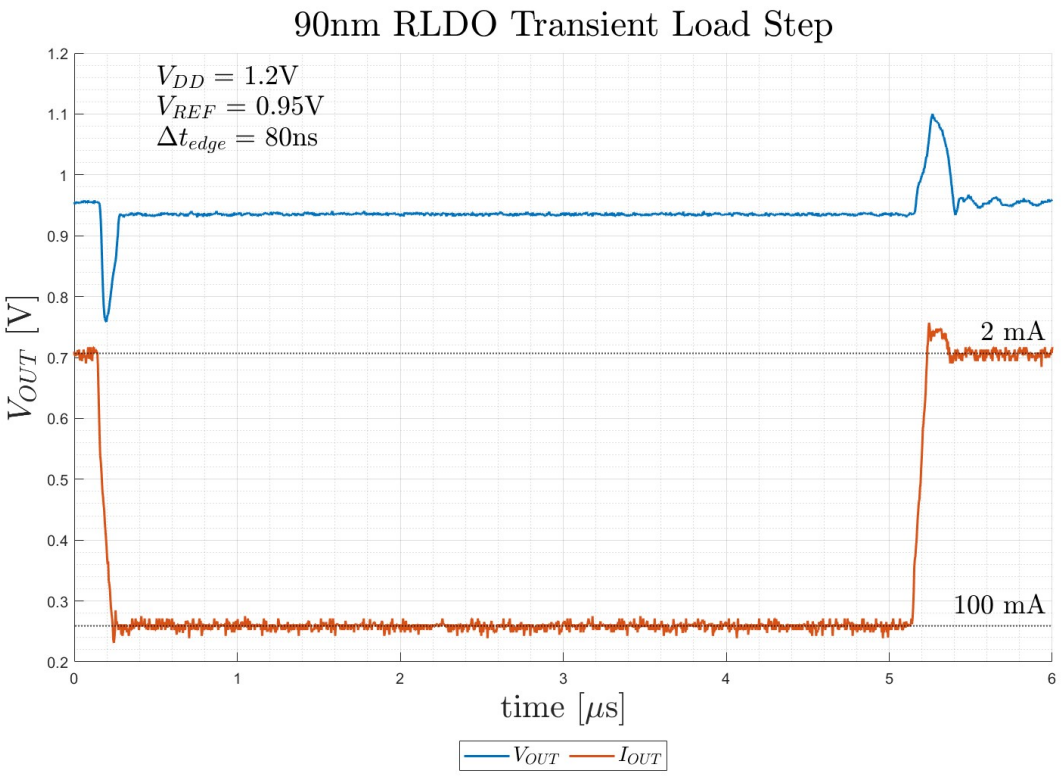

Figure C.1: Chip A RLDO experimental transient current load step results from 2 mA to 100 mA

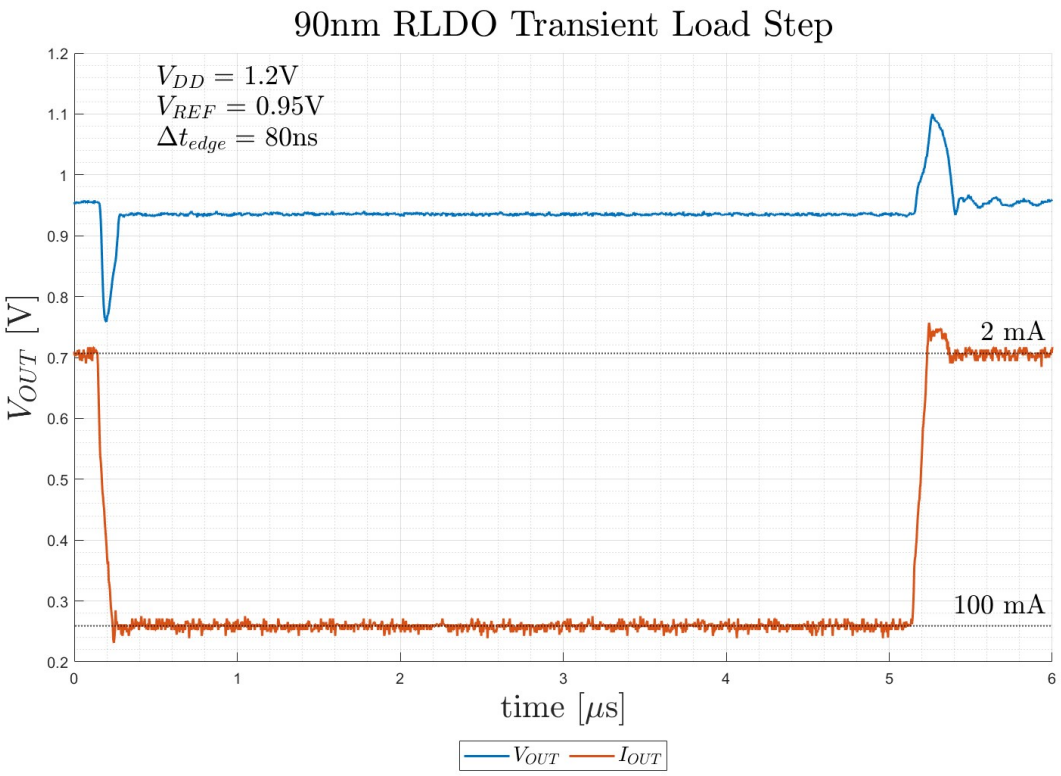

Figure C.2: Chip B RLDO experimental transient current load step results from 2 mA to 100 mA

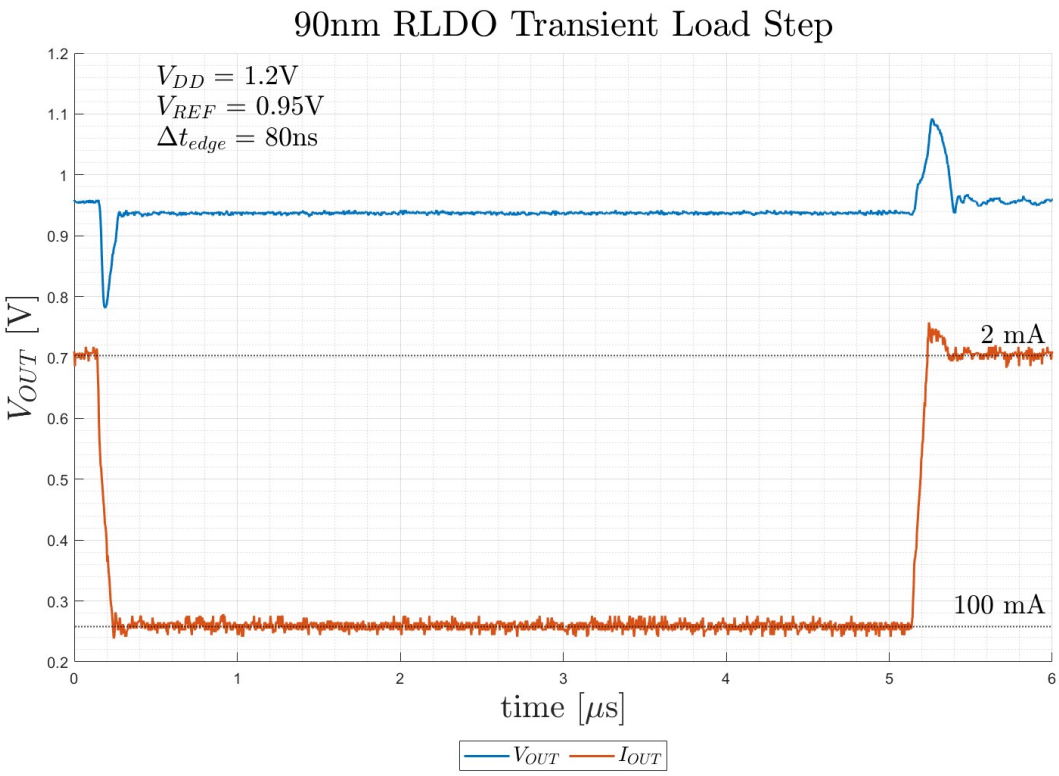

Figure C.3: Chip C RLDO experimental transient current load step results from 2 mA to 100 mA

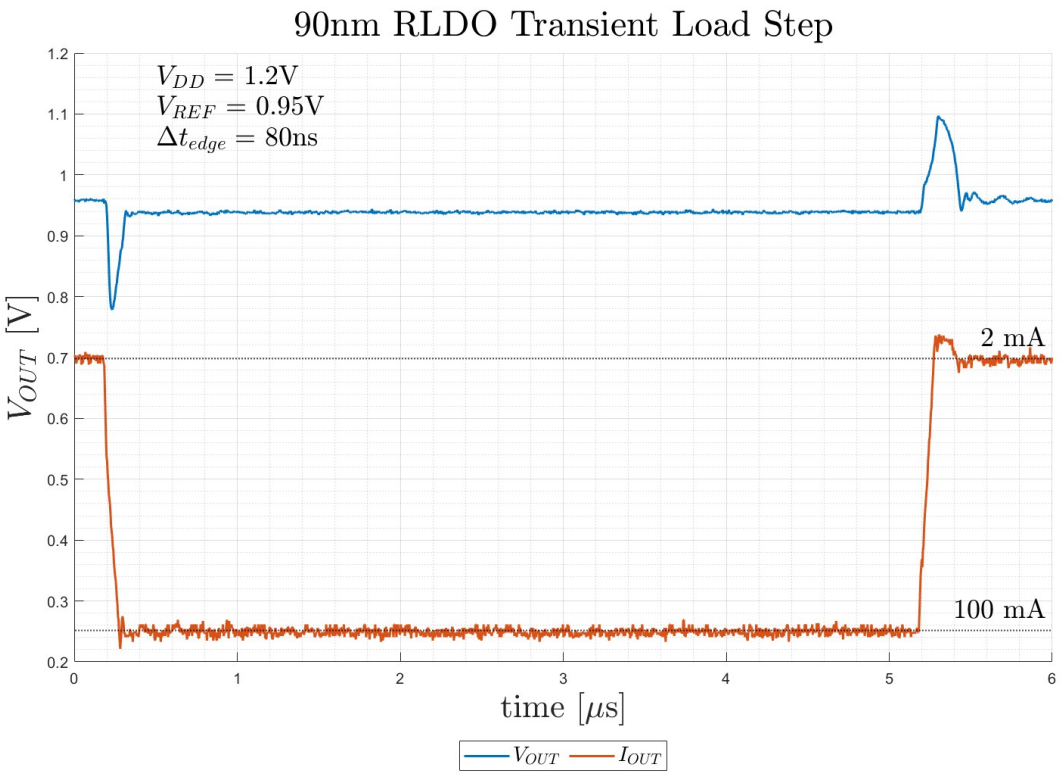

Figure C.4: Chip D RLDO experimental transient current load step results from 2 mA to 100 mA

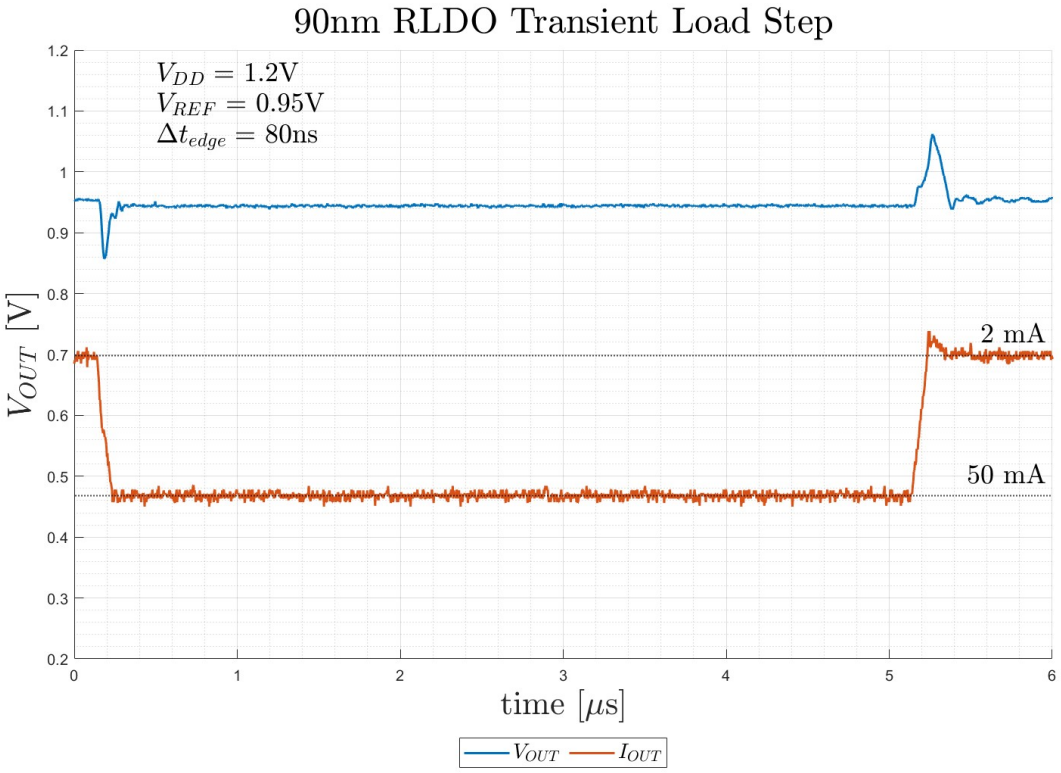

Figure C.5: Chip A RLDO experimental transient current load step results from 2 mA to 50 mA

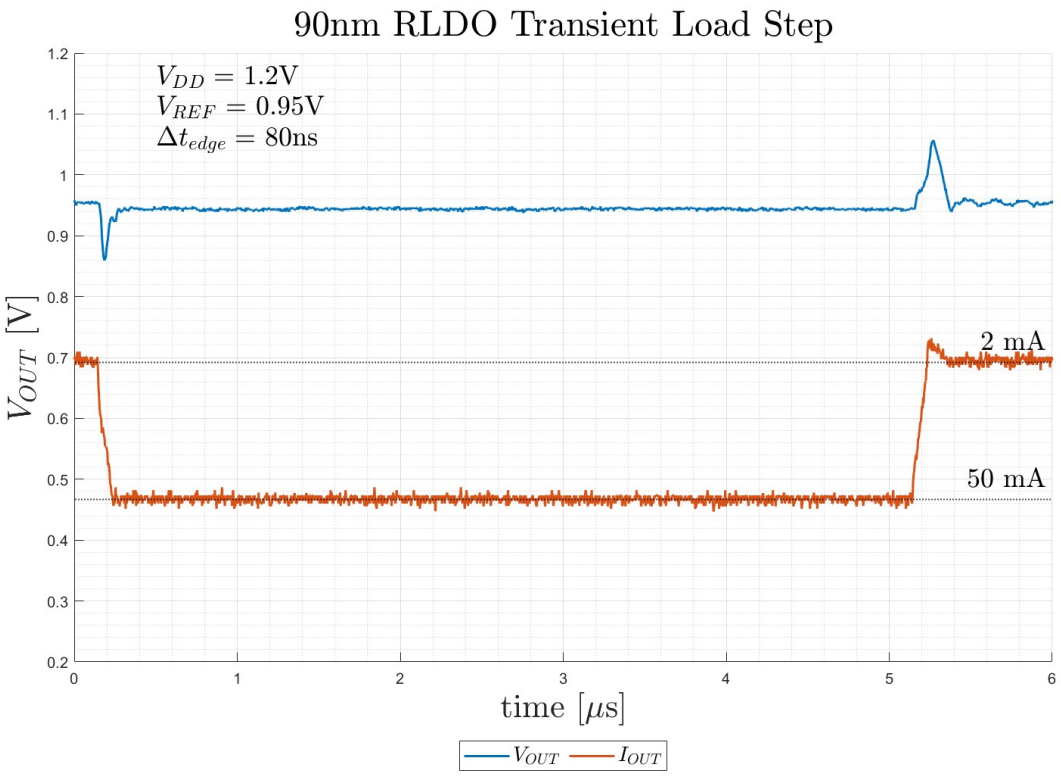

Figure C.6: Chip B RLDO experimental transient current load step results from 2 mA to 50 mA

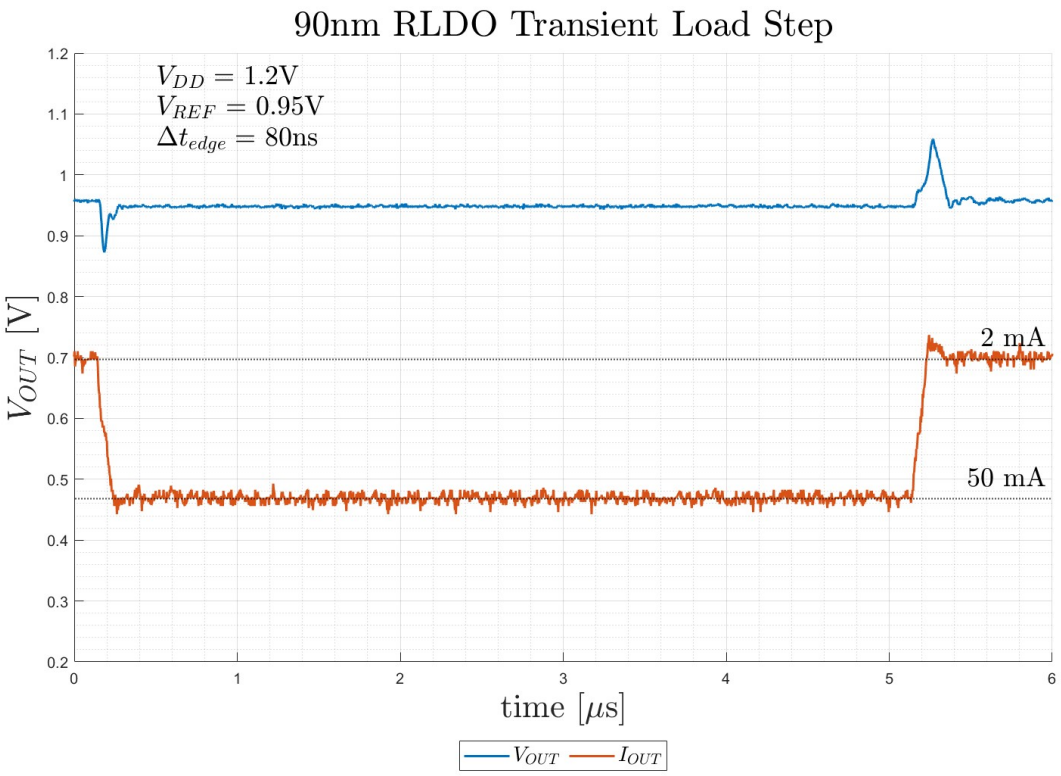

Figure C.7: Chip C RLDO experimental transient current load step results from 2 mA to 50 mA

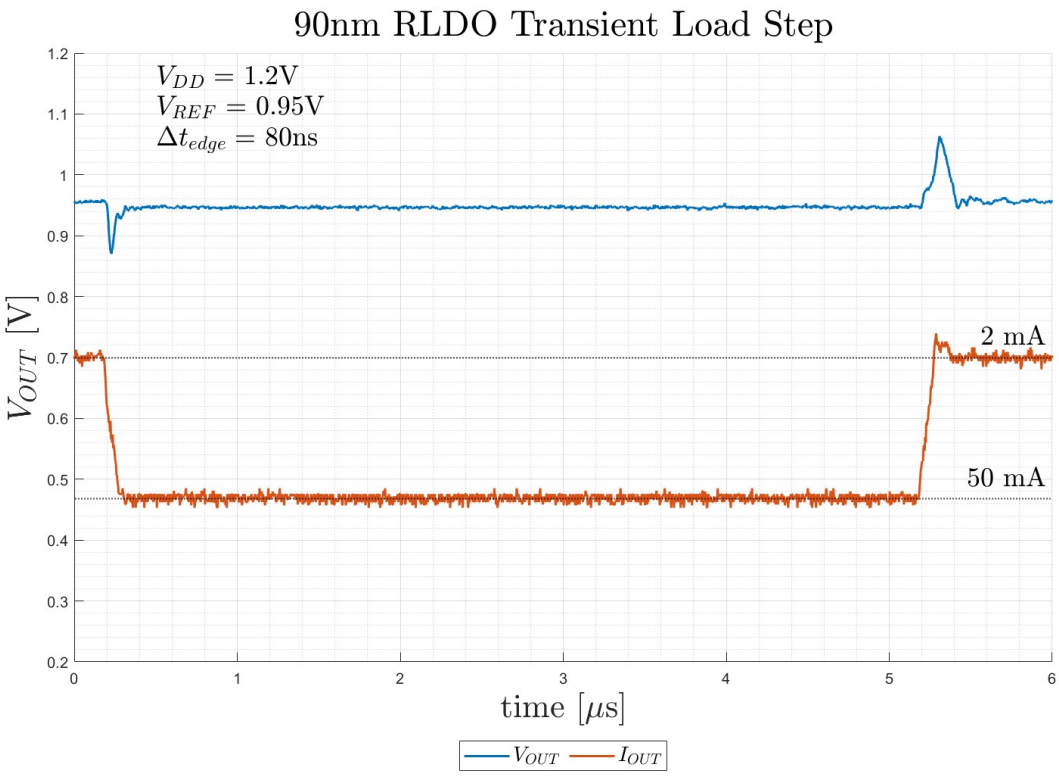

Figure C.8: Chip D RLDO experimental transient current load step results from 2 mA to 50 mA

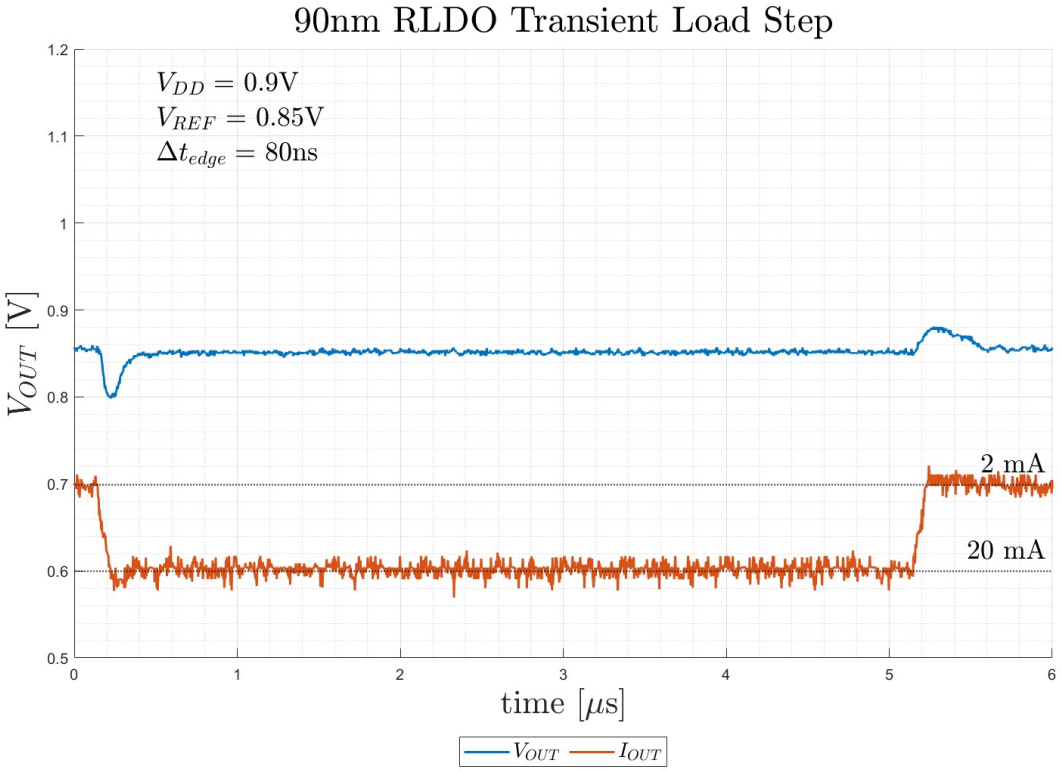

Figure C.9: Chip A RLDO experimental transient current load step results from 2 mA to 20 mA with reduced V_{DD}

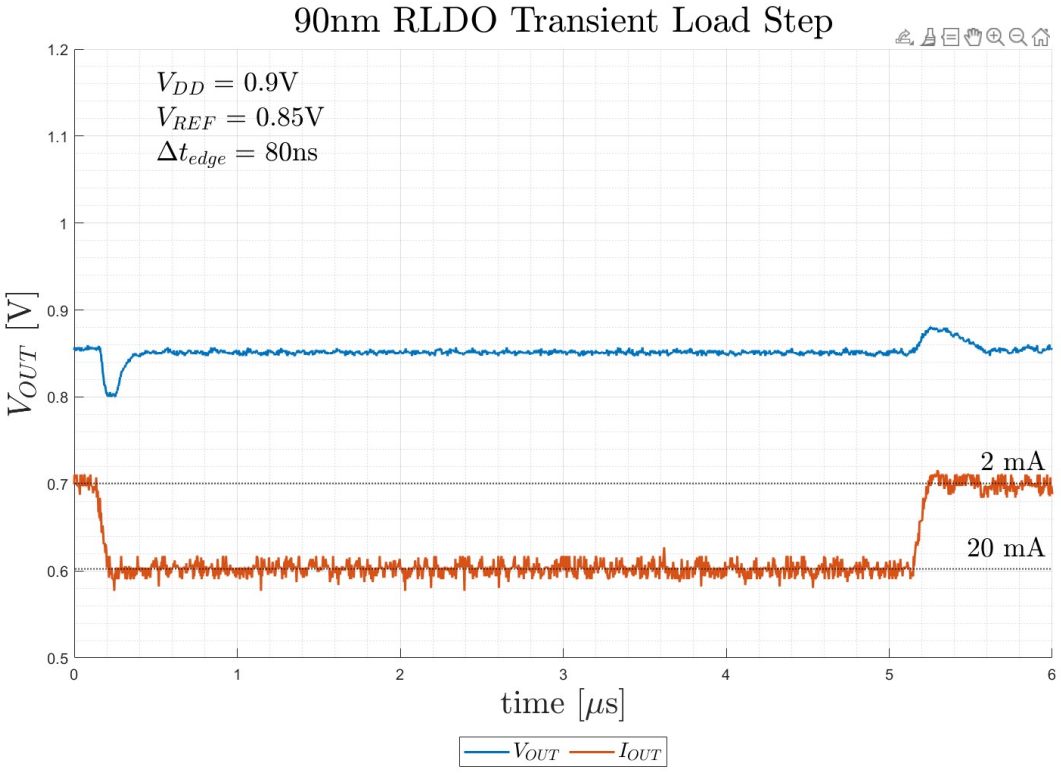

Figure C.10: Chip B RLDO experimental transient current load step results from 2 mA to 20 mA with reduced V_{DD}

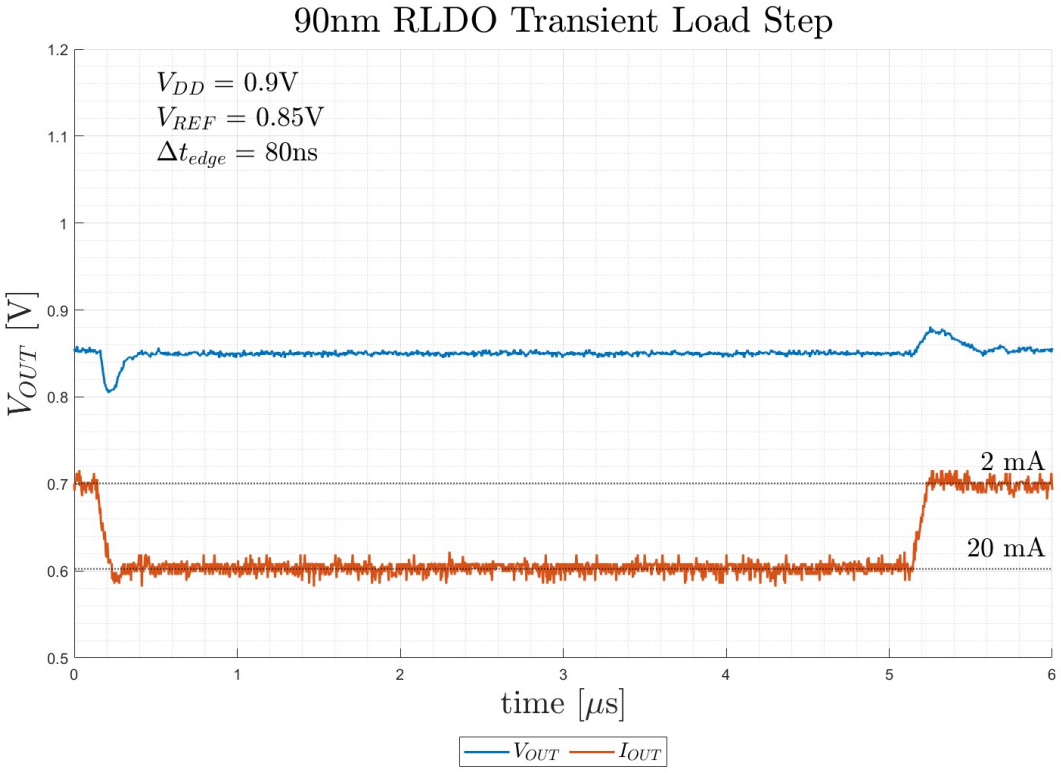

Figure C.11: Chip C RLDO experimental transient current load step results from 2 mA to 20 mA with reduced V_{DD}

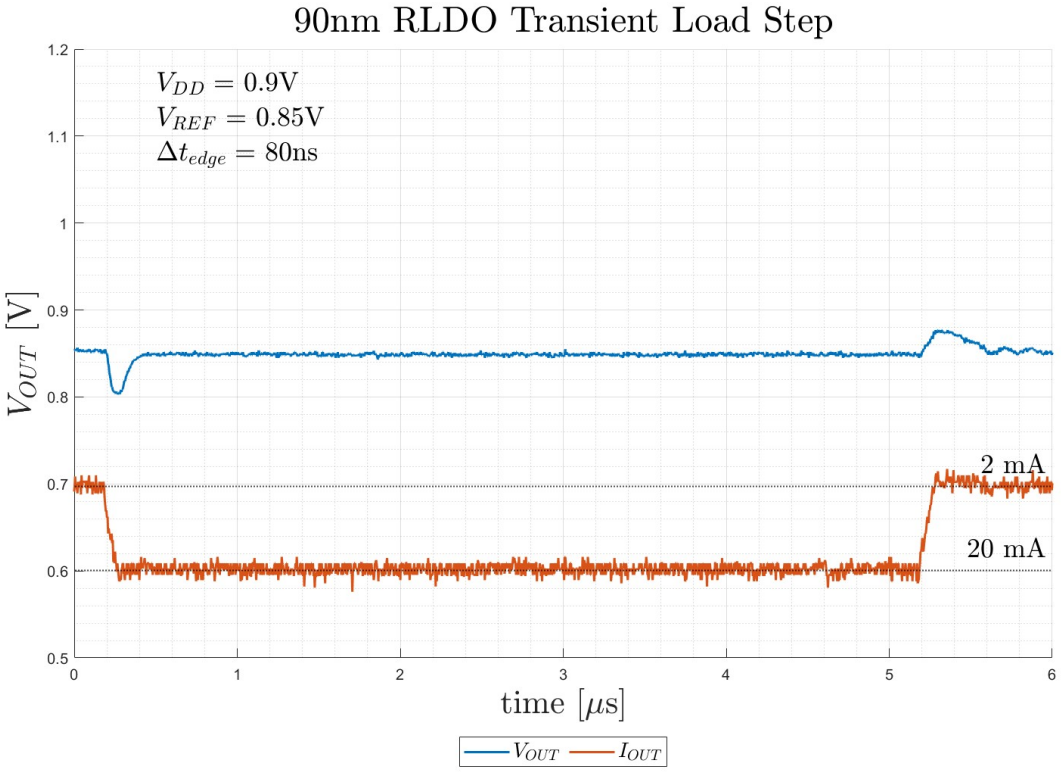

Figure C.12: Chip D RLDO experimental transient current load step results from 2 mA to 20 mA with reduced V_{DD}

Vita

Steven Bradley Corum was born in 1987 in Morristown, TN, where he has spent most of his life. He graduated from Morristown East High School in 2005. His undergraduate education began at Walters State Community College, also in Morristown, TN, and concluded at Tennessee Technological University (TTU) in Cookeville, TN, in 2012. During his time at TTU, he worked for Dr. Robert Qiu in the Wireless Network Research Laboratory as an undergraduate research assistant. His work involved using software-defined radio for RADAR applications, such as target detection and imaging.

In 2013, he commenced his career at MS Technology Inc., where he was contracted to the Uranium Processing Facility (UPF) design project for the Y-12 National Security Complex, working as a Control Systems Engineer. By 2017, he had become a full-time employee of Bechtel National Inc., continuing his role as a Control Systems Engineer on the UPF project. In 2021, he left Bechtel and the UPF project to pursue graduate school at the University of Tennessee, Knoxville.

At the start of 2022, he joined Dr. Benjamin J. Blalock's team at the Integrated Circuits and Systems Laboratory (ICASL) in the Electrical Engineering and Computer Science department of The University of Tennessee, Knoxville. His work at ICASL includes two distinct NASA projects, COLDTech and LuSTR. Both projects involve the design of extreme environment electronics. LuSTR's design has lunar-centric radiation and temperature profiles, and is primarily based on SiGe BiCMOS design but has limited CMOS design. COLDTech, on the other hand, is tailored for Europa and is solely based on SiGe BiCMOS technology. As a Ph.D. student, he continues to research instrumentation-quality ring amplifier based analog-to-digital converters for extreme environments.