A DSP Controlled Multi-Level Inverter Providing DC-Link Voltage Balancing, Ride-Through Enhancement and Common-Mode Voltage Elimination

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A Dissertation of

Doctor of Philosophy

Oregon State University

AN ABSTRACT OF THE DISSERTATION OF

Shaoan Dai for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on October 2, 2003.

Title: A DSP Controlled Multi-Level Inverter Providing DC-Link Voltage Balancing, Ride-Through Enhancement and Common-Mode Voltage Elimination.

Abstract approved:

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Annette von Jouanne

With the development of high performance power electronic and semiconductor technologies, Adjustable Speed Drive (ASD) systems are increasingly applied in residential, commercial and industrial applications. Due to the advantages at higher power ratings, the three-level Neutral-Point-Clamped (NPC) Voltage Source Inverter (VSI) is being employed in industrial and traction applications, static VAR compensation systems, active filtering and utility interconnection applications.

The NPC-VSI is suitable for high voltage and high power applications due to the use of series-connected switching devices. Furthermore, Electro Magnetic Interference (EMI) and the voltage stress across the inverter switches and load can be reduced because of increased levels of the output voltages compared with the conventional 2-level inverters. However, an excessively high voltage may be applied to switching devices if the Neutral-Point (NP) voltage varies from the center voltage of the dc-bus voltage. This is the inherent problem caused by the unbalanced switching states of the NPC inverter. In addition, common-mode voltages may be generated by the NP voltage variation. In response to these drawbacks, various strategies including carrier-based PWM schemes and Space Vector Modulation (SVM) based PWM schemes have been proposed to balance the NP voltage. All the above methods can operate successfully under given operating conditions, but they do result in limitations in the performance.

The major objective of this research is to investigate and enhance the application issues of the NPC-VSI including balancing the dc-bus voltage, in addition to reducing

the common-mode voltage and improving the ride-through ability. Therefore, analysis of the NP voltage generation is presented and existing NP voltage balancing techniques are evaluated. It is found that common-mode voltage cancellation and NP voltage control are difficult to be realized at the same time, by the arithmetic methods. Thus, a hardware method to keep the NP voltage balanced is proposed and implemented while the mitigation of common-mode voltage is being implemented by an arithmetic method. In addition, the ride-through ability is also enhanced through the proposed topology. Correlation of the simulation and experimental results are provided.

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by

Shaoan Dai

A DISSERTATION

Submitted to

Oregon State University

In partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented October 2, 2003

Commencement June 2004

Doctor of Philosophy dissertation of Shaoan Dai presented on October 2, 2003

APPROVED:

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Dean of Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Shaoan Dai, Author

To my mother

ACKNOWLEDGEMENTS

I would like to thank my major professor, Dr. Annette von Jouanne, for her advice and support during the years of my study at Oregon State University. Life blessed me with the opportunity to meet Dr. Annette von Jouanne.

Many thanks and appreciation to the members of my graduate committee: Dr. Alan Wallace, Dr. Gabor C. Temes, Dr. Kartikeya Mayaram and Dr. Jon Herlocker for their guidance and advice in the completion of this dissertation.

I am very grateful to Dr. Haoran Zhang for his advice, help and friendship. Also, I wish to thank the International Industrial Division of Toshiba for the generous hardware contributions that enable the construction of the experimental system. Many thanks to my friends at Oregon State University for their valuable input and assistance, comments and help.

Special thanks to my wife, Hui Ren and my son, Wei Dai, for their support and encouragement of my study. I am forever grateful to my parents, Xueshan Dai and Junxia Li for their gently counsel and support at each turn of the road.

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A DSP CONTROLLED MULTI-LEVEL INVERTER PROVIDING DC-LINK VOLTAGE BALANCING, RIDE-THROUGH ENHANCEMENT AND COMMON-MODE VOLTAGE ELIMINATION

1 INTRODUCTION

1.1 Background

More and more Adjustable Speed Drives (ASDs) are being applied for motor control in commercial and industrial facilities to improve efficiency, process control and productivity. In the ASD market, most ASDs are used to save on energy costs. However, ASDs are also often applied to improve process control. The following data reflects the ASD market penetration according to [1].

USA –18% in currently sold and 12% installed

Europe –24% sold and 19% installed

Japan –45% sold and 38% installed

In the future, an even higher percentage of motors driven by ASDs will appear in commercial and industrial applications.

The ASD systems can be categorized into two primary types: DC and AC drive systems. The DC motors need more maintenance than AC motors because of the commutator and brushes. Furthermore, high power DC motors are more difficult to design than AC motors. AC motors, on the other hand, are more robust, have a lower cost and require less maintenance. For these reasons, ASD systems are more applied to AC or brushless motors even if ASD systems with DC motors have a better performance.

The conventional topology for the control of AC motors is shown in Fig.1-1. ASD systems mainly consist of inverters. With the development of power electronics, high speed switching devices such as the Insulated Gate Bipolar Transistors (IGBTs) and the Insulated Gate Commutated Thyristors (IGCTs) and complex micro controllers

(such as DSP controllers) are widely applied in inverter systems. Large power and high performance ASDs have been developed for industrial applications. In oil field applications, ASDs are widely applied to pumps for saving energy and improving efficiency. In chemical plants, ASDs are being used to provide process control to improve the productivity and control performance. ASDs are also used in pressure control with fans in the central air-conditioning systems.

ASD inverter topologies can be divided into conventional two-level inverters, and multi-level inverters. Most commercial inverters are two-level inverters due to cost considerations. The multi-level inverter topologies are mostly applied to high voltage and high power inverter designs. Considering the complexity of multi-level inverters, very few multi-level inverters with more than four levels have been manufactured. The first Neutral-Point-Clamped (NPC) Inverter topology was proposed by A. Nabae [2] in 1981. After that, several Multi-Level Inverter (MLI) topologies were investigated.

1.2 Conventional Inverter

Conventional inverters are usually referred to as two-level inverters. The common topology is labeled in Fig.1-1. It is widely applied in low power (1-200kW), low voltage (208V, 460V, 575V) commercial inverters.

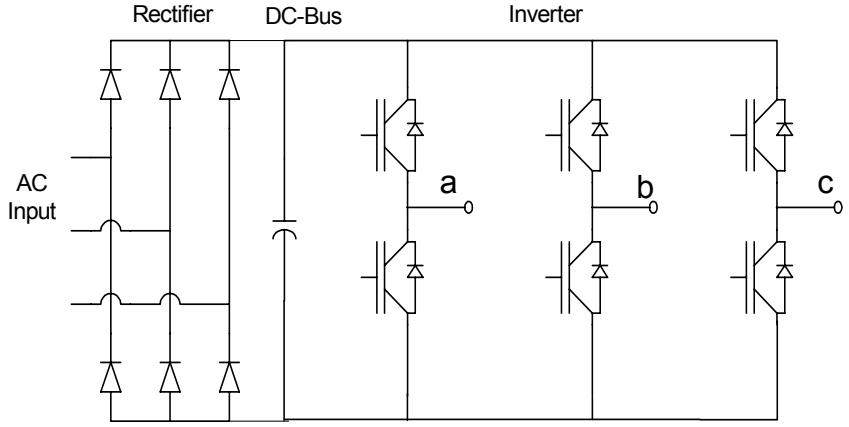

Fig. 1.1 The conventional ASD topology.

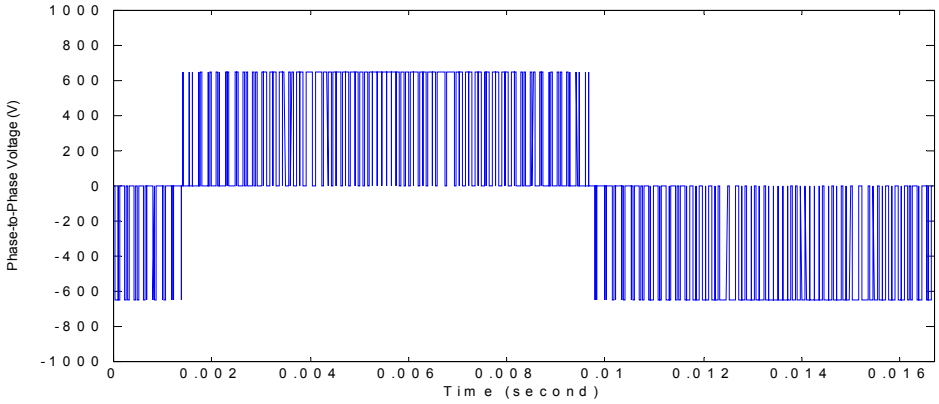

Fig. 1.2 The output waveforms of the conventional inverter.

Fig.1.2 shows the 3-step waveforms of the PWM output voltage of a two-level inverter. From Fig.1.1 and Fig.1.2, it is evident that the voltages across the switching devices in conventional two-level inverters are higher than Vdc, but the number of the switching devices is a minimum. So the necessary voltage ratings of switching devices in the high voltage inverters are double and, therefore, quite high. For reasons such as the ability to use low voltage rating IGBTs, low number of switching devices and a simple controller, the two-level conventional inverter topology is widely and successfully applied in low power and low voltage commercial ASD products.

1.3 Neutral-Point Clamped Inverters

The NPC inverter topology is shown in Fig.1.3. Compared with the 3-step line-to-line output waveforms of two-level conventional inverters, NPC inverters have 5-step waveforms in the line-to-line output voltage shown in Fig.1.4.

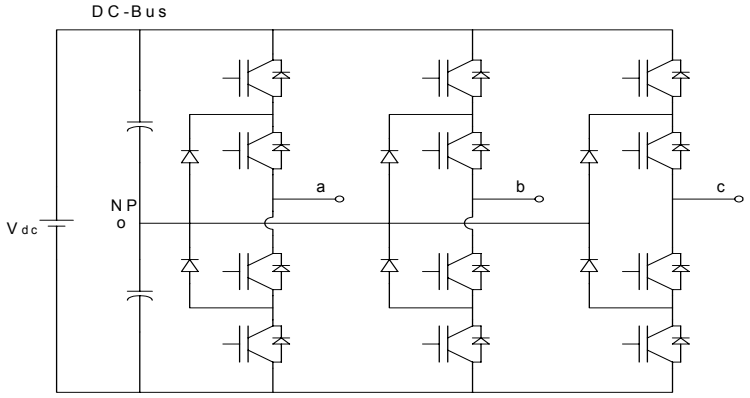

Fig. 1.3 The topology of a neutral-point clamped inverter.

Therefore, the harmonic content is less than that of conventional two-level inverters. That also means that there is reduced rate of voltage rise (*dv/dt*) in the output voltages, less current ripple and less Electro Magnetic Interference (EMI). Also, the voltage stress across the switching devices in NPC inverters is reduced to half of the dc-bus voltage for the same output voltage rating. So the NPC inverter topology can be applied in the medium voltage (2300V, 4160V, 6000V), large power (300-20,000kW) inverters. However, the number of switching devices is obviously increased. In addition, the cost for the controller and the corresponding hardware increases with the increased number of switching devices.

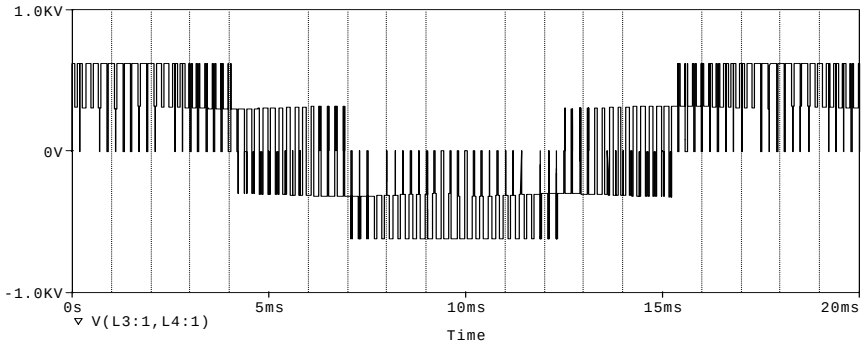

Fig. 1.4 The output line-to-line voltage waveform of a neutral-point clamped Inverter.

The main disadvantage is the Neutral-Point (NP) voltage variation problem. It is an inherent problem because the dc-bus capacitor bank consists of two series-connected sub capacitor banks as shown in Fig.1.3. When the three-phase load is not completely balanced, there will be unequal charging of the dc-bus capacitors that induces an NP voltage variation. The load unbalance and therefore the NP voltage variation can be significant during the startup of the NPC inverter driving an AC motor or when the NPC inverter drives the AC motor at a low speed. In those cases, the lower frequency NP current causes a larger NP voltage variation.

The fluctuation of the NP voltage can cause the switching devices to operate unsafely if the unbalance continues to degrade. If this happens during motor startup, the startup may sometimes fail. If this happens in the low speed operation, it can induce more distortion in the output voltage and cause the AC motor to produce torque ripple. Thus, the fluctuation of NP voltage is a very important problem that needs to be solved for NPC inverters.

1.4 Shaft Voltages and Bearing Currents

Conventional inverters and other switching mode inverters generate common-mode voltages in the motor windings because of the instantaneous unbalanced inverter outputs and unbalanced impedances of the motor. Due to PWM frequency of common voltages and capacitive coupling into the rotor, this kind of common- mode voltage will be built up as shaft voltages and can cause damaging currents to flow through the motor bearings. Bearing current is the main reason for motor bearings to fail prematurely in high frequency PWM inverter applications. The investigations of bearing current effects on motor premature bearing failures were discussed in [3-13].

1.5 Previous Work

1.5.1 Neutral-Point Voltage Balancing

The arithmetical methods to balance NP voltage variations can be categorized into modulation methods and closed-loop control methods. Many approaches relating to modulation methods were proposed and discussed in [14-20]. Some of them use the modified Sinusoidal Pulse-Width Modulation (SPWM) method by injecting the compensating NP voltage into the reference signals in order to control the dc-link voltage. The modified Space-Vector PWM (SVPWM) methods utilize the redundant voltage vectors to balance the NP voltages.

The above methods are the open-loop control techniques for reducing NP voltage variations. The closed-loop control methods induce NP voltage errors into the PWM reference signals to control the NP voltages. With these methods, a better voltage balancing can be achieved but stability problems can appear.

The above arithmetical methods are all based on introducing some form of the output zero sequence voltage information to balance the dc-link voltage. But they don't always work well at all times. The effects of NP voltage balancing are determined by the size of the dc-link capacitors and the load conditions such as modulation indices and power factor angles. Sometimes the balancing may fail during startup with low speed and heavy load, causing the drive to trip out.

1.5.2 Common-Mode Voltage Cancellation

The Common-Mode Voltage (CMV) can be cancelled by arithmetical methods or hardware active filter techniques on the inverter output stage. Some common-mode voltage cancellation or reduction with Space Vector Modulation (SVM) and modified SPWM were proposed and discussed in [3] and [8]. There are some limitations or

hardware requirements on the above methods. The effective arithmetical SVM was proposed in [3]. The modified SVM can effectively eliminate the common-mode voltage caused by the switching mode inverter in theory and considerably reduce the common-mode voltage without additional requirements of hardware in practice.

An active filter method was reported in [11]. That hardware method can effectively reduce the common-mode voltage without modifying the modulation method.

1.5.3 Bearing Current Mitigation

To mitigate bearing currents, two kinds of methods are usually employed. One is to mitigate the source, the common-mode voltage on the motor shaft, which is described as above. Another method is to bypass the bearing currents with a slipping brush or to block the bearing currents from flowing through the motor bearings by insulating them from the motor frame.

The commonly adopted techniques to bypass the bearing currents are a shaft grounding system, conducting grease and a Faraday shield [6, 7] which shields coupling into rotors. The techniques to block bearing currents are insulated bearings and journals and ceramic bearings. But there are some limitations on applying the above methods: often periodic service and maintenance are required.

1.6 Research Objectives

The common-mode voltages and NP voltage variations are the two main problems in the application of NPC inverters. Up to now, there is no arithmetical method which can solve both problems at the same time. This research is to try to balance the NP voltage by using hardware circuits, and mitigate the common-mode voltage through an arithmetical method at the same time.

2 THE PROBLEMS OF NPC INVERTER APPLICATIONS

2.1 CMV and Bearing Currents

2.1.1 Introduction

Common-mode voltages (shaft voltages), bearing currents and the causes of motor bearing failures have been widely investigated [5], [6] and [7]. Before ASDs were widely applied in the industry, shaft voltages were mainly caused by the dissymmetries of the motor magnetic field, which have decreased with improved manufacturing.

With the development of modern power electronics, the fast switching and high power rating semiconductor switching devices such as IGBTs and IGCTs are widely applied in ASDs. Also, the low cost and high performance micro-controllers or Digital Signal Processors (DSPs) make the high performance and low cost ASDs available. More and more ASDs are applied in industry to save energy, improve system efficiency and performance. The shaft voltage and bearing current problems have once more taken people's interests because the high frequency switching devices and methods induce common-mode voltage, exert high *dv/dt* and high voltage to the motor's windings and cause serious problems with shaft voltage and bearing currents.

Common-mode voltage and bearing current issues are discussed in Section 2.1 and 2.2. The NP voltage variation is discussed in detail in Section 2.3. Based on that analysis, evaluations of neutral-point voltage balancing techniques are given in Chapter 3.

2.1.2 Common-Mode Voltage

The common-mode voltage is defined as

$$V_{com} = \frac{1}{3}(V_a + V_b + V_c) \qquad (2.1)$$

Because of 12 switches in the NPC inverter shown in Fig.2.1, there are 27 switch states as shown in Fig.3.2. They produce 19 output voltage vectors including a zero voltage vector. If sum of the output voltages is not zero, a common-mode voltage results. An example of waveforms of phase voltages and the resulting common-mode voltages are shown in Fig.2.2.

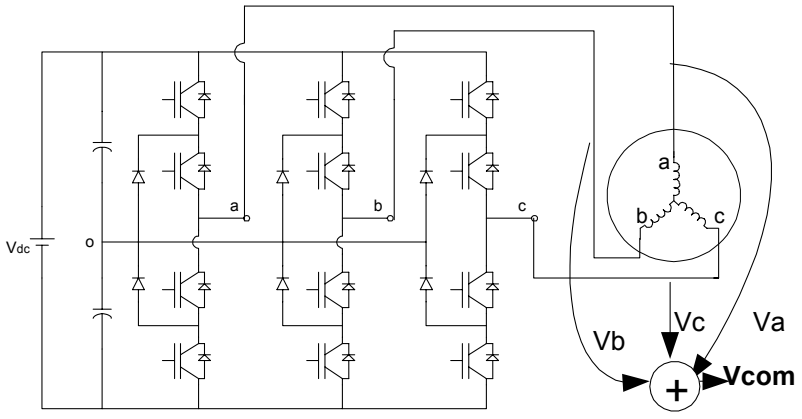

Fig. 2.1 Illustration of common-mode voltage.

The NP voltage variations cause the added variations of three-phase output voltage and induce some harmonics in the output.

$$V_a^{'} = V\sin(\omega t) + v_{np} \qquad (2.2)$$

$$V_b^{'} = V\sin(\omega t - 120°) + v_{np} \qquad (2.3)$$

$$V_c^{'} = V\sin(\omega t + 120°) + v_{np} \qquad (2.4)$$

$$V_{com}^{'} = \frac{1}{3}(V_a^{'} + V_b^{'} + V_c^{'}) = v_{np} \qquad (2.5)$$

Finally, the NP voltage variations generate common-mode voltage at three times the fundamental output frequency, which occurs even if the high frequency and high *dv/dt* switching common-mode voltage is mitigated by some techniques such as filtering. When the common-mode voltage and resulting shaft voltage caused by the NP voltage variation are large enough to break the oil film insulation in the bearings, bearing currents are generated, which by erosion may cause premature failures of the motor bearings. Hence the NP voltage control is important not only for the NPC inverter operation but also for common-mode voltage mitigation.

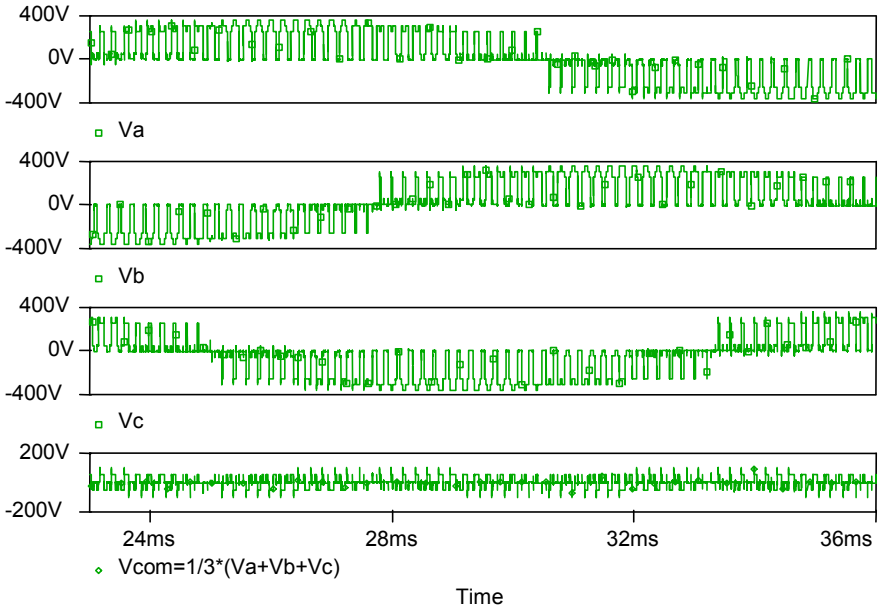

Fig. 2.2 Phase output voltage and the common-mode voltage of an NPC inverter.

The shaft voltage is measured between the motor shaft and the motor frame, which is usually grounded. It is generated by the common-mode voltage coupling through the path that consists of the motor stator windings, rotor windings and the distributed capacitance between them. Its magnitude is dependent on not only the magnitudes of the common-mode voltage but also the coupling impedance. The impedance model was discussed in detail in [7].

2.1.3 Bearing Current

The bearing currents are generated through the path between the inner face of the motor bearing and its outer face by the shaft voltage. Because there is a film of lubricant grease in the bearing, the path from the shaft to the motor frame is insulated by the grease film when the motor is running at a high speed. However, the shaft voltage can be established due to the lubricant grease dielectric ability. Its magnitude may be large enough to break down the grease depending on the drive type, the motor structure and the bearings. It has been observed that even 3V peak shaft voltage may break down the lubricant grease film and cause bearing currents [7]. The bearing currents are generated repeatedly and become the major cause of premature failures of the motor bearings. In order to prevent premature bearing failures, several methods can be used including: mitigating common-mode voltages, short-circuiting the bearing currents and blocking the bearing currents.

2.2 Methods to Cancel Bearing Currents

2.2.1 Mitigation of Common-Mode Voltage

Mitigating common-mode voltage is the ideal method to resolve the bearing current problems because common-mode voltage is the source that can generate the bearing currents. A lot of methods such as different ASD topologies and inverter pulse-width modulation methods have been proposed to mitigate the common-mode voltage [3], [4] and [7]. These methods can effectively reduce the common-mode voltages and common-mode noise. However, the modified topologies generally increase the cost of the ASDs, or special arithmetical modifications give rise to some limitations in the ASD operation. The approach supported in this dissertation was

developed at Oregon State University (OSU) and prevents common-mode voltage generation by skipping the states that generate are responsible.

2.2.2 Short-Circuiting Bearing Current

Short-circuiting bearing current is the second kind of method to cancel the adverse effects of the bearing currents. This can be realized by a shaft grounding system. It is a simple and effective method to prevent shaft voltage. However, it requires periodic maintenance. The commercial grounding system products can be applied to the drive systems with or without ASDs.

2.2.3 Blocking Bearing Current

Blocking bearing current is the third method to prevent bearing currents. This uses insulated motor bearings to block the bearing current. This is also a simple and effective method to protect the motor bearing. However, the modified bearings will increase their costs and sometimes effect their lifetime especially for the bigger motor bearings due to the limitation in the manufacturing techniques.

2.2.4 Active Filter Technique

The active filter method was proposed in [11]. This method applied a closed loop control system to the inverter output terminals. This system supplies a very high common-mode impedance to the inverter output. It can effectively reduce the switching high *dv/dt* common-mode voltages on the motor terminals. However, this method needs careful design of the series common-mode choke in the inverter output, especially for high power applications. Also, it is not suitable for the low frequency

common-mode voltage cancellation due to the low impedance of the ferrite choke at low frequencies.

2.3 Neutral-Point Voltage Variation

2.3.1 Neutral-Point Voltage Variation

Neutral-point voltage variation is the inherent issue in NPC inverters or multi-level inverters. The main reason is that there is the necessary split point in the capacitor bank of the dc-bus. This neutral-point is a floating point where the potential will change if there is any NP current. Again, NP voltage variations need to be mitigated because they may cause start-up failure, CMV and over-voltage across the switching devices. The equivalent circuit of the dc-bus can be shown as the left circuit model in Fig. 2.3 if just the NP voltage and neutral current I_n are concerned. The right portion of Fig. 2.3 shows the AC model (or small signal model) of the NP voltage V_{np} versus the neutral current I_n.
Hence, the voltage V_{np} can be express as

$$V_{np} = \frac{1}{C1 + C2}\int I_n(t)dt = \frac{1}{2C}\int I_n(t)dt \qquad (2.6)$$

Where C1=C2=C.

Because the I_n is the inherent current in the NPC inverter, the NP voltage V_{np} can not be minimized to zero without some additional compensation currents added to the NP point to cancel the neutral current I_n. Hence to reduce NP voltage variation V_{np}, two methods can be applied according to (2.6). One is to reduce the neutral current I_n by inducing a compensation current and the second is increase the dc-bus capacitance C1 and C2 if the maximum I_n and the inverter output frequency are determined.

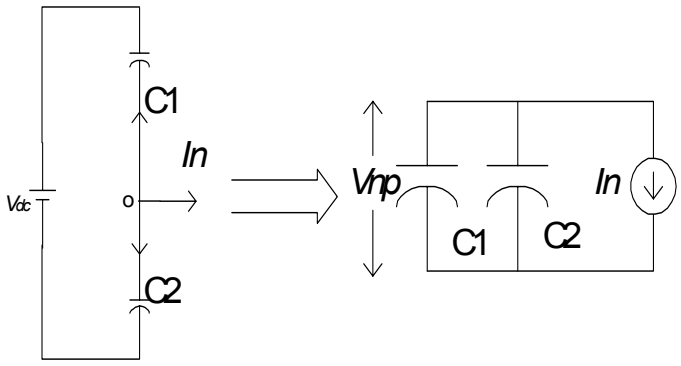

Fig. 2.3. The equivalent dc-bus circuit and NP voltage variation V_{np}.

The first method is widely investigated in the inverter topologies and arithmetical methods including PWM modification and closed loop control of the NP voltage. This will be discussed in Chapter 3. For the second, it is fit for the fixed higher output frequency inverter because a reasonable capacitance value can be applied. Note that fundamental frequency of the NP current in equation (2.6) is three times the inverter frequency. Hence,

$$V_{np} = \frac{1}{2C}\int I_n(t)dt \approx \frac{1}{2C}\int I_{n\_fund}\sin(3\omega t + \theta)dt \qquad (2.7)$$

$$V_{np} \approx \frac{I_n}{6C\omega} \qquad (2.8)$$

where ω is the fundamental output frequency.

From equation (2.8), the NP voltage will become very large if the inverter runs at very low output frequency. For example, for a 460V NPC inverter with some fixed capacitance, if its normal NP voltage variation is 10V peak-to-peak with output frequency 60 Hz, the NP voltage variation will be 100Vpp with output frequency 6Hz, ten times as big as before. So for the very low output frequency, a very big capacitor bank must be applied if a small NP voltage is desired. This will increase the inverter size and cost.

2.3.2 Neutral-Point Current Analysis

The neutral-point currents can be generated by the unbalanced load. The common-mode voltage caused by varying dc-bus voltage or the NPC inverter itself. Even if the load is balanced and the NP potential is not varied, there still are NP-currents. In the following analysis, it is assumed that there is no NP voltage variation and the load is balanced. The schematic of the NP current analysis is shown as Fig. 2.4.

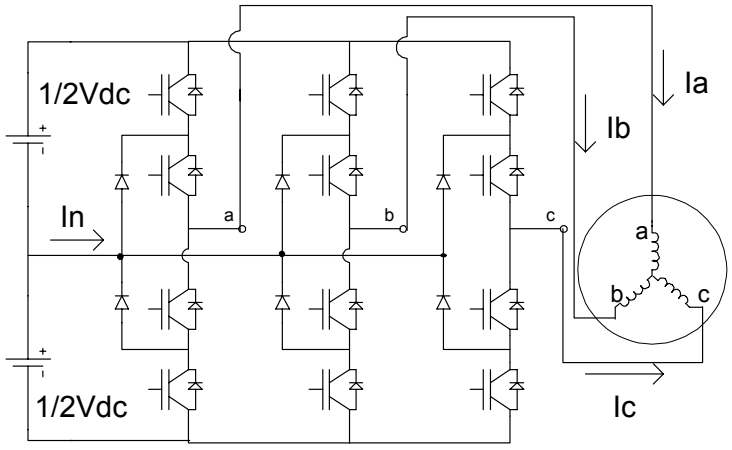

Fig. 2.4 The schematic of NP current analysis.

In Fig. 2.4, the load is balanced. Furthermore, it is assumed that the normalized output voltages and un-normalized currents are sinusoidal as follows:

$$V_a = M\sin(\omega t) \tag{2.9}$$

$$V_b = M\sin(\omega t - 120^\circ) \tag{2.10}$$

$$V_c = M\sin(\omega t + 120^\circ) \tag{2.11}$$

$$i_a = I\sin(\omega t - \varphi) \tag{2.12}$$

$$i_b = I\sin(\omega t - \varphi - 120^\circ) \qquad (2.13)$$

$$i_c = I\sin(\omega t - \varphi + 120^\circ) \qquad (2.14)$$

Where, ω is output frequency. I is output load peak current and φ is load phase angle. The modulation index is expressed as M. The total dc-bus voltage is Vdc. The NP current can be expressed as follows:

$$I_n = i_{na} + i_{nb} + i_{nc} \qquad (2.15)$$

Here, i_{na}, i_{nb} and i_{nc} are the phase a, b and c neutral currents, respectively. When any phase output is clamped to the neutral-point, the neutral-point current related to that clamped phase goes into or out of the neutral-point. The phase and neutral waveforms are shown in Fig. 2.5 for phase B (see also Fig. 2.4).

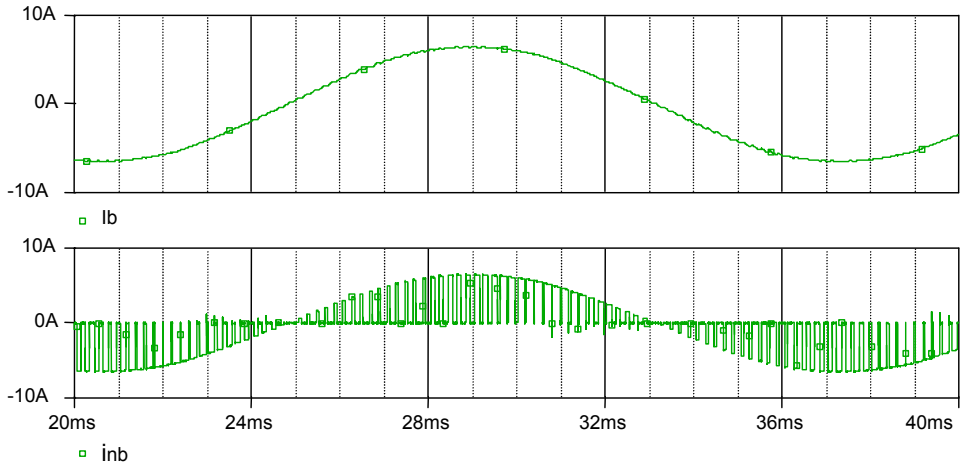

Fig. 2.5 The waveforms of the phase B load current I_b and phase B neutral current i_{nb}.

From Fig. 2.5, the neutral current exists inherently when the output phase voltage is clamped to the neutral-point because of the continuity of the load current. But the neutral current which flows through phase B is proportional to the time duration that the voltage is clamped to the neutral-point. From (2.9), (2.10) and

(2.11), the time ratios of the phase output voltages go to the upper rail or lower rail of the dc-bus are as follows:

Phase A: $R_a = \left|M \sin(\omega t)\right|$ (2.16)

Phase B: $R_b = \left|M \sin(\omega t - 120^\circ)\right|$ (2.17)

Phase C: $R_c = \left|M \sin(\omega t + 120^\circ)\right|$ (2.18)

Where M is amplitude modulation index and defined as $M = \frac{V_{control}}{V_{tripple\_reference}}$.

According to (2.16), (2.17) and (2.18), the time ratios clamped to the neutral-point are expressed as:

$$R_{na} = 1 - R_a = 1 - \left|M \sin(\omega t)\right| \quad (2.19)$$

$$R_{nb} = 1 - R_b = 1 - \left|M \sin(\omega t - 120^\circ)\right| \quad (2.20)$$

$$R_{nc} = 1 - R_c = 1 - \left|M \sin(\omega t + 120^\circ)\right| \quad (2.21)$$

Therefore, the average phase neutral currents can be given by

$$i_{na} = (1 - R_a) i_a = I(1 - \left|M \sin(\omega t - 120^\circ)\right|) \sin(\omega t - \varphi) \quad (2.22)$$

$$i_{nb} = (1 - R_b) i_b = I(1 - \left|M \sin(\omega t - 120^\circ)\right|) \sin(\omega t - \varphi - 120^\circ) \quad (2.23)$$

$$i_{nc} = (1 - R_c) i_c = I(1 - \left|M \sin(\omega t + 120^\circ)\right|) \sin(\omega t - \varphi + 120^\circ) \quad (2.24)$$

Then, from (2.15), the total neutral-point current is given as

$$\begin{aligned} I_n &= i_{na} + i_{nb} + i_{nc} = (1 - R_a) i_a + (1 - R_b) i_b + (1 - R_c) i_c \\ &= -I\Big\{M \sin(\omega t)\left|\sin(\omega t - \varphi) + \right|M \sin(\omega t - 120^\circ)\left|\sin(\omega t - \varphi - 120^\circ)\right. \right. \\ &\qquad \left. \left. + \left|M \sin(\omega t + 120^\circ)\right| \sin(\omega t - \varphi + 120^\circ)\right\} \end{aligned} \quad (2.25)$$

The derivation of I_n is divided into six divisions during one whole period of the output frequency.

Division I (0°~60°) : $I_n = -\frac{1}{2} MI\{\cos\varphi + 2\cos(2\omega t - \varphi + 120^\circ)\}$ (2.26)

Division II (60°~120°) : $I_n = \frac{1}{2} MI\{\cos\varphi + 2\cos(2\omega t - \varphi)\}$ (2.27)

Division III (120°~180°) : $I_n = -\frac{1}{2} MI\{\cos\varphi + 2\cos(2\omega t - \varphi - 120^\circ)\}$ (2.28)

The division IV~VI are the same as I, II, III respectively. The waveforms of the neutral-point current during one output period are shown in Fig. 2.6, Fig. 2.7 and Fig. 2.8.

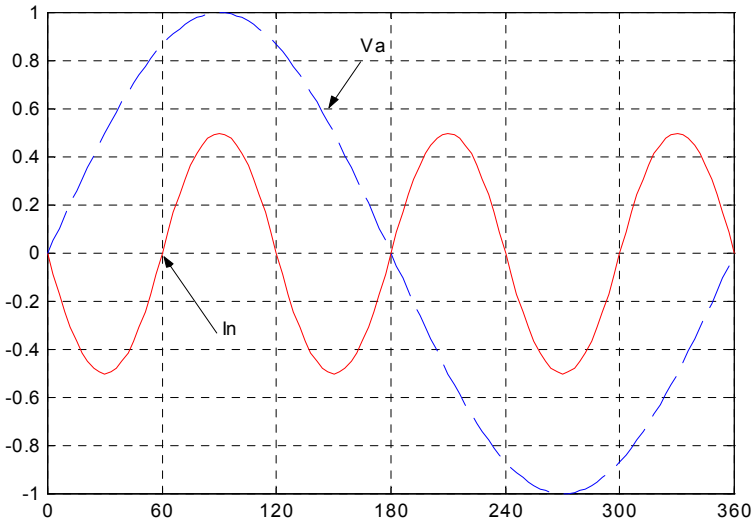

Fig. 2.6 The waveforms of phase A voltage and the neutral current with φ=0.

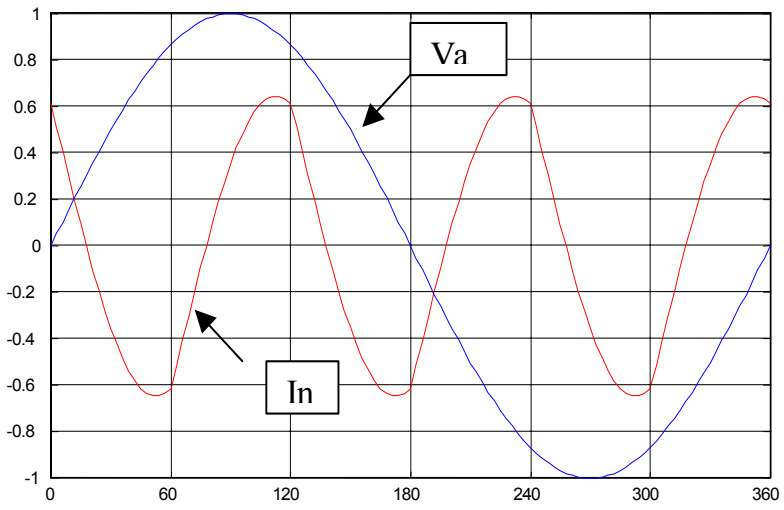

Fig. 2.7 The waveforms of phase A voltage and the neutral current with φ=π/4.

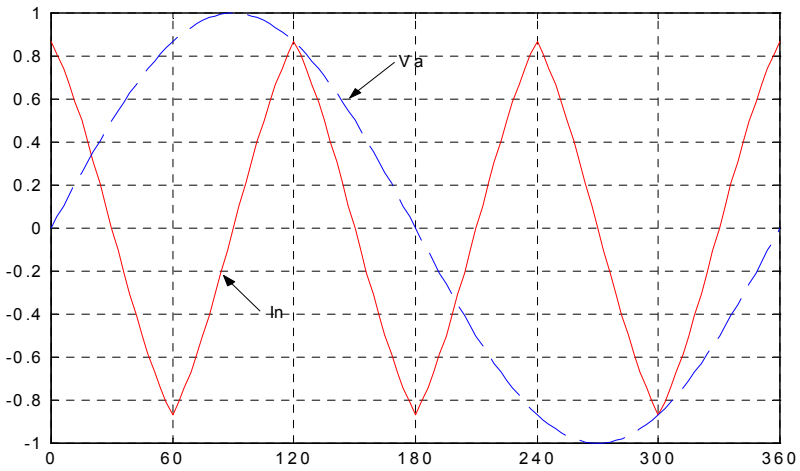

Fig. 2.8 The waveforms of phase A voltage and the neutral current with φ=π/2.

In all three curves, M is set to M=1 and I_n is normalized to 1 by the load current I. Comparing Fig. 2.7 and Fig. 2.8, the waveforms of the neutral current I_n change with

respect to the phase A voltage. In addition, the maximum of the magnitude is changed from 0.5 to 0.866 ($=\sqrt{3}/2$). When the NPC inverter is used in Static *Var* Compensators (SVC), the maximum of the neutral current is equal to the maximum of the load current with an amplitude over-modulation index of 1.16. The wave shapes of the neutral current vary from symmetry ($\varphi=0$) to dissmymmetry ($0<\varphi<\pi/2$) and then to symmetry ($\varphi=\pi/2$) with the load current phase angle varying from 0 to $\pi/2$ as shown in Fig. 2.9.

For the worst case with $\varphi=\pi/2$ and M=1.16, the neutral current is nearly equal to the load current in the magnitude.

Thus,

$$V_{np} = \frac{1}{2C}\int I_n(t)dt \approx \frac{I}{6C\omega} \qquad (2.27)$$

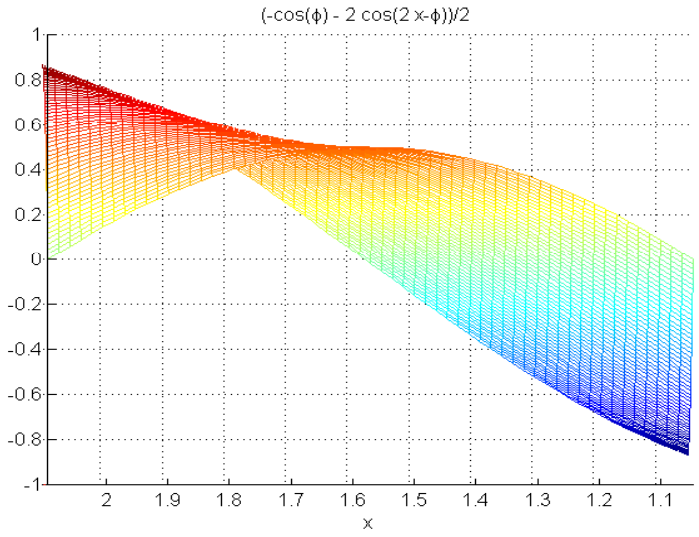

Fig. 2.9 The wave shape variation of the neutral current in the half neutral current period with $\varphi=0$ to $\pi/2$.

For further demonstration and verification of the theory, Fig. 2.10 shows the one phase of the output voltage waveform and the neutral current by PSpice simulation under the condition of $cos\varphi$=0.2.

Furthermore, from the analysis above, the fundamental frequency of the neutral current is the third harmonic of the output frequency because the sign of the neutral currents change every 60°.

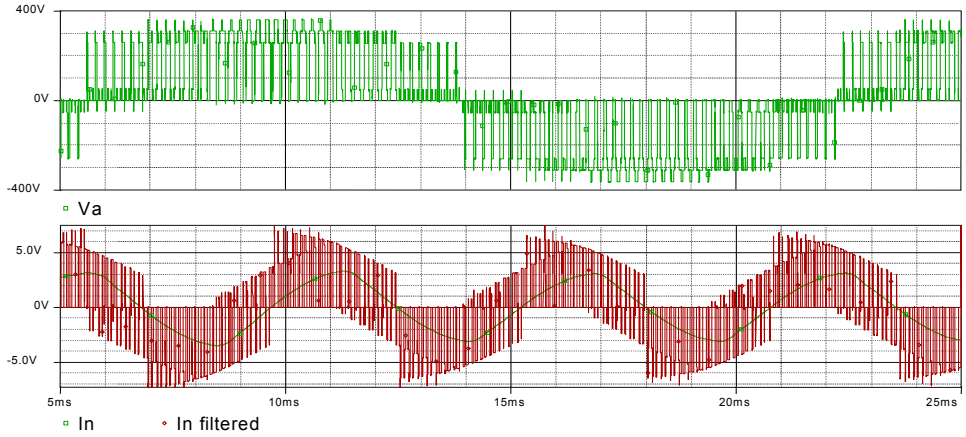

Fig. 2.10 The waveforms of the output voltage and the neutral currents.

The NP voltage variation of the PSpice simulation is shown in Fig. 2.11. The simulation results are given for $cos\varphi$ =0.99. The average neutral current of the simulation exactly matches the theoretical analysis above.

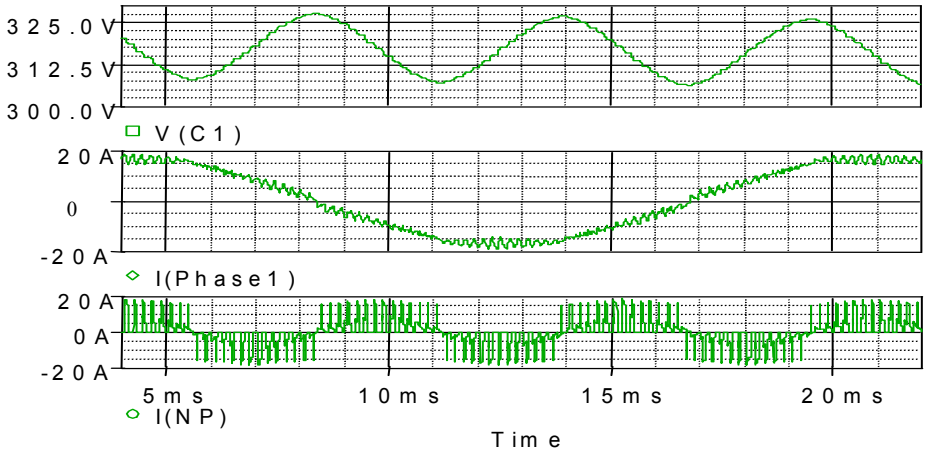

Fig. 2.11 The capacitor voltage V(C1), load current I(Phase1) and neutral-point current I_{NP} without neutral-point voltage control.

2.4 Conclusions

It is well known that bearing currents may cause premature failures. The bearing currents are generated by the shaft voltages through the path from motor shaft to motor frame. However, shaft voltages can be caused by common-mode voltages produced by the switching mode inverters or by the motor unbalanced windings due to the motor design and manufacture. In addition, common-mode voltage also can be induced by the neutral-point voltage variation in the applications of NPC inverters. Therefore, it is very important to control the neutral-point voltage not only for the NPC inverter's safe operation but also for reducing the common-mode voltage generated by the neutral-point voltages in order to mitigate bearing currents. Both the analysis and the simulations in this chapter show the above concepts.

Different kinds of the methods to cancel common-mode voltages were introduced and discussed. The arithmetic methods are preferred although they often limit the output performance of the ASD.

The neutral-point voltage variation has been widely investigated. It directly affects the safe voltage operation area of the switching devices in NPC inverters.

Furthermore, the common-mode voltages caused by the neutral-point voltages may cause bearing currents that may give rise to the premature failures of the motor bearings. The neutral-point voltage is proportional to the neutral currents and inversely proportional to the capacitance of the dc-bus capacitor bank. Usually, the minimum capacitance of the dc-bus capacitor bank can be determined for the fixed operating frequency and the rated load current. However, it is difficult to get an appropriate minimum capacitance for the dc-bus if the output frequency varies from a very low frequency to a high output frequency, especially when the NPC inverter runs at a lower output frequency over a long period of time. The neutral current is a function of the modulation index, load power factor and the load current. The discussion of the relationship and the quantity analysis about the above factors were given and supported by the theoretical analysis and simulation results. The concepts are very important to the NPC inverter design.

3 EVALUATION OF NP VOLTAGE BALANCING METHODS

3.1 Introduction

Various methods have been proposed to maintain the neutral-point voltage. In addition, all the algorithm methods can be categorized into two kinds: carrier-based PWM and space-vector modulation based PWM. For the carrier-based PWM modulations, all the NP voltage control methods utilize some forms of output zero sequence voltage in modulation schemes with closed loop control. As for the space-vector modulation based methods, all the manipulation mechanisms are to use some combinations of the redundant small vectors. The following sections discuss the above two kinds of methods to balancing the neutral-point voltage and the limitations.

3.2 Carrier-based PWM Algorithm

This kind of technique is to add the zero sequence components into the PWM modulation to maintain the neutral-point voltage. The principal is as follows.

Assuming that

$$V_a = M\sin(\omega t) \tag{3.1}$$

$$V_b = M\sin(\omega t - 120^\circ) \tag{3.2}$$

$$V_c = M\sin(\omega t + 120^\circ) \tag{3.3}$$

and $$V_{nps} = N\sin(3\omega t + \alpha) \tag{3.4}$$

Here, α is dependent on the load power factor (φ).

V_{nps} is added to the carrier signals or the SPWM reference signals to cancel the neutral-point voltage V_{np}. This can be realized by the open loop method [16] or the closed loop methods [17], [18].

3.2.1 The Open Loop NP Voltage Control

The compensation reference signal V_{nps} is generated by optimal off-line calculations according to the load power factor.

For the general optimal condition, $N = M/3$, and $\alpha = 180^{\circ} - (\varphi - \delta\varphi)$. Here $cos(\varphi) = P.F.$ and $5° < \delta\varphi < 15°$. It is reported that this method can successfully maintain the neutral-point voltage for general operations. The scheme is very simple and easy to realize. In addition, there is no stability issue in the neutral voltage control where the stability issues have to be carefully considered in the closed loop NP voltage control.

However, there are some shortcomings to the above approach. Due to not considering the effects of the load current variation and the output frequency in the reference signal, the control error may be pretty big or even out of control if the operation points diverge during general operation, for example, if the output frequency of the NPC inverter is ten times lower than the normal operating frequency. Furthermore, the larger variations of the load power factor also reduce the control precision.

Thus, this kind of open loop control is not fit for the practical application in NPC inverters.

3.2.2 The Closed Loop NP Voltage Control

This technique is to apply a feedback control system to maintain the neutral-point voltage for three-level NPC inverters. The basic idea is to measure the voltage errors between the two split dc-bus capacitors' voltages and use a compensation controller to calculate the compensating command signal to be added to each of the PWM modulation signals. It also utilizes the load information, $Icos(\varphi)$, and can give better performance. The block diagram of the NP voltage control system is shown in Fig. 3.1.

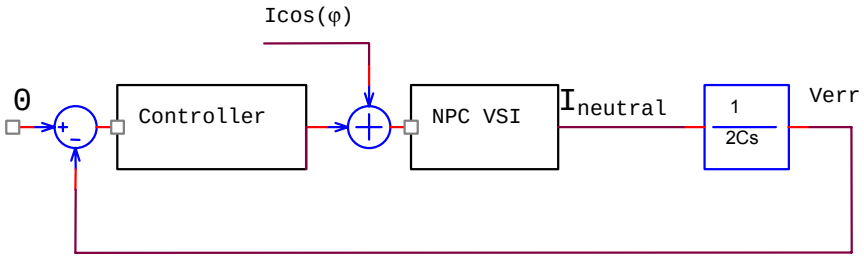

Fig. 3.1 NP voltage feedback control block diagram.

The feedback control loop method can give high precision and robustness to the disturbances or the unbalanced loads. However, there are some practical limitations in spite of the simple control structure.

1. Regeneration issue: the control loop may become unstable if the inverter works at regeneration status. In order to solve this problem, on-line calculation of *Icos(φ)* is needed.
2. Non-linearity problem: because the neutral current is non-linear with respect to the load current, the closed control loop includes a non-linear stage. This affects the system design and stability.
3. Modulation distortion: this is caused by the maximum possible output voltage limitation due to the supply dc-link voltage. When a larger compensating neutral current is needed, the higher output voltage from the drive must be applied to the load. This can give rise to over-modulation that causes distorted output voltage.

From the above discussion, the carrier-based PWM methods are simple but there are some limitations in the application.

3.3 Space Vector Modulation Method

Recently, the SVM method is widely used in NPC inverters to improve the ASD performance. Therefore, the SVM-based PWM technique is mostly applied in the control of the neutral-point voltage when SVM modulation is applied. It uses the small redundant voltage vectors to control the neutral current. Because of its twelve switching devices, there are twenty-seven switching states in NPC inverters. The possible switching states are shown in Fig. 3.2.

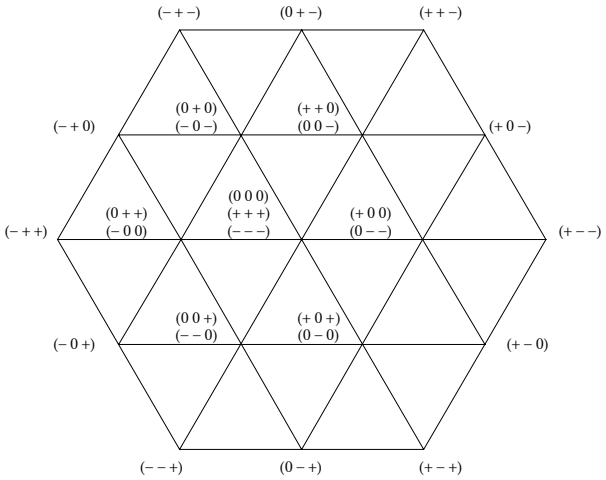

Fig. 3.2 Possible switching states of a three-level NPC inverter.

The neutral current direction is different for different voltage vectors. The neutral current I_n is shown in Table 3.1.

Positive small vectors	I_n	Negative small vectors	I_n	Medium vectors	I_n
0 - -	i_a	+ 0 0	$-i_a$	+ 0 -	i_b
+ + 0	i_c	0 0 -	$-i_c$	0 + -	i_a
- 0 -	i_b	0 + 0	$-i_b$	- + 0	i_c
0 + +	i_a	- 0 0	$-i_a$	- 0 +	i_b
- - 0	i_c	0 0 +	$-i_c$	0 - +	i_a
+ 0 +	i_b	0 - 0	$-i_b$	+ - 0	i_c

Table 3.1. Neutral current I_n for different space voltage vectors.

The neutral-point voltage control in SVM modulation has three types: open loop control, hysteresis closed loop control and linear closed loop control.

Open loop control: the small positive and negative voltage vector is selected alternatively in every switching cycle. Thus, it can compensate the unbalanced load or disturbance similar to the open loop control of the carrier-based PWM.

Hysteresis closed loop control: the selection of the space vector is based on the direction of the neutral current so as to suppress the NP voltage variation. It is very simple in realization and robust in controllability. But it requires the information of the current direction in each phase and may generate current ripples at half of the switching frequency.

Linear closed loop control: this kind of scheme uses the information of the unbalanced NP voltage and the phase currents just like the carrier-based PWM NP voltage closed loop control. Unfortunately, this method may increase the switching loss and cause stability issues.

It is reported that the NP voltage control performance is limited in some operation conditions regardless of the control schemes in [19]. For example, the low frequency ripple can't be balanced at a higher modulation index (0.9) and lower load power factor (0.7). This limits the operation range of the NPC converter.

3.4 Conclusions

Neutral-point voltage variation is widely known as an inherent problem in NPC inverters. Analysis of the NP voltage issues related to carrier-based PWM and space vector PWM have been presented. Also, various strategies have been proposed to balance the NP voltage. The zero sequence voltage and the redundant space voltage vector concept are utilized in the carrier-based PWM and the space vector based PWM, respectively. Most of the successful schemes are the closed loop control schemes although there is a stability issue in the design of closed loop control.

However, all algorithms to date to balance NP voltage are not very satisfactory and have some limitations in the applications. For the carrier-based PWM, modulation distortion is the main issue. In addition, there might be some problems if there is another control loop existing, for example, speed loop control or closed loop control of the torque. The same situation might happen for the space vector based PWM. In spite of the limitations of operating conditions, the SVM-based NP voltage control method can't be available when an algorithm is implemented to cancel the common-mode voltage. That is because the specific voltage vector must be selected to cancel the common-mode voltage and there is no appropriate redundant voltage vector to control the direction of NP current at the same time.

Considering the above issues, a hardware method is proposed to balance the NP voltage so that an algorithm can be used to perform other functions to improve the NPC inverter's performance. The schematic of the hardware method is discussed in details in Chapter 4.

4 BUCK-BOOST APPROACH TO BALANCING NP VOLTAGE

4.1 Introduction

The buck converter topology is widely applied in the switching mode power supplies due to its simplicity and high efficiency. It is designed to produce a lower voltage from a higher voltage supply. In the power supplies such as for current generation microprocessors, the developed buck converter topology, multiphase buck converters are successfully used to supply low voltage, high current and fast response performance. The major advantage of the buck converter is its low power losses and good control stability. For high voltage applications, the efficiency of the buck converter can be much higher than that in the low voltage applications, dependant on the voltage & power range and switching frequency. In addition, its control stability is very easy to be achieved.

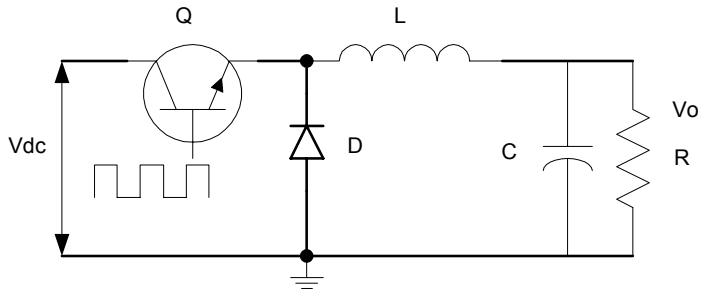

Fig. 4.1 Schematic of the Buck converter.

Boost converters can produce a higher voltage from a lower voltage source. The main features include topology simplicity, high efficiency and low losses. But the controller for the boost converter needs to be carefully designed to meet the requirement of stability. It is widely used in power factor correction applications. The

following discussion is to combine the buck and boost converters into a NP voltage balancing circuit.

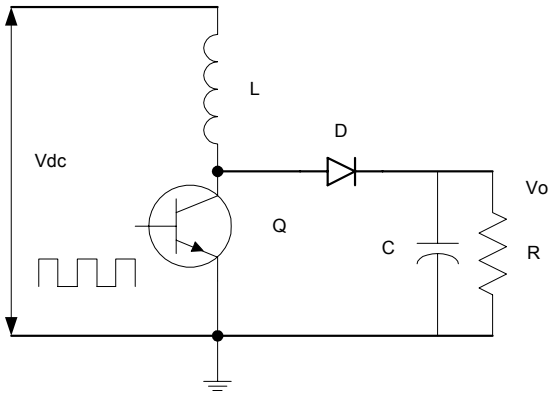

Fig. 4.2 Schematic of the Boost converter.

4.2 Theoretical Operation of the Buck and Boost Balancing Circuit

4.2.1 NP Voltage Balancing Circuit

The NP voltage balancing topology is shown in Fig. 4.3. The circuit consists of buck and boost converters. In the balancing mode, the buck and boost converters work in complementary periods. In the schematic diagram, VDC is the equivalent dc-bus voltage. C1 and C2 are the dc-link capacitors. In the left dash line box, U1, D1, L1 and C2 consist of a buck dc-dc converter. U2, D2, L2 and C1 work in boost dc-dc converter mode in the right dash line frame.

The balancing circuit operation will be described in the following section. From the analysis of the neutral current in Chapter 2, the maximum of the neutral current is almost same as the load current at the worst operating condition. The switching device rating, which is the same as the switching devices used in the power end of the NPC inverter, is enough for the practical application.

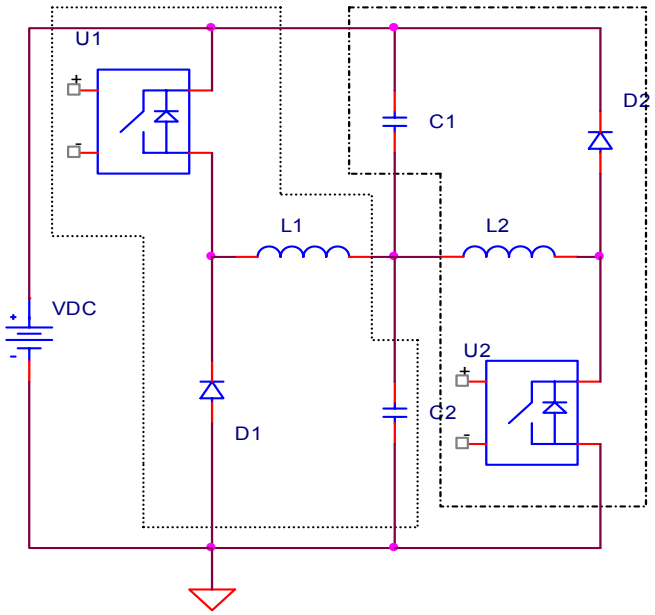

Fig. 4.3 Schematic of the neutral-point voltage balancing circuit.

4.2.2 Buck DC-DC Mode and Boost DC-DC Mode

When the voltage of capacitor C1 (Vc1) is greater than that of capacitor C2 (Vc2), the buck circuit (U1, L1, D1 and C2) starts to operate and regulate the voltage of the capacitor C2 to maintain the balance of the dc-link voltage. The boost converter does not operate during this period. Because Vdc=Vc1+Vc2 and Vdc is kept constant with respect to NP voltage variation, the voltage of C1 decreases as Vc2 increases. Thus the variation of the NP voltage can be quickly balanced by regulating the voltage of one of the two split capacitors on the dc-link. When the switch U1 turns on, the current to charge C2 flows from U1 to L1 to C2. When U1 is off, the energy stored in L1 is transmitted to C2 through the D1, L1 and C2 loop. Note, the described buck circuit is used to regulate Vc2. A PWM method is used to control the voltage of C2.

In the boost dc-dc mode (Vc2>Vc1), the buck converter does not operate. In this mode, the energy in capacitor C2 is indirectly transferred to capacitor C1 because

Vc2>Vc1. The current flows from C2, L2 and U2 to ground. The energy is stored in L2 when the switch U2 is on. When the Switch U2 is off, the energy stored in L2 is transmitted into C1 through D2. Thus during this period the balancing voltage is controlled by regulating the voltage of C1. When Vc1 is equal to half of V_{dc}, the variation of the NP voltage is zero.

4.2.3 Reduced Device Balancing Circuit

In order to save costs and increase reliability, a balancing circuit with a reduced number of switching devices from Fig. 4.3 is obtained as shown in Fig. 4.4. In this situation, the additional ride-through performance is not an issue here. In Fig. 4.4, D1, D2 and L2 shown in Fig. 4.3 are eliminated. The feedback diodes of U1 and U2 operate as D2 and D1 in Fig. 4.3, respectively. The performance and operation of the circuit shown in Fig. 4.4 is the same as in Fig. 4.3. Thus, a simpler balancing circuit can be applied to the NP voltage control, however without ride-through enhancement.

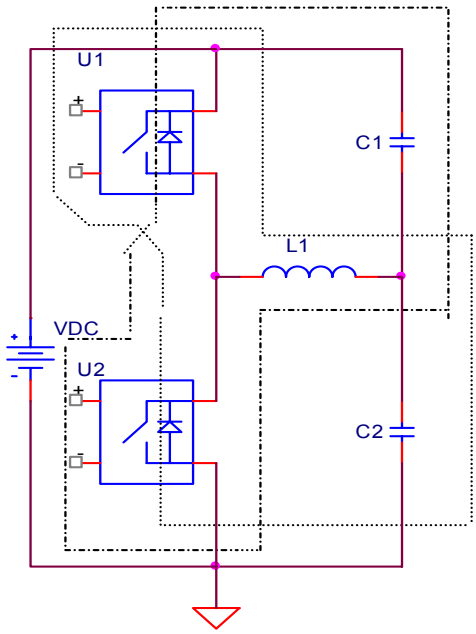

Fig. 4.4 Schematic of the neutral-point voltage balancing circuit with reduced devices.

For the multi-level inverter with the braking switching devices, the inductor L1 is only necessary in the power end and the two braking IGBTs will take the palce of the balancing switching devices as shown in Fig. 4.4. But the additional switching devices for the brake resistor and the balancing inductor are required.

4.3 Common-Mode Voltage Cancellation

There are many Common-Mode Voltage (CMV) techniques proposed. In this dissertation, the emphasis is to investigate the NP balancing problems. Considering the hardware limitation of the experimental system, a simple arithmetical method to cancel CMV is applied into the simulation and the experimental verification.

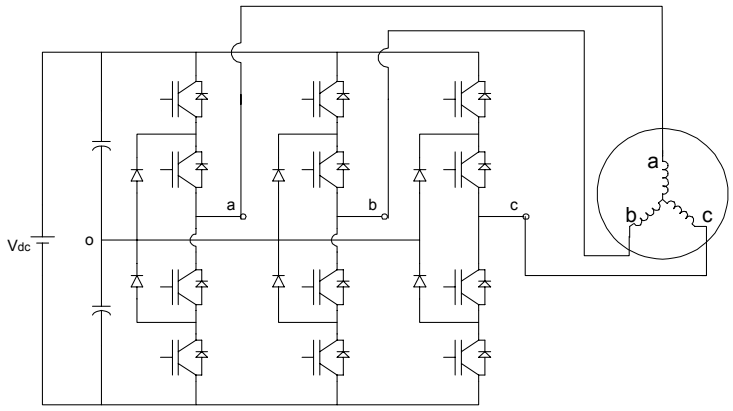

Fig. 4.5 Schematic of the neutral-point clamped inverter with an AC motor load.

$$V_{COM} = \frac{1}{3}(V_a + V_b + V_c) \qquad (4.1)$$

For the normal SPWM method, the waveforms of the common-mode voltage are shown in Fig. 4.6. The production of the IGBT's gate signals is illustrated in Fig. 4.7.

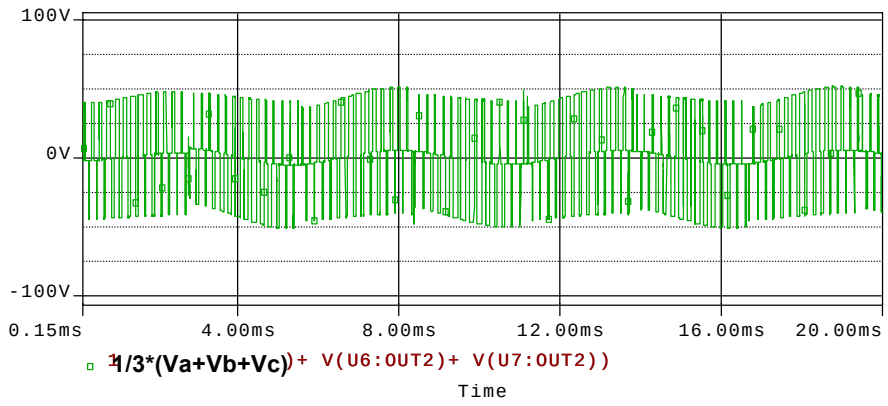

Fig. 4.6 The waveforms of the common-mode voltages.

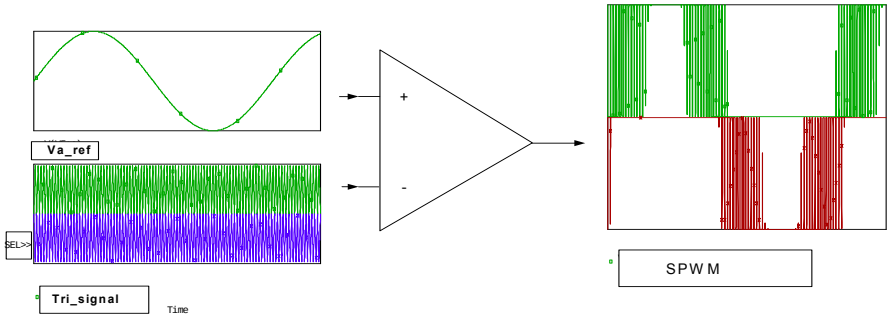

Fig. 4.7 The demonstration of the NPC SPWM.

In (4.2), V_a, V_b and V_c are as follows.

$$V_a = V_m \sin(\omega t) \qquad (4.2)$$

$$V_b = V_m \sin(\omega t + 120^\circ) \qquad (4.3)$$

$$V_c = V_m \sin(\omega t - 120^\circ) \qquad (4.4)$$

In order to mitigate the common-mode voltage, the reference signals are set as follows:

$$V_a^{'} = V_a - V_b = \sqrt{3} V_m \sin(\omega t - 30^\circ) \qquad (4.5)$$

$$V_b^{'} = V_b - V_c = \sqrt{3}V_m \sin(\omega t + 90^\circ) \qquad (4.6)$$

$$V_c^{'} = V_c - V_a = \sqrt{3}V_m \sin(\omega t - 150^\circ) \qquad (4.7)$$

From (4.5), (4.6) and (4.7),

$$V_{cm}^{'} = \frac{1}{3}(V_a^{'} + V_b^{'} + V_c^{'}) = 0 \qquad (4.8)$$

The PSpice simulation results with the common-mode voltage mitigation SPWM described above are shown in Fig. 4.8.

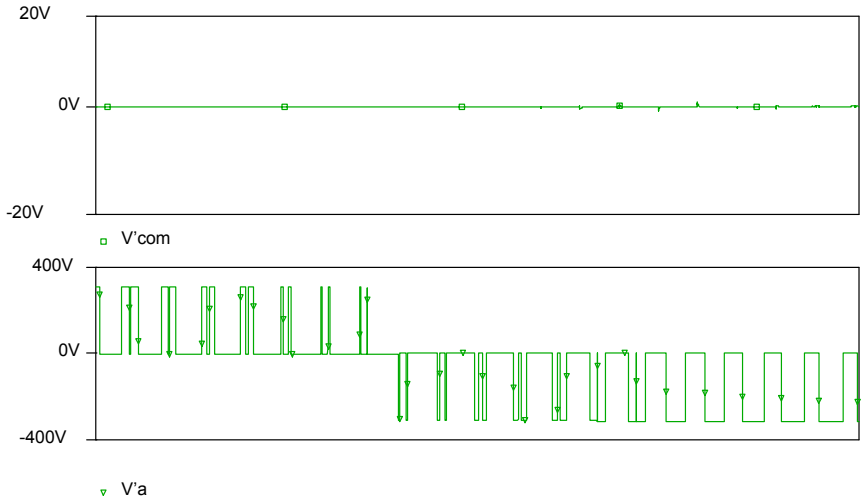

Fig. 4.8 The waveforms of the NPC inverter V'_{com} and V'_a.

4.4 Simulation Results

4.4.1 Introduction

The simulation schematic is shown in Fig. 4.9. In the simulation, the load is a 460V 10hp AC motor. The total dc-bus voltage is set to 620Vdc. The SPWM can be set as the conventional SPWM or simple common-mode voltage mitigation SPWM

dependent on the different simulations. The NP voltage controller consists of two voltage transducers, compensation circuits, two switching devices and other components shown in Fig. 4.9. The AC motor load is equivalent to a R-L-C network in order to simplify the simulation by PSpice, which does not affect the NP voltage variation control and common-mode voltage. The compensation circuits consist of Lag-Lead compensator according to the feedback theory. The NP voltage reference is set to half of the total dc-bus voltage. The controller design will be described in detail in Chapter 5. The simulations are done with and without common-mode voltage mitigation SPWM, respectively.

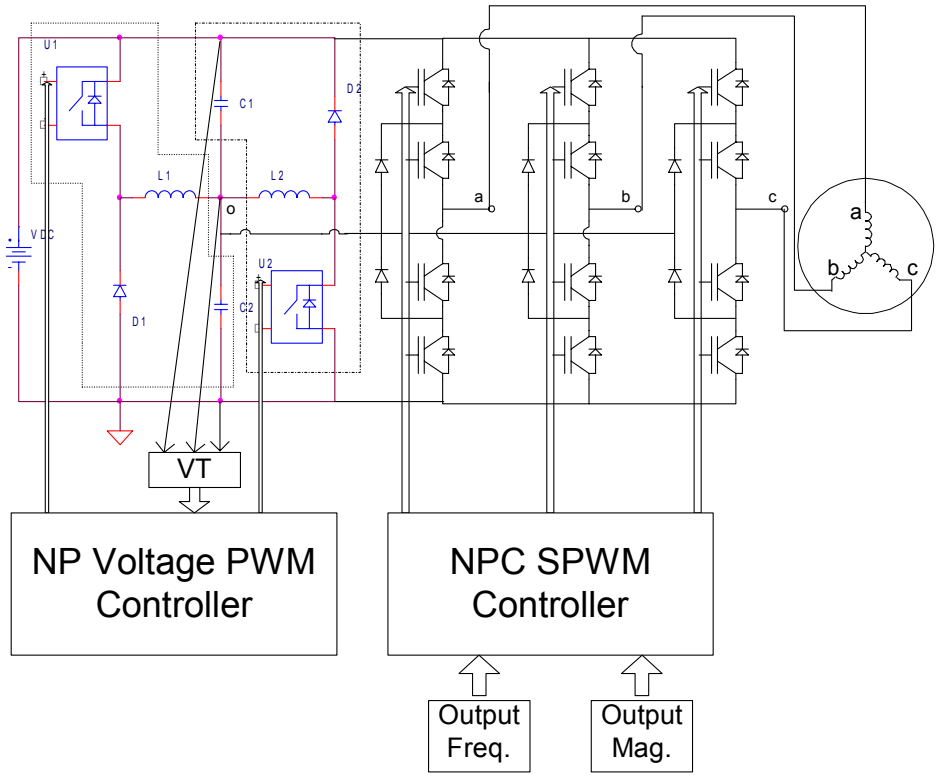

Fig. 4.9 The simulation schematic of the NPC inverter with NP balancing circuits.

4.4.2 The Simulation Results without CMV Mitigation

The conventional SPWM is applied in the PSpice simulation without the common-mode voltage mitigation technique. That means the common-mode voltage will exist as shown Fig. 4.12. The simulation results are shown in Fig. 4.11 and 4.12.

From Fig. 4.10, the dc-link capacitor voltage ripple is ±4.8%. With the proposed control techniques, the capacitor voltage ripple is reduced to no more than ±0.7% of the capacitor voltage as shown in Fig. 4.11. Note that the capacitor voltage ripple (which is as large as the NP ripple) is completely controlled by the boost and buck dc-dc converters.

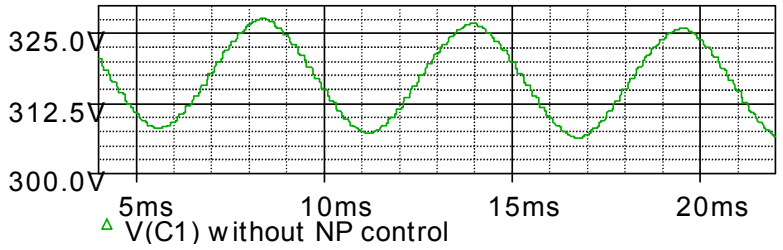

Fig. 4.10 The Capacitor voltage V(C1) ripple without neutral-point control.

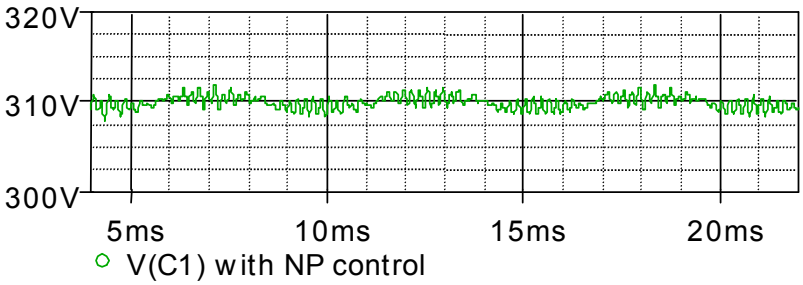

Fig. 4.11 The Capacitor voltage V(C1) ripple with neutral-point voltage control.

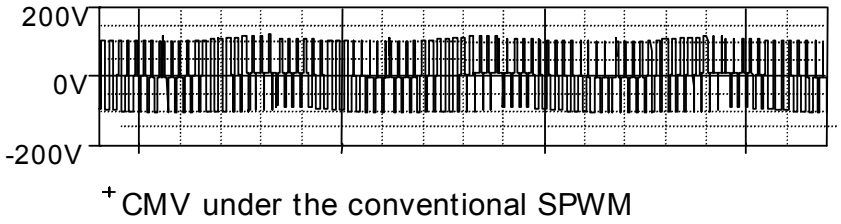

Fig. 4.12 The CMV waveforms under the conventional SPWM.

4.4.3 The Simulation Results with CMV Mitigation

In this section, the results of the simulations with common-mode voltage cancellation will be discussed. The balancing circuit current waveforms are shown in Fig. 4.13. And the waveforms of the common-mode voltages, the NP voltage variation and the load current in different operating modes are shown in Fig. 4.14 and Fig. 4.15, respectively.

The boost and buck converters operate in different intervals in the proposed balancing scheme as shown in Fig. 4.13. The current through L1(I_{L1}) is shown with the solid curve while I_{L2} is shown as the dashed curve. The maximum current of the converter's switching device is decided by the converter inductance and the variation of the NP current. Note that $-I_{L2}$ is shown for clarity.

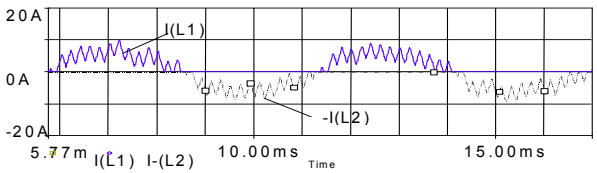

Fig. 4.13 The current waveform of the inductors of the neutral-point voltage control circuit.

The waveforms of the common-mode voltage shown in Fig. 4.14 are similar to the waveforms of the NP voltage variation. But there is no high frequency and high voltage pulses as shown in Fig. 4.12. Compared with those in Fig. 4.14, the waveforms of the common-mode voltages and the NP voltage variation are smaller in Fig. 4.15. The proposed balancing circuits and the arithmetical SPWM with the common-mode voltage cancellation work well at the same time.

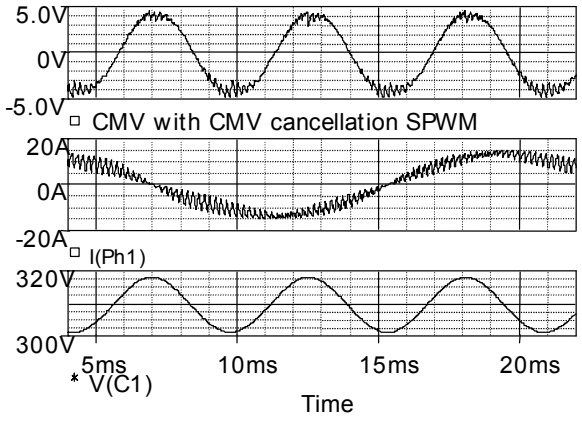

Fig. 4.14 The CMV waveforms with the CMV cancellation SPWM, one phase current of the load and the voltage of one capacitor without neutral-point control.

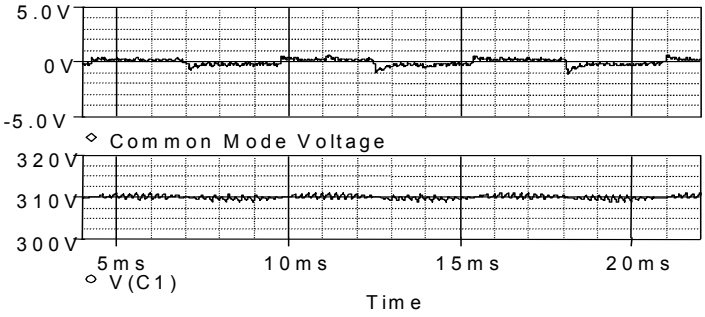

Fig. 4.15 The common-mode voltage waveform and the voltage waveform of capacitor C1.

4.5 Ride-Through Enhancement

4.5.1 Introduction

Ride-through is the ability of an ASD to continue normal operations during a power disturbance. This area has been widely studied [1], [5]. And different ASD systems have different ride-through abilities. An ASD can be tripped by under-voltages, over-voltages and other reasons. However, voltage sag is one of the main reasons that cause under-voltage problems in ASDs. It is reported that the dc-bus capacitor bank of a typical 460V, 60Hz, 10hp AC drive can only supply a 25.8ms (1.55 cycles) of ride-through during a power interruption [1]. Therefore, when a heavy sag happens, it is nearly impossible for the ASD to be only supplied by energy storage elements on the dc-bus if passive approaches are applied. Many active methods can be applied to supply ride-through during the voltage sag. For examples, boost converter [1], active rectifier ASD front end and super-conducting magnetic energy storage systems all can supply ride-through for ASDs.

When a single-phase sag happens, the voltage will drop. But the source may still supply energy to the load. For three-phase voltage sources, if phase A sags, then we have

$V_a = V\sin(\omega t)$,

Here $V = \eta \times V_m$, $\eta = 0 \sim 1$ (sag factor) (4.9)

$V_b = V_m \sin(\omega t - 120°)$ (4.10)

$V_c = V_m \sin(\omega t + 120°)$ (4.11)

Then,

$$V_{ab} = \frac{\sqrt{3} Vm}{\beta} \sin(\omega t + \alpha)\ ; \quad (4.12)$$

$V_{bc} = \sqrt{3}\, V_m \sin(\omega t - 90^{\circ})$ (4.13)

$$V_{ca}= \frac{\sqrt{3}Vm}{\beta}\sin(\omega t+\theta) \qquad (4.14)$$

Here $\beta=\sqrt{\frac{12}{4\eta^2+4\eta+4}}$, $\alpha=\arcsin(1/2\beta)$, $\theta=180^{\circ}-\arcsin(1/2\beta)$.

Thus, when $V_{dc}>\frac{\sqrt{3}Vm}{\beta}$, the rectifier is partly equivalent to single-phase rectifier, and when $\eta= 0$, the rectifier is fully equivalent to the single-phase rectifier illustrated by PSpice simulations in Fig. 4.16.

Therefore, the dc-bus average voltage of the equivalent single-phase rectifier is: $V_{dcavg}=0.9\frac{\sqrt{3}Vm}{\sqrt{2}}$. Assuming V_m=375.6V and $\eta= 0$, then V_{dcavg}=414V. However, if a boost converter is applied, the ride-through of an inverter can be supplied for this case. The same method can be applied to the NPC inverter with a modified NP voltage balancing circuit.

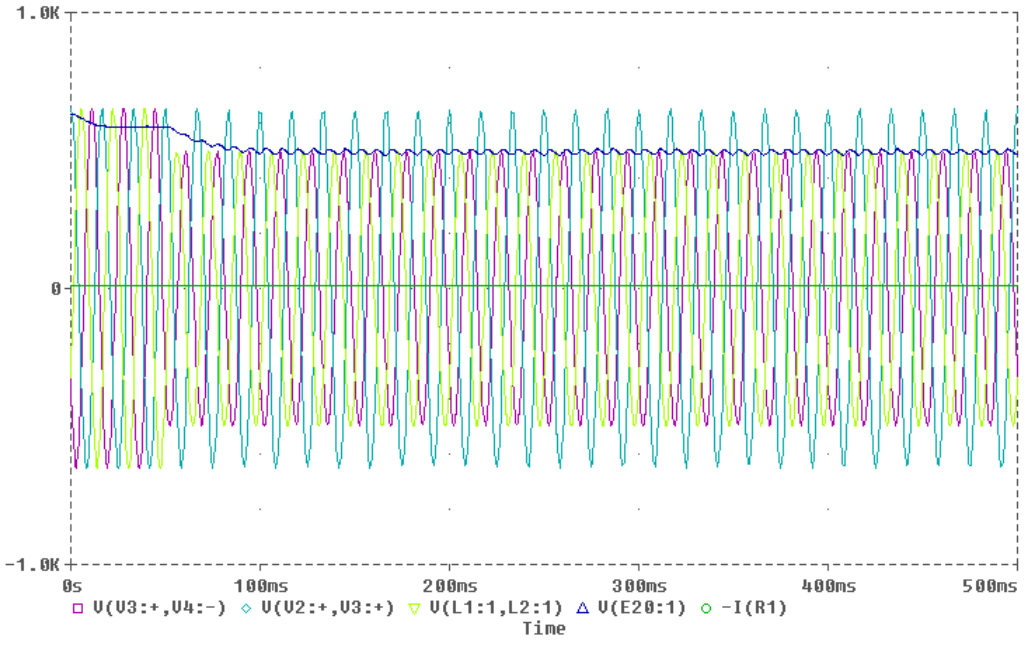

Fig. 4.16 The waveforms of the dc-bus voltage and input AC voltage when a sag happens.

In this section, the modified balancing circuits are controlled to enhance the ride-through of the NPC inverter.

4.5.2 Topology for Ride-Through

A modified NP voltage balancing circuit with ride-through capabilities is shown in Fig. 4.17, through the addition of switching device, U3. When there is no voltage sag, the switch U3 is on, and the modified circuit works as described in Fig. 4.3. When a voltage sag occurs on the supply input that causes Vdc to decrease below the under-voltage protection/trip setting, if no additional ride-through operation mode is available, the MLI will trip off-line. However, with the auxiliary ride-through circuit shown in Fig. 4.17, the switch U3 will turn off and the circuit will operate in the ride-through mode as follows: The boost and buck converters work together to balance the neutral-point voltage and maintain the dc-link voltage. The buck converter regulates the voltage of the capacitor C2. The current from Vdc flows through U1, L1 and C2 when switch U1 is on. The energy is stored in L1 and C2. When the Switch U1 is off, the energy in L1 is transferred to C2. Meanwhile, the boost converter boosts the energy from the capacitor C2 to C1 and regulates the voltage of C1.

Note that the rating of the switching devices used during ride-through operation will be dependent on the desired ride-through performance. Furthermore, the size of the inductor L1 and the capacitor C2 are determined by the voltage and current ripple, since the power is supplied through the lower capacitor C2. Thus, L1 and C2 are different from L2 and C1 in order to maintain the same voltage ripple of Vc2 and Vc1.

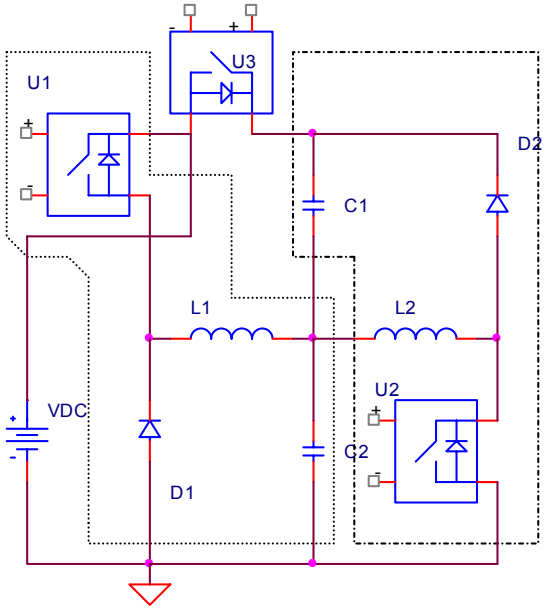

Fig. 4.17 The modified schematic of the neutral-point voltage balancing circuit with ride-through capabilities.

4.5.3 Verification by Simulation

Fig. 4.18 shows the voltage and current waveforms of the NP voltage controller working in the ride-through mode. During an example 40% single-phase voltage sag, the rectifier output voltage is shown to be reduced to 520 Vdc. However, because the voltage of each capacitor is regulated to 310 Vdc, the total dc-link voltage is maintained at 620 Vdc during the sag. Note that the differential voltage of the two capacitors is Vc2-Vc1. Thus the voltage variation about the NP voltage (Vc2-Vc1)/2 is half of the varying magnitude shown in the second waveform of Fig. 4.18.

When the sag occurs, the boost and buck converters will both operate. The current waveform of one of the converter inductors is the fourth curve shown in Fig. 4.18.

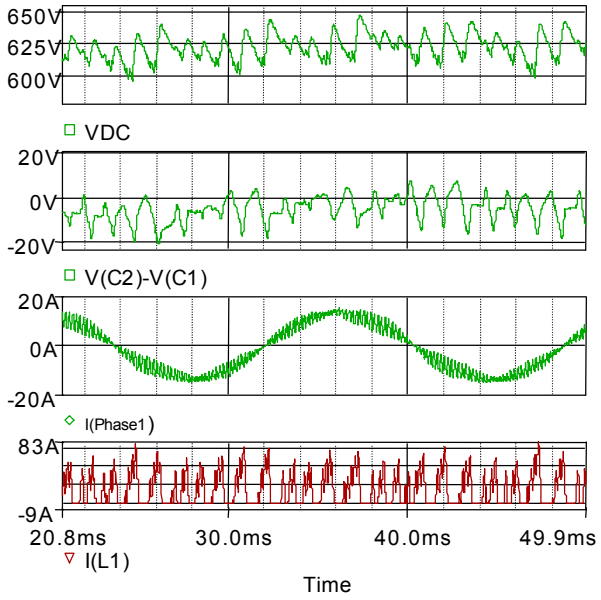

Fig. 4.18 The total dc-link voltage during a 40% single-phase sag, the differential voltage of the two capacitors, the load current and one of the controller inductor current waveforms of the simulation with neutral-point control in ride-through mode.

4.6 Conclusions

The proposed hardware method to control the NP voltage was proposed and discussed in this chapter. The simulation results show that the proposed method can effectively control the NP voltage to appropriate levels. At the same time, the arithmetical SPWM method to mitigate the common-mode voltage was applied to the NPC inverter. The common-mode voltage was cancelled as shown in the simulation results. But the hardware method requires additional switching devices. This will increase the cost of the inverter.

Another method to reduce the cost of the inverter is to use the same switching devices to control the NP voltage during the normal operation or control the dc-bus voltage during the braking operation. The switches of the different operations can be realized by low cost SCRs.

The enhanced balancing circuit with ride-through is presented and simulation results show it running well. This modified topology supplies the ride-through capability in addition to control the neutral-point voltage.

5 NPC INVERTER DESIGN

5.1 System Design

The NPC inverter is modified from the conventional two-level inverter. The initial proof-of-concept experiment setup was a 5hp 460VAC 3-phase motor drive system. All the control functions are implemented by a TMS320F240 DSP controller. The system diagram is shown in Fig. 5.1. The NPC inverter drive system mainly consists of the power input stage, the power output stage, the NP voltage balancing circuits, the IGBTs' base driver boards, voltage and current transducer conditioning circuits, analog & digital I/O interface board and DSP controller board. The functions of the blocks are described as follows.

1. Power input stage: converting AC voltage to dc-voltage. It includes 3-phase rectifier, protection fuses, dc-bus capacitor bank, and dampimg circuits preventing dc-bus resonant oscillation.
2. Power output stage: converting dc-voltage to three-level (positive, zero and negative voltages) phase voltage. It consists of twelve IGBTs and clamped fast-recovery diodes.
3. NP balancing circuits: balancing the two split capacitor banks and maintaining the NP voltage to be half of the total dc-bus voltage. The modified circuits can supply some ride-through ability through the DSP controller.
4. IGBT's base driver: isolating the power stage from the DSP controller circuits and receiving PWM control signals and driving the IGBTs with the appropriate voltage and protection in the NPC inverter. Two types of the commercial driver boards are used to drive the IGBTs, 2 pieces of Toshiba 35589 driver boards for the inverter output stage and 3 pieces of Semikron SHK-10 boards for the balancing circuits.

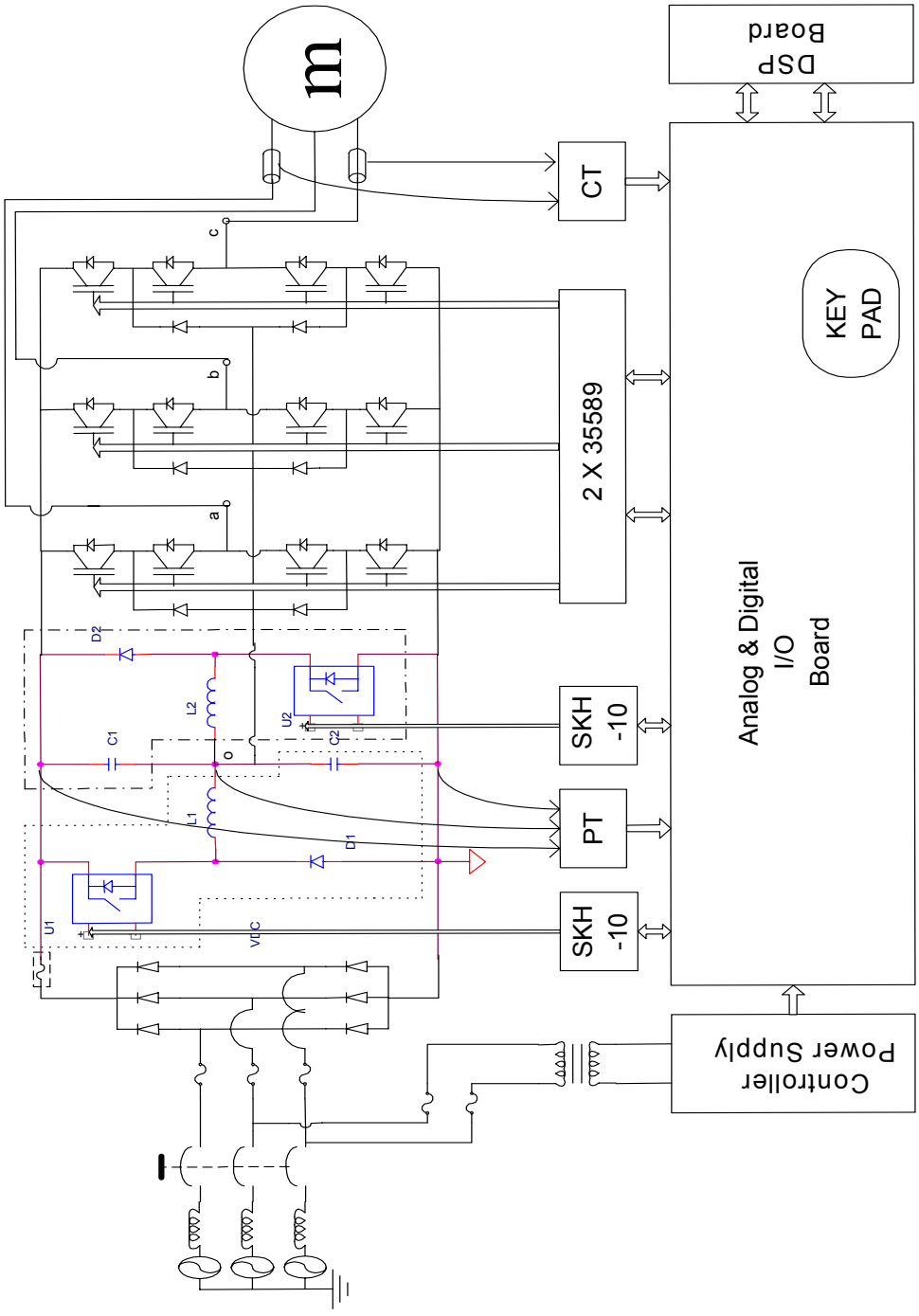

Fig. 5.1 Block diagram of NPC inverter.

5. Voltage & current transducer conditioning circuits: isolating high voltage and measuring the dc-bus voltages and two-phase output current by the transducers for balancing control and under or over voltage protection and over current protection, respectively.
6. Analog & digital I/O interface: conditioning the analog & digital input and output ports, interfacing with the analog bus and digital bus of the DSP controller board. A small keypad is designed on this board for the operation command input.
7. DSP controller board: implementing arithmetical PWM modulation, NP voltage closed-loop control, error detection and fault protection, system configuration setting and information display. Texas Instruments TMS320F240 DSP controller evaluation board is used to implement the above tasks.
8. Other auxiliary circuits and functions: current leakage detection circuits and output power stopping function, start-up inrush current limiting and main power on delay circuits.

The above designs are discussed in the following sections.

5.2 Balancing Circuit Control Design

The balancing circuit topologies were discussed and the simulation results were presented in the previous chapter. The practical consideration of the circuit is studied in this section.

5.2.1 Buck Converter Circuit Design

The buck converter control loop diagram is shown in Fig. 5.2. The control loop consists of an isolated voltage sensor to measure the voltage of the lower capacitor C2, conditioning & anti-aliasing circuits, A/D & digital controller, PWM generator in the DSP chip and an isolated IGBT driver circuit.

The digital controller is designed according to the open loop frequency response. The open loop response without the compensator mainly depends on the equivalent load resistor R_o, inductor L1 and capacitor C2. The resonate frequency is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{5.1}$$

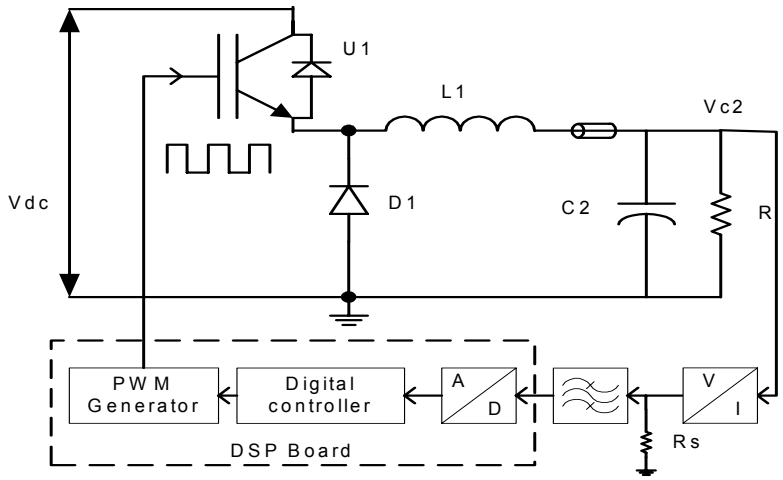

Fig. 5.2 Control loop diagram of the buck converter of the NP voltage control.

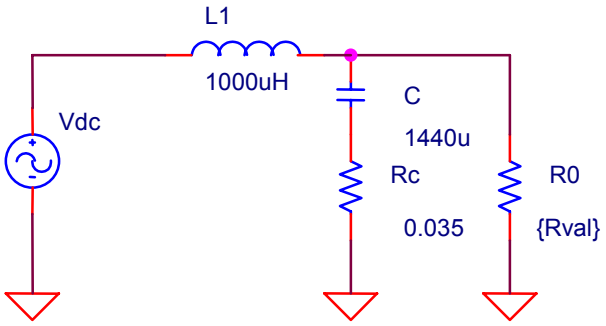

Fig. 5.3

Fig. 5.3 Equivalent Circuit of the buck converter filter.

The L1C frequency characteristic of Fig. 5.3 is shown in Fig. 5.4. From Fig. 5.4, the peak values at f_o vary with R_o variation. The open-loop cross-over frequency of buck converter feedback control loop is ten times less than the L1C resonate frequency f_o. Such a configuration readily guarantees the system stability.

For the dc-bus capacitors, the capacitance is determined by the inverter capacitance. The rectifier filter roll off frequency (-3dB) is given as:

$$f_r = \frac{1}{2\pi\sqrt{R_o C}} \qquad (5.2)$$

$$f_r = \frac{1}{300} f_{in} \sim \frac{1}{100} f_{in} << f_{in} \qquad (5.3)$$

Here, f_{in} is the input frequency of the inverter. And the capacitor is much greater than the requirement of the buck converter. In order to make the control design easy, the inductor L1 must be chosen appropriately to have $\sqrt{\frac{L1}{C}}$ approach Ro as much as possible.

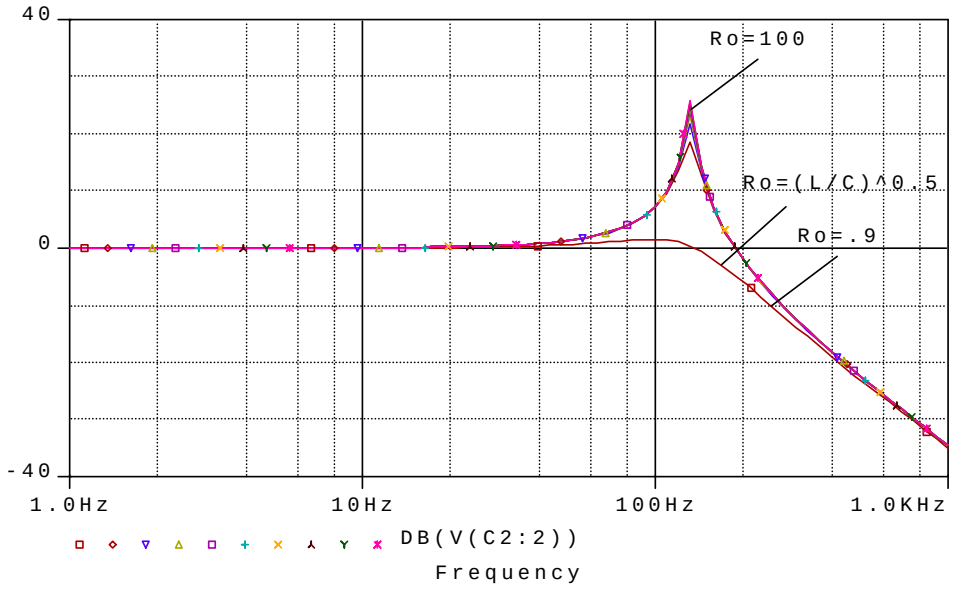

Fig. 5.4 Gain versus frequency for LC filter

Hence, two factors affect the determining value of the inductor L1. One is the current ripple of L1. Another is the bandwidth of the open loop. The maximum inductance of L1 is decided by the NP current variation, $\frac{di_{np}}{dt}$.

$$\frac{di_L}{dt} = \frac{\frac{1}{2}V_{dc}}{L_1} \geq \frac{di_{np}}{dt} \tag{5.4}$$

$$\frac{di_{np}}{dt} = \frac{d}{dt}(I_L \sin(3\omega t + \theta) = 3\omega I_L \cos(3\omega t + \theta) \tag{5.5}$$

$$L_{1\max} = \frac{V_{dc}}{6\omega I_L} \tag{5.6}$$

For a 3-phase, 5hp, 460VAC, 60Hz motor, I_L =9.2A. Assuming I_L =10A and the maximum output frequency is 60Hz, then L_{1max} = 14mH. However, the final value of inductance L1 is decided by a compromise between the inductor ripple current of the buck inverter and its switching frequency, thus:

$$L_1 = \frac{V_{dc}}{2\Delta I_L} \bullet T \tag{5.7}$$

Here T is conduction time, ΔI is current ripple.

Alternatively, consider of the open control loop bandwidth design. For the buck converter frequency characteristic, the open loop bandwidth is limited by the filter resonant frequency f_o shown in Fig. 5.4 if the cross-over frequency is at least 2 or 3 times lower than f_o. Due to the fact that the capacitance of the dc-bus is much larger than that required by the buck converter, the f_o can't be increased unless a smaller inductance values for L1 is chosen. However, a smaller inductance gives rise to a larger current ripple and a higher peak frequency response since $R_o >> \sqrt{\frac{L1}{C}}$ in the frequency response in Fig. 5.4. Hence, a compromise exists between the bandwidth and the current ripple.

The control system precision is determined by the control open loop gain in the effective bandwidth. For the errors caused by the disturbance currents whose frequencies are out of the bandwidth, the buck converter fails to suppress them. They are only controlled by the dc-bus capacitance. The voltages of C2 varying with the NP currents are shown in Fig. 5.5. Because the capacitance of the dc-bus is large enough, it is possible that the variation of NP voltage caused by the NP currents of the higher output frequencies is suppressed by the dc-bus capacitors. Therefore, the bandwidth can be determined by the NP voltage variation magnitude generated by the NP currents. The rule of thumb to choose the bandwidth is as follows.

Considering the worst condition, the maximum of NP current is assumed to be equal to the maximum of the rated load current according to the analysis in Chapter 2. With the following equation, NP voltage variation can be obtained.

$$v_{np} = \frac{I_L}{2\pi fC} \qquad (5.8)$$

When the NP voltage versus frequency characteristic is greater than the setting error of the NP voltage, the corresponding frequency is set as the minimum bandwidth of the open loop. Unfortunately, the bandwidth determined by this method is usually greater than f_o if a larger inductor L1 is selected, because the NP voltage

variation suppressed by the capacitor C exceeds the allowed range with the NP current increase. Therefore, the bandwidth of the buck converter must be decided by the disturbance frequency of interest. Here, the minimum bandwidth is three times as high as the NPC inverter output frequency.

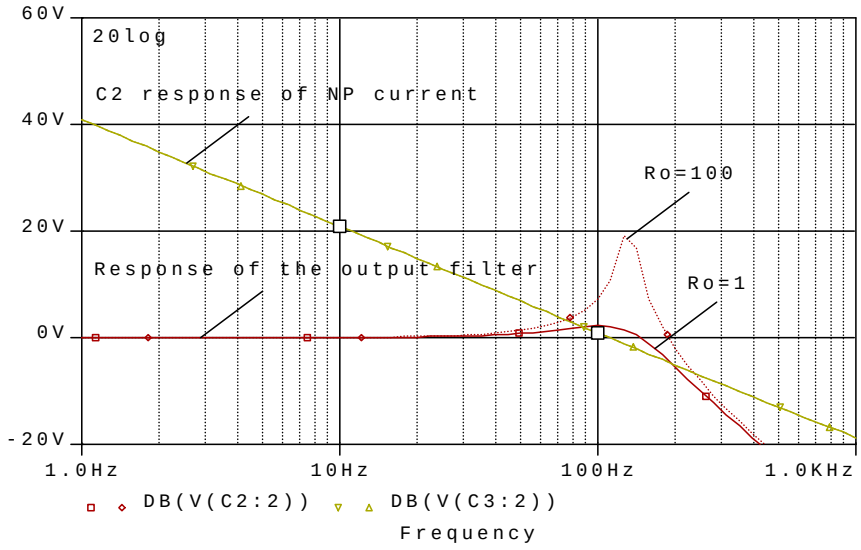

Fig. 5.5 Bode diagram of the LC filter and dc-bus capacitor voltage response to NP current.

In order to minimize the switching frequency effect, the open-loop bandwidth is empirically selected to be less than one tenth of the switching frequency. As the bandwidth of interest is much smaller than the switching frequency, the control loop design can be implemented by the continuous system design method. The balancing circuit switching frequency is chosen as 10kHz considering issues of the switching loss. In addition, a 1mH inductor L1 and two 630μF capacitors for C1 and C2 are used in the balancing circuits for a 5hp AC motor test system.

From all the above considerations, 900Hz for the open loop bandwidth is determined and a leading-lagging compensator, which is realized digitally by DSP control, is applied to enlarge the bandwidth. The open-loop gain bode diagrams are shown in Fig. 5.6.

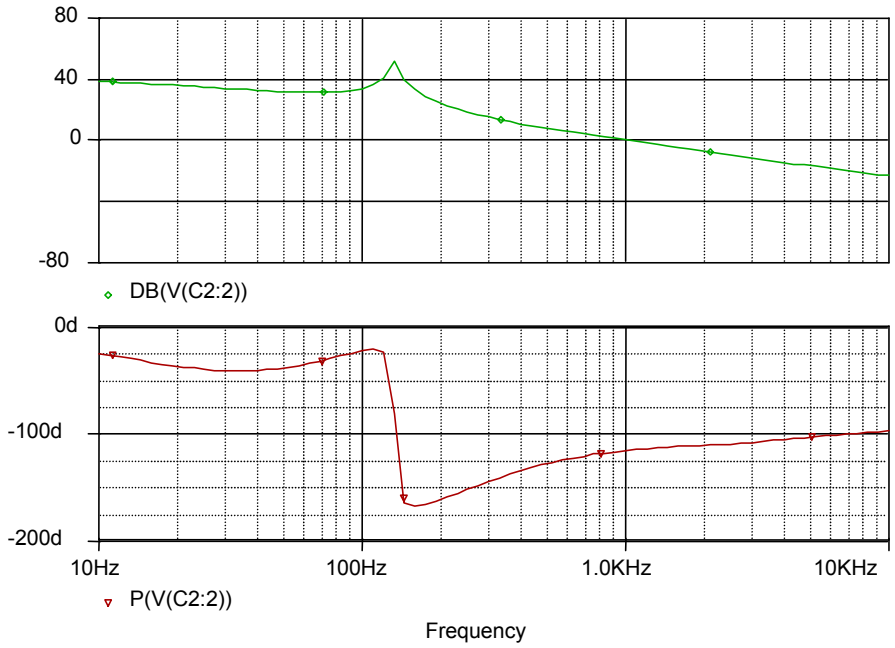

Fig. 5.6 The buck converter open-loop bode diagrams of magnitude (top) and phase (bottom).

5.2.2 Boost Converter Circuit Design

The boost converter is widely used for voltage boost applications. Its simplicity and high efficiency are its main advantages. However, the control stability is an important issue in the boost converter applications due to the existence of a Right-Half-Plane (RHP) zero of its control loop in S-domain. This RHP zero is caused by the delay of the controller delivering energy from the inductor to the load. For example, in Fig. 4.2, an instantaneous load current increment gives rise to a droop in the output voltage. In order to increase the output current, the controller increases the on-time duty to store more energy in the inductor. But it also causes a decreased off-time duty to transfer less energy from the inductor into the capacitor at the same time. This mechanism causes a further decrease in the output voltage. The RHP zero is very

difficult to compensate for. This compensation is discussed in the ride-through design section. Fortunately, when the voltage across the lower capacitor is greater than that across the upper capacitor, the balancing circuit operating in this situation is similar to the buck converter although the topology is like a boost converter. The difference from the normal buck converter is that the current flows from the load rather than into the load.

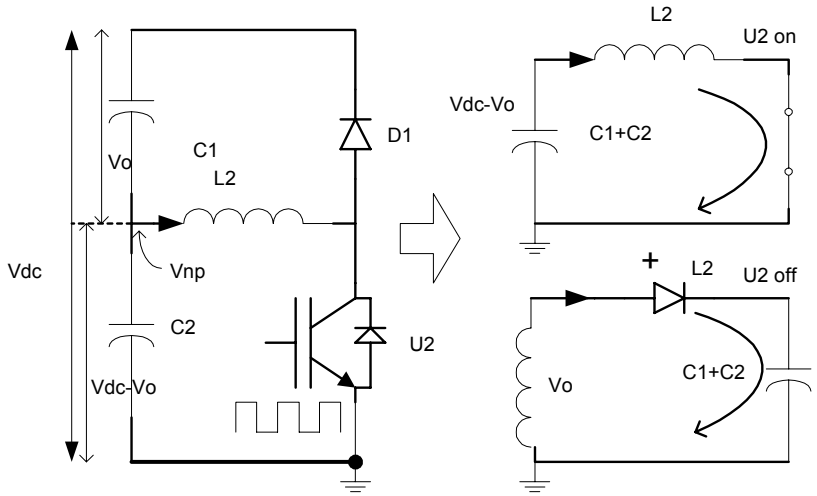

Fig. 5.7 Equivalent small signal circuit of the boost converter.

When V_{C2} is greater than V_{C1}, switching device U2 begins to work and V_{C1} is the control variable Vo shown in Fig. 5.7. During the U2 "on" time, the circuit status is shown in the upper-right figure of Fig. 5.7.

$$V_{L2\_ON} \cdot t_{ON} = (V_{dc} - V_o) \cdot t_{ON} \qquad (5.9)$$

During the period when U2 is off, the circuit becomes that shown in the lower-right figure of Fig. 5.7.

$$V_{L2\_OFF} = V_o \cdot t_{OFF} \qquad (5.10)$$

Here, $t_{ON} = D \cdot T$ and $t_{OFF} = (1 - D) \cdot T$. In the steady state operation of the converter,

$$V_{L2\_ON} \cdot t_{ON} = V_{L2\_OFF} \cdot t_{OFF} \qquad (5.11)$$

Substitute (5.9) and (5.10) into (5.11), to get

$$V_o = D \cdot V_{dc} \qquad (5.12)$$

The same expression as (5.12) can be obtained for the buck converter where Vo represents V_{C2} rather than V_{C1}. From the above analysis, the same control configuration as the buck converter may be applied in the boost converter control by changing the control variables from V_{C2} to V_{C1}. This is very easily realized with the DSP controller. Furthermore, the inductance value of L2 can be selected the same as that of L1 as this scheme is applied.

5.2.3 Other Issues in Balancing Circuit Designs

5.2.3.1 High Frequency Capacitor

The equivalent circuit of one capacitor is shown in Fig. 5.8. It consists of capacitance C_0, the equivalent series resistance (ESR) R_0 and the equivalent series inductance (ESI) L_0. L_0 can be neglected beyond 500kHz. Over a large range of voltage ratings and capacitance values, R_0C_0 tend to be constant. Low ESR resistance of a capacitor can be obtained by choosing a larger capacitance value of the capacitor that is designed for high frequency applications.

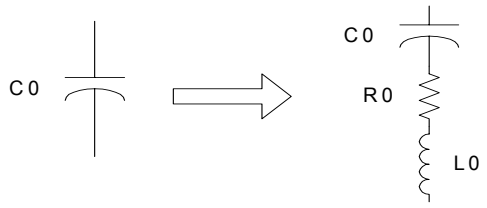

Fig. 5.8 The equivalent circuit of one capacitor.

As the high pulse currents exist in the switching power circuits and the suppressing of voltage ripple is very strict, low ESR and high current capacitors are needed. In the NPC inverter, NP current spikes can be serious as shown in Fig. 5.9. With high *di/dt*, ESR can't be neglected. High NP currents cause more ESR losses in the capacitor. All of the above induce more high frequency voltage ripple on dc-bus, growing higher temperatures in the capacitor, which in turn reduces its lifetime. Therefore, high frequency and low ESR capacitors must be used on the dc-bus of the NPC inverter. However, the capacitor banks on dc-bus usually consist of the conventional aluminum electrolytic capacitors. This kind of capacitor is designed for operation with 50Hz/60Hz rectifiers. Thus, a couple of high switching capacitors combined with the conventional aluminum electrolytic capacitors are used in the balancing circuit design.

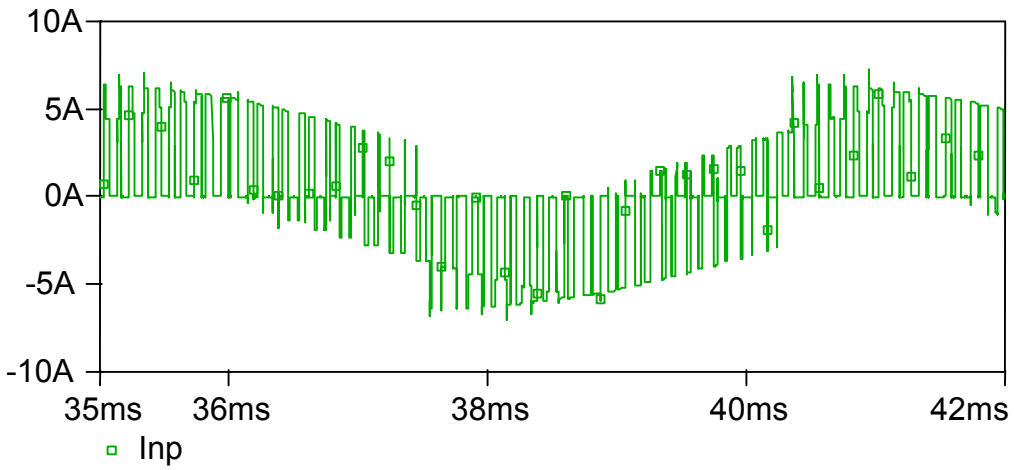

Fig. 5.9 The waveforms of the NP currents with PSpice simulation.

5.2.3.2 Current Feedback Control

A current feedback control can be introduced into the balancing circuits control loop to cancel the effect of the inductors. Fig. 5.10 shows the schematic of th e buck

balancing circuits with a current feedback control loop. This can make the current feedback loop appear as a voltage to current converter when the current feedback loop gain is large enough and hence reduce the order of the output LC filter from the second to the first. The control block diagram is shown in Fig. 5.11. This will make the control loop design easier and solve the overshoot problem in the dc-dc converter. It requires two current transducers for the balancing circuits shown in Fig. 4.3 and one for the simplified balancing circuits shown in Fig. 4.4, respectively.

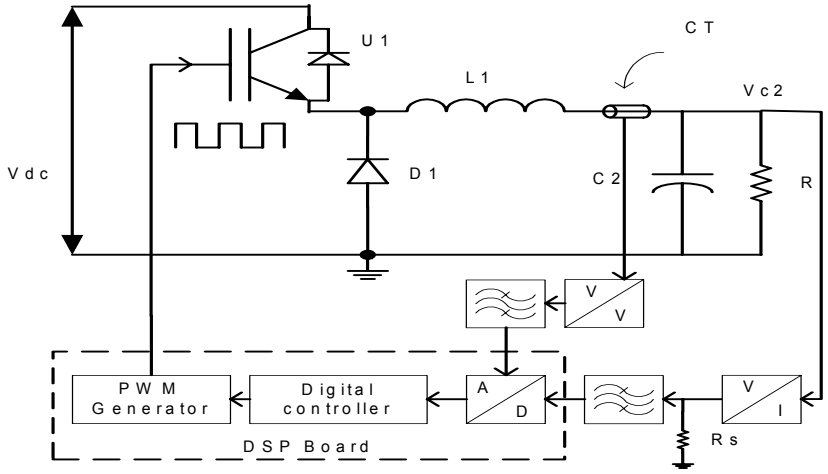

Fig. 5.10 The schematic of balancing circuits control with current feedback loop.

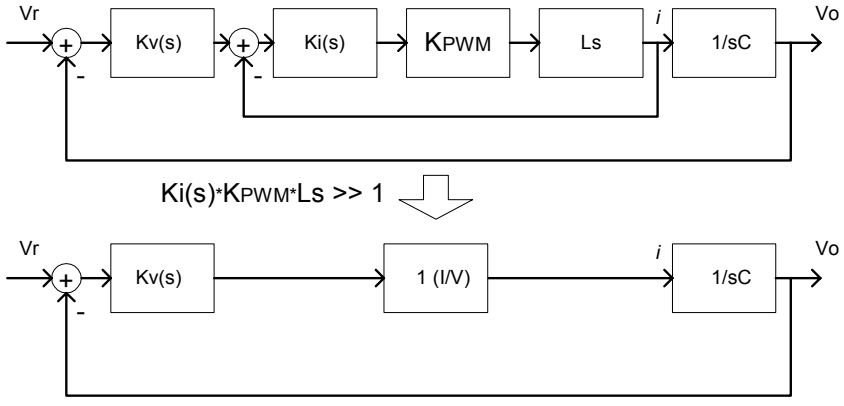

Fig. 5.11 The system block diagram of the balancing circuit.

5.3 Interface Design

The interface board conditions all the analog and digital signals that go into or out of the DSP controller. All signals must be conditioned to conform to the voltage level of the DSP board. Furthermore, a small keypad is placed on the interface board in this NPC inverter design. The designs for the interface circuits are discussed next.

5.3.1 Analog Input Interface Design

Six channels of analog conditioning circuits are needed for the NPC inverter. Two of them are for the dc-bus voltage input. The second pair of them is used for two-phase current measurements on the NPC inverter output. The rest are used to measure the inductor currents of the balancing circuits. As offset and range adjustment of the measurement is needed, voltage level shift circuits must be included in the conditioning circuit. In addition, an anti-aliasing filter is necessary in front of the A/D converters of the DSP controller.

Considering the DSP running speed (clock frequency: 20MHz), the sample frequency is set to 5kHz. The inverter switching frequency is 5kHz and the balancing switching frequency is 10kHz. From the aspect of getting more signal information, a wider bandwidth of anti-aliasing filter is preferred. However, the bandwidth of the anti-aliasing filter must be less than half of the sample frequency. Hence, the bandwidth of the anti-aliasing filter is chosen as 2.5 kHz. This filter is realized by the Sallen-Key low-pass filter shown in Fig. 5.12.

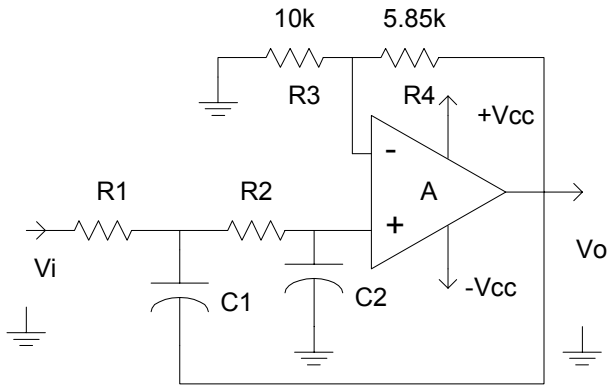

Fig. 5.12 Low-pass Sallen-Key filter circuit.

The second order low-pass filter transfer function is:

$$H_{LP} = -\frac{K}{(\frac{f}{f_C})^2 + \frac{jf}{Qf_C} + 1} \qquad (5.13)$$

Where $f_C = \frac{1}{2\pi\sqrt{R1R2C1C2}}$, $K = 1 + \frac{R4}{R3}$, and $Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2(1-K)}$.

By letting *R1=R2=R, C1=C2=C, K=1+5.85k/10k=1.58*, we can get

$$f_C = \frac{1}{2\pi RC} \qquad (5.14)$$

and $Q=0.707$.

Also, an adjustable high precision voltage reference is designed to offset the transducer operating points. The details of the analog interface circuits are shown in the appendix.

5.3.2 Digital Interface Design

The digital circuit interface includes PWM driver logic circuits, IGBT driver board interface circuits, logic protection circuits and keypad interface circuits. According to the number of the digital I/O ports that the TMS320F240 evaluation

board supplies, the compromise of the I/O assignment can be achieved. The schematic in detail is shown in the appendix. The PWM driver logic circuits are discussed next.

The TMS320F240 has 12 PWM channels. However, only 6 of them have dead-zone time settings. Also, the NPC inverter with NP voltage balancing circuits requires 14 PWM channels. It is very hard to add two more PWM channels into the DSP board or the interface board. A PWM signal assignment circuit is designed to generate the signals to drive the IGBTs. The SPWM generation is shown in Fig. 5.13. From Fig. 5.13, the positive SPWM voltage output goes out of the NPC inverter during the time the reference signal is in the positive half cycle. When the reference signal goes down to the negative, the NPC inverter outputs the positive SPWM voltage. That means the six PWM channels can work for driving the NPC inverter if the appropriate distributing circuit is available.

The schematic of the distribution circuit for one leg is shown in Fig. 5.14. The U/$\underline{\text{L}}$ signal is used to control the inverter to output the positive or negative SPWM voltages. The PWM and the $\underline{\text{PWM}}$ are two of the 6 standard PWM channels featuring full functions in the DSP controller. $\underline{\text{PWM}}$ is the complement of the PWM signal.

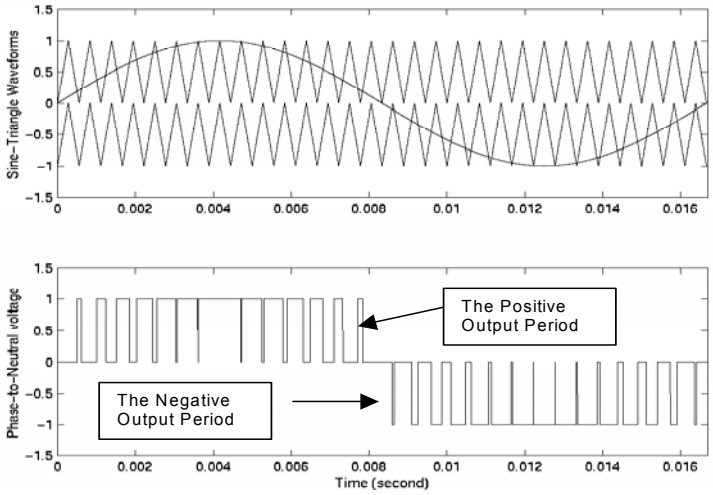

Fig. 5.13 SPWM for the NPC inverter.

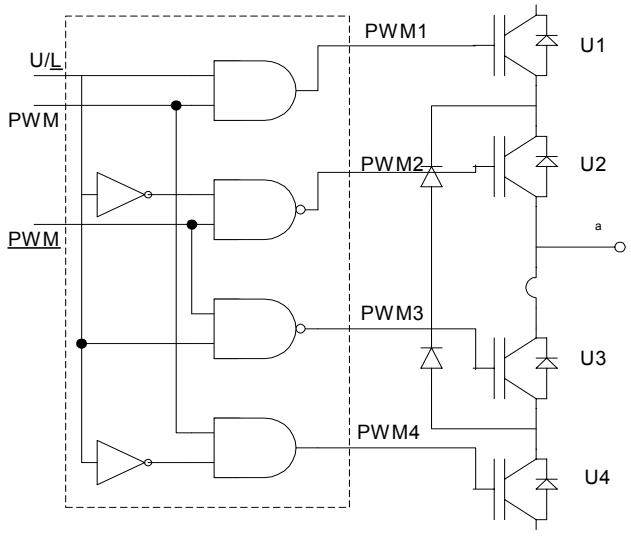

Fig. 5.14 Schematic of the logic circuit to drive the IGBTs of one phase.

When the reference signal is in the positive half cycle, U/L is set to "1", the PWM signal goes to the PWM1 terminal of the logic circuit to control switching device U1. When PWM controls U3, U2 is "ON" and U4 is "OFF" in this period. As the reference signal goes down to the negative, U/L is set to "0". During the negative half cycle, PWM controls U4 and PWM controls U2. But U1 and U3 go to "OFF" and "ON", respectively.

The above logic control circuit is done with two Programmable Logic Array (PLA) chips. The part number used in our application is ATF22V10CQ-15.

5.3.3 Voltage and Current Conditioning Circuits

The voltage measurement circuit consists of a sample resistor and the Hall effect voltage transducer LV 25-P. It supplies galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit). The input voltage can range from 10V to 500V. The voltage measurement circuit is shown in Fig. 5.15. The voltage transducer has a wide bandwidth. The response time at 90% of the primary

voltage is 40μs. Since the maximum dc-bus voltage is 650Vdc for 460VAC input, this meets the requirement of the voltage measurement.

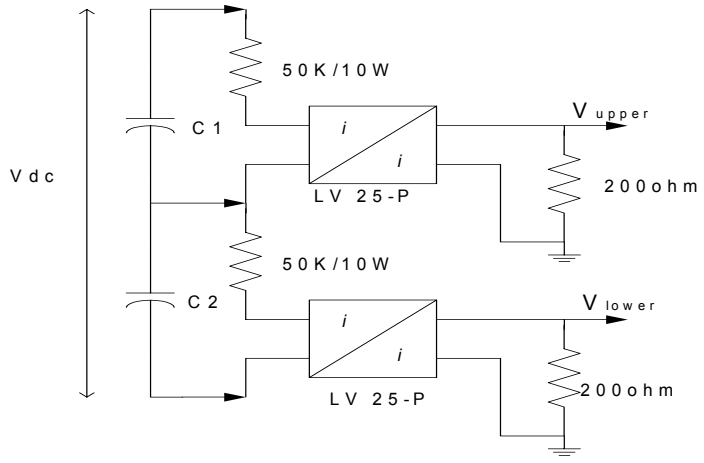

Fig. 5.15 Schematic of the dc-bus voltages measurement circuit.

The current measurements include the two-phase output current measurement in the NPC inverter and two-inductor current measurements in the balancing circuit. For the output current measurement of the NPC inverter, an HEC-02A current transducer is used. Its maximum input current is ±600A and its RMS rated current is 200A. The transfer ratio is 200A/4V. In the balancing circuit, the CSLA1CD current sensor is used for over current protection. The sensed peak current is 57A and the response time is 3μs. The schematic of the current transducer conditioning circuits are shown in appendix B.

5.4 Snubber Design

In the application of IGBTs, snubber circuits are used to protect the IGBTs by improving their switching transient performance. Three types of snubbers are applied

to the IGBTs. They are turn-on snubbers, turn-off snubbers and over voltage snubbers.

1. TURN-ON snubbers: are used to reduce turn-on switching losses at high switching frequencies and limit the maximum diode reverse recovery current.
2. TURN-OFF snubbers: used to reduce the voltage across the IGBT during the time the current is turned off and then reduce turn-off switching losses.
3. OVERVOLTAGE snubbers: minimize the overvoltage caused by the stray inductance.

The overvoltage snubber for a conventional inverter is shown in Fig. 5.16. The snubber for the switching device U1 consists of R1, C1 and D1. Similarly, the snubber for U2 consists of R2, C2 and D2, respectively.

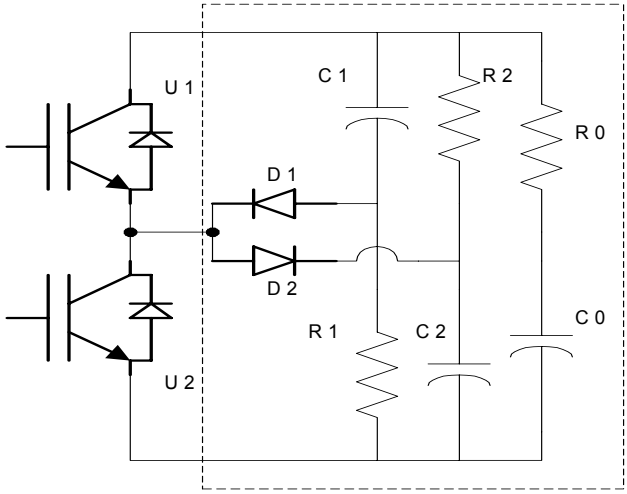

Fig. 5.16 Snubber circuit of the conventional inverter.

In the NPC inverter, overvoltage snubbers are also applied. The topology is shown in Fig. 5.17. *Ri*, *Ci* and *Di* consist of the snubber of the switching device *Ui*. R0 and C0 filter out the noise on the dc-bus. According to [25] and assuming over-voltage is 0.1Vdc,

$$R_i C_i \approx \frac{1}{100} T_{SW} \sim \frac{1}{50} T_{SW} << T_{SW} \qquad (5.15)$$

$$C_i = \frac{100kI_o t_{fi}}{V_{dc}} \tag{5.16}$$

Here k is the factor such that kV_{dc} is the over-voltage without over-voltage snubbers used.

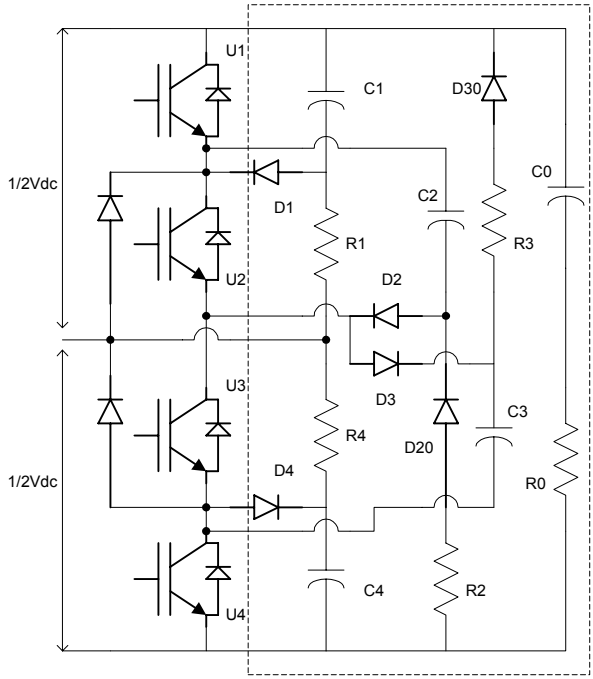

Fig. 5.17 Snubber circuit of the NPC inverter.

6 EXPERIMENTAL RESULTS

6.1 Neutral-Point Voltage Control

The NPC inverter controlled by the TMS320F240 evaluation board can generate 3-phase output voltages in a range of 6Hz to 60Hz. The input voltage is 3-phase 460V 50/60Hz. And the ratio of modulation index to output frequency is constant in order to maintain nearly constant output torque with different output frequencies. For the neutral-point voltage control, half of the dc-bus voltage is set to be the reference of the NP voltage control. When the balancing circuit works during ride-through mode, the reference of the NP voltage is set as 300Vdc. The NP voltage variations with the NP voltage control and without the NP voltage control are measured. In addition, the common-mode voltage mitigation is also applied in the SPWM modulation. The test system consists of a 460V 5hp induction motor.

Fig. 6.1 shows the NPC inverter line-to-line output voltage. From the waveforms, the five-step line-to-line output voltage is obtained by the NPC inverter.

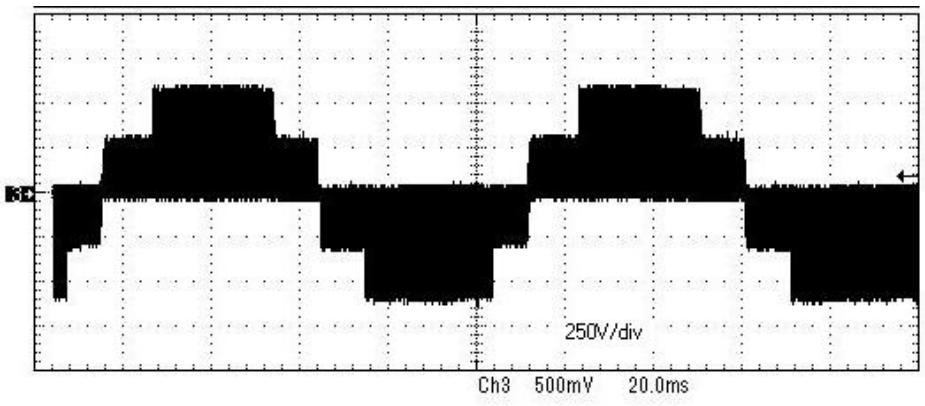

Fig. 6.1 The waveforms of the NPC inverter line-to-line voltage.

The dc-link voltage variation waveforms across C2 are shown in Fig. 6.2, with and without the proposed NP balancing control. The peak-to-peak voltage variation is

30Vpp without NP balancing control and 15Vpp with NP balancing control. It is noted that the additional ripple across C2 is induced by the 3-phase power rectifier. The difference between these experimental results and the simulation results of chapter 4 can be partly attributed to the fact that the simulations were performed under ideal conditions for the balancing circuit and the experimental work has the practical effects of noise. In addition, the practical controller has a 5V dead band error setting. This configuration can suppress the noise of the dc-bus voltage and increase the efficiency of the balancing circuit by setting the control loop to not response to NP voltage errors less than 5V.

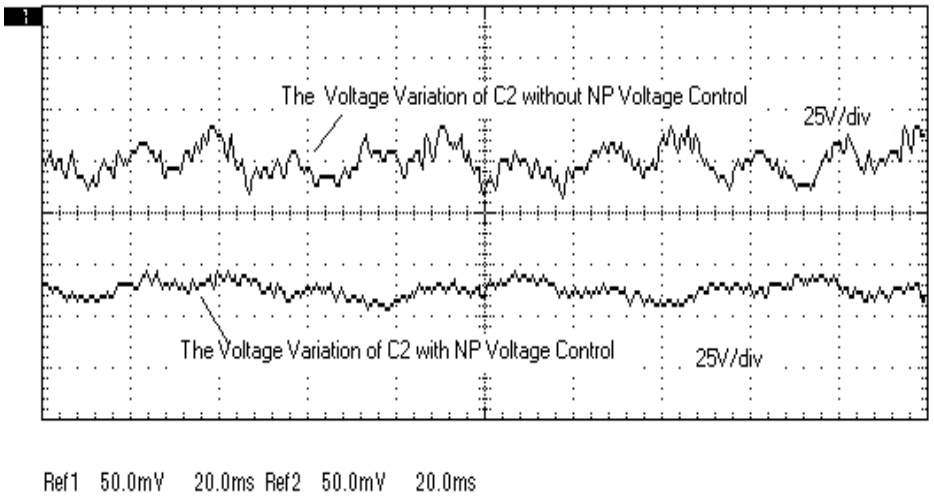

Fig. 6.2 The dc-link voltage variation waveforms across C2 with and without the proposed NP voltage balancing control.

It is difficult to measure the waveforms of common-mode voltage directly unless all three-phase output voltages are measured and added together according to (4.1). Therefore, the shaft voltage is measured here rather than the common-mode voltage. The shaft voltage and bearing current measurements are illustrated in Fig. 6.3. According to the setup shown in Fig. 6.3, the voltage waveforms of the motor shaft isolated from ground are shown in Fig. 6.4. The waveforms demonstrate that the high

performance of NPC inverter can be obtained by the developed common-mode voltage cancellation scheme.

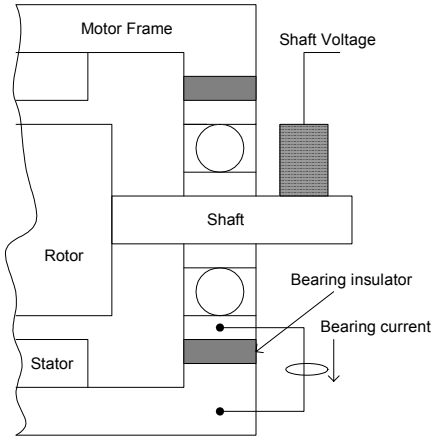

Fig. 6.3 Diagram for the measurements of shaft voltage and bearing current

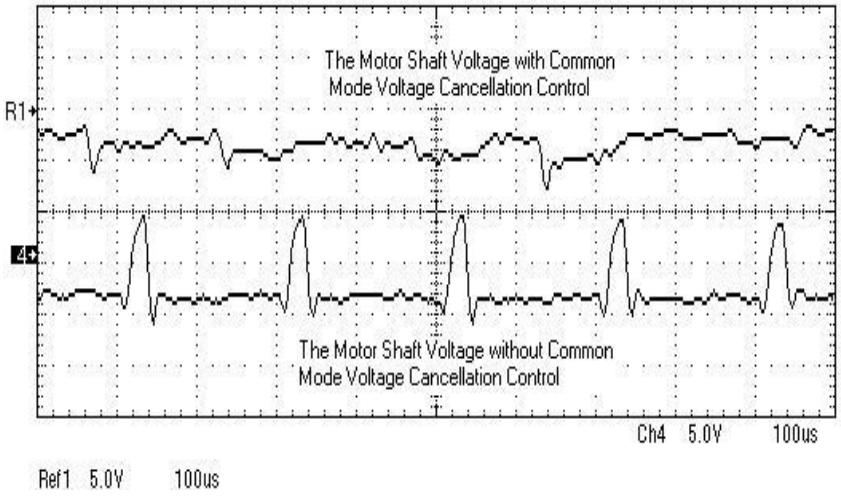

Fig. 6.4 The motor shaft voltage with and without common-mode voltage cancellation control.

6.2 Ride-Through Experiments

The ride-through performance is demonstrated using an example of a 40% single-phase voltage sag, which reduces the rectifier output voltage to 520 Vdc. However, the proposed ride-through approach is set to regulate each capacitor to 300 Vdc, thus maintaining 600 Vdc on the dc-bus. Fig. 6.5 shows the rectifier output dropping to 520Vdc during the sag, and the effect of the ride-through scheme to regulate the total dc-bus voltage, of VC1+VC2, to 600Vdc during the sag (note the scale is 100V/division). Furthermore, the voltage across C2 (300Vdc) shows that the voltages across C1 and C2 are balanced, and each voltage is half of the total dc-bus voltage. Again, the magnitude of the sag that the proposed MLI can ride-through is determined by the selected ratings of the ride-through circuit.

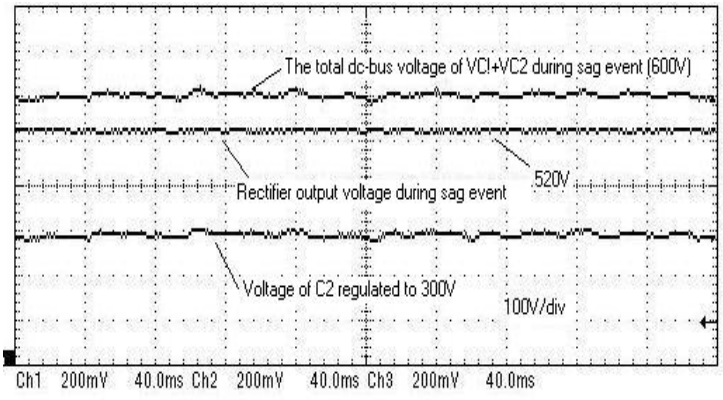

Fig. 6.5 Ride-through performance during a 40% single-phase input voltage sag: The regulated dc-bus voltage of VC1+VC2 (600V, top), the sagged rectifier output voltage (520V, middle), voltage across C2 (300Vdc, bottom) to show that the voltages across C1 and C2 are balanced.

6.3 50KVA NPC Inverter Experiments

In order to present an improved MLI approach at industrial power levels, a 50kVA output was pursued. Thus, the NPC inverter system was upgraded to provide a 50kVA power output. A 460V, 50hp three-phase induction motor with full load

system was used in the experiment. Due to the current limitations of the inductors in the balancing circuits, the 50hp drive experiment was implemented without dc bus balancing control. The current protection and dc-bus capacitor bank were set up for 50kVA. The driven motor was fully loaded on the test-bed in the Motor Systems Resource Facility (MSRF) at OSU. The data measured by the Voltech universal power analyzer PM3300 is listed in Table 6.1. The modulation index is 0.97 and the output frequency is 60Hz in the loaded tests.

	Watts	Volts	Amps	PF	VA	VArs
CH1	11.44k	238.8	60.73	0.788	14.5k	8.92k
CH2	10.62k	236.4	58.80	0.764	13.9k	8.96k
CH3	10.69k	238.6	59.58	0.751	14.2k	9.38k
Σ	32.75k	412.1	59.69	0.768	42.6k	27.26k

Table 6.1. NPC inverter output measurement with load.

6.4 Experimental Conclusions

The experimental results show that the NP voltage can be effectively controlled by a DSP controller. Also, the enhanced ride-through capability can be realized by a modified topology. However, the ride-through capability is dependent on the switching device rating. Furthermore, the inductors need to be redesigned to meet the rating of the ride-through requirements.

7 CONCLUSIONS

7.1 Conclusions

NPC inverters are now widely used in industrial applications. The topology of the series-connected switching devices generates a three-level phase output and a five-level line-to-line output voltage. Thus, there are less harmonics and less voltage stresses applied across the load compared with the conventional two-level inverters. However, neutral-point voltage variation is a serous problem that must be solved in NPC inverter applications. NP voltage variation can cause distortions of the output voltage and excessively high voltages across the switching devices if the neutral-point voltages diverge from the neutral-point of the dc bus voltage. The worst case is during start-up or at very low output frequencies. Furthermore, the neutral-point voltages manifest themselves as common mode voltages on the load, if they are not controlled. In turn, common mode voltages generate shaft voltages that can lead to damaging bearing currents. Bearing currents are reported to be responsible for numerous premature motor bearing failures [9].

The methods to balance the dc bus voltage (control the neutral-point voltage) can be categorized into arithmetic methods and hardware methods. The arithmetic methods include the carrier-based PWM schemes that induce some zero sequence voltage to control neutral-point voltage, and Space Vector Modulation based PWM schemes that make use of the redundant vectors to control the neutral-point current and then suppress the neutral-point voltage variations. All methods can work well under some conditions, but there still are some limitations in the performance and applications. In addition, various techniques to mitigate the common mode voltages were successfully applied in the converter PWM modulations. However, to date there have been no single method presented to resolve the above two problems together. In response to this concern, this dissertation addresses the NP voltage variation control

and pursues the common mode voltage mitigation with a balanced dc bus voltage in NPC inverters.

In this dissertation, the mechanisms of NP voltage variation were presented first. The analysis and simulations have been supplied, and a simple approach to balancing the dc-link voltage has been proposed, which provides enhanced ride-through performance and enables the MLI switching algorithm to be modified for common-mode voltage cancellation. Simulation and experimental results with full DSP control have verified the proposed concepts on 5hp loaded MLI NPC drive systems. With the appropriate design of the balancing controller, the neutral-point voltage variation has been shown to be significantly reduced, while allowing enhanced ride-through performance and common-mode voltage cancellation. The added features of NP balancing and ride-through enhancement come at the expense of with additional components, as detailed in Chapter 4, which increase the cost and complexity of the NPC hardware, the extent of which is dependent on the application.

7.2 Recommendations for Future Work

Commercially available NPC inverters make it possible to construct medium voltage drives with high voltage IGBTs. But NP voltage issues make costly and bulky transformers necessary in commercial systems. Although the proposed approach to control NP potential was designed and implemented through this work, it needs further investigation in high voltage (2300V), high power (10kVA) rating buck-boost circuit designs to make it available in commercial systems. Also, NP voltage variation controlled through the buck-boost circuit by the method of controlling NP current could be a good topic investigated in future work. That might simplify the control loop design of the buck-boost circuit.

In addition to the hardware methods, the combination of different algorithmic methods might be an applicable measure to control NP voltage variation. Space Vector modulation is one of the popular methods used in commercial systems. At

low modulation indexes, the redundant vectors can be used to control NP current, and in turn suppress NP voltage variation. For high modulation indexes, the space vectors that can generate two-level outputs instead of three-level outputs are chosen to drive switching devices in the system. This can make the outputs skip the zero output states or go through transient zero states. It can cause no current or much less current to flow in and out of the NP point so as to reduce NP voltage variation. Because the NPC inverter operates at two-level output modulation with this combination of space vectors, it compromises the NPC inverter performance at high modulation indexes. However, this method might make the input transformer unnecessary in NPC inverters at medium voltage levels. The elimination of the transformer can reduce much of the cost of medium voltage drives and enable more medium voltage level drives applied in ASDs.

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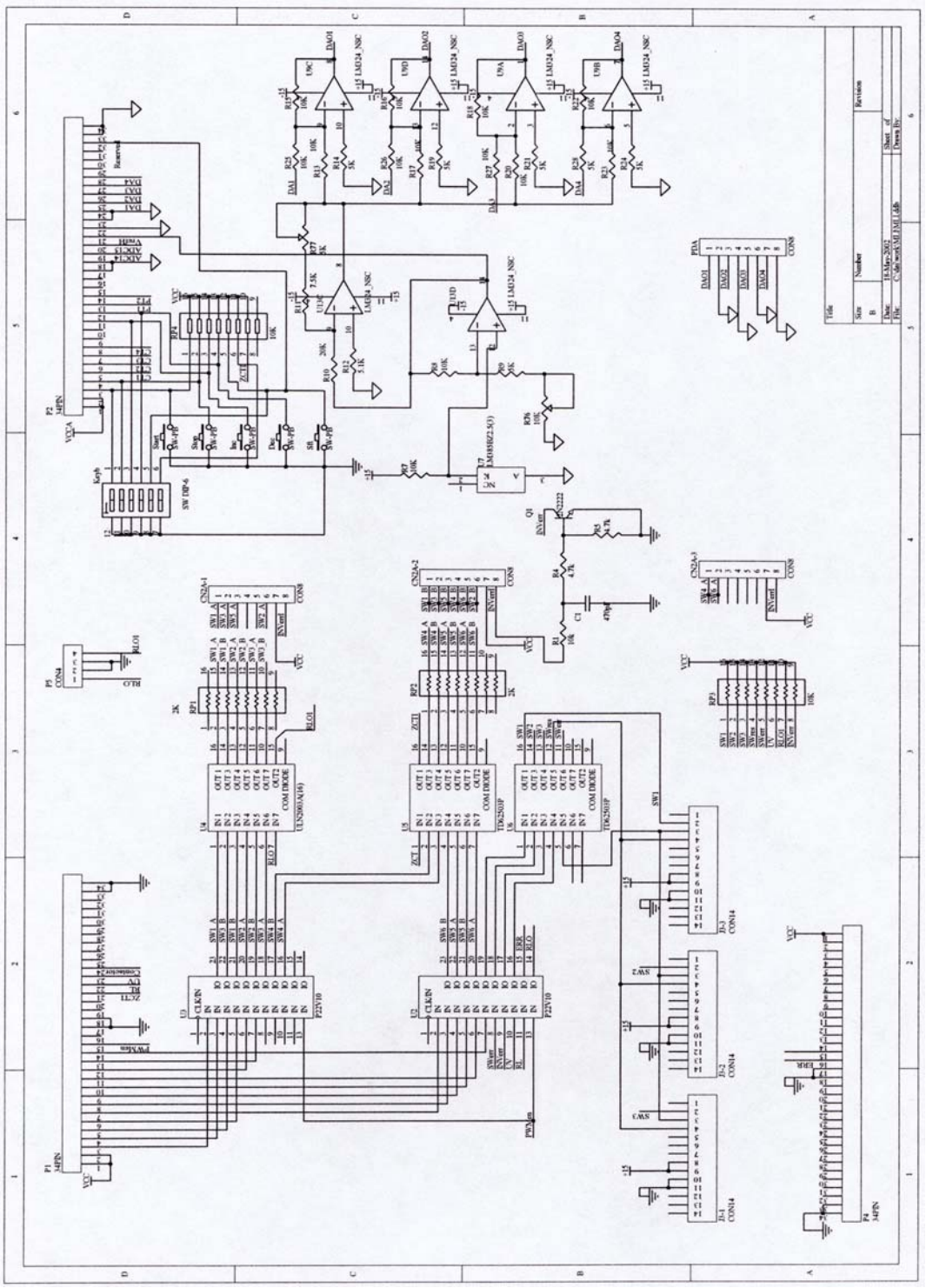
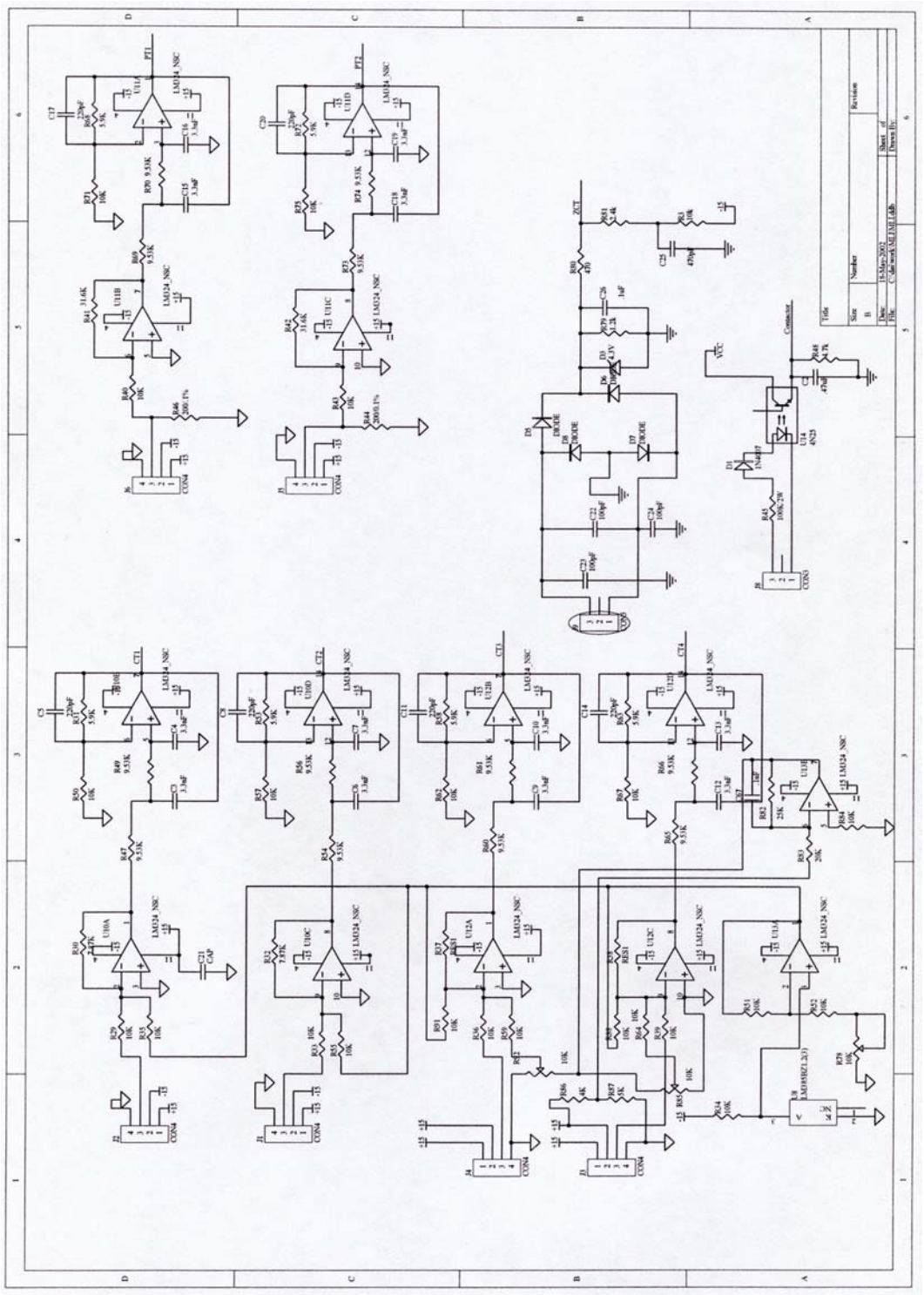
APPENDICES

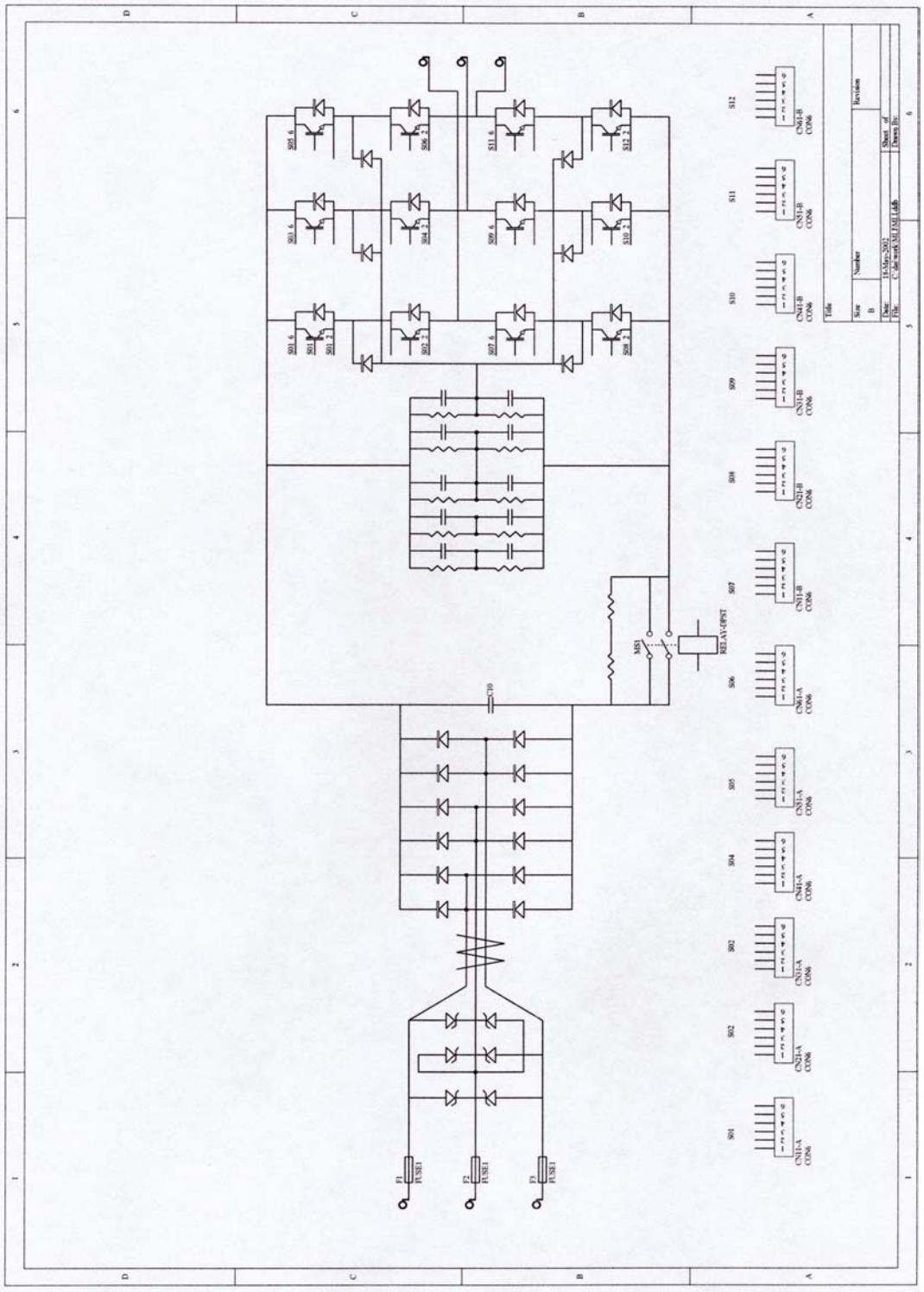
Appendix A. Schematic of digital interface



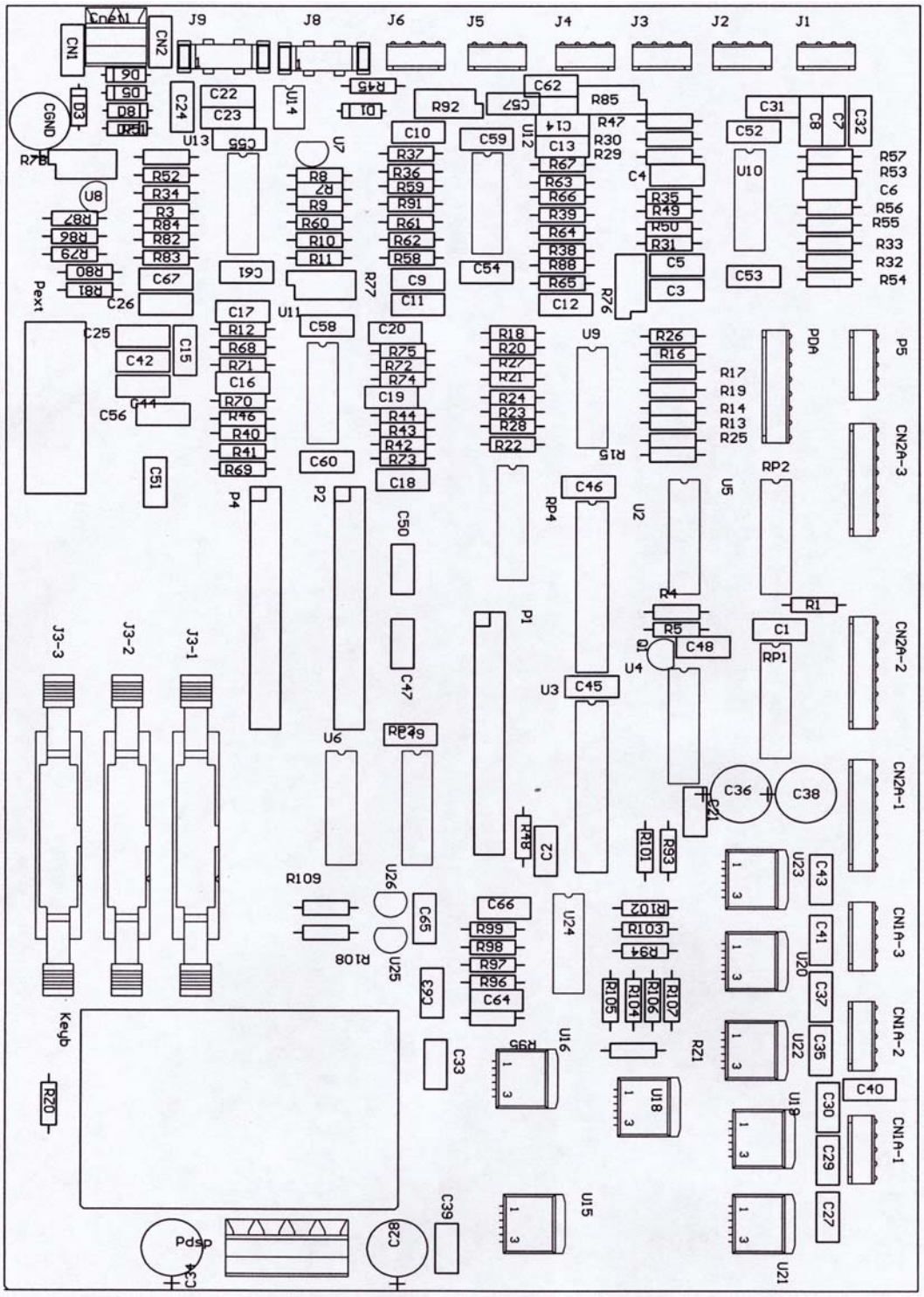
Appendix B. Schematic of analog interface



Appendix C. Schematic of NPC inverter power end



Appendix D. Top silk-layer of the interface board



Appendix E. Code for PLDs

```
PALASM Design Description for PLD1
;---------------------------------- Declaration Segment ------------
TITLE    PWMDECOD.PDS
PATTERN  A
REVISION 2.0
AUTHOR   S.Dai
COMPANY  Oregon State Univ.
DATE     05/26/02

CHIP  PWM_CTRL  PAL22V10

;---------------------------------- PIN Declarations ---------------
PIN  2        PWM2                COMBINATORIAL          ; INPUT
PIN  3        PWM1                COMBINATORIAL          ; INPUT
PIN  4        PWM4                COMBINATORIAL          ; INPUT
PIN  5        PWM3                COMBINATORIAL          ; INPUT
PIN  6        PCTL1               COMBINATORIAL          ; INPUT
PIN  7        PCTL2               COMBINATORIAL          ; INPUT
PIN  12       GND                                        ; INPUT
PIN  13       /EN           COMBINATORIAL                ; INPUT
PIN  16       SW4_B              COMBINATORIAL           ; OUTPUT
PIN  17       SW4_A              COMBINATORIAL           ; OUTPUT
PIN  18       SW3_B              COMBINATORIAL           ; OUTPUT
PIN  19       SW3_A              COMBINATORIAL           ; OUTPUT
PIN  20       SW2_B              COMBINATORIAL           ; OUTPUT
PIN  21       SW2_A              COMBINATORIAL           ; OUTPUT
PIN  22       SW1_B              COMBINATORIAL           ; OUTPUT
PIN  23       SW1_A              COMBINATORIAL           ; OUTPUT
PIN  24       VCC                                        ; INPUT

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

 SW1_A = PWM1*PCTL1*/EN
 SW2_A = PWM2*/PCTL1*/EN+PCTL1*/EN
 SW1_B = PWM2*PCTL1*/EN+/PCTL1*/EN
 SW2_B = PWM1*/PCTL1*/EN

 SW3_A = PWM3*PCTL2*/EN
 SW4_A = PWM4*/PCTL2*/EN+PCTL1*/EN
 SW3_B = PWM4*PCTL2*/EN+/PCTL1*/EN
 SW4_B = PWM3*/PCTL2*/EN
```

```
PALASM Design Description for PLD2
;---------------------------------- Declaration Segment ------------
TITLE    PWMDECOD.PDS
PATTERN  A
REVISION 2.0
AUTHOR   S.Dai
COMPANY  Oregon State Univ.
DATE     05/26/02
CHIP  PWM_CTRL2  PAL22V10

;---------------------------------- PIN Declarations ----------------
PIN  2        PWM6              COMBINATORIAL          ; INPUT
PIN  3        PWM5              COMBINATORIAL          ; INPUT
PIN  4        SW1          COMBINATORIAL               ; INPUT
PIN  5        SW2          COMBINATORIAL               ; INPUT
PIN  6        SW3          COMBINATORIAL               ; INPUT
PIN  7        PCTL3             COMBINATORIAL          ; INPUT
PIN  8        SWERR             COMBINATORIAL          ; INPUT
PIN  9        INVERR            COMBINATORIAL          ; INPUT
PIN  10        UV          COMBINATORIAL               ; INPUT
PIN  11        RL          COMBINATORIAL               ; INPUT
PIN  12        GND                                     ; INPUT
PIN  13        /EN         COMBINATORIAL               ; INPUT
PIN  14        RLO            COMBINATORIAL            ; OUTPUT
PIN  15        ERR            COMBINATORIAL            ; OUTPUT
PIN  16        SWRST             COMBINATORIAL         ; OUTPUT
PIN  17        SW3_O             COMBINATORIAL         ; OUTPUT
PIN  18        SW2_O             COMBINATORIAL         ; OUTPUT
PIN  19        SW1_O             COMBINATORIAL         ; OUTPUT
PIN  20        SW6_B             COMBINATORIAL         ; OUTPUT
PIN  21        SW6_A             COMBINATORIAL         ; OUTPUT
PIN  22        SW5_B             COMBINATORIAL         ; OUTPUT
PIN  23        SW5_A             COMBINATORIAL         ; OUTPUT
PIN  24        VCC                                     ; INPUT
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

 SW5_A = PWM5*PCTL3*/EN
 SW6_A = PWM6*/PCTL3*/EN+PCTL3*/EN
 SW5_B = PWM6*PCTL3*/EN+/PCTL3*/EN
 SW6_B = PWM5*/PCTL3*/EN

 RLO = RL
 ERR = SWERR+INVERR+UV+PWM4*/PCTL2*/EN+PCTL1*/EN
 SW1_O = SW1*/EN
 SW2_O = SW2*/EN
 SW3_O = SW3
 SWRST = /EN+SWERR
```