AN ABSTRACT OF THE DISSERTATION OF

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Title: Timing Jitter and Phase noise in Electronic Oscillators

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In the first part of this dissertation, low frequency l/f or flicker noise in the frequency range of Hz to kHz has been identified and demonstrated to be described by temperature fluctuations in heat conduction in bipolar transistors operated at higher power densities. This noise phenomenon is not described by current SPICE programs used in circuit simulations. This noise in the kHz range can modulate LC oscillators and can be the determining factor in causing phase noise in modern wireless communication systems. At lower frequencies or lower power densities flicker noise may still result from number fluctuations or mobility fluctuations but this is not as important in determining the phase noise at kHz offsets from the carrier frequencies.

In the second part of this dissertation work, we have developed a large signal non-linear transient simulation technique to simulate phase noise due to device noise in electronic oscillators. Simulation results are consistent with Leeson's theory and the magnitude of the sidebands directly scales with the magnitude of injected noise. Simulation also shows phase noise at 4.7 MHz frequency offset is white noise

dominated and in good agreement with the experimental data reported in the literature.

In the third part of this dissertation work, we have developed a large signal non-linear transient simulation technique to simulate timing jitter in electronic oscillators. Simulation results are consistent with the accepted theory, analytical formula and A.Hajimiri's analytical model for white noise. Two important parameters cycle jitter, and cycle to cycle jitter used to describe jitter performance can be obtained from simulation. Simulation results are also compared with measurement and close agreement was observed between them.

We have employed this methodology and investigated the timing jitter in silicon BJT /or SiGe HBT ECL ring oscillators, and we have shown silicon BJT /or SiGe HBT ring oscillators have lower jitter compared to their CMOS counterparts. As such silicon BJT and/or SiGe HBT ring oscillators are a potential choice for low jitter applications.

Timing Jitter and Phase Noise in Electronic Oscillators

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TIMING JITTER AND PHASE NOISE IN ELECTRONIC OSCILLATORS

1. INTRODUCTION

Noise is an important design factor in electronic systems, it determines the lower limit on the level of the signal that can be processed by these devices and circuits. It is very important to understand the mechanism of noise sources.

Generally, there are two groups of noise sources, which are usually classified as device noise and interference. Device noise includes thermal, shot and flicker noise, while interference includes substrate and power supply noise. There is always some way to alleviate substrate and power supply noise but not for device noise.

Of all the noise sources, the origin of flicker noise, which is also known as 1/f noise because the noise spectral density is inversely proportional to frequency, is still unknown. In the past forty years, a large number of papers have been published on the study of 1/f noise in MOSFET's and BJT's [1-46], but controversy still exists and there is no generally accepted model.

In the case of BJT's, one of the original references on flicker noise in bipolar transistors, by E.R. Chenette *et al*., [43] is still used as the basis for modeling noise in bipolar transistors. It gives the low frequency l/f or flicker noise as:

$$\overline{i_n^2} = K \; I_B^n \; / \; f \qquad (1.1)$$

where K is a constant, I_B is the base current, n is a number between one and two, and f is the frequency. Subsequently the physical mechanism for this noise has been attributed to either mobility fluctuations, as described by Hooge's empirical formula,

and/or surface state effects in the base-emitter junction, there is still no universally accepted model. An equation of the above form is used in SPICE, PSPICE and HSPICE models for circuit simulations. However, the original publication [43] also described a component that depended on, V_{CE}, or the collector emitter voltage, although no model or equation was given for this component. Recently we have been able to show that at high power density or high junction temperatures of operation the 1/f noise varies with power dissipation [45], in particular as the collector current is held constant and the collector emitter voltage is varied [46]. In these reports, however, we were there primarily interested in publishing the theoretical results and showing the functional form of the equation describing the manner in which the 1/f noise varies. We did not demonstrate a detailed correspondence. In the research work presented in this dissertation, we will give a detailed comparison between the theory and the 1/f noise measured on bipolar transistors and show that the low frequency noise at higher junction temperatures is described by temperature fluctuations in heat conduction [45,46]. These new results are particularly relevant to phase noise in voltage-controlled oscillators operating with low base circuit impedance since they determine the phase noise at kHz offsets from the carrier frequencies.

Oscillators are integral parts of many electronic applications. For a noise free oscillator, the output is a perfect timing reference with a periodically time-variant signal. However, in reality, due to the existence of noise, all oscillators will exhibit phase noise and timing jitter. Phase noise and timing jitter are the same phenomena

except one description is used in the frequency domain and the other is used in the time domain. Analog and digital designers prefer using phase noise and timing jitter respectively.

With the fast development of wireless communication, there is an increased demand for more available channels, thus RF oscillators employed in wireless communication must meet more stringent requirements for phase noise. The term phase noise, which is used to describe frequency stability, has been widely studied in the past [49-56]. There have been some models developed for predicting phase noise in oscillators, however, those models are based on linear circuit concepts and oscillators are basically non-linear large signal circuits. The time varying nature of oscillators and large non-linearity's have precluded any meaningful application of techniques based on linear approximations, the simulations must be performed in the time domain. In this study, we will develop a large signal transient simulation technique to simulate phase noise due to device noise in a 2-G Hz BJT LC oscillator.

Timing jitter is critical design considerations in nearly every type of digital systems, especially for some high-speed digital circuits such as microprocessors and memories. There have been some studies about timing jitter in electronic systems [57-68], however, none of them describe an efficient technique to simulate jitter. Although some analytical models have been reported for jitter in oscillators [69-73], these models have been developed for white noise only while jitter due to 1/f noise is usually more important since it increases linearly with time. There has been no simulation technique to predict timing jitter due to flicker noise. The lack of a

simulation technique to accurately predict timing jitter makes design of low jitter systems a problem. In this study, we will try to develop a method to efficiently simulate timing jitter.

The possible sources of timing jitter are substrate and power supply noise, and inherent electronic noise of devices such as flicker and white noise. Since there is always some way to alleviate substrate and power supply noise, in a fully optimized design the main source of timing jitter is the inherent electronic device noise, in this work we will only concentrate on jitter due to 1/f and white noise. However, the method described in this study is also applicable to substrate and power supply noise.

The organization of this dissertation work is as follows, in chapter 2, first we will give a general review of noise models in CMOS and BJT devices, then we will describe a new model of 1/f noise in BJT devices based on temperature fluctuations.

In chapter 3, a technique to transform frequency domain noise power into time domain noise data is introduced.

In chapter 4, phase noise resulting from white and flicker noise in a BJT LC oscillator is investigated. Large signal transient time domain SPICE simulations of phase noise resulting from the random-phase flicker and white noise in a 2 GHz BJT LC oscillator have been performed and demonstrated. The simulation results are compared with experimental result reported in the literature.

In chapter 5, we are developing an extension of our large signal transient simulation technique of phase noise to the simulation of timing jitter. Timing jitter due to device noise in a three stage single ended CMOS ring oscillator is studied, and a

methodology to efficiently simulate timing jitter has been developed. Simulation results are discussed and compared with analytical model.

In chapter 6, we have employed this methodology and simulated timing jitter in a nine stage differential CMOS ring oscillator, simulation results are discussed and compared with experimental results.

In chapter 7, we have employed this methodology and investigated the timing jitter in silicon BJT /or SiGe HBT ECL ring oscillators, and we have shown BJT /or SiGe HBT oscillators have lower jitter compared to their CMOS counterparts.

In chapter 8, the conclusions are discussed.

2. NOISE MODELS IN CMOS AND BJT DEVICES

2.1 Current Noise Models in CMOS and BJT Devices

For active MOSFET transistors, dominant noise sources are flicker and thermal noise. In HSPICE, channel thermal noise and flicker noise are modeled by a current source and expressed by the following equations.

For flicker noise,

(i) noimod = 1 noise model

$$\overline{I_{nd}^{\,2}} = \frac{KF \cdot g_m^{\,2}}{C_{ox} \cdot W_{eff} \cdot L_{eff} \cdot f^{AF}} \tag{2.1}$$

(ii) noimod = 2 noise model

$$\overline{I_{nd}^{\,2}} = \frac{q^2 kT\mu_{eff} I_{ds}}{C_{OX} L_{eff}^{\,2} f^{ef} \bullet 10^8}\{Noia \bullet \log\{\frac{N_0 + 2\times 10^{14}}{N_l + 2\times 10^{14}}\} + Noib \bullet (N_0 - N_l)$$

$$+ \frac{Noic}{2}\{N_0^{\,2} - N_l^{\,2})\} + \frac{V_{tm} I_{ds} \Delta L_{clm}}{W_{eff} L_{eff}^{\,2} f^{ef} \bullet 10^8} \bullet \frac{Noia + Noib \bullet N_l + Noic \bullet N_l^{\,2}}{(N_l + 2\times 10^{14})^2} \tag{2.2}$$

A noise equation selector parameter noimod is used to select whether noimod=1 or noimod=2 noise model is used in the small signal AC noise analysis. In noimod=1 noise model, AF is flicker noise exponent which is 1 at default and KF is flicker noise coefficient. Reasonable values for KF are in the range of 1 x 10^{-19} to 1 x 10^{-25} V^2F.

For thermal noise in channel,

$$\overline{I_{nd}^{\,2}} = \frac{8 \cdot kT \cdot g_m}{3} \tag{2.3}$$

Noise sources in bipolar transistors include shot noise due to collector and base currents, which can be modeled as follows

$$\overline{I_{nb}^{\,2}} = 2qI_b \tag{2.4}$$

$$\overline{I_{nc}^{\,2}} = 2qI_c \tag{2.5}$$

where q is the magnitude of electronic charge (1.6 x 10^{-19} C), I_b is the base current, I_c is the collector current.

Thermal noise of the base resistance, modeled as

$$\overline{V_{nb}^{\,2}} = 4kTr_b \tag{2.6}$$

and the flicker noise of the base current,

$$\overline{i_n^2} = k_F I_b^n / f \tag{2.7}$$

where K_F is a constant, I_b is the base current, n is a number between one and two, and f is the frequency.

The current flicker noise model in bipolar transistors is based upon original work done in the 1963 time frame [43]. At that time and given the state of technology with only poor surface passivation techniques, the l/f noise in bipolar transistors was all attributed to surface effects [1] in the base-emitter junction. This leads to the commonly used pi-model for noise in bipolar transistors, or Van der Ziel model, described in most textbooks [48] and circuit simulation programs based on SPICE. This overlooks the more recent work and perhaps better-accepted model for l/f noise in that it is not a surface effect but rather a bulk phenomena [3,22] described by

Hooge's equation. Unfortunately, Hooge's equation is only an empirical one. In the following, we will introduce a new flicker noise model, which is described by temperature fluctuations in heat conduction.

2.2 1/f noise Due to Temperature Fluctuations in Heat Conduction in Bipolar Transistors

2.2.1 Theory

The R-C transmission lines previously analyzed [45,46] are diffusion lines and potential and currents are described by the diffusion equation;

$$\frac{\partial^2 V}{\partial x^2} = R\,C\,\frac{\partial V}{\partial t} \tag{2.8}$$

This is the same type of equation describing heat conduction [47];

$$a\,\frac{\partial^2 T}{\partial x^2} = \frac{\partial T}{\partial t} \tag{2.9}$$

where, a, is the thermal diffusivity, m^2/sec in MKS units and, T, is the temperature. Based on the solution in rectangular coordinates, a mean square fluctuation in the collector current or mean square noise current equation can be obtained as [46]:

$$\overline{i_n^2} = 2qI\left(\frac{\Delta V}{(kT/q)}\right)^2\left(\frac{\Delta T}{T}\right)^2\left(\frac{\omega_{cth}}{\omega}\right) \tag{2.10}$$

where now,

$$\Delta T = V_{CE}\;I\,\frac{d}{K\;A} \tag{2.11}$$

As it turns out the approximation in rectangular coordinates of a plate-wall model is probably not a good approximation of the actual situation. A more complicated but better fitting model to the actual situation is one in spherical coordinates which is analyzed in the following sections. In the spherical coordinates, an equivalent circuit representation can be made for heat conduction as shown in Fig. 2.1 where for each volume element,

$$R=\mathrm{l}/(\mathrm{K}4\pi r^2) \qquad K/W\cdot m \tag{2.12}$$

$$C=C_p\,\rho\,4\pi r^2 \qquad J/K\cdot m \tag{2.13}$$

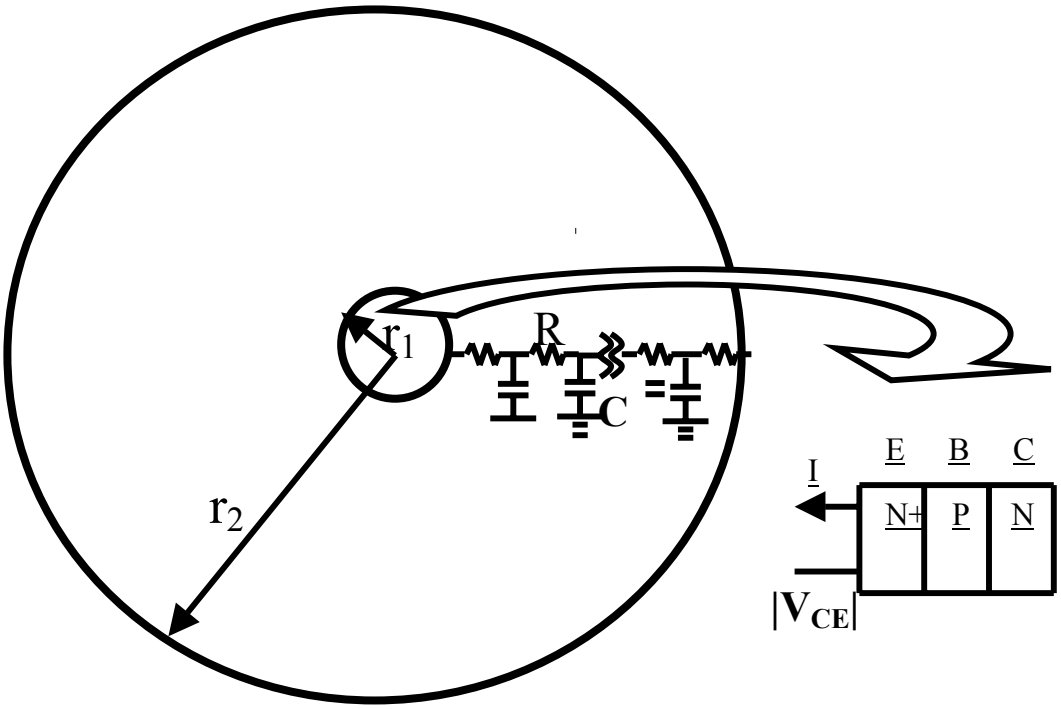


Figure 2.1 Power dissipation in a transistor and heat conduction model in spherical coordinates

where, K, is the thermal conductivity, C_p , the heat capacity, ρ , the density, and, $4\pi r^2$, the surface area of the sphere whose radius is, r, through which there is heat conduction. Temperature is analogous to voltage and heat flux analogous to current. The thermal conductivity and diffusivity are not independent but are related in a form which we will later find useful,

$$\frac{a}{\mathrm{K}} = \frac{1}{C_p\ \rho} \qquad \frac{K \cdot m^3}{J} \tag{2.14}$$

The time invariant steady state, or DC, solution for this line when terminated by a heat sink with infinite heat capacity is then a linear variation in temperature and the thermal impedance is,

$$Z_S(DC) = R_{DC}\ ,$$

$$R_{DC} = \int_{r1}^{r2} R\,dr = \int_{r1}^{r2} \frac{1}{4\pi K r^2}\,dr = \frac{1}{4\pi K}\left(\frac{1}{r_1} - \frac{1}{r_2}\right) \approx \frac{1}{4\pi K r_1} \tag{2.15}$$

Here we assume r_2 is infinite. From results shown later we know that, $r_1 << r_2$, so this assumption is reasonable.

The heat flux; $flux = k 4\pi r^2 \frac{dT}{dr}$ and for the total line

$$flux = \frac{\Delta T}{R_{DC}} \tag{2.16}$$

The steady state time dependent solutions of this differential equation and transmission line, from r_1 to r_2, in response to a high frequency sinusoidal excitation in temperature T at the sending end of this line are described by the AC impedance looking into this line, Z_S .

A. Solutions with an infinite heat sink

We have previously always assumed an infinite heat sink at the interface between the device and the outside world. An infinite heat sink is one with infinite heat capacity or infinite capacitor which acts as a short circuit on the line at all frequencies. At very low frequencies, then the sending end impedance Z_S is just R_{DC}. At higher frequencies, the sending end impedance is very difficult to calculate and express using a simple formula. However if frequencies are high enough the line will be a long lossy line and then the sending end impedance is just Z_o, where;

$$Z_O = \frac{Z}{Y} = \sqrt{\frac{R}{j\omega C}} = \frac{1}{4\pi K r^2}\sqrt{\frac{a}{j\omega}},$$

$$\left|Z_S(r_1)\right|^2 = \left|Z_O(r_1)\right|^2 = \frac{a}{(4\pi K)^2 \omega r_1^4} = \frac{R_{DC}^2 a}{r_1^2 \omega} \tag{2.17}$$

if we let $\omega_{cth} = \frac{a}{r_1^2}$, then Eqn. (2.17) also can be written as

$$\left|Z_S(r_1)\right|^2 = \frac{R_{DC}^2 \omega_{cth}}{\omega} \tag{2.18}$$

Fig. 2.2(b) shows then the impedance looking into the transmission line with a short circuit termination with a $l/\omega^{1/2}$ frequency dependence.

B. Solutions without an infinite heat sink

Apparently the assumption or approximation of an infinite heat sink at the interface between the device and the outside world is probably not a good approximation nor very representative of the actual situation. The next simplest assumption is one

where there is a finite thermal resistance between the device and a large heat sink or the outside world shown as $R_{contact}$ in Fig. 2.2(a) and the heat capacity of the sink is shown as C_{sink}. If this thermal contact resistance is very high then the line can be regarded as being open circuited. In this case the temperature fluctuations are limited by the total heat capacitance of the device,

$$C_{total} = \int_{r_1}^{r_2} C_p \rho 4\pi r^2 dr = \frac{4}{3} C_p \rho \pi (r_2^3 - r_1^3) \approx \frac{4}{3} C_p \rho \pi r_2^3 \tag{2.19}$$

This will become important at radian frequencies, ω_x, which is the corner frequency between this capacitance and the total DC heat resistance of the sample, R_{DC}:

$$\omega_x = \frac{1}{C_{total} R_{DC}} = \frac{K 4\pi r_1}{C_p \rho \frac{4}{3} \pi r_2^3} = \frac{3 a r_1}{r_2^3} \tag{2.20}$$

If $\omega < \omega_x$, the line appears capacitive, and the sending end impedance is just

$$|Z_S| = \frac{1}{C_p \rho \frac{4}{3} \pi r_2^3 \omega} \tag{2.21}$$

Fig. 2.2(b) also shows the impedance looking into the transmission line with an open circuit termination with a $1/\omega$ frequency dependence.

If there is a finite thermal contact resistance $R_{contact}$ connected to a large capacity heat sink, the DC resistance at low frequency will be the sum of the DC thermal resistance of the line and the contact resistance. While the solutions to the transmission line equations would be difficult to obtain with this finite termination they can be estimated as illustrated in Fig. 2.2(b). We can see the transmission line can be approximated by short-circuited characteristics at high frequencies, which would result in an approximate, $1/\omega^{1/2}$, frequency dependence of the thermal

impedance. Since the noise in the kHz range can modulate LC oscillators and can be the determining factor in causing phase noise in modern wireless communication

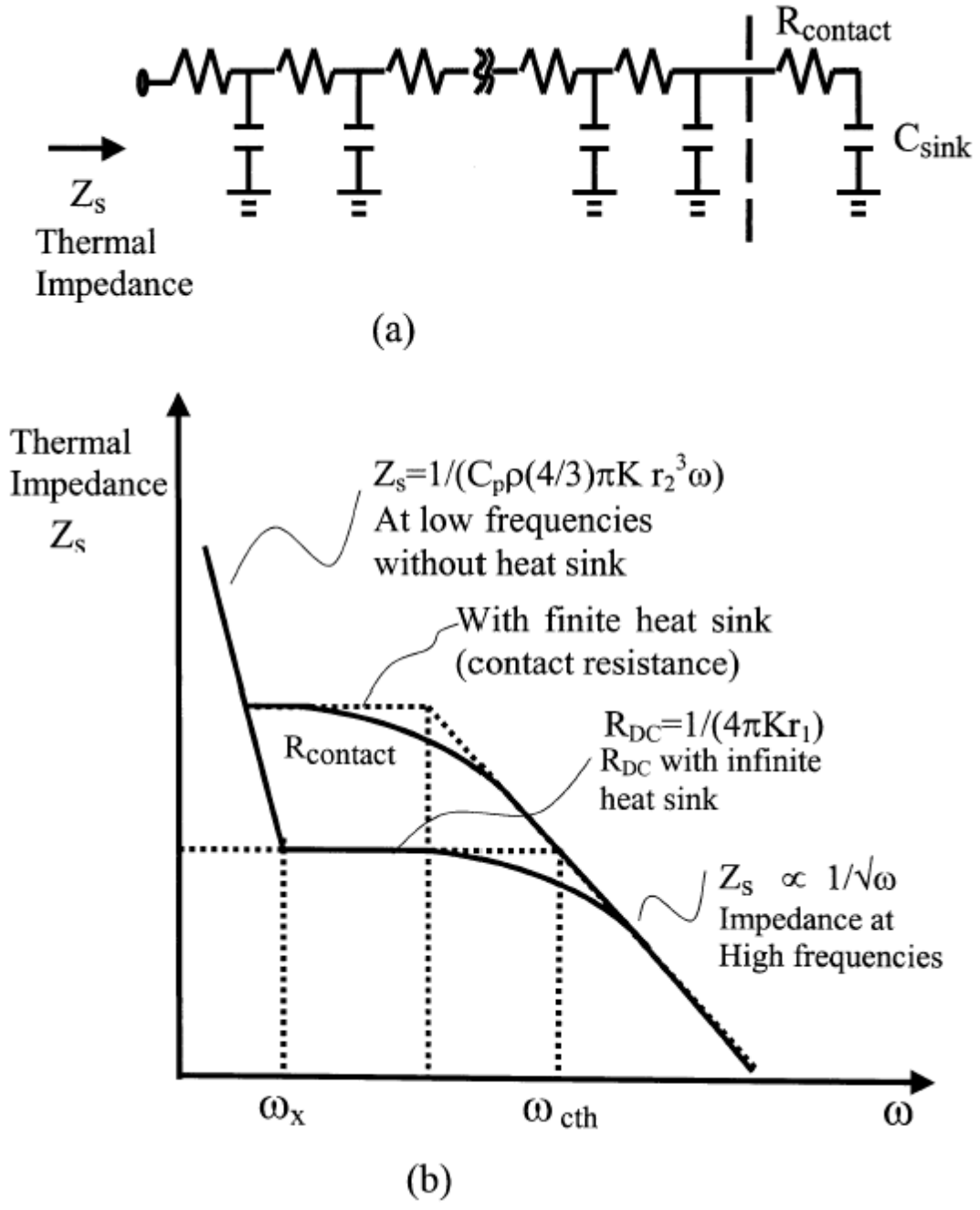


Figure 2.2 Steady state heat conduction due to power dissipation in the transmission line model

systems, and the noise at very low frequencies is not as important, we will just consider the approximation of short-circuited characteristics of the transmission line. As is the case with electrical current, which is made up of a large number of individual events, heat flux is associated with the transfer of energy to lattice vibrations in discrete elements. We will assume here that the heat energy is transferred to the lattice over very short time periods in the units of V_{DC} q where V_{DC} is the applied DC voltage. We are assuming here that the transit time of the electron through the electron device is small, as is usually the case. Using Carson's theorem, where the average number of individual events is, $\overline{N}$, then;

$$S_V(f) = 2\ \bar{N}\ \left|f(\omega)\right|^2 \tag{2.22}$$

if each individual event occurs in a short time then

$$S_v(f) = 2\bar{N}V_{DC}^2\ q^2 \tag{2.23}$$

But the heat flux is just the mean number of individual units of energy times the energy associated with each, $flux = \overline{N}qV_{DC}$. So the spectral intensity of the heat flux becomes,

$$S_v(f) = 2qV_{DC}flux = \overline{f_n^2} \tag{2.24}$$

This spectral intensity will cause a mean square temperature variation with spectral intensity at the surface of the sample given by

$$\overline{T_n^2} = \overline{f_n^2}\left|Z_S\right|^2 \tag{2.25}$$

again the solution is simple in the two limiting cases; at low frequencies then;

$$\begin{aligned}\overline{T_n^2} &= 2qV_{DC}\,flux\cdot R_{DC}^2 \\ &= 2qV_{DC}\cdot\frac{\Delta T}{R_{DC}}\cdot R_{DC}^2 \\ &= 2qV_{DC}\,\Delta T\,R_{DC}\end{aligned} \tag{2.26}$$

while at high frequencies;

$$\begin{aligned}\overline{T_n^2} &= 2qV_{DC}\,flux\cdot\frac{R_{DC}^2\cdot\omega_{cth}}{\omega} \\ &= 2qV_{DC}\cdot\frac{\Delta T}{R_{DC}}\cdot\frac{R_{DC}^2\cdot\omega_{cth}}{\omega} \\ &= 2qV_{DC}\,\Delta T\,R_{DC}\frac{\omega_{cth}}{\omega}\end{aligned} \tag{2.27}$$

If the heat source, in Fig. 2.1, is a transistor where the transistor base is by-passed by a large capacitor to keep the base at a fixed potential then the modulation of the base-emitter diode temperature will modulate the collector current since

$$I = B\exp\left(\frac{qV_{BE}}{kT}-\frac{E_G}{kT}\right) \tag{2.28}$$

$$dI/dT=(1/T)\ (q\Delta V/kT)\ I \tag{2.29}$$

where $\Delta V=\left(\frac{E_G}{q}-V_{BE}\right)$, V_{BE} is the base-emitter junction forward bias voltage and E_G the bandgap energy. The mean square fluctuation in temperature from Eqn. (2.27) will be determined mostly by power dissipation in the collector-base junction and the resulting temperature increase, ΔT, and then,

$$\begin{aligned}\overline{T_n^2} &= 2qV_{DC}\Delta T \cdot R_{DC}\frac{\omega_{cth}}{\omega} \\ &= 2qV_{DC}\Delta T \cdot \frac{\Delta T}{flux}\frac{\omega_{cth}}{\omega} \\ &= 2qV_{DC} \cdot \frac{(\Delta T)^2}{\overline{N}qV_{DC}}\frac{\omega_{cth}}{\omega} \\ &= (2q/I)(\Delta T)^2\left(\frac{\omega_{cth}}{\omega}\right)\end{aligned} \tag{2.30}$$

This results in a mean square fluctuation in the collector current or mean square noise current.

$$\begin{aligned}\overline{i_n^2} &= \frac{1}{T^2}\left(\frac{q\Delta V}{kT}\right)^2 I^2 \cdot \overline{T^2} \\ &= 2qI\left(\frac{\Delta V}{(kT/q)}\right)^2\left(\frac{\Delta T}{T}\right)^2\left(\frac{\omega_{cth}}{\omega}\right)\end{aligned} \tag{2.31}$$

where now,

$$\begin{aligned}\Delta T &= flux \cdot R_{DC} \\ &= \overline{N}qV_{DC} \cdot \frac{1}{4\pi kr_1} \\ &= V_{CE}I\frac{1}{4\pi Kr_1}\end{aligned} \tag{2.32}$$

is the temperature increase due mostly to power dissipation in the base-collector junction, and V_{CE} is the collector-emitter voltage, assuming an infinite heat sink.

2.2.2 Experimental Results

In this study, we used small silicon epitaxial planar common commercial discrete bipolar transistors, of type npn2222A. In order to generate large power dissipation which results in a high junction temperature, the devices were operated at high

collector currents and high collector-emitter voltages. Next, we determined a way to measure the temperature increase, ΔT, of the device due to the high power dissipation. It is well known the base-emitter voltage, V_{BE}, of bipolar transistor exhibits a negative temperature coefficient, TC. So if we can get the temperature coefficient, TC, then we can get the temperature increase, ΔT, from the measured value of V_{BE}. Since the power dissipation of a diode-connected bipolar transistor is small, the junction temperature will be approximately the ambient temperature. We first measured the V_{BE} of a diode-connected bipolar transistor, for the simplicity we just fix the V_{CE} at 1V with different ambient temperatures. The results are shown in Fig. 2.3. We get the temperature coefficient TC as being -1.4mV/K for I_C=10mA and -1.2mV/K for I_C=30mA respectively. The graphs of V_{BE} measured at different ambient temperatures with V_{CE}=15V are also shown in Fig. 2.3, first for I_C=10mA and then for I_C=30mA. From the difference in V_{BE} between V_{CE}=1V and V_{CE}=15V, we can calculate the temperature increase, ΔT. For example, ΔT is approximately 17 ^oC for I_C=10mA, V_{CE}=15V. If we assume an infinite heat sink and use Equation (2.32), we get r_1=4.6834x10^{-4}cm, which is a reasonable value for these bipolar transistors. However, the actual value of r_1 is probably larger than this value and the thermal impedance of the sample is small and the total thermal impedance limited by the contact impedance.

Finally, we determine from experiment whether 1/f noise has dependence on $(\Delta T/T)^2$ by holding the collector current and the collector-emitter voltage constant and measuring the collector current noise under different ambient temperatures such as in

air, in home-temperature water, in hot water, and in dry ice. Fig. 2.4 shows the measured collector current noise versus $(\Delta T/T)^2$ at f=1.0Hz first for I_C=10mA and then for I_C=30mA. From this figure, we can see the trend lines fit the experimental data very well. This serves to verify our theory and the dependence of noise power on temperature increase and power dissipation.

Fig. 2.5 shows the automated measurement results of the device noise spectral density at I_C=10mA and V_{CE} =15V. The low frequency measurements are done using the techniques described previously [46]. At higher frequencies a newer faster analog to digital converter board, ADC board, has been used for the measurements. These results are also shown in this figure, which indicates an agreement between the two measurement results and previous measurement results [46]. Eqn. (2.31) has been used to calculate the mean square collector noise current at frequencies less than, ω_{cth} , assuming that the factors limiting the temperature increase are the external thermal contact resistance.

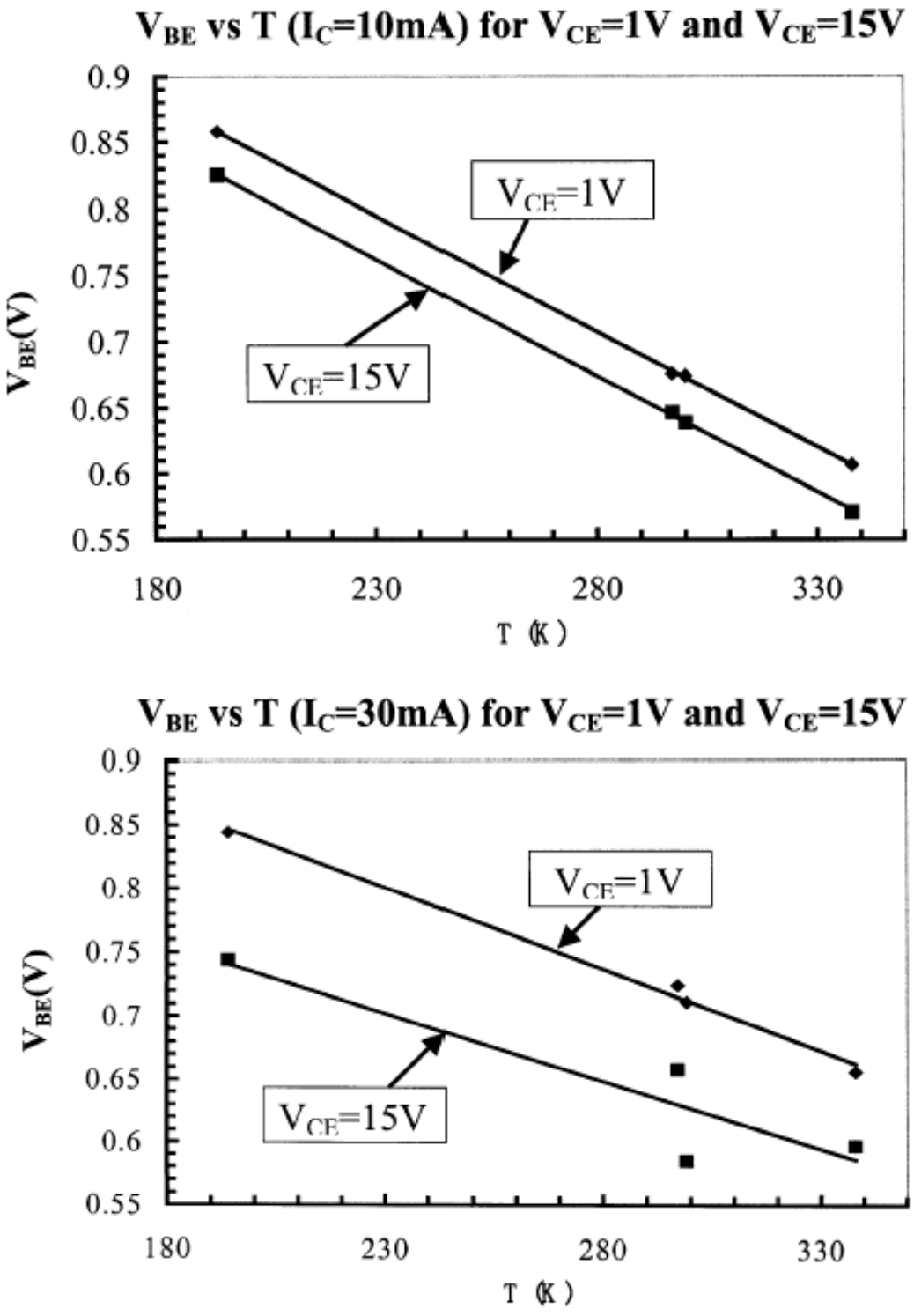


Figure 2.3 Measured base-emitter voltage V_{BE} at V_{CE} =1V and V_{CE} =15V with different ambient temperatures for I_C=10mA and I_C=30mA respectively

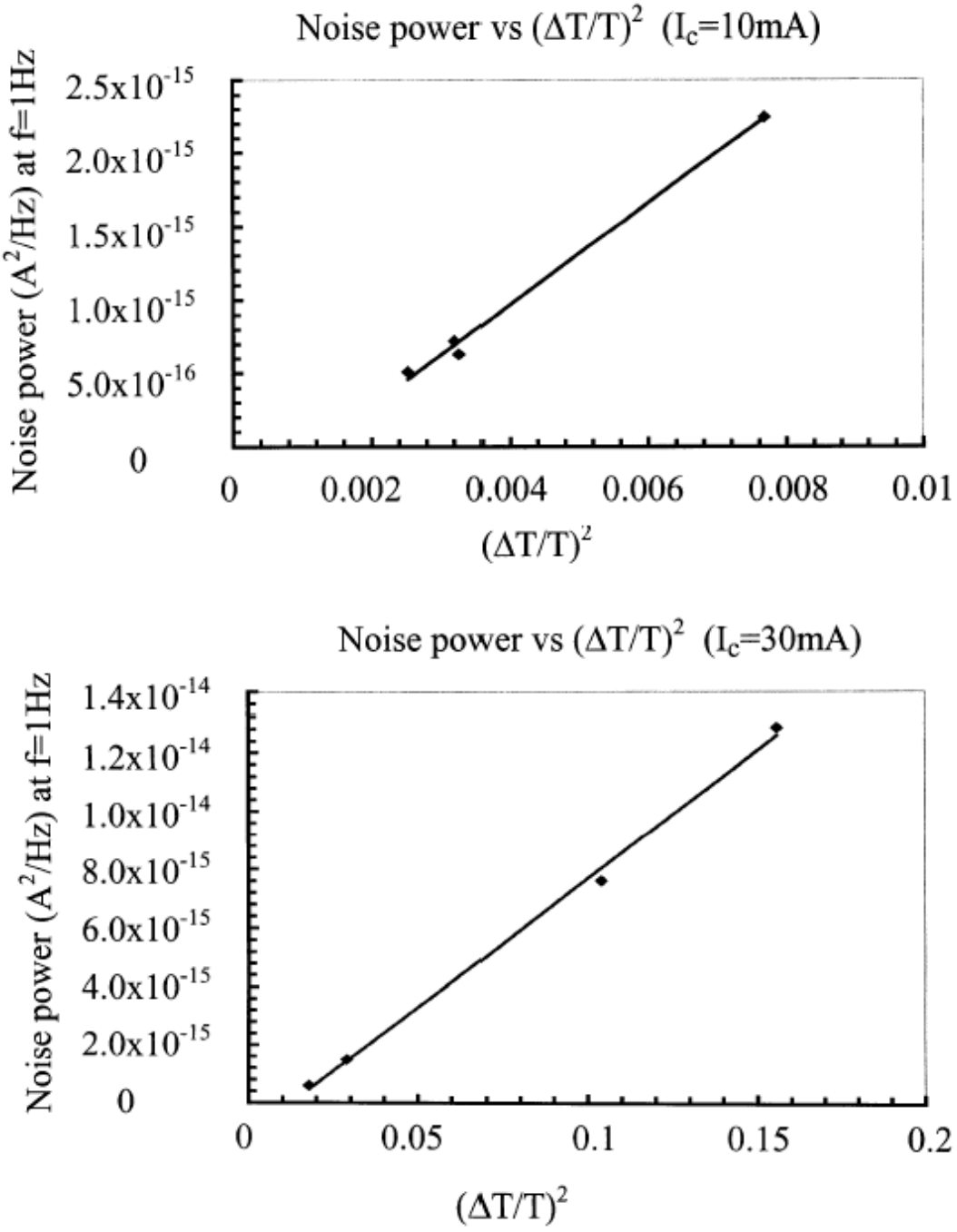


Figure 2.4 Measured current noise power at f=1Hz versus $(\Delta T/T)^2$ for V_{CE}=15V and I_C=10mA and 30mA respectively

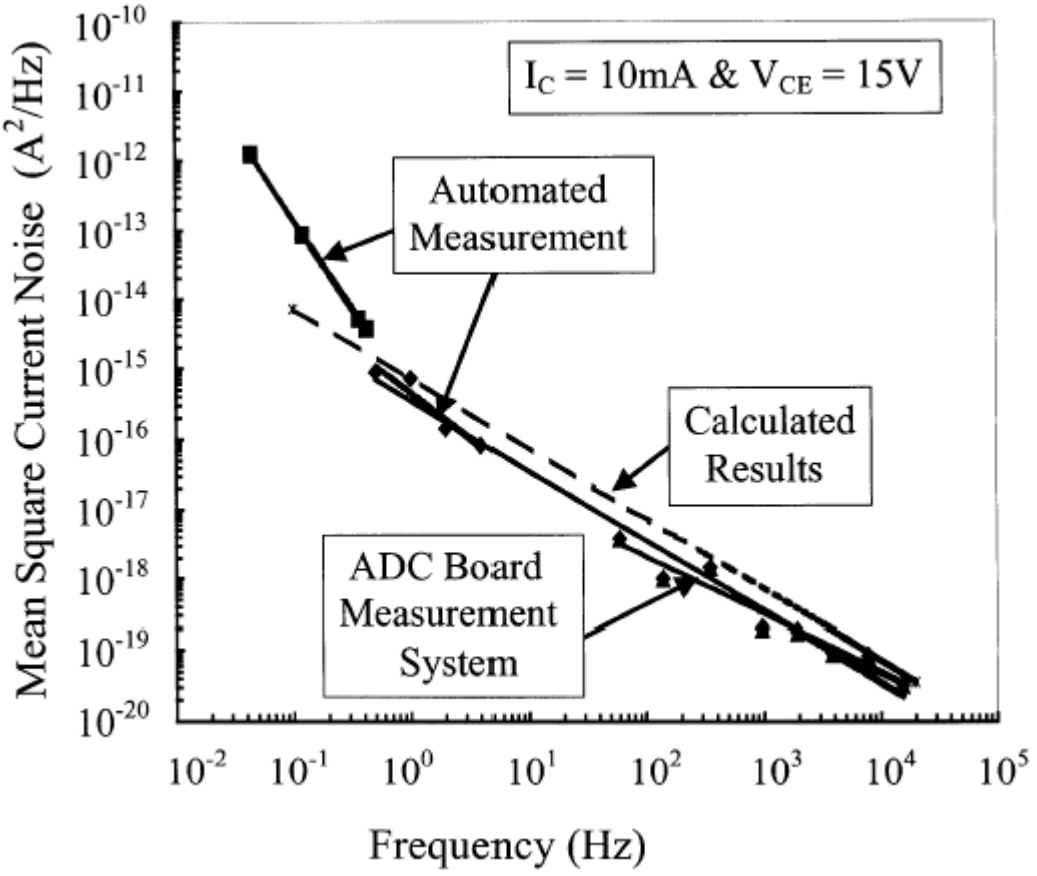


Figure 2.5 A comparison between mean square collector noise current measured on a bipolar transistor with high power dissipation (V_{CE}=15V, I_C=10mA) and that calculated using $(\Delta T/T)^2$.

3. MODELING OF RANDOM PHASE FLICKER NOISE AND WHITE NOISE

The flicker noise and white noise are modeled as

$$\overline{i_{nf}^{\,2}} = \frac{C}{f} \tag{3.1}$$

$$\overline{i_{nw}^{\,2}} = C_{white} \tag{3.2}$$

where C is the noise power for flicker noise at 1 Hz, C_{white} is the white noise power.

We can use Eqn.(3.1) and Eqn.(3.2) to describe different power spectral density values of flicker or white noise in a range of frequencies with a step frequency, fs. Then the amplitudes of current components, Iamp (A), associated with the flicker noise or white noise can be calculated by the following equations:

$$I_{flick} = (\overline{i_{nf}^{\,2}})^{1/2} \quad or \quad I_{white} = (\overline{i_{nw}^{\,2}})^{1/2} \tag{3.3}$$

$$I_{amp} = I_{flick} \bullet (f_s)^{1/2} \quad or \quad I_{amp} = I_{white} \bullet (f_s)^{1/2} \tag{3.4}$$

An ideal sinusoidal current signal can then be expressed as

$$Ind(i) = Iamp(i) \bullet \sin[2\pi f(i)t + \Phi(i)] \tag{3.5}$$

where Φ(i) is the random phase, f is frequency, i is the index of the frequency, which changes from 1 to the end of the frequency range used in the simulation.

The “rand” function in MATLAB is used to create a pseudo-random Φ(i), by using randomly created internal data in the computer. Then all the individual current

components, Ind(i), are summed together to get the random-phase flicker noise, I_{flick}', or random-phase white noise, I_{white}', in the defined frequency range.

$$I_{flick}' = \Sigma Ind(i) \quad or \quad I_{white}' = \Sigma Ind(i) \qquad \text{i=range of the frequencies} \qquad (3.6)$$

4. PHASE NOISE IN A 2-G HZ BJT LC OSCILLATOR

4.1 Characterization of Phase Noise

Frequency stability is an important factor for an oscillator maintaining the same value of frequency over a given time. The term phase noise is commonly used for describing short noise random frequency fluctuations of a signal. The definition of phase noise is shown as follows. The output of an ideal sinusoidal oscillator may be expressed as:

$$V(t) = V(0) \bullet \sin(2\pi ft) \tag{4.1}$$

where V(0) is the nominal amplitude of the signal, and f is the nominal frequency of oscillation. In a practical oscillator, the output is more generally given by

$$V(t) = V(0) \bullet [1 + A(t)] \bullet \sin[2\pi ft + q(t)] \tag{4.2}$$

where A(t) and q(t) are the amplitude and phase fluctuation of the signal respectively. Usually white, or frequency independent, and flicker (1/f) noise are the generating sources of phase noise. Since all practical oscillators employ some kind of amplitude-limiting mechanism, most oscillators operate in saturation region with the amplitude noise component 20 dB lower than the phase noise component, so usually it is phase noise dominated, we will assume that A(t)<<1 [49] and only study phase noise.

Phase noise is usually expressed as Single Side Band (SSB) power, which is the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset f

(frequency) Hertz away from the carrier, to the total signal power. If given logarithmically, phase noise is expressed in dB relative to the carrier per Hz bandwidth as dBc/Hz.

$$S_c(f) = 10\log\frac{P_{ssb}}{P_s} \tag{4.3}$$

where P_s is the carrier power and P_{ssb} is the sideband power in one Hz bandwidth at an offset frequency of f from the center (Fig. 4.1) [53].

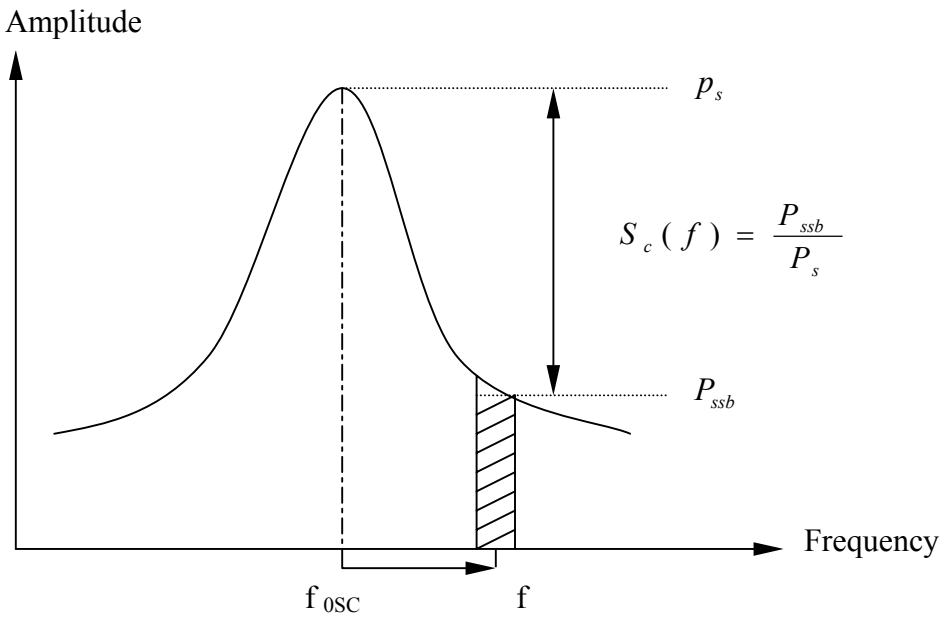


Figure 4.1 Single sideband phase noise to carrier ratio [53].

4.2 Simulation of Phase Noise in LC BJT Oscillator

Instead of using a conventional SPICE model $\overline{i_{nf}^2} = KF\frac{I_B^{AF}}{f}$ for describing the flicker noise, we recently have been able to show that the flicker noise in a bipolar

transistor with a low impedance between the base and emitter can be expressed in the following form [46],

$$\overline{i_{nf}^{\,2}} = 2qI_C(\frac{f_c}{f}) \tag{4.4}$$

where I_C is the collector current. The corner frequency, fc, is defined as the frequency at which the flicker noise $\overline{i_{nf}^{\,2}}$ is equal to the collector current shot noise or white noise $\overline{i_{nw}^{\,2}} = 2qI_C$ in a bipolar transistor. Different corner frequencies will cause different amplitudes of flicker noise. Here we use fc=36kHz such as we have more recently measured [46] for a typical small bipolar device.

The circuit used in our simulation is based on a low phase noise LC BJT voltage controlled oscillator introduced by Zannoth etc [56], carrier frequency is 2-GHz. The circuit diagram is shown in Fig.4.2. The design is based on a LC-resonator with vertical-coupled inductors, the equivalent circuit of the coupled inductor is shown in Fig.4.3, which is used as a subcircuit in the HSPICE simulation.

In our simulation, the random-phase flicker noise I_{flick}', or random-phase white noise I_{white}', obtained from MATLAB, is injected into the signal path as a piece wise linear waveform at the collector of q4. After that, a transient analysis is performed for the oscillator with the flicker or white noise source over a relatively large number of oscillation periods and the output is written as a series of points equally spaced in time. The internal FFT function in HSPICE is used to compute the FFT of HSPICE simulation output in the time domain. To get the best results, a Blackman-Harris window with 16384 points, NP=16384, is used in the FFT analysis. In the simulation, FFT analysis is starting from 19.56 ns to exclude the starting period that

is not oscillating. Simulation shows this period distorts the FFT output very much, thus has to be excluded. [Detailed procedure of phase noise simulation in Oscillators is in Appendix C]

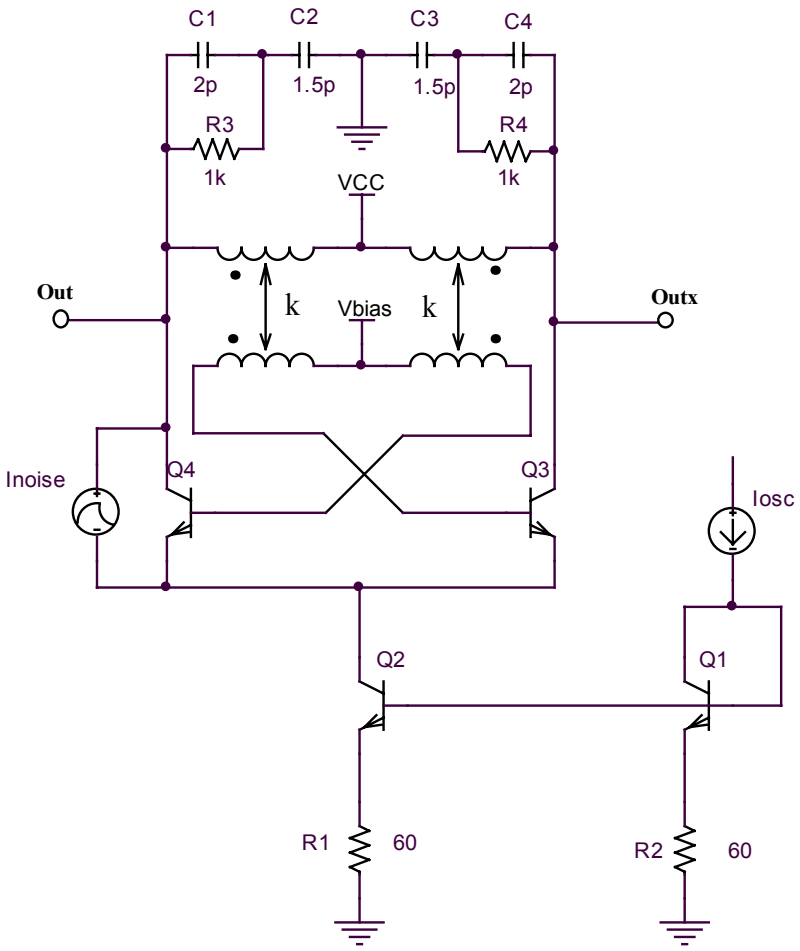


Figure 4.2 BJT LC VCO for simulation [56]

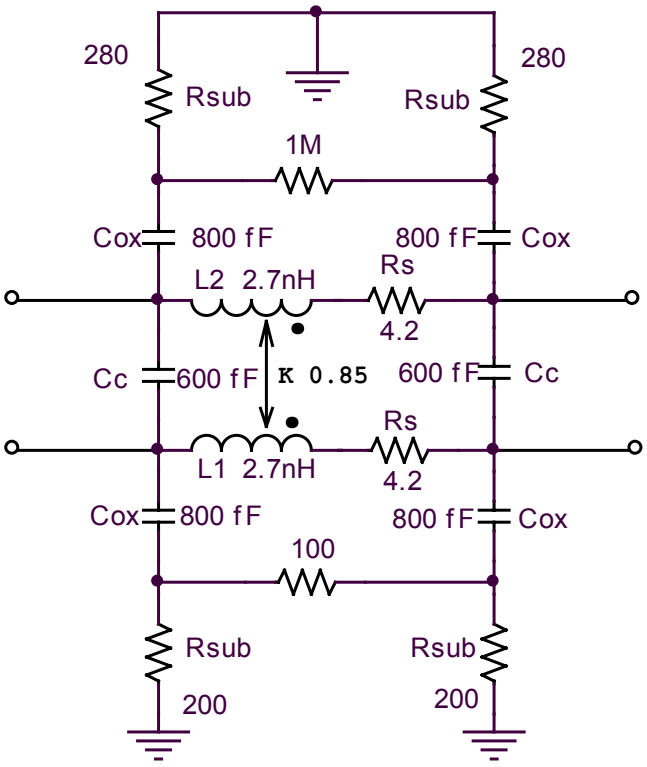


Figure 4.3 Equivalent circuit of the inductor [56]

4.3 Simulation Results and Discussion

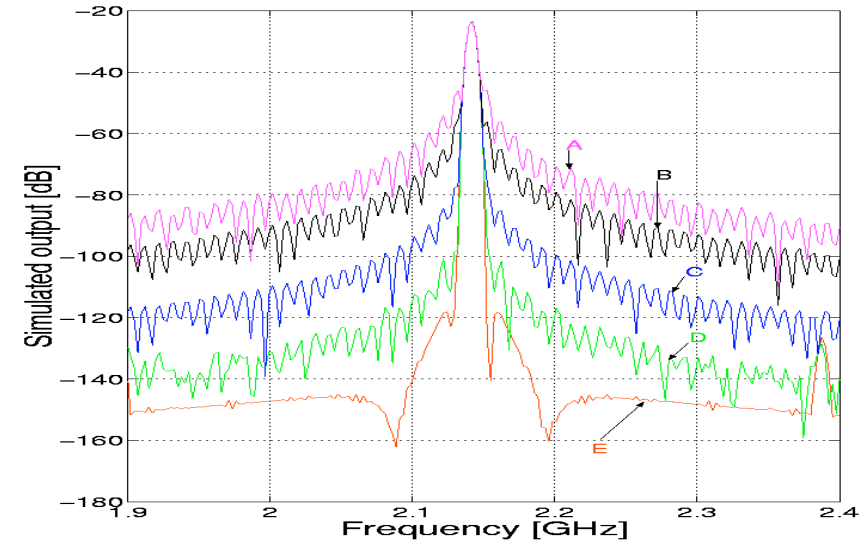
Five different conditions of random-phase flicker or white noise, including one without added noise, are applied to the LC oscillator. Fig.4.4 shows the simulated output power spectral corresponding to these five different conditions, Fig.4.4 (a) for injected flicker noise, while Fig.4.4 (b) for injected white noise, these correspond to five different fc values or white noise sources. It can be seen that when there is no random-phase noise introduced into the oscillator, the sideband harmonics with peaks exist, while as the random-phase noise is injected and noise increases, these

harmonics are gradually buried in the additional noise. The sideband power increases with the amplitude of the injected noise.

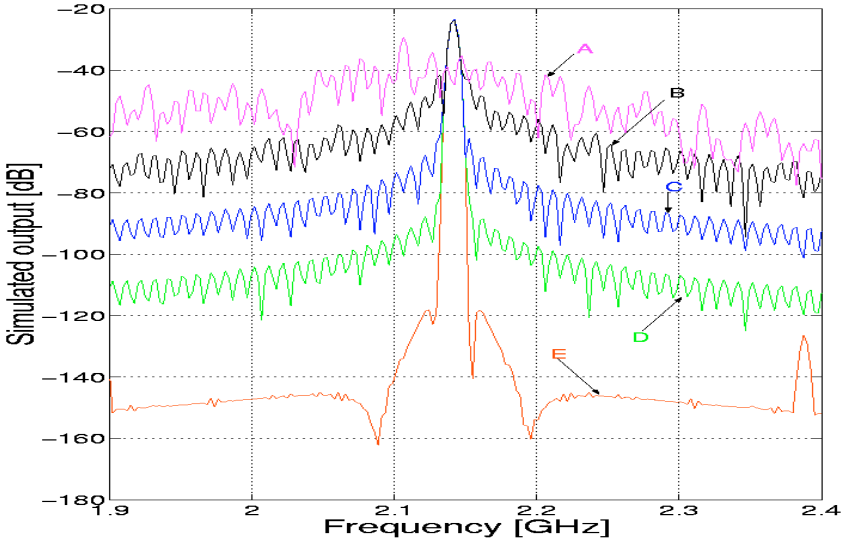
Fig.4.5 (a) shows the phase noise sideband power spectra density for flicker noise with four different fc values, while Fig.4.5 (b) for white noise with four different noise sources. According to Leeson's theory, phase noise resulting from flicker noise has a $1/f^3$ dependence, while from white noise has a $1/f^2$ dependence on offset frequency. These $1/f^3$ and $1/f^2$ dependencies are clearly shown in Fig.4.5.

Fig.4.6 shows the phase noise sideband power below carrier per Hz (dBc/Hz) versus injected flicker noise or white noise at 4.7 MHz offset from carrier frequency. It is clearly from Fig.4.6 that the magnitude of the sideband directly scales with the magnitude of injected noise. By projecting back to the actual case of the simulated circuit, which is fc=36.232 kHz and white noise $2qI_C=1.1\times10^{-21}$ A^2/Hz, we obtain the phase noise at 4.7 MHz offset resulting from flicker noise is -150.7 dBC/Hz, from white noise is –132 dBc/Hz. At this point it is white noise dominated. The simulation results are in good agreement with the experimental value of –136 dBc/Hz at this offset frequency reported in the literature by Zannoth and Kolb [56].

Fig.4.7 shows the projected results with comparison to observed one, it is shown they match each other and our simulation is able to predict phase noise correctly.



(a)



(b)

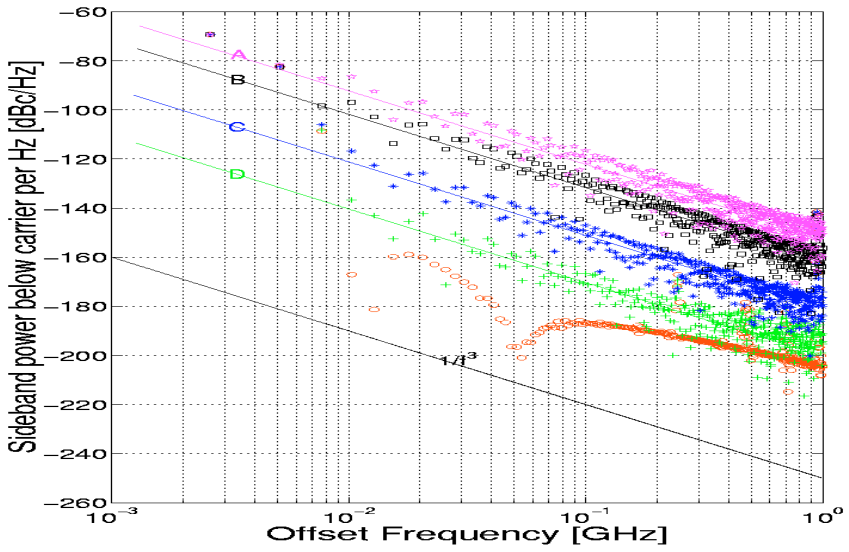
Figure 4.4 Simulated output power spectral of LC oscillator

(a) flicker noise with different fc values

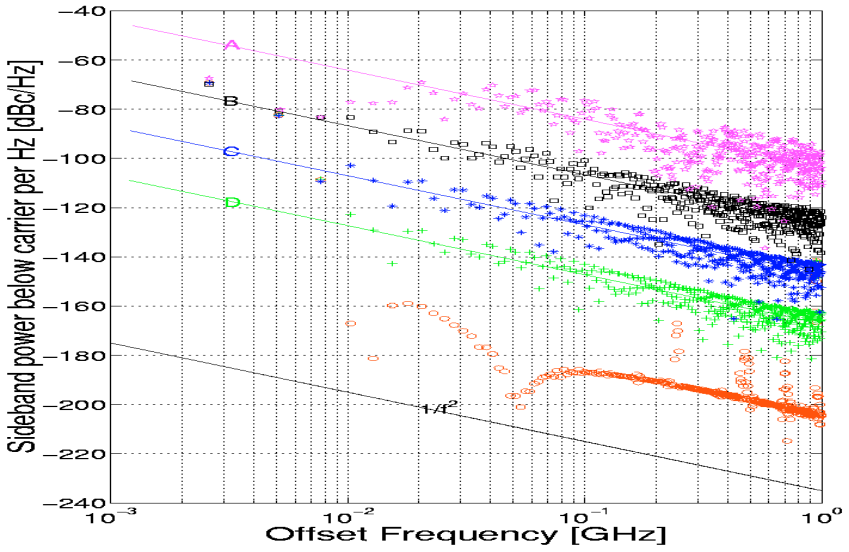
A. fc=400 GHz B. fc=40 GHz
C. fc=400 MHz D. fc=4 MHz
E. No flicker noise injected

(b) white noise with different noise sources

A. white noise=1.1×10^{-14} A^2/Hz B. white noise=1.1×10^{-16} A^2/Hz
C white noise=1.1×10^{-18} A^2/Hz D. white noise=1.1×10^{-20} A^2/Hz
E. No white noise injected



(a)



(b)

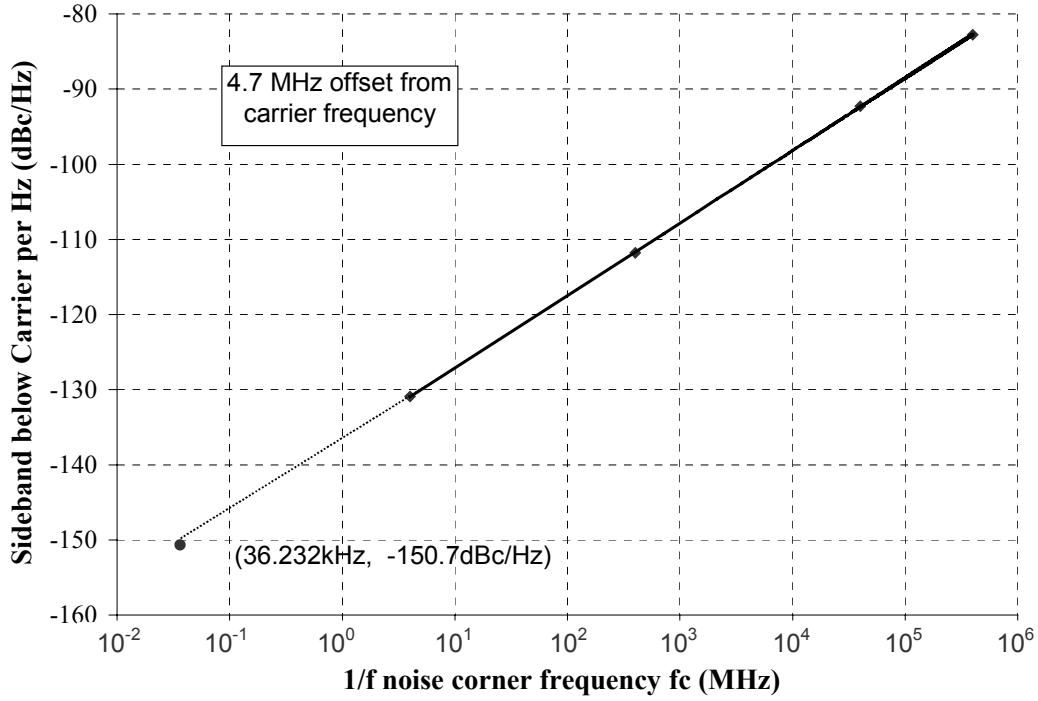
Figure 4.5 Simulated sideband power below carrier per Hz versus offset from the carrier (fosc=2 GHz)

(a) flicker noise with different fc values

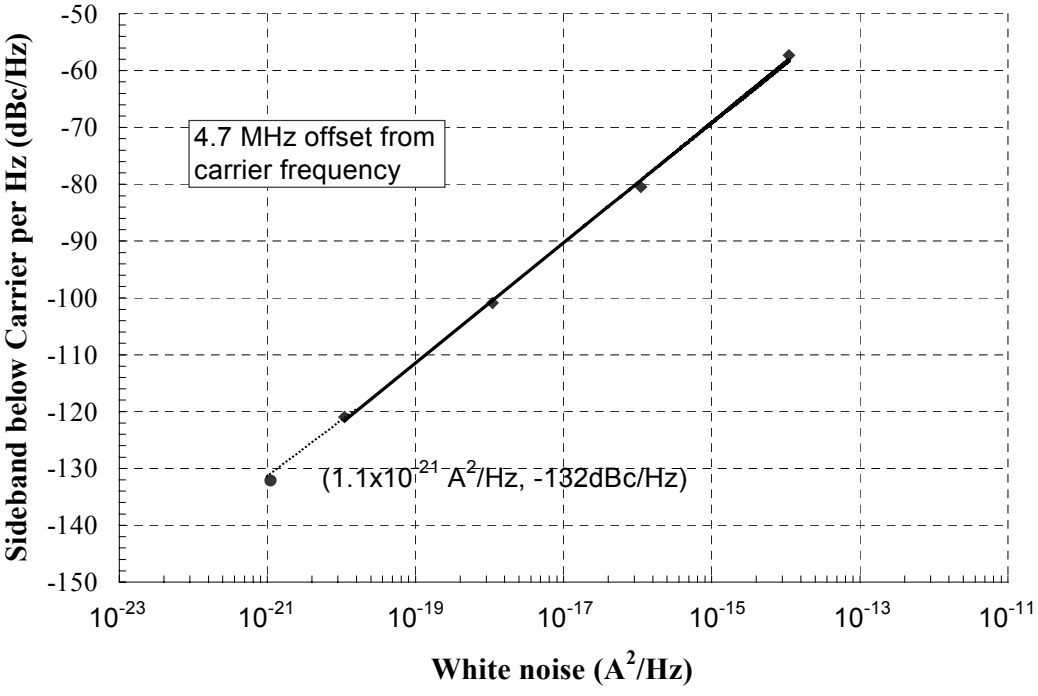
A. fc=400 GHz B. fc=40 GHz
C. fc=400 MHz D. fc=4 MHz

(b) white noise with different noise sources

A. white noise=1.1×10^{-14} A^2/Hz B. white noise=1.1×10^{-16} A^2/Hz
C white noise=1.1×10^{-18} A^2/Hz D. white noise=1.1×10^{-20} A^2/Hz



(a)



(b)

Figure 4.6 Simulated sideband power below carrier per Hz versus injected noise at 4.7 MHz offset from carrier frequency

(a) versus fc values (injected flicker noise)
(b) versus white noise sources(injected white noise)

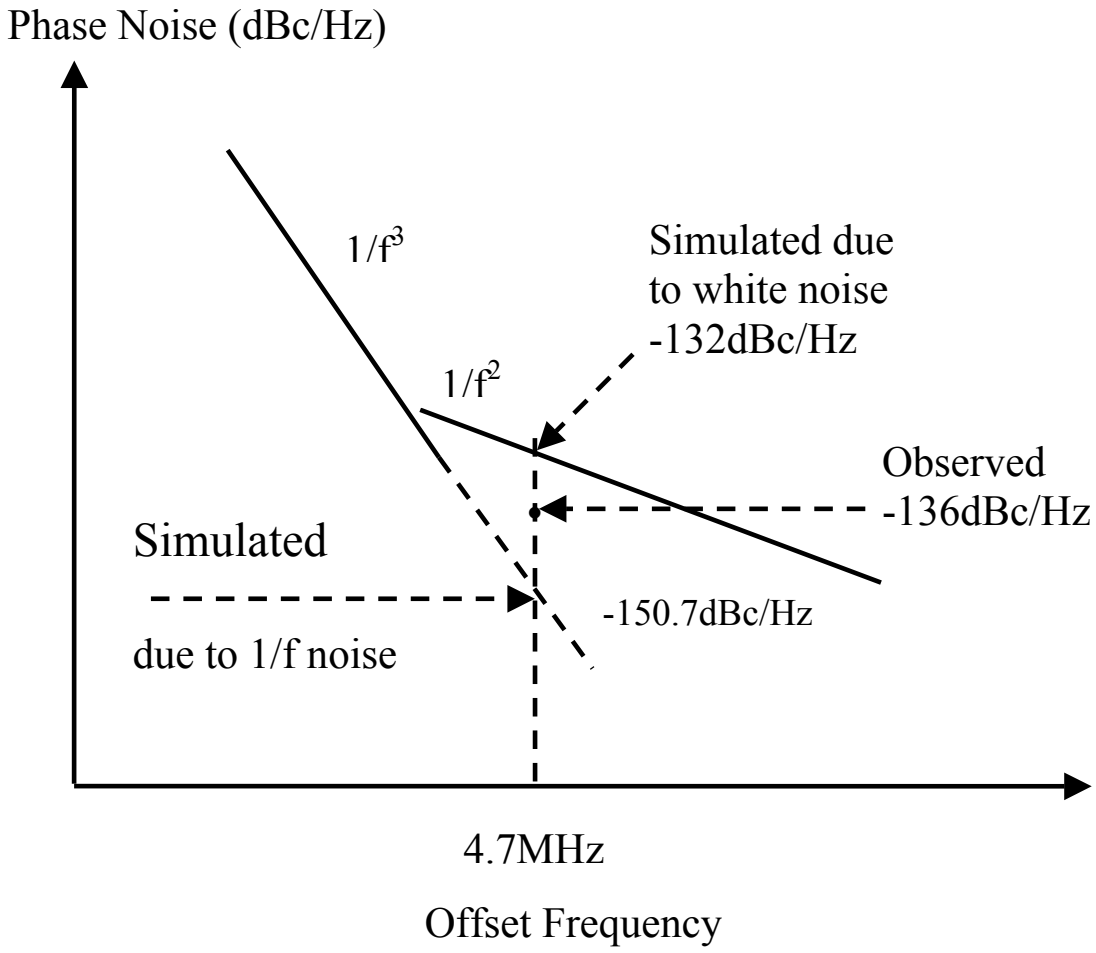


Figure 4.7 Projected results with comparison to observed one

5. TIMING JITTER IN SINGLE ENDED CMOS RING OSCILLATORS

5.1 Definitions of Timing Jitter

In an ideal oscillator, the output is a perfect timing reference with fixed period. However, in practice, due to the existence of noise, the period itself is a function of time, the expected timing edges never occur exactly where desired, as illustrated in Fig.5.1. The deviation from ideal reference is an indication of jitter, noted as $\Delta T_n = T_n - \overline{T}$, where n refers to n th period, T_n is the n th period and $\overline{T}$ is the ideal reference. Jitter is defined as "short-term variations of the significant instants of a digital signal from their ideal positions in time" [79], noted as ΔT_n (n th period).

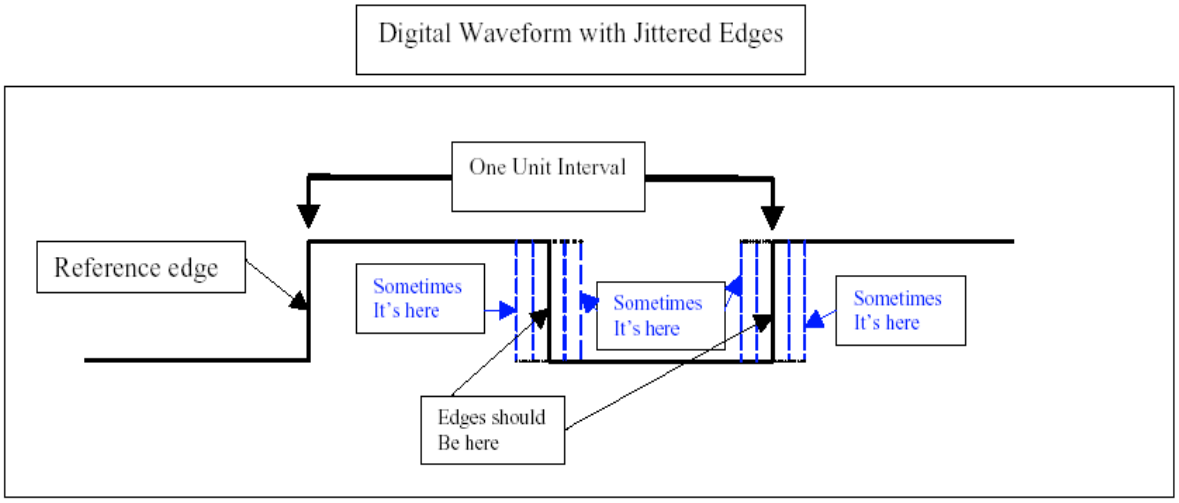


Figure 5.1 Illustration of timing jitter [79]

There have been three kinds of timing jitter as described in the literature [69]. The first one is called absolute jitter or long term jitter

$$\Delta T_{abs}(N) = \sum_{n=1}^{N} \Delta T_n \tag{5.1}$$

which is the total error with respect to an ideal oscillator[Fig. 5.2 (a)].

The second type of jitter is cycle jitter, defined as the rms value of the timing error ΔT_n.

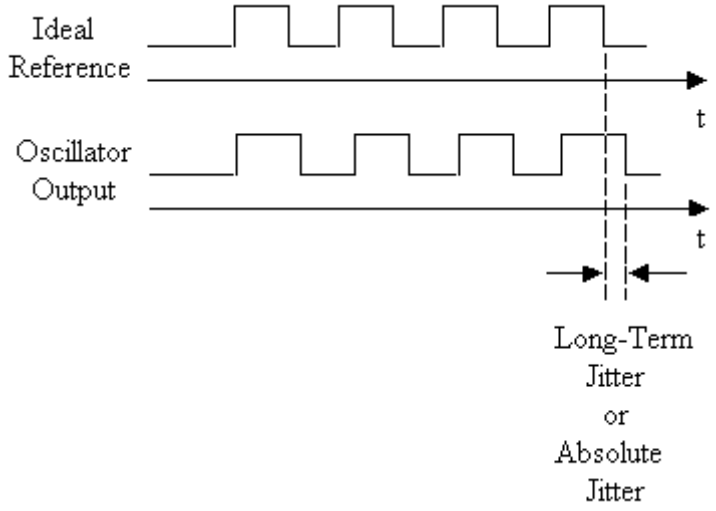
$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{5.2}$$

The third type of jitter is cycle to cycle jitter [Fig. 5.2 (b)], defined as

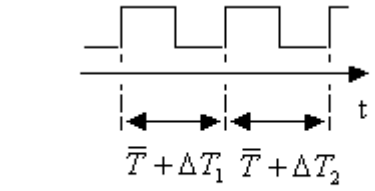
$$\Delta T_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_{n+1} - T_n)^2} \tag{5.3}$$

representing the rms difference between two consecutive periods.

For the above three different definitions, absolute jitter is more frequently used in describing phase-locked loops. While for a free running oscillator, the last two are more meaningful and often used.



(a)



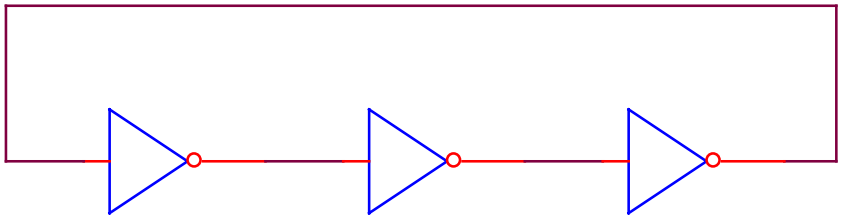
$\Delta T_2 - \Delta T_1 = Cycle \;\; to \;\; Cycle \;\; Jitter$

(b)

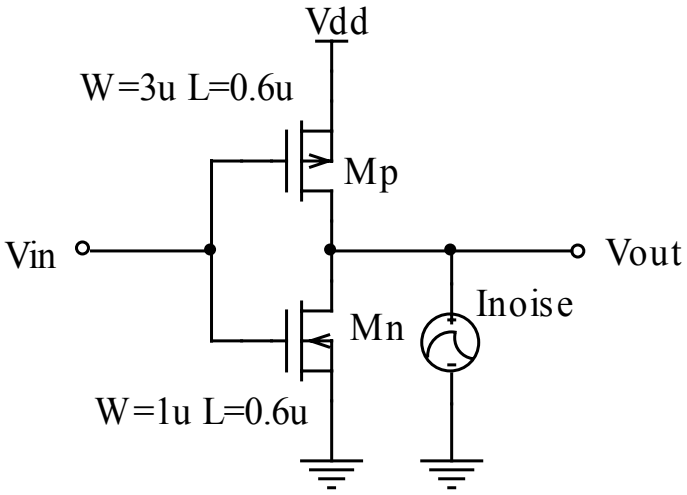
Figure 5.2 Illustration of (a) long term jitter and (b) cycle to cycle jitter [69]

5.2 Stationary Approach in Single Ended CMOS Ring Oscillators

The circuit to be simulated is shown in Fig.5.3, it is a single-ended three stage ring oscillator, circuit parameters are shown in the diagram and V_{dd}=5 V. The simulations were performed in PSPICE using BSIM 3.3 transistor model.



(a)

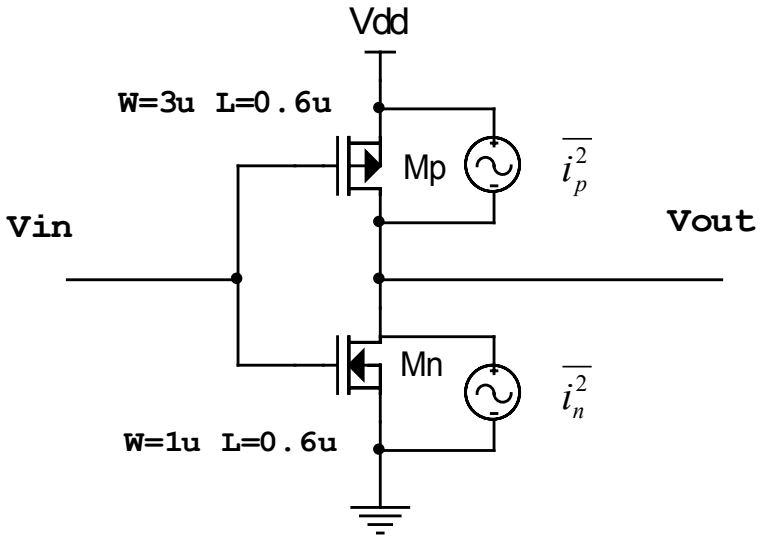


(b)

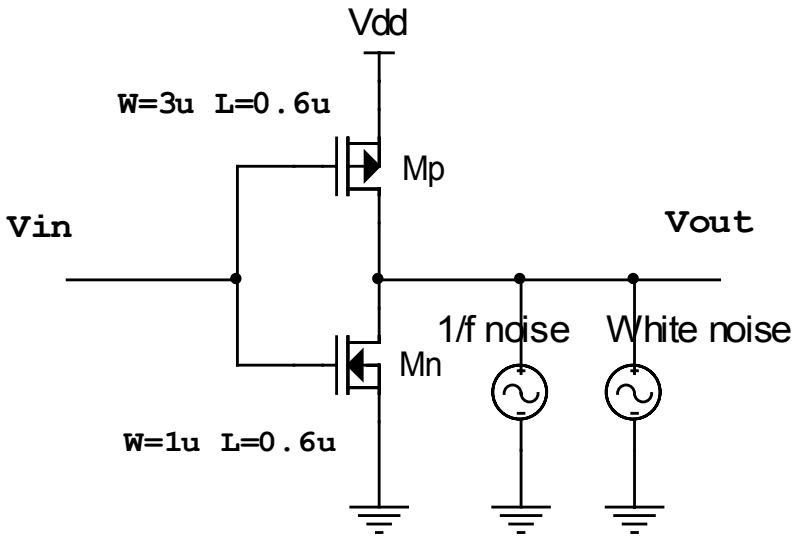
Figure 5.3 Single ended ring oscillator (a) block diagram
(b) implementation of one stage

The primary concern in this section is to study the impact of device noise on timing jitter. The schematic for the inverter cell is repeated in Fig. 5.4 (a) with noise source added, these are the intrinsic output referred noise sources for each transistor. In our simulations, we use a common stationary approach to estimate the effects of all the noise sources [51][71]. An equivalent output referred noise source is used to represent the effects of all internal noise sources in the circuit, as shown in Fig.5.4 (b). The two noise sources at output means we will inject and study 1/f noise and

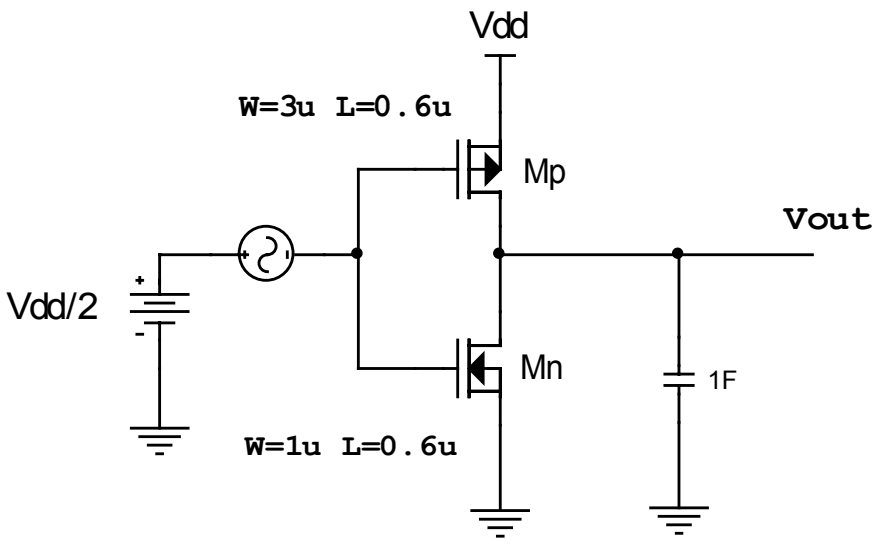
white noise separately. This equivalent noise power is calculated when the stage is half way through a transition. A linear circuit simulation is performed to get this noise power, as shown in Fig. 5.4 (c).



(a)



(b)



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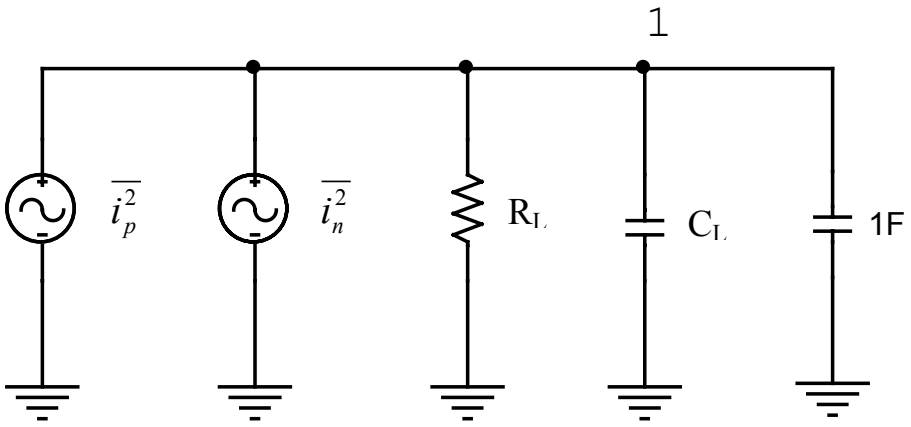


(d)

Figure 5.4 Illustration of Stationary Approach in Single Ended CMOS Ring Oscillators

(a) Inverter cell with noise sources

(b) Equivalent output referred noise source

(c) Circuit used to get the device noise power

(d) Equivalent circuit for AC noise analysis

The small-signal equivalent circuit of the inverter cell for AC noise analysis, in this case, is shown in Fig. 5.4(d), where $\overline{i_n^2}$ and $\overline{i_p^2}$ represent the output referred noise sources due to NMOS and PMOS respectively, R_L and C_L represent the total resistance and capacitance at the output node. The introduction of the additional 1F capacitor is to find the total output referred noise. Since the impedance of 1F capacitor is much lower than that of R_L and C_L, all the noise current will flow through this way. If we have measured the noise voltage at node 1, then divided by impedance of 1F capacitor, we could obtain the total equivalent output referred noise current.

5.3 Simulation of timing jitter in single ended CMOS ring oscillators

In our simulation, the random-phase flicker noise I_{flick}', or random-phase white noise I_{white}', obtained from MATLAB, is injected into the signal path as a piece wise linear waveform at the output of each stage. A transient analysis is performed for the oscillator with the flicker or white noise source over a relatively large number of oscillation periods and the output is written as a series of points equally spaced in time. Then at the output of circuit, the periods of consecutive clock samples were measured with PSPICE and transferred to MATLAB to calculate the timing jitter. The steps used to calculate timing jitter are as follows; interpolation of the voltage waveform to find the zero crossings, calculation of the periods T_n and ΔT_n with respect to ideal reference $\overline{T}$, and calculation of absolute jitter, cycle jitter and cycle to cycle jitter. [Detailed procedure of timing jitter simulation in Oscillators is in Appendix D]

As indicated above, we need to know the ideal reference $\overline{T}$ to find the timing jitter, thus we have to simulate the noise free case first to get $\overline{T}$. Ideally, this should be a periodically time-variant signal that is a perfect timing reference. However, due to

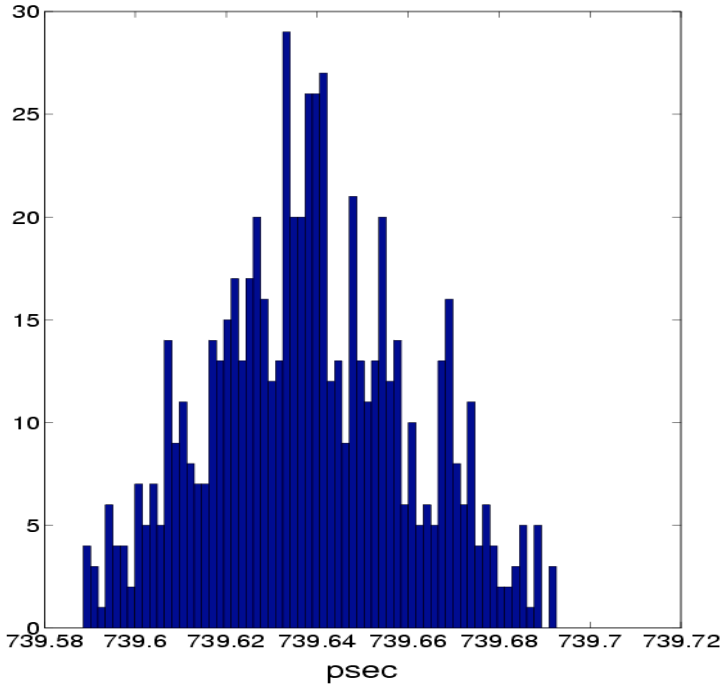


Figure 5.5 Histogram of output clock for noise free case

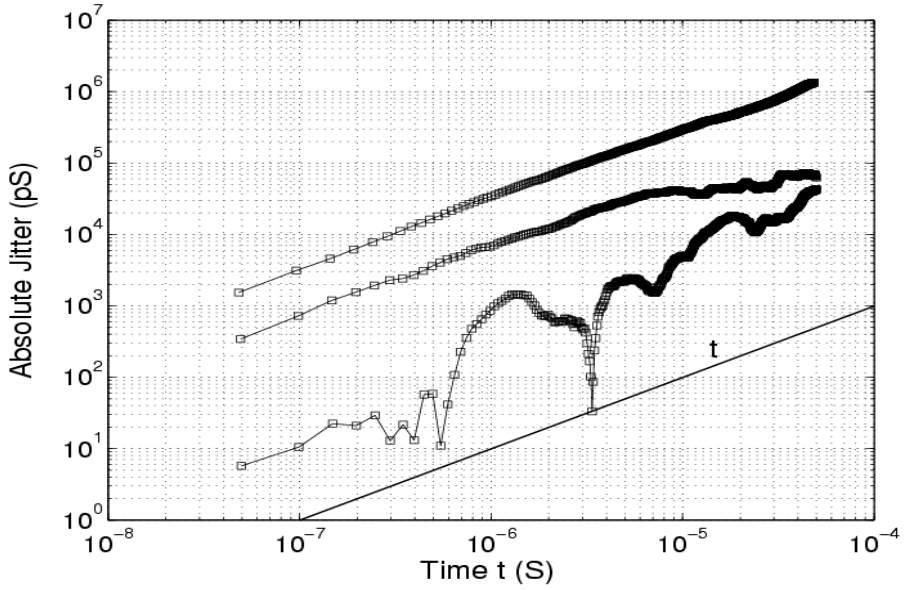
internal computational errors, we get a resulting clock period as shown in Fig.5.5. Even in noise free case, we have distribution of periods, though it is small. It appears as if some kind of noise source exists, so in our simulations we will model the computational errors as a special noise source. This kind of computational error also exists in the noise injected case, that is, in addition to the timing jitter from actual noise, there is another kind of "jitter" due to computational errors. We have made some simple compensation, not described here, to try to reduce these kind of errors.

5.4 Simulation results and discussion

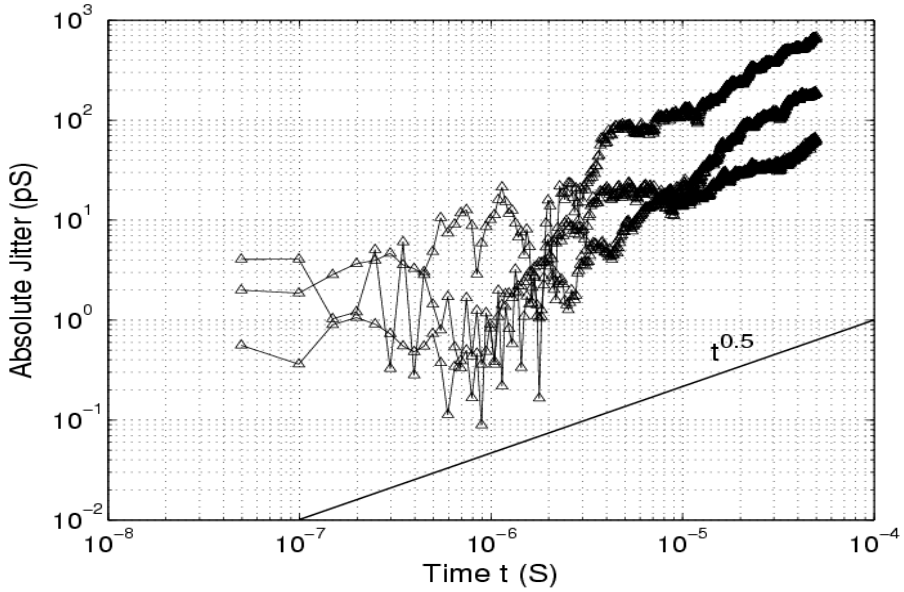
Simulation results are shown in Fig. 5.6 to Fig. 5.9. Fig. 5.6 shows the absolute jitter versus time, Fig. 5.7 and Fig. 5.8 show cycle jitter and cycle to cycle jitter versus time. The top part shows jitter due to flicker noise while lower part shows jitter due to white noise, and in each case three different conditions of random-phase flicker or white noise are applied to the ring oscillator. From Fig. 5.6 we can see the variation of absolute jitter due to flicker noise has a dependence on the time, t, while for white noise, it has a, $t^{0.5}$, dependence. These are consistent with accepted theory in the literature [69-73]. As shown in Fig. 5.6, with an increase of time, the variation of absolute jitter due to white noise gradually loses a, $t^{0.5}$, dependence due to computational errors. This is also shown in Fig. 5.7 and Fig. 5.8, for cycle jitter and cycle to cycle jitter due to white noise, they are supposed to be constant while in the graph, they start to increase after some time.

Another interesting phenomena is that an increase of injected noise will suppress the computational errors, as shown in Fig. 5.7 and Fig. 5.8. For larger injected noise, cycle jitter and cycle to cycle jitter will remain constant for a longer time. Fig. 5.9 shows the cycle to cycle jitter as a function of injected flicker noise or white noise, data was taken from the range where cycle to cycle jitter is constant. From Fig. 5.9 we can see the magnitude of cycle to cycle jitter scales with the magnitude of injected noise. By projecting back to a realistic case for the simulated circuit, which is $C = 2.8464 \times 10^{-13} \quad A^2 / Hz$ for flicker noise and $C_{white} = 5.3438 \times 10^{-24} \quad A^2 / Hz$

for white noise, we obtain a cycle to cycle jitter 0.19 ps for flicker noise and 0.0191 ps for white noise.

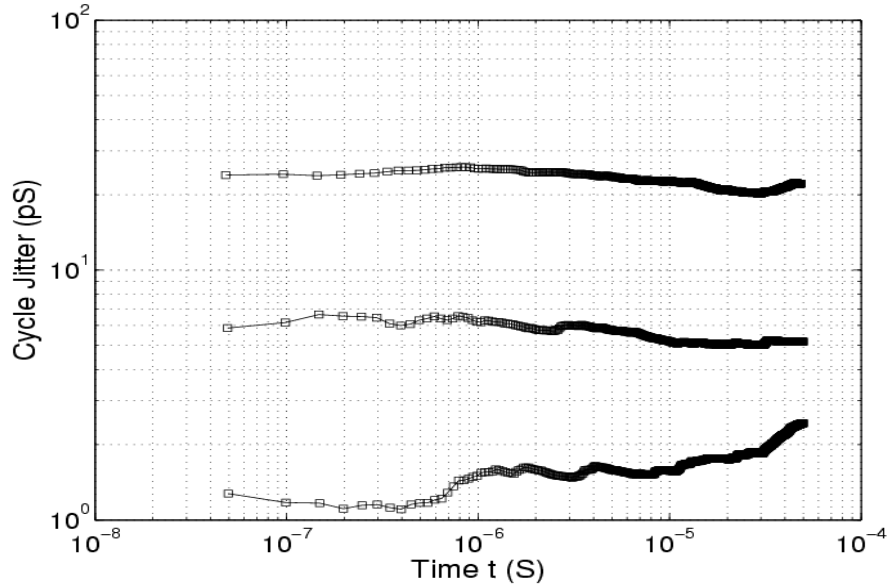


(a)

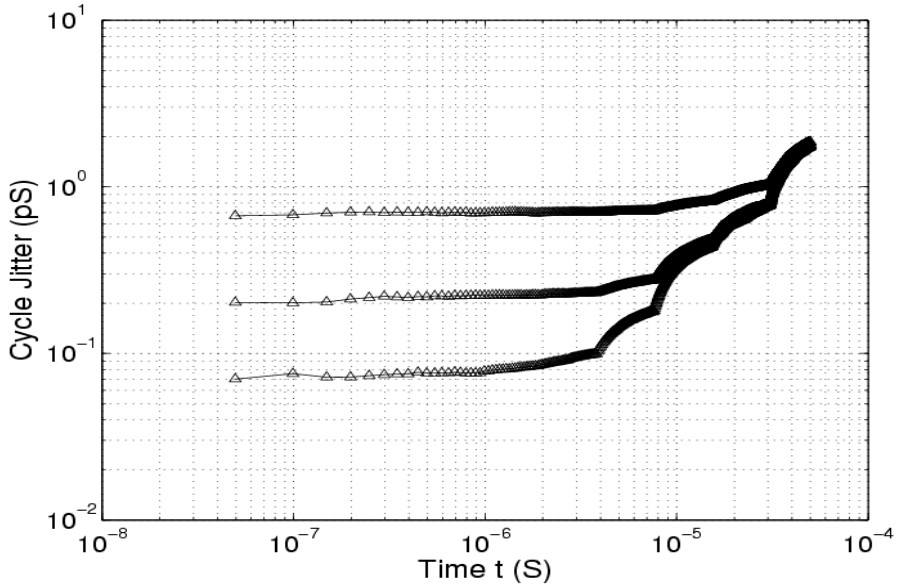


(b)

Figure 5.6 Absolute jitter as a function of time
(a) flicker noise
(b) white noise

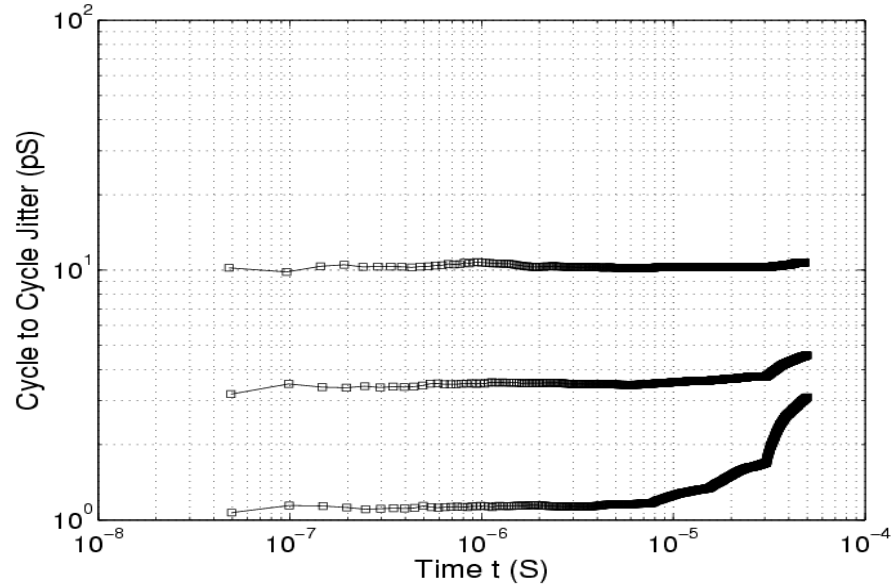


(a)

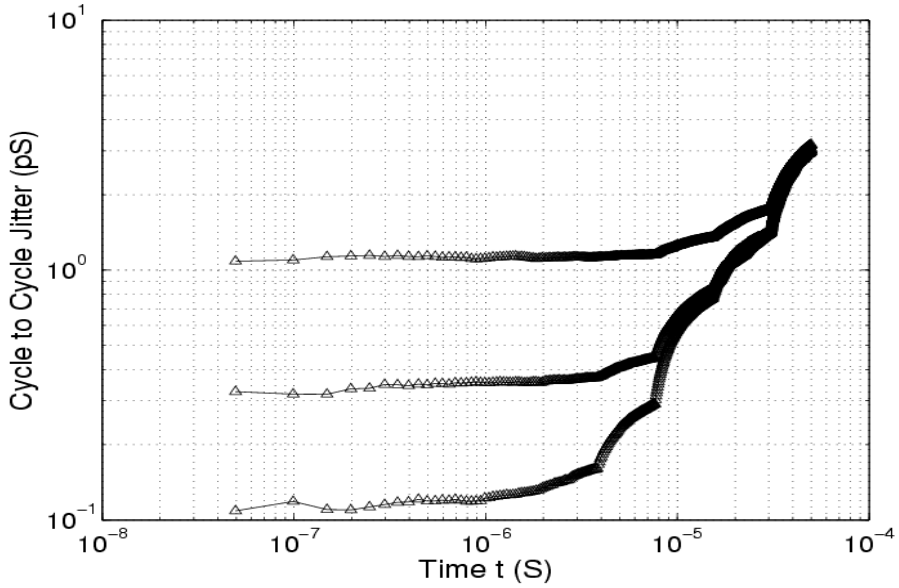


(b)

Figure 5.7 Cycle jitter as a function of time
(a) flicker noise
(b) white noise

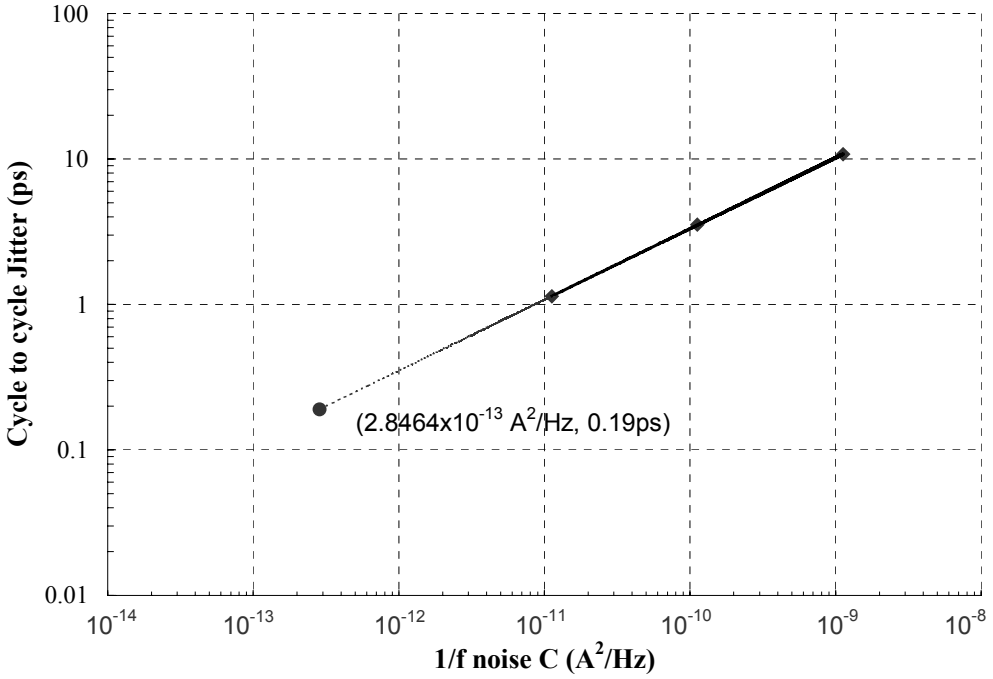


(a)

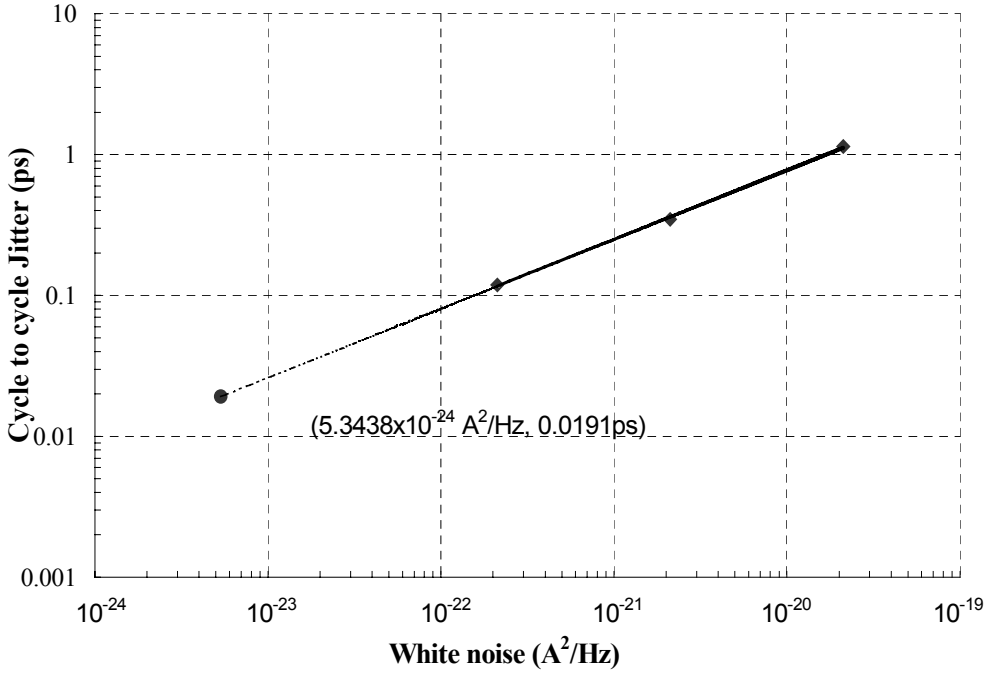


(b)

Figure 5.8 Cycle to cycle jitter as a function of time
(a) flicker noise
(b) white noise



(a)



(b)

Figure 5.9 Cycle to cycle jitter as a function of injected
(a) flicker noise
(b) white noise

For cycle jitter due to white noise, we can obtain it from the relationship between cycle jitter and cycle to cycle jitter, which is $\Delta T_{cc} = \sqrt{2}\Delta T_c$ and $\Delta T_c = 0.0135$ in this case. If we compare cycle jitter and cycle to cycle jitter for the three different noise conditions in our simulation, we can see this relationship holds, as shown in Table 5.1, the small deviation from $\sqrt{2}$ is due to the resolution of PSPICE, we have observed a better value in HSPICE.

Table 5.1 Relationship between cycle jitter and cycle to cycle jitter for white noise

	Cycle jitter (ps) ΔT_c	Cycle to cycle jitter (ps) ΔT_{cc}	$\Delta T_{cc} / \Delta T_c$
Injected noise 1	0.07610	0.11914	1.566
Injected noise 2	0.21849	0.34739	1.590
Injected noise 3	0.70650	1.14074	1.615

Herzel and Razavi have given an equation relating the rms value of absolute jitter and cycle to cycle jitter for white noise [69].

$$\Delta T_{abs} = \sqrt{\frac{f_0}{2}} \Delta T_{cc} \sqrt{\Delta t} \tag{5.4}$$

Since we have obtained the cycle to cycle jitter for white noise from our simulations, it is easy to get the rms absolute jitter using Equation (5.4). We have calculated the

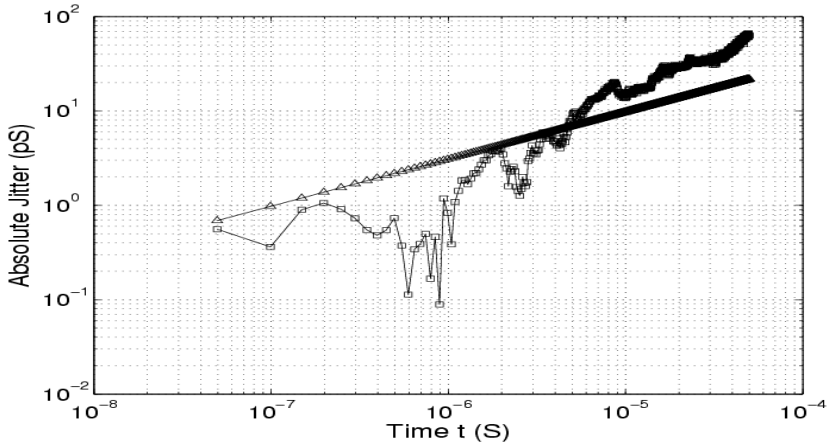
rms value of absolute jitter due to white noise for the three different noise conditions and have compared these to the simulated absolute jitter, the simulated absolute jitter should be very near the rms value and this trend is clearly shown in Fig.5.10.

In the above simulations, the frequency range for the injected noise is from 1Hz to1GHz, since the oscillation frequency is 1.352GHz, only timing jitter from low frequency noise due to an up conversion effect is involved in the simulations. In reality, there is also timing jitter from high frequency noise due to down conversion. We have extended the upper frequency limit to 20GHz, which is a typical cut off frequency for CMOS technology, and have repeated the above simulation procedure again. We get a cycle to cycle jitter of 0.0627ps for white noise. By using Equation (5.4), we have calculated the rms value of absolute jitter due to device white noise, as plotted in Fig. 5.11. Fig. 5.11 also shows the rms value calculated from an analytical formula introduced by A.Hajimiri [71]

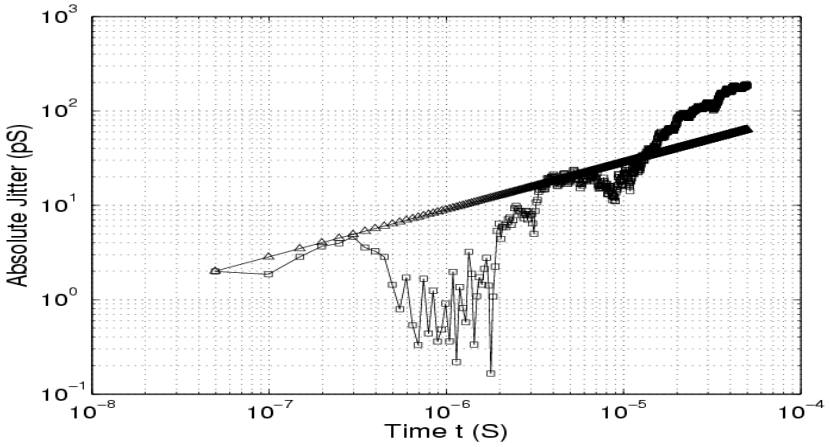
$$\Delta T_{abs} = \kappa\sqrt{\Delta t} \tag{5.5}$$

$$\kappa = \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \tag{5.6}$$

where η is 0.75 for single ended ring oscillators, P is total power dissipation, V_{DD} is the power supply voltage, V_{char} is the characteristic voltage of the device, defined as $V_{char} = \Delta V / \gamma$ for long channel devices, γ is 2/3 for long channel devices and $\Delta V = (V_{DD}/2) - V_T$.



(a)



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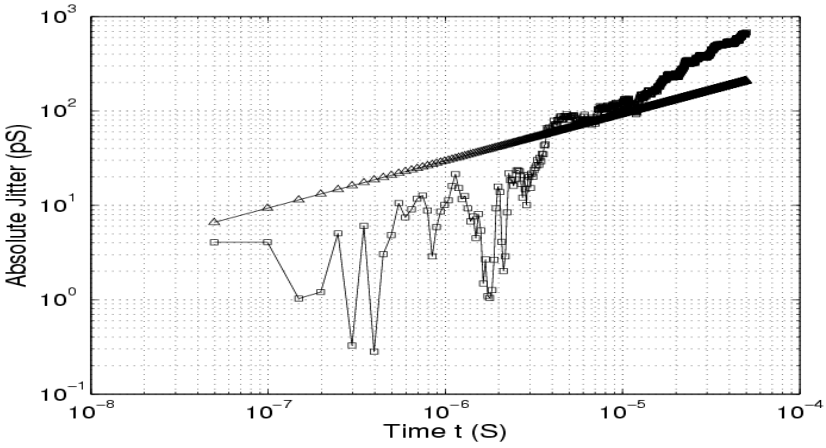


(c)

Figure 5.10 Comparison between simulated absolute jitter and calculated rms value
(a) Injected noise 1
(b) Injected noise 2
(c) Injected noise 3

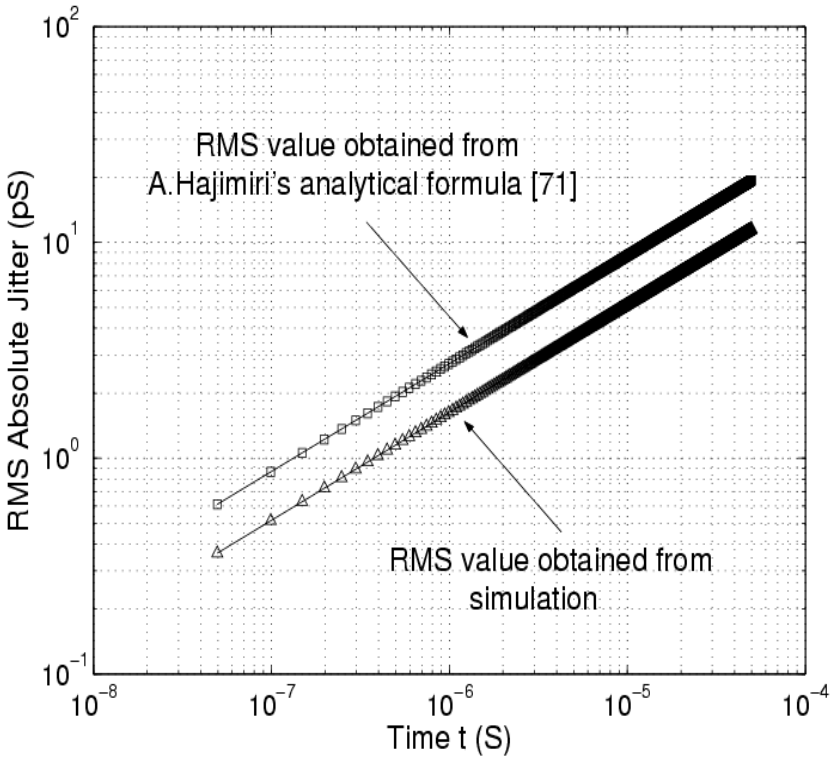


Figure 5.11 RMS absolute jitter versus time for white noise

From Fig.5.11, we can see at 1us, simulations predict a rms value of 1.63 ps, while A. Hajimiri's analytical formula yields 2.746 ps. The difference comes from the fact that there are some assumptions when deriving (5.6) in [71] such as $V_{TN} = |V_{TP}|$, which is not true in our case. Also the total channel noise given by Equation (18) in [71], 1.4472×10^{-23} A^2/Hz, is larger than our value obtained from analog simulations of device noise, 5.3438×10^{-24} A^2/Hz. A further check shows if we project back to the noise value 1.4472×10^{-23} A^2/Hz and then calculate the rms absolute jitter at a 1us interval, we obtain 2.678ps, which is very close to the analytical value 2.746ps obtained from A.Hajimiri's formula. A summary of the above analysis is shown in Table 5.2.

Table 5.2 Comparison of simulation results and A. Hajimiri's analytical model for RMS absolute jitter due to white noise at 1us

	Simulated value	Analytical value
RMS absolute jitter at 1us	1.63 ps (1)	2.746 ps (2)
	2.678 ps (2)	

(1) Corresponding to when total channel noise is $5.3438\times10^{-24}\,A^2/Hz$, obtained from analog simulations of device noise.

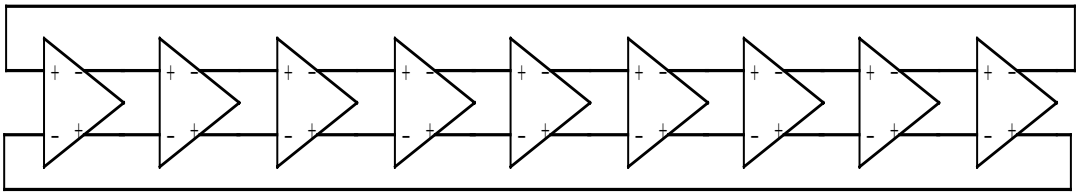
(2) Corresponding to when total channel noise is $1.4472\times10^{-23}\,A^2/Hz$, given by Equation (18) in [71]. The RMS value of absolute jitter obtained from simulations matches that obtained from A.Hajimiri's formula.

Fig.5.11 predicts the jitter performance due to white noise in a ring oscillator. If it were possible to derive a similar analytical relationship between rms absolute jitter and cycle to cycle jitter for flicker noise, we could then easily predict the whole jitter performance.

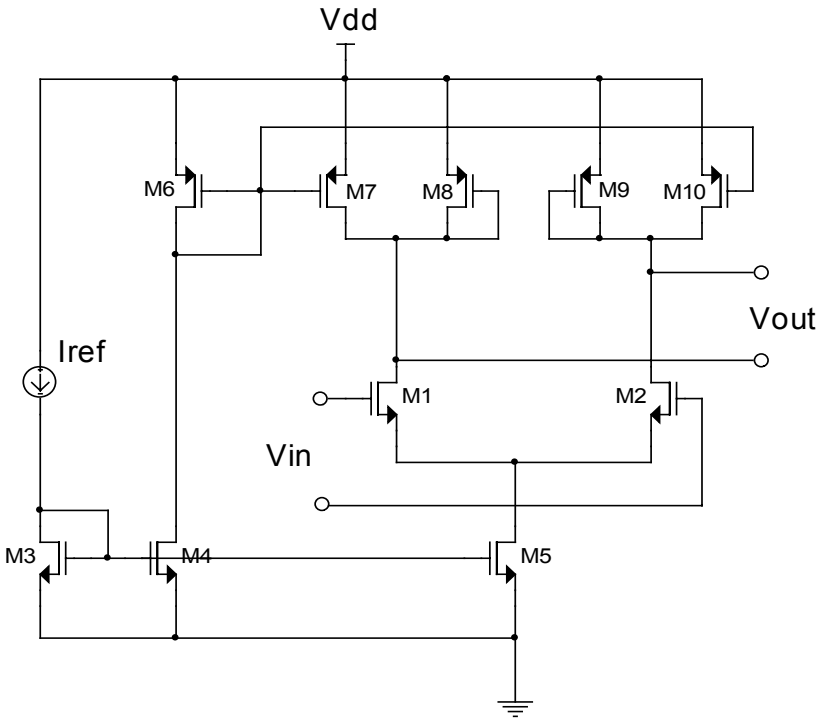
6. TIMING JITTER IN DIFFERENTIAL CMOS RING OSCILLATORS

6.1 Stationary Approach in Differential CMOS Ring Oscillators

The circuit to be simulated is shown in Fig.6.1, it is a nine-stage differential CMOS ring oscillator. The simulations were performed in HSPICE using IBM 0.18um transistor model.



(a)



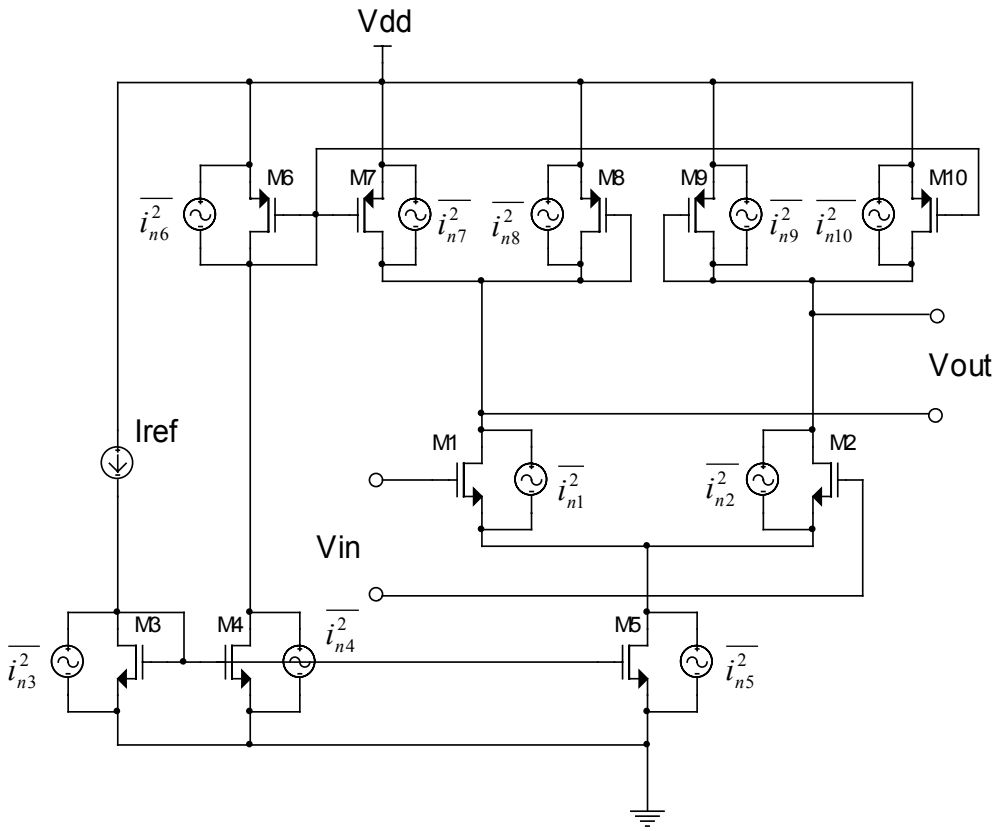
(b)

Figure 6.1 CMOS differential ring oscillator
(a) block diagram
(b) implementation of one stage

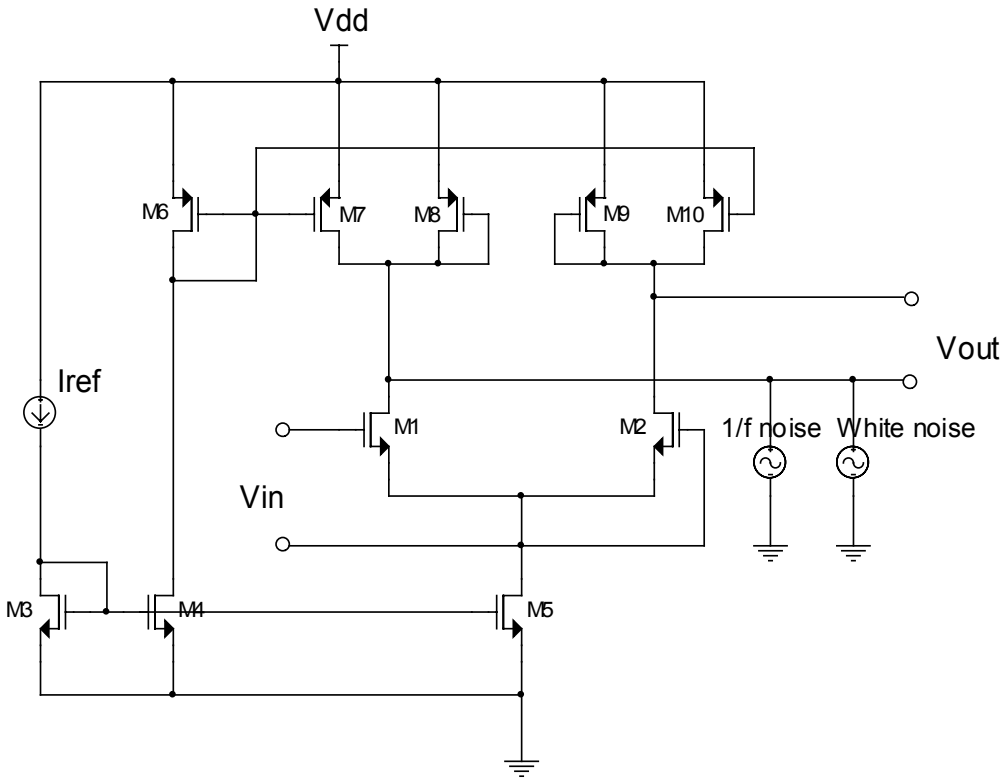
As in the case of single ended CMOS ring oscillator, in differential one, the primary concern is still to study the impact of device noise on timing jitter. The schematic for the inverter cell is repeated in Fig. 6.2 (a) with noise source added, where $\overline{i_{n1}^2}$,$\overline{i_{n2}^2}$,…, $\overline{i_{n10}^2}$ are the noise power spectral densities for transistors M_1,…M_{10}, these are the intrinsic output referred noise sources for each transistor. In our simulations, we use a common stationary approach to estimate the effects of all the noise sources [51][71]. Since we take differential output, the effects of all internal noise sources in the circuit can be replaced by an equivalent output referred noise source at one output, as shown in Fig. 6.2 (b). The two noise sources at output means we will inject and study 1/f noise and white noise separately. This equivalent noise power is calculated at a fixed DC bias condition that corresponds to DC biasing point of the oscillator. A linear circuit simulation is performed to get this noise power, as shown in Fig. 6.2 (c).

The small-signal equivalent circuit of the inverter cell for AC noise analysis is shown in Fig. 6.2 (d), where R_L and C_L represent the total resistance and capacitance at the output node. Differential noise analysis should be used in this case since we will take differential output. To determine the output, AC, differential voltage noise, the circuit in Fig. 6.2 (d) should be replaced by the circuit in Fig. 6.2 (e). In this circuit, the noise sources from each side are combined together, common mode noise sources associated with the current mirrors, M3-M6, are cancelled by each other, while differential ones added.

The introduction of the additional 1F capacitor is to find the total output referred noise. Since the impedance of 1F capacitor is much lower than that of R_L and C_L, all the noise current will flow through this way. If we have measured the differential noise voltage at node 1 and 2, then divided by impedance of 1F capacitor, we could obtain the total equivalent output referred noise current.

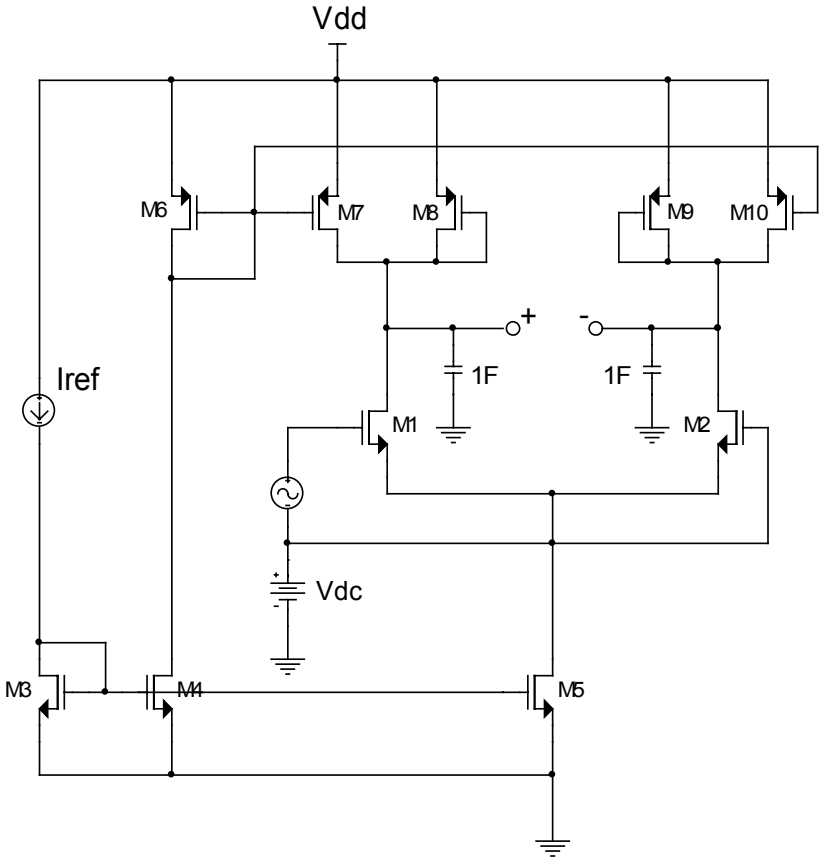


(a)



(b)

Figure 6.2 (Continued)



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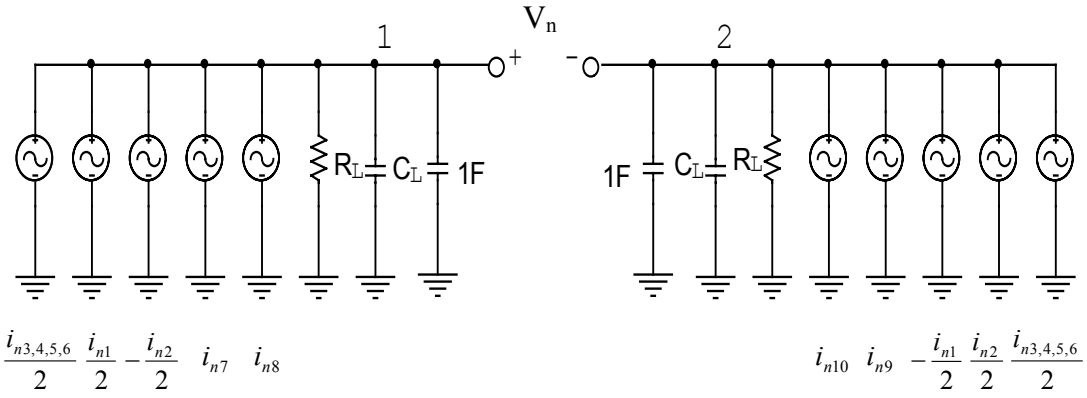
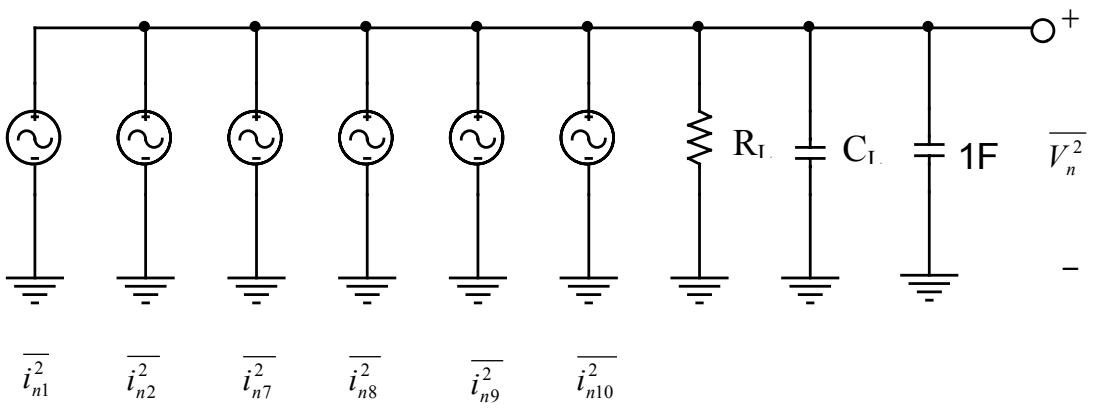


(d)

Figure 6.2 (Continued)



(e)

Figure 6.2 Illustration of stationary approach in differential CMOS Ring Oscillators
(a) Differential inverter cell with noise sources
(b) Equivalent output referred noise source
(c) Circuit used to get the device noise power
(d) Equivalent circuit for AC noise analysis
(e) Simplified differential AC noise analysis circuit

6.2 Simulation of Timing Jitter in Differential CMOS Ring Oscillators, Results and Discussion

Simulation procedures are the same as single ended CMOS ring oscillator, so they won't be repeated here. Simulation results are shown in Fig. 6.3 to Fig. 6.5. Fig. 6.3 shows the absolute jitter versus time, Fig. 6.4 and Fig. 6.5 show cycle jitter and cycle to cycle jitter versus time. The top part shows jitter due to flicker noise while lower part shows jitter due to white noise. From Fig. 6.3 we can see the variation of absolute jitter due to flicker noise has a dependence on the time, t, while for white noise, it has a, $t^{0.5}$, dependence. These are consistent with accepted theory in the literature [69-73]. Fig. 6.3 shows the measured rms value of absolute jitter due to flicker noise [Provided by Teradyne Inc.], as we expect, the simulated absolute jitter should be very near the rms value and this trend is clearly shown in Fig. 6.3 (a).

The cycle to cycle jitter we have obtained is 0.425 ps for flicker noise and 0.445 ps for white noise. Cycle jitter due to white noise is $\Delta T_c = 0.325\,\text{ps}$, the relationship between cycle jitter and cycle to cycle jitter due to white noise from simulations is consistent with the analytical formula $\Delta T_{cc} = \sqrt{2}\Delta T_c$, as shown in Table 6.1.

Table 6.1 Relationship between cycle jitter and cycle to cycle jitter for white noise

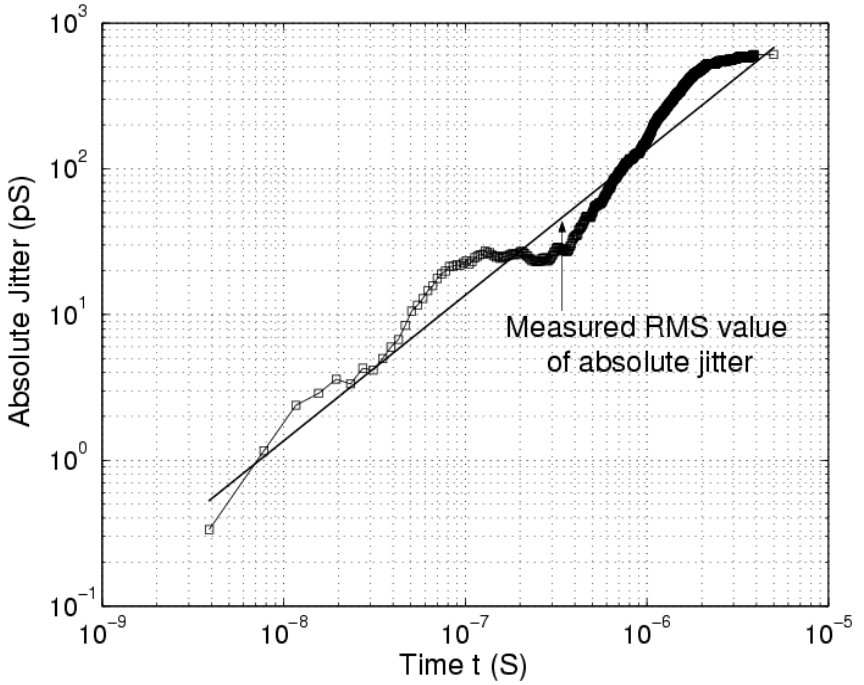
Cycle jitter (ps) ΔT_c	Cycle to cycle jitter (ps) ΔT_{cc}	$\Delta T_{cc} \big/ \Delta T_c$
0.325	0.445	1.369

Herzel and Razavi have given an equation relating the rms value of absolute jitter and cycle to cycle jitter for white noise [69].

$$\Delta T_{abs} = \sqrt{\frac{f_0}{2}} \Delta T_{cc} \sqrt{\Delta t} \tag{6.1}$$

Since we have obtained the cycle to cycle jitter for white noise from our simulations, it is easy to get the rms absolute jitter using Equation (6.1). We have calculated the rms value of absolute jitter due to white noise and have compared it to the simulated absolute jitter, plotted in Fig.6.3 (b), as in the case of flicker noise, the simulated absolute jitter varies but is near the rms value.

From the above analysis, the agreement between simulation and expected values all serves to verify the validity of our technique.



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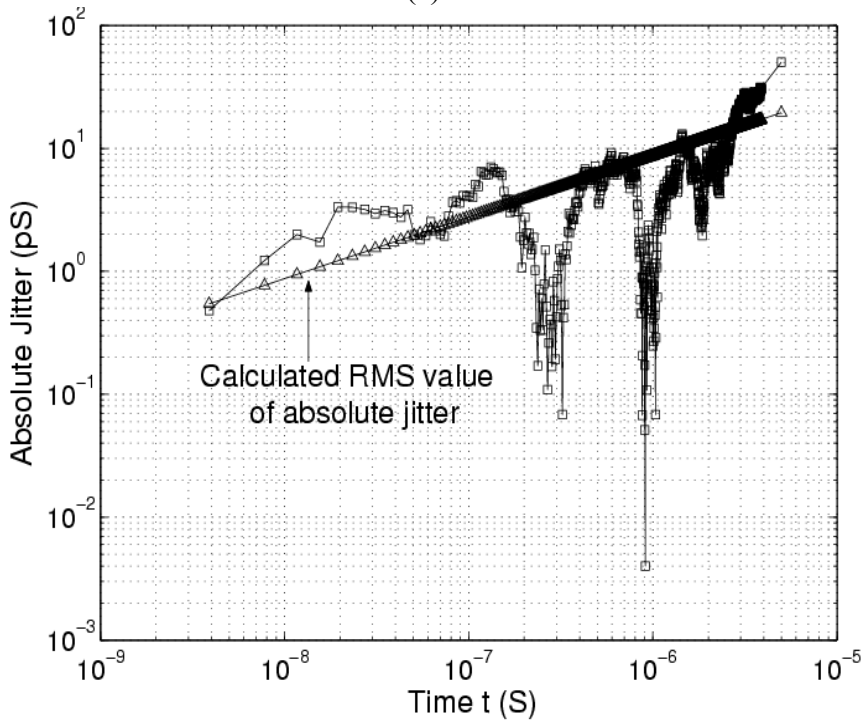
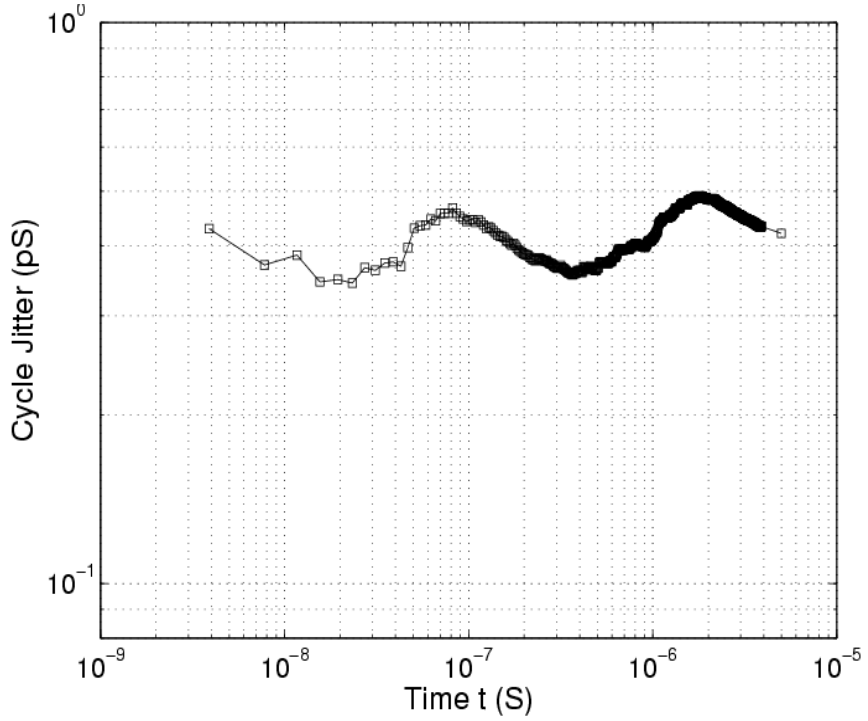


(b)

Figure 6.3 Absolute jitter as a function of time
(a) flicker noise
(b) white noise



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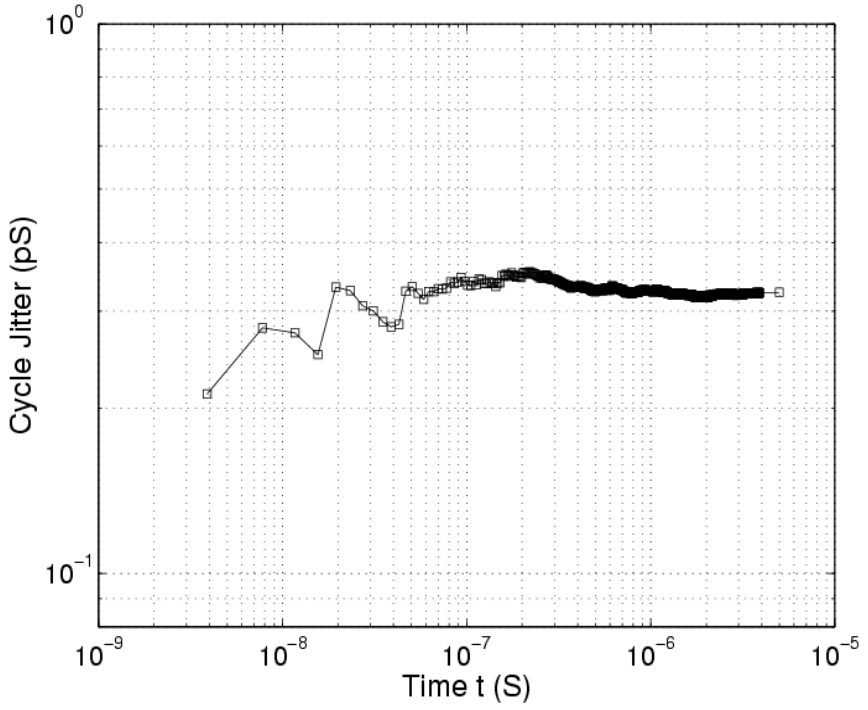
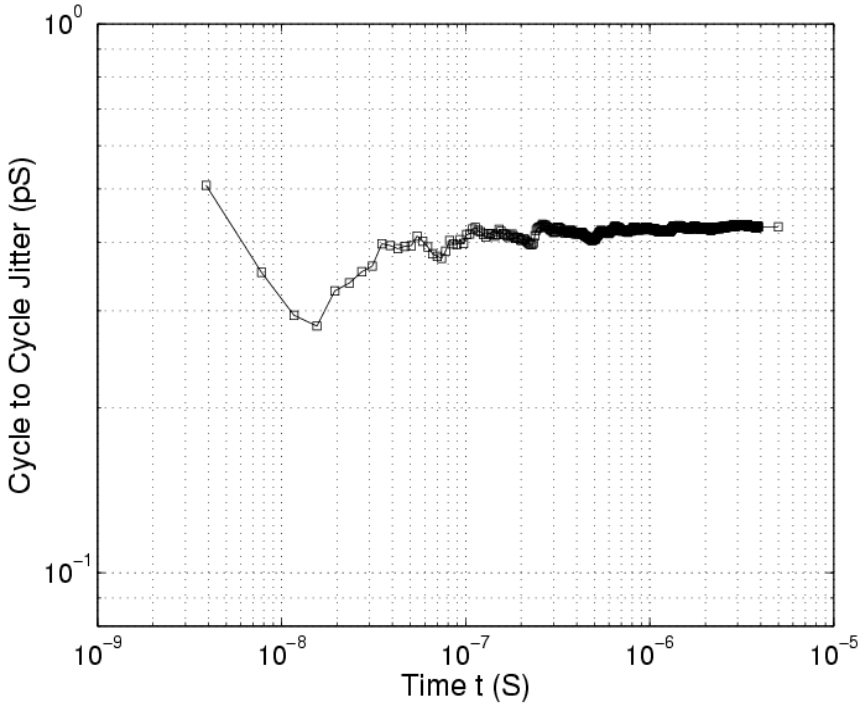


(b)

Figure 6.4 Cycle jitter as a function of time
(a) flicker noise
(b) white noise



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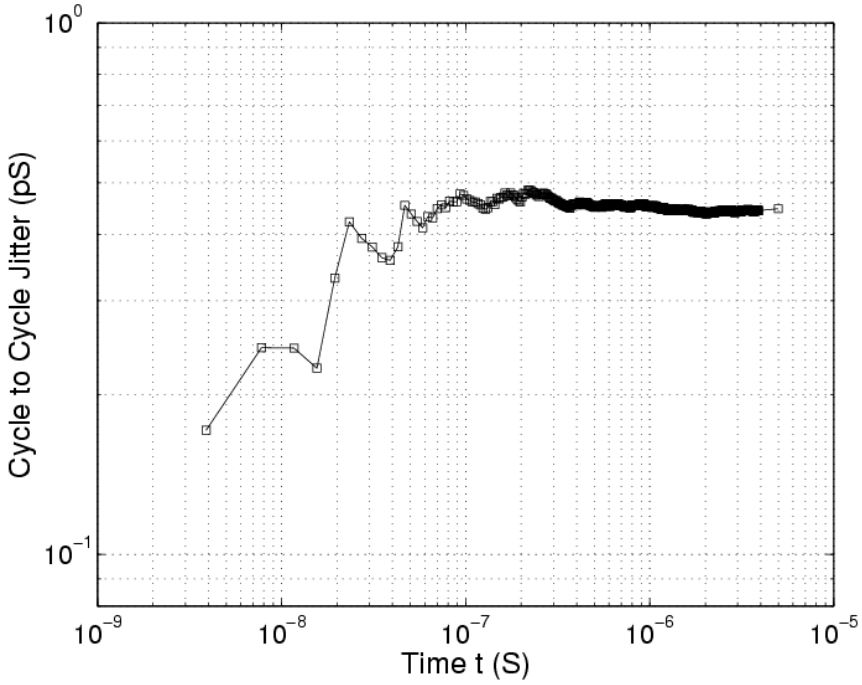


(b)

Figure 6.5 Cycle to cycle jitter as a function of time
(a) flicker noise
(b) white noise

7. TIMING JITTER IN SILICON BJT /OR SIGE HBT ECL RING OSCILLATORS

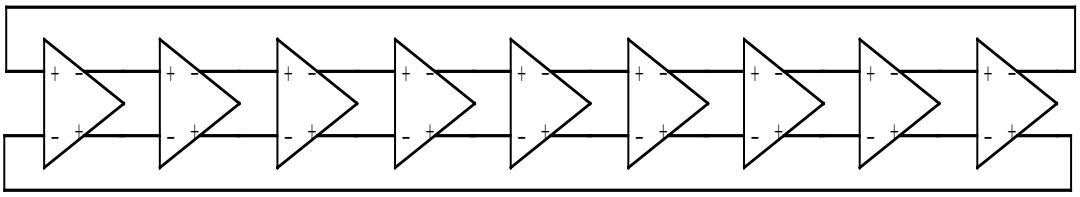
7.1 Stationary Approach in Silicon BJT /OR SiGe HBT ECL Ring Oscillators

We have employed the above methodology and investigated the timing jitter in silicon BJT /or SiGe HBT ECL ring oscillators. The circuit diagram is shown in Fig.7.1. It is a nine stage silicon BJT/or SiGe HBT ECL ring oscillator with V_{dd}=3 V [48][74][75]. The simulations were performed in HSPICE using a simple generic transistor model with a unity current gain frequency of 16 GHz and an IBM SiGe HBT transistor model respectively.

As in the case of the CMOS differential ring oscillator, in a silicon BJT/or SiGe HBT ECL ring oscillator, we use a common stationary approach to estimate the effects of all the noise sources. An equivalent output referred noise source is used to represent the effects of all internal noise sources in the circuit. Fig.7.2 shows an illustration of the total equivalent output noise power for one stage. The total equivalent output noise power for one stage of the silicon BJT and SiGe HBT oscillators are obtained from an analog noise SPICE simulation at output of one stage and calculated at a fixed DC bias condition when the stage is half way through a transition, as shown in Fig. 7.3.

Since in the silicon BJT transistor model, the default flicker noise coefficient KF is set to zero, we use the following method to obtain the PSD of flicker noise. The flicker noise is modeled by setting the total equivalent output noise corner frequency

fc to be 40kHz after the white noise has already been obtained from the circuit in Fig.7.3. Such a low l/f noise corner frequency, or even lower corner frequency, is commonly observed on small silicon bipolar transistor devices. In the SiGe HBT transistor model, flicker noise is calculated by the IBM default flicker noise coefficient KF.



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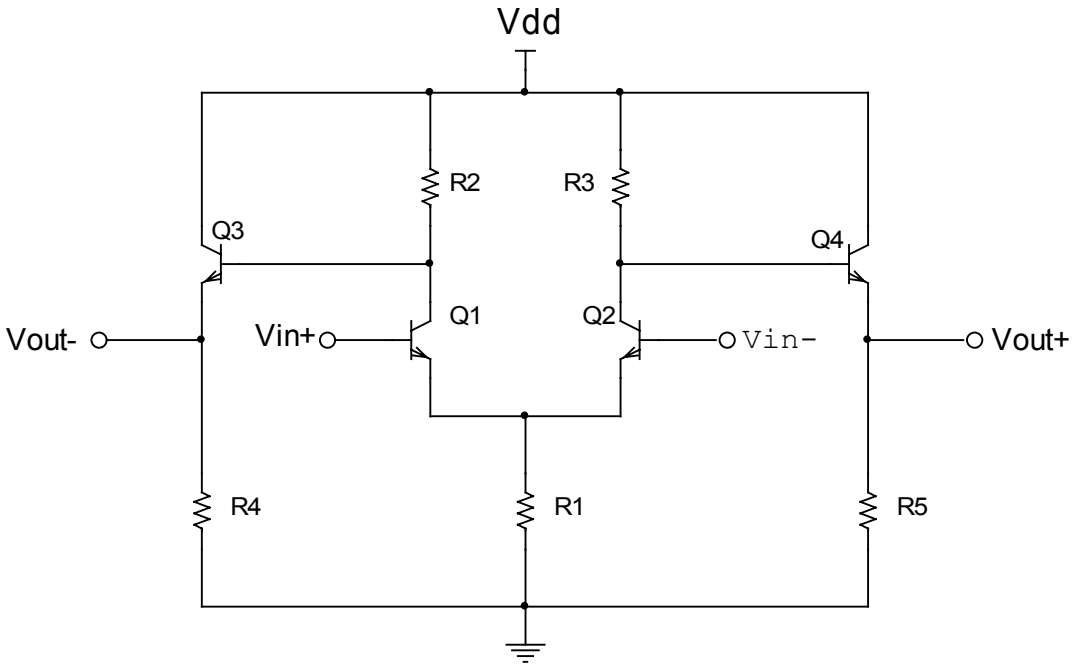


(b)

Figure 7.1 Nine stage silicon BJT/or SiGe HBT ECL ring oscillator
(a) block diagram
(b) implementation of one stage

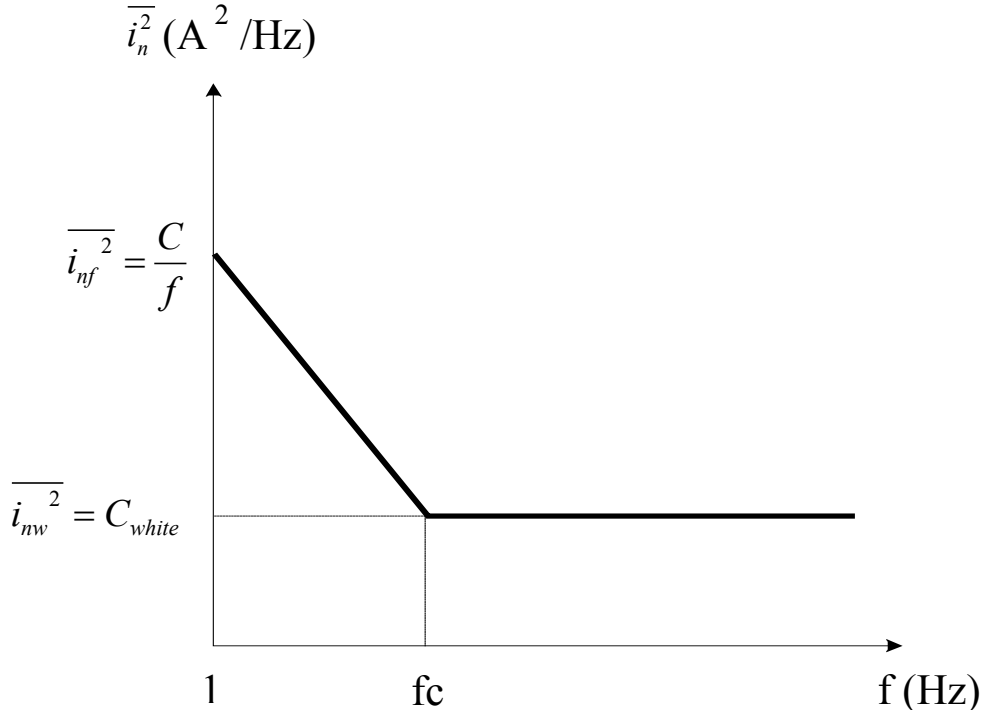


Figure 7.2 Illustration of output noise power for one stage of a silicon BJT/or SiGe HBT ring oscillator

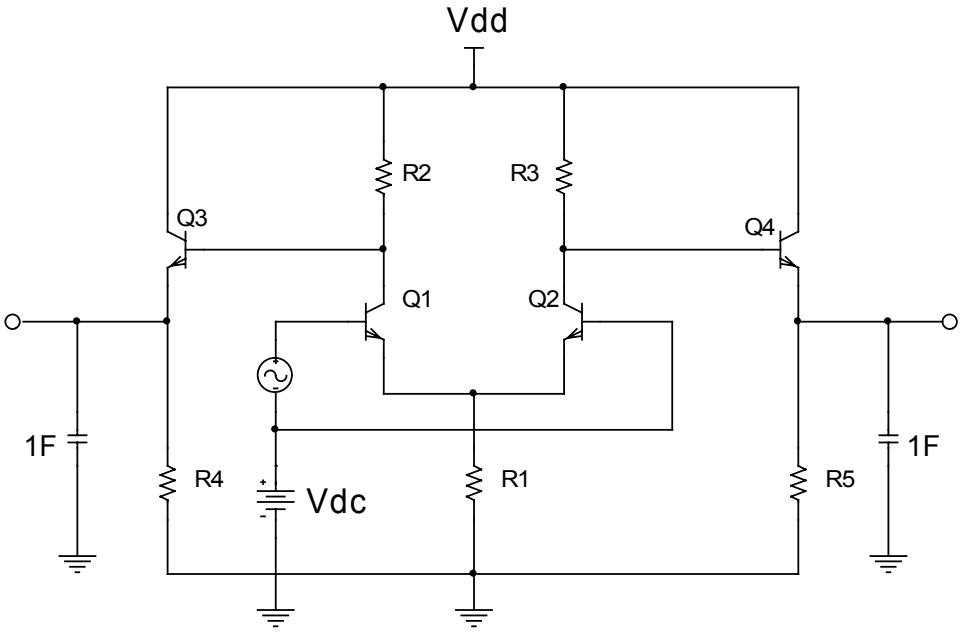


Figure 7.3 Circuit used to get the device noise power for silicon BJT/or SiGe HBT ECL ring oscillator

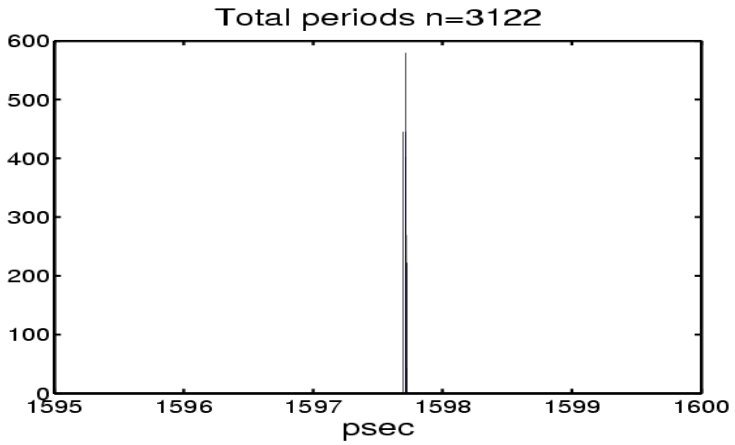
7.2 Simulation of Timing Jitter in Silicon BJT /OR SiGe HBT ECL Ring Oscillators, Results and Discussion

Simulation procedures are the same as CMOS differential ones, so they won't be repeated here. Fig. 7.4 shows the histograms of silicon BJT ECL ring oscillator clock periods for the noise free case, and the noise-injected case, SiGe HBT cases are similar but not shown here. Part (a) for the noise free case shows most of the clock periods being near a single value. Part (b) shows the variations in clock periods with white noise while Part (c) shows the variations in clock periods with flicker noise. These distributions in clock periods represent clock jitter.

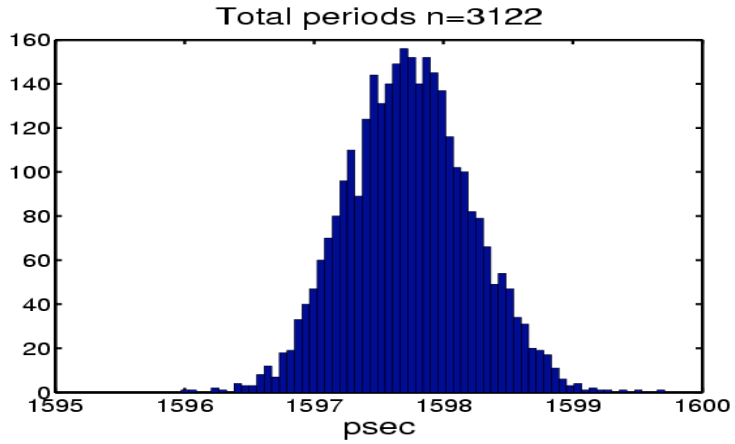
Fig. 7.5 shows the absolute jitter as a function of time for silicon BJT ring oscillator due to flicker noise. Simulation shows a jitter of 6ps for flicker noise after a 1us interval.

Fig. 7.6 shows the absolute jitter as a function of time for a SiGe HBT ECL ring oscillator due to flicker noise. Simulation shows a jitter of 144ps for flicker noise after a 1us interval.

For a free running oscillator, cycle jitter and cycle to cycle jitter are often used, however in some cases, we are more concerned with absolute jitter. We have compared the simulation results of absolute jitter for CMOS, silicon BJT and SiGe HBT ring oscillators. The results are shown in Table 7.1. From Table 7.1, we can see, compared to a CMOS ring oscillator, the silicon BJT ring oscillator has a much lower jitter while these two oscillators have a similar oscillation frequency. For the



(a)



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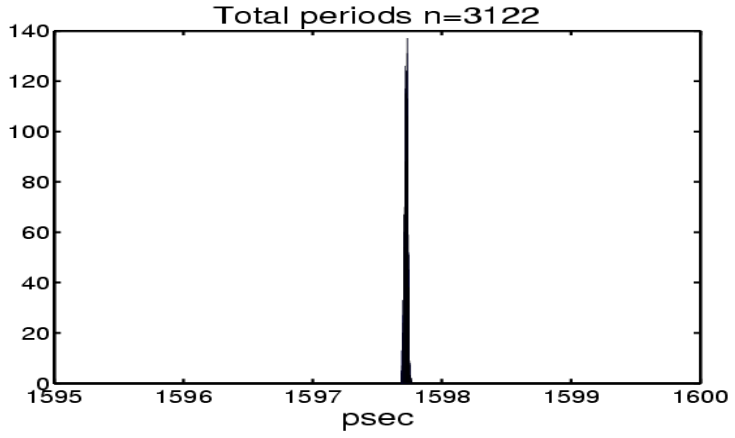

(c)

Figure 7.4 Histogram of silicon BJT ECL ring oscillator clock periods
(a) for noise free case
(b) for white noise-injected case
(c) for flicker noise-injected case

SiGe HBT ring oscillator, the absolute jitter is close to that of the CMOS one, however, we should note that the oscillation frequency of the SiGe HBT ring oscillator is much higher than that of the CMOS one, at the same time interval it has more clock periods. Since absolute jitter is an accumulated effect, the more clock periods, the more jitter which will accumulate. If we make a comparison at the same number of clock periods, we should expect a lower jitter for the SiGe HBT ring oscillator. Thus silicon BJT and/or SiGe HBT ring oscillators are a potential choice for low jitter applications.

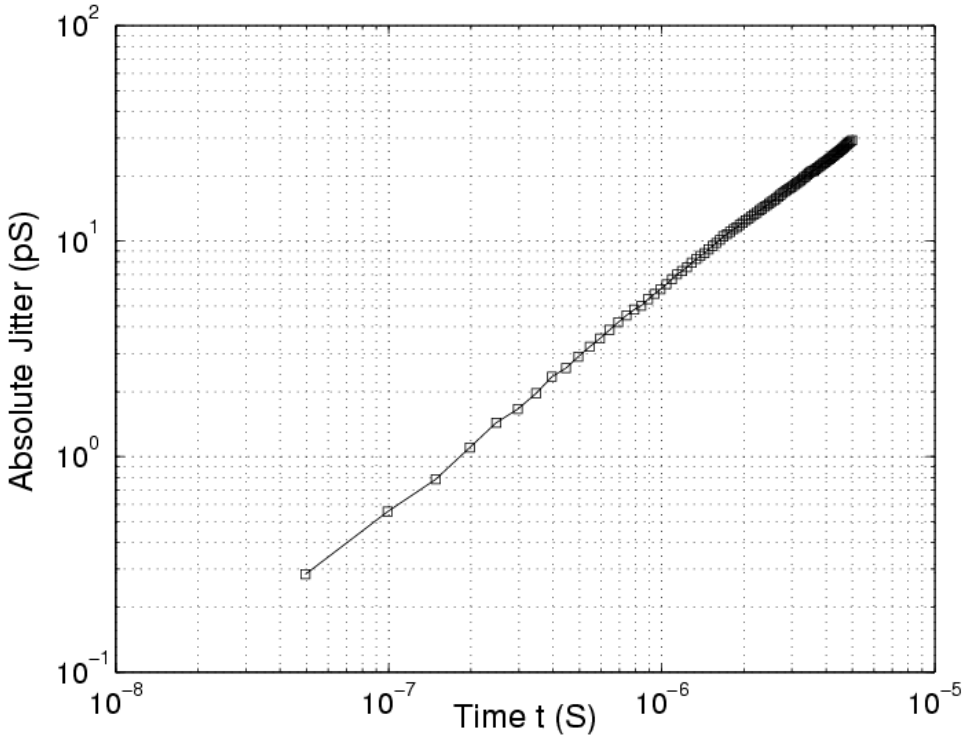

Figure 7.5 Absolute jitter as a function of time for silicon BJT ECL ring oscillator due to flicker noise

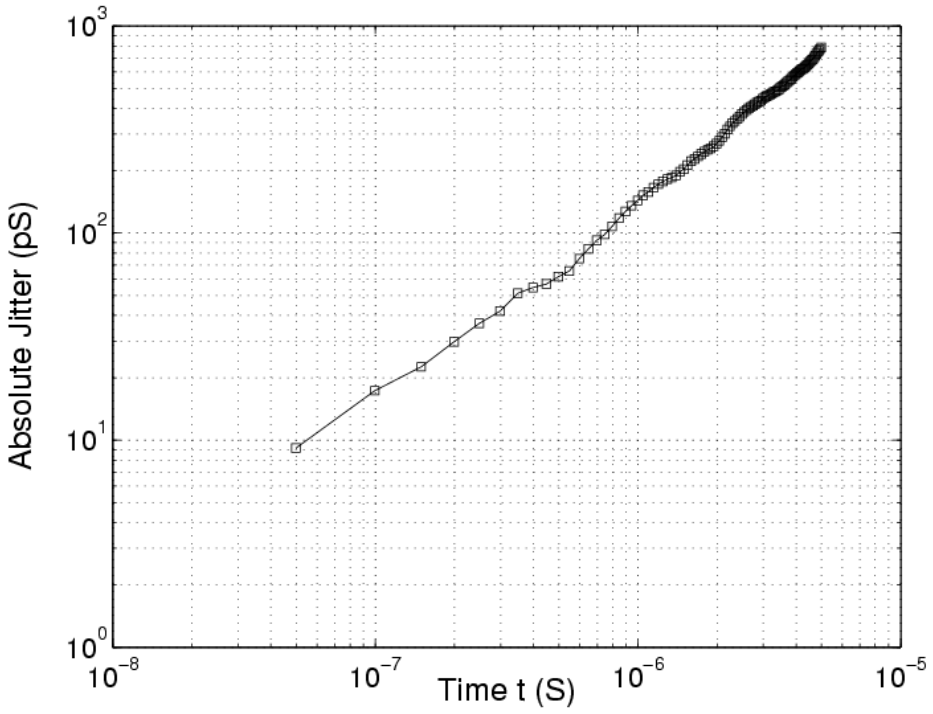

Figure 7.6 Absolute jitter as a function of time for SiGe HBT ECL ring oscillator due to flicker noise

Table 7.1 Absolute jitter due to flicker noise at 1us for three different types of oscillator

Oscillator type	Absolute Jitter (ps)	Oscillation Frequency (MHz)
CMOS	152	772
Silicon BJT	6	626
SiGe HBT	144	2271

8. CONCLUSION

In the first part of this dissertation work, we have demonstrated from theory and experiment that 1/f noise in bipolar transistors, with a low impedance in the base circuit, has a strong dependence on collector-emitter voltage and power dissipation at frequencies in the kHz range. A detailed comparison between the theory and the 1/f noise measured on bipolar transistors has been given in this dissertation work. It can be seen our theory fits the experimental data at the higher frequencies. At low frequency 1Hz and below, further work needs to be done to refine the model. However, noise at such low frequencies is not relevant to phase noise in communication systems. These new results are particularly relevant to phase noise in voltage-controlled oscillators and the engineering choice of whether to use CMOS or bipolar technology in wireless communication systems.

Interestingly enough temperature fluctuations might well describe some of the low frequency noise observed in vacuum tube devices and for which there never was any completely satisfactory explanation.

In the second part of this dissertation work, we have developed a large signal transient simulation technique to simulate phase noise due to device noise in a 2G Hz BJT LC oscillator. Flicker and white noise are simulated as a sum of sine waves with different amplitudes and random phase in MATLAB, which has a 1/f or white characteristics after FFT, then injecting into LC BJT oscillator and upconvert into phase noise. The simulation results are consistent with the empirical theory that the

phase noise resulting from direct upconvertion of flicker noise has a $1/f^3$ and white noise has a $1/f^2$ dependence on offset frequency. It is also shown that phase noise at 4.7 MHz offset from flicker noise is -150.7 dBC/Hz and from white noise is –132 dBc/Hz. At this point it is white noise dominated. The simulation result is in good agreement with the experimental value of –136 dBc/Hz at this offset frequency reported in the literature by Zannoth and Kolb [56], our simulation is able to predict phase noise correctly. The development of such technique to simulate phase noise in the oscillator will be very helpful in designing low phase noise oscillators.

In the third part of this dissertation work, we have developed a time-domain method to simulate timing jitter due to device noise and have applied it to a three stage single-ended and a nine-stage differential ring oscillator. An equivalent output referred noise source is used to represent the effect of all internal noise sources in the circuit. Flicker and white noise, which is simulated as a sum of sine waves with random phase by using MATLAB, is then modeled as the equivalent output referred noise and injected into the output of each stage as a PSPICE/HSPICE piecewise linear waveform. A time domain transient analysis is then performed and output data is analyzed by MATLAB to calculate the timing jitter. Simulation results show the variation of absolute jitter due to flicker noise has a, t, dependence, while for white noise, it has a, $t^{0.5}$, dependence. These are consistent with accepted theory. Two important parameters cycle jitter and cycle to cycle jitter used to describe jitter performance can be obtained from the simulations. A comparison between simulated data and an analytical formula is also given in this dissertation work, and it shows

that the simulated absolute jitter is near the rms value predicted by an analytical formula. The relationship between cycle jitter and cycle to cycle jitter due to white noise from simulations is consistent with the analytical formula. The rms value of absolute jitter due to white noise obtained from simulations matches that obtained from A.Hajimiri's formula. Simulation results are also compared with measurement results, it is shown that simulation results are very close to measurement results. All these serve to verify the validity of this technique.

There have been some analytical techniques to predict jitter [69-73], unfortunately, however, the analytical techniques have been developed only for white noise and not 1/f noise. The absolute jitter due to 1/f noise is usually more important since it increases linearly with time [71]. We have demonstrated here a technique to simulate the absolute jitter due to 1/f noise.

We have employed this methodology and investigated timing jitter in silicon BJT and SiGe HBT ECL ring oscillators. We have shown silicon BJT and SiGe HBT oscillators have lower jitter compared to their CMOS counterparts. As such silicon BJT and/or SiGe HBT ring oscillators are a potential choice for low jitter applications. Silicon BJT and/or SiGe HBT's have much lower l/f noise corner frequencies [76,77] than CMOS devices.

The method described in this dissertation is also applicable to other types of oscillators such as LC oscillators, as well as other kinds of noise source as power supply and substrate noise. The ability to predict the impact of timing jitter in electronic circuits via simulation is useful in designing low jitter circuits [78].

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APPENDICES

Appendix A: Device Noise Measurement

Two kinds of approaches are used to determine the device noise. One is an automated measurement, Fig. A.1. shows the schematic of the automated noise measurement system for NPN bipolar transistor. In order to reduce any power supply noise effect at the collector node, the NPN transistor is connected upside down with negative power supplies to its base and emitter.

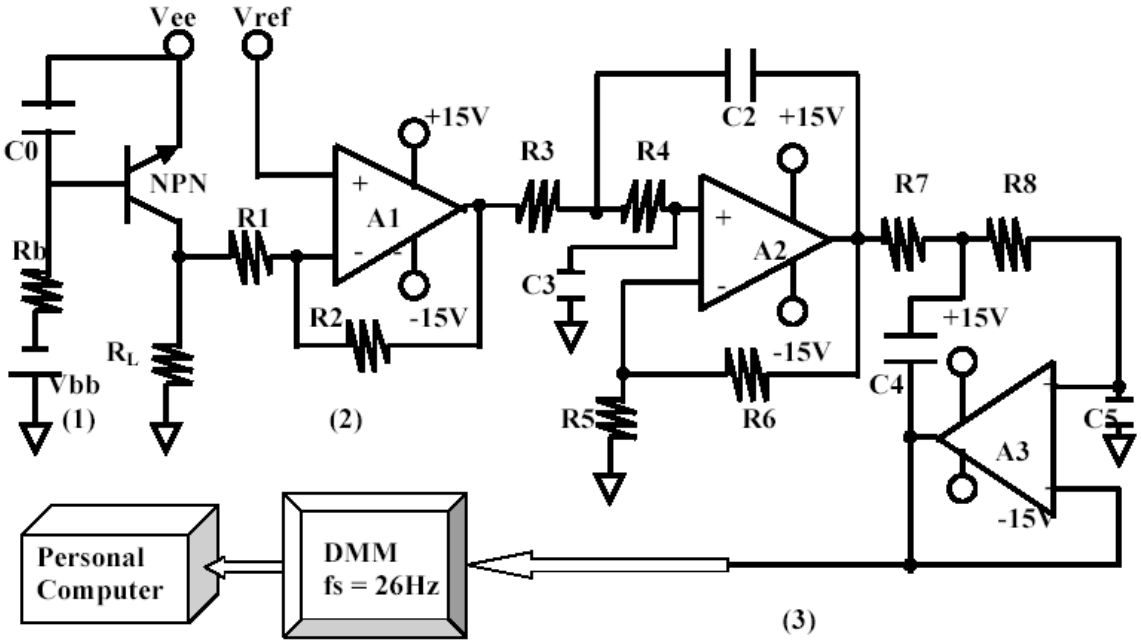

Figure A.1 Automated Noise Measurement System

The other one, ADC board based measurement system has been developed for measurement at higher frequencies. Fig. A.2. shows the schematic of such measurement system. The transistor setup is the same as that in the automated setup.

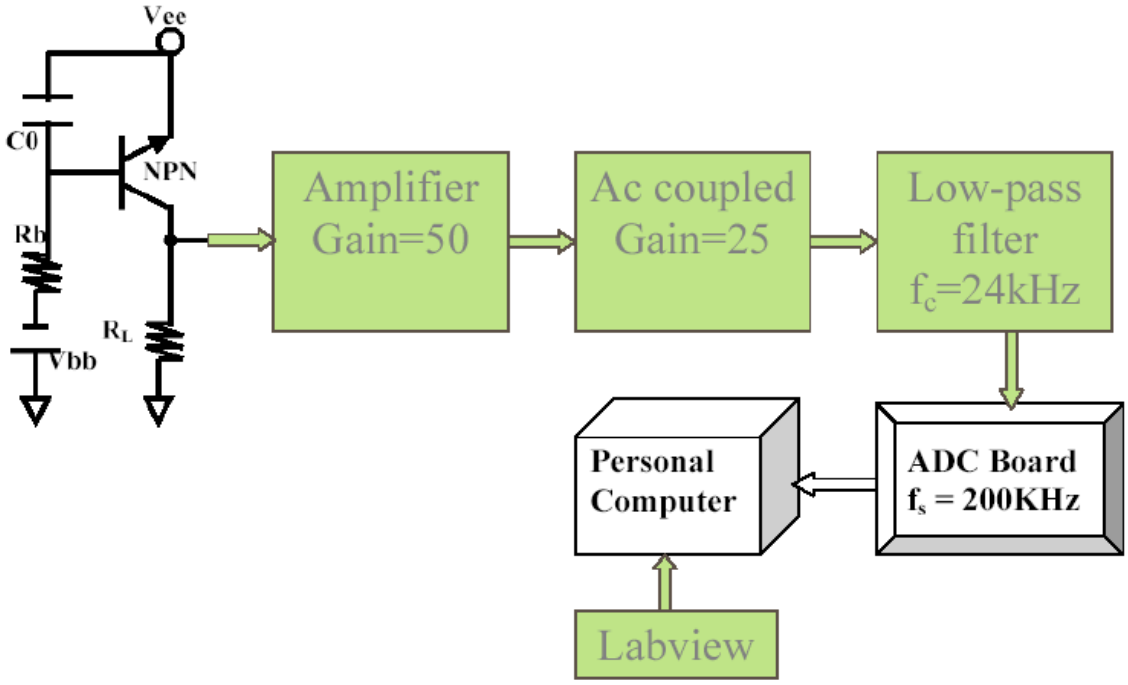

Figure A.2 ADC Board Based Noise Measurement System

The measured time domain noise data is post processed by a MATLAB program. The results are plotted in frequency domain.

```
% PSD of npn bjt 1/f noise
% data is taken from lab

clear all; close all

item = 'Measured NPN BJT current  noise';
load 'pn2222a3.dat'              %BJT 100000 data
Vout = pn2222a3;
%Vref = ;    %balance voltage supply --need to change each data
date = '5/16/00';                        %the date when data is taken
fs=26;                           %sampling rate of DMM
gain=90;                         %noise amplification by LM741
Rload=100;       %load resistor
Vnoise = Vout./gain;
%Vnoise = (Vref - Vout)./gain;  %unit= V
Inoise = ( Vnoise./Rload);    %unit= A
L = length(Inoise);      % L is also a window size. As L get larger magnitude of FFT
% gets closer to theoretical value

%SETUP AXIS
f = fs .* ( 0:1/L:1-1/L ); % up to f=fs
f = f(1:L/2); % up to fs/2
time=(0:L-1)/fs;

%PSD of NOISE
mag = (1/(L*fs))*abs( fft(Inoise) ).^2; %unit= A^2/Hz
mag = mag(1:L/2);

figure(1);
subplot(2,1,1);
        plot(time,Inoise); grid on;
        %axis([0.1,100,1e-22,1e-8]);%
        title(sprintf('%s (%d pts, %s)',item,L,date));
        xlabel('Time (S)');
        ylabel('Magnitude (A)');
        zoom on

subplot(2,1,2);
        loglog(f,mag,'r'), hold on, grid
```

```
        %axis([0.1,100,1e-22,1e-8]);
        title('PSD of NPN BJT PN2222A Noise RL=100.0 ohm Vee=11.2V
Ic=10mA');
        %title('PSD of Collector Current  Noise  (Rl=100 ohm)');
        xlabel('Frequency (Hz)'); ylabel('PSD of collector current noise (A^2/Hz)');
  hold on, loglog(f,1e-17./f.^2,'k')
  hold on, loglog(f,1e-17./f.^1,'b-.'),
  zoom on
  hold off
```

Appendix B: MATLAB Program for Modeling of Random Phase Flicker Noise and White Noise

I. Random-Phase Flicker Noise Simulation by Matlab (File name: cmosfjll.m)

```
clear all; close all

AF=1;              % known constant
CF=5.82286e-14;    % assumed CF value

% frequency changes from 1Hz to 10 GHz in logspace

f=logspace(0,10,1000);
nf=length(f);
deltaf=diff(f);
f(:,nf)=[ ];

rand('state',sum(100*clock)); % rand function in MATLAB

x=rand(length(f),1);

% HSPICE Level 2&3 1/f noise in NMOS
flicker=CF./(f.^AF);                % unit=A^2/Hz
Ind=flicker.^0.5;                   % unit=A/Hz^0.5

% amplitude of drain current noise
Iamp=Ind.*deltaf.^(1/2);            % unit=A

% Save data into files for MS EXCEL use
f1=f'; flicker1=flicker'; Iamp1=Iamp';
outputdata1=[f1 flicker1]; outputdata2=[f1 Iamp1];
save figure1.dat outputdata1 -ascii
save figure2.dat outputdata2 -ascii

figure(1)
subplot(2,2,1)
loglog(f,flicker,'-*'); grid on;
%title('Modeling flicker noise with KF= ');
xlabel('Frequency (Hz)');
ylabel('Flicker noise (A^2/Hz)'); zoom on
```

```
subplot(2,2,2)
        loglog(f,Iamp,'*'); grid on;
        axis([1e0,1e9,1e-7, 1e-5]);
        %title('Calculated amplitude of sine waves with KF= ');
        xlabel('Frequency (Hz)');
        ylabel('Amplitude of sine waves (A)');
zoom on

n=100;
tstart=0;
tstop=0.5e-6;
outputdata3=[ ];

for i=1:n

% total MATLAB simulation time with 100ps sampling delay
% total simulation time needs to be larger than the final Tstop Value in the transient
% analysis

t=tstart:1e-10:tstop;

%for i=1:length(f)
%       x=rand(1);
%        sum1(i,:)=Iamp(i)*sin(2*pi*f(i)*t+2*pi*x);
%end
%        sum2=sum(sum1);

Imat=repmat(Iamp',1,length(t));
fmat=repmat(f',1,length(t));
tmat=repmat(t,length(f),1);

xmat=repmat(x,1,length(t));

sum1=Imat.*sin(2*pi*fmat.*tmat+2*pi*xmat);

sum2=sum(sum1);

t1=t'; sum3=sum2';
noise1=[t1 sum3];
noise2=[outputdata3;noise1];
outputdata3=noise2;

clear t t1 *mat sum* noise*;

tstart=tstop+1e-10;
```

```
tstop=tstop+0.5e-6;

end

% Save data into file for HSPICE simulation and EXCEL use

save figure3.dat outputdata3 -ascii

% 1/f noise with random phase
% data is taken from Matlab simulation
load 'figure3.dat'
time=figure3(:,1);
noise=figure3(:,2);

subplot(2,2,3)
        plot(time*1e6,noise*1e6); grid on;
        xlabel('Time  (us)');
        ylabel('Sum of Sine waves with random phase (uA)');
        %title('Sum of sine waves with random phase with KF=   ');

fs=1e10;                        % sampling frequency

L=32768;   % L is also a window size. As L get larger magnitude of FFT gets closer
% to theoretical value

%SETUP AXIS
f1 = fs.* ( 0:1/L:1-1/L ); % up to f=fs
a = L/2;
a = round(a);
f = f1(2:a);                % up to fs/2

mag = fft(noise,L); % L is the size of windows

% Power Spectral Density (PSD)
power = mag.* conj(mag) /(fs* L);
power = power(2:a);
subplot(2,2,4);
        loglog(f,power,'*')
        axis([0,1e9,1e-24, 1e-14]);
        grid on;
        %title('Power spectral density of the sum of sine waves with random phase');
        xlabel('Frequency (Hz)');
        ylabel('PSD of the Sum  (A^2/Hz)');
        hold on;
loglog(f,1e-10./f.^1,'k'), text(1e6, 2e-16, '1/f');
```

```
zoom on;

% Save data into file for EXCEL use
f2=f'; mag1=power;
outputdata4=[f2 mag1];
save figure4.dat outputdata4 -ascii
```

II. Random-Phase White Noise Simulation by Matlab (File name: whitel_jitter.m)

```
clear all; close all

% frequency changes from 1Hz to 20 GHz in logspace

f=logspace(0,10.3011,1000);
nf=length(f);
deltaf=diff(f);
f(:,nf)=[ ];

rand('state',sum(100*clock)); % rand function in MATLAB

x=rand(length(f),1);

% HSPICE white noise
white=2.1121e-20*ones(size(f));      % unit=A^2/Hz
Ind=white.^0.5;                      % unit=A/Hz^0.5

% amplitude of current noise
Iamp=Ind.*deltaf.^(1/2);               % unit=A

% Save data into files for MS EXCEL use
f1=f'; white1=white'; Iamp1=Iamp';
outputdata1=[f1 white1]; outputdata2=[f1 Iamp1];
save figure1.dat outputdata1 -ascii
save figure2.dat outputdata2 -ascii

figure(1)
subplot(2,2,1)
        loglog(f,white,'-*'); grid on;
        %title('Modeling white noise with white nosie=1.1e-14 A^2/Hz');
        xlabel('Frequency (Hz)');
        ylabel('white noise (A^2/Hz) (A^2/Hz)'); zoom on
```

```
subplot(2,2,2)
        loglog(f,Iamp,'*'); grid on;
        %axis([1e0,1e9,1e-8, 1e-6]);
        %title('Amplitude of sine waves when white nosie=1.1e-14 A^2/Hz');
        xlabel('Frequency (Hz)');
        ylabel('Amplitude of sine waves (A)');
zoom on

n=100;
tstart=0;
tstop=0.5e-6;
outputdata3=[ ];

for i=1:n

% total MATLAB simulation time with 100ps sampling delay
% total simulation time needs to be larger than the final Tstop Value in the transient
% analysis

t=tstart:1e-10:tstop;

%for i=1:length(f)
%       x=rand(1);
%        sum1(i,:)=Iamp(i)*sin(2*pi*f(i)*t+2*pi*x);
%end
%        sum2=sum(sum1);

Imat=repmat(Iamp',1,length(t));
fmat=repmat(f',1,length(t));
tmat=repmat(t,length(f),1);

xmat=repmat(x,1,length(t));

sum1=Imat.*sin(2*pi*fmat.*tmat+2*pi*xmat);

sum2=sum(sum1);

t1=t'; sum3=sum2';
noise1=[t1 sum3];
noise2=[outputdata3;noise1];
outputdata3=noise2;

clear t t1 *mat sum* noise*;

tstart=tstop+1e-10;
```

```
tstop=tstop+0.5e-6;

end

% Save data into file for HSPICE simulation and EXCEL use

save figure3.dat outputdata3 -ascii

% white  noise with random phase
% data is taken from Matlab simulation

load 'figure3.dat'
time=figure3(:,1);
noise=figure3(:,2);

subplot(2,2,3)
        plot(time*1e6,noise*1e6); grid on;
        xlabel('Time  (us)');
        ylabel('Sum of Sine waves with random phase (uA)');
        %title('Sum of sine waves with random phase');

fs=1e10;                        % sampling frequency

L=32768;   % L is also a window size. As L get larger magnitude of FFT gets closer
% to theoretical value

%SETUP AXIS
f1 = fs.* ( 0:1/L:1-1/L ); % up to f=fs
a = L/2;
a = round(a);
f = f1(2:a);                % up to fs/2

mag = fft(noise,L); % L is the size of windows

% Power Spectral Density (PSD)
power = mag.* conj(mag) /(fs* L);
power = power(2:a);
subplot(2,2,4);
        loglog(f,power,'*')
        %axis([0,1e9,1e-24, 1e-16]);
        grid on;
        %title('Power spectral density of the sum of sine waves with random phase');
        xlabel('Frequency (Hz)');
        ylabel('PSD of the Sum  (A^2/Hz)');
        hold on;
```

```
zoom on;

% Save data into file for EXCEL use
f2=f'; mag1=power;
outputdata4=[f2 mag1];
save figure4.dat outputdata4 -ascii
```

Appendix C: Procedure of Phase Noise Simulation in Oscillators

I. Noise data creation

Create noise data by using cmosfjll.m (for flicker noise) and whitel_jitter.m (for white noise) if PSD of flicker noise and white noise is given

II. HSPICE PWL Noise source

Write noise data into HSPICE PWL format, named as for example flicker.dat. Here is an example.

```
* Injection of 1/f noise

Inoise 9 4 pwl(0.0000000e+00   5.4859467e-07
+  1.0000000e-10   7.2983248e-07
+  2.0000000e-10   8.6251607e-07
+  3.0000000e-10   9.6382932e-07
+  4.0000000e-10   1.0562798e-06
+  5.0000000e-10   1.1569508e-06
+  6.0000000e-10   1.2689078e-06
+  7.0000000e-10   1.3778292e-06
+  8.0000000e-10   1.4551343e-06
+  9.0000000e-10   1.4666769e-06
+  1.0000000e-09   1.3841976e-06
+  1.1000000e-09   1.1958028e-06
+  1.2000000e-09   9.1205438e-07
+  1.3000000e-09   5.6566431e-07
+  1.4000000e-09   2.0481241e-07
+  1.5000000e-09  -1.1794364e-07)
```

III. Noise source injection

Add PWL formatted noise data into noise free case file by add

.include flicker.dat command in sample.sp file, run noise injected case simulation.

The following setup should be included in spice file at all simulations

```
.include flicker.dat
.options ACCURATE=1
.option post
.op
.tran 0.00489e-10 0.41076us
.fft v(9) np=16384 window=harris
.end
```

output file is sample.lis

IV. Extract FFT analysis data from sample.lis

On the Unix command line, run

```
cat sample.lis | awk '{while($0 !~ /frequency/) {getline;} while($0 !~ /job/)
{printf("%s %s\n",$2, $3); getline;}; if($0 ~ /job/) {exit;}}' >! sample.txt
```

V. Post process noise injected case data

Phase noise is expressed in the unit of dBc/Hz, which stands for dB below carrier per Hz. The output from HSPICE FFT analysis is not in this unit, we need to normalize the results to dB below carrier per Hz.

If Harris Window np = 2048 points

transient analysis up to 0.0978 uS

Then sampling time $\Delta t = \frac{0.0978}{2048} = 4.775 \times 10^{-11} S$

Sampling frequency $f = \frac{1}{\Delta t} = \frac{1}{4.775 \times 10^{-11}} = 20.94 GHz$

Simulation output is up to half of sampling frequency

Frequency interval $\Delta f = \frac{20.94 \times 10^{9}}{2048} = 1.02 \times 10^{7} Hz$

$$
\begin{aligned}
dBc/Hz &= 10 \cdot \log(\frac{V \cdot V^*}{\Delta f}) \\
&= 10 \cdot \log(V \cdot V^*) - 10 \cdot \log(\Delta f) \\
&= 10 \cdot \log(V \cdot V^*) - 10 \cdot \log(1.02 \times 10^7) \\
&= 10 \cdot \log(V \cdot V^*) - 70.09
\end{aligned}
$$

where $10 \cdot \log(V \cdot V^*)$ is dB below carrier, since in HSPICE FFT output, the results have already been expressed in the units of dB, $10 \cdot \log(V \cdot V^*)$ is just the difference between offset and carrier frequency.

Appendix D: Procedure of Timing Jitter Simulation in Oscillators

I. Noise Free case

(1) Run noise free case simulation first, for example sample.sp

The following setup should be included in spice file at all simulations

.options ACCURATE=1 INGOLD=1 NUMDGT=10

.print tran V(output node)

output file is sample.lis

(2) Extract transient analysis data from sample.lis

On the Unix command line, run
New_d2m sample.lis

If everything is right, we should get an output file with the same name sample.lis but only transient analysis data in it.

Rename sample.lis to sample.dat

Unix command: remove sample.lis sample.dat

(3) Process noise free case data

Use MATLAB file cjabs_s6PI.m to process sample.dat

S=load(' sample.dat ')

Output file: ZPTVNI

II. Noise injected case

(1) Noise data creation

Create noise data by using cmosfjll.m (for flicker noise) and whitel_jitter.m (for white noise) if PSD values of flicker noise and white noise are given, usually the PSD values are obtained from stationary approaches described in chapter 5,6,7.

(2) HSPICE PWL Noise source

Write noise data into HSPICE PWL format, named as for example flicker.dat. Here is an example.

```
* injection of 1/f noise

Inoise 9 4 pwl(0.0000000e+00   5.4859467e-07
+  1.0000000e-10   7.2983248e-07
+  2.0000000e-10   8.6251607e-07
+  3.0000000e-10   9.6382932e-07
+  4.0000000e-10   1.0562798e-06
+  5.0000000e-10   1.1569508e-06
+  6.0000000e-10   1.2689078e-06
+  7.0000000e-10   1.3778292e-06
+  8.0000000e-10   1.4551343e-06
+  9.0000000e-10   1.4666769e-06
+  1.0000000e-09   1.3841976e-06
+  1.1000000e-09   1.1958028e-06
+  1.2000000e-09   9.1205438e-07
+  1.3000000e-09   5.6566431e-07
+  1.4000000e-09   2.0481241e-07
+  1.5000000e-09  -1.1794364e-07)
```

(3) Noise source injection

Add PWL formatted noise data into noise free case file by add

.include flicker.dat command in sample.sp file, run noise injected case simulation.

The following setup should be included in spice file at all simulations

.options ACCURATE=1 INGOLD=1 NUMDGT=10
.print tran V(output node)
output file is sample.lis

(4) Extract transient analysis data from sample.lis

In Unix command line, run

New_d2m sample.lis

If everything is right, we should get an output file with the same name sample.lis but only transient analysis data in it.

Rename sample.lis to sample.dat

Unix command: remove sample.lis sample.dat

(5) Process noise injected case data

Use MATLAB file cjabs_s6PII.m to process sample.dat

S=load(' sample.dat ')

Output file: ZPTVNN, NOISEJ

III. Post Process files

(1) File for extract transient analysis data from sample.lis (File name: New_d2m)

```
#!/usr/local/bin/perl

print "processing....$ARGV[0]\n";

# Get file name from argument list
$inFile = $ARGV[0];

unless( open(infp, $inFile) )
{
        die("\n Can not open $inFile\n");
}
$tempFile = $ARGV[0]."temp";

unless( open(outfp, ">$tempFile"))
{
        die("\n Can not open Temp File\n");
}

#Read line from infp
$line = <infp>;

$StartDataFlag =0;

while( ($line ne "") && ($StartDataFlag !=1) )
{
        if( index( $line, "transient analysis") != -1)
        {
                #find the transient analysis result, so skip 5 other lines.
                $line = <infp>;
                $line = <infp>;
                $line = <infp>;
                $line = <infp>;
                $line = <infp>;
                $line = <infp>;
                $StartDataFlag = 1;
        }
        else
        {
                $line = <infp>;
        }
```

```
}

#start to get the result

$line = <infp>;
while ( $line ne "" )
{       if( $line !~ /y/)
        {
                print outfp ($line);
        }
        else
        {
                close (infp);
                close (outfp);

                @Cmd=("mv","-f",$tempFile,$ARGV[0]);
                system(@Cmd);
                exit;
        }
        $line = <infp>;
}
```

(2) File for calculation of timing jitter-Part I (File name: cjabs_s6PI.m)

```
% Simulation of clock jitter (First Part)

clear all; close all;

format long;

% Noise-Free Case

% Load Data

S=load('sample.dat');

%S(1:7999,:)=[ ];

Vmax=max(S);

Vmin=min(S);

Vc=(Vmax(1,2)+Vmin(1,2))/2;
```

```
tI=S(1:20000,1);

VI=S(1:20000,2);

ndim=size(S);

nvj=ndim(1,1);
%nvj=15990000

for i=1:nvj

        S(i,2)=S(i,2)-Vc;

end

for i=2:nvj

        if S(i-1,1)==S(i,1);
        error(['Error i=',int2str(i)]);
        end
end

disp('Right, processing...1');


j=0;

for i=1:2

        if S(i,2)==0 & S(i+1,2)>0;
        j=j+1;
        Z(j)=S(i,1);
    elseif S(i,2)<0 & S(i+1,2)>0
        Y=[S(i,1) S(i+1,1) S(i+2,1) S(i+3,1) S(i+4,1) S(i+5,1)];
        X=[S(i,2) S(i+1,2) S(i+2,2) S(i+3,2) S(i+4,2) S(i+5,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

for i=4:nvj-2

        if S(i-1,2)==0 & S(i,2)>0;
        j=j+1;
```

```
        Z(j)=S(i-1,1);
    elseif S(i-1,2)<0 & S(i,2)>0
        Y=[S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1) S(i+2,1)];
        X=[S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2) S(i+2,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

for i=nvj-2:nvj-1

        if S(i,2)==0 & S(i+1,2)>0;
        j=j+1;
        Z(j)=S(i,1);
    elseif S(i,2)<0 & S(i+1,2)>0
        Y=[S(i-4,1) S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1)];
        X=[S(i-4,2) S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

if S(nvj,2)==0 & S(nvj-1,2)<0;
        j=j+1;
        Z(j)=S(nvj,1);
end

clear S;

ZI=Z;

PTI=diff(ZI);

PTI=PTI*1e12;

nI=length(PTI);

save ZPTVNI ZI PTI tI VI nI;
```

(3) File for calculation of timing jitter-Part II (File name: cjabs_s6PII.m)

```
% Simulation of clock jitter (Second Part)
```

```
clear all; close all;

format long;

% Noise-Injected Case

% Load Data

S=load('sample.dat');

%S(1:7999,:)=[ ];

Vmax=max(S);

Vmin=min(S);

Vc=(Vmax(1,2)+Vmin(1,2))/2;

tN=S(1:20000,1);

VN=S(1:20000,2);

ndim=size(S);

nvj=ndim(1,1);
%nvj=15990000

for i=1:nvj

        S(i,2)=S(i,2)-Vc;

end

for i=2:nvj

        if S(i-1,1)==S(i,1);
        error(['Error i=',int2str(i)]);
        end
end

disp('Right, processing...2');


j=0;
```

```
for i=1:2

        if S(i,2)==0 & S(i+1,2)>0;
        j=j+1;
        Z(j)=S(i,1);
    elseif S(i,2)<0 & S(i+1,2)>0
        Y=[S(i,1) S(i+1,1) S(i+2,1) S(i+3,1) S(i+4,1) S(i+5,1)];
        X=[S(i,2) S(i+1,2) S(i+2,2) S(i+3,2) S(i+4,2) S(i+5,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

for i=4:nvj-2

        if S(i-1,2)==0 & S(i,2)>0;
        j=j+1;
        Z(j)=S(i-1,1);
    elseif S(i-1,2)<0 & S(i,2)>0
        Y=[S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1) S(i+2,1)];
        X=[S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2) S(i+2,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

for i=nvj-2:nvj-1

        if S(i,2)==0 & S(i+1,2)>0;
        j=j+1;
        Z(j)=S(i,1);
    elseif S(i,2)<0 & S(i+1,2)>0
        Y=[S(i-4,1) S(i-3,1) S(i-2,1) S(i-1,1) S(i,1) S(i+1,1)];
        X=[S(i-4,2) S(i-3,2) S(i-2,2) S(i-1,2) S(i,2) S(i+1,2)];
        j=j+1;
        Z(j)=interp1(X,Y,0,'spline');
    end
end

if S(nvj,2)==0 & S(nvj-1,2)<0;
        j=j+1;
        Z(j)=S(nvj,1);
end

clear S;
```

```
load ZPTVNI;

% Plot clock output

figure(1);

plot(tI,VI,'r');

figure(2);

hist(PTI,64);

xlabel('psec');
title(['Total periods n=',int2str(nI)]);

% Plot clock output

figure(3);

plot(tN,VN,'r');


ZN=Z;

PTN=diff(ZN);

PTN=PTN*1e12;

nN=length(PTN);

save ZPTVNN ZN PTN tN VN nN;

figure(4);

hist(PTN,64);

xlabel('psec');
title(['Total periods n=',int2str(nN)]);

if nN>=nI;

nf=nI;
ZN=ZN(1:nf+1);
PTN=PTN(1:nf);
```

```
elseif nN<nI;
nf=nN;
ZI=ZI(1:nf+1);
PTI=PTI(1:nf);

end

deltaT=PTN-PTI;
nr=1000;
a=floor(nf/nr);

for i=1:nr-1

n=a*i;

deltaTc=deltaT(1:n);

pkpt(i)=max(deltaTc)-min(deltaTc);

absjitter(i)=abs(sum(deltaTc));

cjitter(i)=sqrt((sum(deltaTc.^2))/n);

ccjitter(i)=sqrt((sum((diff(deltaTc)).^2))/(n-1));

t(i)=ZN(n+1);

mdeltat(i)=ZN(n+1)-ZN(1);

end

i=i+1;

n=nf;

deltaTc=deltaT;

pkpt(i)=max(deltaTc)-min(deltaTc);

absjitter(i)=abs(sum(deltaTc));

cjitter(i)=sqrt((sum(deltaTc.^2))/n);

ccjitter(i)=sqrt((sum((diff(deltaTc)).^2))/(n-1));
```

```
t(i)=ZN(n+1);

mdeltat(i)=ZN(n+1)-ZN(1);

save NOISEJ;

% --- Final output plot

figure(5);

plot(mdeltat,absjitter,'rs-'); grid on;

title(' ');
xlabel('Time deltat (S)');
ylabel('Absolute Jitter (pS)');
```