AN ABSTRACT OF THE THESIS OF

Farshad Farahbakhshian for the degree of Master of Science in Electrical and Computer Engineering presented on Decemeber 10th, 2014.

Title: Dynamic Biasing for Ring Amplification

Abstract approved: _____

Un-Ku Moon

New amplifier architectures are presented using non-traditional methods of biasing. Time-based dynamic biasing and signal-based dynamic biasing are discussed in the context of new architectures. This includes a new form of ring amplification with a dynamic deadzone, allowing for a structure whose coarse path does not consume static power.

Dynamic Biasing for Ring Amplification

by

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APPROVED:

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Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

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Farshad Farahbakhshian, Author

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"In The End, Nothing Really Matters"

-Dr. Un-Ku Moon

1.1   Moore's Law

Since the beginning of Moore's observation in 1965, the semi-conductor industry has set into motion one of the most interesting laws, or perhaps self-fulfilling prophecies, in recent human history. By observing that the number of components integrated into a circuit doubled each year [3], Moore's law was born. With that prediction, the semi-conductor industry put forth a vigorous effort to ensure the trend continued. Today, Moore's law effectively means that every 18 months, the minimum transistor size will scaled down by about 30 percent. There has been great motivation for this reduction; reducing minimum transistor size has led to smaller integrated circuits (ICs), better performance, better power efficiency, more reliability [3], and more yield. While there is no telling how much longer Moore's law will continue to occur, there is a problem facing analog designers whom do not reap the benefits that the industry has become accustomed to.

Process scaling has been a pressing issue in analog design. It would appear that as minimum gate length is shrunk, digital circuits are performing better, but

analog circuits are performing worse. Regardless of this issue, the process nodes will continue to shrink as long as it provides a larger profit margin for the semiconductor industry. This leaves analog designers with an impressive challenge to either mitigate or perhaps even extinguish the problems associated with process scaling.

Scaling affects many of the performance metrics used to describe analog components in circuits. In the following subsections, process scaling's effects on gain bandwidth and output swing in the context of an amplifier will be discussed.

1.1.1   Gain

Gain is the ratio of amplification from the input of an amplifier to the output. It is useful for determining how accurate a given amplifier is and is typically measured in logarithmic units of decibels (dB). High gain can be achieved by either having high output resistance (Ro), high transconductance (gm) or by leveraging different architectures, some of which may include cascoding of transistors. Typically these variables are constant in the time domain, meaning the circuit's biasing is static. As process nodes decrease, Ro tends to decrease at a faster rate than gm increases. For this reason, the intrinsic gain of devices decreases with process node shrinkage [4, 5]. To make the problem even worse, cascoding transistors becomes a less viable option since the supply voltage also decreases with process node. This usually translates to multiple stage amplifiers which will consume more power than their single stage counter parts. The effects of process scaling on gain are shown in Fig.
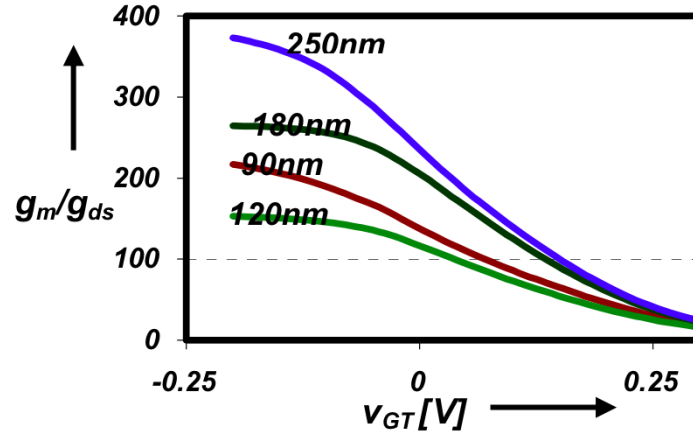
Figure 1.1: Gain versus Gate Voltage Across Various Process Nodes

1.1 [6].

$$Gain(dB) = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) dB \qquad (1.1)$$

1.1.2 Bandwidth

Bandwidth is the only variable out of the three mentioned that actually improves with process node shrinkage. This is true for both transconductance and slew rate, which both heavily influence the bandwidth of the entire system. As process nodes are reduced in size, transistors are better suited for having smaller on-resistance. The effects of process scaling on bandwidth are shown in Fig. 1.2 [6].
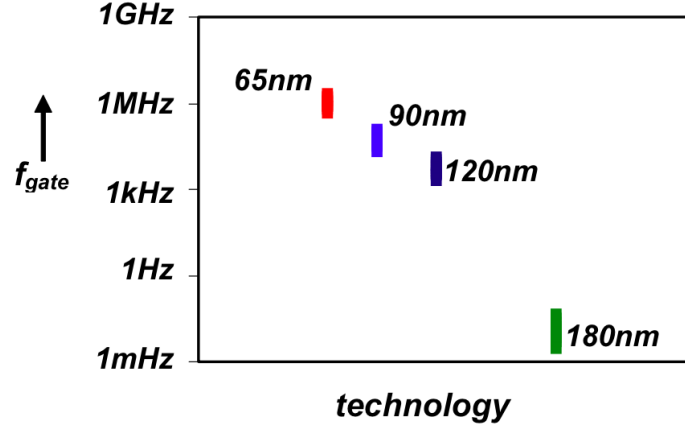
Figure 1.2: Bandwidth versus Process Node

1.1.3 Output Swing

As process node decreases to smaller minimum lengths, the voltage supply typically scales down as well. As the device decreases in size, the gate oxide thickness also decreases, requiring the voltage across all devices to decrease to maintain reliability. This means that there is less room for the output swing for the same architecture, which tends to hurt the dynamic range of the amplifier, translating to lower overall system accuracy. This trend can be shown in Fig. 1.3 [7]. Typically the design trade-off between architectures is decided on the application, however, as process nodes are decreased the number of viable design options are also decreased. Output swing is crucial for a high signal-to-noise ratio (SNR) system. SNR is defined:

$$SNR(dB) = 20 \cdot \log \left(\frac{V_{signal}}{V_{noise}} \right) dB \tag{1.2}$$

$$SNR(dB) = 20 \cdot \log\left(\frac{\Gamma \cdot V_{signal} \cdot \sqrt{C}}{\sqrt{KT}}\right) dB \qquad (1.3)$$

Which also can be defined in terms of sample capacitance sizing, C, and thermal noise K. Where Γ is a constant dependent on the feedback used in the switched capacitor environment. Currently in a 180nm process, a 1.8V supply is used. In a 65nm process, 1V is used as the supply. Assuming the same Γ and sampling capacitor size, this would translate to a 5.1 dB loss between the two systems. To compensate for the loss in SNR, the sampling capacitor can be increased. To achieve the same SNR between the two systems, the sampling capacitor size would have to be increased by 3.24 times the previous size.

1.1.4   The Path Ahead

Most designs are concerned with achieving the best possible Figure of Merit (FoM), shown in equation 1.4. With the recent surplus of Successive Approximation Register (SAR) ADCs being published in conferences such as International Solid-State Circuits Conference (ISSCC) and VLSI, it can be extrapolated that many designers are benefiting from using mostly digital architectures like SAR ADCS to achieve great performance numbers.

This is a reflection of one of the ways the analog problem is being mitigated. The overall system can reduce the total analog circuitry and rely on digital components to perform analog functions, in turn reducing the performance limits imposed by the scaling of analog components. More circuits are using digital calibration
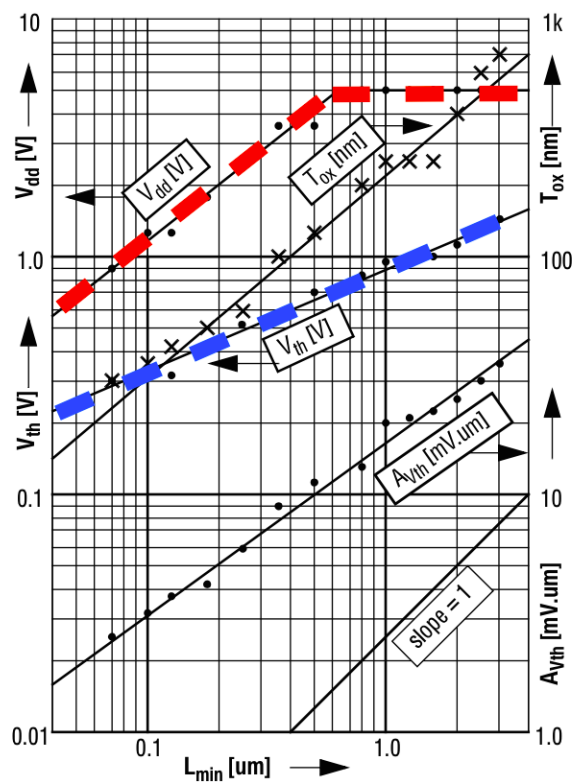
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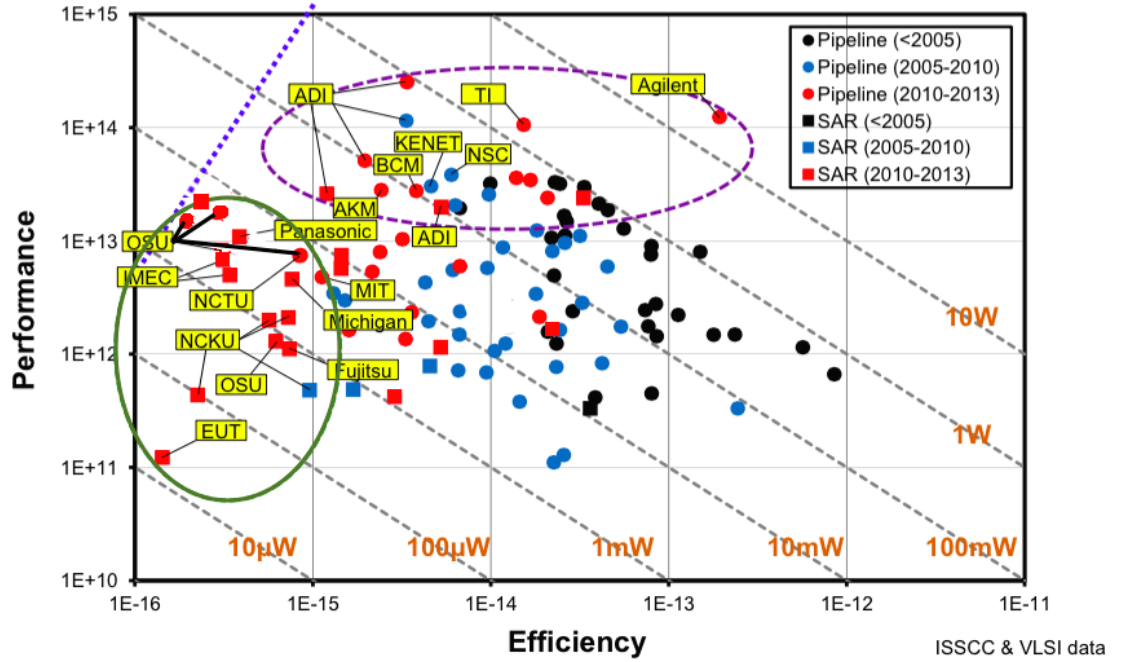
Figure 1.4: Performance versus Efficiency of Pipeline and SAR ADCs.

to fix analog errors and are taking architectures that rely on digital components to achieve high performance, rather than analog ones. However, there is another path is to fix the problems associated with analog components. Demonstrated by the pipeline ADCs that use ring amplifiers to replace traditional amplifiers, analog components can be used to achieve state of the art performance.

$$FoM = \frac{Power}{Bandwidth \cdot 2^{ENOB}} \qquad (1.4)$$

As shown in Fig. 1.4 [8], the ADCs that are capable of achieving high performance while still maintaining great efficiency are mostly SAR ADCs. Looking closely at the highest performance and best efficiency, there are two pipeline ADCS from 2010-2013. These pipeline ADCs replaced traditional amplifiers with ring amplifiers to achieve high efficiency. Analog circuitry does not have to be the culprit for low power efficiency. The rest of this thesis is dedicated to unveiling the performance enhancements used by the ring amplifier to achieve great FoM in an analog realm.

Chapter 2: Dynamic Biasing in Switched-Capacitor Systems

"Remember That There is No Such Thing as a Free Lunch."

-Dr. Karti Mayaram

2.0.5   Introduction

Traditional amplifiers used in switched-capacitor based systems are typically continuous-time amplifiers. Due to it's continuous-time nature, the specifications of the amplifier, such as gain, bandwidth and power, are static. This begs the question of what possible performance enhancements can be made by catering to a switched-capacitor environment. As demonstrated by the robust performance of the ring-amplifier [2], dynamic systems in switched-capacitor environments can achieve very high performance in recent pipeline ADCs while providing a scalable solution. In this chapter, dynamic-biasing is presented as a means of designing a circuit that have different functions in different points in time, to boost performance. This results in little cost in power in switched-capacitor circuits.
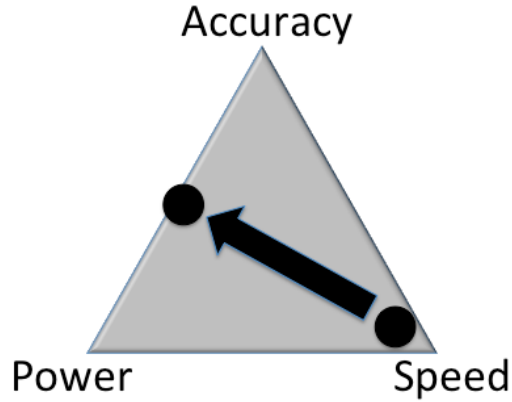
Figure 2.1: Triangle of Design Trade-offs

2.1 Dynamic Biasing

Dynamic biasing creates a circuit whose gain and bandwidth are changing over the course of the amplification phase to only consume power when it is neccesary to. This means that accuracy, power and speed are no longer static variables but rather dynamic variables that change over time. This behaviour can be conceptualized by the triangle of design trade-offs shown in Fig. 2.1. The triangle represents the designers choice to cater a design's biasing to one that emphasizes a certain amount of speed performance, accuracy performance or power performance. A design that is both fast and accurate will likely consume more power than a design that is accurate but slow. This conceptualization begs a question; in a switched-capacitor system, is it necessary to have a fast system towards the end of the amplification period? As it turns out, the answer is no [1]. As depicted in 2.1, the system begins in a speed emphasized state and ends in a accuracy emphasized state, allowing the

VDD

Vin

Vout

Φ

Φ

GND
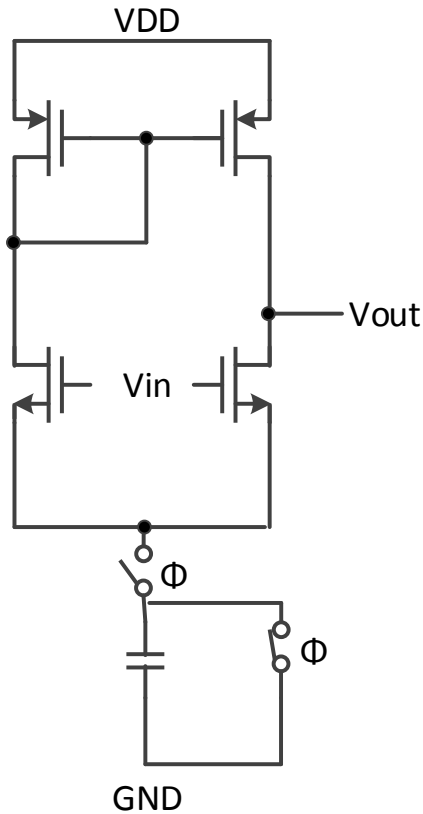
Figure 2.2: Original Dynamic Amplifier Proposed in [1]

system to reap the benefits of dynamic biasing.

Dynamically biased circuits were introduced in [9, 1]. The general architecture typically incorporates a capacitor as a means of providing temporary current to boost slewing and bandwidth in the beginning of the amplification phase. One of the amplifiers proposed by [1] is shown in Fig. 2.2. The amplifier begins in a high-bandwidth state and finishes in a high-gain state. While this new method of

design has great FoM benefits, it does have a new variable of design, time, which the designer has to take into account at which point in time the circuit transitions from a high-bandwidth state to a high-gain state. Dynamic biasing can be achieved in two ways, which are discussed in the following subsections.

2.1.1   Time-Based Dynamic Biasing

Time-based biasing enables the transition from point A (high-bandwidth state) to point B (high-gain, low power state), shown Fig. 2.3, over the course of a specific time period. Depending on the architecture, the behavior of the sweeping from A to B usually occurs in a resistor-capacitor (RC) charging to a voltage or a transistor charging a capacitor. The advantage of time-based biasing is that it allows the designers to allocate different corners of the triangle of design depending on the application. The architecture in [1], however, is susceptible to process variation since it completely depends on the absolute value of the capacitor. An error in the absolute value of the capacitor may cause the system to spend too little or too much time in any corner of the triangle. Building upon the dynamic amplifier from [1], a modified form of the dynamic amplifier is proposed in Fig. 2.4.

The advantage of the architecture shown in Fig. 2.4 is that it is less susceptible to process variation and is easier to design for. By having a transistor in parallel with the capacitor, the transistor is able to fix any errors caused by process variation in the capacitor. The designer would design the architecture based on the gain specification without the capacitor. Then, to boost bandwidth, the capacitor
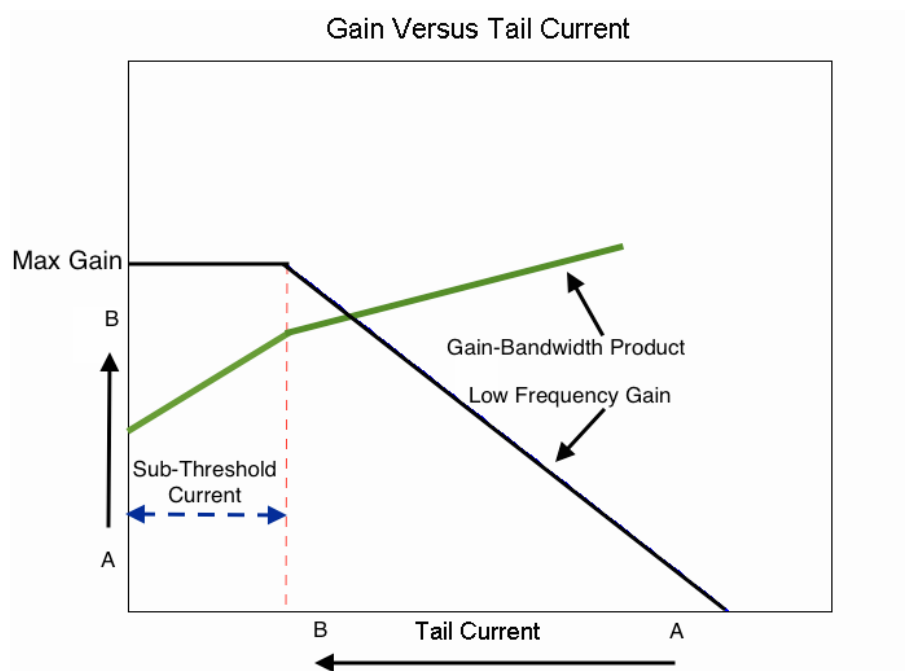
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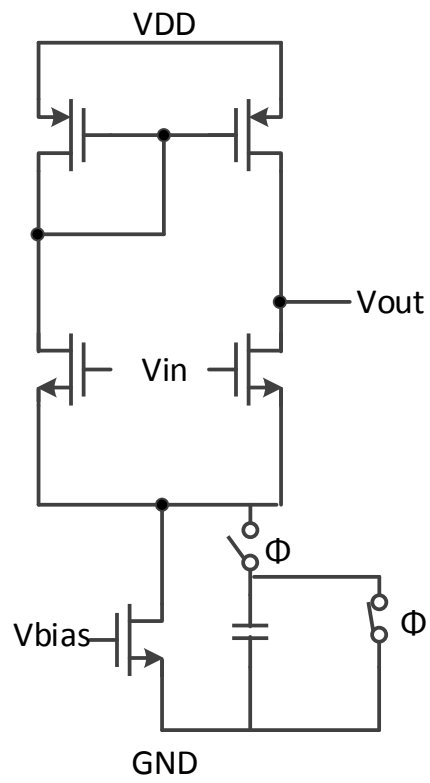
Figure 2.4: Proposed Dynamically Biased CMOS Amplifier
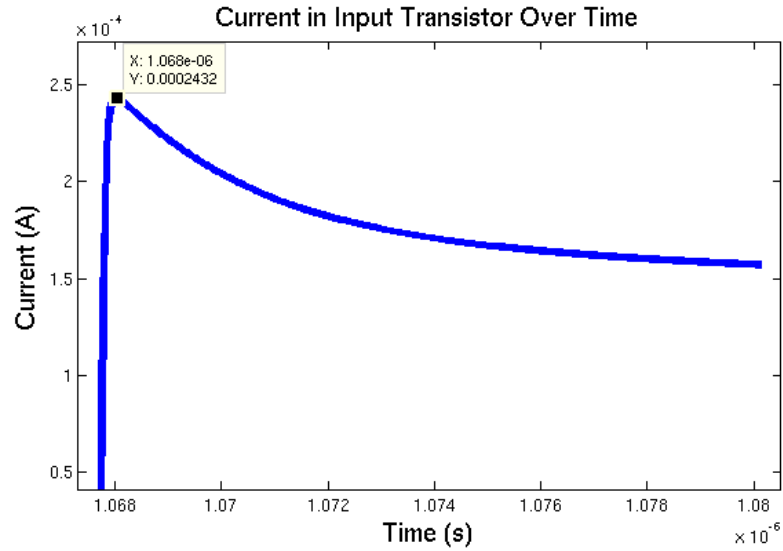
Figure 2.5: Current vs Time during Amplification Phase of Circuit shown in Fig. 2.4

is considered in the design to boost current in the beginning of the phase.

When Φ (the sample phase) is turned on, the capacitor is discharged and grounded. During the amplification phase, the empty capacitor is connected to the circuit. This capacitor temporarily increases the current through the system until the capacitor is charged. During this period, the input pair transistors experience increased transconductance and current, as shown in equation 2.1 and Fig. 2.5. Due to equation 2.1's dependence on current, transconductance is no longer static and is changing porportionally to the square root of the current. The current is dependent on the source voltage of the input pair and the capacitor used, which is shown in equations 2.2 and 2.3.

$$gm = \sqrt{2 \cdot Id \cdot UnCox \cdot \frac{W}{L}} \tag{2.1}$$

Table 2.1: Comparison of Performance for Circuit in Fig. 2.4

Cap. Size (pF)	Tail (um)	Gain (dB)	Settle Time (ns)	Power (uW)
No Cap.	1/0.5	21	15	226
5	1/0.5	38	15	650
No Cap.*	5/0.5	38	15	1000

$$Id = \frac{UnCox}{2} \cdot \frac{W}{L} \cdot (Vg - Vs - Vth)^2 \qquad (2.2)$$

Where Vs is changing over the amplification period and can be modeled by:

$$Vs \propto 1 - e^{-t/RC} \qquad (2.3)$$

Where R is the effective resistance of the transistor.

Shown in Table 2.1, the time-biased dynamic biasing can be used to save as much as 35 percent of the power used in an amplifier without hindering performance in speed or accuracy.

2.1.2   Signal-Based Dynamic Biasing

Another form of dynamic biasing is signal-based dynamic biasing. The best example of signal-based dynamic biasing is the ring amplifier [10]. Shown in Fig. 2.6, the ring amplifier performs as two different circuits depending on the proper-

ties of the signal being amplified. Unlike the time-based dynamic biasing scheme, the signal-based variant works independently of time variables. However, it incorporates similar behavior; it begins in a high-bandwidth state and ends in a low-bandwidth state.

2.2 Ring Amplification

The ring amplifier can be understood by viewing the capacitors as simple voltage offsets (known as the deadzone voltage). The capacitor's voltage values are dependent on the voltage embedded in the capacitors. These offsets effectively bias the output transistors into sub-threshold. By biasing the output transistors such that they are almost turned off , the ring amplifier manages to achieve very high gain (while maintaining great power efficiency). However, an amplifier whose output stage is almost shut off will not provide strong transconductance or slewing capabilities. This is where signal dependency allows the ring amplifier to achieve high slewing and bandwidth; the capacitor allows high-frequency signals through. The offsets allow the output stage to be turned off in steady state. Fig. 2.8 shows the average supply current decreases as the deadzone is increased, emphasizing the advantage of embedding a deadzone voltage to save power.

The capacitors effectively bias the output transistors for high gain for low-amplitude feedback signals (such as when the amplifier is close to it's target output voltage), but also allow high-amplitude feedback signals to dynamically bias the output for more current and speed. Initially while slewing, the feedback signal
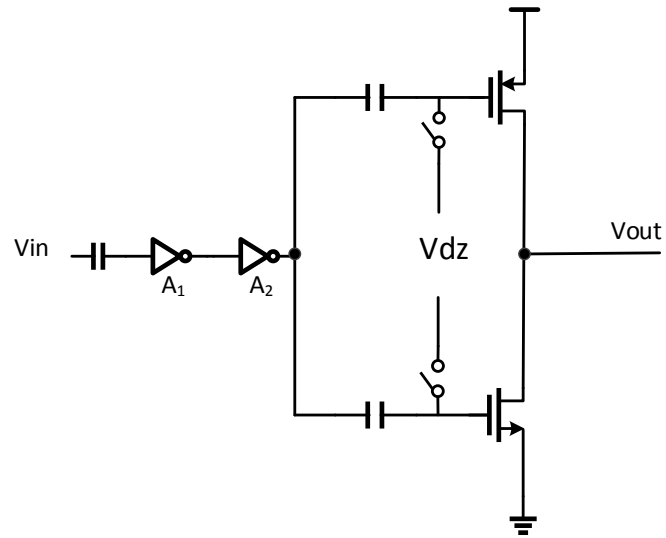
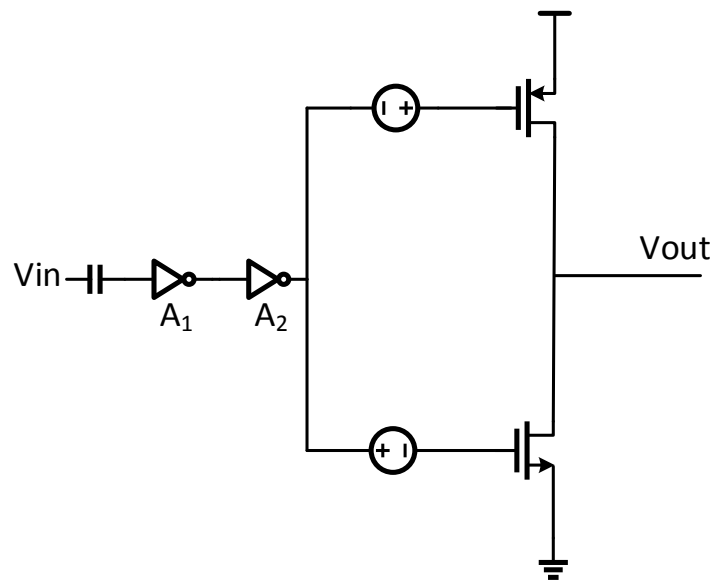Figure 2.6: Ring Amplifier Schematic

Figure 2.7: Ring Amplifier Schematic with Simple Offsets Representing Capacitor's Function

Supply Current vs Deadzone

Supply Current (uA)

Deadzone Voltage (V)
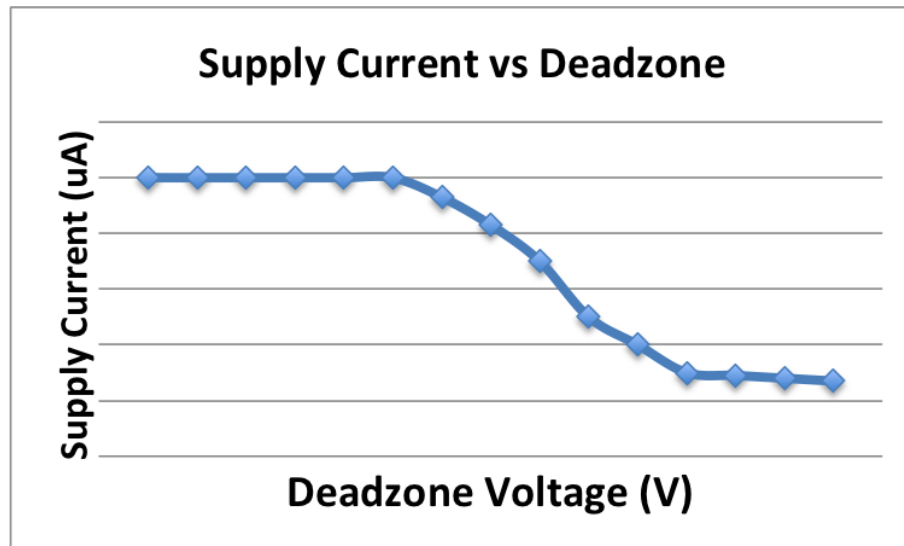
Figure 2.8: Supply Current versus Deadzone Showing Output Turning Off

is high in amplitude and also is composed of high-frequency components, which allows the system to act like three cascaded inverters (bypassing the capacitors) and simply approaching the desired amplified signal. As the output stage gets closer to the final target voltage, the feedback signal amplitude decreases as does the high frequency components of the signal. This slowly turns the output off, reaching steady-state and allowing the system to achieve a high-gain, power efficient state.

2.2.1 Slew State

During the initial amplification phase, the capacitors are effectively bypassed allowing for the ring amplifier to behave like a oscillator whose output is fully on and approaching the target output. This allows the system to efficiently slew, and would otherwise continue to oscillate if it weren't for the offsets embedded in the
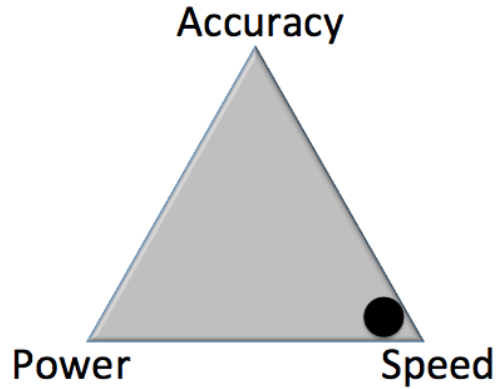
Figure 2.9: Interal Biasing during Slewing State of Ring Amplifier

capacitors prior to the output stage. In the context of the triangle of design trade offs, the signal is essentially biasing the system to operate in a high speed state, as shown in Fig. 2.9. During this state, the ring amplifier behaves similarily to a zero crossing based circuit [11, 12]. This can be attributed to the fact that the ring amplifier behaves like push and pull current sources.

2.2.2   Stabilization State

After the ring amplifier output has approached its target value, it will continue to temporarily oscillate around the target value depending on the gain of the system and the embedded deadzone. This state is effectively the transition state, which can be depicted in Fig. 2.10. As the system provides negative feedback to itself, it eventually reaches steady state.
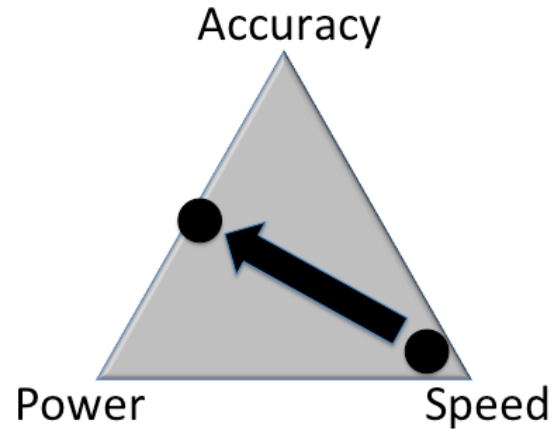
Figure 2.10: Interal Biasing during Stabilization State of Ring Amplifier

2.2.3 Steady State

Once steady state is achieved, the system can turn off its output through the biasing mechanism provided by the deadzone voltage, saving power while increasing the gain. Since the system is very close to its target value, high bandwidth is no longer needed and thus the system slowly turns off its output to transition into the high gain state. The system will continue to approach the final value until the amplification phase is over. This state is depicted in Fig. 2.11, where the output transistor are close to being off, leading to high gain and low power consumption.

2.2.4 Advantages

The main advantage of the ring amplifier is the ability to consume power only when it is necessary. Power consumption is relatively high when the ring amplifier

Figure 2.11: Interal Biasing during Steady State of Ring Amplifier

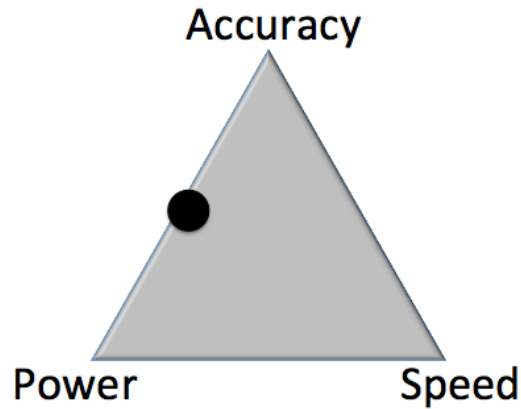is in the slewing state. For a given amplification period, this could be as low as 10% of the total amplification period. This means that up to 90% of the time, the ring amplifier can be operating in a low power state without any sacrifices made to bandwidth or gain. From an architectural perspective, the ring amplifier only has a PMOS and NMOS at the output; the ring amplifier is able to provide rail-to-rail performance. Comparing the signal-based biasing used by the ring amplifier to time-based biasing such as the one shown in Fig. 2.4, there is a clear advantage to the ring amplifier. The ring-amplifier, when biased correctly, will optimize its efficiency for a given signal and cater to the requirements of the signal, regardless of output voltage amplitude. The time-based variant will instead always have the same dynamic biasing behaviour regardless of the signal seen at the input, leading to situations with non-optimal design points.

2.2.5   Requirements for Performance Enhancement

In order to fully utilize the performance enhancements achieved via signal-based biasing of the ring amplifier, the output stage must be very close to the cut-off region. Without this requirement, the output stage will continue to be on, consuming power and also lowering the gain of the output, which is the stage with the highest gain. Due to this requirement, it is ideal to embed the deadzone voltage prior to the last stage, rather than the 2nd stage to have better control of the deadzone voltage. If the deadzone is too large, however, the feedback signal might not have a large enough amplitude to bias the output into a high slew state. These concerns must be addressed to properly design a fully functionally ring amplifier.
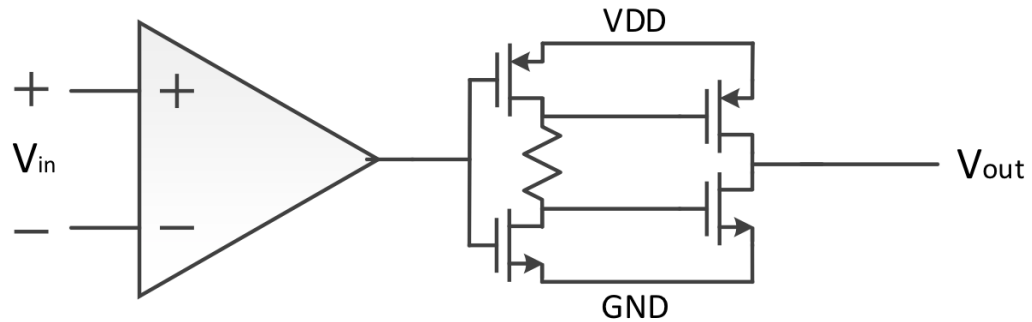
Figure 2.12: Self-Biasing Ring Amplifier

2.2.6   Self-Biased Ring Amplifier

One disadvantage of the ring amplifier presented is the need to have a relatively accurate deadzone, usually implemented with an off-chip reference. The work in [13] provides a novel solution to fix this problem. By using a resistor to generate a deadzone voltage in the second stage, a self-biasing scheme is presented and is capable of more efficiently slewing and settling for a given voltage by using a dynamic biasing scheme. The schematic is shown in Fig. 2.12. The circuit uses the resistor to generate a deadzone voltage dependent on the size of the resistor used; the larger the resistor used, the larger the deadzone voltage will be.

Chapter 3: Coarse and Fine Ring Amplifier

"Work With What You Got"

-Dr. Karti Mayaram

3.1 Introduction

Ring amplification has allowed pipeline ADCs to achieve the best FoM in recent years. The increase in performance in ring amplifiers has been a result of incorporating some form of coarse-fine architecture where separate paths are used for slewing and high gain [10, 14]. A ring amplifier designed for high accuracy, on the order of 70dB or above, may have problems with slewing. This is mainly due to the output needing to be biased into sub-threshold in order to achieve high gain. For this reason, a coarse path can be very helpful in decoupling gain from slew rate. A ring amplifier aiming for high gain, low power and high bandwidth is significantly harder to design than one that only aims to achieve two functions per path. In the case of [2], the fine path is responsible for maintaining low power while achieving high gain and the coarse path is responsible for maintaining low power while achieving high bandwidth.

3.2 Structure Overview

Various techniques have been used to mitigate the problems associated with scaling. These approaches include techniques such as Correlated Level Shifting (CLS) and Split-CLS [15, 16]. These methods allow for high gain circuits, such as a largely cascoded operational amplifier without rail-to-rail performance to achieve great rail-to-rail performance. However, these approaches require an extra amplification period and therefore are slow compared to their non-CLS counterparts. In Split-CLS, different amplifiers are used to slew and achieve fine amplification. During the first period, a low accuracy op-amp is used to slew towards the correct voltage. Then, during the next period, the fine amplifier fixes any mistakes made by the previous. Having a dual approach makes sense by alleviating the design requirements per path. However, it would be ideal to not have to sacrifice speed or power to achieve high gain and rail-to-rail performance.

Having a coarse path allows for a similar benefit to Split-CLS, without the time delay needed for another amplification period. It has a coarse path in area, as opposed to in time. For this reason, [2] uses the coarse and fine architecture used in Fig. 3.1. The structure uses the coarse path as a means to slew towards the correct amplified voltage but also provide pseudo common-mode feedback. This leaves the fine path to fix any error made by the coarse path, allowing it to be a single-ended solution with low slew rate. The coarse path turns off when it reaches coarse voltage. The fine path then corrects any errors made by the coarse path, finishing with an accuracy over 75dB. It should be observed that initially, both the

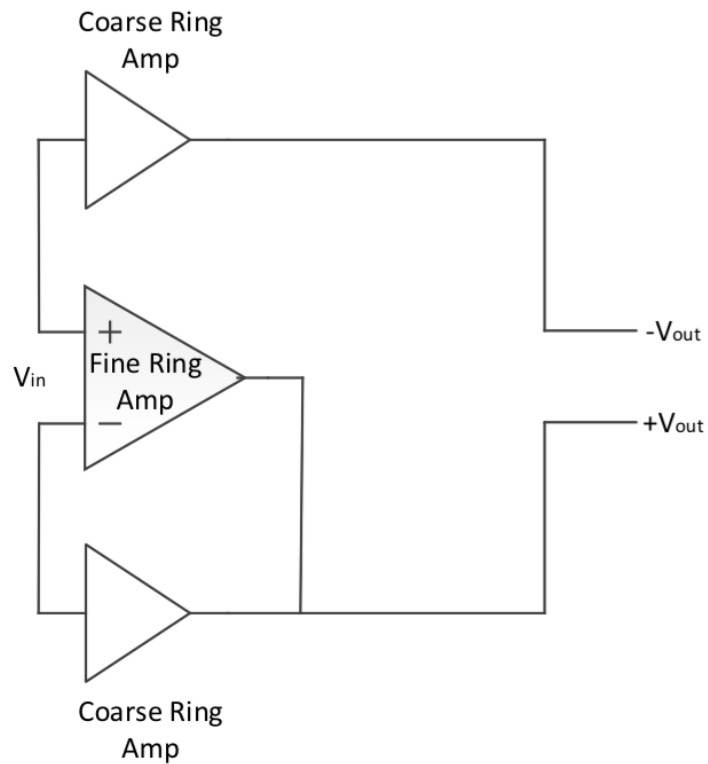Figure 3.1: Architecture used in the Ring-Amp Only Pipeline ADC from [2]

fine and coarse path are on.

3.3 Dynamic Deadzone Coarse Ring Amplifier

3.3.1 Introduction

Perhaps the largest disadvantage for coarse amplification is the extra power needed for additional components. [2] uses two ring amplifiers to provide coarse amplification, which is ideal for increasing the slew rate of the system, however, it adds an

additional two power consuming amplifiers consisting of sixteen transistors total [2]. Aside from the output stages of the two amplifiers, all other stages consume static power. By providing a structure whose internal stages do not consume static power, a new form of ring amplification can be used to further improve efficiency. In the following section, a new form of ring amplification is proposed.

3.3.2   Structure

The proposed amplifier is shown in Fig. 3.2. The dynamic deadzone ring amplifier no longer has a static deadzone. It's deadzone is generated automatically by the current provided by the 2nd stage inverter. Initially, the system has no deadzone allowing the output transistors to be fully on. As the capacitor accumulates charge and increases in voltage, it generates an increasing deadzone which eventually turns off the output. This behaviour can be shown in Fig. 3.3. The structure no longer uses static current in the second stage due to the capacitor eventually becoming a open circuit.

Table 3.1: Current Savings Among Different Capacitor Sizes

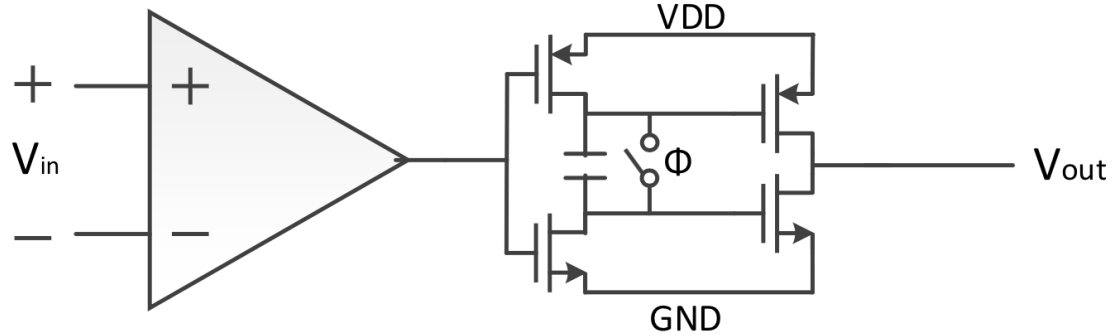| Capacitor Size (fF)	Avg. Current (uA)
No Cap. (Short)	11
150	8
100	6.9
50	3.5

Figure 3.2: Proposed Dynamic Deadzone Ring Amplifier

3.3.3   Advantages

The advtantage of the dynamic deadzone amplifier is it's ability to allow an architecture to have coarse amplification for no static power cost which translates to low power consumption. The disadvantage of this structure is that is does not provide high gain due to its more or less unpredictable deadzone. The coarse amplifier used in [2] is essentially a ring amplifier capable of achieving 10 ENOB, however, it uses additional static current in the second stage. The dynamic deadzone ring amplifier does not consume static power in the second or third stage. As shown in Fig. 3.5, the structure is capable of achieving about 7 ENOB. The amount of power saved is dependent on the capacitor size used, as shown in Table 3.1. The voltage deadzone increasing over time can be observed in Fig. 3.3. As the deadzone increases over the time, the output turns off and the current in the second stage will approach zero amps, as shown in Fig. 3.4. The dynamic ring amplifier is ideal for coarse amplification as it provides slewing virtually for free.
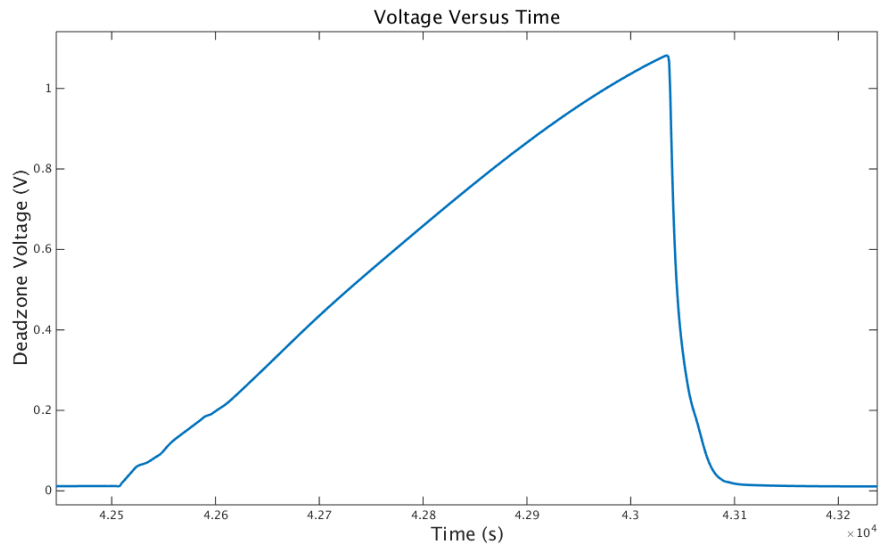
Figure 3.3: Deadzone versus Time in Dynamic Deadzone Ring Amplifier during Amplification Period
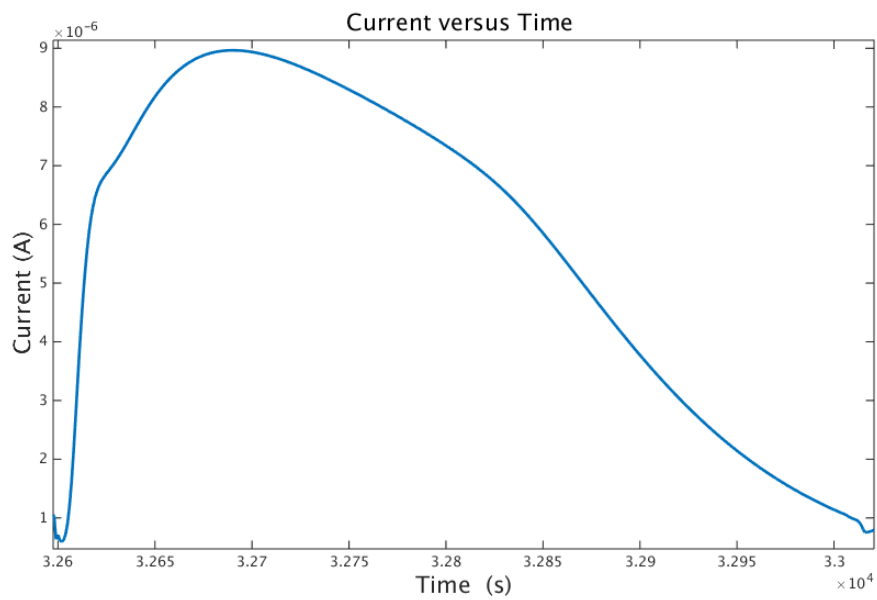

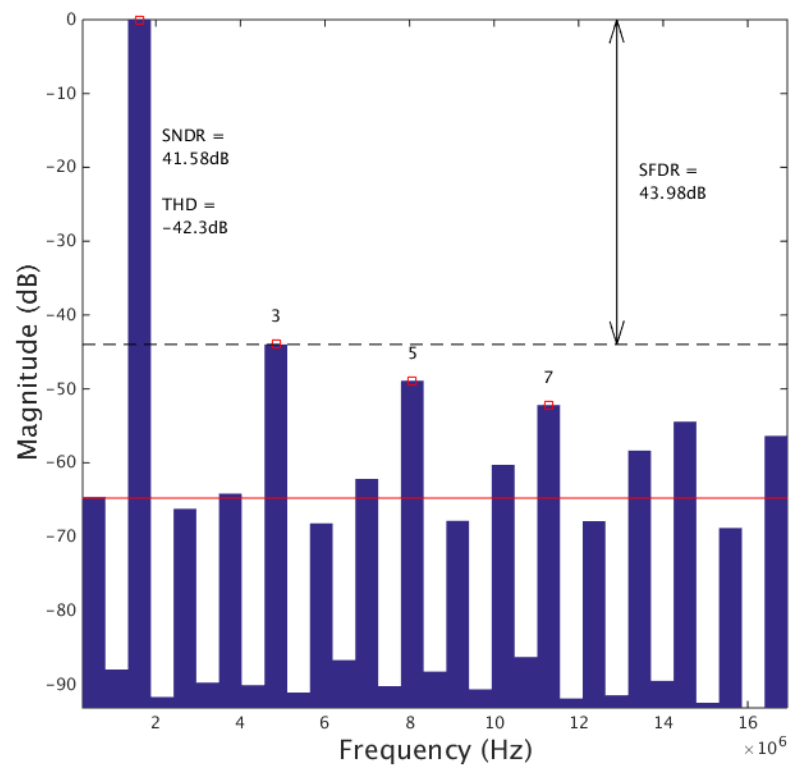Figure 3.4: Current in Second Stage of Dynamic Deadzone Ring Amplifier

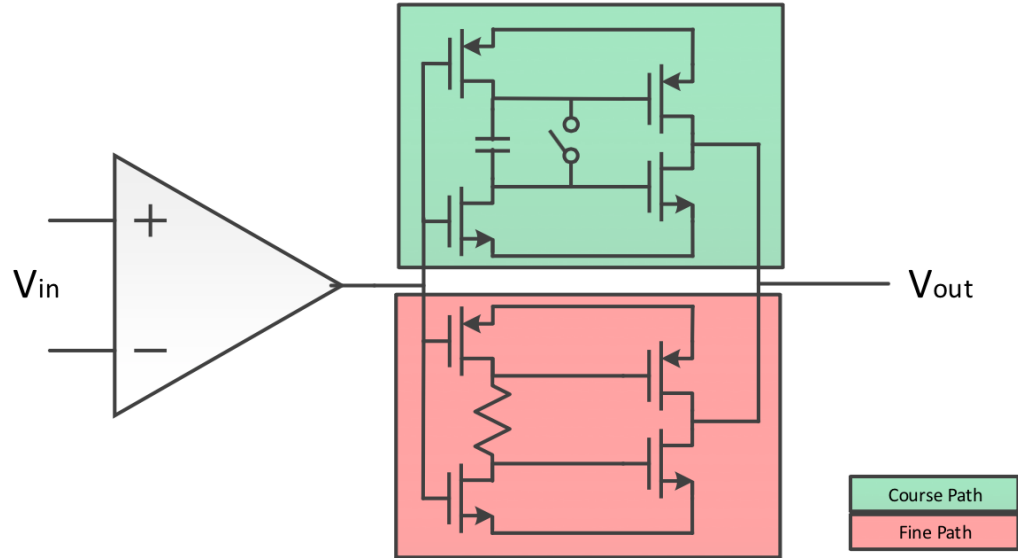Figure 3.5: FFT Output Spectrum of Dynamic Deadzone Ring Amplifier

Figure 3.6: Proposed Coarse and Fine Ring Amplifier

3.4 Architecture

By combining the proposed dynamic deadzone ring amplifier with the resistor based ring amplifier structure provided by [13], a new high accuracy amplifier can be implemented. This new architecture no longer needs external pins for deadzone control, as the new system has self-biased deadzones in both the coarse path and the fine path. The proposed architecture is shown in Fig. 3.6. The new architecture has a shared first stage, which enables the coarse path to consume only dynamic power. Compared to [2], the architecture is fully differential and it also is fully self-biased. Compared to the previous self-biasing scheme from [13], the new architecture achieves a better THD performance.

The fine path enables the system to achieve high gain without consuming high

power and maintains rail-to-rail performance due to its simple output stage. The coarse path enables high bandwidth through its efficient slewing capabilities and only consumes dynamic power. The overall system effectively achieves a low power, high bandwidth and high gain design which would otherwise not be possible without dynamic biasing. This architecture is capable of achieving over 85dB THD, shown in Fig. 3.7

3.5   Results

The proposed amplifier structure is capable of achieving over 85dB THD performance. The current consumption of the amplifier and each stage is shown in table 3.2. The capacitor based ring amplifier virtually adds no static power to achieve the coarse amplification. In fact, over 90 percent of the power consumption of the architecture is consumed by the first stage. The benefit of the coarse amplifier can be evidenced by the output spectrum of a single resistor biased ring amplifier whose output devices have been increased to accommodate for the slewing required to settle in time, shown in Fig. 3.8. The structure no longer has a coarse path and can only achieve THD on the order of 60dB. The self-biased ring amplifier with larger output devices does not have enough output resistance to achieve accuracies above 70dB.
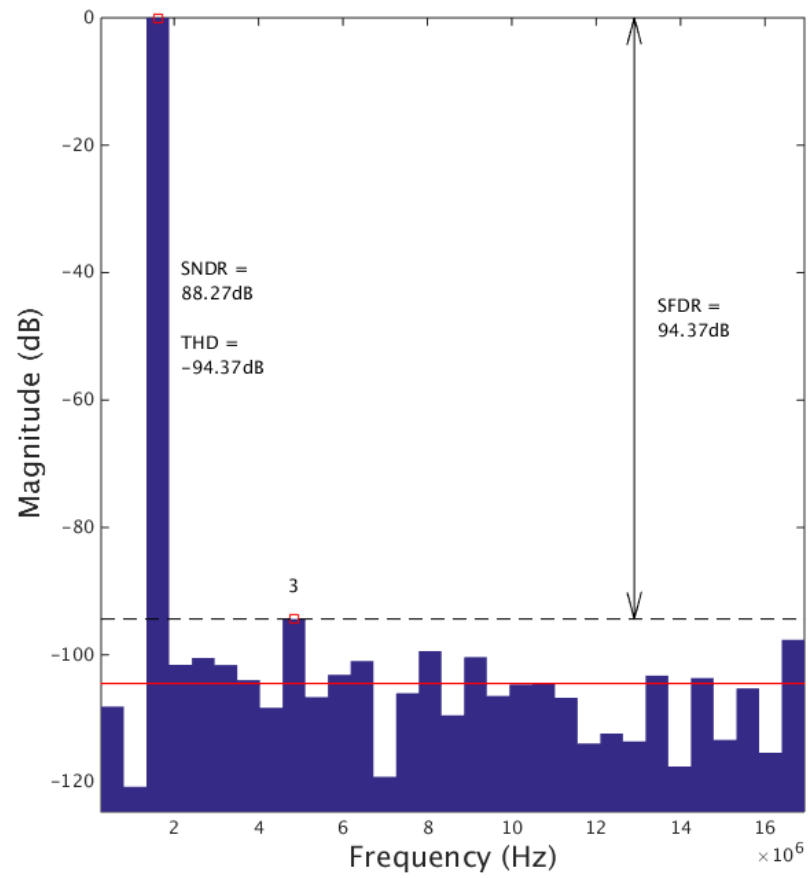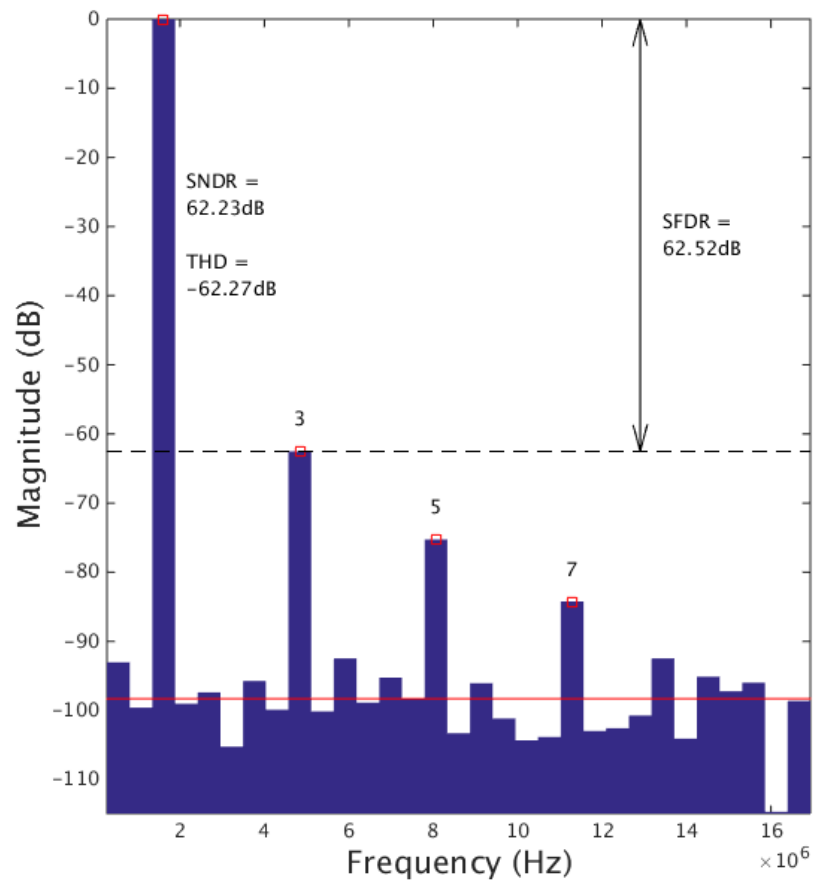
Figure 3.7: FFT Output Spectrum of Proposed Architecture

Figure 3.8: FFT Output Spectrum of Single Resistor Based Ring Amplifier

Table 3.2: Current Consumption Per Stage

Stage	Avg. Current (uA)
Stage 1	500
Stage 2 Coarse	8.7
Stage 2 Fine	20
Stage 3 Coarse	1.1
Stage 3 Fine	0.6
Total	530.4

Chapter 4: Conclusion

"Death Is The Amplifier Of Life"

-Roger Traylor

4.1   The Benefits of Dynamic Biasing

Dynamic biasing has enabled designers with a new dimension of design to push the limits of analog performance. By providing a biasing system that changes over time, a system can cater to gain and bandwidth without drastically increasing power consumption. Dynamic biasing has started to reap benefits in the biomedical applications, such as the design proposed by [17].

4.2   Proposed Research in Dynamic Biasing

Looking forward, there is still much to be researched in dynamic biasing. The immediate research topic is leveraging dynamic biasing's affect on noise. As suggested by [18], turning off the output in a feedback system actually has benefits for noise reduction. This would imply that ring amplifiers can further reduce power consumption by leveraging the noise benefits from turning off the output. Using work from this thesis, a possible leveraging point would be a time-based dynami-

cally biased first stage to reduce the noise in the first stage, which is the dominant noise source.

4.3   The Future of Dynamic Biasing

Perhaps the biggest challenge in dynamic biasing is the industry's adoption of it. The semi-conductor industry is more concerned with yield rather than a prototype chip achieving great performance numbers. For this reason, self-biasing structures are more attractive than manually biased deadzones, due to its hands-off nature. The remaining issue would be process variation's effects on the performance of time-based and signal-based dynamic biasing schemes. With that said, dynamic biasing may be what analog circuits have needed to keep up with the constant scaling in the semi-conductor industry. No longer will the analog blocks be the limitation in performance.

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