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Title: A Survey on Continuous-Time ΔΣ Modulators---Theory, Designs and Implementations

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Recently, delta-sigma modulation has become a widely applied technique for high-performance analog-to-digital conversion of narrow-band signals. Most of the early designs used discrete-time structure for good accuracy and good linearity. The transfer functions are independent of the clock frequency. However, high unity-gain bandwidths of the opamps are required to satisfy the settling accuracy required in the discrete-time designs. Continuous-time structure can potentially achieve higher clock frequency with less power consumption. the anti-aliasing filter can also be eliminated due to the anti-aliasing property of CT ΔΣ modulators. On the other hand, CT ΔΣ ADC have their own problems, such as jitter sensitivity and excess loop delay.

In this thesis, the state-of-the-art of CT ΔΣ modulator is reviewed. The problems in the design of CT ΔΣ ADCs are analyzed and solutions to them are described. The theory, design and implementations of CT ΔΣ modulator will also be reviewed.

A Survey on Continuous-Time $\Delta\Sigma$ Modulators

---Theory, Design, and Implementation

by

Xiaoran Gao

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1 INTRODUCTION

1.1 Motivation

Delta-sigma (ΔΣ) data converters have been developed since the 1960's. Nowadays it is one of the most popular architectures used in high-performance analog-to-digital and digital-to-analog converters, especially in high resolution and medium-to-low speed applications. By using oversampling and noise shaping, the stringent demand on analog circuit imperfection (matching, *etc.*) is greatly relaxed.

ΔΣ ADCs can be divided into two categories: discrete-time (DT) or continuous-time (CT) ΔΣ ADCs. Most of the early designs used DT structure for good accuracy and good linearity. In DT designs, the transfer functions are independent of the clock frequency. However, high unity-gain bandwidths of the opamps are required to satisfy the settling accuracy required in the DT designs.

CT ΔΣ ADCs can potentially achieve higher clock frequency with less power consumption. The anti-aliasing filter can also be eliminated due to the anti-aliasing property of CT ΔΣ ADCs. On the other hand, CT ΔΣ A/D converters have their own problems, such as jitter sensitivity and excess loop delay.

In this thesis, the state-of-the-art of CT ΔΣ ADCs is reviewed. The problems in the design of CT ΔΣ ADCs are analyzed and solutions to them are reviewed.

1.2 Thesis Organization

The thesis is organized as follows. Section 2 provides some background information on CT $\Delta\Sigma$ modulators. Section 3 gives an introduction of the architecture of the CT $\Delta\Sigma$ A/D converters. Section 4 gives a review of the design considerations in the CT $\Delta\Sigma$ A/D converters. Section 5 reviews several recent implementations of CT $\Delta\Sigma$ modulators. Finally, Section 6 concludes the thesis.

2. OVERVIEW OF OVERSAMPLING ΔΣ ADC

This section provides an introduction to analog-to-digital converters (A/D converter or ADC). The concepts of quantization, oversampling and noise shaping are introduced. The performance and stability of ΔΣ modulators are reviewed. The discrete-time and continuous-time ΔΣ modulators are compared.

2.1 Sampling and quantization

The conversion of the analog signal to the digital signal can be divided into two steps: the sampling in time and the quantization in amplitude. A typical block diagram of a ΔΣ modulator is given in Fig 2.1.

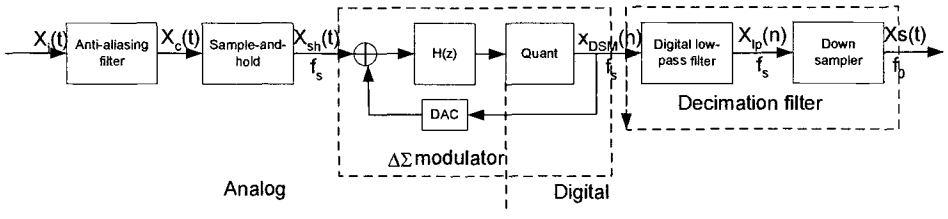


Fig. 2.1 Block diagram of an oversampling A/D converter

If the signal $x(t)$ is band-limited to $|f| \leq f_B$, where f_B is the signal bandwidth, the sampling process is reversible as long as the Nyquist theorem is fulfilled, *i.e.*, $f_S \geq 2f_B = f_N$. Since the analog-to-digital conversion usually takes several clock periods of time, it is often necessary to hold the input signal constant until the conversion is complete. This is accomplished by the sample-and-hold (S/H) circuit. To prevent aliasing, an anti-aliasing filter (AAF) is often placed before the S/H circuit.

The quantization converts the signal with continuous amplitude into a discrete number. For B-bit resolution, the continuous amplitude is rounded off to the

closest level of a total of 2^B levels. The quantization level is defined as $\Delta = \frac{FS}{2^B - 1}$, where FS is the full-scale input of the quantizer. As long as a quantizer is not overloaded, the quantization error, *i.e.* the difference between input and output, is limited to $\frac{\Delta}{2}$. Since quantization is a non-reversible process, one of the important objectives in A/D converter design is to reduce this error.

Under many circumstances, the quantization noise can be treated as white noise and its power and spectral density is

$$P_q = \sigma_q^2 = \int_{-\Delta/2}^{\Delta/2} q^2 P(q) dq = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \qquad S_q = \frac{\Delta^2}{12} \frac{1}{f_S} \tag{1}$$

For a B-bit A/D converter, the signal to quantization noise ratio (SQNR) is defined as

$$SQNR = 10\log\frac{P_x}{P_e} = 10\log\left(\frac{\frac{(2^{B-1})^2 \Delta^2}{2}}{\frac{\Delta^2}{12}}\right) = 10\log\left(\frac{3}{2} 2^{2B}\right) \approx 6.02B + 1.76dB \tag{2}$$

The SQNR is one of the most important parameters of the A/D converter.

2.2 Oversampling and Noise Shaping

The main idea of oversampling ADCs is that by sampling at a much higher rate than the Nyquist frequency and filtering the out-of-band noise components, the quantization noise left in the signal band can be reduce.

When we analyze a modulator, we will set a linear model shown in Fig. 2.2.

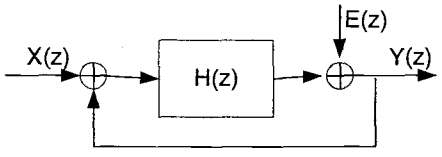


Fig. 2.2 A modulator's linear model

We can write the output signal as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function. Below are the results of the output of modulator in the z-transform domain

$$Y(z) = \frac{H(z)}{1-H(z)}X(z) + \frac{1}{1-H(z)}E(z) = STF(z)\cdot X(z) + NTF(z)\cdot E(z) \tag{3}$$

where

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \tag{4}$$

and

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{5}$$

where STF is the signal transfer function and NTF is the noise transfer function. The main feature of a $\Delta\Sigma$ modulator is the different transfer behavior for the quantization error signal and the input signal.

For the first order $\Delta\Sigma$ modulator, as shown Fig. 2.3, we have

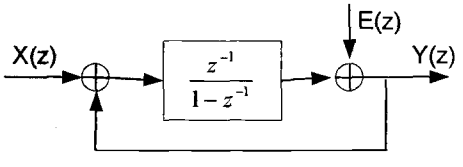


Fig. 2.3 A the one-order $\Delta\Sigma$ modulator model

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z) \tag{6}$$

and

$$STF(z) = \frac{Y(z)}{X(z)} = z^{-1}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = 1 - z^{-1}$$

This means that the STF is a one clock period delay and the NTF of the ΔΣ modulator is a high-pass filter function, in which the high-pass characteristic is called "noise-shaping". In time domain, (6) may become

$$y[n] = x[n-1] + e[n] - e[n-1] \tag{7}$$

Therefore, the digital output contains a delayed analog input signal x, and a differentiated version of the quantization error e. Hence, the amplification of in-band noise and distortion at the output does not happen. Usually, the in-band quantization noise is strongly suppressed by a high gain of loop filter in the signal band. This process is called noise shaping.

If $OSR >> 1$, the in-band quantization noise power (IBN) can be expressed as

$$IBN = \sigma_{q\_dsm}^2 = \frac{\sigma_q^2}{f_{so}} \int_{-f_s/2}^{f_s/2} |1 - e^{-j2\pi f / f_{os}}|^2 \, df = \frac{\sigma_q^2 \times \pi^2}{3 \times OSR^3} \tag{8}$$

and its SQNR is

$$SQNR\ (dB) = 10 \log\left(\frac{P_x}{P_q \times \frac{\pi^2}{3OSR^3}}\right)$$

$$\approx 6.02B + 1.76 + 30 \log(OSR) - 10 \log\frac{\pi^2}{3}, \left(f \in [-\frac{f_s}{2}, \frac{f_s}{2}]\right) \tag{9}$$

As can be seen from the above equation, we gains around 9 dB, or 1.5 bit in SQNR for the doubling of the OSR.

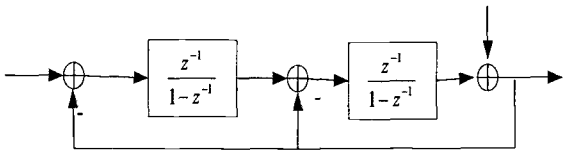


Fig. 2.4 The second order $\Delta\Sigma$ modulator

Similarly, for the second-order $\Delta\Sigma$ modulator shown in Fig. 2.4, the STF and NTF are

$STF = z^{-2}, NTF = (1-z^{-1})^2$

For large OSR, its IBN is

$$\sigma^2_{q\_dsm} = \frac{\sigma_q^2}{f_{so}} \int_{-f_s/2}^{f_s/2} |1-e^{-j2\pi f/f_{os}}|^4 \, df \approx \frac{\sigma_q^2 \times \pi^4}{5 \times OSR^5} \tag{10}$$

and the SQNR can be expressed as

$$SQNR(dB) \approx 6.02B + 1.76 + 50\log(OSR) - 10\log\frac{\pi^4}{5} \tag{11}$$

This means we can now get 2.5 bits in SQNR for every doubling of the OSR.

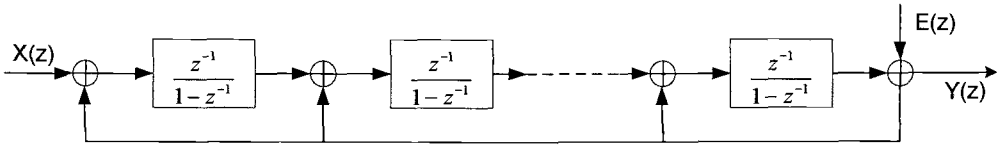


Fig. 2.5 N^{th}-order modulator

Similarly, for N-th order modulators, as shown in Fig. 2.5, the STF and NTF are $STF = z^{-N}, NTF = (1-z^{-1})^N$. For large OSR, the in-band integrated noise power is

$$\sigma^2_{q\_dsm} = \frac{\sigma_q^2}{f_{so}} \int_{-f_s/2}^{f_s/2} |1-e^{-j2\pi f/f_{os}}|^{2N} \, df \approx \frac{\sigma_q^2 \times \pi^{2N}}{(2N+1) \times OSR^{2N+1}} \tag{12}$$

and the SQNR can be expressed as

$$SQNR \approx 6.02B + 1.76 - 10\log(\frac{\pi^{2N}}{2N+1}) + 10 \times (2N+1)\log(OSR). \qquad (13)$$

In general, the SQNR will improve with the OSR at a rate of 6N + 3 dB/octave, or equivalently, N+0.5 bit/octave with N^{th} -order noise shaping.

2.3 Performance Increase and Improvement in the ΔΣ Modulators

Increasing rapidly the out-of-band gain of a high-order NTF will result in instability of ΔΣ modulators. When we follow the same analysis for the first order modulator, we discover that in the second order modulator $STF(z) = z^{-2}$ and $NTF(z) = (1 - z^{-1})^2$. In the case of an N^{th} order modulator, the same analysis give us $STF = z^{-N}$ and $NTF = (1 - z^{-1})^N$. $(1 - z^{-1})$ is called the filtering function or noise transfer function. As mentioned, the operating principle of ΔΣ modulators is based on shaping the quantization noise away from in-band to higher frequencies by means of a loop filter. The NTF of the ΔΣ modulator is a highpass filter function. It suppresses e at a frequency of around zero, but the NTF also enhances e at higher frequencies around $f_s/2$. It is clear that a high order modulator and a lot of oversampling will obtain a great deal of gain. But, when the out-of-band gain of higher order NTF increases rapidly, the $(1 - z^{-1})^N$ modulator is highly prone to instability through overloading the quantizer. It will result in oscillation. In order to enhance the stability, usually the loop gain is adjusted by scaling.

Increasing the OSR of a ΔΣ modulator will exponentially improve performance. However, for high signal bandwidth and high OSR, the sampling frequency increases the power consumption significantly. For ΔΣ modulators with signal bandwidth up to tens of kilohertz, a large OSR, from 64 to 256, is usually used with significant noise shaping, achieving a high resolution.

For a multi-bit quantizer, the resolution is increased proportionally to $(2^B - 1)^2$, the loop is inherently more stable since the quantizer gain is well-defined, and the no-overload range of the quantizer is increased. Multi-bit modulators may have very high *ENOB* even at low OSR values. By using multi-bit quantization, it will be possible to solve the feedback DAC nonlinearity. Although single-bit oversampling converters can realize highly linear data conversion, they also have some shortcomings [D. A. Johns1997]. For example, single-bit oversampling modulators are prone to instability due to the high degree of nonlinearity in the feedback. Another disadvantage is the existence of idle tones.

2.4 The Stability of ΔΣ A/D Converters

The ΔΣ modulator architecture is *stable* if all the internal state variables of the loop filter are bounded over time and the input to the quantizer is within specified limits, given any initial condition within a subset of state space and any input signal within certain bounds [T. Zourntos2002].

A way to ensure stability is to avoid the overload of the quantizer. This, however, is a very conservative approach, since modulators can be stable even if the quantizer occasionally overloads. Another explanation for instability [K. C.-H. Chao1990] is that as the signal at the input of the quantizer exceeds the quantizer limits, the amount of quantization noise |E(z)| increases. This excess noise is circulated through the loop and can cause an even larger signal to appear at the quantizer input, eventually causing instability. For a fourth-order loop, it has been determined through simulations that $|H_E(z)| < 2$ for |z| =1 at high frequencies is a necessary condition for stable operation with zero input. It should be noted that this rule is based on simulations and reduces the probability of instability rather than eliminating it.

Mathematical analysis of modulator instability in the general case is extremely difficult. Most approaches are based on state-space analysis and statistics. Zourntos applies variable-structure methods in the development of stable compensated modulators [T. Zourntos2003]. This method is based on switching methods found in variable structure control theory, provides a guarantee of stability with the "safety net" of a noise-shaped response even while the controller is active. Maeyer proposes a method based on the Nyquist stability criterion [J. D. Maeyer2006]. It uses the vector gain margin as a robust stability margin to design robustly stable modulators. Engelen proposes a design rule which is based on the describing function method, in which the nonlinear quantizer is modeled by a quasi-linear, signal-dependent transfer [J. V. Engelen1999] and [J. A. E. P.V. Engelen1999]. Thus, the commonly used "linear signal gain" model for a one-bit quantizer is extended with a phase shift, which is a phase uncertainty and represents the inaccuracy in time with which the zero-crossings of the quantizer input signal are detected. Simulation is used extensively to ensure stability in the practical design.

2.5 Comparison Between DT and CT $\Delta\Sigma$ Modulators

Most DT $\Delta\Sigma$ modulators are based on switched capacitor circuit techniques for good accuracy and good linearity. In DT design, the transfer functions are independent of the clock frequency [R. Schreier2005]. However, in switched-capacitor circuits, amplifiers with high unity-gain bandwidths of the opamps are required to satisfy the settling accuracy requirements. This limits the clock frequency and thus the input signal bandwidth.

CT $\Delta\Sigma$ modulators can potentially operate at higher clock frequencies with less power consumption. Since sampling only happens at the quantizer, there is no stringent requirement on opamp settling. Thus, the opamp specification is significantly relaxed [S. Yan2004]. However, CT $\Delta\Sigma$ modulators are usually more

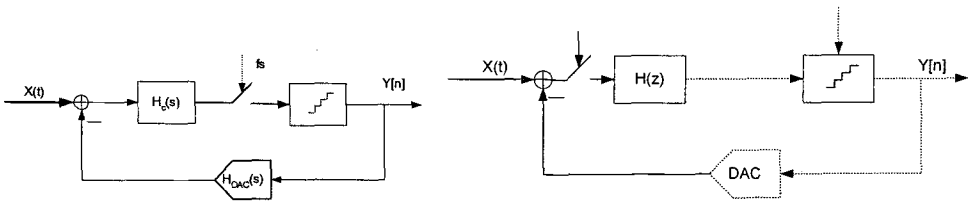
difficult to design and simulate than their DT counterparts. Circuit non-idealities, such as jitter sensitivity and excess loop delay, also limit the performance of continuous-time CT ΔΣ modulators.

2.6 Continuous-Time Loop Filter Synthesis

We will divide design synthesis into two parts: one is single-stage ADCs; and the other is multi-stage ADCs

The design synthesis of single-stage ADCs

The first method is Impulse-Invariant Transformation (IIT). As mentioned, a CT ΔΣ modulator is a combination of continuous and discrete systems. Since the discrete-time ΔΣ A/D converters have already been extensively studied and a great deal of resources and tools of design have already been developed, a simple way to design a continuous-time ΔΣ modulator is to transform the design of a discrete-time ΔΣ modulator into a CT ΔΣ modulator.



(a) (b)

Fig. 2.6 A diagram of (a) a CT ΔΣ modulator and (b) a DT ΔΣ modulator

As shown in Fig. 2.6, if after the transformation the sampled impulse response of the loop filter in the CT ΔΣ modulator matches its DT counterpart, *i.e.*, $q(n) = q(t)|_{t=nT_s}$, the transformation is called the impulse invariant transformation (IIT), which can be defined as

$$Z^{-1}\{H(z)\} = L^{-1}\{H_{DAC}(s)H_c(s)\}|_{t=nT_s} \tag{14}$$

where Z^{-1} represents the inverse z-transform, L^{-1} represents the inverse Laplace transform, and $H_{DAC}(s)$ represents the Laplace transform of the DAC waveform. Different DAC waveforms have different effects on the performances of the ΔΣ ADCs [J. Fang 2005].

The second method is a direct transformation approach [S. Paton2004] and [L. Breems2001]. Instead of matching a CT modulator to a DT modulator, a CT loop filter is designed as a starting point. Then this CT loop filter is optimized until it meets the specification.

The third approach is a transformation in state-space representation [R. Schreier1996] and [B. Zhang1996]. A set of state-space equations are used to design the CT ΔΣ modulators based on the DT ΔΣ modulators.

The design synthesis of multi-stage ADCs

The first method is the impulse invariance transform (IIT). The DT-to-CT conversion requires a conversion of the loop-filter to the CT-domain and adopts the same cancellation logic or filter for the discrete time modulators [M. Ortmanns2001][H. Shamsi2006]. It is necessary to provide every integrator input of the later stages with every (weighted) CT state variable and the feedback DAC output of all previous stages [M. Ortmanns2005].

The second method is a discretization of a CT system by using the state-space approach or the modified z-transform [O. Oliaei2003]. Arbitrary feedback waveform may be used.

The third method is the direct synthesis method [R. Tortosa2005][R. Tortosa2007] [S. Paton2006]. It is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-

continuous time transformation, as has been done in previous approaches. In addition to placing the zeroes of the loop filter in an optimum way, the direct methodology leads to more efficient architectures in terms of circuitry complexity, power consumption and robustness with respect to circuit non-idealities[R. Tortosa2005].

The fourth method is the mixed-mode methodology [C. H. Lin1999]. It is necessary to determine the correct s-domain and z-domain recombination of individual modulator outputs. This mixed-mode expression is quite tricky but it is more convenient in analysis of cascaded system.

The fifth method is a lifting method [M. Keller2006]. It will be applied to overcome the disadvantages afflicted with DT-to-CT transformation (e.g. less ideal anti-aliasing filter performance, increased circuit complexity) and to establish a time-efficient DT simulation model for the method which is entirely performed in the CT domain.

3 ARCHITECTURES

In this section we will review the topologies of the CT ΔΣ modulators, which include single-stage and multi-stage structures.

3. 1 Single-Stage CT ΔΣ Modulator Topologies

Loop filter architectures

Fig. 3.1 shows the general structure of a single-stage ΔΣ modulator. It is divided into two parts: the linear part (the loop filter) and the non-linear part (the quantizer).

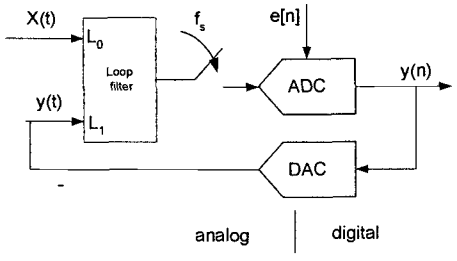


Fig. 3.1 General structure of a single-quantizer ΔΣ modulator

In order to analyze, this non-linear model may be simplified and transformed into a modified linear model, as shown in Fig. 3.2.

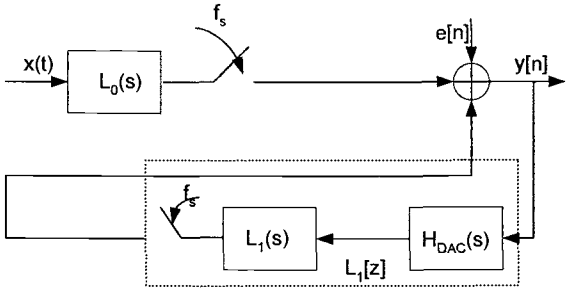


Fig. 3.2 Modified single-stage ΔΣ modulator

The NTF and STF are derived [A. Buhmann2006]:

$$NTF[z] = \frac{1}{1 - Z\{L^{-1} \mid H_{DAC}(s) \cdot L_1(s) \mid_{nT_s}\}} \approx \frac{1}{1 - L_1[z]} \tag{1}$$

$$STF = \frac{L_0(s)}{1 - Z\{L^{-1} \mid H_{DAC}(s) \cdot L_1(s) \mid_{nT_s}\}} \approx \frac{L_0(s)}{1 - L_1(z)} \tag{2}$$

where Z stands for Z-transform, L^{-1} represents the inverse Laplace transform. Note that no argument is given for the STF since it is a mixture between a CT and DT equation.

The single-loop high-order $\Delta\Sigma$ modulators can be divided into two structures: one is the loop filter with distributed feedback and input coupling---the CIFB and CRFB, and the other is a loop filter with distributed feedforward and input coupling---the CIFF and CRFF structures, as shown in Fig. 3.3 and Fig. 3.4.

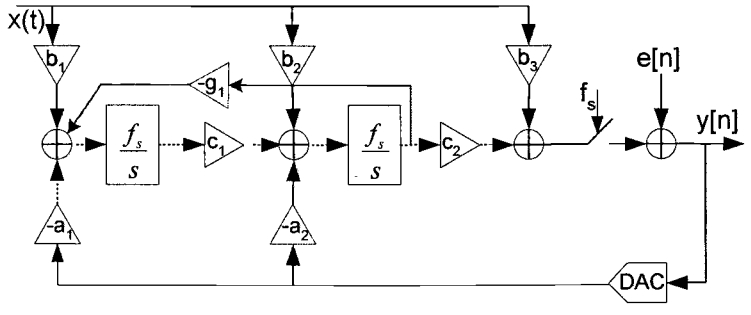


Fig. 3.3 CIFB ($g_1 = 0$) and CRFB ($g_1 \neq 0$)

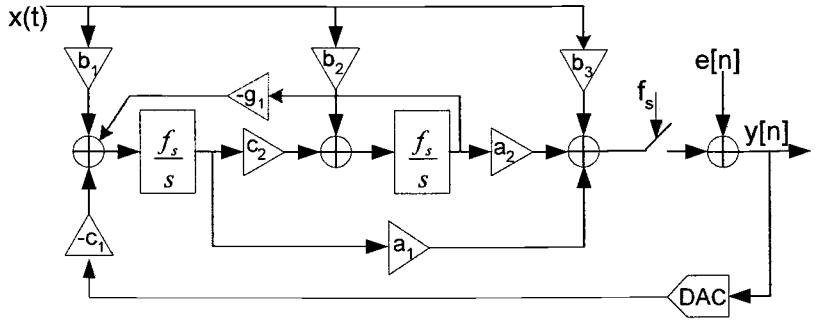


Fig. 3.4 CIFF($g_1 = 0$) and CRFF($g_1 \neq 0$)

From equation (2), we can derive the general expression of the STF according to [N. Beilleau2004] for the different CT $\Delta\Sigma$ modulators (CIFF, CIFB, CRFF and

CRFB). At system level, the modulator design is usually focused on maximizing the signal to noise ratio (SNR). Considering only the SNR criterion, feedforward and feedback topologies are equivalent because they can be designed to provide the same NTF. However, if we consider the STF, these topologies have different performances. First, the feedforward architectures have a filtering characteristic as a 1st order filter due to the path from the 1st integrator output to the adder before the sampling. The feedback architectures have an n^{th} order filter characteristics because the input signal passes through all the integrators. For the same NTF, the curve of CIFB amplitude falls steeper than CIFF. Second, another problem of feedforward architecture is out of band peaks. This is due to the zeros which do not exactly cancel the poles. This becomes a major drawback when the input signal is amplified by these peaks, resulting in integrator overload. Some methods may reduce the effect of the peaking, e.g., using surface acoustic wave (SAW) filter [R. Schreier2006] or adding a high-pass feedback path to a conventional $\Delta\Sigma$ ADC [K. Philips2004].

As the STF is considered, even though the feedback architectures are better than the feedforward architectures, the feedforward architectures are often preferred to the feedback architectures due to lower distortion, easier circuit implementation and less power consumption. [N. Beilleau2004]

Variations of loop filter

In [G. Mitteregger2006], in order to save power and to maintain a good anti-alias filter characteristic in the STF, a combination of a feedforward and a feedback stabilized loop filter is implemented as shown in Fig. 3.5. The feedback path to the second integrator input is replaced by the feedforward path k_{4FF} in order to eliminate one DAC. Another advantage of this loop filter topology is that the bandwidth of the first integrator can be large, as there is no feedback to the following stage and the output signal swing of this integrator can be scaled only

with its bandwidth. A high bandwidth of the first integrator suppresses the thermal noise of the following integrators.

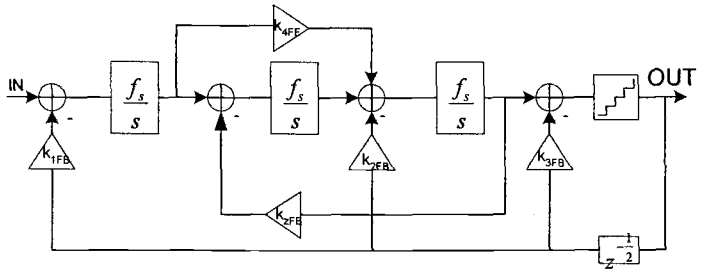


Fig. 3.5 Mixed CRFF and CRFB architecture

Chao proposed another kind hybrid configuration as shown in Fig. 3.6 [K. C. –H. Chao1990]. The most important feature of this topology is the feedforward structure with coefficients (a_1, a_2, a_3, a_4) and a feedback structure with coefficients (b_1, b_2, b_3, b_4). The large number of loop coefficients not only allows one to stabilize the modulator, but also to optimize the NTF.

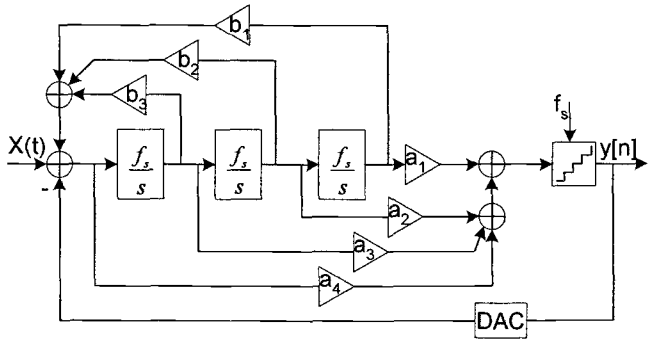


Fig. 3.6 The a_i coefficients implement the poles of the quantization noise response, and the b_i coefficients produce the zeros.

Schreier proposed a modified feedforward architecture to take advantage of the characteristic low distortion and high dynamic range of a feedforward topology as shown in Fig. 3.7 [R. Schreier2006]. The first, second, and third resonators in the loop filter are signal resonators. The final resonator is the image resonator. Placing the image resonator at the end frees the preceding resonators from the

need to process image signals and thereby prevents mismatch in those resonators from reflecting image noise into the passband.

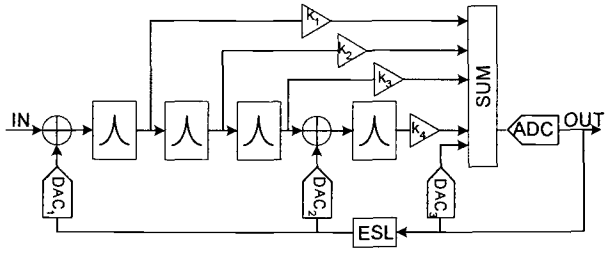


Fig. 3.7 Fourth order (SWA) continuous-time ΔΣ modulator

Yan proposed a 3-order CRFF architecture, as shown in Fig. 3.8 [S. Yan2004]. One clock delay is purposely introduced in front of DAC_A in the main noise-shaping loop to accommodate the nonzero time delay of the internal DAC. To keep the output of the loop filter unchanged at the sampling instants, a feedback path is added from the output to the input of the internal ADC, formed by a half clock cycle delay and DAC_B. This additional feedback is only one feature in this design architecture.

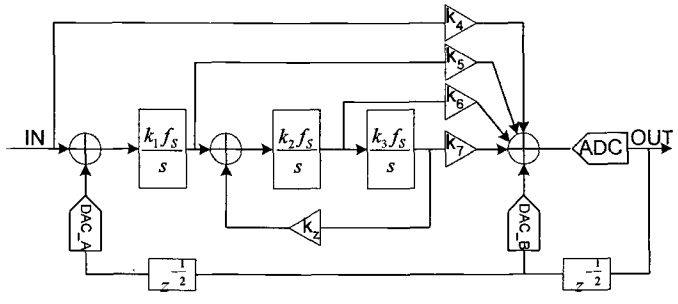


Fig. 3. 8 Conventional continuous-time ΔΣ modulator
with an additional feedback path

Cosand proposed a CRFF structure with an extra feedback path [A. E. Cosand2004]. An additional feedback path is added back to the input of the quantizer. This additional feedback path improves the overall noise transfer function and stability by allowing the high-frequency quantization noise to be fed

back around a shorter feedback path. Adding this extra feedback path allows one to improve the wide-band SNR by 10 dB and achieves a higher margin of stability.

Paton proposed a conventional 4-order CRFF continuous-time ΔΣ modulator topology [S. Paton2004], as shown in Fig. 3.9. A multiple feedforward topology has the advantage of requiring only one DAC, compared to its multiple feedback counterpart that needs as many DACs as the modulator order. Due to the low OSR and the circuit-imposed excess loop delay of this particular design, a second DAC is needed to partially compensate the excess loop delay. The gain of this DAC (coefficient *fbe*) is programmable such that stability can be improved for a wide range of delays. This DAC is placed around the quantizer to keep its linearity requirements low.

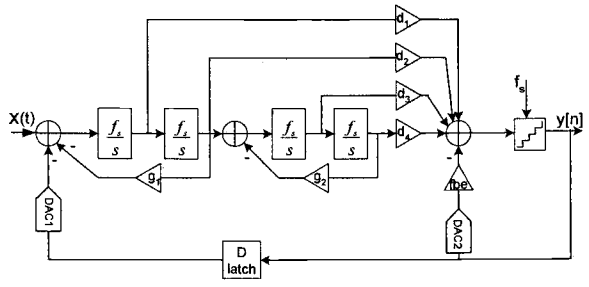


Fig. 3. 9 A 4-order CRFF CT ΔΣ modulator architecture

As mentioned before, most of the implementation of CT ΔΣ modulators use the modified feedforward architecture because of the low distortion and high dynamic range of the feedforward topology. The disadvantage of a feedforward topology is the out-of-band peaking of STF

Hybrid CT ΔΣ modulator

A loop filter with combined CT and DT circuits is an alternative approach to realize a high-performance ΔΣ modulator. The primary reason for using continuous-time stage instead of discrete-time stage is noise. The dynamic range of the converter is determined by the feedback and the first integrator noise

performance [B.D. Signore1990]. This combined loop filter structure offers several important advantages. First, since there is no sampling of the input voltage, signal-dependent clock feedthrough and noise resampling in the first integrator do not exist. Secondly, any signal-dependent glitches coupled into the first integrator are averaged out over the clock period. This averaging characteristic of the CT integrator greatly reduces the harmonic distortion due to coupling. Thirdly, the input impedance of the first integrator is purely resistive, hence, it does not emit EMI back to the input pins. Finally, the intrinsic anti-alias filtering property of the CT first stage is preserved.

Nguyen proposed a ΔΣ modulator with hybrid structure [K. Nguyen2005] as shown in Fig. 3.10. A data-directed scrambler is used to spectrally shape the error caused by the feedback DAC's unit element mismatch into the out-of-band frequency region. The feedforward SC path from the analog input to the second integrator reduces the distortion and opamp output. The disadvantage of this feedforward path is that the input impedance is no longer resistive.

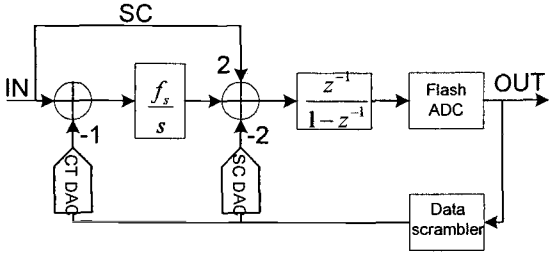


Fig. 3. 10 A ΔΣ modulator with the loop filter implemented by Hybrid DT and CT circuits

The hybrid structure is used [H. Tao1999] as well. As shown in Fig. 3.11, a four-order direct-conversion bandpass ΔΣ modulator is designed. This ΔΣ modulator uses a low Q CT bandpass filter in the first stage, followed by the analog I/Q modulator to translate the narrow-band signal from its carrier frequency to baseband.

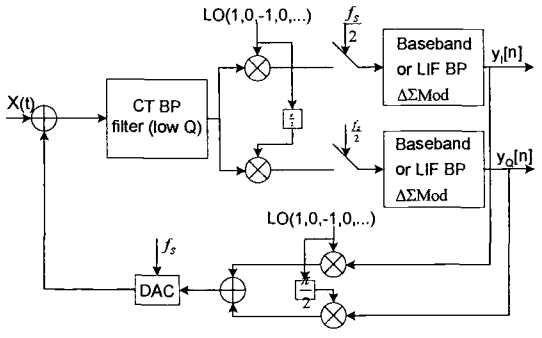


Fig. 3.11 Direct-conversion bandpass ΔΣ modulator
with mixed CT and DT components

Song presented a 5th-order continuous-time ΔΣ modulator with a hybrid active-passive loop filter consisting of only three amplifiers [T. Song2006-1] and [T. Song2006-2], as shown in Fig. 3.12. Passive networks do not consume power and do not introduce distortion. The active integrators provide gain and minimize internal noise contributions. It is a low power, high bandwidth continuous-time ΔΣ modulator.

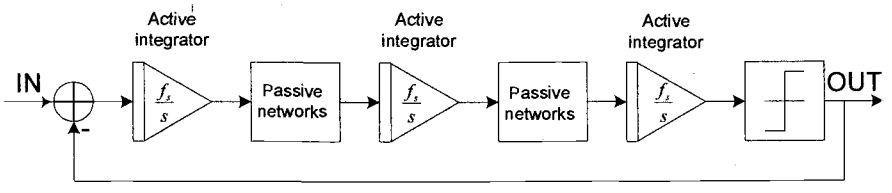


Fig. 3. 12 A 5th-order CT ΔΣ modulator with a hybrid active-passive loop filter

Complex or Quadrature Bandpass CT ΔΣ modulator

The complex or quadrature bandpass CT ΔΣ modulator, as shown in Fig. 3.13, is reviewed in this section. Commonly, in the baseband receive path, low-IF (LIF), or zero-IF(ZIF) in phase and quadrature signals (I/Q) or real and complex signal from a transceiver quadrature mixer are converted to digital, bandpass or low-pass filtered and down-sampled. The architectures of these bandpass CT ΔΣ modulators have usually combined two separate and independent basic topologies with pairs of resonators. It usually consists of two ΔΣ modulators. For example, Baggini and

Silva proposed a bandpass CT CRFF ΔΣ modulators built with real and complex resonators [B. Baggini2006] and [P. G. R. Silva2007]. Arias proposed a 2^{nd}-order CT CRFB ΔΣ modulator with real and complex resonators [J. Arias2006]. While two separate and independent I and Q ADCs are used in low-pass mode for heterodyne and ZIF receivers, complex (I+jQ) ADC is used in bandpass mode for LIF receivers. In low-pass mode, the cross-coupling networks are switched off. In this mode, we obtain two independent and totally equal I and Q m^{th} -order converters. The ADC operates in the complex bandpass mode, when the cross-coupling networks are activated or switched on. Therefore, we obtain a dual-mode combination I and Q m^{th} -order converters.

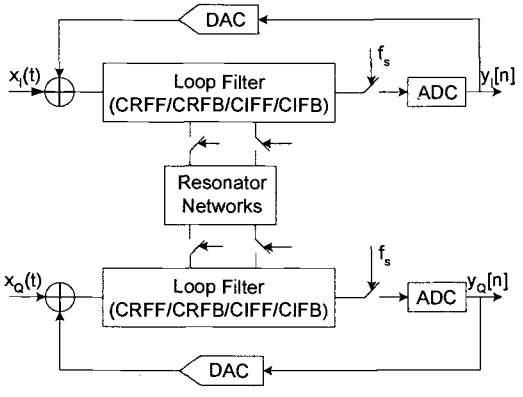


Fig. 3.13 a complex/quadrature basspass CT ΔΣ modulators

The bandpass and quadrature modulators preserve many of the advantages of lowpass ΔΣ modulation and are particularly useful in modem receiver systems where high-frequency narrowband signals are converted to digital form without down-converting to baseband. At the system level, the two primary advantages of bandpass conversion are the elimination of one or more analog downconversion operations, and the preservation of the spectral separation between the signal and various low-frequency noise and distortion components. At the circuit level, bandpass conversion is more efficient than converting the entire frequency band

between 0 and $f_0 + f_B/2$, since no power is wasted on the accurate conversion of unwanted signals between 0 and $f_0 - f_B/2$.

Time-Interleaved (TI) ADC

Since a ΔΣ modulator oversamples the data, the signal bandwidth is limited by the maximum sampling frequency, the OSR, the opamp bandwidth and the sampling switches[K. S. Lee2007]. One method to add another degree of freedom is to use parallel ΔΣ structures. The simplest method of making parallel converters is through the use of time-interleaving. Time-interleaved ΔΣ modulator topologies based on block filtering theory. Block digital filtering can be used to DT TI ΔΣ modulator [R. Khoini-Poorfard1997] as shown in Fig 3.14. Assuming the same initial conditions, Fig 3. 14 (a) is equivalent to Fig 3. 14 (b) from an input-output point of view. A block digital filter is a system in which parallelism is used to reduce the speed requirement on each processing element.

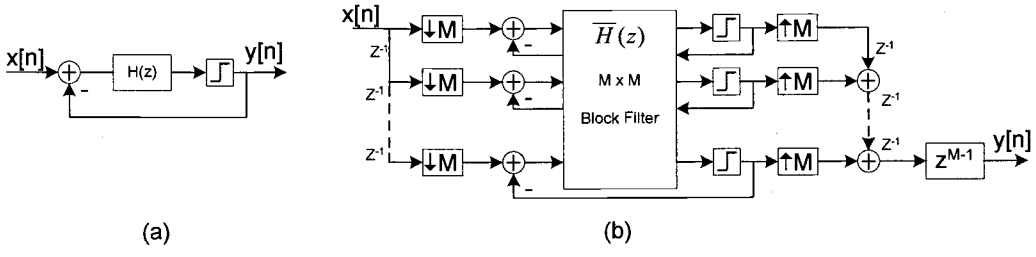
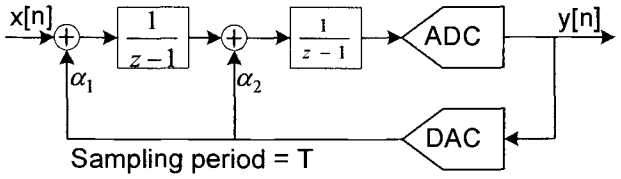


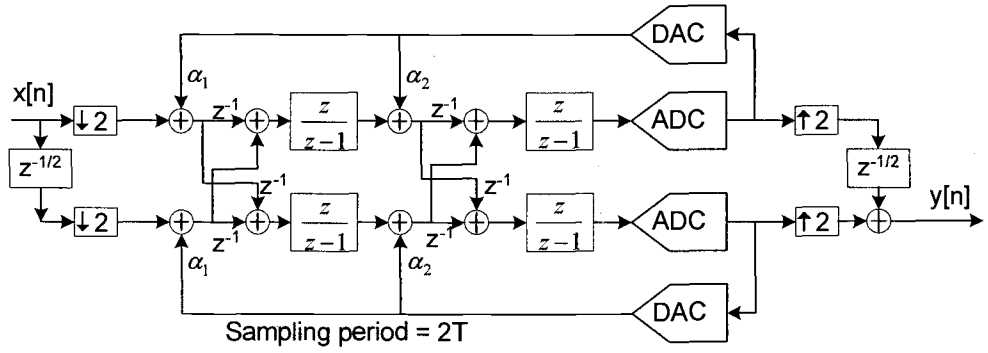
Fig 3. 14 DT TI ΔΣ modulator

However, CT ΔΣ modulators can also be time-interleaved [T.C. Caldwell2005-1] and [T. C. Caldwell2005-2]. A CT TI ΔΣ modulator combines the advantages of the time-interleaving and continuous-time filter. Employing the CT loop filter instead of the DT loop filter is one way to increase the input signal bandwidth. And employing the parallelism of time-interleaving reduces the speed requirement on each processing element.

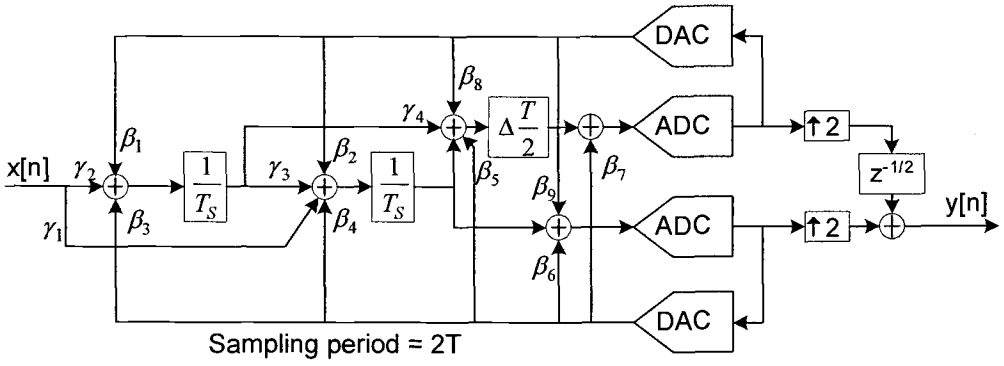
Caldwell presents the combination of these two techniques by introducing a method of CT TI ΔΣ modulators[T.C.Caldwell2006], as shown in Fig. 3.15,



(a)



(b)



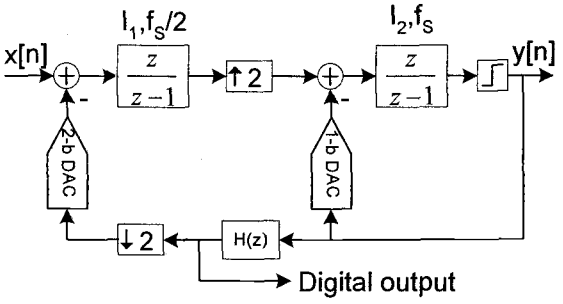
(c)

Fig. 3. 15 (a) A 2nd-order DT ΔΣ modulator (b) DT to DT TI modulator transform (c)CT TI modulator with additional DAC feedback path

where the ADCs and DACs are operating at half of the original frequency. Thus, clock jitter has about half the impact on the ΔΣ modulator. Furthermore, the higher bandwidth requirements on an RZ DAC operating at high speeds

(assuming the choice of an RZ DAC pulse to reduce the excess loop delay) is reduced by a factor of two by time interleaving. The characteristics of CT TI ΔΣ modulator are that it may obtain more bandwidth at the cost of hardware complexity.

In the above approach, parallelism is applied to every integrator, including the first one. However, the performances of the overall modulator strongly depend on the first integrator. In [F. Colordro2006], time-interleaving is not applied to the first integrator, which leads to a reduction in the area and power consumption when compared to other TI and parallel implementations as shown in Fig. 3. 16. This is a promising technique for the design of high speed, low-power modulators. The anti-aliasing filter H(z) is required before the quantizer output is down-sampled and fed back to the modulator input.



(a)

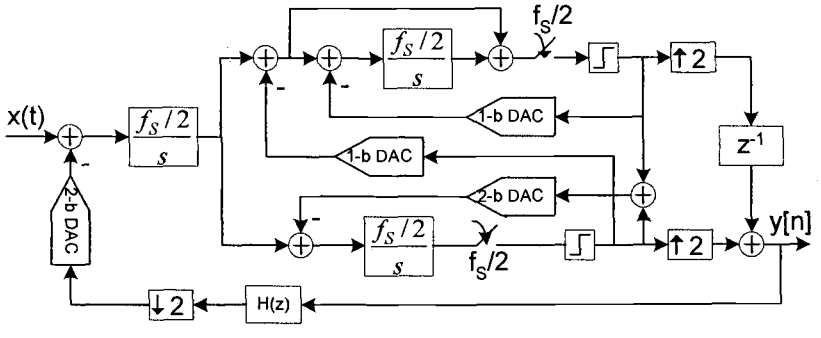


Fig. 3.16 (a) 2nd-order multirate ΔΣ modulator

(b) DT transform to parallel-CT ΔΣ modulator

This is a parallel CT ΔΣ modulator. It can be concluded that the SNDR of a CT ΔΣ modulator improves by using parallelism. This architecture still suffers from the quantizer domino effect so that additional work is still required to get a feasible circuit implementation for this modulator.

To conclude the considerations on single-stage modulators, it should be noted that there are numerous architectures. The implementation of the loop filter is expressed in the building of the CT ΔΣ modulator. However, the effort spent on architectural optimization is always based on the same reasons: to obtain a stable modulator with maximum quantization noise and interferer suppression, while keeping the signal swing requirements as low as possible [A. Buhmann2006].

3. 2 Multi-Stage CT ΔΣ Modulator Topologies

In a single-loop ΔΣ modulator, when the oversampling ratio (OSR) is low, it is difficult to obtain high SQNR by increasing the order of the loop filter, since it tends to reduce the stability of the modulator.

To solve this problem, the cascade, also called multi-stage or MASH (for Multi-stAge noise-Shaping) modulator structures are used. The main idea is to feed the quantization error of the previous ΔΣ modulator stage into another ΔΣ modulator stage and combine the outputs of both stages in digital filter. By doing this, higher-order noise shaping can be obtained. Meanwhile, because a cascaded modulator is constructed from low-order ΔΣ modulators, the stability of the low-order **ΔΣ** modulators is maintained.

Multi-Stage Loop Filter Structure

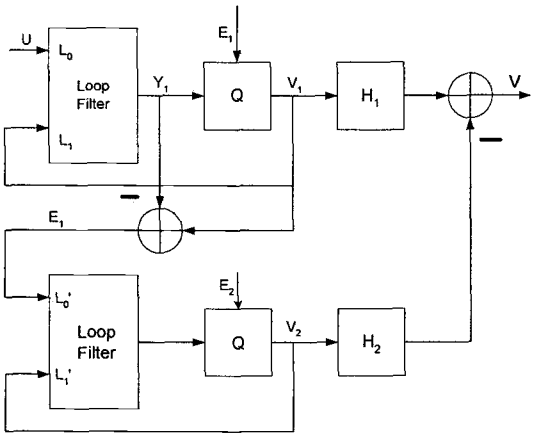


Fig. 3. 17 A two-stage MASH structure

As is shown in Fig.3.17, the output signal of the first stage and the second stage are given by

$$V_1(z) = STF_1(z) \cdot U(z) + NTF_1(z) \cdot E_1(z) \tag{3}$$

$$V_2(z) = STF_2(z) \cdot E_1(z) + NTF_2(z) \cdot E_2(z) \tag{4}$$

where $STF_1(z)$, $STF_2(z)$, $NTF_1(z)$ and $NTF_2(z)$ are the signal and noise transfer functions of the first and second stages, respectively. The digital filter stages $H_1(z)$ and $H_2(z)$ at the outputs of the two modulator loops are designed such that in the overall output $V(z)$ of the quantization noise of the first stage $E_1(z)$ has been completely eliminated. Thus $H_1(z)$ and $H_2(z)$ has to satisfy the condition as follows

$$H_1(z)NTF_1(z) - H_2(z)STF_2(z) = 0 \tag{5}$$

The simplest (and usually most practical) choices for $H_1(z)$ and $H_2(z)$ are $H_1(z) = STF_2(z)$ and $H_2(z) = NTF_1(z)$. The overall output is then

$$\begin{aligned} V(z) &= H_1(z)V_1(z) - H_2(z)V_2(z) \\ &= STF_1(z) \cdot STF_2(z) \cdot U(z) - NTF_1(z) \cdot NTF_2(z) \cdot E_2(z) \end{aligned} \tag{6}$$

Only the filtered quantization error of the second stage remains. Similarly, we can get the general expression for the output of *n*-stage MASH structure as shown in Fig 3. 18.

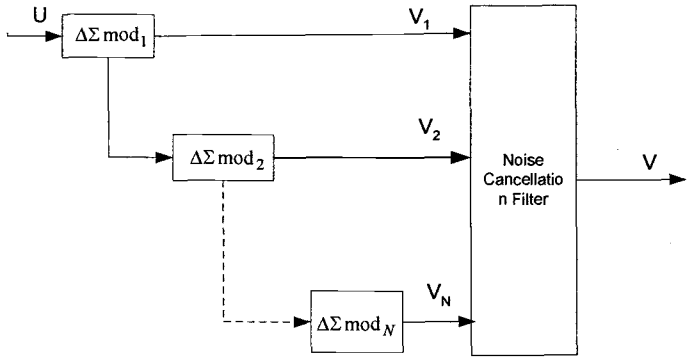


Fig 3.18 A N-stages MASH structure

$$V(z) = STF_1(z) \cdot STF_2(z) \cdot ... STF_n(z) \cdot U(z) - NTF_1(z) \cdot NTF_2(z) \cdot .... \cdot NTF_n(z) \cdot E_n(z) \quad (7)$$

Only the filtered quantization error of the last stage remains. For instance, for 2-2 cascaded modulator, $STF_1(z) = STF_2(z) = z^{-2}$, $NTF_1(z) = (1 - z^{-1})^2$ and $NTF_2(z) = (1 - z^{-1})^2$, the overall output will be

$$V(z) = z^{-4} U(z) - (1 - z^{-1})^4 E_2(z)$$

Thus, in terms of quantization noise shaping performance, the 2-2 cascaded modulator is equivalent to a 4th-order single-stage modulator. At the same time, the stability of the 2-2 cascaded modulator is the same as that of the second-order single stage modulator. It can be shown that an *m*-stage cascaded ΔΣ modulator with first or second order modulators has better performance than an m^{th} -order single-stage ΔΣ modulator when tones are concerned [W. Chou1989].

Compared with single-stage CT ΔΣ modulators, the characteristics of the cascaded continuous-time ΔΣ modulators achieve the high resolution with high

OSR and ultra low voltage, lower power consumption in [C. H. Lin1999], reduce stability problems, increase the effectiveness of each integrator in quantization noise suppression, have larger modularity, offer better dynamic range at a relative low OSR, have a high-order noise-shaping characteristics, and increase the effective bandwidth. However, there is a noise leakage problem in multi-stage structure which originates from the mismatch between analog and digital transfer functions. This leakage degrades the performance, and thus, correction algorithms are necessary.

Multi-Stage Architectures

The multi-stage approach relies on the cancellation of the quantization error by cascading low order single-stage modulators, i.e. first and second order, rather than on filtering as performed by single-stage modulators. We summarize papers published in Table 3.1.

Table 3.1. Cascade topologies in recent papers

Year	Name	Cascade Level	1st-stage AP	2nd or 3rd stage AP
2007	L. Breems	cascade 2-2	(3), (4)	I21
2007	R. Tortosa	cascade 3-2	(3)	I21
2007	M. Keller	cascade 2-1	(1), (2),(4)	I21
2007	M. Renedo	cascade 2-2	(1), (3)	I21, I22, I23
2007	S. Kulchycki	cascade 2-1	Before & after ADC	I21
2006	H. Shamsi	cascade 2-1-1	(3),(4)	I21/I31
2006	M. Keller	cascade 2-1-1	(2), (3), (4)	I21 & I31
2006	S. Paton	cascade 2-2	(1), (2), (3), (4)	I21
2006	R. Tortosa1	cascade 2-2-1	(2)	I21
2006	R. Tortosa2	cascade 2-1-1 & 2-1-1-1	(3)/(2)	I21/I31, I21/I31/I41
2005	R. Tortosa	cascade 2-1-1	(3)	I21/I31
2005	M.Ortmanns	cascade 2-1-1	(2), (3), (4)	I21/I31
2004	M. Keller	cascade 2-1-1	(3), (4)/(2), (3), (4)	I21/I31

2004	L. Breems	cascade 2-2	(3), (4)	I21
2003	P. Benabes	cascade	(3), (4)	I21
2003	O. Oliaei	cascade 2-1 & 2-2	(2), (3), (4)/(3), (4)	I21/I21, I22
2001	M. Ortmanns	cascade 2-1	(2), (3), ADC	I21
1999	C. Lin	cascade 2-1	(3)	I21

Note that the numbers of the first stage access points (AP) are the same Fig 3. 19 and the letter *I* and the numbers of the second- or third stage access points are the input of the first, second or third integrator in Fig 3.19. It may be seen that the order of the first stage is not more than third order, since it is not possible to achieve an ideal third order or higher order noise shaping. In order to clearly explain multi-stage architectures, we use two-stage MASH in our examples. We conclude that two-stage architectures most papers represent may be a topology to explain as shown in Fig 3. 19. Note that when we activate some dashed lines, it represents that the line is connected. Otherwise, the line is disconnected. The purpose of block Σ is to estimate the quantization noise of the first stage and remove or attenuate any input signal component inside the band of interest. The gain block K has been included to amplify the first quantization noise up to full scale of the second stage. The simplest choice for block Σ is to implement a linear combination of the incoming signals: the input signal U(t), the integrator outputs $X_{1A}(t)$ and $X_{2A}(t)$, and the output of the first modulator $Y_{DAC}(t)$ followed by a DAC. Then

$$U_B(t) = k_u \cdot U(t) + k_1 \cdot X_{1A}(t) + k_2 \cdot X_{2A}(t) + k_y \cdot Y_{DAC}(t) \qquad (8)$$

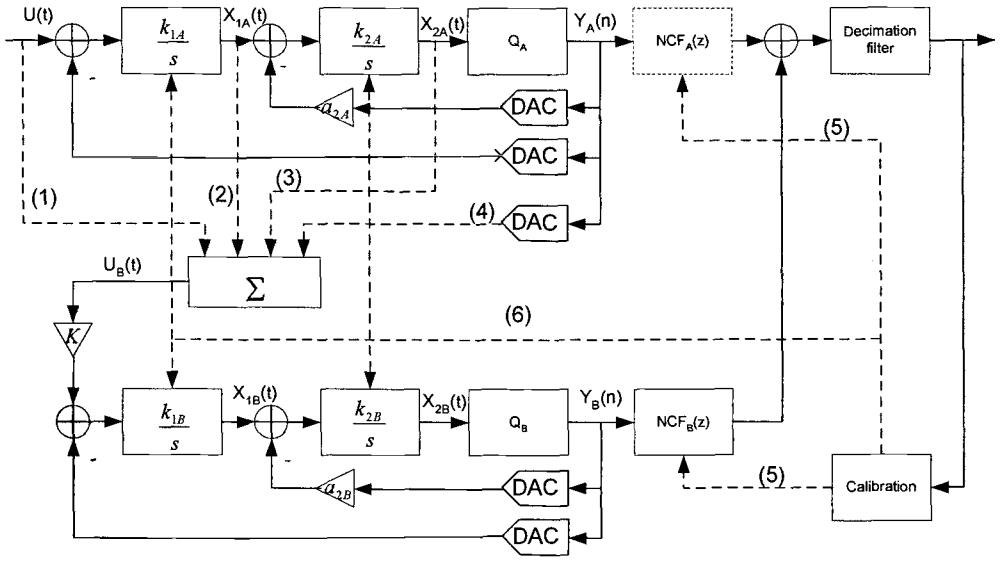


Fig 3.19 General architecture for two-stages CT modulator

where k_U, k_1, k_2, and k_Y are coefficients. In order to conveniently analyze, these coefficient values may be just 0 or 1 or -1. For recent papers, we will divide them into *A*, *B*, *C* and *D* classes.

A class includes lines (2), (3) and (4) activated (k_U=0, k_1= k_2= 1 and k_Y=-1). $U_B(t)$ is determined by $X_{1A}(t)$, $X_{2A}(t)$ and $Y_{DAC}(t)$. Such circuits are in [M. Keller2007], [M. Keller2004], [M. Keller2006], [M. Ortmanns2005A], [M. Ortmanns2001], [M. Ortmanns2005B] and [O. Oliaei2003]. By employing auxiliary feedforward paths, the cascaded CT ΔΣ modulator is derived. But this class architecture is complicated, involving a lot of additional feed-forward paths. These auxiliary feed-forward paths increase the input referred thermal noise and put hard conditions for the opamps of the integrators because they should drive a lot of feedforward paths, and the feedback factor of the opamp's will be small.

B class is line (3) and line (4) activated (k_U= k_1=0, k_2= 1andk_Y=-1). $U_B(t)$ is determined by$X_{2A}(t)$and $Y_{DAC}(t)$. References include [L. J. Breems2004], [L. J. Breems2007], [R. Rutten2006], [M. Keller2004], [P. Benabes2003], [H. Shamsi2006], [O. Oliaei2003] and [M. S. Renedo2007]. By using this structure, the loop gain of each stage is isolated from the loop gain of the other stage [H. Shamsi2006]. It has harder requirement for mismatch between the analog and digital filter coefficients due to process variations, and the amount of SQNR improvement by means of noise cancellation is limited by the accuracy of the coefficients. To compensate for mismatch between the digital NCF and the analog filter, calibration is needed. In [L. J. Breems2004], calibration compensates NCF while (5) is activated. In [L. J. Breems2007], calibration compensates integrators while (6) is activated. The quantization error signal of the first-stage, which is the difference between the sampler input or output signal and the output of the DAC, is fed to the input of the second-stage. The sampler input signal is a continuous-time signal and as a result, the quantizer error signal can become larger than half a least significant bit (LSB). Therefore, care should be taken that the error signal does not overload the second stage. Based on *B* class, Renedo uses the interstage feedback technique, which is that the difference between the input of ADC and the output DAC in the second-stage is fed back to the input of ADC in the first stage [M. S. Renedo2007]. The loop filter resonator is not needed to introduce an NTF zero. Interstage feedback is used to improve the loop filter stability and make possible the application of a very simple mismatch digital correction method.

C class is line (3) activated (k_U= k_1=0, k_2=1 andk_Y=0). $U_B(t)$ is determined by$X_{2A}(t)$. This is done in [R. Tortosa2007], [R. Tortosa2006], [R. Tortosa2006], [R. Tortosa2006], [R. Tortosa2005] and [C. H. Lin1999]. The number of integrating paths can be reduced if the whole cascaded $\Delta\Sigma$ modulator is directly synthesized in the CT domain. Then no calibration is used to compensate for

mismatch and element tolerances, thus optimizing their performance in terms of circuit complexity, power consumption and sensitivity with respect to mismatch.

D class is line (1) and line (3) activated (k_U= 1, k_1=0, k_2=1 and k_Y=0). $U_B(t)$ is determined by $U(t)$ and $X_{2A}(t)$. An example is the cascade 2-2 CT $\Delta\Sigma$ modulator [M. S. Renedo2007]. The Fig. 3.19 didn't show the lines between *U(t)* and $X_{1B}(t)$ and $X_{2B}(t)$. The first quantization error is obtained from the quantizer input of the first stage. To remove the input signal in the second stage, feedforward coefficients going from the input signal to the second stage are applied. Through a proper selection for the values of these coefficients, the input signal at the integrator outputs is high-pass shaped. This allows the interstage gain *K* to be incremented, hence improving the SNR without overloading the second stage. Thus, the first quantization error is scaled by *K* and shaped by the STF of the second stage, which limits the practical value of K. In addition, the second-stage overload can be controlled without changing the NCFs. Hence, the tuning of the cascaded CT $\Delta\Sigma$ modulator is simplified. The anti-aliasing functionality is also preserved.

Finally, Kulchychki presents a modulator architecture that combines the benefits of CT and DT circuits [S. D. Kulchycki2007], as shown in Fig 3. 20. The second-order first stage of a two-stage cascade is implemented in CT, while the first-order second stage is a DT circuit. Calibration of the integrator time constants in the CT stage mitigates the performance impact of mismatch between the analog and digital coefficients in the cascade.

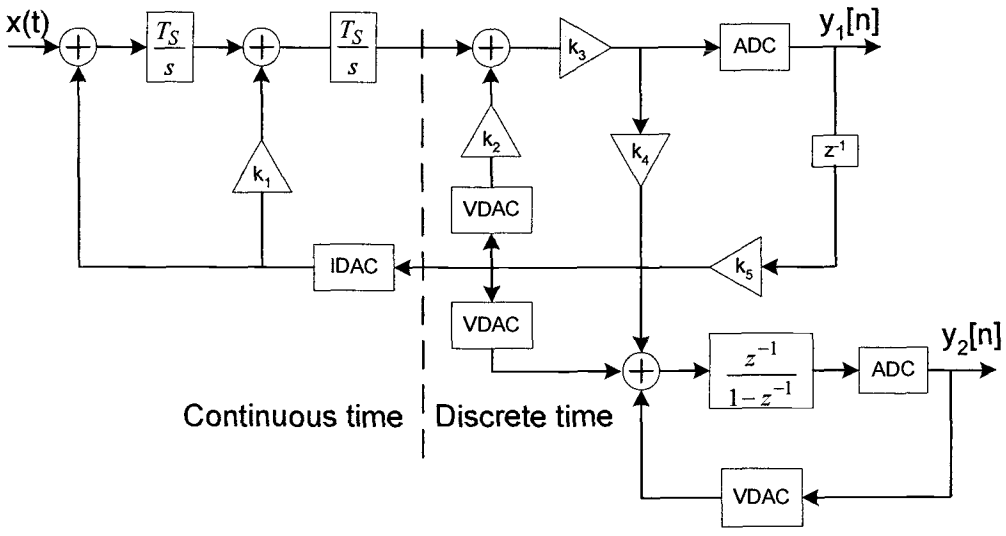


Fig 3. 20 CT/DT modulator architecture

In short, multi-stage CT $\Delta\Sigma$ modulator architectures have stability and high resolution. However, since there is mismatch problem and complexity in multi-stage, so far it still is not popular in application.

4 NON-IDEALITIES AND CORRECTION TECHNIQUES

As shown in Fig.4.1 [A. Buhmann2006], the performance of the ΔΣ ADC is influenced by the various non-idealities existing in the loop filter, the quantizer and the DAC. In this section, these non-idealities are discussed and the correction techniques are reviewed.

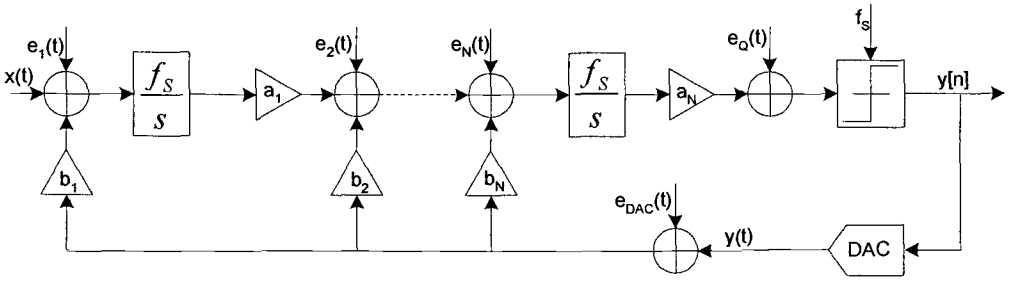


Fig. 4.1 Errors distribution in ΔΣ modulator

Every error will contribute its non-ideality to ΔΣ modulator. No matter which kind of architecture is used, single-stage or multi-stage, they are most sensitive to any input referred noise and distortion of the first integrator $e_1(t)$ and the error at the feedback DAC $e_{DAC}(t)$. Compared to the errors entering the first integrator, errors entering the system at other points are less critical. They often are suppressed by the preceding or following integrator.

4.1 Non-idealities in the DAC (I)---Excess loop delay

Excess loop delay is a timing non-ideality. Excess loop delay in a CT ΔΣ modulator refers to a delay between the sampling clock edge and the change in output bit as seen at the feedback point in the modulator [J. A. Cherry1999]. The loop delay occurs when the comparator response in the quantizer is a longer decision time and the propagation time in the latch and the DAC are too long. The signal-dependent delay in the quantizer can be absorbed or buffered by using an additional latching stage after the quantizer. However, this latching stage does not

absorb the delay in the feedback DAC itself and when the sampling frequency is very high, the delay introduced by the DAC will contribute more to the total loop delay and degrades the performance of the CT ΔΣ modulator.

Excess loop delay can be modeled by $t_d = \tau_d \cdot T$, as depicted in Fig. 4.2 for an NRZ DAC pulse. The value of τ_d is dependent on the switching speed f_t of the transistors, the quantizer clock f_S, the number of transistors n_t in the feedback path, as well as the loading on each transistor. Their relationship may be represented by $\tau_d \approx \frac{n_t \cdot f_S}{f_t}$ [J. A. Cherry1999]

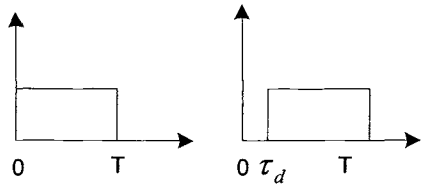


Fig. 4.2 Excess loop delay for an NRZ DAC

Excess loop delay can have two different effects in CT ΔΣ modulators: firstly, a delay that shifts the DAC pulse but retains the entire pulse in the actual sampling instant, like an RZ DAC pulse as shown in Fig. 4.3; Secondly, a delay that shifts the DAC pulse into the next sampling instant, like an NRZ DAC as shown in Fig. 4.4.

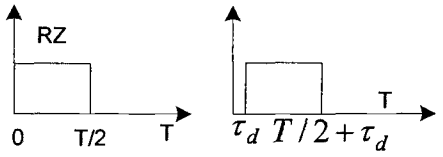


Fig 4.3 Excess loop for a RZ DAC

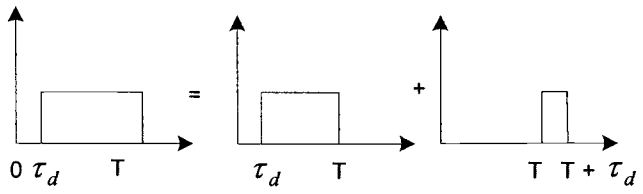


Fig. 4.4 Two-pulse represents excess loop delay for an NRZ DAC

For simplicity, we assume a perfectly rectangular DAC pulse of magnitude 1 that lasts from α to β. We consider the $\Delta\Sigma$ modulator with NRZ DAC pulse. For this type of DAC, $(\alpha,\beta) = (0,T)$. Any excess loop delay $\tau_d > 0$ causes $\beta > T$, which means the end of the pulse extends beyond $t = T$. If we use a DAC pulse with $\beta < T$, then the pulses would extend past $t = T$ only if the condition $\tau_d > T - \beta$ held. If we used an RZ DAC instead of an NRZ DAC, for a given $\tau_d \leq 0.5T$, the order of the equivalent DT loop filter may be equal to the order of the CT loop filter by tuning the parameters. So, an RZ code is to reduce pulse distortion and avoid the excess loop delay [J. A. Cherry1999A]. He concludes that in general, in any CT modulator with enough excess delay to push the falling edge of a DAC pulse past $t = T$, the order of the equivalent DT loop filter is one higher than the order of the CT loop filter [J. A. Cherry1999A].

Excess loop delay will make a CT $\Delta\Sigma$ modulator unstable, and decreases the dynamic range. The filter coefficients depend on the loop delay of the DAC feedback pulses [R. Schoof2007]. As loop delay increases, a full sample of feedback delay causes SNR loss [J. A. Cherry1999A]. Usually in CT $\Delta\Sigma$ modulators, for an excess loop delay of 20% [R. Schoofs2007] to 22% [K. P. J. Thormas2005] of the clock period, the modulator can be stable. The effect of loop delay will tend to become more severe as clock speeds are increased. If the loop delay causes the DAC pulse to extend beyond T, then the modulator order increases by one, which may eventually make a CT $\Delta\Sigma$ modulator unstable [J. A.

Cherry1998]. As excess loop delay increases, the in-band noise (IBN) increases and the maximum stable amplitude (MSA) decreases. The result will decrease the dynamic range [J. A. Cherry1999A].

When we design a CT $\Delta\Sigma$ modulator, we should reduce the influence of the excess loop delay to the system. Various methods have been proposed to compensate for excess loop delay, including different DAC waveforms, feedback coefficient tuning and the inclusion of zero-order feedbacks. Choosing the right DAC pulse shape in combination with tuning of the feedback parameters (either in the design phase or automatically on-line) can greatly reduce the performance degradation brought by the excess loop delay. Note that by reducing the loop gain to compensate for the loop delay, it will deteriorate the NTF and cause the modulator to have less dynamic range and more IBN [J. A. Cherry1999]

The following methods provide ways to reduce the effect of excess loop delay.

(1) Add one or half a period delay in the feedback loop [H. Aboushady2004]. This delay should be sufficiently large to cover comparator and digital circuitry delay. It will be shown that in $\Delta\Sigma$ modulators it is possible to compensate for the loop-delay without additional coefficients.

(2) One clock delay is purposely introduced in front of DAC_A in the main noise-shaping loop to accommodate the nonzero time delay of the internal ADC as shown in Fig 4. 5 [S. Yan2004]. To keep the output of the new loop filter unchanged at the sampling instants, a feedback path is added from the output to the input of the internal ADC, formed by a half clock cycle delay and DAC_B. Thanks to the architectural improvements, the total time delay of the internal ADC and the feedback DAC is relaxed to nearly one clock period. Thus, the excess loop delay problem of conventional CT $\Delta\Sigma$ modulators is eliminated.

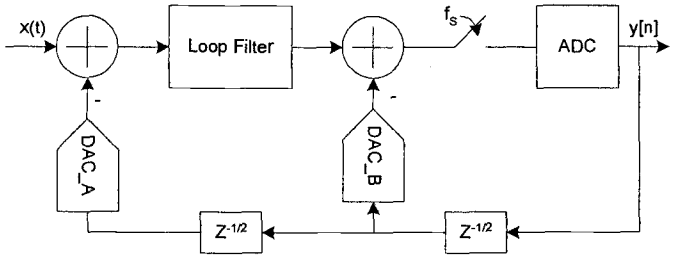


Fig. 4. 5 A loop filter architecture for eliminating excess loop delay

(3) Tiew [K. T. Tiew2005] provides a technique that compensates for the inter-symbol interference and excess loop delay in the 1-bit feedback DAC. The three DACs matching technique is based on acquiring the error signal by using two additional DACs which are matched to the feedback DAC, as shown in Fig 4. 6.

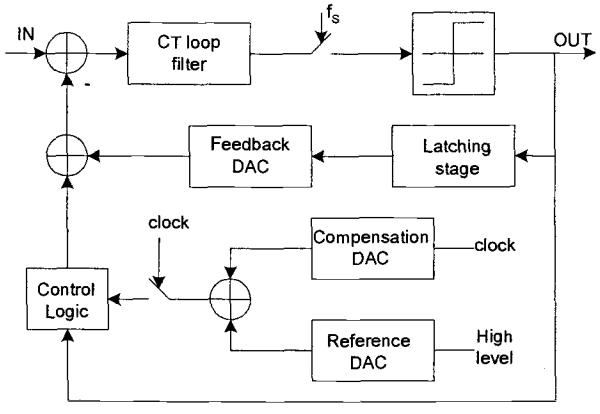


Fig. 4.6 Continuous-time ΔΣ modulator
with three DACs nonidealities compensation

This technique does not require a prior knowledge of the NRZ DAC output pulse in response to the input transition. It could potentially compensate for most of the NRZ DAC non-idealities at a high sampling frequency. In the presence of DAC nonidealities, the peak SNR could be enhanced by using the three DACs nonidealities compensation scheme. It is shown that the technique works well within reasonable mismatch levels among the DACs.

(4) Adaptive DAC pulse-shaping coefficient tuning [W. Gao1997] is based on the nonidealities estimation. Extra feedbacks are added to provide an extra degree of freedom. The pulse-shaping coefficients ($k_{a1}, k_{b1}, k_{a2}, k_{b2}, \ldots$) are tuned in order to obtain a match between the desired prototype transfer function and the actual realized loop transfer function, as shown in Fig. 4.7.

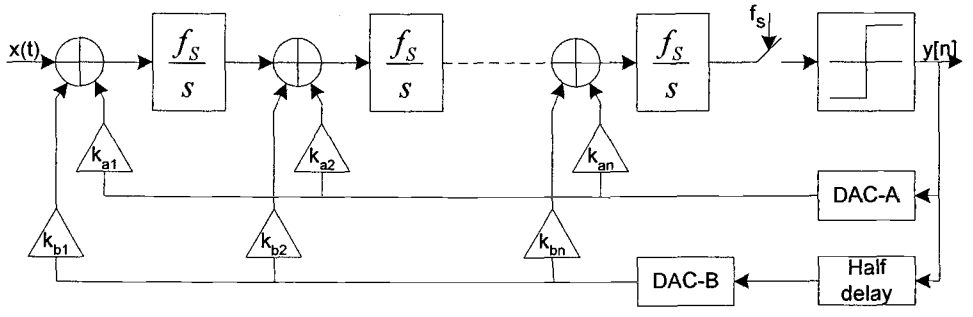


Fig. 4. 7 Continuous-time $\Delta\Sigma$ modulator
with DAC pulse-shaping coefficient tuning

These parameters are tuned based on the amount of excess loop delay. The pulse-shaping tuning strategy can be generalized to correct for other nonidealities.

(5) Based on multi-feedback architecture, we could have used two of NRZ, RZ, and half-return-zero (HRZ), or for that matter any other two different pulses, but these three types are easiest to build in a practical circuit [J. A. Cherry1999A]. RZ DAC pulse and HRZ DAC pulse in feedback are improved [K. P. J. Thormas2005], as shown in Fig. 4. 7.

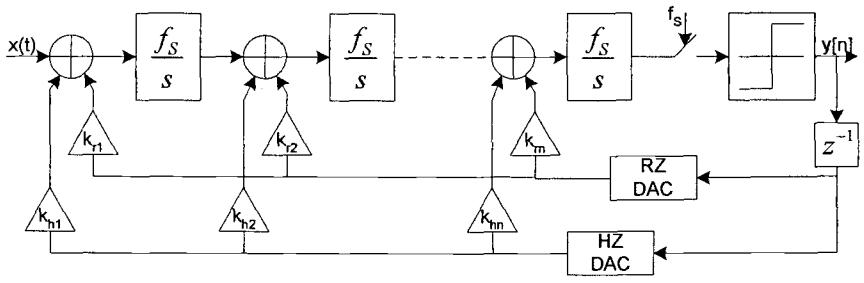


Fig. 4. 8 A continuous-time ΔΣ modulator with HZ DAC and RZ DAC pulses

(6) Based on a CRFB CT ΔΣ modulator with NRZ DAC pulse, Shamsi [H. Shamsi2005] inserts an RZ feedback DAC pulse as shown in Fig 4.8, which RZ feedback DAC pulse is instead of HRZ feedback DAC pulse in [J. A. Cherry1999].

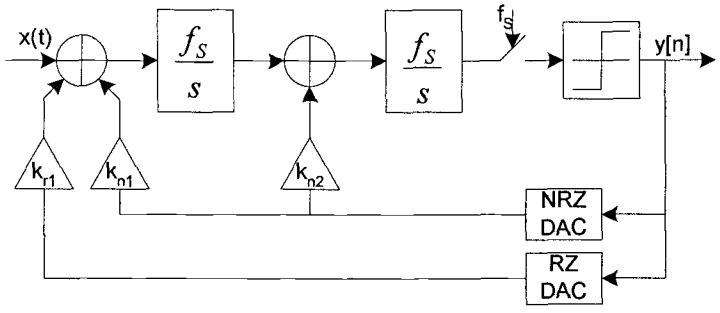


Fig 4.9 The structure of an RZ second order continuous-time ΔΣ modulator

The RZ feedback insertion method can be employed for the excess loop delay compensation.

(7) Additional feedback insertion [A. Latiri2005] adds an extra feedback path before the quantizer to compensate for the excess loop-delay, as shown in Fig. 4.9. This method is valid for both the lowpass and the bandpass ΔΣ modulators.

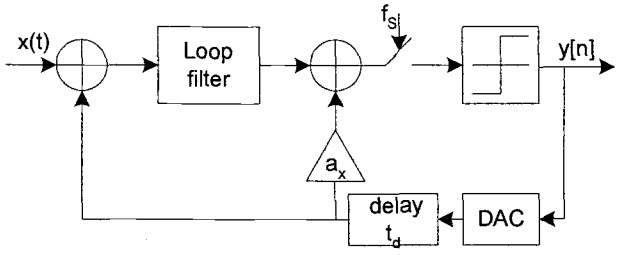


Fig. 4.10 A continuous-time ΔΣ modulator with an additional feedback insertion

From the above, in order to overcome and mitigate excess loop delay, we may select the RZ DAC pulse and purposely add delay in feedback.

4.2 Non-Idealities in DAC (II)---Clock Jitter

Jitter which causes a variation in the width and/or phase of the DAC pulses in a CT ΔΣ modulator degrades modulator performance by whitening the in-band noise [J. A. Cherry1998].

Clock jitter is caused by the random variations of the sampling frequency. It depends on the purity of the clock source. In the CT ΔΣ modulator, as shown in Fig 4.11, there exist two error sources due to a clock jitter. The first one is at the quantizer and the second one is at the feedback DAC. The sampled error entering the system, which occurs at the internal quantizer in the CT case, is rejected by the high in-band loop gain. Hence, the sampled error is neglected in practice. The clock jitter has a great influence on the feedback DAC in CT ΔΣ modulator, because the presence of the clock jitter in the DAC waveform changes both the duration and position of the DAC waveform and adds a random phase white noise to the feedback output signal spectrum, causing a time-variant behavior and whitening the quantization noise in the band of interest and lowering SNR. For low jitter values, the SNR is determined by the thermal noise. When jitter is raised, the performance drops.

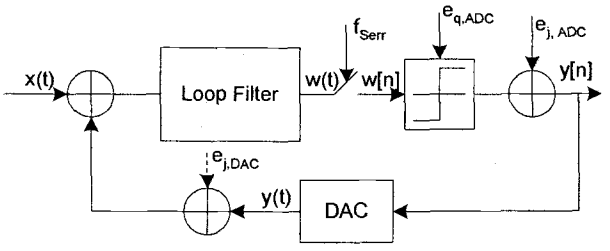


Fig. 4.11 Jitter error sources distribution in typical CT ΔΣ modulator

Due to time jitter in the clock signal, both the width and the position of the feedback pulse change. The pulse-position jitter has much less effect than the pulse-width error. Clock jitter induced by the variations of the pulse-width degrades the performance much more than any other jitter induced errors in the feedback DAC of the CT ΔΣ modulator [M. Ortmanns2005]. This is because pulse-width jitter alters the amount of charge transferred within one clock cycle, while pulse delay jitter only alters the integration over time of a constant amount of charge. It turns out that the latter error is at least first order noise shaped. Pulse-width jitter dominates over phase jitter because it directly affects the feedback charge [R. Schoofs2007]..

Clock Jitter Models

Various models for clock jitter are proposed for CT ΔΣ modulators. In the first model, the clock jitter can be modeled as an additive white noise in the feedback path [H. Shamsi2006C] as shown in Fig 4.12. The model is applicable to different DAC waveforms. A discrete-time modeling technique is proposed [P. M. Chopp2007]. This technique is applicable to different DAC waveforms as well. In [Y. S. Chang2006], an auto-regressive (AR) jitter model is proposed to predict the SNR degradation due to the unwanted phase modulation on DAC output pulses caused by timing error of a clock.

For the graph in the additive noise model proposed [H. Shamsi2006C], $\hat{G}(s)$ and $\hat{H}(s)$ represent the feedforward and feedback gains in a CT $\Delta\Sigma$ modulator in s-domain, respectively.

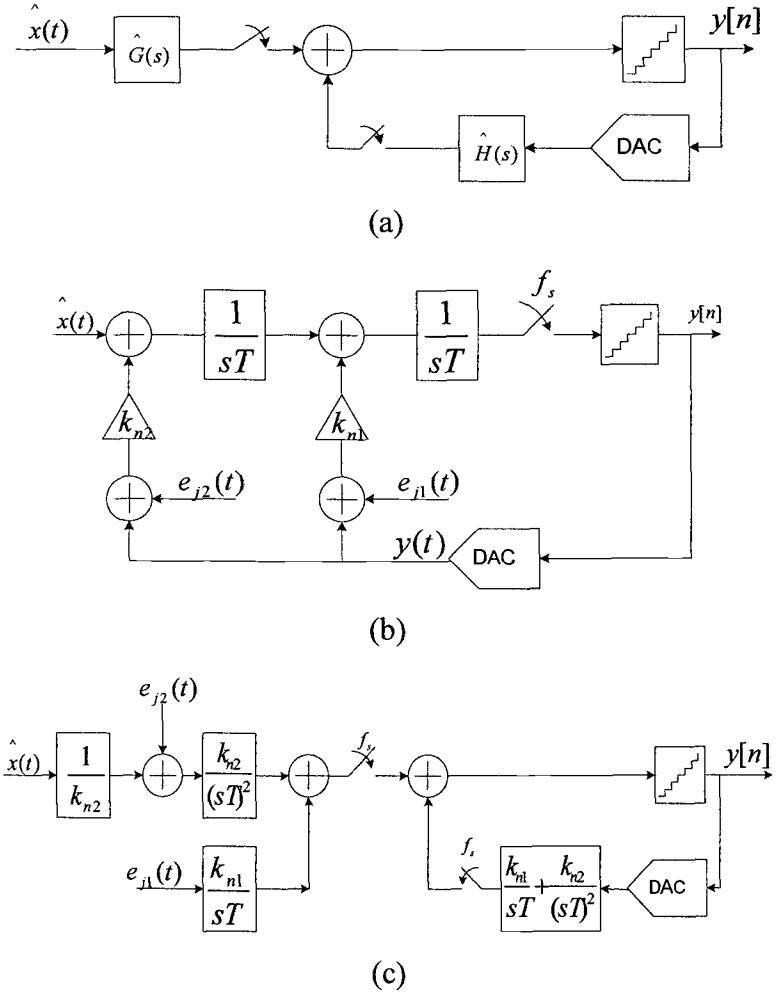


Fig. 4. 12 (a) A general block diagram of a CT $\Delta\Sigma$ modulator. (b) The block diagram modeling the clock jitter effect. (c) The simplification of modeling the clock jitter effects

The clock jitter is modeled as two additive noises, $e_{j1}(t)$ and $e_{j2}(t)$. In order to model the effects of $e_{j1}(t)$ and $e_{j2}(t)$ at the output of the modulator, the model is furthermore simplified, as shown in Fig. 4.12(c). For simplicity, the feedforward gains of $e_{j1}(t)$ and $e_{j2}(t)$ are defined as

$$\hat{G}_1(j2\pi f) = \frac{k_{n1}}{j2\pi fT} \tag{1}$$

$$\hat{G}_2(j2\pi f) = \frac{k_{n2}}{(j2\pi fT)^2} \tag{2}$$

By using the definition of the OSR, the feedforward gains of the additive jitter noise can be expressed as

$$\hat{G}_1(j2\pi f) = \frac{k_{n1} \times OSR \times 2f_B}{j2\pi f} \tag{3}$$

$$\hat{G}_2(j2\pi f) = \frac{k_{n2} \times (OSR \times 2f_B)^2}{(j2\pi f)^2} \tag{4}$$

Since in $\Delta\Sigma$ modulators, the OSR parameter usually varies from 8 to 128, we have

$$|\hat{G}_1(j2\pi f)| << |\hat{G}_2(j2\pi f)| \tag{5}$$

In a good design of the CT $\Delta\Sigma$ modulator, the coefficients of the modulator, k_{n1} and k_{n2} are roughly near to each other, and their difference is low. Therefore, by using (5), the effects of $e_{j1}(t)$ at the output of the modulator can be neglected in the signal band, compared with the effects of $e_{j2}(t)$. For additive jitter noise $e_{j2}(t)$ is transferred to the output of the modulator as the input signal $\hat{x}(t)$.

$$\begin{aligned} P_{jitter} &= [\frac{x(t)}{k_{n2}} + e_{j2}(t)] \times \frac{k_{n2}}{(sT)^2} + [\frac{k_{n1}}{sT} + \frac{k_{n2}}{(sT)^2}] \times y(t) \\ &= x(t) \times \frac{1}{(sT)^2} + [\frac{k_{n1}}{sT} + \frac{k_{n2}}{(sT)^2}] \times y(t) + e_{j2}(t) \times \frac{k_{n2}}{(sT)^2} \end{aligned} \tag{6}$$

$$P_{ieal} = \{[x(t) + k_{n2}y(t)] \times \frac{1}{sT} + k_{n1}y(t)\} \times \frac{1}{sT}$$
$$= x(t) \times (\frac{1}{sT})^2 + [\frac{k_{n2}}{(sT)^2} + \frac{k_{n1}}{sT}] \times y(t) \quad (7)$$

Compared the output of the modulator with jitter (6) with the output of the ideal modulator (7), we know that the clock jitter noise increases the inband power of the modulator. Since in a ΔΣmodulator, the inband frequency products of the input signal of the modulator are transferred to the output of the modulator as they are, so the clock jitter effects at the output of the modulator will be $k_{n2} \times e_{j2}(t)$.

The Suppression of Jitter Effects

There are many methods to suppress the effect of jitter. The jitter has different influence on different DAC waveforms, which include rectangular (NRZ, RZ, HRZ, multi-bit NRZ, multi-bit RZ) pulses, peaking or shaped feedback pulse, triangular feedback waveform, sine-shaped feedback waveform, exponentially decaying feedback pulse and linearly or quadratically sloping feedback waveform[J. Fang2005], [F. Gerfers2006], [J. A. Cherry1999B] [H. Shamsi2006C] [H. Shamsi2006D] [H. Zare-Hoseini2006].

A. Prediction and Analysis

For clock jitter analysis, the noise due to clock jitter in single-loop low pass CT ΔΣ modulators was examined using NRZ DAC waveforms [K. Reddy2006] and [K. Reddy2007]. It was shown that noise transfer functions with optimized zeros result in lower jitter noise than those with all zeros at the origin. It also was shown the jitter noise and quantization noise cannot be reduced simultaneously, and there is an optimum out-of-band which minimizes the total noise. For clock prediction, by using the state-space approach, a precise method for the prediction of the spectrum of the jitter-induced noise is proposed [O. Oliaei2003]. The results are applicable to all types of analog-to-digital or digital-to-analog ΔΣ

modulator. Based on the use of state-space formulation, closed-form expressions were derived for the noise power and SNR [R. Tortosa2005]. It was shown that the jitter-induced noise can be separated into two main components: one depending on the modulator loop filter and the other one due to the input signal. The latter allows us to accurately predict the SNR degradation and to optimize the modulator performance in terms of jitter insensitivity. However, this state-space approach of the clock jitter is complicated since involves the analysis of a time-variant system. Besides, this analysis is limited for RZ DAC waveforms only and its solution is not applicable for NRZ DAC waveforms [H. Shamsi2006C].

B. **Rectangular DAC Waveform**

For rectangular DAC waveform, the jitter-induce noise depends on both the width and the position of the waveform. It has been shown that a variation of the width of the pulse is much worse than all other timing effects, having a larger negative effect on the performance of the modulator.

Rectangular DAC waveforms will be influenced by inter-symbol interference (ISI). If an NRZ signaling is used, a data-dependent transient exists at the DAC's output node due to its parasitic node capacitance. This data-dependent transient causes ISI, which degrades the linearity of the modulator. Even though a NRZ code will not contribute to nonlinearity, in measurements, harmonics were seen due to the NRZ code. These harmonics are the result of asymmetric switching errors in the DAC. Although we may build the DAC fully differentially, which has symmetric DAC rising and falling edges, the transported charge for a "high" or a "low" code is not the same. Mismatch in the DAC latch and mismatch in the sampling switches create different charge injection into the output noise of the DAC. Therefore, a fully differential circuit cannot remove the ISI. For lower frequencies, these effects can be neglected but cannot be ignored for high clock frequencies, such as beyond 100MHz. One approach to reduce the effects of

limited rise and fall times is to use RZ pulses. RZ feedback DACs have been used to mitigate distortion arising from different rise and fall times in NRZ DACs. By using RZ signaling, the DAC's output reset to a constant DC level before the next input comes in, removes the data-dependent transient and thus improves the linearity of the modulator. Although an RZ scheme, in other single-ended designs, ensure that unequal rise and fall times of the DAC pulses do not contribute to the distortion, in a fully differential system unequal rise and fall times appear as a common-mode signal and do not contribute distortion provided there is adequate common-mode rejection. It is well known that the RZ signaling scheme is required in the feedback DAC of a CT $\Delta\Sigma$ modulator for low distortion. Therefore, RZ DAC pulses may overcome ISI.

On the other hand, since the distortion in DAC depends on the preceding symbol, it is signal-dependent and will result in harmonic components and intermodulation products. The distortion in a 1-bit NRZ DAC is caused by ISI as shown in Fig. 4.13.

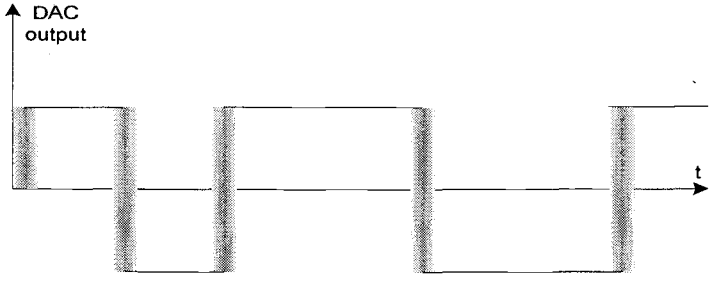


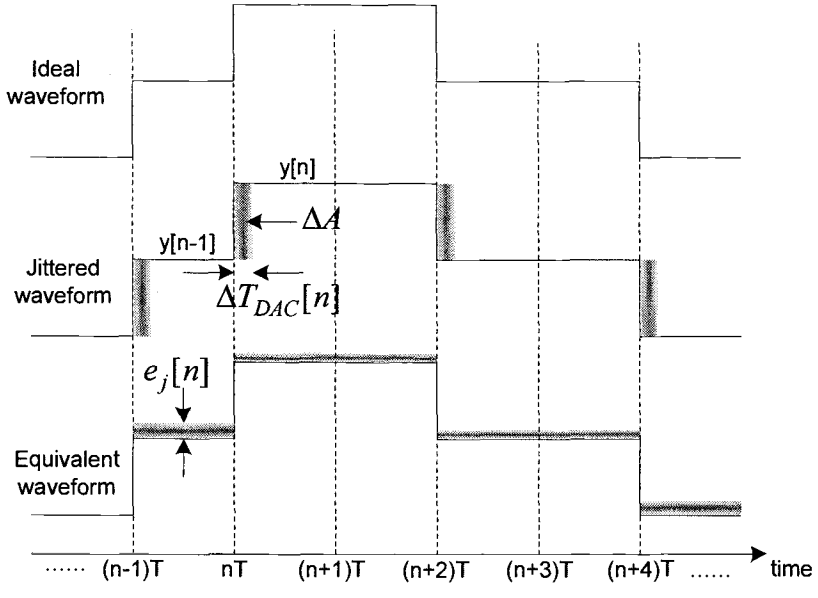
Fig. 4.13 Distortion due to limited rise and fall times of a DAC using NRZ pulse

Because the NRZ DAC pulse transition in practice will have a limited rise and fall time, the effective DAC feedback level will depend on whether or not there is an output transition from one level to the opposite level. In case of a transition, the effective DAC feedback level will be less than that without transition.

To ease the analysis of the effect of the DAC clock jitter on the CT modulator, the timing error of the DAC output signal transition edges is modeled as an equivalent error in the signal magnitude. DAC sampling uncertainties produce errors in the area of the feedback pulses for every sampling period. We can find the equivalent additive error sequence $e_j[n]$ that produces the same area error in a feedback pulse train with ideal timing [S. Paton2004]. If the DAC sampling uncertainty between the $(n-1)^{th}$ and the n^{th} clock period is $\Delta T_{DAC}[n]$, then the equivalent magnitude error $e_j[n]$ for the n^{th} DAC pulse with an ideal timing is given by

$$e_j[n] = \frac{\Delta A}{T} = (y[n] - y[n-1]) \cdot \frac{\Delta T_{DAC}[n]}{T} \tag{8}$$

where ΔA is the area difference between the ideal waveform and the jittered waveform during the n^{th} clock period, and $y[n]$ is the modulator output. The jitter-induced noise for NRZ DAC is illustrated as shown in Fig 4.14 [X. Chen2007].



$$\Delta A = (y[n] - y[n-1])\Delta T_{DAC}[n] \qquad \Delta A = e_j[n] \cdot T$$

Fig. 4. 14 Model of the jitter-induced noise for NRZ DAC

Assuming that the output of the modulator and the clock jitter are independent, the variance of $e_j[n]$ can be expressed as

$$\sigma_{e_j}^2 = \frac{1}{T^2}\sigma_{DAC}^2\sigma_{dy}^2 \tag{9}$$

where $dy[n] = (y[n] - y[n-1])/T$, σ_{DAC}^2 is the standard deviation of the adjacent output difference, and σ_{dy}^2 is the standard deviation of the clock jitter.

In comparison with NRZ waveform, which involves only one transition in each clock period, RZ and HRZ waveform involve two transitions in each clock period. Thus the amplitude of the additive jitter noise of the RZ and HRZ waveforms is twice the amplitude of its NRZ counterpart.

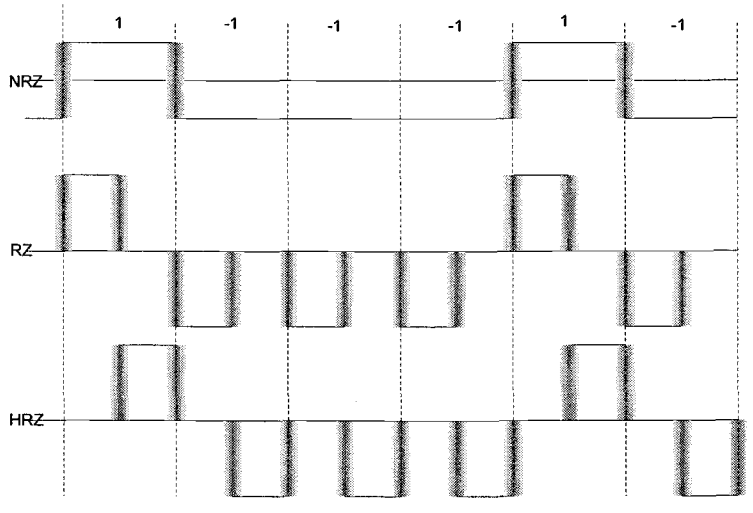


Fig. 4.15 NRZ, RZ, HRZ including jitter

As illustration in Fig. 4.15, assuming that the duty cycle of the RZ and HRZ pulse shaping is 0.5, the amplitude of the RZ DAC and HRZ DAC have to be twice as high as that of the NRZ DAC, to keep the area of the DAC output waveform unchanged.

Furthermore, we may analyze and derive the standard variations of the rectangular feedback DAC pulses [Z. Li2007B].

$$\sigma^2_{e_j,NRZ} = \frac{1}{T^2}\sigma^2_{DAC,NRZ}\sigma^2_{dy} \tag{10}$$

$$\sigma^2_{e_j,RZ} = \frac{2}{T^2}\sigma^2_{DAC,RZ}\sigma^2_{dy} \tag{11}$$

$$\sigma^2_{e_j,HRZ} = \frac{2}{T^2}\sigma^2_{DAC,HRZ}\sigma^2_{dy} \tag{12}$$

From (9), (10) and (11), the jitter noise power can be lowered by reducing the standard deviation of the adjacent modulator output difference. In other words, if the step size of the quantizer is reduced, the jitter noise is lowered. This means that using multi-bit DACs can reduce their sensitivity to clock jitter. For RZ and HRZ DAC, the output error due to jitter is proportional to the output value, not the difference. The coefficient "2" in the above two equations takes into account the fact that both RZ and HRZ DACs are affected by jitter twice in one cycle, at both their rising and falling edges. Multi-bit NRZ DAC should provide best jitter noise immunity than the other two in that its outputs do not need to reset to zero for every clock cycle and hence the average adjacent output difference is smaller. Note that the more levels the quantizer has, the smaller the jitter induced error will be. However, this is only true for multi-bit NRZ DAC, not for RZ and HRZ DACs [Z. Li2007B].

For a NRZ DAC pulse-shaped feedback, assuming the sinusoidal input signal amplitude is A, the oversampling ratio is OSR, the period of the sampling clock is T, the standard deviation of the clock jitter is $\sigma^2_{\Delta y}$, and the standard deviation of the adjacent modulator output difference is $\sigma^2_{DAC,NRZ}$, the signal-to-jitter ratio of a CT $\Delta\Sigma$ modulator can be expressed as [J. A. Cherry2000] [Z. Li2007]

$$SNR_{jitter,NRZ} = \frac{P_s}{P_{jitter}} = \frac{\frac{A^2}{2}}{\sigma_{e_j,NRZ}^2 / OSR} = \frac{OSR \cdot A^2}{2\sigma_{DAC,NRZ}^2 (\frac{\sigma_{\Delta y}}{T})^2} \quad (13)$$

$$SNR_{jitter,RZ} = \frac{P_s}{P_{jitter}} = \frac{\frac{A^2}{2}}{\sigma_{e_j,RZ}^2 / OSR} = \frac{OSR \cdot A^2}{4 \cdot \sigma_{DAC,RZ}^2 (\frac{\sigma_{\Delta y}}{T})^2} \quad (14)$$

$$SNR_{jitter,HRZ} = \frac{P_s}{P_{jitter}} = \frac{\frac{A^2}{2}}{\sigma_{e_j,HRZ}^2 / OSR} = \frac{OSR \cdot A^2}{4 \cdot \sigma_{DAC,HRZ}^2 (\frac{\sigma_{\Delta y}}{T})^2} \quad (15)$$

From (13), (14) and (15) known, the SNR of NRZ DAC is higher than the RZ DAC or HRZ DAC in the same condition.

Traditionally, in single-bit ΔΣ modulators, SNR degradation due to loop-delay may be significantly reduced by using a RZ feedback signal. RZ feedback DACs have been used in continuous-time ΔΣ modulators to overcome ISI due to unequal rising and falling edges of the feedback DAC waveform. The NRZ DAC pulse suffers from ISI. A CT ΔΣ modulator with the RZ DAC pulse is more sensitive to clock jitter than its NRZ counterpart [H. Shamsi2006C]. The RZ DAC may not provide sufficient feedback level, especially at high sampling frequency. The use of RZ DACs in a multi-bit modulator can lead to severe sensitivity to clock jitter when compared to CT ΔΣ modulators with NRZ DACs [S. Yan2004]. So, in the multi-bit CT ΔΣ modulators, an NRZ feedback signal is preference in order to take advantage of their reduced sensitivity to clock jitter [H. Aboushady2004]. A general rule of thumb is that jitter noise in a RZ DAC will have 6dB higher noise level in the signal band [K. T. Tiew2005]

C. Multilevel Pulse Signals by Using FIR DAC and An Additional Delay

Finite impulse response (FIR) filters allow a single-bit modulator to achieve a jitter performance comparable with that of a multi-bit structure without causing harmonic distortion. Multi-bit NRZ DACs reduces the requirement on the clock jitter. Since the jitter-induced noise is proportional to the step height of the DAC waveform, each additional bit of the DAC means that DAC's output height is decreased corresponding to a lower sensitivity to jitter. However, the number of bits of DAC is constrained by the power consumption in quantizer. Increasing the number of DAC's bits introduces linearity problems that need additional circuits for compensations.

As proposed in [O. Oliaei2003C], the FIR filters are implemented using the semi-digital approach. Weighted current sources realize the filter coefficients. The filter in the feedback path of the first integrator is required to have a lowpass filter which smoothes out the feedback waveform by attenuating the high-frequency quantization noise, and reduces the sensitivity to clock jitter in a continuous-time structure. The other filters are required only to ensure the stability of the system. By reducing the power of the feedback signal, the comb filter decreases the jitter-induced noise. Although the output signal of the FIR filters is a multilevel signal, mismatch between current sources only shifts the frequency response of the filters and has no non-linear effect. It has been shown that FIR filters offer significant improvement for both small and large input signals when an NRZ DAC pulse scheme is used. FIR remains valid for higher-order and continuous-time systems including FIR filters in the feedback. However, the sensitivity of the NRZ DAC pulse scheme to the quantizer delay still remains an issue. Furthermore, multi-bit NRZ DAC schemes suffer from the memory effects. Most practical design employ an RZ DAC pulse scheme to avoid the memory effect associated with the NRZ DAC pulse scheme.

In [B. M Putter2004] an FIR filter is added before the DAC to generate a multilevel signal from a two-level quantizer, thus reducing the sensitivity to clock jitter while maintaining high linearity. The feedback DAC is built as a FIRDAC with a flat impulse response, making it an inherently linear multilevel converter. However, the jitter cancellation performance in this technique is signal-dependent. The result for input with high amplitude is worse than low amplitude. Also the excess loop delay is increased, thus may lead to instability.

Tanihata [M. Tanihata2006] proposed a phase shift technique and applied it to multi-level CT $\Delta\Sigma$ modulator as shown in Fig. 4.16. The feedback-signal shaping reduced the sensitivity to the jitter in the sampling timing.

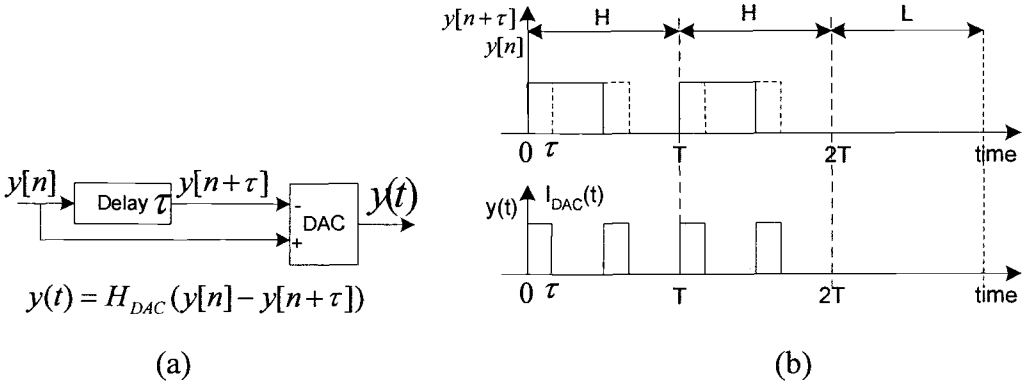


Fig. 4.16 (a) block diagram of phase shift technique (b) input and output of DAC

A delay unit is used to shift the phase of the comparator output, and the delayed signal is subtracted from the original one. This results in a series of pulses with a width equal to one another. Even if there is a jitter, the pulse area remains at the same value, because a constant delay is added and subtracted from the original input.

D. Decaying Pulse Waveform

Decaying DAC waveform is employed to reduce the sensitivity to jitter. It is reported that CT $\Delta\Sigma$ modulators with decaying DAC waveforms to diminish the

influence of pulse width jitter enabled theoretically even lower jitter sensitivity than the DT approach [M. Ortmanns2003]. A modified switched-capacitor (SC) feedback structure reduces the sensitivity to clock jitter due to the sloping pulse form of discharging capacitor, while keeping the advantages of the CT design concerning speed and power in [M. Ortmanns2001] and [M. Ortmanns2002]. In order to retain the advantages of the CT modulators in speed, a resistor was connected in series of the switched capacitor. This DAC structure is called switched-capacitor-resistor (SCR) feedback, which puts only moderate design constrains on the respective integrators [F. Gerfers2006]. The implementation of CT $\Delta\Sigma$ modulator with SCR feedback is based on RZ as shown in Fig. 4.17. At the clock jitter variance, the CT $\Delta\Sigma$ modulator with RZ DAC pulse suffers more penalties in inband noise than NRZ DAC modulator

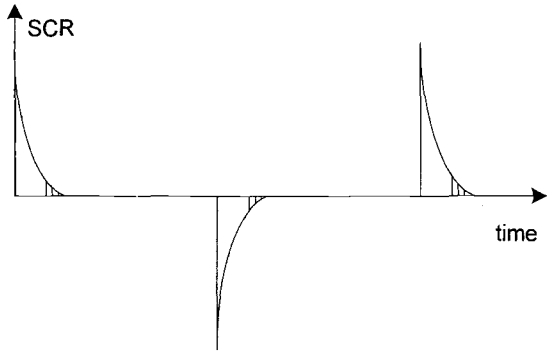


Fig. 4.17 DAC pulse in CT $\Delta\Sigma$ modulator with SCR DAC pulses

Decaying waveform may be different, like exponential, linearly or quadratical sloping DAC waveforms. Fig 4.18 is a quadratic-slope DAC pulse. The shape of the pulse can be chosen according to the jitter requirements, but without the demand of very high speed filters. These decaying pulse shape DAC architectures greatly reduce the sensitivity to clock jitter.

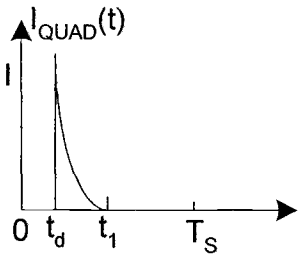


Fig. 4. 18 Quadratic-slope DAC pulse

Compared exponentially decaying feedback pulse with rectangular feedback pulse [R. Schoolfs2007], an exponentially decaying feedback pulse is generated that contains only a small amount of current in the tail at the moment that the clock determines the ending of the pulse.

E. Switched-current feedback pulse, and switched-capacitor feedback pulse

The feedback DAC of the $\Delta\Sigma$ modulator can be implemented by switching charge (switched-capacitor) or switched-currents in [E. J. van der Zwan1996], [R. H. M. van Veldhoven2003] and [P. G. R. Silva2007].

For pulse width jitter in a CT 1-bit $\Delta\Sigma$ modulator with SI DAC, if the clock jitter causes timing errors Δt with variance σ_s^2 causing a variation on the pulse width, the variance of the error charge σ_q^2 transferred per clock cycle T_s can be calculated from

$$\sigma_q^2 = \frac{\sigma_s^2 \cdot I_{DAC}^2}{\delta^2} \tag{16}$$

where I_{DAC} is the amplitude of the feedback current, δ is the pulse width duration per clock cycle. For an NRZ pulse, $\delta = 1$ and for an RZ pulse, $0 < \delta < 1$, as shown in Fig 4.19 .

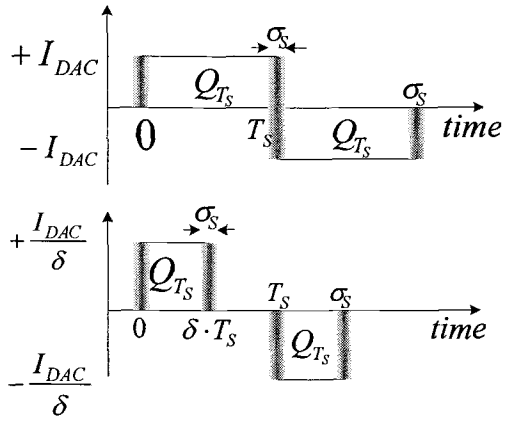


Fig. 4.19 SNR limitation due to jitter on the pulse width (SI)

A disadvantage of the RZ interval is the higher clock frequency needed to create the RZ interval. For example, $\delta = 0.5$, the feedback pulse is two time shorter in time, and to deliver the same amount of charge Q_{T_S} , the pulse has be twice in amplitude. The error charge due to time jitter is expected to be two times higher compared to the NRZ pulse.

The maximum signal amplitude is -3dB compared to the DAC current levels, so the maximum variance of signal charge is

$$Q_{signal}^2 = \frac{I_{DAC}^2 \cdot T_S^2}{4} \tag{17}$$

assuming that the noise power that is introduced by the jitter is white, the maximum achievable SNR due to pulse width jitter is

$$SNR_{JITTER,SI} = 10\log(\frac{\delta \cdot OSR}{4 \cdot f_S^2 \cdot \sigma_S^2}) \tag{18}$$

For pulse width jitter in a continuous-time 1-bit $\Delta\Sigma$ modulator with SC DAC, using an SC feedback circuit can implement the feedback DAC of the modulator. The feedback current in the SC DAC pulse is shown in Fig 4. 20.

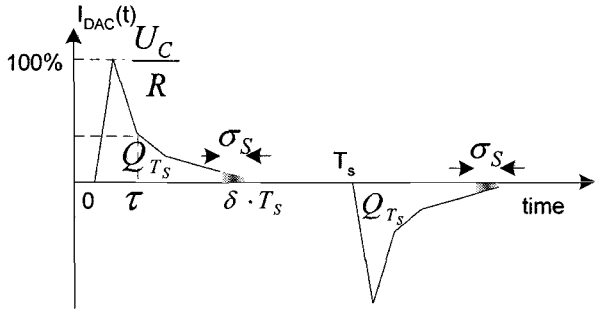


Fig. 4.20 SNR limitation due to jitter on the pulse width (SC)

The integrated feedback charge Q_{T_S} is the same as in the switched current example ($Q_{T_S,SI} = Q_{T_S,SC}$), because the same amount of charge has to be fed back to the input to assure the same gain from input to output of the modulator. From Fig. 4.20, it can be seen that the error charge due to clock jitter is dependent on the settling-time constant $\tau = RC$ of the DAC. Assuming that $\sigma_S << T_S, \tau$, the variance of the error charge transferred per clock cycle T_S can be calculated by

$$\sigma_q^2 = \sigma_S^2 \cdot \delta \cdot \frac{U_C^2}{R^2} (e^{-\frac{T_S \cdot \delta}{\tau}})^2 \tag{19}$$

where U_C is the capacitor voltage. Generally, R is determined by switch resistance and the equivalent input impedance of the integrator stage. The variance of signal charge can be derived by

$$Q_{signal}^2 = \frac{U_C^2 \cdot C^2}{4} (1 - e^{-\frac{T_S \cdot \delta}{\tau}})^2 \tag{20}$$

Simplifying, the SNR limitation due to pulse width jitter in a modulator with SC feedback can be calculated as

$$SNR_{JITTER,SC} = 10\log(\frac{\delta \cdot OSR}{4 \cdot f_S^2 \cdot \sigma_S^2} (\frac{1 - e^{-\frac{T_S \cdot \delta}{\tau}}}{\frac{T_S \cdot \delta}{\tau}})^2) \tag{21}$$

Compared (18) and (21), we find that the improvement from SI to SC DAC pulse is given by

$$\Delta SNR = 20\log(|\frac{(1-e^{\frac{T_S\cdot\delta}{\tau}})}{T_S\cdot\delta/\tau}|) \tag{22}$$

Consequently, the SC DAC is less sensitive to clock jitter than the SI DAC.

For a pulse position jitter in a continuous-time 1-bit $\Delta\Sigma$ modulator, the position of the feedback pulse due to time jitter is shifted in time while keeping its integrated feedback charge Q_{T_S} constant as shown in Fig 4.21.

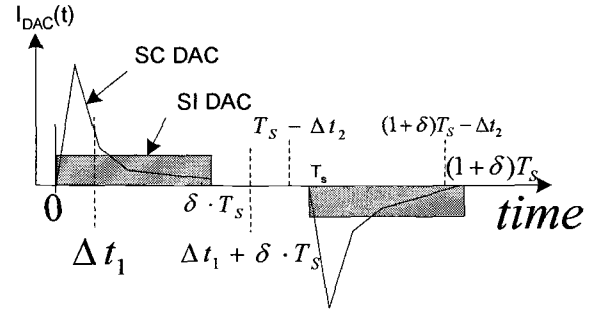


Fig. 4.21 SNR limitation due to jitter on the pulse position (SI and SC)

The SI or SC feedback pulse is shifted over a time $\Delta t_{1,2}$ by the time jitter on the clock. The SNR due to pulse position jitter is calculated by

$$SNR = 10\log(\frac{1}{4\cdot\pi^2\cdot f_b^2\cdot\sigma_S^2}) \tag{23}$$

where f_b is the input signal frequency. At high input frequencies the degradation is the most severe. Pulse position jitter is assumed to have the same effect on both SI and SC feedback $\Delta\Sigma$ modulator.

Based on the SI principle, Zare-Hoseinin [H. Zare-Hoseinin2006A] further improves SI DAC and presents a switched-shaped-current (SSI) technique, which a switched DAC structure is used with an elegant shaped-current output named

SSI. This topology is an SI structure with a shaped current signal, which suppresses the effects of clock-jitter adequately as shown in Fig. 4. 22. It does not impose any power consumption increase in the modulator (as it is near pulse-shaped) and is fully compatible for multi-bit operation.

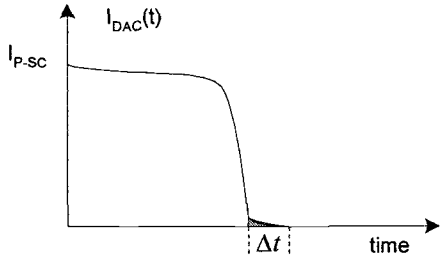


Fig. 4. 22 Switched shaped-current (SSI) DAC pulse

F. Sine-shape DAC waveform

Beilleau [N. Beilleau2006] and Luschas [S. Luschas2002] proved that the sine-shaped feedback is less sensitive to clock jitter compared to rectangular feedbacks as shown in Fig. 4.23. The clock transition takes place when the sine-shaped DAC pulse is at its minimum slope and hence results in a lower charge error [H. Zare-Hoseini2006B]. Both RZ and NRZ Sine-shaped DACs can be used. While the RZ ones are simpler, they have more power in high frequency. On the other hand, the NRZ type is more sophisticated but can achieve a better performance in jitter sensitivity. However, sine-shaped DACs are not as effective as SC DACs. It is difficulty to realize (especially NRZ types) and to reduce the sensitivity to the pulse position jitter, feedback delay, power consumption and noise issues [H. Zare-Hoseini2006B]. Since the input data and the DAC waveform must be synchronized with the clock, Luschas [S. Luschas2002] needs the use of additional synchronization blocks and a phase-locked loop in the implementation.

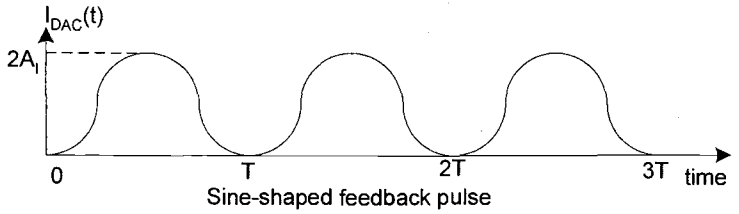
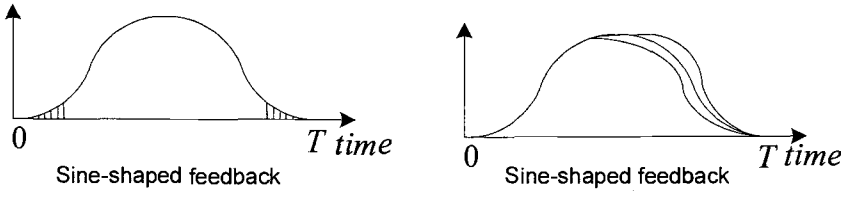


Fig. 4.23 Shaped DAC feedback pulse

To mitigate the effects of switching distortion and clock jitter, Luschas [S. Luschas2004] uses a cosine-shaped feedback waveform which has 2nd order jitter suppression since the amplitude and the slope at the sampling instances *nTs* are zero. Compared with the sine-shaped DAC proposed [S. Luschas2004], the method proposed [A. Latiri2005] does not require the use of synchronization circuitry, as long as the quantizer response-time doesn't exceed half a sample period (RZ). The DAC is designed in a manner that the jitter affects the feedback signal only at the sampling instants. Whereas, for the sine-shaped DAC, the jitter intervenes also at half periods as shown in Fig. 4. 24.



(a) Luschas (b) Lastiri

Fig. 4.24 Jitter effect in Sine-shape DAC

G. Other methods for reducing sensitivity to jitter

Hernandez [L. Hernandez2006] proposed a spectral shaping technique to reduce the jitter sensitivity. It uses an error estimation circuit that spectrally shapes the jitter noise at the output of the modulator. With this technique, the first order shaping of the jitter noise can be achieved. Hernandez [L. Hernandez2003] used *resonators* implemented with transmission lines to desensitize the modulator with

regard to the varying effects in the feedback path such as clock jitter and DAC pulse distortion. Another advantage is the possibility of including excess loop delay into the NTF of the modulator. It is shown in [M. Ortmanns2005C] that clock jitter arises to be a major concern for all $\Delta\Sigma$ architectures (including DT and CT), if low gain bandwidth integrators are used. This is because that the sloping feedback pulses are decelerated. Higher resolutions can be obtained by oversampling more or clocking more slowly [J. A. Cherry1998].

Summary

In Table 4.1 [H. Zare-Hoseini2006B], various techniques to reduce the clock jitter sensitivity are compared in terms of effectiveness, power consumption, speed and ease of realization.

Table 4.1 The performance comparison for clock jitter cancellation techniques

	SI RZ	M-bit NRZ	FIR	SC	RZ SIN	NRZ SIN	SSI
Ease of realization	Best	Good	Bad	Better	Bad	Worst	Good
Jitter cancellation	Worst	Good	Good	Best	Better	Better	Best
Linearity concerns	Best	Worst	Better	Better	Bad	Bad	Better
Speed	Better	Best	Bad	Bad	Better	Better	Better
Power consumption*	Better	Good	Good	Worst	Worst	Bad	Better

*Power consumption of the whole modulator including the DAC.

4.3 Non-Idealities of CT Integrators

In the architecture of a CT $\Delta\Sigma$ modulator, an integrator is implemented with continuous-time integrators, *e.g.*, active-*RC*, *Gm-C*, as shown in Fig. 4.25 [A. Leuciuc2001].

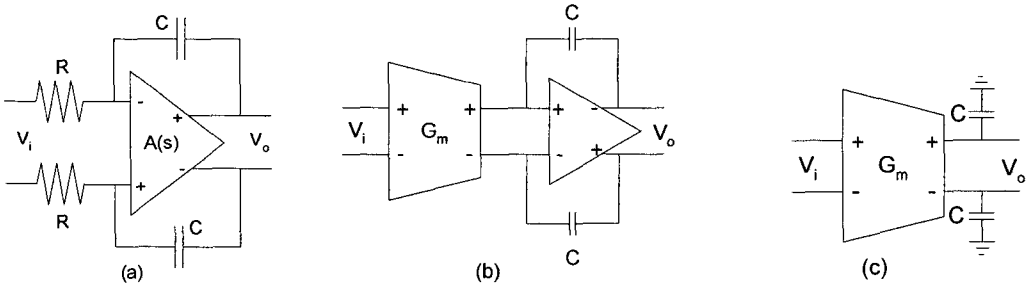


Fig. 4. 25 Continuous-time integrators (a) active-*RC* integrator (b) OTA-opamp-C integrator (c) *Gm-C* integrators

Active-*RC* integrators have excellent linearity and simplicity but have a less frequency range due to the presence of local feedback across the opamp. For *RC*-time constant tuning, the use of small-valued resistors requires large capacitors and increases the power consumption; small-valued capacitors need large value resistors which are difficult to implement in standard processes. An OTA-opamp-C integrator may be derived from active-*RC* configurations by replacing the resistors with operational transconductance amplifiers (OTA). Due to the local feedback, the reduced frequency range is still a problem. However, they have poor linearity because of the nonlinear behavior of the input transconductors. MOSFET-C integrators are a particular case of OTA-opamp-C integrators in which the input transconductor is realized with MOSFETs working in a triode region as voltage controlled resistors. Gm-C integrators have a feed-forward structure and therefore their operating frequency range is much higher compared to the two previous approaches. However, they also have poor linearity and additional linearization circuitry must be included.

The loop filter is very important in ΔΣ modulators, because it defines the signal and noise transfer functions. Any nonidealities of the integrators will directly change the transfer function of the loop filter and therefore degrade the overall performance of the modulator. The nonidealities of an integrator are mainly caused by finite gain and gain bandwidth (GBW) of the amplifiers used to build the integrators. The finite gain and GBW of the opamps in the integrators degrade the SNR of the ΔΣ modulator and may cause stability problems.

In this section, we review the nonidealities of the integrators and the solutions to them. The focus is on active-*RC* integrators since they are most widely used due to the high linearity. There are two approaches to solve the nonidealities of the integrators. One is to use opamps with high gain and GBW. The other approach is to use compensation techniques.

In [F. Chen2006], a single-ended single-input active-*RC* integrator is analyzed Fig.4.26.

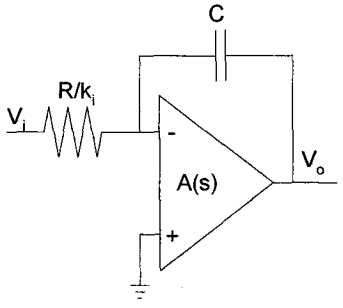


Fig. 4.26 Single-ended single-input active-RC integrator

Assuming the opamp is ideal, the integrator transfer function (*ITF*) can be expressed as

$$ITF(s) = \frac{V_o}{V_i} = -\frac{k_i}{sRC} \tag{24}$$

where RC is the integrator time constant and k_i is the scaling coefficient. However, in fact, a real amplifier has finite DC gain and GBW and can be modeled as

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_p}} = \frac{\omega_t}{s + \omega_p} \tag{25}$$

where A_0 is the DC gain; ω_p is the -3dB frequency; and $\omega_t = A_0 \cdot \omega_p$ is the GBW of the amplifier. Due to the nonidealities of the integrator, the actual ITF is

$$ITF(s) = \frac{V_o}{V_i} = -\frac{k_i}{sRC} \frac{1}{1 + \frac{1}{A(s)}(1 + \frac{k_i}{sRC})} \tag{26}$$

Based on the above equation, the ITF in presence of finite DC gain can be derived as

$$ITF(s) = -\frac{k_i}{sRC} \frac{1}{1 + \frac{1}{A_0}(1 + \frac{k_i}{sRC})} = -\frac{k - \varepsilon}{sRC + \varepsilon} \tag{27}$$

where $\varepsilon = \frac{k_i}{1 + A_0}$ is the error parameter, which is the function of both DC gain A_0 and the scaling coefficient k_i. When $A_0 >> 1$, the amplifier transfer function can be approximated by $A(s) \approx \frac{\omega_t}{s}$. Then equation (26) can be rewritten as

$$ITF(s) = -\frac{k_i}{sRC} \frac{\frac{\omega_t}{\omega_t + k_i / RC}}{1 + \frac{s}{\omega_t + k_i / RC}} \tag{28}$$

Similarly, the ITF of an m-input active-RC integrator, as shown in Fig 4. 27, can be expressed as

$$ITF(s)|_i = -\frac{1}{R_i}\frac{1}{\frac{C}{A_0\omega_p}s^2 + \left(\frac{(A_0+1)C}{A_0} + \frac{1}{A_0\omega_P}(\sum_{k=1}^{n}\frac{1}{R_k})\right)s + \frac{1}{A_0}\left(\sum_{k=1}^{n}\frac{1}{R_k}\right)} \quad (29)$$

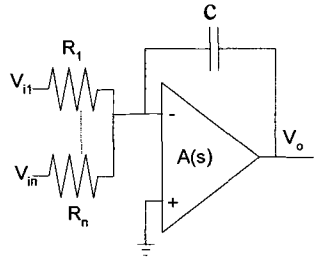


Fig. 4.27 Single-ended n-input active RC-integrator

It is reasonable to approximate the real opamp's characteristics with a single-pole model as follows:

$$A(s) = \frac{A_0}{1+\frac{s}{\omega_p}} = \frac{A_0\cdot\omega_p}{\omega_p+s} = \frac{\omega_t}{\omega_p+s} \approx \frac{\omega_t}{s} \quad (30)$$

where ω_t is unit gain bandwidth, which is equal to $A_0\cdot\omega_p$. The equation (28) can be simplified as

$$ITF(s)|_i = -\frac{1}{R_i}\frac{1}{\frac{C}{A_0\omega_p}s^2 + \left(C + \frac{1}{A_0\omega_P}(\sum_{k=1}^{n}\frac{1}{R_k})\right)s}$$

$$= -\frac{1}{sR_iC}\cdot\frac{1-\frac{\left(\sum_{k=1}^{n}\frac{1}{R_kC}\right)}{\omega_t+\left(\sum_{k=1}^{n}\frac{1}{R_kC}\right)}}{1+\frac{s}{\omega_t+\left(\sum_{k=1}^{n}\frac{1}{R_kC}\right)}} \quad (31)$$

As shown in (31), the opamp non-ideality leads to a gain error and a non-dominant pole in the ITF. For convenience, we normalize the *RC* time constants of the integrators to the sampling period T_s of the CT $\Delta\Sigma$ modulator

$$\frac{1}{R_k C} = \frac{k_k}{T_s} = k_k f_s \tag{32}$$

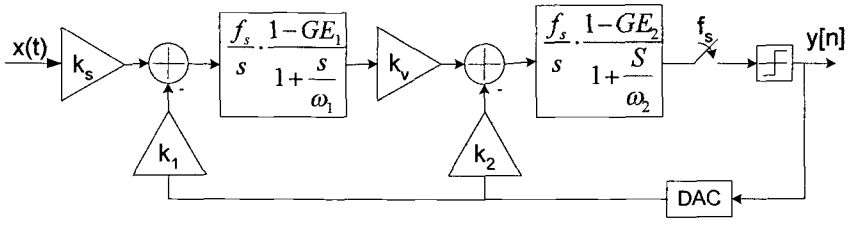
We define the gain error (*GE*) and the pole frequency ω as

$$GE = \frac{\omega_t}{\omega_t + \sum_{k=1}^{n} | k_k \cdot f_s |} \text{ and } \omega = \omega_t + \sum_{k=1}^{n} | k_k \cdot f_s | \tag{33}$$

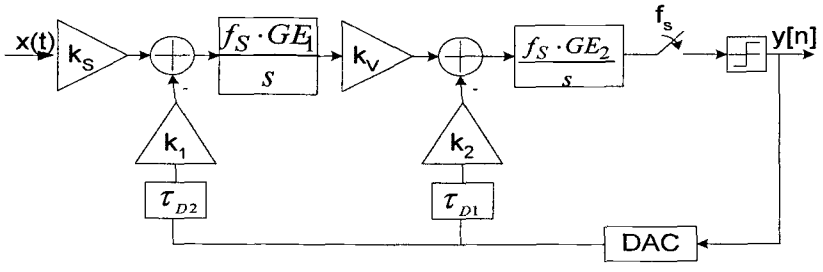
The ITF of the non-ideal integrator can be expressed as

$$ITF(s)|_{V_{ii} \sim V_o} = -\frac{k_i}{sT_s} \frac{1-GE}{1+\frac{s}{\omega}} \tag{34}$$

In order to further understand the influence of gain error on a $\Delta\Sigma$ modulator, we will use a model to simplify the analysis, only RZ and NRZ feedback DAC pulses are regarded, as shown in Fig. 4.28 [M. Ortmanns2004].



(a) Integrators with gain error and second pole



(b) Complete model for finite GBW modulator

Fig. 4.28. Derivation of a finite GBW model for a second-order modulator.

Fig.4.28 (a) replaces the ITF blocks by the expressions given in (30). The feedback transfer functions are scaled single or double-pole systems. Due to the rectangular form of the feedback pulse under consideration, the combination of these feedback transfer functions with the integrators in the forward path results in nonideal integrator outputs as delayed slopes. It can be seen that the delayed slope, i.e., the additional feedback poles, can be modeled as integrator step response with a fixed time delay τ_D. This approximation results in a complete model of a second-order modulator with finite GBW amplifiers as shown in Fig. 4. 28 (b). It has been shown that finite GBW of the opamp non-idealities in the integrators can be modeled as integrator gain errors and additional integrator poles and zeros. The additional poles have a similar influence as a feedback. It has the same effect as the excess loop delay, which is different for each feedback path and depends on the number of integrators seen by that loop. Due to this delay, the modulator performance suffers in terms of increased in-band noise, and reduced maximum stable amplitude, and dynamic range.

For rectangular feedback the non-dominant pole can be modeled as feedback delay. Thus, a compensation is possible as correction of gain-errors and a modified compensation for excess loop delay [M. Ortmanns2004]. A possible technique for the error compensation may be delay compensation by coefficient tuning, or by additional feedback parameters or concurrent delay and gain error compensation by coefficient tuning. It has been shown that for low values of the GBW, the main performance degradation is caused by the induced loop delays, having the worst influence on modulators with NRZ feedback DAC. Sobot replaced the tunable loop filter transfer function with the filter function with fractional delays in $\Delta\Sigma$ modulator [R. Sobot2006]. The architecture exploits the fact the overall $\Delta\Sigma$ loop delay (including the excess loop delay) must be equal to a fractional multiple of the sampling period, which is matched by the CT loop

filter transfer function. A consequence of this approach is that the excess loop delay can be incorporated in the transfer function.

To reduce the effect of the non-ideal opamp, coefficient pre-distortion technique is used to correct gain error and extra resistors are connected in series with the capacitors to cancel poles [F. Chen2006]

Variation of *RC* time constant

Since coefficients in the loop filter are determined by the absolute RC time constant, which may vary greatly due to process variation, and resistance and tranconductance values change values change substantially with temperature, continuous-time ΔΣ modulator is its high sensitivity to process variations, power supply variation, sampling rate variation and temperature variation [D. A. Johns1997]. Thus, when we design a continuous-time filter, tuning circuitry is needed to compensate for change in *RC* product and modify transconductance value such that the resulting overall time constants are set to known values. We may directly tune a continuous-time integrated filter without or with looking at its output signal. The purpose of tuning is that a deviation of the time constants from their nominal values is usually unacceptable. The tuning process has two aspects: 1) estimating the deviation in time constants of the loop filter from the nominal value; 2) adjusting the loop filter components in a manner as to bring the time constants close to the nominal value [D. A. Johns1997].

The large *RC* time constant variations in CT ΔΣ modulators arise from large absolute tolerances of integrated resistors Δ_R and capacitors Δ_C, and the relative tolerances ε_R and ε_C [F. Gerfers2003]. The absolute tolerance $\Delta_{R,C}$ represents the variations of the resistors and capacitors from chip to chip, whereas the relative mismatches $\varepsilon_{R,C}$ represent the derivation from device to device on one chip. Both

errors act like a mismatch in the scaling coefficients and they strongly depend on dimensions and process. Considering the influence of the absolute tolerance $\Delta_{R,C}$, the *ITF* becomes

$$ITF_{\Delta_{R,C}} = \frac{1}{sRC} \approx \frac{f_s}{s(1+\Delta_{R,C})} \tag{35}$$

where $\Delta_{R,C} \in \pm\sqrt{(\Delta_R)^2 + (\Delta_C)^2}$. Considering this effect, the total in-band noise (IBN) at the output of a single-loop modulator of order M is

$$IBN(\Delta_{R,C}) \approx \frac{\Delta^2}{12k_1^2 k_q^2} \cdot \frac{\pi^{2M-1}(1+\Delta_{R,C})^{2M-1}}{(2M+1)\cdot OSR^{2M+1}} \tag{36}$$

For the third-order single-loop modulator, it can be seen that for $\Delta_{R,C} = \pm 20\%$, there is an IBN degradation of 3~4dB. Considering the influence of the relative tolerances $\varepsilon_{R,C}$, by using the same way as the absolute accuracy, Gerfers shows that the relative mismatch is less influence for CT low-pass single-loop $\Delta\Sigma$ modulators [F. Gerfers2003].

In many applications, such as the high resolution $\Delta\Sigma$ modulators and anti-aliasing filters, high linearity, low power, and small silicon area are more important design concerns than the tuning precision. The typical tuning accuracy required in those applications can be relaxed to around $\pm 10\%$. That is, a $\pm 10\%$ variation in the integrator time constant can be tolerated. Therefore, Xia proposed an improved tuning circuit to preserve the linearity of the circuit-to-be-tuned [B. Xia2004]. This new discrete *RC* time constant auto-tuning structure generates a control word and sets on-chip capacitors to obtain an *RC* time-constant accuracy of $\pm 2-10\%$. This scheme reduces accuracy to get high linearity.

The *RC* time constant sensitivity problem in CT $\Delta\Sigma$ modulator is very important. When *RC* time constant becomes smaller, a better *SQNR* may result due to the higher loop filter gain. However, the system becomes unstable when the

normalized time constant *RC* decreases to approximately 0.88 [S. Yan2004], 0.76 [X. Chen2007], 0.94 [Z. Li2007] 0.85 [T. Song2006-1] and [B. Xia2004]. If the *RC* time constant is larger than nominal, although the modulators are more stable, less efficient noise shaping results due to smaller loop filter gain, and hence the *SQNR* performance degrades [S. Yan2004].

Many techniques may tune the *RC*-time constant in a CT $\Delta\Sigma$ modulator.

1. Based on the principle that the in-band gain and the out-of-band performance of a modulator are related, Pavan provides a digital technique for estimating and correcting time constant shifts in CT $\Delta\Sigma$ modulators [S. Pavan2007]. The variance of the high pass filtered output stream of the modulator was seen to be an indicator of the time constants (or k_p) of the loop filter. An alternative indicator is the variance of $p(n) \equiv v(n) - v(n-1)$, where $v(n)$ is the modulator output, which is a good indicator of the modulator *RC* time constants. The tuning technique does not use any extra analog components.
2. Based on the idea of minimizing the variance of the in-band noise, Breems compensates for the *RC* time constant spread [L. J. Breems2007]. An automatic capacitor trimming scheme is employed to tune the time constants of the active-RC integrators. The integrator feedback capacitors are implemented as banks of digitally switched binary weight elements. The digital control code is provided by a calibrating circuit which compares a replica of the RC time constant to the period of the input reference clock.
3. A discrete capacitor tuning scheme is employed [S. Yan2004] and [Z. Li2007] to calibrate the time constant of the active-RC and gm-C integrators.
4. In [K. Nguyen2005], its compensation method is similar with a master-slave tuning scheme. It adjusts both the integrating capacitors and the

integration period. It uses the on-chip reference voltage to calibrate the master tuning circuits. To compensate for larger *RC* value due to process variation, or higher modulator clock frequency, the integrating capacitors of the CT first stage are discretely sized down by a finite-state machine. For a smaller *RC* value, or a lower modulator clock frequency, the integration interval is kept constant.

4.4 Errors of the Internal Quantizer

Quantizer clock jitter and quantizer metastability are the two major factors which cause a variation in the width of the DAC pulses in a CT ΔΣ modulator to degrade modulator performance by whitening the in-band noise [J. A. Cherry1998]. CT ΔΣ modulators are especially sensitive to quantizer metastability.

The quantizer metastability refers to the fact that the quantizer inputs with a small magnitude takes longer to resolve than inputs with a large magnitude [J. A. Cherry1999B]. The quantizer is a regenerative circuit with finite regeneration gain. The regeneration means that the quantizer has recovery and amplification for the input signal. Besides the signal magnitude, the slope of the input signal also affects the regeneration time. The input to the quantizer in a ΔΣ modulator is decorrelated from the modulator input to the degree that it appears random. An actual quantizer does not instantaneously make a decision for an input signal. Hence, the times when the quantizer input is near zero also appear random. This means that even with a perfectly uniform sampling clock, at certain unpredictable sampling instants, slightly more charge is transferred for the previous clock period, and slightly less for the next period. The effect is to modulate out-of-band noise into the signal band and degrade converter resolution. Therefore, the quantizer metastability can result in worsened sensitivity of an otherwise ideal CT ΔΣ modulator to small input levels [J. A. Cherry1999B].

To describe a real quantizer performance effect, Cherry characterizes metastability in a practical integrated quantizer using the quantizer output zero-crossing time and rise time as a function of both quantizer input voltage and the slope of the input voltage at the sampling instant, and predicts the maximum-achievable performance of a practical CT $\Delta\Sigma$ modulator given jitter and metastability constraints [J. A. Cherry1999B].

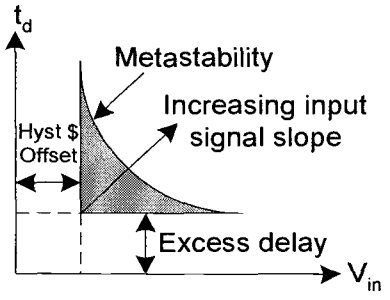


Fig. 4.29 Real quantizer characteristics of a comparator.

A real quantizer, seen in Fig. 4.29, where t_d refers to the delay of the comparator and V_{in} is the input signal amplitude, exhibits the effects of excess loop delay, hysteresis and metastability simultaneously. Excess loop delay is a nonzero delay between the quantizer clock and the feedback output and is caused by finite transistor switching speed. It results in higher in-band quantization noise and may lead to instability. Hysteresis refers to the memory characteristics of a quantizer, which means the quantizer sometimes does not make a decision to change the output bit when it should, but the performance of a $\Delta\Sigma$ modulator does not suffer much because of hysteresis. Like a DC offset, the hysteresis will also degrade the noise performance of the $\Delta\Sigma$ modulators. In order to reduce the hysteresis, the comparator should be reset before entering the regeneration period. Metastability causes quantizer inputs near zero to take longer to resolve; metastability severity is proportional to the area under the curve. Quantizer metastability imposes two additional DR-limiting effects on top of those caused by excess loop delay and hysteresis. First, at low input amplitudes, there is the output limit cycle behavior.

Second, at other input amplitudes, spectral whitening occurs, metastability introduces a random variation in the feedback charge, and this folds out-of-band noise into the signal band in the same way clock jitter does.

The effects of comparator metastability can be analyzed by modeling any metastability delay as a noise signal that is added to the outputs of the DAC [E. H. Dagher2004]. To determine the variance of this noise signal, the comparator with metastability is modeled as $Ke^{-s(T_q+\Delta t(n))}$, where K is the comparator's variable gain, T_q is the comparator's average delay, and $\Delta t(n)$ is assumed to be an independent zero mean random signal for a busy comparator input signal. Because the error introduced by comparator metastability is only present when the comparator transitions between stable states, the equivalent metastability error current $i_e(n)$ at the output of each DAC is

$$i_e(n) = [y(n) - y(n-1)]\frac{\Delta t(n)}{T} I_{DAC} \tag{37}$$

where T is the $\Delta\Sigma$ modulator's sampling period, $y(n)$ is the $\Delta\Sigma$ modulator's output at time nT, and I_{DAC} is the DAC's output current. The variance $\sigma_{i_e}^2$ of this error current $i_e(n)$ is

$$\sigma_{i_e}^2 \approx \sigma_{\Delta y}^2 \frac{\sigma_{\Delta t}^2}{T^2} I_{DAC}^2 \tag{38}$$

where $\sigma_{\Delta y}^2$ is the variance of [y(n)-y(n-1)] and $\sigma_{\Delta t}^2$ is the variance of the $\Delta t(n)$.

Because the DAC's output is added to the $\Delta\Sigma$ modulator's input, the metastability noise at the output of DAC is shaped by the $\Delta\Sigma$ modulator's STF. Assuming that the $\Delta\Sigma$ modulator's input is a full-scale sinusoidal signal with power $\sigma_S^2 = I_{IN}^2/2$, then the $\Delta\Sigma$ modulator's signal to metastability noise ratio (SMNR) over the frequency band of interest is

$$SMNR = 10\log_{10}\left(\frac{\sigma_S^2}{\frac{\sigma_{i_e}^2}{OSR}}\right) = 10\log_{10}\left(\frac{OSR \times \frac{I_{IN}^2}{2}}{\sigma_{\Delta y}^2 \frac{\sigma_{\Delta t}^2}{T^2} I_{DAC}^2}\right) \tag{39}$$

Or equivalently

$$\sigma_{\Delta t}^2 = \frac{OSR \times \frac{I_{IN}^2}{2}}{\sigma_{\Delta y}^2 \frac{1}{T^2} I_{DAC}^2 \times 10^{\frac{SMNR}{10}}}. \tag{40}$$

Typically, $\sigma_{\Delta y}^2$ is estimated empirically by simulation a $\Delta\Sigma$ modulator with an ideal comparator that has no metastability.

Several methods were proposed [J. A. Cherry1999B] to mitigate the performance loss due to the metastability, such as scaling the quantizer input to have a span as large as possible; decreasing the regeneration time by inserting a preamplifier stage and increasing the gain-bandwidth product of the regenerative circuits; adding additional latching stages and using improved modulator architectures. A new regenerative circuit architecture is provided [Y. L. Guillou2006] to reduce the effect of quantizer metastability. The regenerative circuit can be described as a single-pole system where the voltage difference at $t = n \cdot T_s$ increases with a time constant inversely proportional to the GBW product of the system $V_o[n] = I_i[n]e^{GBW \cdot t}$, where $I_i[n]$ and $V_o[n]$ are the input and output quantizer, respectively. For a fixed GBW product, the higher the input level of the quantizer, the faster its output $V_o[n]$ is above V_{TH}. In case of a fixed quantizer input $I_i[n]$ the larger the GBW product, the faster the quantizer.

A new sampling circuit topology was described in [A.Strak2004]. This circuit shapes clock-jitter-induced sampling noise in much the same way as $\Delta\Sigma$ ADC shapes quantization noise. The sampling circuit consists of a CT integrator

followed by two switches: one for the output and one for the feedback. The main benefit of this converter is that its sampling noise due to jitter is, to a large extent, independent of the signal frequency. This means that as the signal frequency increases, the new sampling circuit maintains high sampling accuracy. It obtains as well a high inband signal-to-jitter-noise ratio (SJNR). By using two flash ADCs in parallel [S. Benabid2004], Benadid offers the fastest conversion rates to allow doubled sampling frequency, 1.2 GHz. But it has the disadvantage of high input capacitance as the number of comparators increases exponentially with the number of bits. Using a fast-settling switched-voltage technique implements for single-bit quantizer topology, Schoofs [R. Schoofs07] incorporates a lock feedback path that improves stability. This technique for local feedback pulses in the quantizer deals with the high-speed requirements.

One way to counteract quantizer clock jitter and metastability is to use a multi-bit feedback loop which requires a (high resolution) multi-bit quantizer. Using a multi-bit quantizer (as opposed to a single bit quantizer) in the loop has the following several advantages [P. Sankar2007].

- The more levels, the lower the quantization noise. This enhances the dynamic range.
- The modulator becomes a better approximation to a linear system, which makes the modulators intrinsically more stable. The noise transfer function (NTF) of the loop can be made more aggressive without compromising stability.
- The resolution of $\Delta\Sigma$ ADCs is increased because the resolution is proportional to the quantizer resolution.
- The jitter requirements may be reduced. If a NRZ feedback DAC is used, multi-bit operation results in a reduced sensitivity to clock jitter. Usually, the noise produced by clock jitter is directly proportional to the quantization step.

- Each additional bit in the quantizer and in the DAC decreases the DAC step height, with a corresponding increase in the resolution of the ADC.
- Since the quantization error is smaller (for the same NTF), the slew rate requirements on the integrators of the loop filter are greatly relaxed. Hence, they can operate on a lower bias current.

From the above reasoning, it is clear that the number of bits in the quantizer should be as high as possible.

The drawback of a multi-bit solution is that the power consumption of the quantizer is doubled for every additional bit, and needs a big die area. In addition, most implementations of multi-bit $\Delta\Sigma$ modulators use a flash ADC as a quantizer. The low power supply and reference voltage affect the resolution of the flash ADC.

There are several ways to overcome these drawbacks. First, a high-resolution quantizer with a reduced number of comparators in the multi-bit quantizer can be implemented [J. D. Maeyer07]. The basic idea of the new modulator is to decrease the signal range at the input of the quantizer. Based on three possible architectures that realize this concept, the new architecture as compared to conventional modulator achieves the same performance, with much less comparators in the quantizer. Secondly, a new pulse-width CT $\Delta\Sigma$ modulator is implemented by replacing the quantizer and sampler of CT multi-bit $\Delta\Sigma$ modulator for a comparator with hysteresis and a new sampler clocked at higher rate [F. Colodro2005]. The cost is that the new pulse-width modulator has to be clocked at f_S while the conventional is operated at a frequency F times smaller ($F = f_S / f_{\max}$). So, the complexity is relaxed for this structure at expense of higher sampling frequency. Thirdly, the power consumption can be considerably reduced by using a tracking ADC composed of three comparators with interpolation instead of using a 4-bit flash quantizer [L. Dorrer2005]. It is thus

seen that multi-bit modulation results in a reduced power dissipation. Fourthly, a successive approximation (SA) ADC can be used [L. Samid2006], which is simple and has small die area. One of the advantages of using SA-ADC as multi-bit quantizer is the possibility of using a linearization technique in the feedback DAC of the modulator with a NRZ-feedback signal, where the multi-bit SA-ADC and feedback DAC can operate simultaneously. The excess loop delay will be avoided. In order to reach a high SNR and to reduce the clock jitter sensitivity, increasing the quantizer bits does not drastically increase the power dissipation and the area of the modulator.

5 IMPLEMENTATION OF CT $\Delta\Sigma$ MODULATORS

This section reviews the state-of-art of CT $\Delta\Sigma$ modulator implementations. It will include the key factors in system level design and circuit implementations. Four design implementations will be presented.

5.1 System Architecture Considerations

There are many factors to consider in system design, including design methodology, topology (single-stage and multi-stage), loop filter, DAC, sampler and quantizer, performances, and so on.

Figure of Merit (FOM)

Figure of merit (FOM) is a quantity used to characterize the performance of the $\Delta\Sigma$ ADCs. The FOM takes the overall power consumption P, the dynamic range, supply voltage, and the signal bandwidth f_B into account from different abstraction levels, and is defined as

$$FOM = \frac{P}{2^B \cdot 2f_B} \tag{1}$$

where B is the conversion resolution in bits. The minimal FOM represents the optimal structure referenced to the oversampling ratio $OSR = f_S/(2f_B)$ and overall power consumption that fulfils the specifications [F. Gerfers2003].

Dynamic Range (DR)

Linearity limits the value of the *largest* useful signals that can occur in the filter, whereas noise limits the value of the *smallest* useful signals. Thus, we find that linearity and noise together determine the useful dynamic range of a filter [D. A. Johns1997].

The dynamic range of the system is defined as the difference between the smallest and the largest input levels (in decibels) which give $SNR \geq 0$ [J. A. Cherry1999A]. At low input levels, SNR is limited by inband noise (IBN), while a large-enough input level eventually compromises the linearity and/or the stability of the modulator. There exists a maximum stable input amplitude (MSA); the DR may be found from the IBN and the MSA.

The resolution of an oversampling $\Delta\Sigma$ A/D modulator is a function of the OSR, noise-shaping loop order (L) and the number of quantizer levels (N) [Z. Li2007], as expressed by

$$DR = \frac{P_S}{P_N} = \frac{3}{2} \times (\frac{2L+1}{\pi^{2L}}) \times (2^N - 1)^2 \times OSR^{2L+1} \qquad (2)$$

These parameters were selected to obtain the DR well above the required limit. This allows the NTF of the CT modulator to be adapted to a more robust design at the expense of a lower DR [S. Paton2004]. Although (2) is valid only if the NTF is $(1-z^{-1})^L$, which is not true for most wideband, high resolution $\Delta\Sigma$ modulators, it does give a qualitative guidance on selecting OSR, L, and N in the system level design [Z. Li2007]. The DR at a high OSR is greater than at a low OSR [J. A. Cherry1999]. The power efficiency is required to achieve much higher dynamic range/bandwidth specifications within the power budget.

Several noise sources can degrade the dynamic range of a CT $\Delta\Sigma$ modulator, including noise in the reference voltage of the feedback DAC, noise introduced by clock jitter, quantization noise generated by the quantizer, and noise (*1/f* and thermal) from the circuitry [R. H. M. V. Veldhoven2002]. On the other hand, the dynamic range of the modulator depends on excess loop delay. As excess loop delay increases, the MSA reduces. Since DR is exactly the difference between MSA and adjusted IBN, the dynamic range also reduces [J. A. Cherry1999]. The circuit noise in the loop filter of the $\Delta\Sigma$ modulator usually originates from the

input stage. The noise contributions of subsequent stages are noise-shaped, whereas the ones closer to the comparator experience higher in-band attenuation. It is shown that pulse-area variations, which comprises the pulse-width variation and the pulse-height variation, cause mixing of quantization noise into the pass-band, thereby reducing the dynamic range of the ADC. It is shown that high jitter frequency components corresponding to large quantization noise value causes a larger dynamic range degradation than low jitter frequency components [B. Baggini2006].

Total Harmonic Distortion (THD)

The total harmonic distortion (THD) of a signal is defined as the ratio of the total power of the second and higher harmonic components to the power of the fundamental signal component [D. A. Johns1997]. The THD is found using the following relation:

$$THD = 10\log(\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}{V_f^2}) \text{ in dB} \tag{3}$$

where V_f is the amplitude of the fundamental and V_{hi} is the amplitude of the i^{th} harmonic component. Sometimes, the THD is presented as a percentage value. In this case,

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \cdots}}{V_f} \times 100 \tag{4}$$

For practical reasons, typically the power of only the first few harmonics (say, the first 5) are included since the distortion components usually fall off quickly for higher harmonics.

A meaningful measurement must include the bandwidth of measurement. *THD+N* means total harmonic distortion power plus noise power. It is defined to be the ratio between the output signal with and without the sine wave input:

$$THD + N = \frac{P + N}{S} \tag{5}$$

where P is total harmonic distortion powers, N is noise power, and S is total output power. This measurement includes effects from intermodulation distortion, interference, and so on, instead of just harmonic distortion.

Third-Order Intercept Point (IP3)

Intermodulation distortion (IMD) is used to measure the linearity of amplifiers, gain blocks, mixers, and filters. Two tone IMD is measured by applying two spectrally pure sinewaves to the ADC at frequencies f_1 and f_2, usually relatively close together. The amplitude of each tone is set slightly more than 6 dB below full-scale so that the ADC does not clip when the two tones add in-phase. The locations of the second and third-order products are shown in Fig 5. 1 [W. Kester2006].

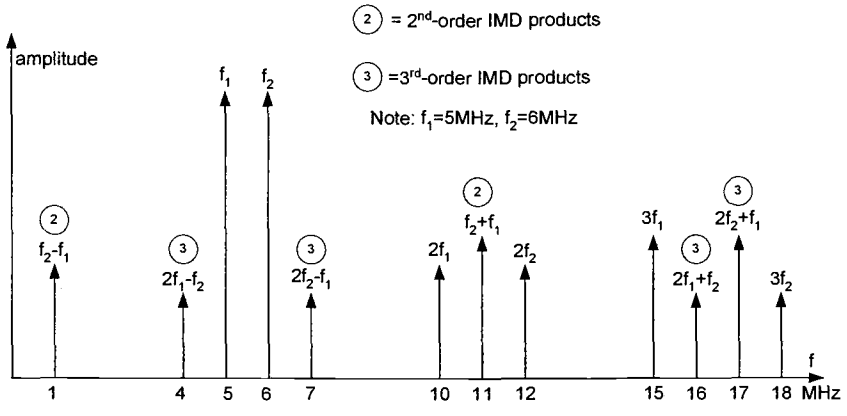


Fig. 5.1 2nd-order and 3rd-order intermodulation products for $f = 5MHz$ and $f_2 = 6MHz$

Note that 2nd-order products fall at the frequencies which can be filtered. However, 3rd-order products are so close to two-tone that they are difficult to filter. 3rd-order IMD products can make out small signals in the presence of larger ones. It is common practice to specify the 3rd-order IMD products in terms of the 3rd-order intercept point (IP3) as is shown by Fig 5.2. Two spectrally pure tones are applied to the system. With a low level two-tone input signal, and two data points, one

can draw the 2nd-order and the 3rd-order IMD lines as they are shown in Fig 5.2. When the input reaches a certain level, however, the output signal begins to soft-limit, or compress. A parameter of interest here is the 1-dB compression point. This is the point where the output signal is compressed 1 dB from an ideal input/output transfer function (solid). Nevertheless, both the 2nd-order and the 3rd-order intercept lines may be extended, to intersect the (dotted) extension of the ideal output signal line. These intersections are called the 2nd-order and the 3rd-order intercept points, respectively, or IP2 and IP3. OIP3 and IIP3 are output and input of 3rd-order intercept points, respectively. These power level values are usually referenced to the output power of the device delivered to a matched load expressed in dBm.

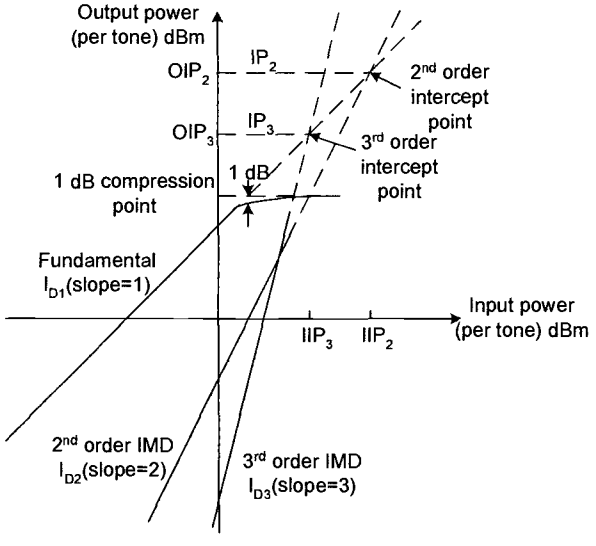


Fig. 5.2. Definition of intercept points and 1-dB compression points

It should be noted that IP2, IP3, and the 1-dB compression point are all a function of frequency, and as one would expect, the distortion is worse at higher frequencies. For a given frequency, knowing the 3rd-order intercept point allows calculation of the approximate level of the 3rd-order IMD products as a function of output signal level.

One can use intermodulation to measure the filter linearity near the upper passband edge. The third-order intercept point (IP3) is as a measure for the third-order distortion component [D. A. Johns1997]. For fully differential circuits, the even-order distortion components are ideally zero or small. Defining H_{D1} and H_{D3} to be the amplitudes of the fundamental and third-harmonic terms, the ratio of $HD_3 = \frac{H_{D3}}{H_{D1}}$ is defined as the third-order harmonic distortion ratio. Defining I_{D1} and I_{D3} to be the first and third intermodulation distortion levels, the ratio of $ID_3 = \frac{I_{D3}}{I_{D1}}$ is defined as the third-order intermodulation ratio. Knowledge of the third-order intercept point is quite useful in determining what signal level should be chosen to achieve a desired *ID3*.

So, the second and third intercept points (IP2 and IP3) are figures of merit for the specifications of amplifier and filter and allow distortion products to be computed for various signal amplitudes.

Spurious-Free Dynamic Range (SFDR)

The concept of 2nd- and 3rd-order intercept points is not valid for an ADC, because the distortion products do not vary in a predictable manner (as a function of signal amplitude). The ADC does not gradually begin to compress signals approaching full-scale (there is no 1-dB compression point). On the other hand, for signals much below full-scale, the distortion floor remains relatively constant and is independent of signal level. For these reasons, the 2nd and 3rd order IMD intercept points are not specified for ADCs and DACs. The single- or multi-tone SFDR specification is the most accepted way to measure data converter distortion [W. Kester2006].

In $\Delta\Sigma$ modulator ADCs, linearity is typically specified as spurious-free dynamic range (SFDR). SFDR can be defined as the signal-to-noise ratio when the power of the third-order intermodulation products I_{D3} equals the noise power N_o [D. A. Johns1997]. Alternatively, one can measure SFDR using the input-signal levels as the difference between the level that results in $I_{D3} = N_o$ and the level A_{N_o} that results in a fundamental output level equal to N_o, as shown in Fig 5.3. It is typically expressed in decibels.

$$SFDR = I_{D1}^* - N_o = I_{D1}^* - I_{D3}^* \tag{6}$$

where I_{D1}^* and I_{D3}^* refer to the output and distortion levels when $I_{D3} = N_o$. If the output level is increased, the distortion products will increase and limit the dynamic-range performance. If the output level is decreased, the distortion products will be buried below the noise floor, and the noise will limit dynamic-range performance. However, note that the dynamic-range performance is actually 3 dB below the SFDR value since the dynamic range is the ratio of the signal power to the distortion plus the noise power.

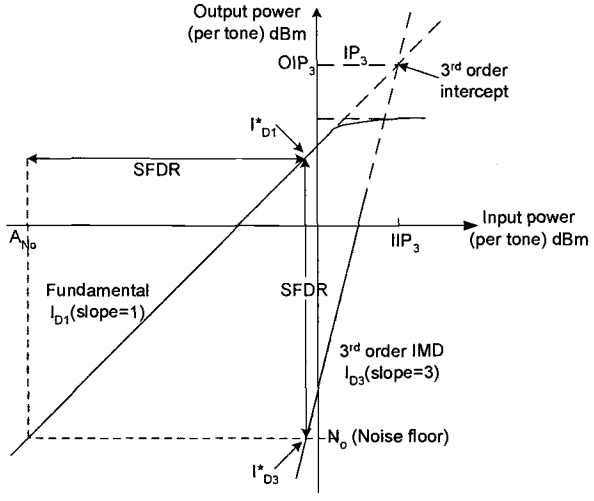


Fig 5.3. Definition of Spurious-Free Dynamic Range

Two-tone and multi-tone SFDR are often measured in communication applications. The 2-tone intermodulation performance of the 14-bit, 80-MSPS ADC is as shown in Fig. 5.4 [W. Kester2006]. The input tones are at 69.3 MHz and 70.3 MHz and are located in the second Nyquist Zone. The aliased tones therefore occur at 9.7 MHz and 10.7 MHz in the first Nyquist Zone. High SFDR increase the receiver's ability to capture small signals in the presence of large ones, and prevents the small signals from being masked by the intermodulation products of the larger ones.

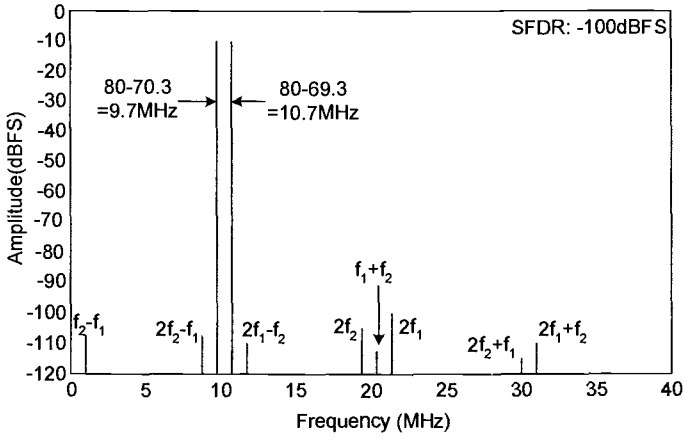


Fig 5.4. 14-bit 80-MSPS ADC two tone FFT for f1 and f2 input tones

Modulator Topology Selections

Topology selections are usually based on resolution and stability. Several modulators have been successfully built using the following techniques: 1) cascaded topologies with single-bit quantization in all loops; 2) cascaded topologies with multi-bit quantization in one or more loops; 3) multi-bit single-loop modulators.

For single-bit, single-loop modulators, we have to reduce the integrator gain to maintain the stability when the loop order is increased. Single-loop topologies are very tolerant of nonidealities such as *RC* time-constant variation and finite

amplifier gain. Thus, little SNR improvement can be obtained by simply increasing the loop filter order at a low OSR.

Multi-loop cascaded topologies, with two or three cascaded loops of first- and/or second-order modulators, solve the stability problem of single-loop high-order modulators. Large *RC* time-constant variation will introduce a mismatch between the analog noise-shaping transfer function and the digital noise cancellation characteristic, from which significant SNR degradation may result. Accurate matching is required between them.

For multi-bit internal quantization, since multi-bit quantizers are more linear than single-bit quantizers, the stability of multi-bit single-loop modulators is significantly improved. Thus, more aggressive noise-shaping transfer functions can be employed, with the benefit of extra dynamic range. The multi-bit quantizer also reduces the jitter sensitivity of the ADC.

A multiple feedforward (FF) topology has the advantage of requiring only one DAC, compared to its multiple feedback (FB) counterpart that needs as many DACs as the modulator order. In comparison with an FF-structure, the FB-structure features large signal swing requirements and stability issues which demand a less aggressive NTF. Since CIFB requires several DACs feeding back to each integrator output, it is not an area-efficient solution when multi-bit DACs are used [Z. Li2007]. In an FF structure there is only one loop and any additional delay of the blocks (DAC, integrators ...) decreases the stability of the loop. The FF-architecture shows reduced anti-aliasing behavior and in addition a strong STF peaking around the cutoff frequency. Comparing the FF- with the FB-topology, the FB-structure has a better out of band signal suppression.

DT or CT ΔΣ Modulator Selection

There are several advantages in CT ΔΣ modulators: (1) CT modulators can potentially operate at higher clock frequencies and/or with less power consumption. (2) Intrinsic anti-alias property of the continuous-time loop filter significantly suppresses the aliasing. (3) since sampler is inside the noise-shaping loop, any sampling error, together with the quantization noise, is significantly suppressed by the high gain of the loop filter in the bandwidth of interest. Thus, the performance requirement of the sampler is relaxed. Drawbacks include that they are more sensitive to nonidealities such as clock jitter and excess loop delay than DT ΔΣ modulators, and that their design methodologies are less well developed than those of DT architectures.

Multi-Bit DAC Mismatch

For ΔΣ modulator with multi-bit quantization, DAC feedback linearity is critical [R. Schreier2006]. The component mismatch in DAC can limit the modulator dynamic range to less than 10 bits if no calibration is used [Z. Li2007]. Due to the low OSR, large transistor threshold voltage and current factor mismatch, dynamic element matching is not sufficient to suppress the DAC mismatch to the required level. On the contrary, a DAC with current calibration can achieve more than 14 bits of linearity with less hardware consumption and less excess loop delay. Mismatch-shaping technique can improve DAC linearity [T. Shui1999]. A drawback of mismatch-shaping is that it increases the feedback delay of the ADC, which alters the NTF and can even destabilize the modulator.

Tone Generation

ΔΣ modulators are known to suffer from tones introduced by DC offsets that develop regular patterns in the 1-b output code [E. J. van der Zwan1996]. Such low-frequency tones will not be filtered out by the next stage low-pass filter and can lead to annoying tones in the desired range. The dc offset reduces the

dynamic range of the modulator. It has been shown that tones exist even in higher-order modulators [D. A. Johns1997]. If v_{offset} is the input DC offset voltage and v_{quant} is the full-scale input level, tones occur in the output spectrum of the $\Delta\Sigma$ modulator at frequencies [E. J. van der Zwan1996]

$$f_{tone1} = \frac{v_{offset}}{v_{quant}} \cdot OSR \times f_s \tag{7}$$

$$f_{tone2} = (1 - \frac{v_{offset}}{v_{quant}}) \cdot \frac{OSR \times f_s}{2} \tag{8}$$

From (7) and (8), we may estimate the tone1 and tone2 occur in the output spectrum of the $\Delta\Sigma$ modulator.

Stable Input Range

$\Delta\Sigma$ modulators suffer from large signal instability because the DAC cannot feedback a large enough signal in time to compensate for the input signal (i.e., the phase and the gain margin of the loop is too small) [K. Philips2004]. The error signal and the internal signals in the loop (i.e., the outputs of the various integrators) therefore grow and further reduce the gain and the phase margin, resulting in instability. Well-designed single-bit modulators typically achieve a maximum modulation depth of about 70%, i.e., -3dB below digital full-scale. This modulation depth represents a good compromise between aggressive noise shaping and stability. The input level $V_{in,\max}$ corresponding to this maximum DAC output of $0.7V_{DAC}$ is called the stable input range. $V_{in,\max}$ is frequency dependent and can be calculated if the STF of the modulator is known:

$$V_{in,\max}(j\omega) = \frac{0.7V_{DAC}}{STF(j\omega)} \tag{9}$$

In many practical designs, the stable input range of the $\Delta\Sigma$ modulator is the dominant limitation on the allowable interferer level.

Inter-Symbol Interference

[K. Nguyen2005] Inter-symbol interference (ISI) error is the result of mismatch in the rise and fall time in the CT feedback DAC output waveform, which degrades the SNR and THD+N performance of the converter. Usually, it may be mitigated by fully differential or RZ DAC waveform.

5. 2 Circuit Design and Implementation

The key factors in circuit design include modulator loop architecture, integrator (resonator) selection, various filters (loop filter, noise cancellation filter, decimation filter), tuning circuit (including RC time constant tuning and mismatch calibration), adder and comparator, summation circuit, clock generation circuit, sampler, internal ADC selection, feedback DAC pulse selection, current-mode DACs, timing control loop, and the like.

Integrators.

A lot of effort has been put on architectural optimizations in order obtain a stable CT $\Delta\Sigma$ modulator with maximum quantization noise and interferer suppression and with minimal signal swing requirements.

The loop filter of $\Delta\Sigma$ modulators can be implemented in different ways. Every integrator contributes nonlinearity to $\Delta\Sigma$ modulator. The integrator's linearity requirement can be derived from the $\Delta\Sigma$ modulator's linearity specification. A more aggressive NTF results in greater in-band "noise" due to nonlinearity [P. Sankar2007]. For a multi-bit modulator, integrator nonlinearity causes the in-band noise (IBN) floor to rise. On the contrary, for single-bit modulators, integrator nonlinearity results in harmonic distortion of the input sinusoid.

The key aspects of the design of the amplifiers of the resonator are the gain and the delay. A reasonable gain is required to prevent deterioration of the overall

filter transfer characteristic. The delay of the amplifier should be small to prevent the resonator from oscillating. Usually, the resonators in the loop filter have been implemented with (opamp-RC) integrators and local feedback.

Generally, almost all lowpass CT $\Delta\Sigma$ modulator are composed of Gm-C or active-RC filter or a combination of both.

The choice of an active-RC integrator may be made for several reasons. First, compared to the other integrators, active-*RC* integrators have superior linearity, simplicity, larger output signal swing, parasitic insensitivity as well as overall power consumption. Linearity limitations mainly result from the resistor as well as the amplifier. Second, the virtual ground of the amplifier is ideal as a current feedback point for the current-steering DACs employed in the topology. Since the amplifier will process its output to keep its virtual ground swing small, the issue of DAC nonlinearity due to finite output conductance is minimized. It provides a good virtual ground for the modulator feedback DACs. It eases design, especially with low supply voltages. Third, the topology is well suited for low-voltage operation in that large signals are seen only at the input resistor and the output of the amplifier where careful design can allow nearly rail-rail operation. The bandwidth of the first integrator can be large, as there is no feedback to the following stage and the output signal swing of this integrator can be scaled only with its bandwidth. A high bandwidth of the first integrator suppresses the thermal noise of the following integrators.

Gm-C integrators can operate at higher frequencies with simpler circuit structure and less power consumption. They are constructed from a transconductance amplifier and a capacitor (Gm-C). They are easily tunable, present only a capacitive load for previous integrators and generate only small excess phase shift. The transconductance amplifier's specifications of interest are linearity, output

noise, and bandwidth. The transconductance amplifier's noise requirement can be derived from the $\Delta\Sigma$ modulator's input referred noise specification. The sizes of Gm-C are determined by taking into account the contribution of thermal noise to the total ADC noise, and by making this noise low enough to avoid the degradation of the effective resolution of the converter. If the thermal noise is made much lower than the quantization noise, there will be a noticeable increase in power consumption. Therefore, there is a trade-off between resolution and power consumption. For the high-speed low-power building blocks of the $\Delta\Sigma$ modulator, Schoofs shows that Gm-C integrators are better than active-*RC* integrators in the low-pass filter of the modulator because they show a better tradeoff between power, speed, and accuracy[R. Schoofs2007]. It is shown that the most efficient filter implementation for CT $\Delta\Sigma$ modulator with moderate resolutions consists of Gm-C integrators. Some linearization techniques have been described [A. Leuciuc2001]: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistors or MOS transistors), shifted level biasing, series connection of multiple differential pairs, combination of the above methods, pseudo-differential stages (using transistors in the triode region or in saturation).

For a multi-stage modulator, the first stage dominantly determines the entire modulator's noise, linearity and distortion performance. Since the noise performance of input stage is precuarily determined by the thermal noise of the input and DAC resistors, most of the power is consumed in the first integrator. Other integrators' nonidealities in the $\Delta\Sigma$ modulator are noise shaped by the first order and second order, respectively, and have more relaxed requirement with respect to noise and distortion. Any cross-over distortion of the output stage may be suppressed by the high gain first stage when referred back to the input. Any slewing in the first stage will severely degrade the THD+N performance of the converter. The opamp should ensure that the integrator is never slew limited, even

with the largest sample-to-sample code jump. Therefore, an active-*RC* integrator may be selected as the first-stage integrator for its excellent linearity. The second- and third-stage integrators could be Gm-C type.

Quantizer

The non-ideality of the internal quantizer has the least effect on the ΔΣ modulator. Offset calibration may be required to guarantee a monotonic transfer characteristic and to reduce the nonlinearity of the quantizer. The effect of comparator hysteresis on the overall ΔΣ modulator is negligible, provided an adequate recovery of the comparator takes place. In contrast, delay and metastability are a design concern. Fast accurate comparisons are required to avoid metastability resulting in noise leakage. The performance of a one-bit ADC in the quantizer is mainly determined by the offset voltage and the bit error rate of the comparator used. The bit error rate is related to the metastability of the comparator: when the input signal of the comparator decreases, the decision time of the comparator increases. Most commonly, flash ADCs are used, whose output is latched to eliminate signal dependent delay. The accuracy of a flash quantizer depends on the input offset of its comparators, which is directly related to the area of the input devices and hence the input capacitance. Tracking ADC and successive approximation ADC can also be used. In order to achieve low-power operation, it is important to keep the input loading of the quantizer small.

DAC

The DAC pulse shape has to be determined before performing the transformation from the equivalent DT loop transfer function to the CT loop transfer function. The sensitivity to clock jitter in a CT ΔΣ modulator is also determined by the DAC pulse. Moreover, the DAC pulse shape has a great influence on the sensitivity to excess loop delay. It has been shown that the RZ DAC has less inter-symbol interference and pulse distortion. Multi-bit feedback DAC is usually

implemented as current steering DACs for two reasons: 1) its potential for high-speed operation and 2) the convenience to interface the DAC output current with the CT loop filter [M. S. Kappes2003]. Due to the limitations in matching, a current-steering DAC composed of unit elements has limited linearity. Several approaches can be used to improve the linearity performance of the feedback DAC: (1) to calibrate the DAC using a master reference such that unit elements mismatches are corrected. (2) to use dynamic element mismatch shaping (DEM) to either randomize or noise shape the mismatch-induced distortion out of band. The latter was due to the ease with which the mismatch shaping can be employed. In order to reduce the nonlinear distortion due to mismatch between the DAC unity elements, a dynamic element matching (DEM) block shuffles the unit elements in the DAC. In this way, the power of the harmonics introduced by DAC mismatch is spread into white noise, increasing the linear range of the modulator. In [L. Dorrer2005], Dorrer proposed a scheme to put the DEM block outside the time critical loop, thus the excess loop delay is not increased. In [K. Nguyen2005], a data-directed scrambler is proposed to spectrally shape the error caused by the feedback DAC's unit element mismatch into the out-of-band frequency region. However, Kappes [M. S. Kappes2003] pointed out that the DEM logic is effective in reducing the nonlinearity of the DAC, but the noise floor of the ADC rises when DEM is applied. Simulations indicate that this is a result of excessive charge feedthrough in the DAC. As very small feedback currents are used in the DAC, the clock feedthrough can become a significant component of the feedback current.

5.3 Implementations

Implementation example I: a wideband low-power CT ΔΣ modulator for next generation wireless applications [X. Chen2007].

The wideband low-power CT ΔΣ modulator in this example was implemented as shown in Fig 5.5 from [X. Chen2007].

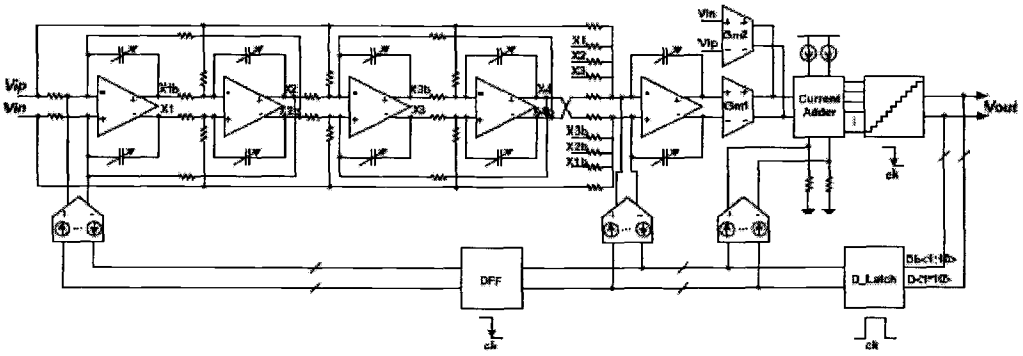


Fig. 5.5 Wideband low-power CT ΔΣ modulator

In order to meet the design goal, a modified feed-forward modulator architecture was used. To start with, an extra feedback path was introduced to move the first stage out of the 1st-order loop to reduce the speed requirement, and hence the power consumption of the first opamp. In addition, it also divides the big adder in front of the quantizer into two smaller ones to ease the circuit realization. Second, several direct feed-in branches to the input of each integrator and the adder were added and optimized to cancel the out-of-band peaking in the signal transfer function, which equivalently increases the dynamic range of the modulator. Finally, a direct feedback path was introduced to relax the quantizer delay requirement, addressing the issue of the excess loop delay. NRZ DAC pulse was adopted to reduce the clock jitter sensitivity. In order to maximize the loop speed, a fast current adder was used, and the sampling capacitor of the comparator is minimized. A neutralization technique was used to cancel the input capacitor of the comparator. A fully differential layout scheme was used to minimize the

offset and distortion. Table 5.1 shows the summary of the measured chip characteristics while the input signal frequency is 2 MHz.

Table 5.1: Summary of the measured chip results

Specifications		Value
Peak SNDR	BW=25 MHz	52dB
	BW=20MHz	56dB
Peak SNR	BW=25MHz	52.5dB
	BW=20MHz	58dB
Dynamic Range	BW=25MHz	55dB
	BW=20MHz	60dB
Clock frequency		400MHz
Power supply		1.8V
Power consumption		1.8mW
Die area w/o pad		1.3mm × 0.9mm
Fabrication Process		0.18 μm 1P6M mixed/RF CMOS

Implementation Example II: A 14 Bit CT ΔΣ A/D modulator with 2.5 MHz Signal Bandwidth [Z. Li 2007].

A fifth-order single-stage dual-loop continuous-time ΔΣ modulator has been implemented in a 0.25 μm CMOS process as shown in Fig 5.6 from [Z. Li2007]. The modulator implements a 14 bit, 2.5MHz signal bandwidth CT ΔΣ modulator.

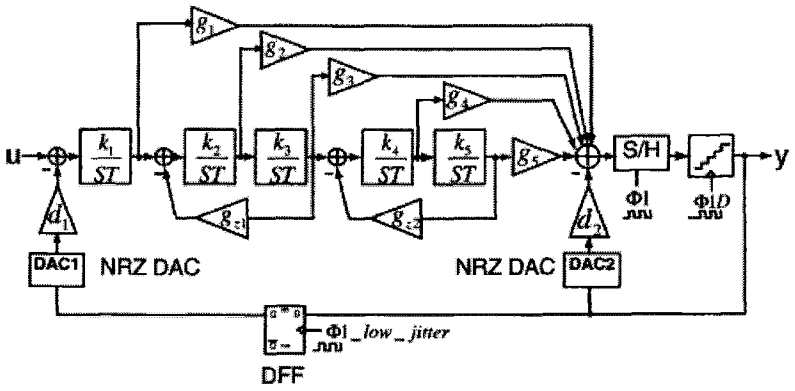


Fig. 5.6 A continuous-time ΔΣ A/D modulator with 2.5 MHz signal bandwidth

Noise shaping for the quantization noise was provided by a high-order loop filter. A multi-bit quantizer was used to increase resolution and to enhance loop stability. The architecture is insensitive to the extra loop delay caused by the quantizer. The zeros of the noise transfer function are optimized to achieve better quantization noise attenuation in the signal band. A dual-loop architecture was chosen to relax the quantizer delay requirement due to the excess loop delay. A multi-bit NRZ DAC was adopted to reduce clock jitter sensitivity below the 14 bit noise floor. All integrator capacitors are tunable to compensate to the effect of process variations. Self-calibration is used to compensate the mismatch in the current-steering DAC. Except for the first integrator, all integrators are implemented as Gm-C integrators to reduce power consumption. Table 5.2 summarizes the measured characteristics of the prototype chip.

Table 5.2 Summary of the measured chip results

specifications	Values
Peak SNDR	80.5dB
Peak SNR	81dB
Peak SFDR	98.4dB
Dynamic range	85dB

Input signal bandwidth	2.5MHz
Clock frequency	60MHz
Oversampling ratio (OSR)	12
Power supply	2.5V
Power consumption	50mW
Die area w/o pads	2.1mm × 1.3mm
Die area w/ pads	2.5mm × 1.7mm
Fabrication process	0.25 μm 5-matel mixed /RF CMOS

Implementation III: A 375-mW Quadrature Bandpass ΔΣ ADC with 8.5-MHz BW and 90-dB DR at 44MHz [R. Schreier2006]

A quadrature bandpass ΔΣ ADC with 8.5-MHz bandwidth and 90dB dynamic range at 44-MHz was implemented in 0.18- μm CMOS as shown in Fig. 5.7.

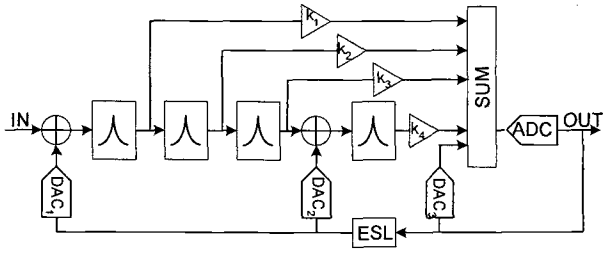


Fig. 5.7 A Quadrature Bandpass ΔΣ ADC
with 8.5-MHz BW and 90-dB DR at 44 MHz

Several innovations were used in this design.(1) The distribution of zeros and poles of the NTF were optimized considering the tradeoff between in-band noise suppression, image-band noise suppression, and out-of-band noise gain. (2) A modified feedforward architecture was employed to take advantage of the characteristic low distortion and high dynamic range of a feedforward topology. (3) SAW filter was used to attenuate the signals which lie in the vicinity of the peaks of the signal transfer function (STF). (4) Three signal resonators and one

image signal resonator were used. Placing the image resonator at the end of chain relieves the preceding resonators of the need to process image signals and thereby prevents mismatch in signal resonators from reflecting image noise into the passband. (5) DAC2 was used at the input of the image resonator. Without DAC2, it turns out that the NTF is extremely sensitive to coefficient errors. DAC2 alleviates this difficulty by providing a path for negative-frequency energy directly from the output of the quantizer. (6) Element selection logic (ESL) block shapes DAC mismatch noise to improve DAC linearity; In addition, to prevent the influence from feedback delay which is produced by mismatch shaping, a full clock period is allocated for the quantization and element selection operations. (7) The timing adjustment block was used to ensure accurate placement of the sampling instant relative to the feedback interval. (8) An important feature of this $\Delta\Sigma$ ADC is its variable full-scale range. It is controlled by changing the least-significant-bit size of DAC1, while simultaneously changing the gain of the first resonator in an inverse manner. As a result of this arrangement, the gain through the combination of DAC1 and resonator 1 is independent of the full-scale setting. The absolute magnitude of the noise of DAC1 is reduced when its LSB is decreased, regardless of whether the noise is thermal, mismatch, or jitter noise. The increased gain in resonator 1 reduces the input-referred contributions of all noise sources after resonator1.

Additional innovations include circuit techniques that allow the Q of an active-RC resonator to be high despite finite amplifier gain and bandwidth. With these techniques, the realized Q-factors exceeded the design requirement by nearly a factor of 2. Gain scaling was used to extend the ADC's dynamic range without increasing its power consumption. Table 5.3 provides a summary of the ADC's key specifications.

Table 5.3 ADC Performance Data

parameter	value	Notes
Center frequency	44MHz	$f_S/6$
Bandwidth	8.5MHz	
Clock rate	264MHz	
Peak SNR	77dB	
Instantaneous dynamic range	85dB	
Full-scale range	12dB	-8.5 to + 3.5 dBmA
Total dynamic range	90dB	
Input IP3	+33dBmA	Full-scale=max
Alias attenuation	>60dB	
Image rejection	50dB	
Power consumption	375mW	ADC
	50mW	Decimation filter
Area	2.5 mm^2	0.18 μm CMOS

Implementation Example IV: An IF-to-baseband ΔΣ Modulator for AM/FM/IBOC Radio Receivers with a 118 dB Dynamic Range [P. G. R. Silva2007]

In order to eliminate the automatic gain control (AGC) loop, the variable gain amplifier (VGA) and the AM filter, high DR (>100dB) were used in the ADC. As shown in Fig. 5.8 from [P. G. R. Silva2007], the high-resolution quadrature ΔΣ modulator combines the anti-aliasing suppression of a CT loop filter, the low jitter sensitivity of a SC feedback DAC implementation, and the low power consumption of passive mixers for IF-to-baseband down-conversion. This modulator has the following characteristics.

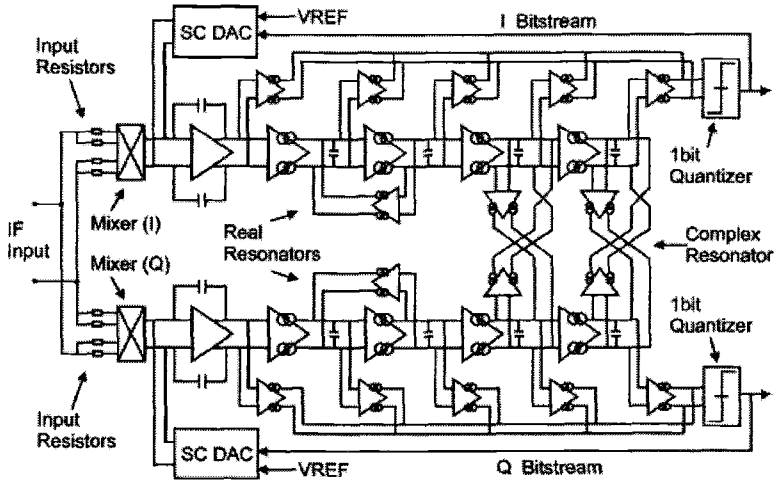


Fig.5.8 Single-bit fifth –order CT IF-to-baseband complex ΔΣ modulator

First, a single-bit quantizer is used together with a single-bit, inherently linear, SC feedback DAC. In this design, most of the feedback charges are integrated at the beginning of the DAC duty-cycle. As a result, a CT ΔΣ modulator implemented with a SC DAC can tolerate larger delays between the quantizer and feedback DAC clock signals. This architecture is also less sensitive to jitter-induced errors. Second, a single-bit fifth-order loop filter with feedforward coefficients is used. The feedforward coefficients provide first-order roll-off at the unity open-loop gain frequency and ensure the modulator's stability. Third, the *I* and *Q* analog input are processed by two modulators. The required quantization noise attenuation inside the signal band is provided by real and complex resonators. The real resonators are implemented through the local feedback path around the second and third integrators, and the cross-connections between *I* and *Q* ΔΣ modulators implement two complex resonators. Fourth, the active-RC integrator is used as the first integrator for its high linearity. To save power, the other integrators and resonators are implemented by Gm-C stages. Table 5.4 presents the summary of performance for this IF-to-Baseband ADC

Table 5.4 summary of performance

ΔΣ modulator	5^{th}-order complex CT, 1b with SC DAC		
Input voltage range	0.5 V_{rms}, fully differential		
Sampling rate	41.7MHz		
mode	AM	FM	IBOC
Signal bandwidth	3kHz	200kHz	500kHz
Dynamic range	118dB	98dB	86dB
Peak SNDR	113dB	90dB	88dB
SFDR	90dB	90dB	88dB
Intermod. distance	Mixer OFF	Mixer ON	
IM2	102dB	92dB	
IM3	98dB	91dB	
Image rejection	Typical 63dB, σ =6dB		
Active area	$6mm^2$		
Power consumption	210mW (I+Q)		
Supply voltage	1.8V		
Process	1P, 5M, standard 0.18 μm CMOS		

At the end of the chapter, we summarize some works on CT ΔΣ modulators, as shown in Table 5.5, which includes papers published during the past ten years.

Table 5.5

Year	Author	ARCH	SNDR(dB)	SNR(dB)	BW(MHz)	DR(dB)	SF(MHz)	OSR	PWR(mW)	SUP(V)	TECH
2008	S. Pavan	4bit flash, 3rd-order active-RC	90.8	92.5	0.024	93.5	3.072	64	0.09	1.8	0.18um
2008	T. Song	5th-order active-passive GPS WCD	63.4	63.9	2	68	150		2.7	1.5	0.25um
2007	K. Pun	1-bit,3rd-order active-RC, RO DAC	74	76	0.025	68	3.2	64	0.3	0.5	0.18um
2007	Z. Li	5-b (17levels), 5th-order, NRZ DAC	80.5	81	2.5	85	60	12	50	2.5	0.25um
2007	L. Breems	4b, 2-2,Q,CT ADC, FM	71	69	20	77	340		56	1.2	90nm
2007	P. Silva	1b, 5th-order complex CT,1b with SC DAC, AM/FM/IBOC	113/90/78		0.003/0.2/0	118/98/86	41.7	42/10	210	1.8	0.18um
2007	X. Chen	11level,5th,Real,wireless	52/56	52/58	25/20	55/60	400	8	18	1.8	0.18um
2006	G. Mitteregger	4b,3rd-RC,M-CRFB, flash ADC, real, CT, ADC	74	76	20	80	640	16	20	1.2	0.13um
2006	J. Arias	3b, 2nd,LP, Q, CT ADC, wireless	53.5	55	20	56	320	16	32	2.5	0.25um
2006	R. Schreier	4b,4th-order, active-RC,FF, ESL, QBP, flash ADC, CT, ADC,TV		77	8.5	90	264	31	375	3.3	0.18um
2006	B. Baggini	b, 2x4th-order, daul-mode real/complex, CIFF, BP CT GSM/EDGE				75	0.2/0.27		22	1.5/2.65	0.25um
2006	T. Caldwell	2 x 3rd-order LPs, CTTI	57/49	58/50	10/20/	61/55	100/200	5	101/103	1.8	0.18um
2005	L. Dorrer	4-bit,3rd-order,CT, ADC, tracking, DEM, UMTS	70	74	2	75	104		3	1.5	0.13um
2005	K. Nguyen	4b,2nd,CT-DT,RZ, ADC,audio		99	0.02	106		128	18	3.3	0.35um
2004	E. Dagher	1b,2nd,CT wireless	89	79	1.23	76.4	2000	192	18	1.8	0.18um
2004	S. Paton	4b,4th-RC,M-CRFF, CT, ADC, vedio/wireless	63.7	64.6	15	67	300	10	70	1.5	0.13um
2004	L. Breems	4b, 2-2,I&Q,CT, comm	56	63	10/20/	67	160	8x	122/216	1.8	0.18um
2004	S.Yan	5b, 3rd,NRZ DAC, M-CRFF, CT, flash ADC, ADSL	83	84	1.1	88	35.2	16	62	3.3	0.5um
2004	K. Philips	1b,4th,CT ADC, Bluetooth	46/57/59	46~59	1	89	64		2		0.18um
2003	F. Gerfers	12b, 3rd-RC,LP,CT	70	73	0.025	80	2.4	48	0.135	1.5	0.5um
2003	M. Kappes	4b flash, 2nd-order BP, NRZ DAC, CT ABC, without/with DEM wireless		64	1	68	48	24x	2.2	1.8	0.18um
2003	R. Veldhoven	1b with SC DAC, 5th-order CT, I/Q,feedforward, GSM/CDMA/UMTS		70/80/90	3.84/1.228/0.2	74/83/92	153.6/76.8/26	40/64/65	2*4.5/2*4.1/2*3.	2.9	0.18um
2002	O. Bajdechi	1b,10b, 4th,CT, microphone	62		0.011	80		64	1.7	1.8	0.5um
2002	R. Veldhoven	1.5b,4th,I&Q,CT, UMTS	68	66	2	70	153.6	40	2*3.3	1.8	0.18um
2000	L. Breems	1b, 4th,QBP,CT, mixer	84	82	200	82	13		3.6	2.5	0.35um
2000	E. Zwan	1b, 5th,Q.CT AM/FM		94/79	0.009/0.2	97/82	21.07	32	8	2.5	0.25um
1999	H.Tao	1b, QBP,CT-DT	45	54	0.2	49	400	500	238A/92D	2.7A/3.3D	0.35um
1999	J. Engelen	1b, 6th, BP,CT,digitl radio	63.5/76		0.2/0.009	67/81	30~80		60	3.3/5	0.5um
1996	E. Zwan	b, 4th CT audio	74	80	0.0034	80	0.512	64	0.2	2.2	0.5um

6 SUMMARY

This thesis is a review of the continuous-time ΔΣ ADCs, which have many advantages over its DT counterparts. Thus the research in this area is becoming more and more important. In this thesis, the following areas are covered.

- Continuous-time ΔΣ modulator follows the same principles as the digital time ΔΣ modulator, like oversampling and noise shaping.
- Impulse invariant transform is used to transform the DT design into CT design.
- Different architectures, such as time-interleaving, CT/DT hybrid, active/passive hybrid, lowpass filter and bandpass filter, feedback and feedforward, are discussed.
- The effect of circuit non-idealities and the correction methods are discussed.
- Four successful design examples are reviewed.

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