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Gábor C. Temes

Although the digital revolution can realize many of past analog components in the digital forms, our world is surrounded with analog signals such as voice, temperature, etc. The bridge between these two worlds is one of key performance limitations among overall systems and it includes analog filters and data converters.

This thesis studies two design techniques with respect to the improvement of the performances of the bridge circuits; one is an implementation of the delta-sigma A/D converter with a new architecture and another is a proposed correlated double-sampling technique for continuous analog filters. A circuit implementation for the new architecture converter is proposed and implemented in AKM 0.18μm CMOS technology. The test results show that the modulator achieves 72dB of SNDR from the 1.8 V supply voltage. A newly proposed correlated double sampling technique compensates the gain error of a high-Q Tow-Thomas filter which originates from the op-amp imperfections. The gain error is reduced to 0.6dB from 2.5dB with the correlated double sampling technique.

Improved Design Techniques for Analog and Mixed Circuits

by

Yoshio Nishida

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Yoshio Nishida, Author

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Improved Design Techniques for Analog and Mixed Circuits

CHAPTER 1. INTRODUCTION

With the advancement of CMOS IC technology in these decades, higher computing power has made the production of one micro-chip possible with the application of digital technology. Since digital signal circuits are more immune to the noise as well as process variations, many signal processing tasks in past analog forms are now realized by digital components nowadays. These improvements have made the implementation of signal processing systems much cheaper, yet more reliable. Moreover, along with software programming, they provide a great degree of flexibility in the signal processing world. However, almost all natural signals surrounding us are in the form of analog, such as voice, temperature, color, and so on. This inevitable fact emphasizes the importance of interface between these two worlds.

Fig. 1.1 [1] illustrates fundamental requirements for a digital signal processing system that treat an analog signal. The infinite frequency band of analog signal is band-limited by an anti-aliasing filter to avoid “aliasing”. The sample and hold circuit (S/H) converts a continuous-time signal into a discrete-time form, which is universal in a synchronized digital world. The following analog-to-digital (A/D) converter quantizes the discrete-time analog signal and encodes it into a form of digital code. After the digital signal is processed by a sophisticated digital system, a reverse interface process by digital-to-analog converter and reconstruction filter develops an

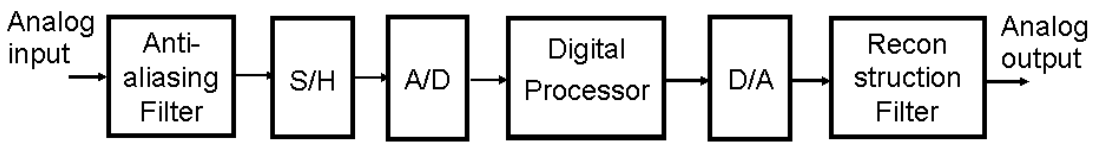


Fig. 1.1 A digital processing system

equivalent analog signal of the processed digital output signal. Usually a S/H is integrated into the A/D converter.

There are various implementation schemes proposed for A/D and D/A converters in IC technology; a flash type, an integration type, a pipelined type, and so on [2]. The main reason to select a certain type of architecture is determined by the performance required in the system application. Each type of architecture exhibits its own pros and cons in the performance. For example, signal bandwidth and resolution are universal indicators for converter blocks. Power supply voltage and power consumption have been the main driving factors for their development. Delta-sigma ($\Delta\Sigma$) converters have advantages over other types of converter systems in terms of their high dynamic range performance and low power consumption. Two signal processing techniques, "oversampling" and "noise-shaping", highly suppress the quantization noise, which is an inevitable product of conversion systems within the signal bandwidth. Consequently, high dynamic range is achieved [3]. Because of the capability of necessary digital systems in the microchip, more and more circuit designers are attracted by the $\Delta\Sigma$ converters. The structures of basic $\Delta\Sigma$ converters have been modified in many ways. Among the various structures of $\Delta\Sigma$ ADCs, an

enhanced-split architecture has been proposed recently [4] and this architecture, compared with the conventional ones, features several advantages. It provides enhanced noise shaping without any stability issues. Unlike multi-stage noise shaping (MASH) architecture, it also does not suffer from the quantization noise leakage. Rather, it shows equivalent analog complexity. Based on the premises above, the purposes of my research will focus on the implementation of the new architecture in CMOS technology.

A modern digital signal system contains one or more continuous-time analog filters internally because of the signal band limits, as seen in Fig. 1.1. Active-type filters are preferred in integrated circuits since they need less area as well as less insertion loss than the passive-type ones [5]. Active-type filters employ active devices such as operational amplifiers (op-amps). Modern CMOS technology provides finer size of devices, which operate with a lower voltage supply. This is a driving factor for higher performance of digital computer chips; however, it also makes the design of high-gain op-amps more difficult. In addition, it even imparts higher 1/f noise level to the circuits. Correlated Double Sampling (CDS) technique is one of the well-known circuit techniques that reduce the effect of those non-idealities of op-amps [3]. This technique has been successfully implemented in discrete-time circuits, such as discrete-time sample-and-hold circuits, discrete-time integrators, etc. However, it was not implemented in continuous-time circuits. Therefore, another purpose of my research is to seek a circuit strategy that applies the CDS technique for those continuous-time filters and to analyze the structures.

1.1. Objective

This study has two main objectives. One objective is to investigate high-performance ΔΣ modulators in both system level and circuit level and to develop an enhanced split ΔΣ A/D converter in a CMOS technology. In the modulator, another new type of Data-Weighted-Averaging technique is also employed [6]. Another objective is to investigate the Correlated Double Sampling (CDS) technique used in the discrete-time circuits and to propose a CDS circuit for improving the performances of continuous-time filters.

The first objective that identified the performance limitations of state-of-the-art ΔΣ modulators (Chapter 2) and designed a prototype of enhanced-split ΔΣ A/D converters with the use of AKM 0.18μm CMOS process technology (Chapter 3) has been accomplished. The performance is verified with the new architecture (Chapter 4.)

The latter objective is accomplished by identifying a correlated double sampling (CDS) technique. By proposing some circuit configurations in order to apply CDS technique for RC continuous-time filters, the circuit performances are compared with non-CDS filters and CDS filter exhibits superior performances (Chapter 5.)

1.2. Thesis organization

This dissertation consists of six chapters. The first chapter discusses the objectives of this thesis research as well as its organization. Chapter 2 provides some background knowledge about ΔΣ A/D converters, and relevant techniques that can be

used to boost the performance of ΔΣ A/D converters. Different from the old techniques, two newly proposed techniques discussed in chapter 3 are employed in my design of the converter circuit. After implementation in a 0.18μm CMOS technology, chapter 4 discusses the experimental results of ADC as well as those of op-amps which are main circuits in the ADC. Chapter 5 features another theme: the CDS technique for continuous-time filters. Chapter 6 is the concluding chapter, where the conclusions along with the future work revolving around this research are discussed.

CHAPTER 2. OVERVIEW OF DELTA-SIGMA A/D CONVERTERS

This chapter introduces the concepts of delta-sigma (ΔΣ) analog-to-digital converters (ADCs), which employ oversampling and noise-shaping techniques. Following this, it discusses what improves their performance and the pros and cons of the solutions.

Fundamentally, analog-to-digital converters (ADCs) contain a sampler which samples the continuous analog signal, and a quantizer approximating the sampled analog signal into finite discrete-voltage signals. Figure 2.1 illustrates the architecture, in which an AAF (Anti-Aliasing Filter) precedes a sampler (sample-and-hold, S/H) and limits the bandwidth of the input signal to half of the sampling rate, in order to avoid "aliasing". In the holding period, when a sampled analog signal is kept unchanged, the quantizer carries out the quantization. Since continuous analog signals are quantized to finite resolution digital signals, this process generates quantization errors. Delta-sigma converters focus on the reduction of the quantization errors, which is described in Section 2.1.

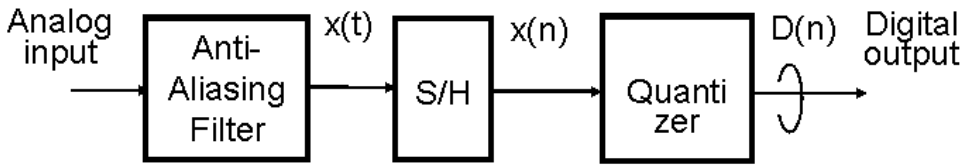


Fig. 2.1 Fundamental analog-to-digital converter

2.1. Single-loop noise-shaping

The key ideas contained in delta-sigma converters are twofold: oversampling in order to spread a quantization noise power over a wide band and noise-shaping for changing the noise power spectrum into a high-pass-like one, while keeping a signal power. Quantization function is inherently nonlinear and it is known to be dependent on the sampled signal. The complete analysis for this nonlinear function is still a very complicated task. Instead, the so-called "input-independent white-noise approximation" model is traditionally used for the system analysis [7]. In this model, the probability density function of the quantization error is a uniform distribution over $[-\Delta/2, \Delta/2]$, where Δ is a least significant bit error (LSB), and the total quantization noise power is

$$e^2_{rms} = \frac{\Delta^2}{12} \ . \qquad (2.1)$$

The power spectrum density (PSD) of a quantization noise, say E(f), is uniformly distributed over the range $[-f_s/2, f_s/2]$ under the condition of busy input signal and hereby the E(f) value is assumed to be e;

$$e^2_{rms} = \int_{-fs/2}^{fs/2} E^2(f)\, df = f_s e^2 , \qquad (2.2)$$

where f_s denotes the sampling frequency.

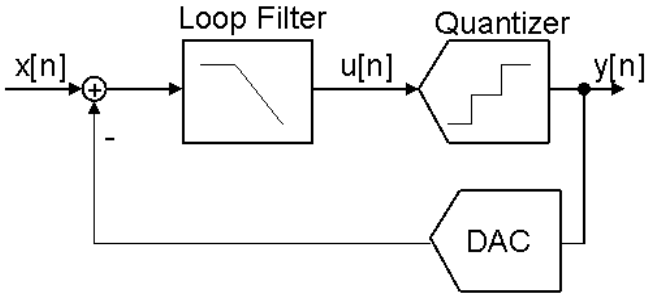
Since the total quantization noise power is constant for a fixed quantizer bit, e^2 decreases for higher sampling frequency, which is a core concept of oversampling technique. The "Nyquist Rate" is twice as signal bandwidth $f_{B,}$ and the oversampling ratio is defined as the ratio of sampling frequency and Nyquist Rate:

$$OSR = \frac{f_s}{2f_B} \tag{2.3}$$

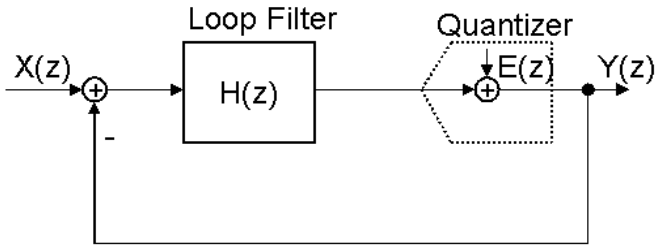
Large part of the quantization noise power spread beyond the signal bandwidth is ideally removed by a digital low pass filter (i.e. a decimator), and the in-band noise power is

$$P_N = \int_{-fs/2}^{fs/2} e^2 \,|\, H_{LPF}(f) \,|^2 \, df = \int_{-f_B}^{f_B} e^2 \, df = \frac{e^2{}_{rms}}{OSR} \,. \tag{2.4}$$

Accordingly, the in-band quantization noise power is reduced by increasing OSR. For example, the in-band noise power is halved by doubling the oversampling ratio, which is equivalent to a 3dB noise power reduction. The in-band quantization noise can be reduced more by using noise shaping technique, which is explained next. A generalized delta-sigma converter consists of a loop filter, a quantizer, and a Digital-to-Analog Converter (DAC), as shown in Fig.2.2 (a). Based on the linear approximation model (Fig. 2.2 (b)), the converter output is represented in the z-domain by



(a) Block diagram



(b) Linear model

Fig. 2.2 Delta-sigma A/D converter

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) \quad . \tag{2.5}$$

Therefore, the Signal Transfer Function (STF) and the Noise Transfer Function (NTF) are

$$STF(z) = \frac{H(z)}{1+H(z)} \approx 1 \tag{2.6}$$

$$\mathrm{NTF}(z) = \frac{1}{1+\mathrm{H}(z)} = 1 - \mathrm{STF}(z) \approx \frac{1}{\mathrm{H}(z)} \ . \qquad (2.7)$$

By using an integrator featuring a large gain in-band for the loop filter, the STF can be approximated by unity, while the NTF becomes very small. This means that an in-band input signal passes to the output, while quantization noise can be suppressed by the high gain of the integrator. The delta-sigma converter benefits from these two techniques: oversampling and noise-shaping, to suppress the in-band quantization noise. Next, the main parameters for ideal delta-sigma converters are introduced into this model, such as loop-filter order (L), quantization bits (B), and oversampling ratio (OSR). Then, one of main performance indexes, Signal-to-Quantization-Noise-Ratio (SQNR) is considered. For an ideal Lth-order low-pass delta-sigma converter, its signal transfer function and noise transfer function are an Lth-order delay and Lth-order maximally flat high-pass filter transfer function, respectively, as indicated below:

$$\mathrm{STF}(z) = z^{-\mathrm{L}} \qquad (2.8)$$

$$\mathrm{NTF}(z) = (1 - z^{-1})^{\mathrm{L}} \qquad (2.9)$$

Similarly to the discussion above, the quantization noise power after passing through a decimator, which filters out out-of-band part, is

$$Q_L = \int_{-f_S/2}^{f_S/2} e^2 \left|1 - z^{-1}\right|^{2L} \left|H_{LPF}\right|^2 df = \frac{\Delta^2 \pi^{2L}}{12(2L+1)OSR^{2L+1}} \quad . \qquad (2.10)$$

The signal power of a sinusoid wave, whose peak amplitude is 1, is (assuming 2^B quantization levels)

$$P_{sin} = \frac{(2^B)^2 \Delta^2}{8} \quad . \qquad (2.11)$$

Note that for this ideal case the overload level is not considered, that is actually critical for high order converters, and it is assumed to be full scale of the input. Accordingly,

$$SQNR_{dB} = 10 \log_{10} \frac{P_{sin}}{Q_L}$$

$$= 6.02B + (20L+10)\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L+1} + 1.76 \, . \qquad (2.12)$$

A general guidance to improve SQNR can be obtained from the observation of this equation. Fig. 2.3 plots the SQNR of ΔΣ A/D converter.

Doubling the oversampling ratio leads to a (6L+3) dB SQNR increase; however, for a wide bandwidth converter, high-speed circuits are required and a technology limit exists.

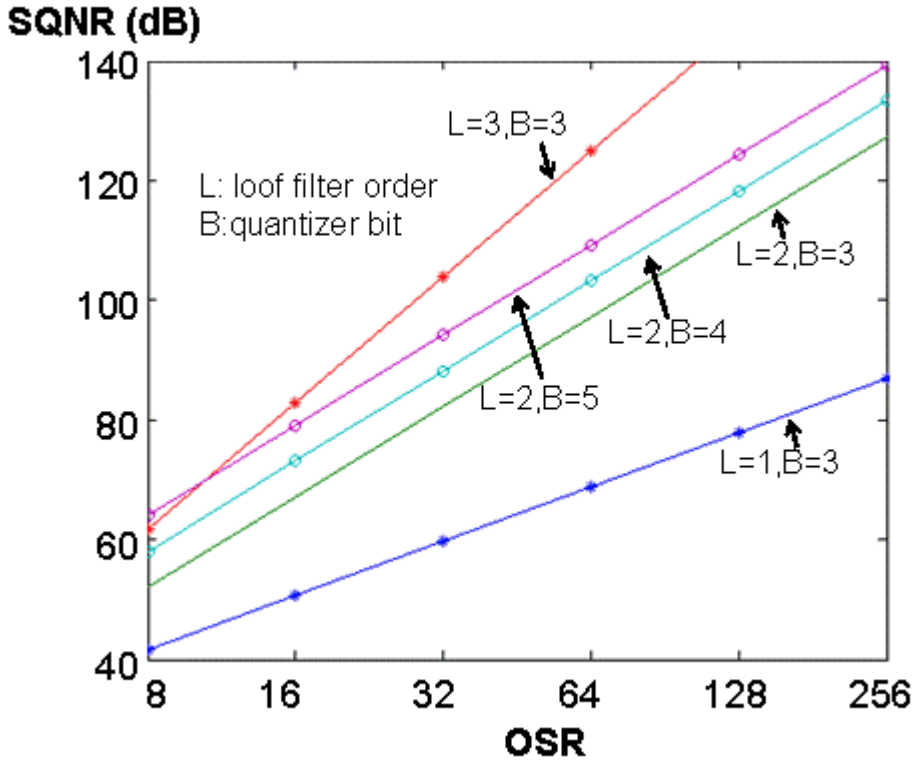


Fig. 2.3 Signal-to-quantization noise ratio of a ΔΣ A/D converter

Employing multiple bits in the quantization process is another way to improve SQNR. Doubling quantization levels improves the SQNR by (6.02×B) dB, since it reduces the total quantization noise power. Moreover, another big benefit is that it improves the stability. This also leads to a more aggressive noise shaping. However, multi-bit quantization suffers from capacitor mismatch errors of the internal DAC. There have been several proposed solutions of reducing the effect of the unavoidable mismatch noise. The next section discusses multi-bit quantization and several schemes to decrease the effect of mismatch errors.

Using a higher order loop-filter, which means increasing L, also increases SQNR by suppressing in-band quantization noise, but higher order modulator (>2) face a stability problem, and stability problem is still unsolved completely.

One architectural solution is to cascade stable modulators and the outputs are processed by noise-cancellation logic. This is the so-called multi-stage noise-shaping, and it has an advantage over other modulators in terms of stability. Stability problem is still not completely solved; therefore, this technique is employed in the design of high order noise-shaping modulator. However, one of its disadvantages is quantization noise-leakage. Section 2.3 discusses this architecture.

2.2. Multi-bit quantization

The performance of a multi-bit delta-sigma converter exceeds that of its counterpart, i.e., a single-bit one, in terms of the Signal-to-Quantization-Noise Ratio, described in the preceding section. Moreover, its stability is also improved. Stability is related to the number of the quantization bits [8], [9]. For a quantizer input u[n], the converter output y[n] is

$$y[n] = u[n] + e[n] , \qquad (2.13)$$

where e[n] is a quantization noise sequence. Referring to equations (2.5), (2.6), and (2.7), the converter output is expressed in time domain as

$$y[n] = \sum_k stf[k]x[n-k] + \sum_k ntf[k]e[n-k] \quad . \qquad (2.14)$$

These two equations and the condition $|e[n]| \leq 1/2^B$ (here the maximum input amplitude of a quantizer is $1+1/2^B$) leads to a L_1-norm stability test by using Cauchy's inequality, i.e.,

$$2^B \geq \frac{\|ntf[n]\|_{L_1}}{1 - \|x[n]\|_\infty \cdot \|stf[n]\|_{L_1}} \quad . \qquad (2.15)$$

Note that the maximum converter's input is defined as $\|x[n]\|_\infty$. An interesting observation is that ntf L_1-norm can be increased with higher number of quantizer's bits, that is, more aggressive noise shaping is possible. Stable maximum input range can also be increased for higher bit numbers. Another observation is that the ntf and the maximum stable input are correlated. Some researchers [11], [12] demonstrated these relations between quantization bit, maximum stable input, and maximum NTF. Although one of the popular rules of thumb analyzed by Sodini and Lee [10] for a 1bit-quantizer points out that the maximum NTF gain (NTF_∞) should be kept under 2 for stable single-bit converters, multi-bit quantization enables NTF_∞ much more than 2, and accordingly more suppressed in-band quantization noise. Reference [11] shows a case of a 4 bit quantizer. A maximum stable input for multi-bit converter is also derived empirically in [12]. By just increasing the number of the levels, an N-level quantizer (say, $N=2^B+1$) exhibits a stable input range as

$$R_N = R_2 + \frac{N-2}{N-1}(1 - R_2) \quad . \qquad (2.16)$$

Here, R_2 is the normalized maximum stable input range for the 2-level converter. By trading the expanded stable input range and the suppression of in-band quantization noise by controlling NTF, more than 6.02dB of SQNR improvement for an additional bit results if keeping the stable input range the same as that of 2-level converter.

Although multi-bit quantization is an attractive architecture to attain higher SQNR and more stability than the single-bit architecture, it has one destructive drawback on the modulator, namely, the mismatch error of the multi-bit DAC in the modulator loop. Therefore, the multi-bit quantization usually requires a calibration to reduce the mismatch noise.

There have been several proposed techniques to reduce the effects of mismatch errors of the internal DAC. A straightforward and simple way is physical trimming. The DAC is constructed from a set of capacitors, or current sources, or resistors. Capacitors are trimmed by switching small capacitors [13]. Current sources are tuned by changing the gate voltage [14]. Resistors are directly cut by a laser beam. These capacitor and resistor trimming techniques are, however, done in a factory or at a power-up; therefore, cannot compensate their variation due to aging and temperature. The technique in [14] requires highly-tuned analog circuits. To take into account these drawbacks, some sophisticated correction techniques have been studied and developed. The *zero-order shaping* technique [15] converts a DAC mismatch error into a flat wide-band noise. This algorithm selects different units each time randomly

and thus the mismatch error at one time is forced to be uncorrelated with one at other time for a same input value. The DAC error can be reduced by increasing the oversampling ratio and wordlength. This is an advantage for high OSR converters; on the other hand this is also a disadvantage for low OSR. The *second-order shaping* technique converts a DAC mismatch error into a 2nd-order high-pass filtered noise. One sophisticated way has been developed by using a pseudo digital second-order delta-sigma modulator in order to shape the mismatch noise [16], [17]. This technique requires a sorting for the vector quantizer, which leads to a high complexity and a large delay. Therefore, it is not suitable for wide-band delta-sigma converters.

The *first-order shaping* technique converts a DAC mismatch error into a 1st-order high-pass filtered noise and it can be implemented simply by a unit element rotation schemes. One popular scheme is known as "Data-Weighted Averaging (DWA)" [18], [19]. The fundamental idea behind of DWA is to use all of unit elements at the maximum rate as possible, while ensuring that each element is used the same number of times. Not only does it result in better performance, but also its simple implementation makes this technique popular. However, because the same set of elements is used cyclically and repeatedly controlled by a single pointer, there is an interaction between DAC error and ADC output waveform. This causes an inherent tone generation problem for this technique. The tones are influenced by many circuits and system parameters; therefore, special attention has to be paid to the problem [20]. From the system viewpoint, some tones are included in-band when lowering the oversampling ratio, so that they heavily degrade the SNDR.

2.3. Multi-stage modulator

A multi-stage modulator is the most popular solution in order to obtain a high-order quantization noise shaping without any stability problems, which is caused by high- order loop filters. It is implemented with a cascade of multiple stable low-order (less than or equal 2nd) loops. From this structure, it is sometimes called MASH (Multi-stAge noise SHaping).

A general MASH structure is shown in Fig. 2.4. The signal transfer function and the noise transfer function of each stage are denoted by STFn and NTFn, respectively. Each stage (ADC_1 to ADC_k) is a low-order (< 3) delta-sigma modulator or a Nyquist-rate converter except for the first stage. The first stage produces a digital output (V1) from the input analog signal and also it conveys the quantization noise (E1) to the second stage. The second stage processes the quantization noise into a digital signal and the quantization noise of this stage (E2) is conveyed to the following stage. Like this, each stage, except for the last stage conveys the quantization noise to next stage. The digital outputs from all stages are digitally processed by the noise cancellation logic into the final output of the modulator (V). If the digital transfer functions are approximated to the analog ones to a high degree, the quantization noises, except for the one from the last stage, are cancelled. Then the final output is

$$V = (STF_1 \bullet STF_2 \bullet\bullet\bullet STF_k)U + (NTF_1 \bullet NTF_2 \bullet\bullet\bullet NTF_k)E_k \,. \qquad (2.17)$$

The overall noise shaping can be the summation of the orders of all stages. This is an

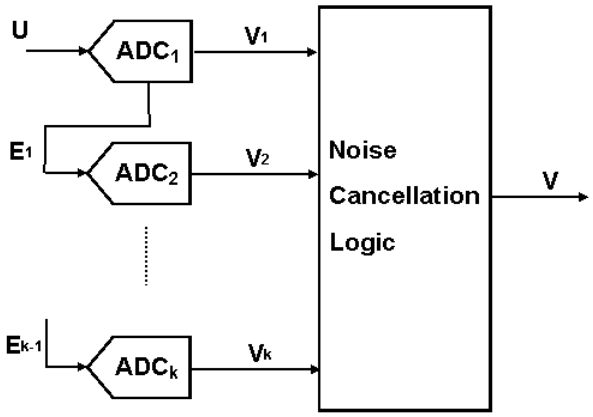


Fig. 2.4 Cascaded delta-sigma modulator (MASH)

ideal case with an assumption of perfect transfer function approximations. In fact, quantization noise leakage will occur when the analog and digital transfer functions cannot be matched well. This is usually caused by the imperfections in the analog circuits. Since these leaked quantization noises are unshaped or shaped by low-order filtering, the suppression in the signal bandwidth is imperfect, so that it heavily degrades the overall performance of the modulator.

Fig. 2.5 illustrates an example of a 1-1 MASH structure. The output is given by

$$V(z) = V_1H_1 - V_2H_2$$

$$= H_1z^{-1}U + [(1-z^{-1})H_1 - z^{-1}H_2]E_1 - (1-z^{-1})H_2E_2 \ . \qquad (2.18)$$

Assuming H_1 is equal to STF_2 and H_2 to NTF_1,

$$V(z) = z^{-2}U - (1 - z^{-1})^2 E_2 \ . \tag{2.19}$$

However, when the analog transfer functions do not match the digital transfer functions, the noise leakage is

$$e_1 = [NTF_{a1}H_1 - STF_{a2}H_2]E_1 \ , \tag{2.20}$$

where NTFa and STFa are the analog noise transfer function and analog signal transfer function, respectively. As a first approximation [21],

$$| e_1 | = | (1/A) + (z - 1) \cdot [D + 2/A] | \cdot | E_1 | \ . \tag{2.21}$$

In this equation, A is the finite dc-gain of the op-amp and D is the mismatch factor of the capacitors. To reduce the unwanted error, a high dc-gain op-amp and high accuracy capacitors are required. This phenomenon is in contrast to single-stage modulators, which are usually immune to the imperfections.

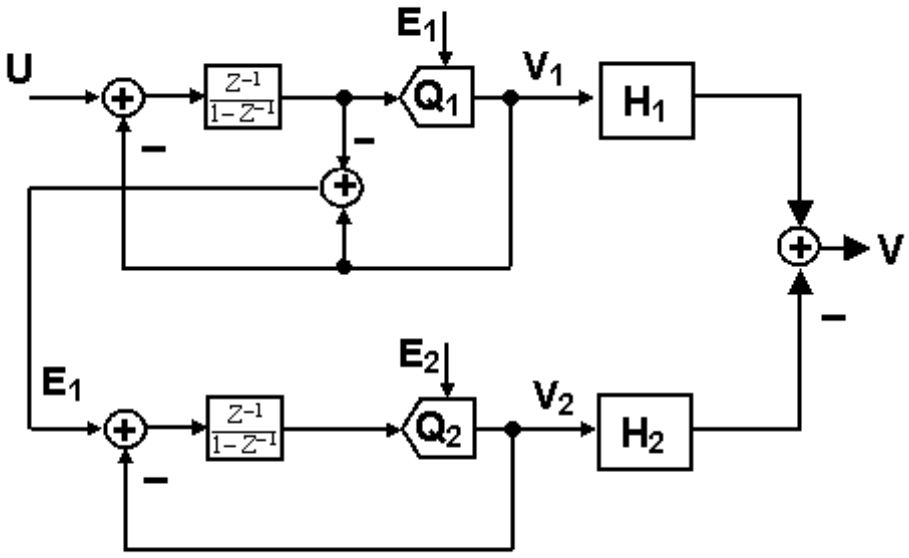


Fig. 2.5 Cascaded delta-sigma A/D converter

CHAPTER 3. DESIGN TECHNIQUES FOR ENHANCED DUAL-PATH DELTA-SIGMA ADC

The increasing demand for higher performance communication devices has fueled the research and development in wide bandwidth delta-sigma modulators in the last decade [22]-[24]. An enhanced-split architecture has been proposed recently [4], and this architecture features several advantages over the conventional ones; it provides enhanced noise shaping without any stability issues. Unlike multi-stage noise shaping (MASH) architecture, this does not suffer from quantization noise leakage and shows equivalent analog complexity. This chapter focuses on the implementation scheme of an analog-to-digital converter (ADC) employing the novel architecture in order to attain a high dynamic range for a relatively wide-band signal bandwidth (80-dB signal-to-noise ratio for a 2-MHz signal bandwidth.) One more new technique is also included in the modulator; Segmented Data-Weighted-Averaging (SDWA) to mitigate the effect of internal DAC mismatches [6].

Firstly, these novel techniques are described in the section 3.1. Next, architectural level design is explained in the following section. Circuit design in AKM 0.8μm CMOS technology is exhibited in a later section.

3.1. Enhanced split architecture and segmented data-weighted-average

The idea behind the enhanced split architecture [4] is to increase the order of noise shaping by coupling the delayed quantization noise of two modulators and then

averaging the digital outputs of the modulators, shown in Figure 3.1. According to the reference [4], the final modulator output is

$$Vc = U + NTF(1-z^{-1})(Q_1+Q_2)/2 \,, \qquad (3.1)$$

where $$NTF_1 = NTF_2 = NTF \quad . \qquad (3.2)$$

The idea behind the segmented data-weighted-average (SeDWA) [6] is to reduce the calculation time for the pointers of conventional DWA by segmenting DAC unit elements to several sets. By breaking the complete rotation, it exhibits less tonal power. Figure 3.2 is an example of two segments.

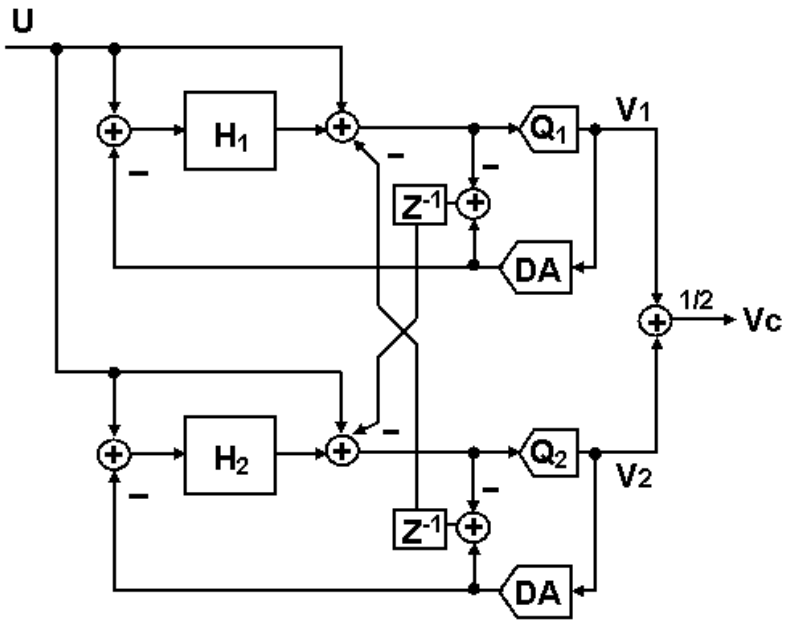


Fig. 3.1 Enhanced split architecture

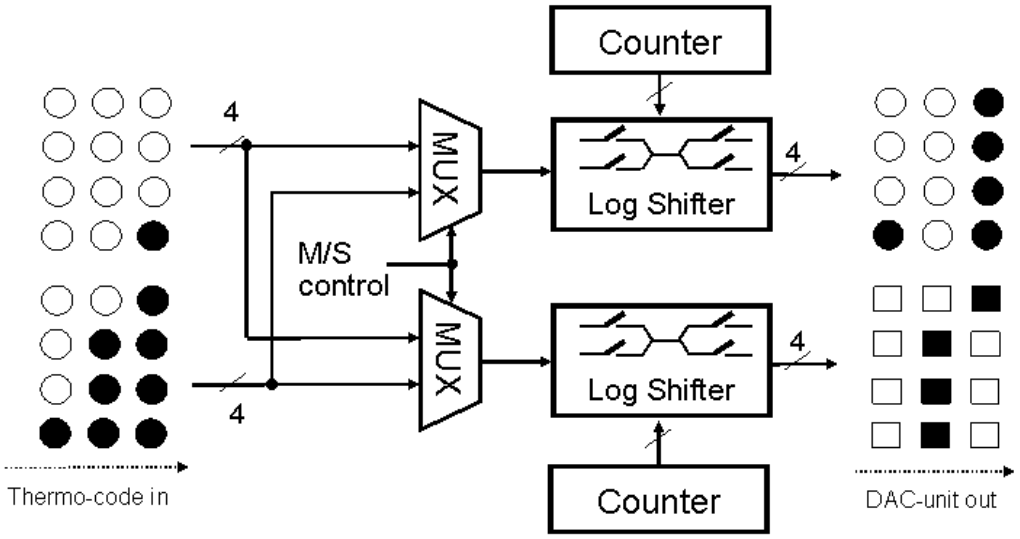


Fig. 3.2 Segmented data-weighted-averaging

3.2. Architectural design

A fully-differential dual-path structure, shown in Fig. 3.3, is employed for the reduction of common-mode errors in the system-level. The effects of common-mode error reduction were observed in the experiments of the first generation dual-path modulator.

Delayed-feed-in structure mitigates the timing constraint of feedback analog signal. Since a scrambling circuit remains in the feedback path in a multi-bit delta-sigma ADC to reduce the influence of the DAC mismatch error in the signal band, the gate delay of the scrambler is critical at a higher sampling rate. The half-time delay in the feedback path relaxes this timing constraint.

Dynamic range scaling of the active adder output requires the input-output transfer gain of the quantizer to equal 2. Two paths from the other modulator implement the quantization noise cross-coupling. One is from an auxiliary DAC output and another from the input of quantizer.

Due to the cross-couplings of the delayed quantization noises, the final output is

$$V = U + NTF\left(1 - z^{-1}\right)\left(\frac{Q_1 - Q_2}{2}\right) , \tag{3.3}$$

where $$NTF = \left(1 - z^{-1}\right)^2 . \tag{3.4}$$

Here, the noise transfer functions of +path and –path are assumed to be the same. Consequently, third-order noise shaping is realized in this circuit. Fig. 3.4 compares the output signals of a modulator with quantization noise cross-coupling and one without. Nine-level quantizer and an oversampling ratio (OSR) of 16 are assigned for the modulators. The simulated signal-to-(noise+distortion) ratio (SNDR) was 77.6-dB for the enhanced architecture, while 63.1-dB for the unenhanced one.

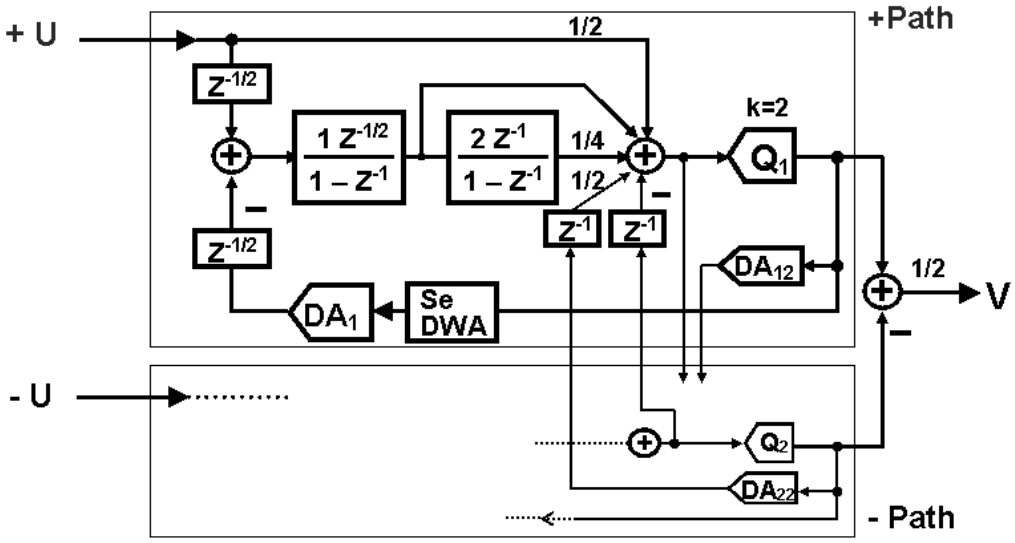
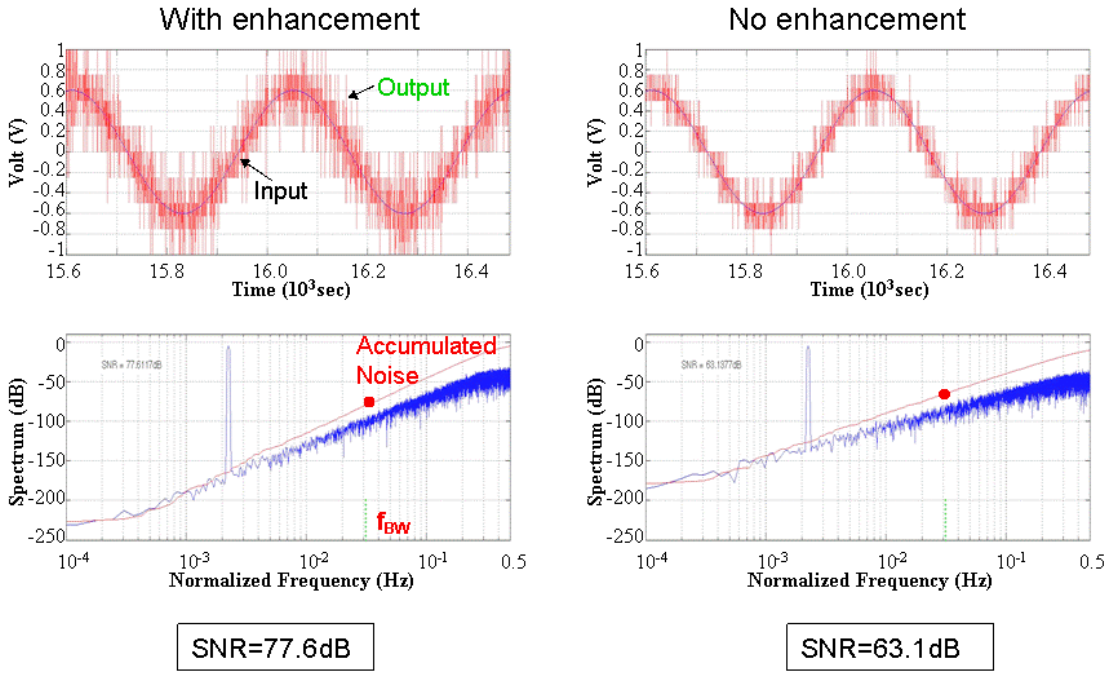


Fig. 3.3 Fully-differential enhanced modulator



(a) Enhanced modulator **(b) Unenhanced modulator**

Fig. 3.4 Comparison between modulator performances with and without enhancement

3.3. Enhancement block and supporting clock generator

The function of quantization noise cross-coupling is implemented in simple switched capacitor circuits. Fig. 3.5 indicates the switched capacitor implementation of the enhanced architecture. A single-ended circuit is shown here for simplicity; however, a fully-differential circuit is employed in the design. The enhancement block is incorporated into the active adder, which is vital for a low-distortion structure in order to avoid signal attenuation [25], [26]. The output of an auxiliary DAC is delayed by a digital latch, and the delayed output is added to the active adder in a similar way as for a front-end DAC. Another path from the quantizer input is delayed by switched capacitor circuits and the output charge is transferred to the other modulator by the cross connection. C_{FB2} with the surrounding switches and C_{FB3} with the surrounding switches are operated in a time-interleaved manner. At a time C_{FB2} holds the output charge and C_{FB3} transfers another charge, and vice versa. Neither channel mismatch error in the time-interleaved blocks, nor additional DAC mismatch errors produce major deterioration in the modulator performance, because of the location of the noise injection. The charge transfer functions described above are incorporated using additional clock signals, which are provided by the circuits shown in Fig. 3.6. Non-overlapping clocks (Φ_1 and Φ_2) and delayed clocks (Φ_{1d} and Φ_{2d}) are generated by using an established design methodology [27]. The output of the one-bit counter (Φ_{1ctr}) is used for a selection signal which creates 2-phase clock signals; for example, Φ_{11} and Φ_{12} from Φ_1. Two NAND gates detect a rising edge of clock signal Φ_{2d} and the following falling edge of clock signal Φ_1.

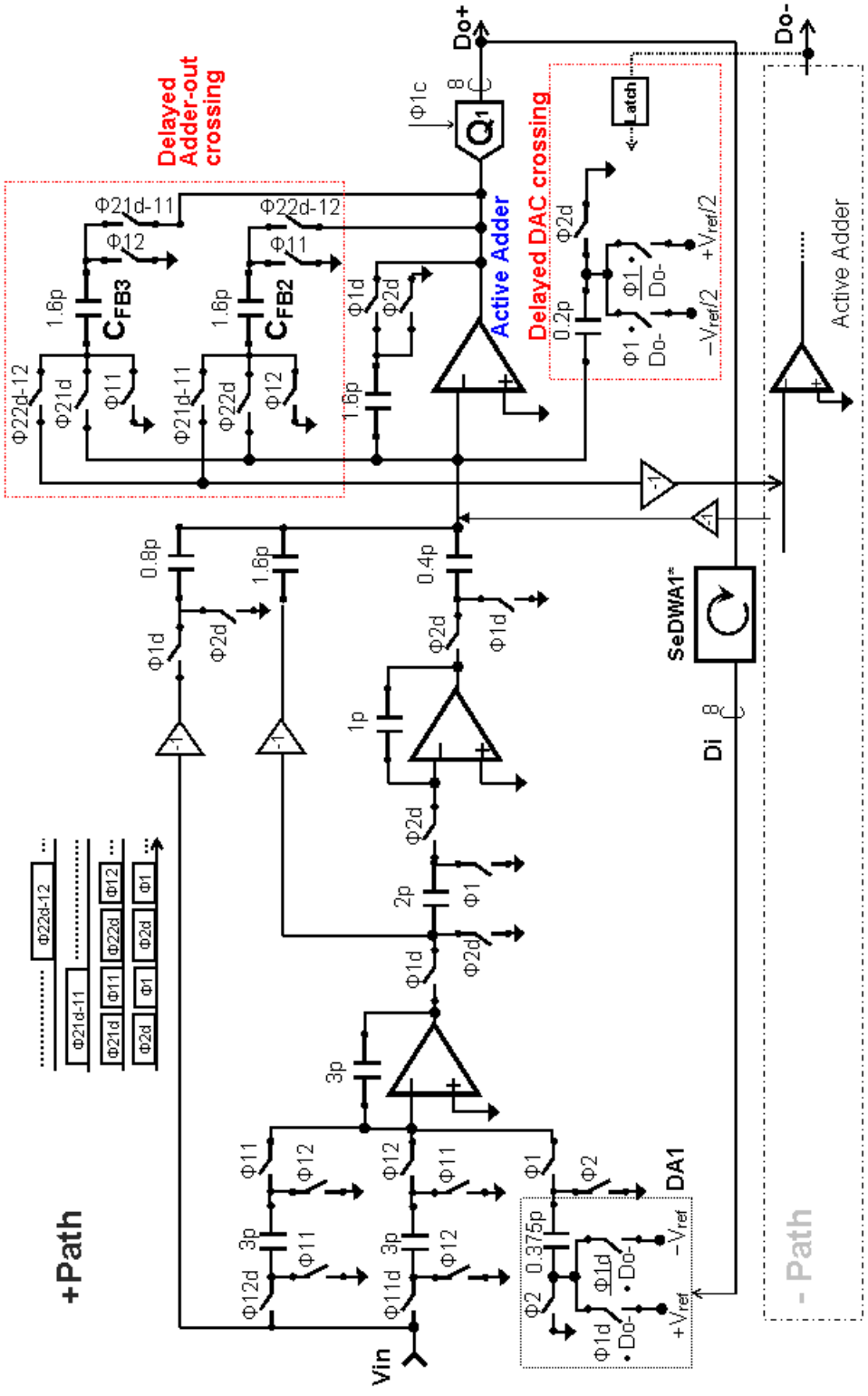


Fig. 3.5 Switched capacitor loop-filter implementation

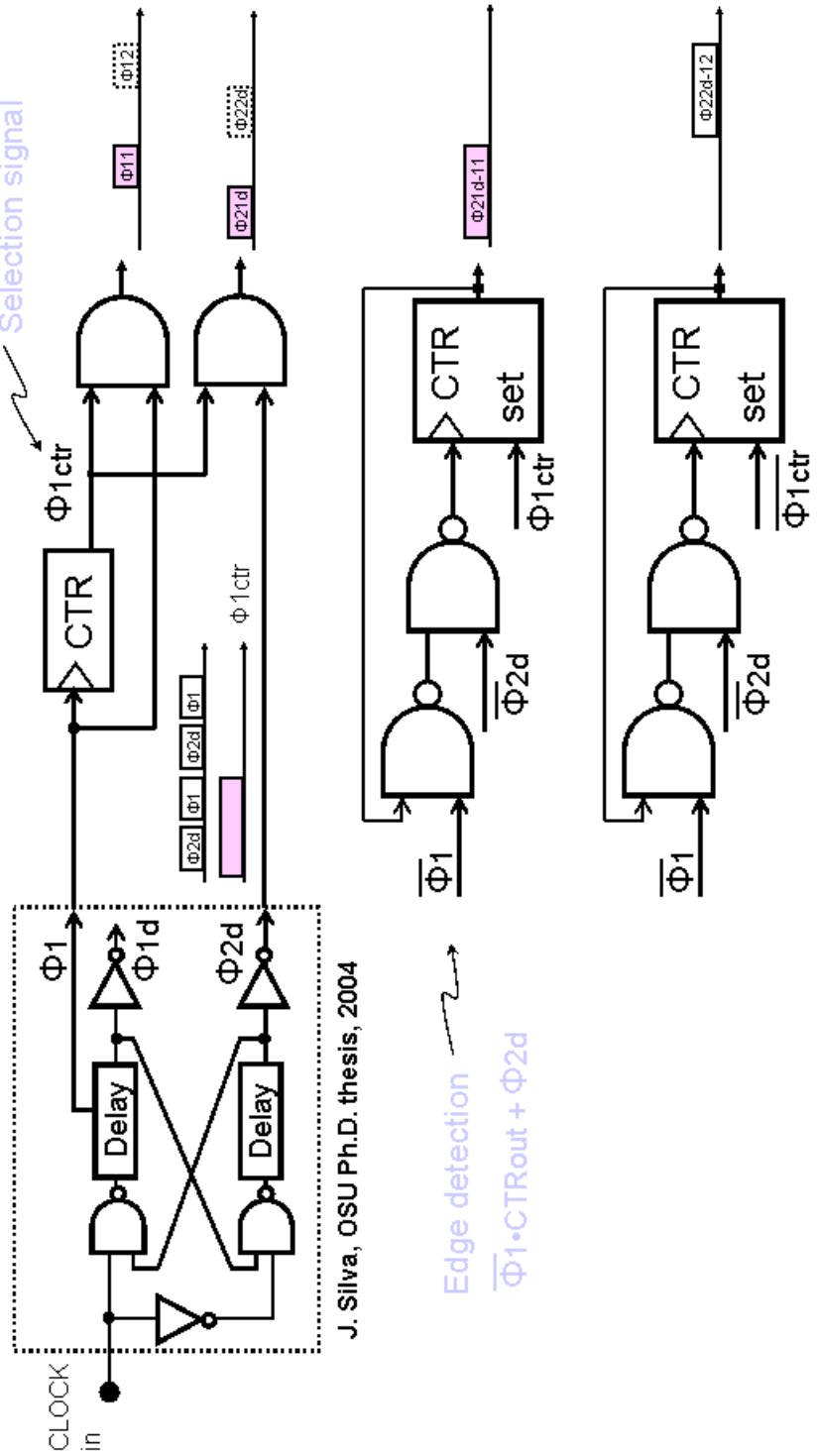


Fig. 3.6 Clock generator implementation

3.4. Circuit design

The front-end switched capacitor stage, which contains the first integrator and the Digital-to-Analog converter, is the most critical circuit in the modulator because front-end errors do not benefit from noise suppression. Since thermal noise from the front-end switched-capacitor is one of the dominant noise factors, the capacitor value is considered from the noise power permitted. Fig. 3.7 indicates the SNDR versus front-end capacitor value. The broken-line is the SNDR of large capacitor values for the comparison plot. Only thermal noises from the front-end sampling capacitors are included in the simulations. 3pF is picked for the actual value. Fig. 3.8 shows the THD versus front-end switch on-resistance value. For lower distortion (THD -80dB) with a margin, 120 ohm is targeted to the switch resistances. The slew-rate and gain-bandwidth of the integrator op-amp are examined by a behavioral simulation shown in Fig.3.9, where the op-amp DC gain is assumed to be 55dB, and no other non-ideality is included in the quantizers and DACs. More than 200V/μs normalized slew-rate is estimated for the first-stage op-amp. Based on the simulation, high bandwidth is not required and it is no more than 100MHz. However, following the general rule of thumb for 0.1-% settling [28], more than 142-MHz of bandwidth is estimated.

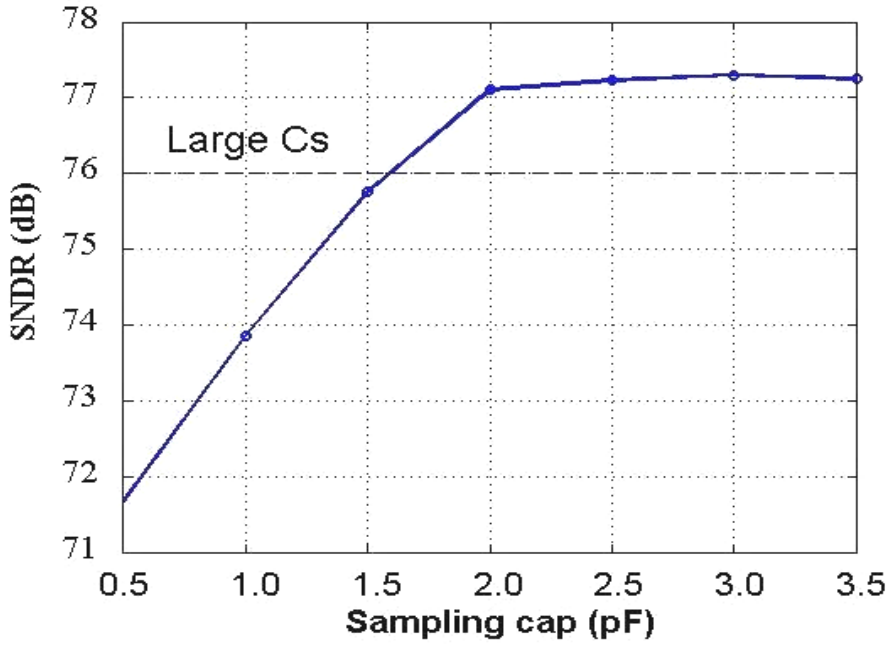


Fig.3.7 Sampling capacitor

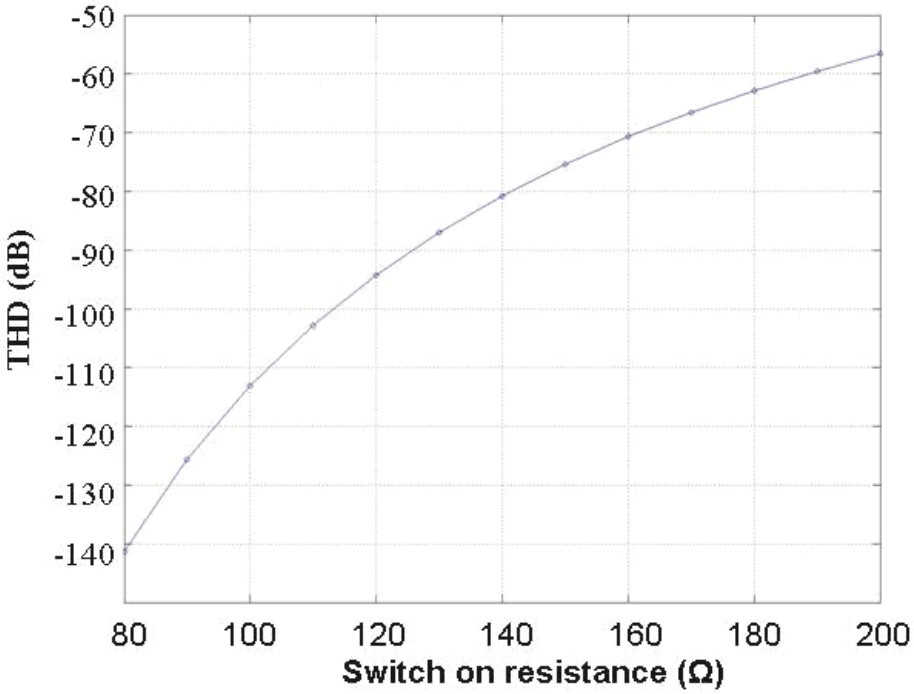


Fig.3.8 Switch resistance

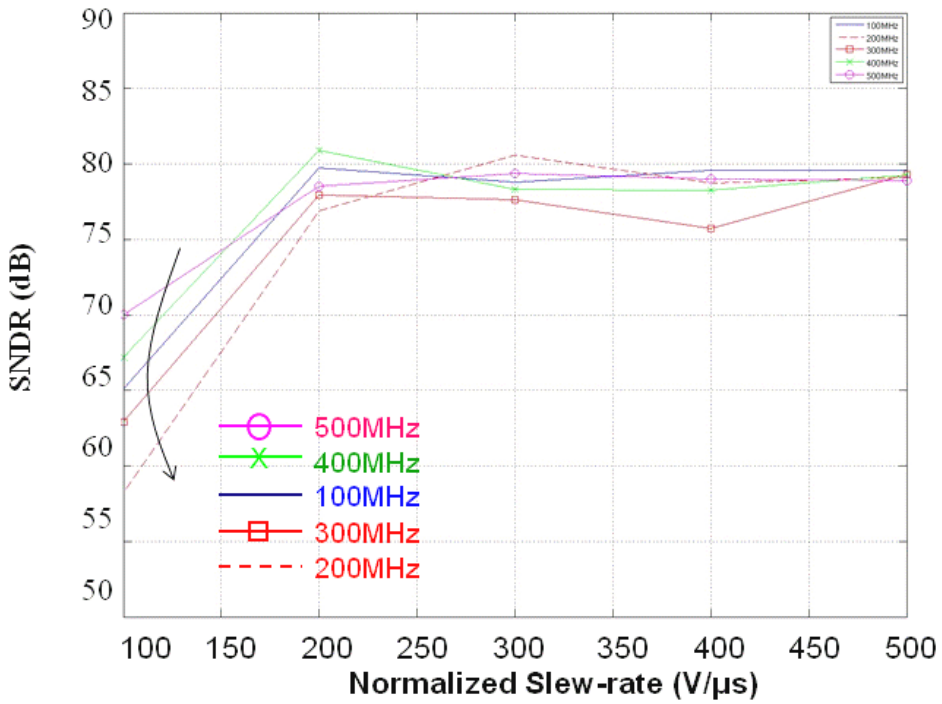


Fig.3.9 Op-amp gain-bandwidth and slew-rate

A gain-boosted folded-cascode topology is employed for the operational amplifier in the first stage integrator, which is shown in Fig. 3.10. A switched capacitor common-mode feedback (CMFB) circuit is employed in the amplifier. SPICE simulations indicate 61-dB DC gain, 194-MHz unity-gain frequency (78-degree phase margin) at integrating phase with 243-V/μsec of slew-rate and 1.96-nV/sqrt(Hz) input-referred noise density. Fig. 3.11 shows the unit comparator circuit, which is a key element of the quantizer block. Gain-boosting is applied to the preamp in order to reduce the effect of the latch offset. Auto-zero technique reduces the residual input offset of the comparators. The comparator function was verified by a SPICE simulation for the 64-MHz sampling frequency.

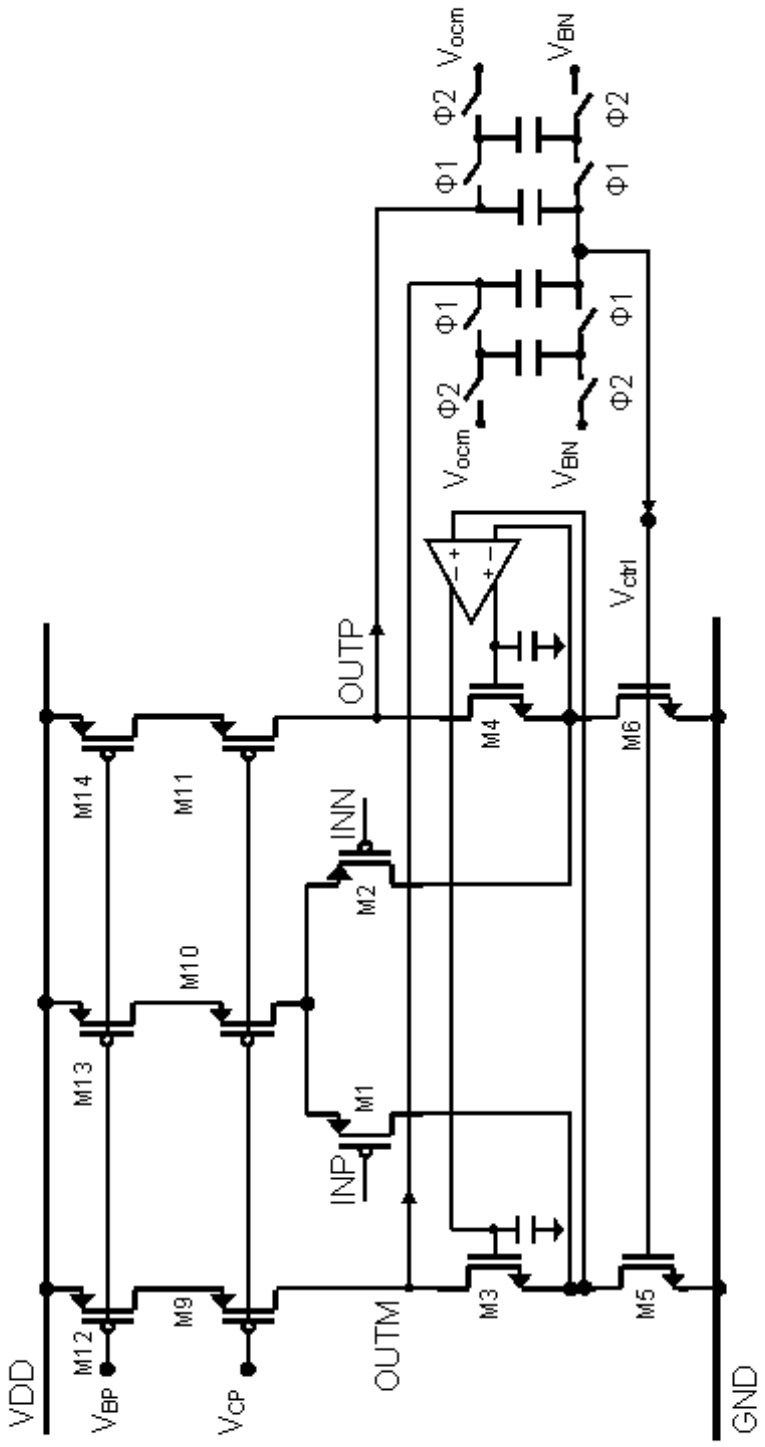


Fig. 3.10 Operational amplifier

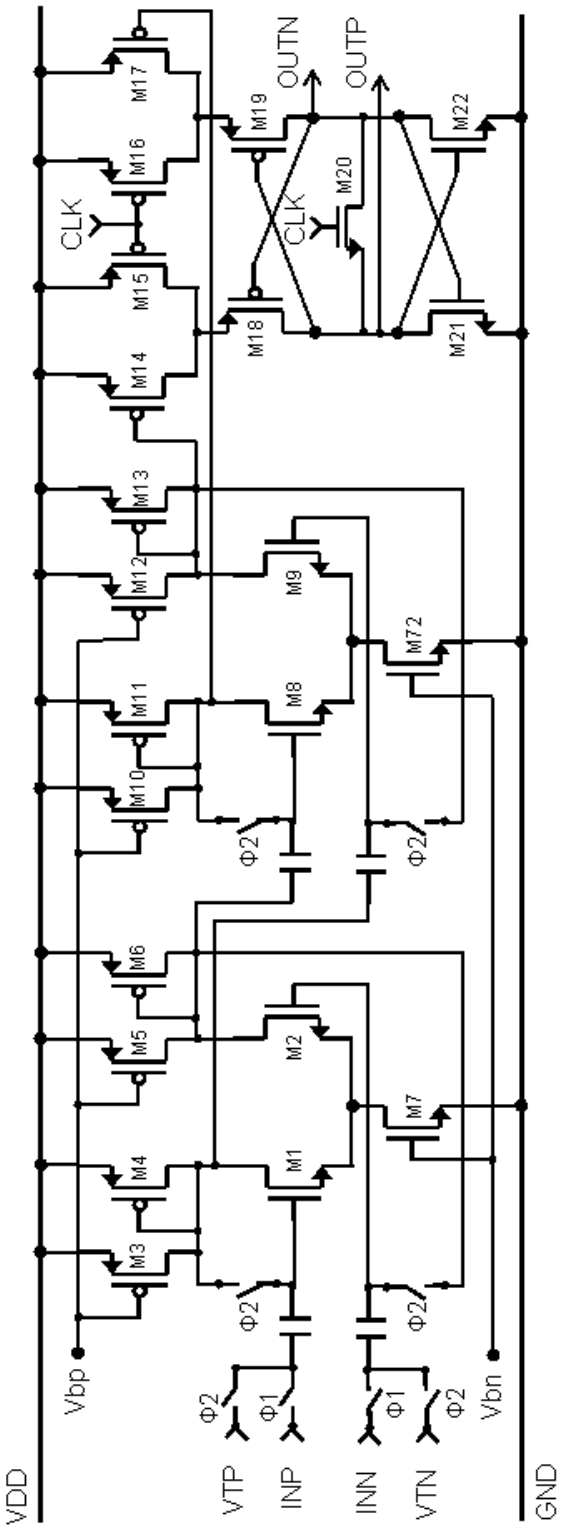


Fig. 3.11 Comparator

CHAPTER 4. EXPERIMENTAL RESULTS

For the enhanced dual-path Delta-Sigma A/D converter described in the last chapter, two circuits were fabricated to verify the performance. One is the core circuits in the modulator, which are the analog operational amplifiers used for the integrators. Another is the whole delta-sigma modulator. In this chapter, the test setups and experimental results of these circuits are described. The first section describes experiments with the op-amps, followed by experiments with the whole modulator in section 4.2.

4.1 Operational amplifier experiments

The operational amplifiers (op-amps) used in the modulator were tested in order to check their functionalities. Two types of op-amps are employed in the loop-filter, as described in the previous chapter. One is a gain-boosted folded-cascode amplifier with a switched capacitor common-mode feedback circuit (CMFB), which is called op-amp 1. Another is a lower-power folded-cascode amplifier with a continuous-time CMFB circuit, which is called op-amp 2. For the purpose of the experiments, a white board is used and the peripheral components are built in it. The board is shown in Fig. 4.1. The test set-up is described in the following, and it is shown in Fig.4.2. The DC voltage is provided to the inverting input while a sine wave signal is connected to the non-inverting input. A low-frequency signal can be provided from an HP3325B, while a higher-frequency signal from an Agilent 8665A. Two

phases of a clock signal are provided from an AWG420. One voltage supply is necessary for the experiment. Analog outputs are acquired by a digital oscilloscope TDS380 and the data plotted by MATLAB software. Fig. 4.3 shows the die photograph of op-amps.

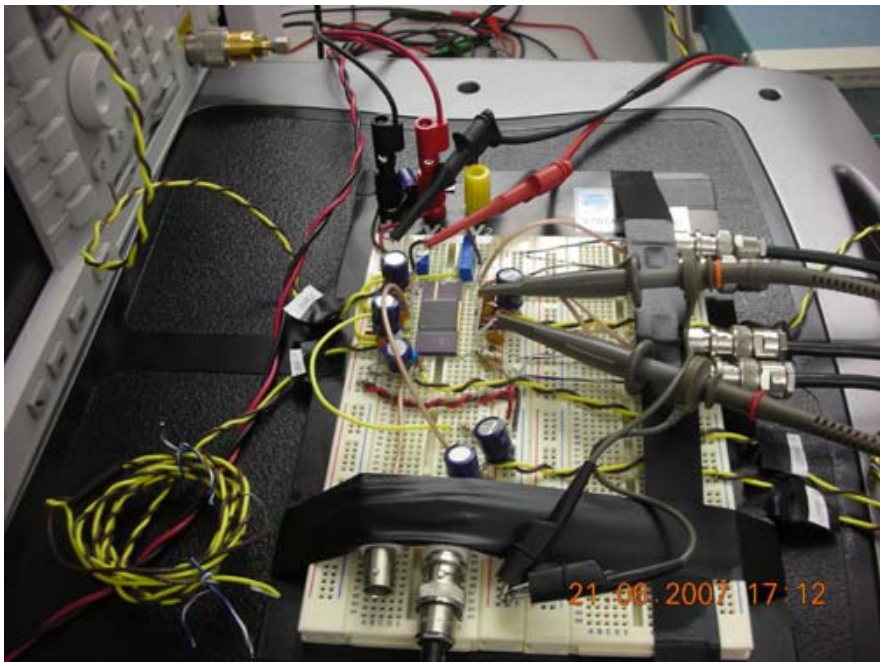


Fig. 4.1 Experimental board

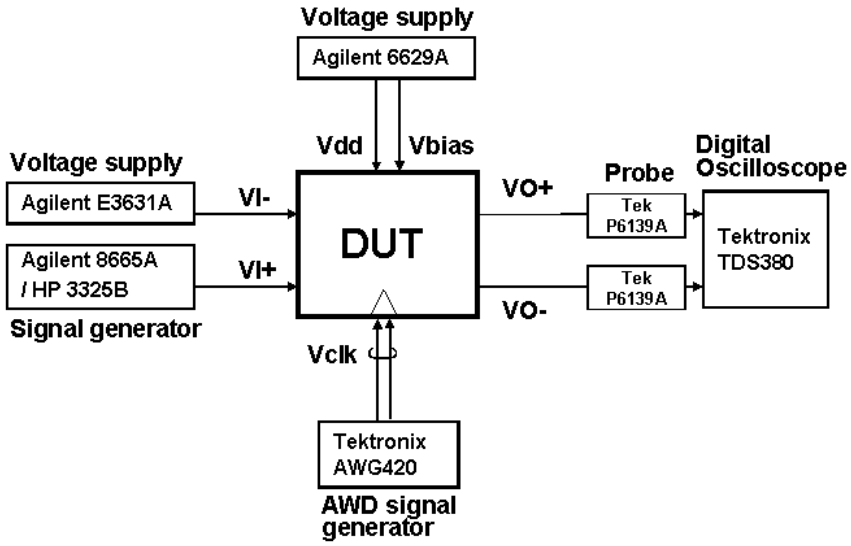


Fig.4.2 Test set-up

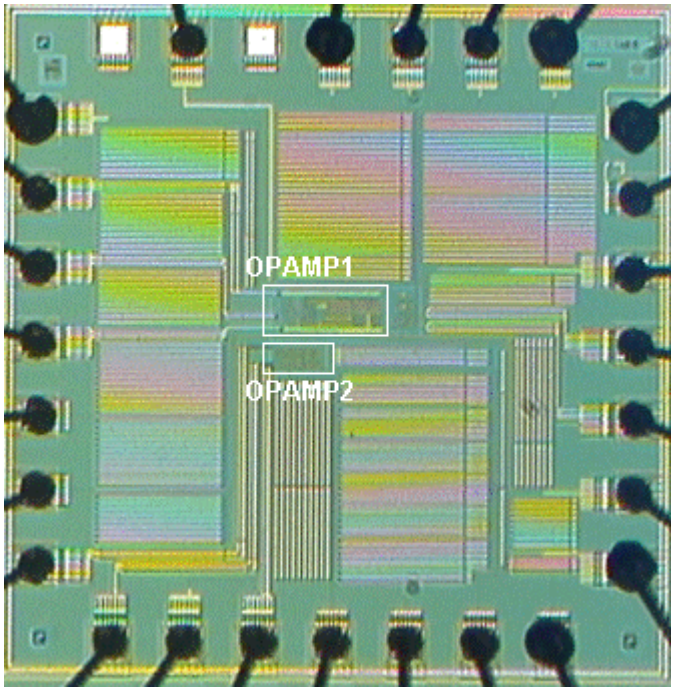
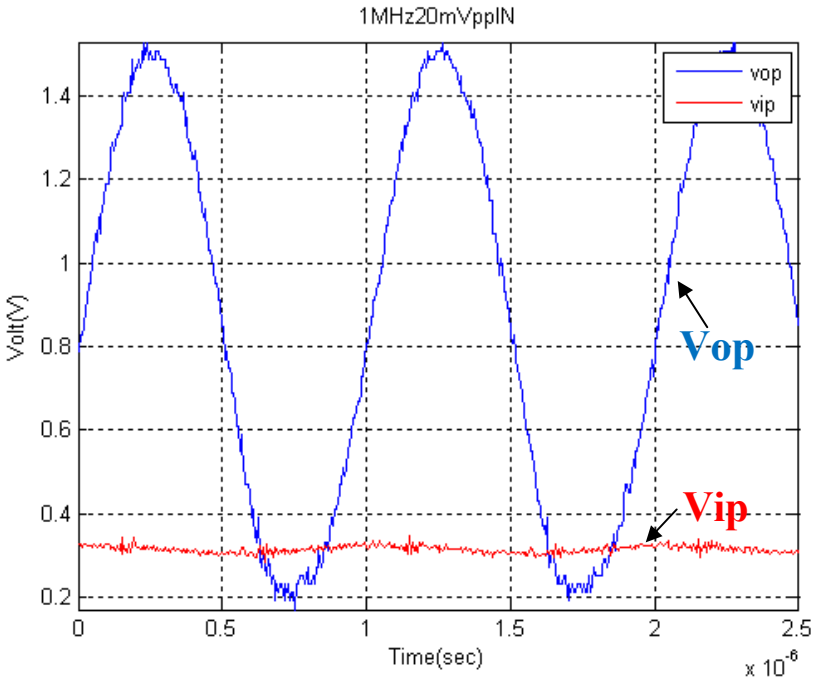


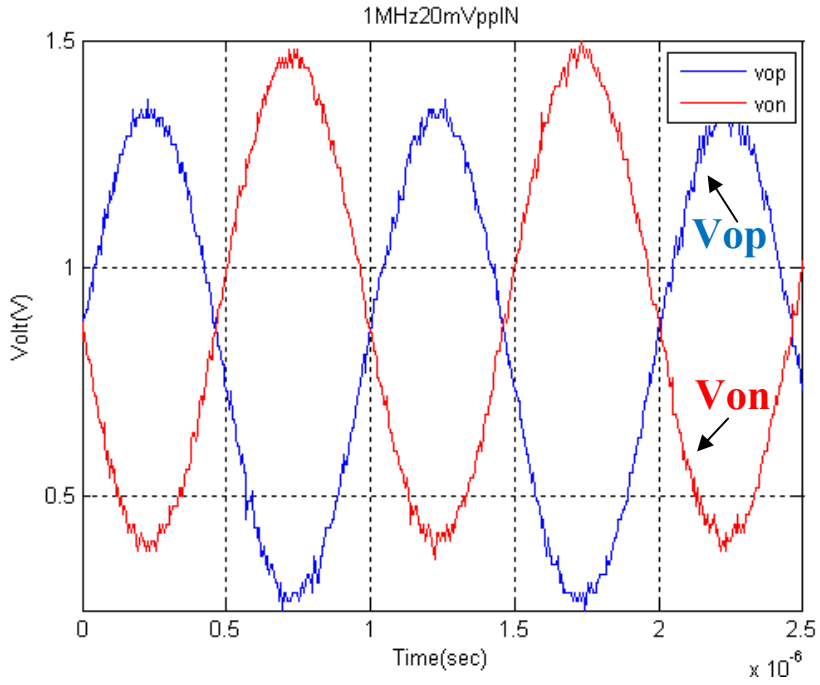
Fig.4.3 Die photograph

Fig. 4.4 (a) shows the non-inverted output signal for a 20-mVpp input signal. More than 40-dB of voltage gain is achieved. The output common-mode voltage is about 0.9-V, as shown in Fig. 4.4 (b), which is expected from the simulation. Fig.4.5 (a) and (b) shows the output signals and clock signal for the common-mode feedback circuit. Although some spikes can be seen in the outputs because of the switched capacitor CMFB, the output is usable. Fig.4.6 to Fig.4.11 show the output and input signals observed for input signals of several frequencies. Fig.4.12 summarizes the frequency response of the op-amp 1 and it is compared with the simulation results. Since probe Tek6139A has 8pF of input capacitance, 13pF to 18pF load capacitance is assumed to the op-amp simulations. As shown in Fig. 4.12, there exist some discrepancies between simulation and measurement data, which can be reflected on the decrease of few dB gain.

And the measured bandwidth is found to be lower than the simulation one. The reason of this may be caused either by a reduced trans-conductance of transistor device or by an inaccurate simulation model which fails to completely match with the real device. Figures 4.13 to 4.20 show time-domain experimental results and frequency-domain results of op-amp 2. As seen in Fig. 4.20, the DC gain is less than the simulation result by about 5dB. This is because of the parasitic resistance in the continuous-time CMFB in op-amp 2. The finding is similar as op-amp 1 in that some discrepancies also existed between simulation and measurement data, which can be reflected on the gain reduction.

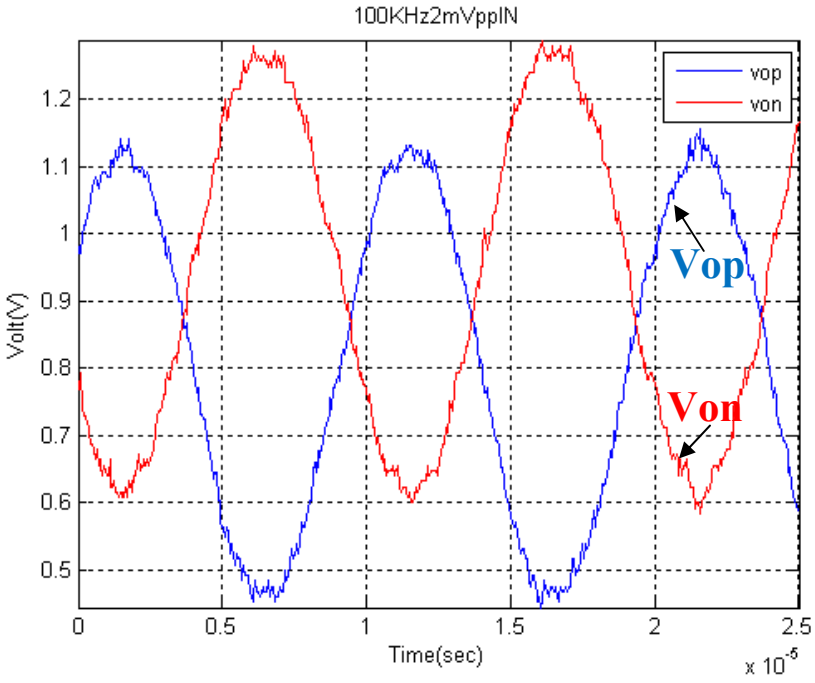


(a) Output and input signals

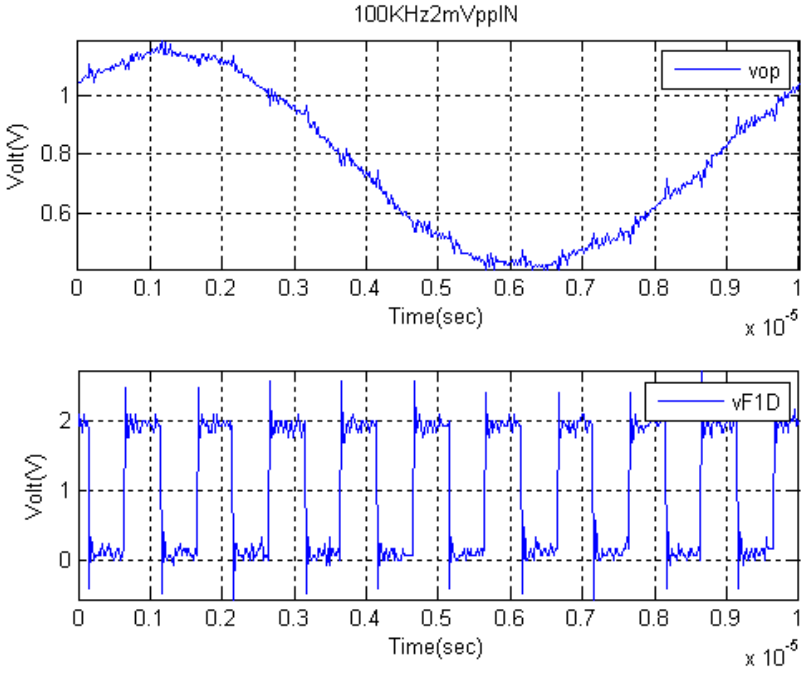


(b) Output signals

Fig.4.4 Time-domain experimental results for a 1-MHz input (op-amp 1)



(a) Output signals



(b) Output and clock signals

Fig.4.5 Time-domain experimental results for a 100-kHz input (op-amp 1)

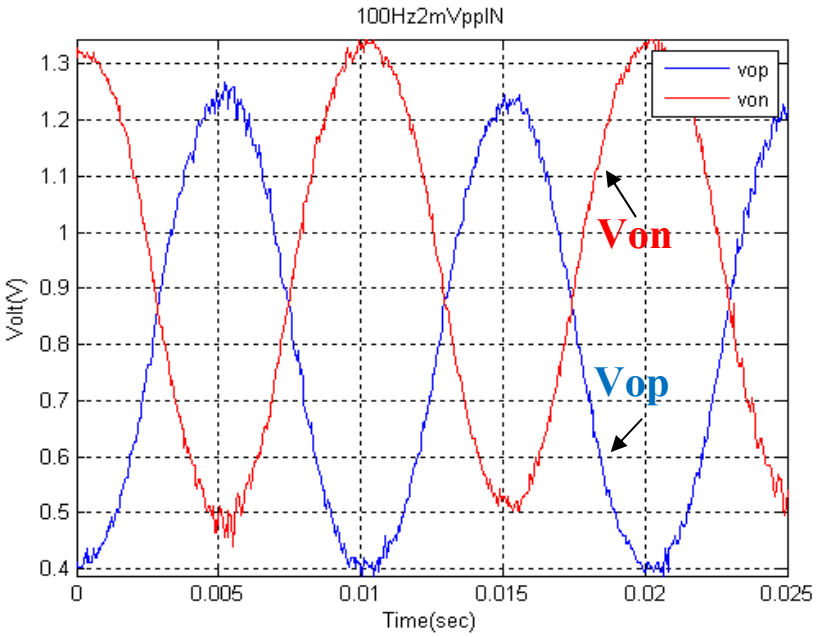


Fig.4.6 Time-domain experimental results for a 100-Hz input (op-amp 1)

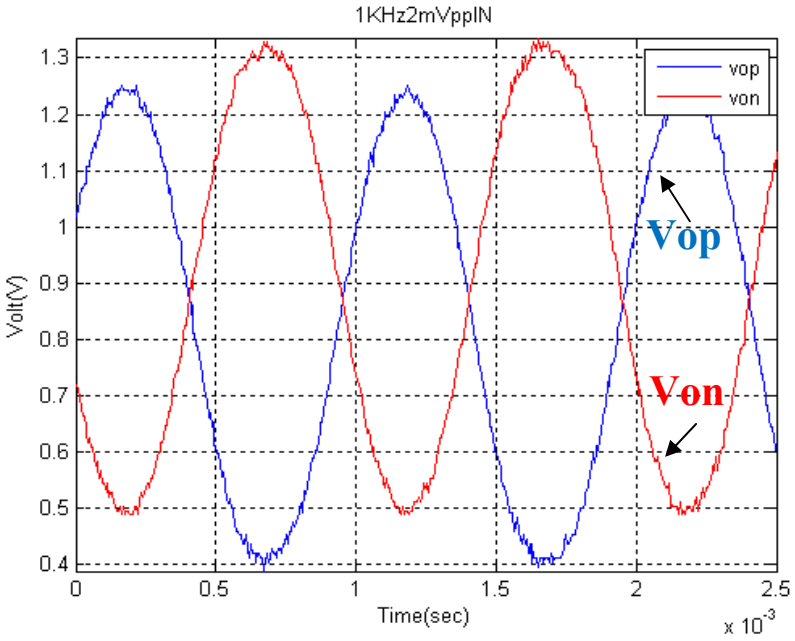


Fig.4.7 Time-domain experimental results for a 1-kHz input (op-amp 1)

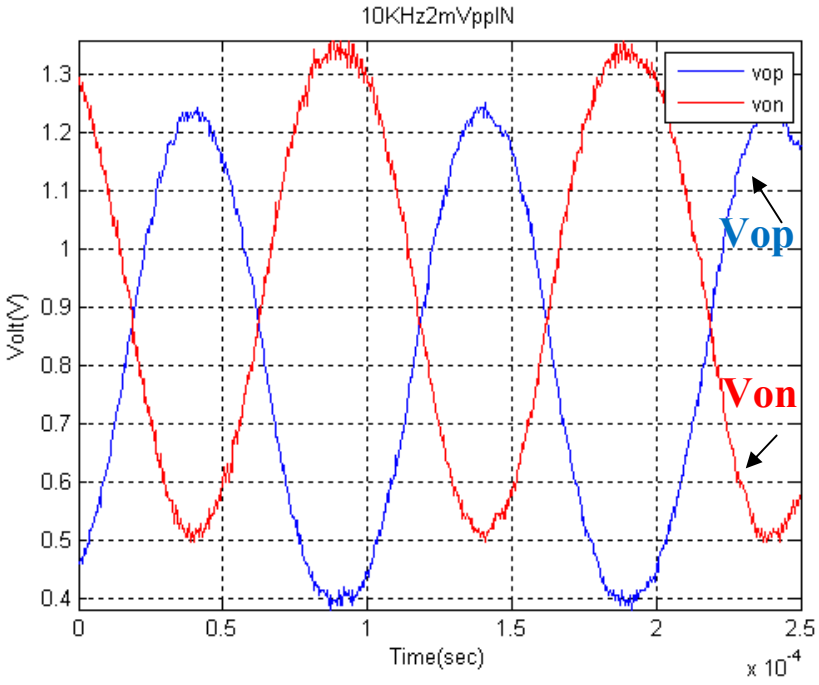
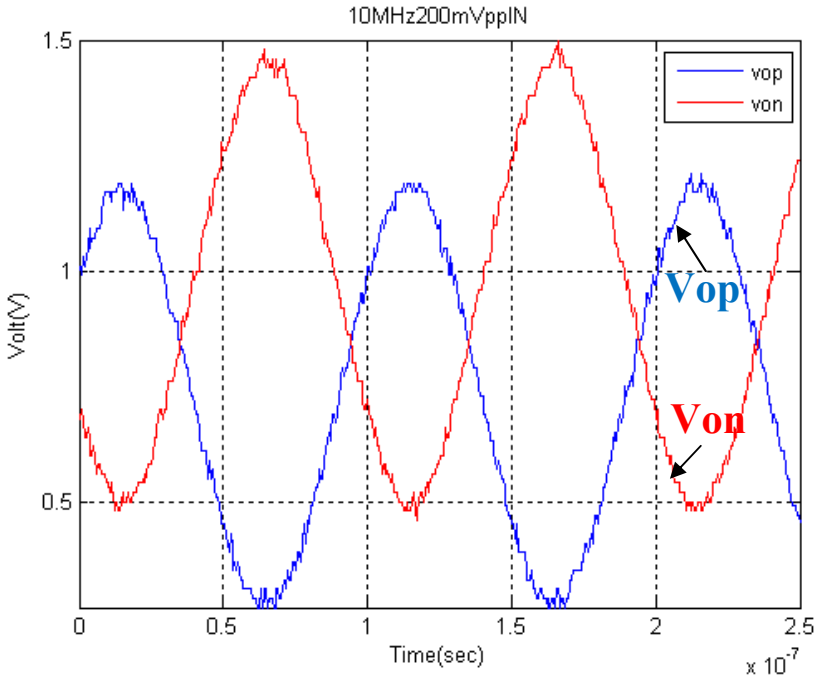
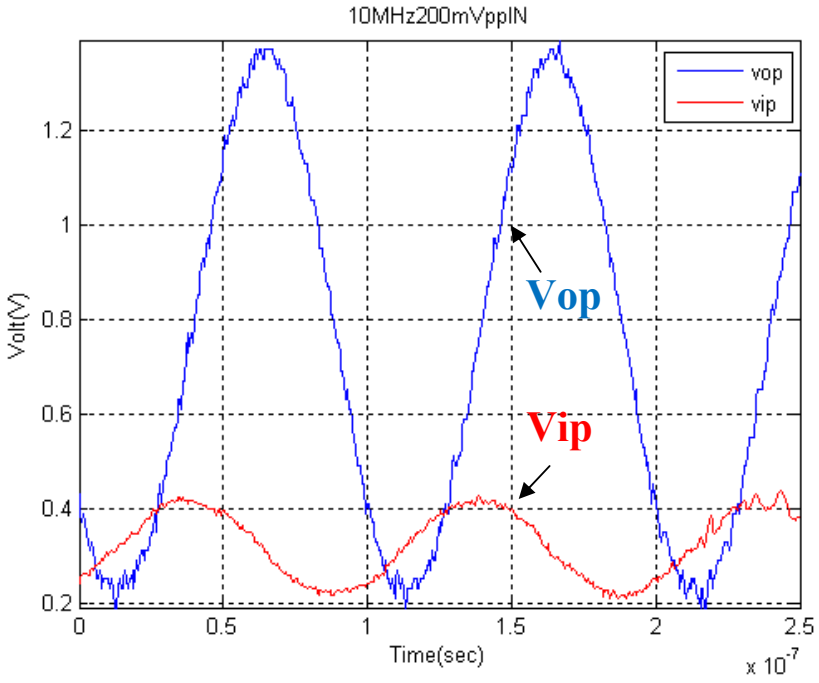


Fig.4.8 Time-domain experimental results for a 10-kHz input (op-amp 1)



(a) Output signals



(b) Output and input signals

Fig.4.9 Time-domain experimental results for a 10-MHz input (op-amp 1)

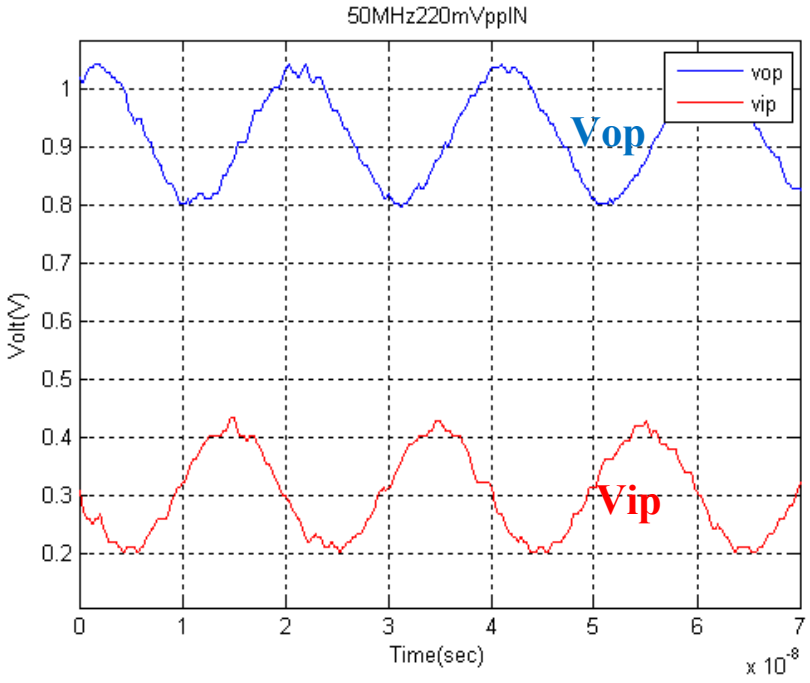


Fig.4.10 Time-domain experimental results for a 50-MHz input (op-amp 1)

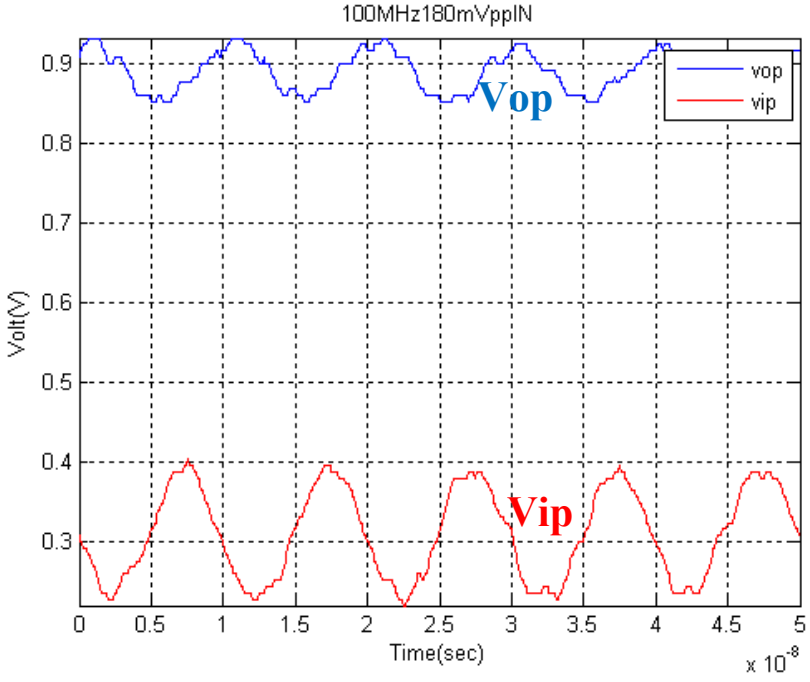


Fig.4.11 Time-domain experimental results for a 100-MHz input (op-amp 1)

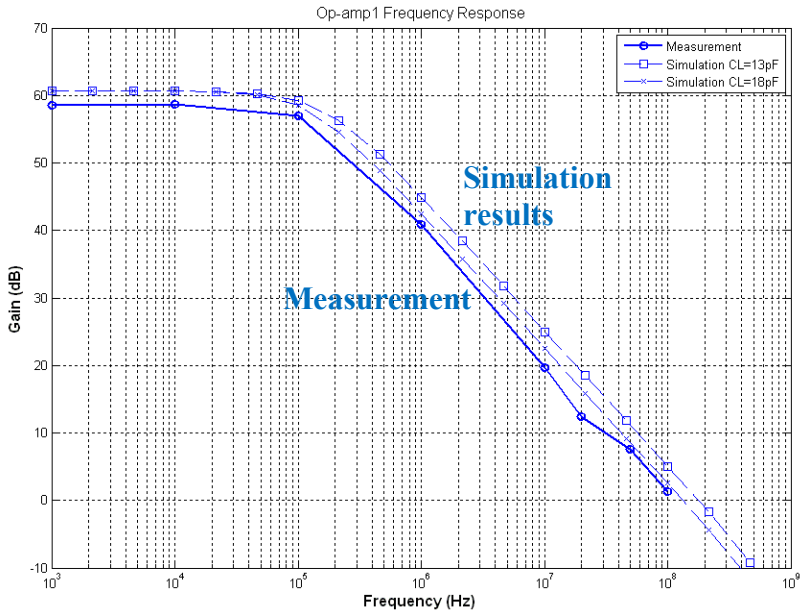


Fig.4.12 Frequency-domain experimental results (op-amp 1)

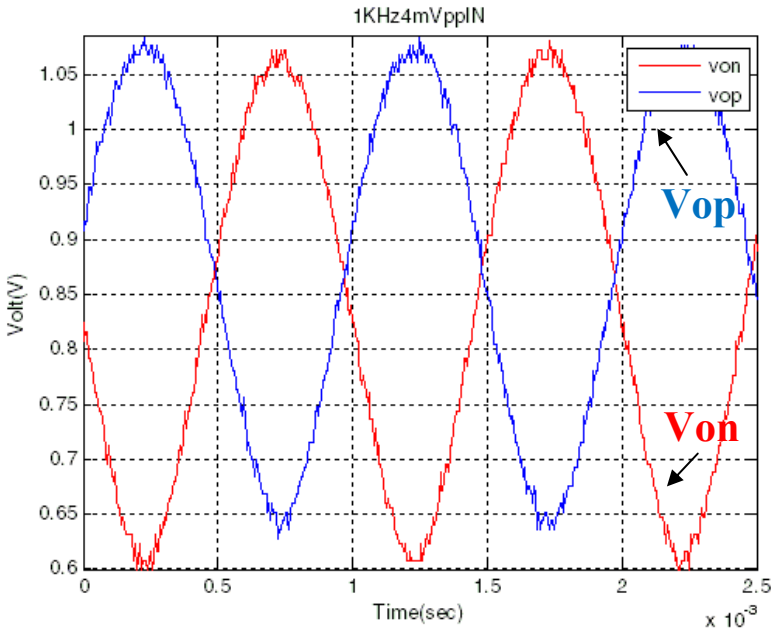


Fig.4.13 Time-domain experimental results for a 1-kHz input (op-amp 2)

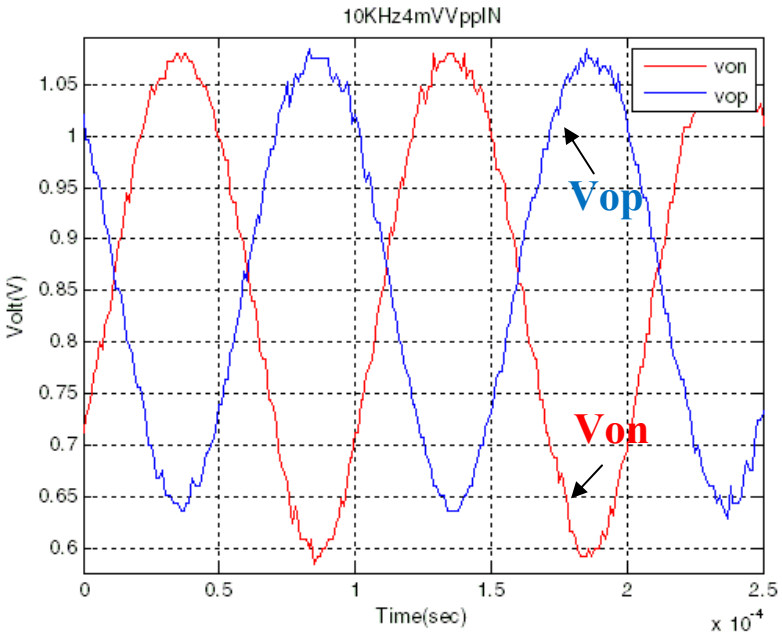


Fig.4.14 Time-domain experimental results for a 10-kHz input (op-amp 2)

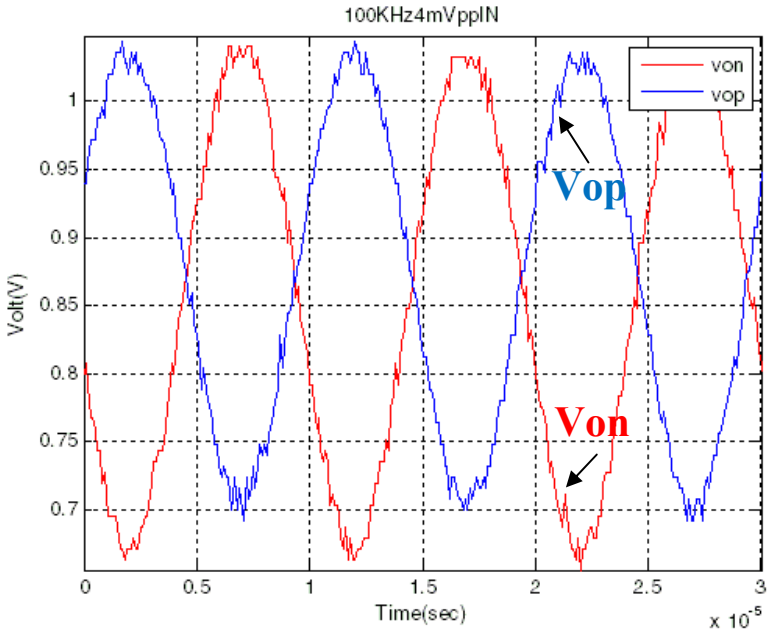
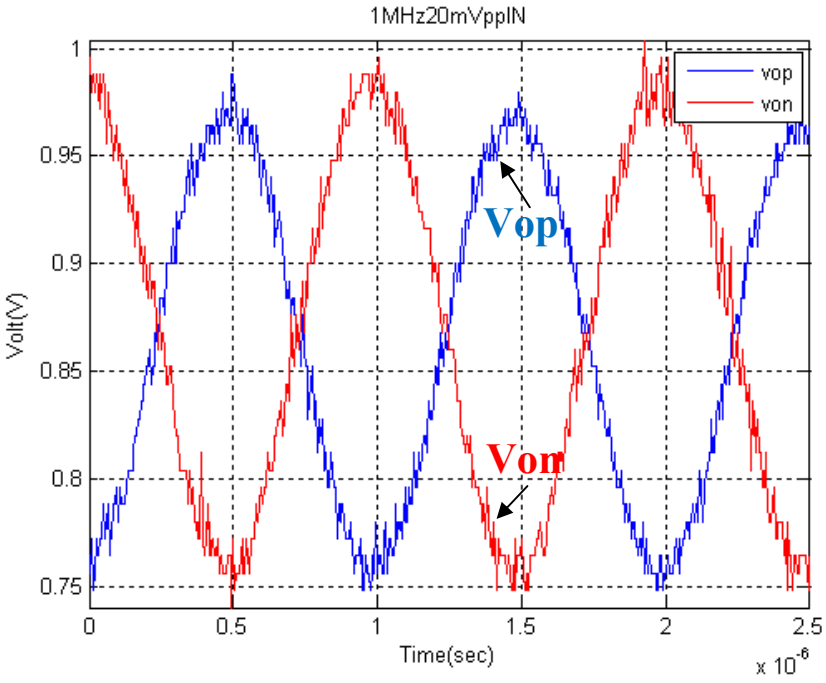
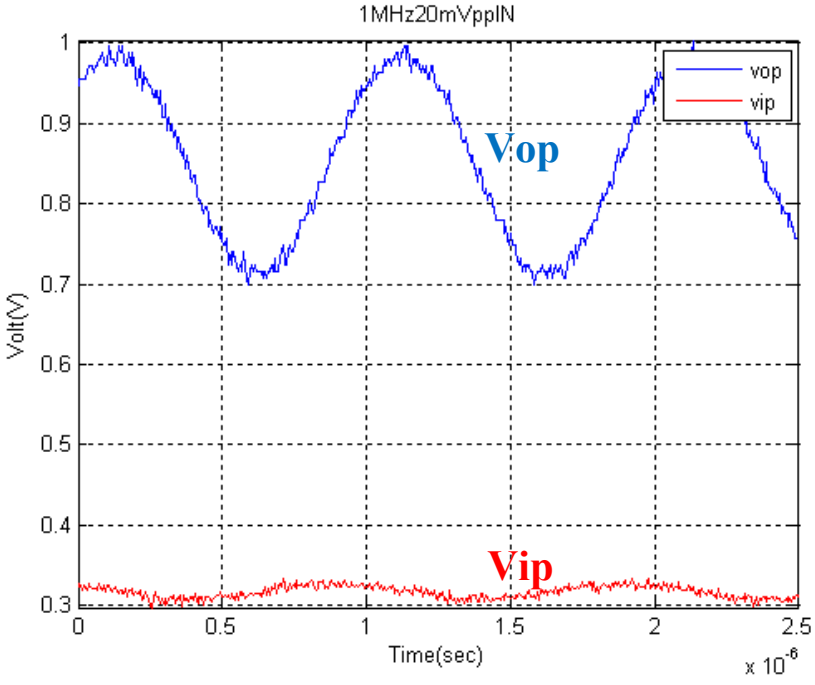


Fig.4.15 Time-domain experimental results for a 100-kHz input (op-amp 2)

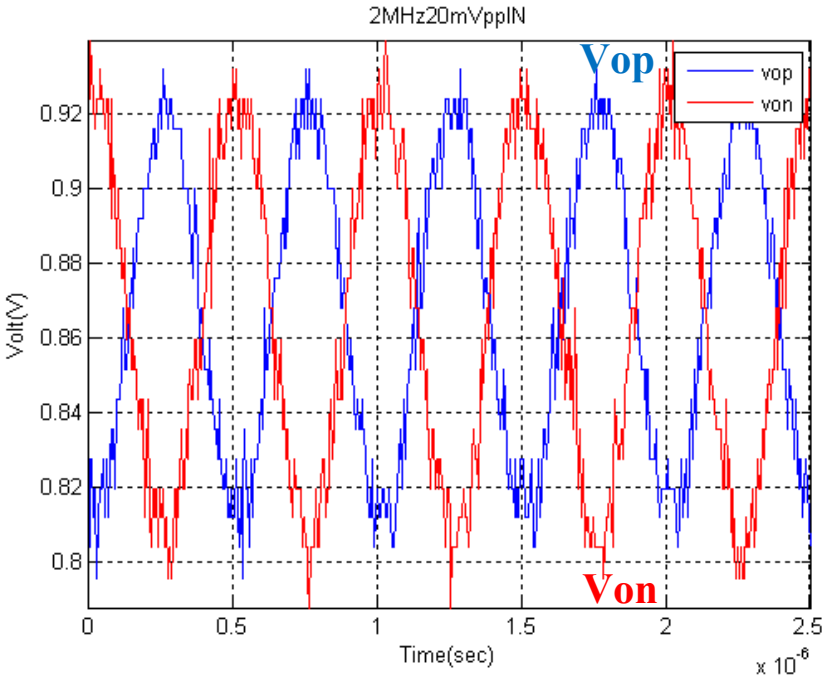


(a) Output signals

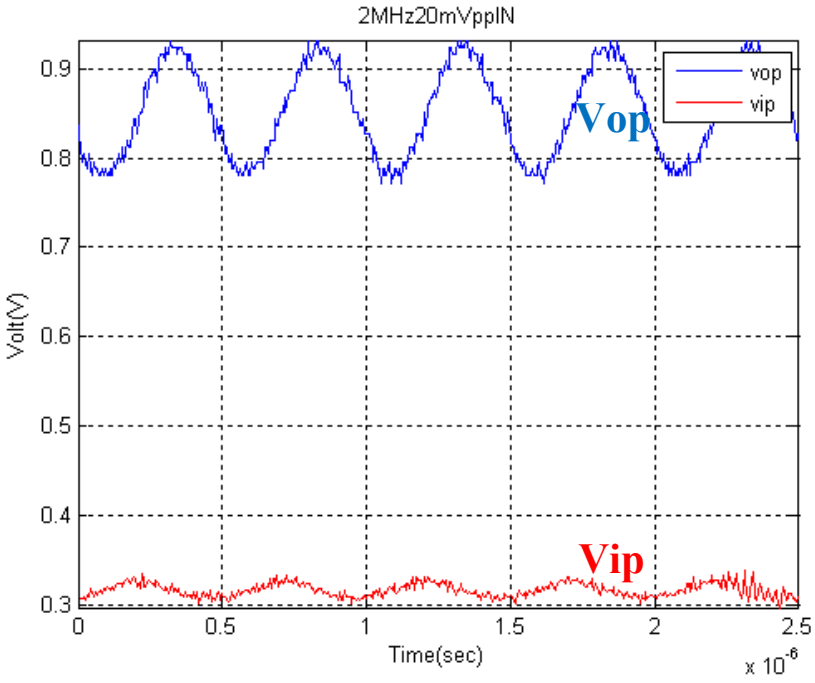


(b) Output and input signals

Fig.4.16 Time-domain experimental results for a 1-MHz input (op-amp 2)

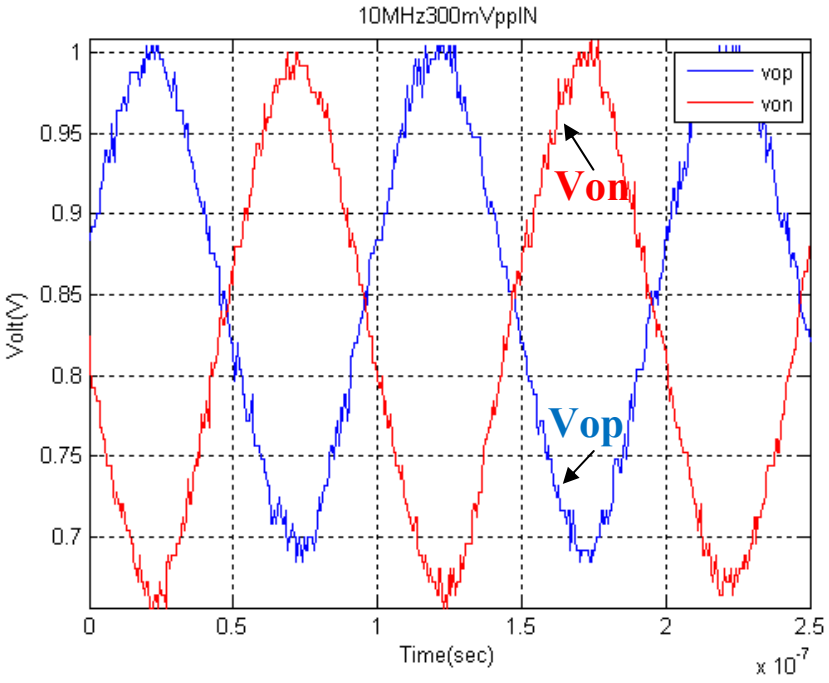


(a) Output signals

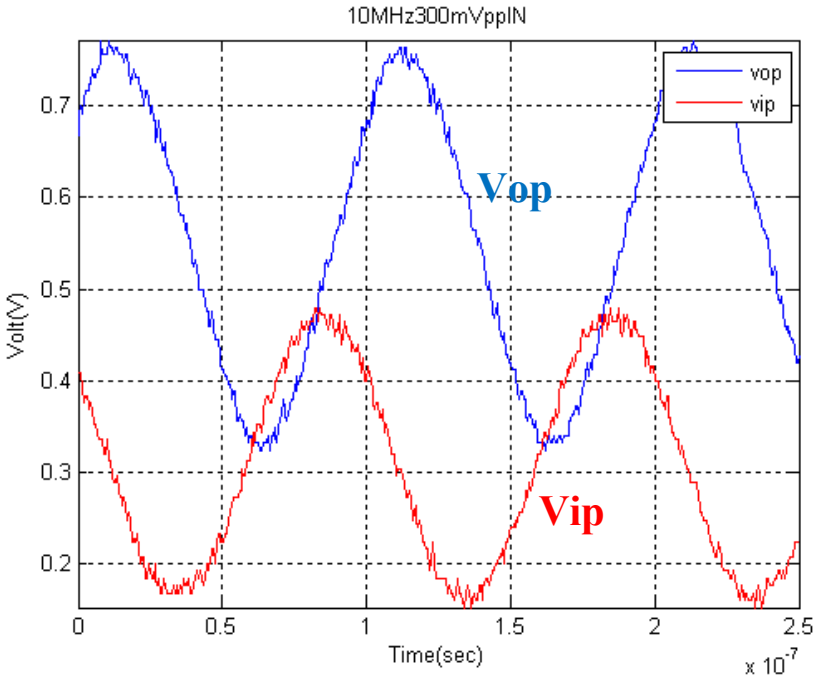


(b) Output and input signals

Fig.4.17 Time-domain experimental results for a 2-MHz input (op-amp 2)



(a) Output signals



(b) Output and input signals

Fig.4.18 Time-domain experimental results for a 10-MHz input (op-amp 2)

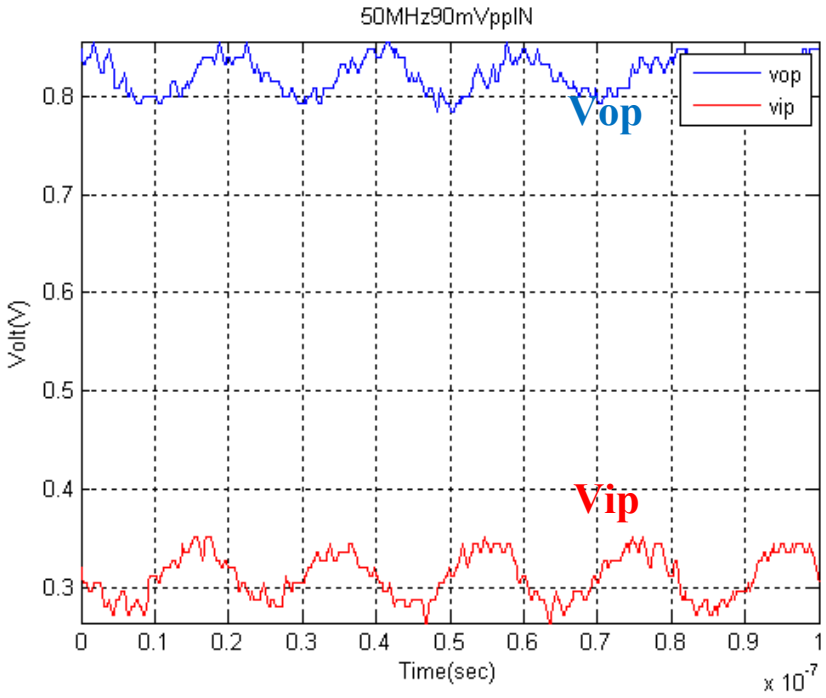


Fig.4.19 Time-domain experimental results for a 50-MHz input (op-amp 2)

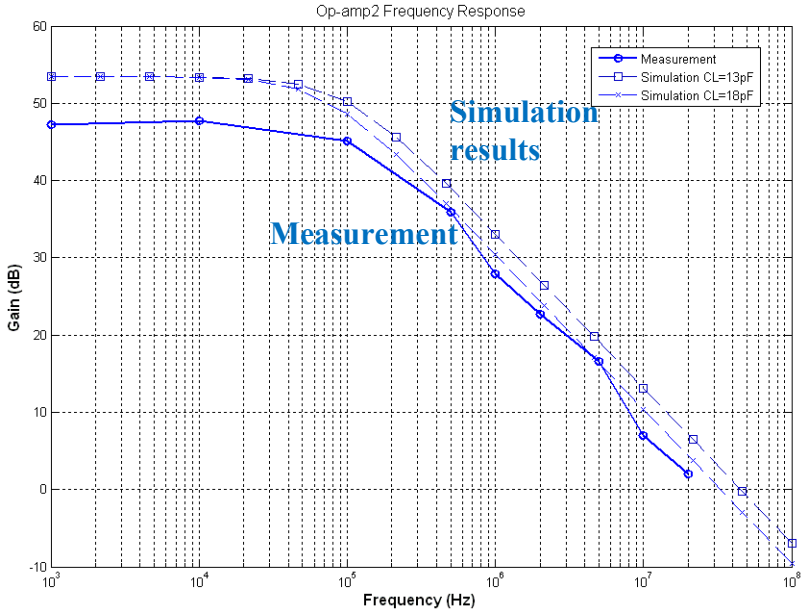


Fig.4.20 Frequency-domain experimental results (op-amp 2)

4.2 Delta-sigma A/D converter experiments

A 4-layer printed circuit board (PCB) was designed and fabricated in order to test the performance of the A/D converter. The board is shown in Fig. 4.21. Both top and bottom layers are used for signal routes, while inner layers (2^{nd} and 3^{rd} layers) are implemented for ground and power planes, respectively. A single plane is applied to both analog and digital ground, not separate planes, in order to avoid return current problems [29]. Several considerations were taken in the layout design to lower the noise in the board [30], [31]. Power supply voltages are provided by a low noise voltage regulator through ferrite beads, and a 10uF tantalum capacitor was used for reducing low-frequency noise. Moreover, ceramic capacitors are placed close to the chip to suppress high-frequency noise. All analog reference voltages are driven by commercialized current-feedback op-amps. Differential input signals are traced symmetrically and in a short lead straight to the chip inputs. A clock signal is also provided at a short distance with shield lines on both sides, since a longer trace of the clock signal generates more interference noise. The digital block is surrounded by a shielded line to absorb digital noise. Sharp corners are avoided to reduce EM (electromagnetic) noise.

The test set-up for the prototype chips is described in what follows and it is shown in Fig.4.22. Low-frequency high-accuracy differential signal can be provided from the Audio Precision (AP), while higher-frequency single-ended signal from radio frequency (RF) generator. The single-ended signal is filtered by the passive band-pass filter components and converted to fully-differential signal inside the PCB. A clock

signal is provided by the RF signal generator. Two voltage supplies are necessary for the PCB; one is +1.8V and another is +/- 5V. In order to drive the logic analyzer, the ADC outputs are buffered by a commercial CMOS driver. The acquired data are analyzed by MATLAB software. Fig. 4.23(a) and (b) show the die photograph and the one path modulator photograph, respectively.

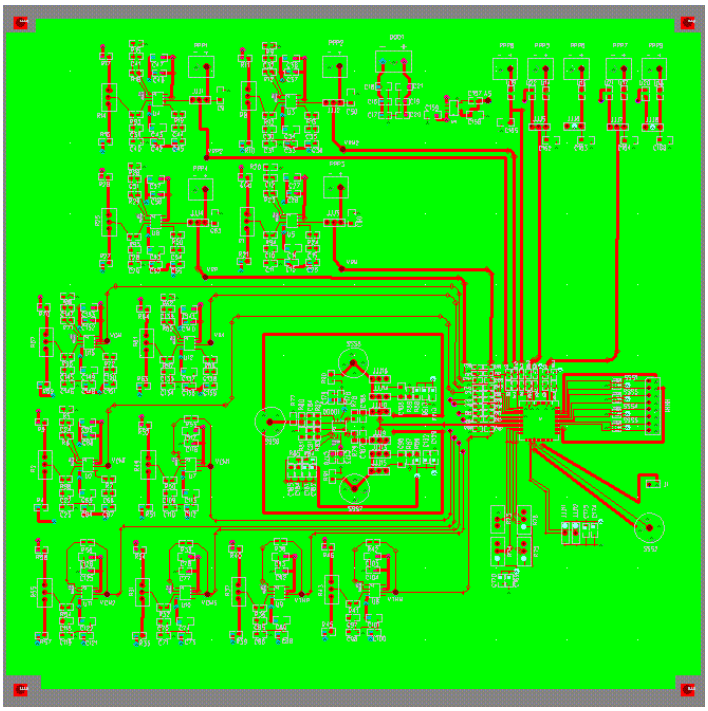


Fig. 4.21 Printed circuit board

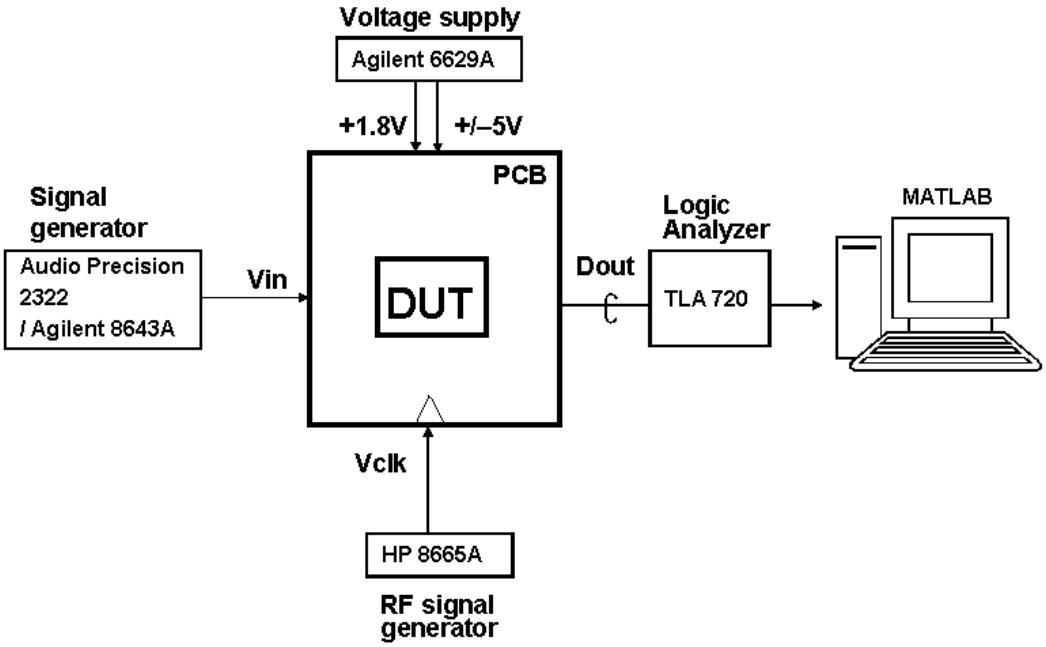
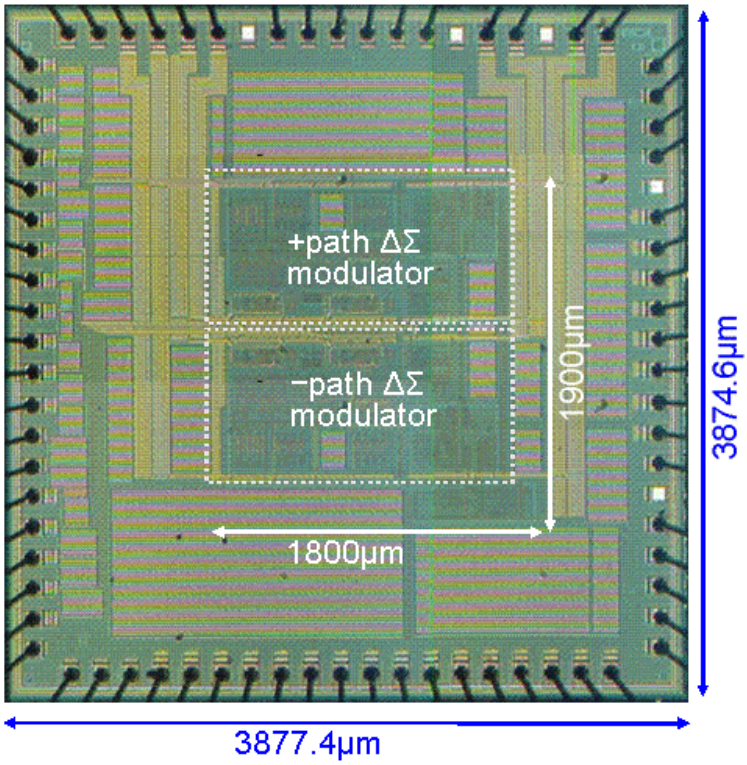
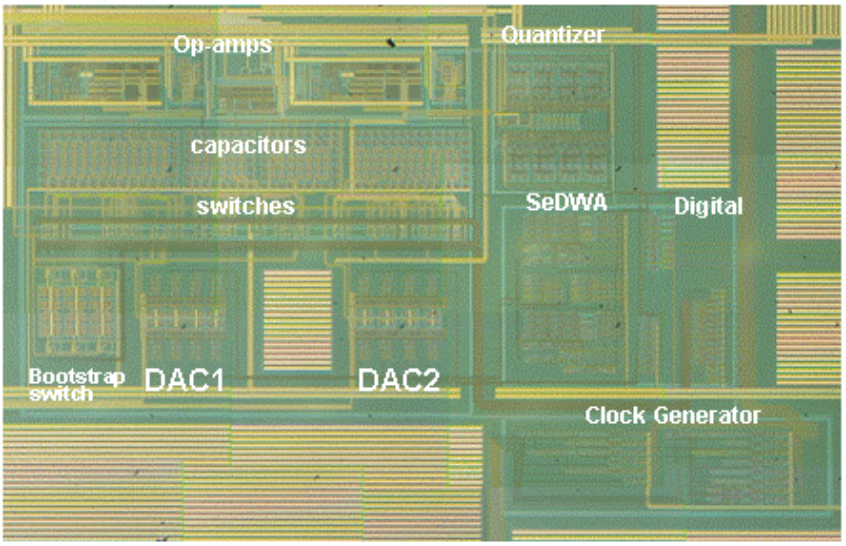


Fig. 4.22 Experimental set-up



(a) Die photograph



(b) One path modulator photograph

Fig. 4.23 Photographs

Fig. 4.24(a) and (b) show the time-domain outputs and the output spectrum of the modulator when a -4.5dB input signal is applied, respectively. When the input frequency is 100kHz with a sampling frequency of 40MHz, a 72dB SNDR can be achieved. In the measurement, the oversampling ratio is 16 and the bandwidth is 1.256MHz. The measured SNDR (i.e., 72dB SNDR) is lower than the expected value acquired from the simulation. Relevant reasons are stated in later paragraphs. Despite of lower measured SNDR, the value of this experiment proves circuit functionality since the value can not be attained without enhancement. The 2^{nd} harmonic is -101dB and the 3^{rd} one is -94dB. This high linearity can be achieved by SeDWA technique. Fig. 2.25 and 2.26 show the output spectrum under the conditions of -10dB and -70dB input.

Fig. 4.27 shows the output spectrum of modulator under the conditions of -6dB input signal and 50-MHz sampling frequency. Compared with 40-MHz sampling frequency, the in-band noise power increases and the peak SNDR becomes 66dB. Relevant reasons are stated in later paragraphs. However, it is also found that only the 5^{th} harmonic is -97dB and others are suppressed under -100dB. This proves high linearity. Fig 2.28 shows SNDR when the input amplitude is changed under the condition of 40-MHz sampling frequency. The peak SNDRs are 72dB, 75dB, and 78dB for the signal-band of 1.256MHz, 1.0MHz, and 0.628MHz, respectively.

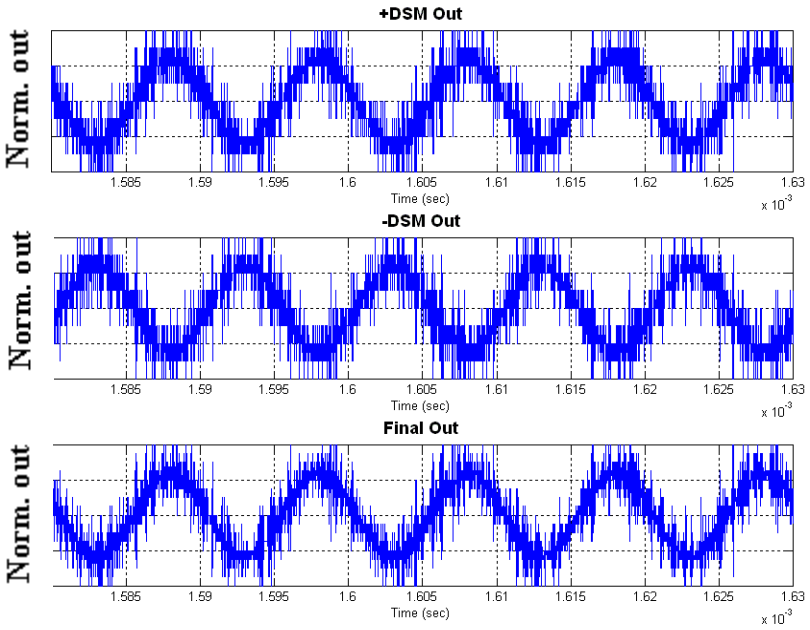
The following discussions explain why there exist differences between experimental and simulation results of modulator:

- One factor that limits SNDR of the whole modulator is the bandwidth of each

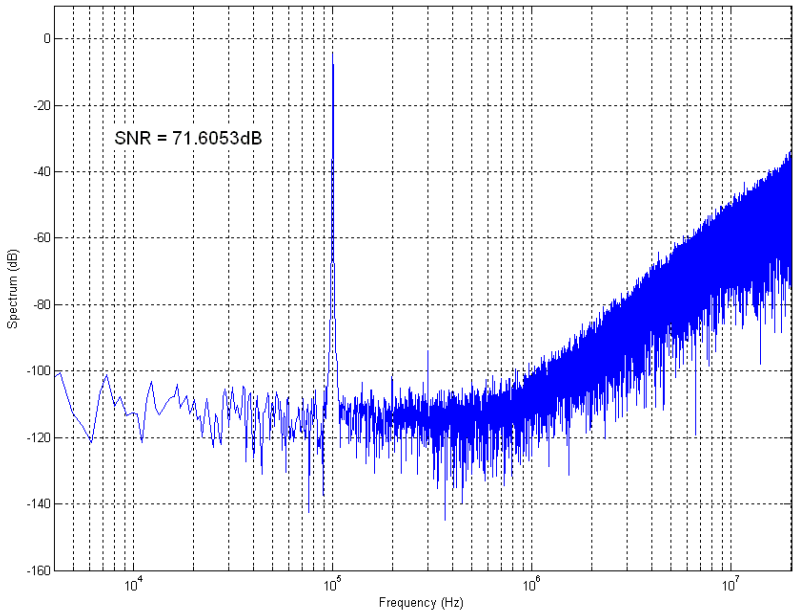
op-amp in the integrators. The example is shown in Section 3.4. Based on the experiment results shown in Section 4.1, the bandwidths are found reduced in fabricated devices, which may cause performance degradation.

▪ Despite low power, some harmonics are found existing on the output spectrum. According to this experiment, the input signal offset can change the power of harmonics. Such change is related to input paths. The input parasitic resistances of input paths somehow increase the resistance on the sampling phase. Relevant issues are described in Section 3.4.

▪ It is found that in-band noise increases with the increase of clock frequency. Since in-band noise is related to digital clocks, digital noise couplings or/and reference voltage fluctuations to some extent affects the performance degradation.



(a) Outputs



(b) Output spectrum

Fig. 4.24 Experimental results (F_{in}=100kHz, F_s=40MHz)

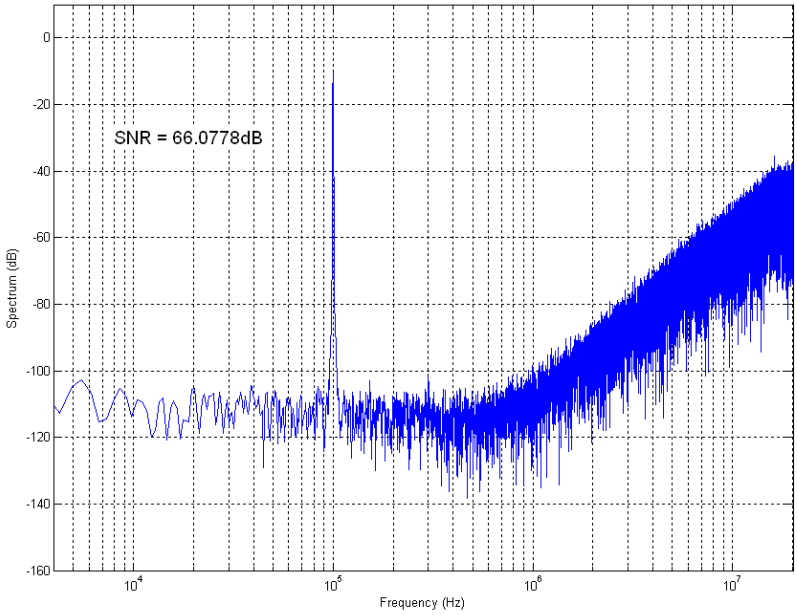


Fig. 4.25 Experimental result (F_{in}=100kHz, F_s=40MHz)

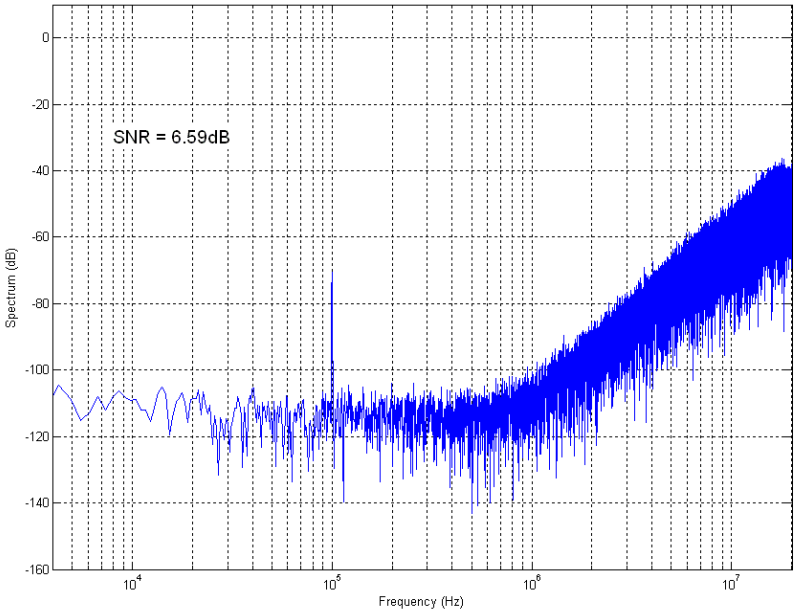


Fig. 4.26 Experimental result (F_{in}=100kHz, F_s=40MHz)

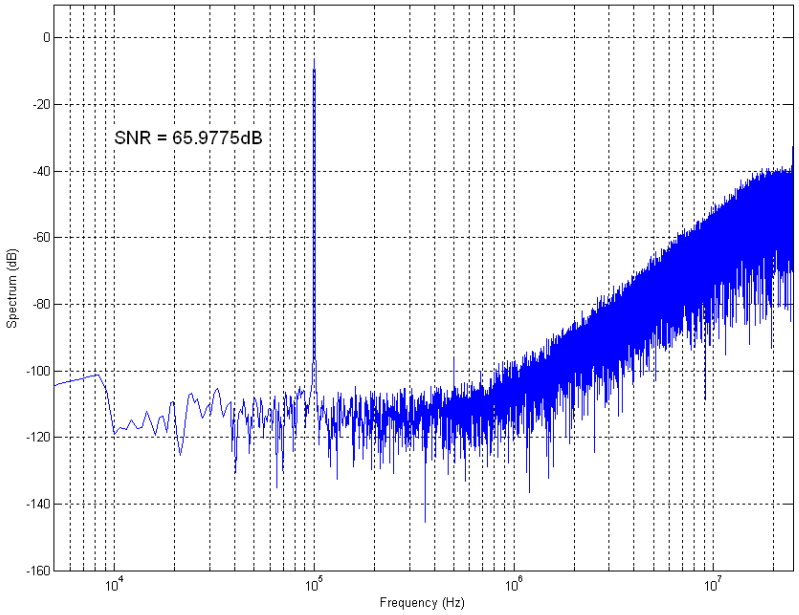


Fig. 4.27 Experimental result (F_{in}=100kHz, F_s=50MHz)

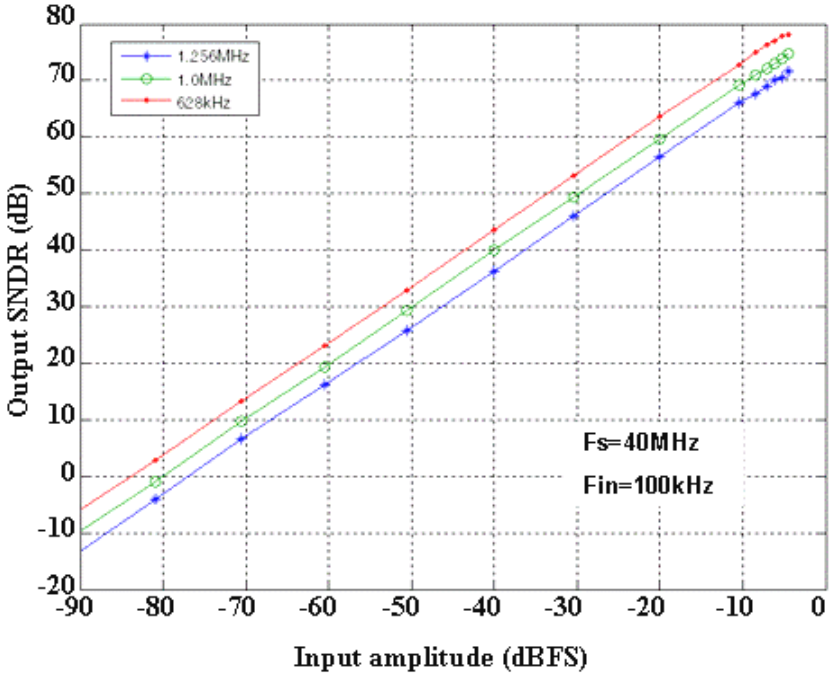


Fig. 4.28 SNDR vs. input amplitude (F_{in}=100kHz, F_s=40MHz)

Table 4.1 shows the performance summary of the prototype chip. It was fabricated in a 0.18μm CMOS process technology and it dissipates 42mW from analog circuits and 16mW from digital circuits at 1.8-V power supply under the condition of 40MHz sampling frequency.

Table 4.1 Performance summary

Sampling Frequency	40MHz
Peak SNDR	72dB@100kHz in (1.256MHz fB) 75dB@100kHz in (1.0MHz fB) 78dB@100kHz in (628kHz fB)
Peak SFDR	90dB@100kHz in
Input Range	1.44Vpp (differential)
Power Consumption	42.4mW (analog) 16.0mW (digital)
Process Technology	0.18μm CMOS

CHAPTER 5. CORRELATED DOUBLE SAMPLING TECHNIQUE FOR CONTINUOUS-TIME FILTERS

There are two main streams of analog filters in terms of analog signal processing: discrete-time filters, usually switched capacitor filters, and continuous-time filter such as an R-C active filter. Switched capacitor filters became very popular due to this accurate frequency-response and no post design tuning required in an integrated circuit technology. Moreover, the switched capacitor technique is not based on absolute voltage processing, but on charge transfer function which makes easy voltage level adjustments in a low voltage supply. It is, however, limited in the ability to process high-frequency signals due to using high sampling rate in order to relax the preceding anti-aliasing filter. Accordingly, switched capacitor filters have been mainly used in low-frequency and high accurate filtering. Continuous-time filters, on the contrary, have supremacy in high-frequency signal processing [3], [32].

No matter which type of filter is used, discrete-time or continuous-time, it basically utilizes the virtual ground property of a high-gain operational amplifier (op-amp). However, the op-amp has several imperfections degrading a constructed circuit's performance and the imperfections are becoming more and more critical in today's sub-micrometer process era. For example, lower voltage-gain due to lower supply voltage, larger offset voltage caused by larger device mismatches, higher flicker noise, and so on. Correlated Double Sampling (CDS) is one of the feasible circuit techniques to reduce the effects of some of these imperfections [33]. In the past, this technique was exploited in discrete switched-capacitor circuits successfully

(i.e. [34], [35]) and our next question is how about applying CDS technique to a continuous circuit. This chapter answers this question. Basic knowledge of the CDS technique is introduced in the next section 5.1. Integrator circuit is a key component in a continuous-time filter and a proposed CDS integrator is explained in section 5.2. Tow-Thomas biquad filters employing the CDS integrator are described in the following section 5.3.

5.1. Correlated double sampling technique

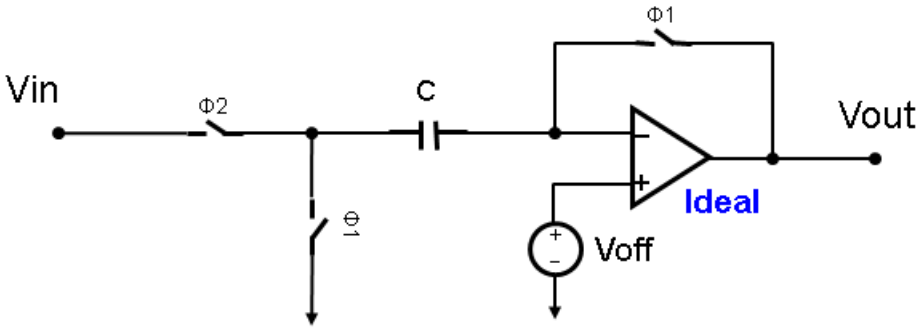
The basic idea behind the CDS technique is to sample the disturbing signal, such as noise, offset, and so on, and then to cancel the noise by subtracting it from the signal plus noise [33]. The contaminated signal is usually captured at the input or output node of op-amp.

An offset-cancellation comparator is a simple example of CDS shown in Fig. 5.1 (a). In the figure, V_{off} denotes the input-referred offset voltage of the op-amp and otherwise an ideal op-amp is assumed. During clock phase Φ1, the offset voltage V_{off} is stored in capacitor C at the op-amp input, and then this unwanted voltage is subtracted from the input signal V_{in} in the following clock phase Φ2. In the z-domain, the transfer relation between the output signal and the offset signal is expressed as

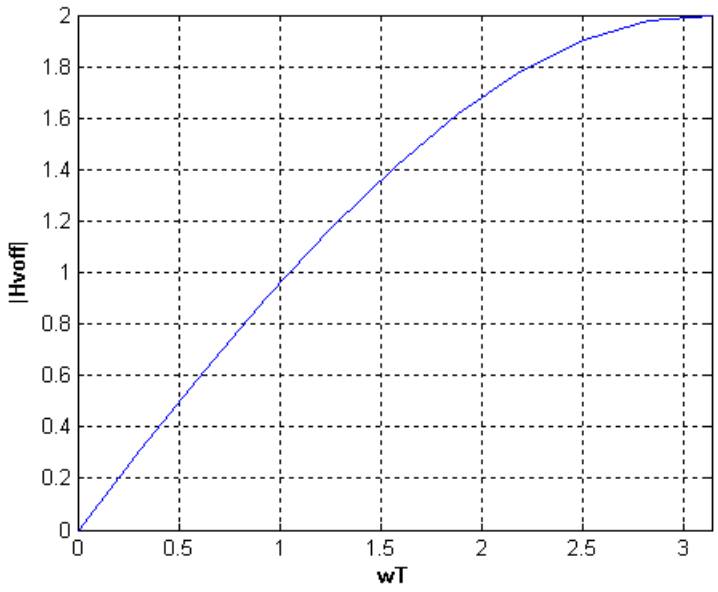
$$V_{out}(z) = (1 - z^{-1}) \bullet V_{off}(z). \tag{5.1}$$

Therefore, the magnitude of the transfer function is simply

$$\left|H_{off}(\omega)\right| = 2\left|\sin(\frac{\omega T}{2})\right|. \tag{5.2}$$



(a) Circuit diagram



(b) Magnitude of offset voltage transfer function

Fig. 5.1 Offset-cancelling comparator

The above equation shows that the offset voltage is suppressed at the DC frequency by this operation, seen from Fig. 5.1 (b). Moreover, much of the input-referred flicker noise is also suppressed. This example is sometimes called auto-zeroing, which is one CDS technique.

Fig. 5.2 shows a gain-and offset-compensated discrete-time integrator with a switched capacitor (SC) circuitry. During clock phase Φ1, the input-referred unwanted voltage is stored in capacitor C1 and at the same time feedback capacitor C2 is completely disconnected at one node to keep the output information. In the next clock phase Φ2, the compensation capacitor C3 is connected to input V_{in} to make the equivalent charge transfer. This indicates the integration operation of this circuit. From a simple analysis [36], it is proved that the output offset is reduced to

$$V_{os} = \mu(\frac{C_1}{C_2})V_{os} \quad . \tag{5.3}$$

In the above equation, μ = 1/A (A is the DC gain of the op-amp) and Vos is the offset voltage of the op-amp. The pole error is also reduced as given below

$$\Delta p = (\frac{C_1}{C_2})\mu^2 \quad . \tag{5.4}$$

Other popular integrators were developed by Nagaraj [33], [37], which are shown in Figures 5.3 and 5.4, respectively. Both integrators exhibit superior suppression of the offset voltage and flicker noise. Theoretically, the predictive Nagaraj integrator has smaller gain error by introducing the predictive path. However, the integrator gain is mainly determined by the matching accuracy of the capacitors. Extensive analysis has been conducted and described in [38].

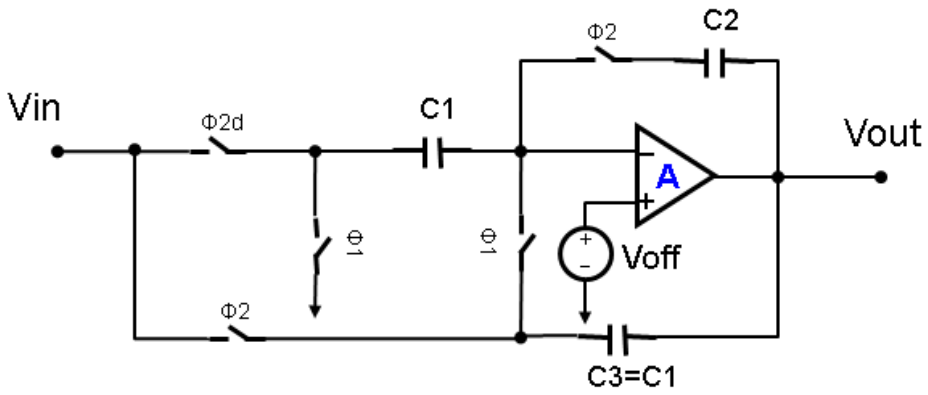


Fig. 5.2 An offset- and gain-compensated SC integrator

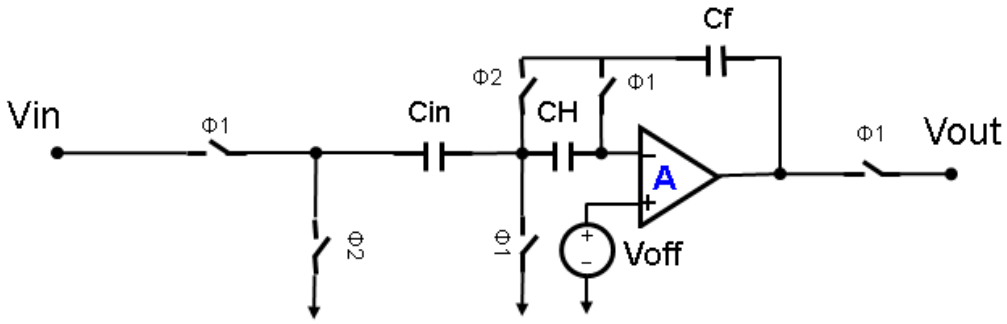


Fig. 5.3 Nagaraj offset- and gain-compensated SC integrator

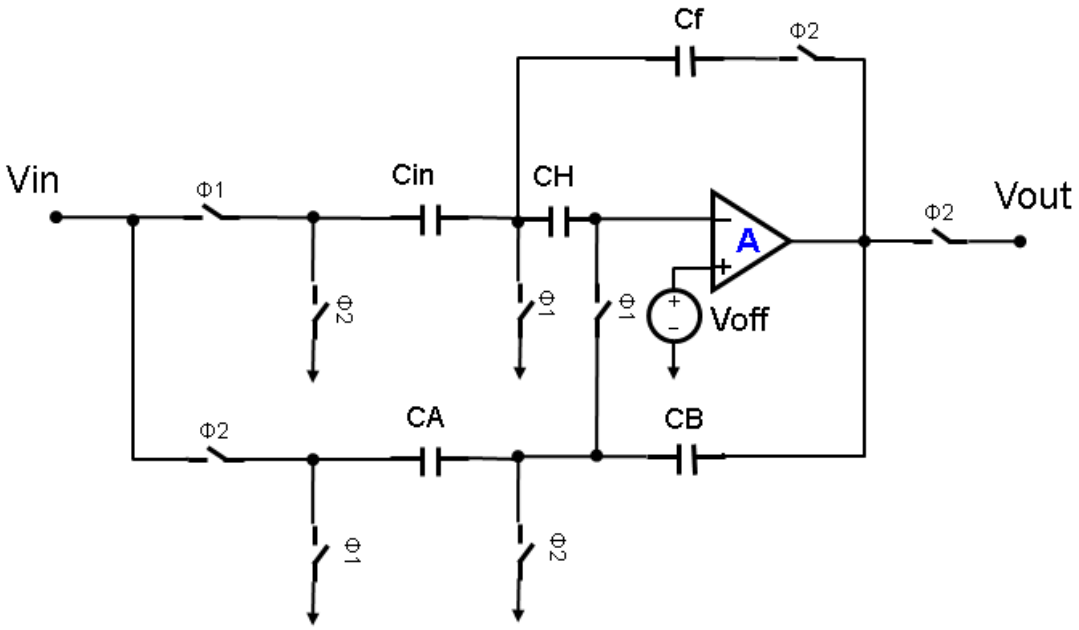


Fig. 5.4 Nagaraj predictive SC integrator

5.2. Continuous-time integrator with CDS circuit

A CDS circuit applicable to a continuous-time integrator (Miller integrator) is proposed and both the detailed analysis and the performance improvement are described in this section.

The output of an ideal integrator, constructed by op-amp with the infinite voltage-gain and zero input-offset voltage, is an accumulation of input signal, as in equation (5.5) by assuming the initial output $V_{out,0} = V_{out}(0)$.

$$V_{out}(t) = -\frac{1}{RC}\int_0^t V_{in}(\tau)d\tau + V_{out,0} \qquad (5.5)$$

However, a realistic op-amp has a finite voltage-gain (A) and a non-zero input-offset voltage (V_{os}). For a non-ideal integrator, which is constructed from a realistic op-amp, the output and output error are

$$V_{out}(t) = -\frac{1}{(1+\mu)RC}\int_0^t V_{in}(\tau)d\tau + V_{out,0} + V_{err,non-ideal}(t) \qquad (5.6)$$

$$V_{err,non-ideal}(t) = -\frac{\mu}{(1+\mu)RC}\int_0^t V_{out}(\tau)d\tau + \frac{1}{(1+\mu)RC}\int_0^t V_{OS}\,d\tau \ , \quad (5.7)$$

where μ=1/A. The R-C constant of the output slightly changes due to finite op-amp gain. The output error is accumulated from initial time and the op-amp's input offset cannot be cancelled. The CDS technique reduces this output error. Fig. 5.5 shows the circuit diagram of compensated integrator, which applies CDS compensation circuit to non-ideal integrator. The compensation circuit samples the op-amp's input-referred error voltage at the end of clock phase Φ_1 and then provides an improved virtual ground to the R-C branch during the following clock phrase Φ_2. During clock phase Φ_2 (at time n-1+Δ to n), the output $V_{out}(t)$ and the output error $V_{err,comp}(t)$ are expressed as

$$V_{out}(t) = -\frac{1}{(1+\mu)RC}\int_{n-1+\Delta}^t V_{in}(\tau)d\tau + V_{out,n-1+\Delta} + V_{err,comp}(t) \qquad (5.8)$$

$$V_{err,comp}(t) = -\frac{\mu}{(1+\mu)RC}\int_{n-1+\Delta}^t (V_{out}(\tau) - V_{out,n-1+\Delta})d\tau \ , \qquad (5.9)$$

where and $V_{out,n-1+\Delta} = V_{out}(n-1+\Delta)$. Thanks to the CDS technique, the output error is compensated locally when output changes slowly and the op-amp's input offset does not affect the output error in clock phase Φ_2. The reduction effect of op-amp's offset

by using CDS technique was confirmed by simulation. In order to stabilize the integrator circuit, a feedback resistor R was inserted parallel to the integration capacitor C, and simulation shows that the gain of error voltage is reduced from 1.961V/V (without compensation circuit) to 0.213V/V (with compensation circuit). Another advantage of the CDS technique is its lowering gain-error. Gain-frequency responses are compared between ideal integrator, non-ideal integrator without CDS and non-ideal integrator with CDS in Fig.5.6. The gain error for the non-ideal integrator can be made smaller by allowing longer period of clock phase Φ2, which provides improved virtual ground with R-C branch for a longer time. Table 1 lists the gain error for several clock duty cycles.

In this research, another circuit configuration is also proposed, which is indicated in Fig.5.7. The CDS function of this circuit is the same as that of Fig.5.5 circuit, but it is cheaper by sharing a feedback capacitor with an integration capacitor. However, a simple switched capacitor level-shift technique, which is described in the next section, is not used for this CDS integrator; therefore, further research has been done based on the Fig.5.5 circuit.

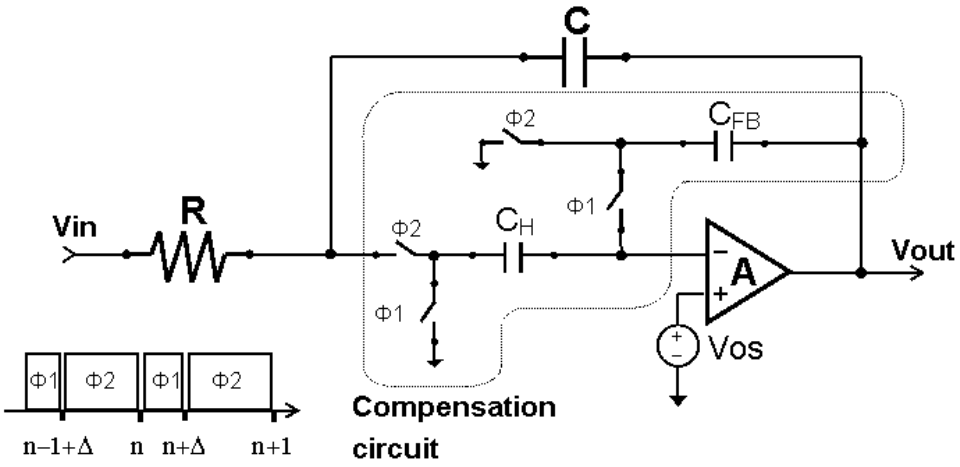


Fig. 5.5 A Miller integrator with CDS circuit

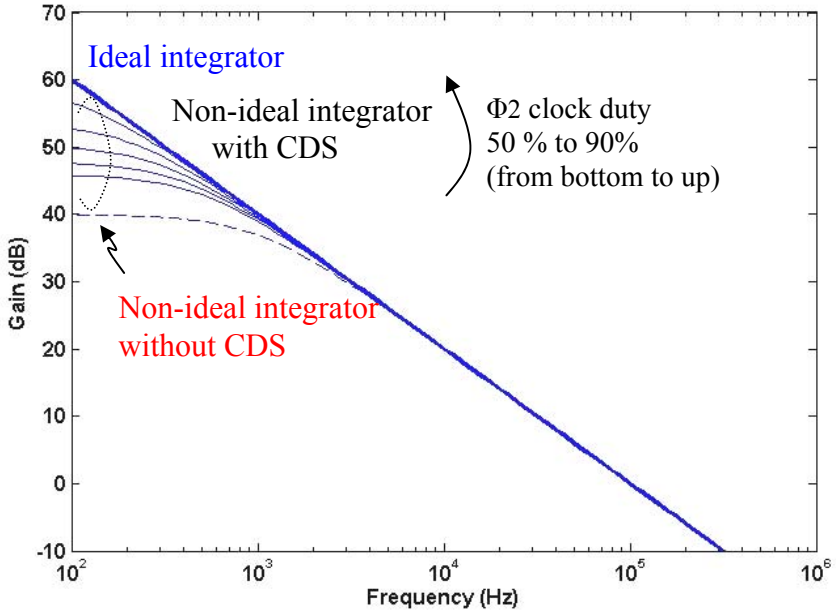


Fig.5.6 Integrator's gain-frequency response
(A=∞-V/V and V_{os}=0-V for ideal integrator,
while A=100-V/V, V_{os}=5-mV for non-ideal integrator)

Table 5.1 Gain error of compensated integrator (F_{in}=100-Hz)

Φ2 clock duty cycle	Gain Error
90%	3.3dB
80%	6.9dB
70%	9.8dB
60%	11.9dB
50%	13.6dB
Non-Ideal Integrator	20dB

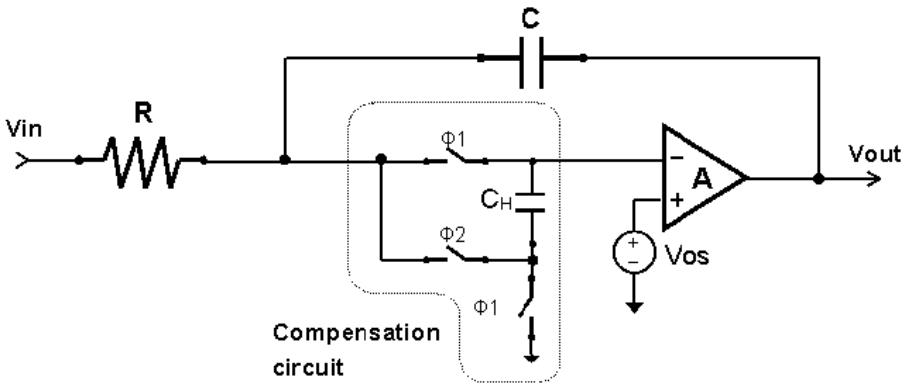


Fig. 5.7 A Miller integrator with another CDS circuit

5.3. Tow-Thomas biquad filter

The CDS Miller integrator, presented in the previous section, can be applied to a Tow-Thomas biquad filter with a high Q-factor. In this section, the circuitry considerations and filter performance are described.

A single-ended circuit configuration is shown in Fig. 5.8. The first integrator is the most critical in terms of input referred error voltage, and therefore the CDS circuit is applied to the first stage. In order for both op-amps to operate with a low supply voltage, the input common-mode voltage of op-amps is set at close to ground while the output common-mode voltage to half of the supply voltage [39]. A switched-capacitor level-shift for the first op-amp and a current source [39] for the second one adjust their input common-mode voltages. Another simple level-shift technique uses a resistor [39] to make the dominant pole of the 2nd integrator to shift in a low voltage-gain op-amp used and accordingly causes the filter cut-off frequency to shift. Therefore, a current source is used instead. The differential Tow-Thomas circuit in Fig. 5.9 is our circuit structure. Fig. 5.10 shows the filters gain-frequency response, in which ideal filter has a low-pass transfer function with a corner frequency of 100-kHz and a Q-factor of 10. By using the CDS technique, the peak gain, which is ideally 20-dB, is compensated from 17.5-dB to 19.4-dB and the pass-band low-frequency gain is also improved from - 2.9-mdB to - 0.27-mdB (ideally, 0-dB). Fig. 5.11 shows the error transfer function (ETF) of the 1st op-amp's input error signal (Vos1 in Fig. 5.8). Narrow-band low-frequency error signal, such as an input offset and a flicker noise, can be attenuated to about one fifth thanks to CDS, while it is amplified by 2 without

CDS. Moreover, the effect of higher frequency noise, such as a thermal noise, is also reduced. Accordingly, as seen in Fig. 5.12, the output offset is highly attenuated by CDS with a 10.38-KHz sine wave input. Fig. 5.13 indicates that no significant harmonics appears for – 20-dB (0.2-Vpp) input while about – 100-dB harmonics and inter-modulation products come out for – 6-dB (1-Vpp) input. The power Spectral Density of the filter output noise, which originates from only switched thermal noise, was simulated using a behavioral noise model of an equivalent 1-kΩ on-resistance. The switching noise has similar characteristics as the overall filter response and the calculated total noise power is 43.5-nV^2 (Fig. 5.14). Simulations indicated that this noise can be reduced by increasing the CDS frequency or increasing the CDS capacitors' value (C_H, C_{FB} in Fig. 5.8) or reducing the on-resistances of the switches. More detail and accurate analysis requires a transistor-level simulation.

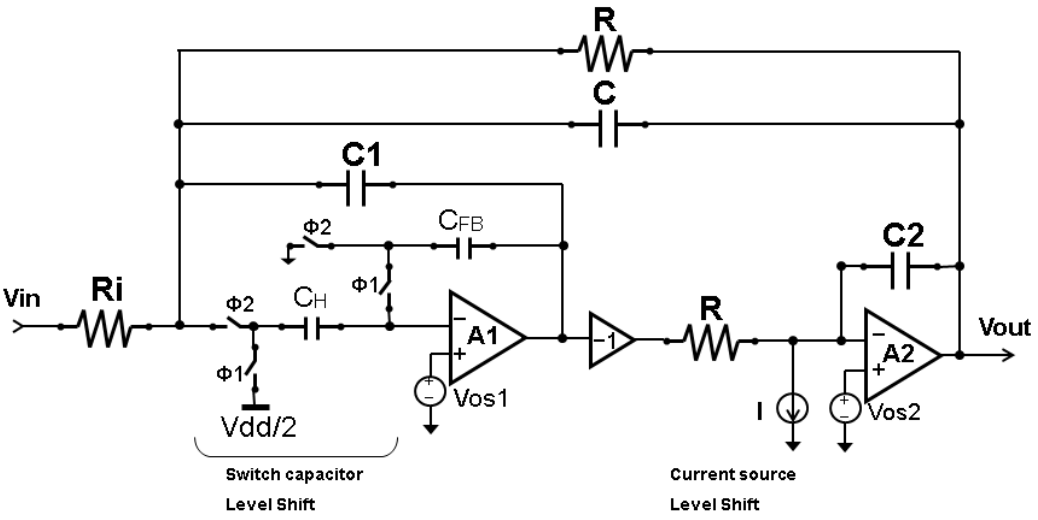


Fig. 5.8 Tow-Thomas biquad filter with a high Q

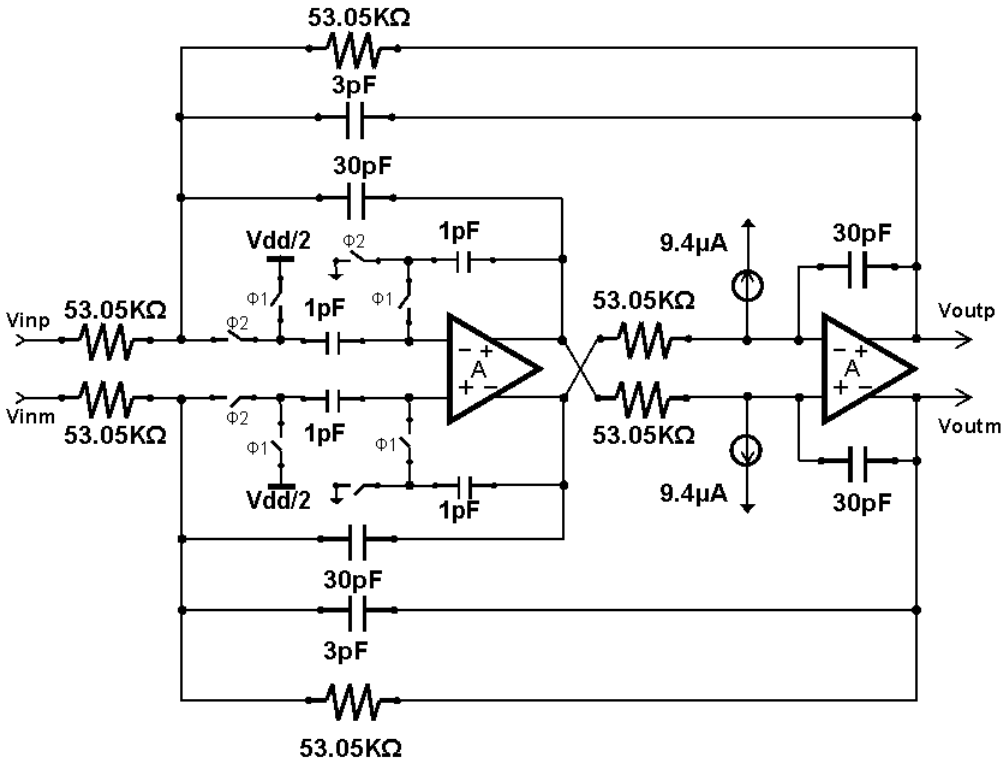


Fig. 5.9 Fully-differential biquad filter

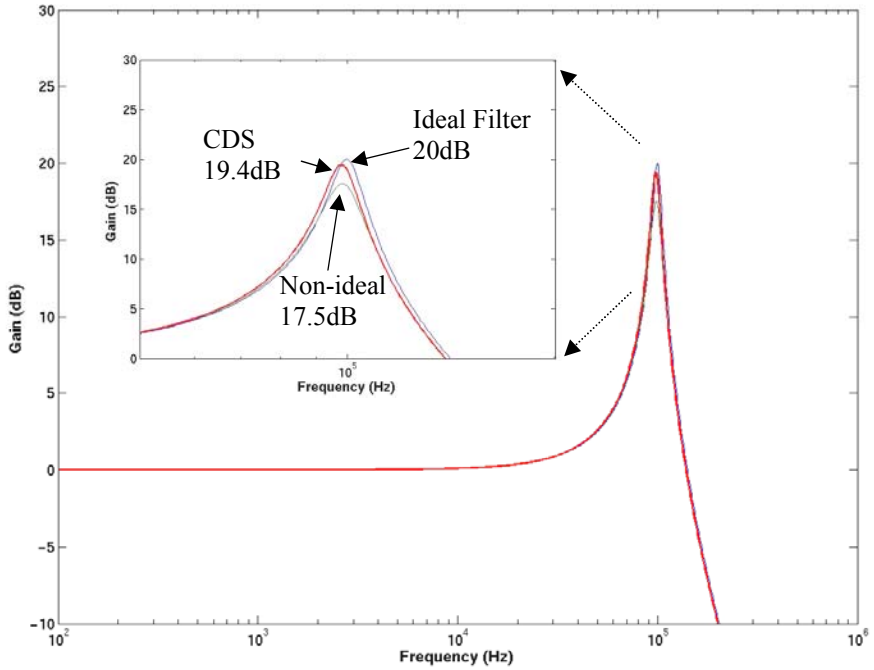


Fig. 5.10 Filter gain-frequency response ($A_1=A_2=\infty$ and $V_{os1}=V_{os2}=0$ for ideal filter, while $A_1=A_2=100$ and $V_{os1}=20mV$ and $V_{os2}=3mV$ for non-ideal filter and CDS filter)

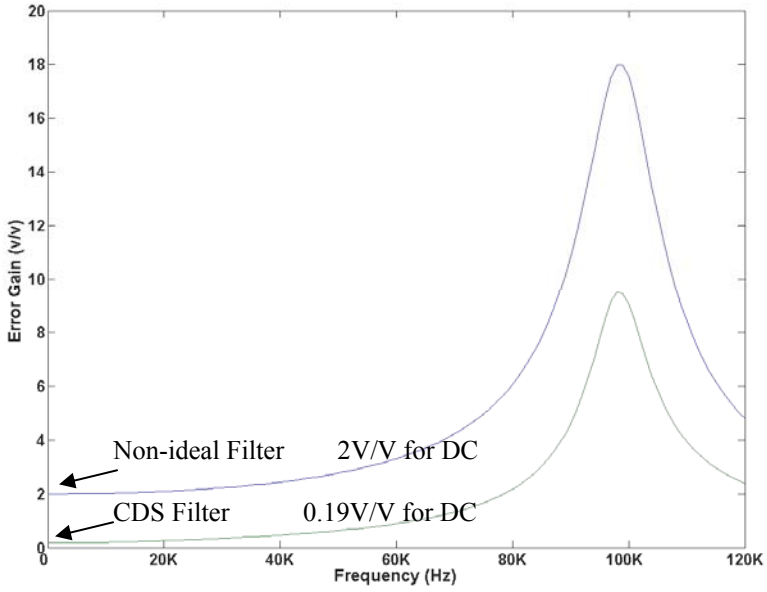


Fig. 5.11 ETF of the 1st op-amp input error

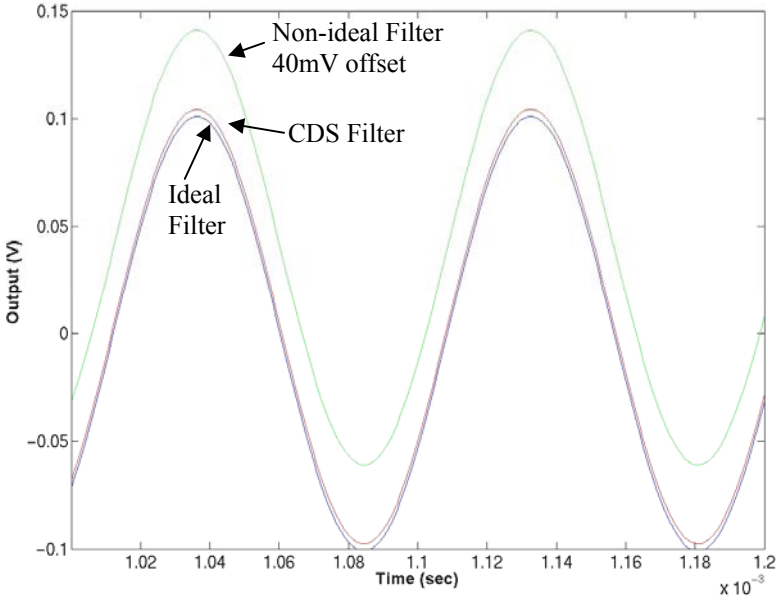
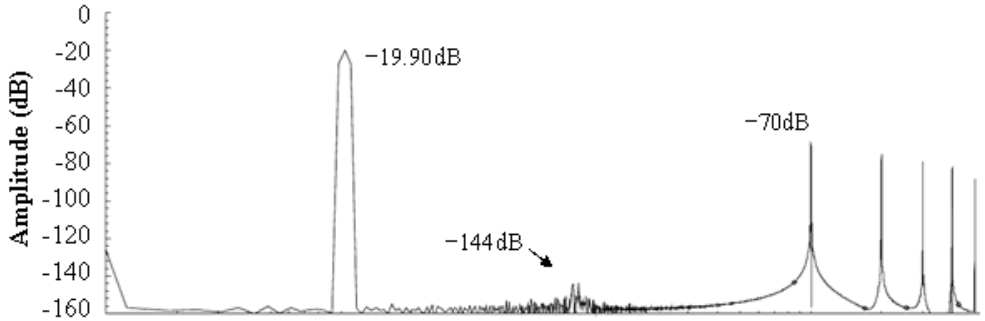
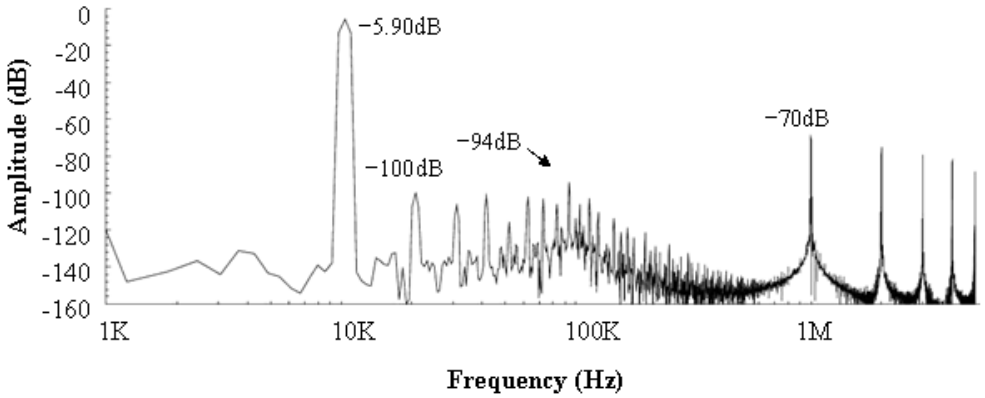


Fig. 5.12 Filter outputs



(a) Input level -20dB (0.2Vpp)



(b) Input level -6dB (1Vpp)

Fig. 5.13 Output power spectrums
(A_1=A_2=100, V_{os1}=20mV, V_{os2}=3mV, Op-amp BW 100MHz)

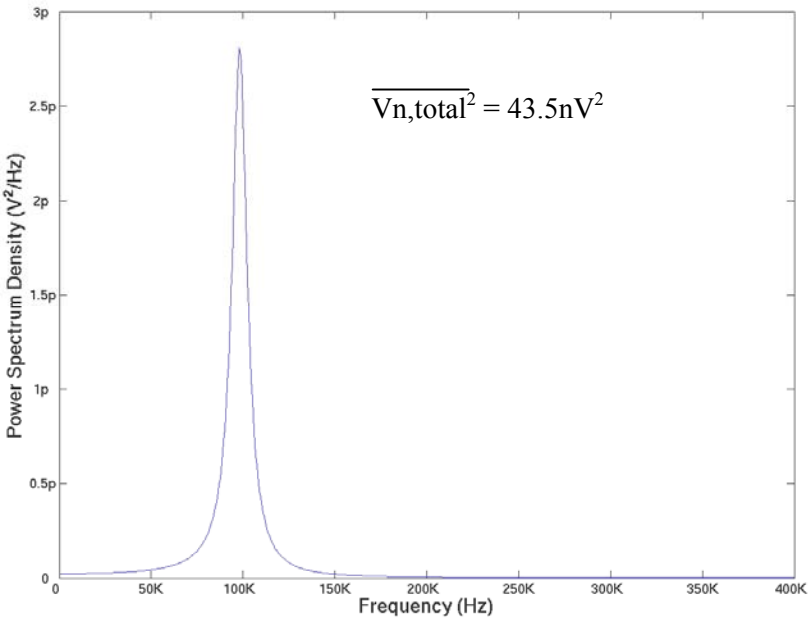


Fig. 5.14 Switch thermal noise (Ron=1kΩ)

CHAPTER 6. CONCLUSION

6.1. Summary

In this study, improved design techniques for analog circuits and mixed analog/digital circuits were analyzed. Contributions of this study are described as follows:

First, an enhanced sprit delta-sigma A/D converter was implemented by a proposed circuit scheme, i.e., a delayed noise cross coupling using switched capacitor technique and a crock generator used for the controlling of coupling. The proposed implementation scheme was verified through experiments on a prototype converter. In addition, experiments conducted in this study also verified another technique, i.e., segmented DWA. Hardware verification is one great value this study demonstrated.

Second, another contribution this study made is reflected on its proposed correlated double sampling (CDS) technique for continuous-time filters. The proposed CDS circuit was applied to a Tow-Thomas biquad filter that possesses a high Q-factor. The filter exhibits superior performance over the non-CDS filters with respect to time-domain output offset and output frequency response.

To sum up, this study is summarized as follows:

First, this study analyzed the fundamentals of delta-sigma A/D converters and the schemes of their accuracy improvement.

Second, it designed the delta-sigma A/D converter by incorporating two techniques, i.e., an enhanced split architecture and a segmented data-weighted-

average. Circuit implementation schemes in CMOS technology for these two techniques were proposed and incorporated in the design. In the mean time, some critical circuit parameters were also analyzed and discussed.

Third, an A/D converter was designed, fabricated and tested to demonstrate its practical performance.

Fourth, it also discussed the fundamentals of correlated double sampling techniques, and their applications to discrete-time integrators.

Last, this study proposed and analyzed in detail a novel correlated double sampling technique for continuous-time analog filters.

6.2. Future work

Throughout this study, I hoped to shed light on research of relevant fields. For future work, several remaining issues are provided:

First, the op-amps used in the delta-sigma A/D converters require high slew-rate which consumes high power consumption in the modulator. Some low power techniques such as dynamic biasing (i.e. [40]) are to be analyzed.

Second, the proposed correlated-double-sampling integrator was analyzed in detail. The implementation of this technique in a low-voltage CMOS may be another topic for future researchers' interest.

Third, to use chopper techniques (i.e. [41]) to reduce the thermal noise of CDS also deserves future researchers' attention.

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