AN ABSTRACT OF THE DISSERTATION OF

Drake A. Miller for the degree of Doctor of Philosophy in

Electrical and Computer Engineering presented on March 7, 2011.

Title: Random Dopants and Low-Frequency Noise Reduction in

Deep-Submicron MOSFET Technology

Abstract approved: ____

Leonard Forbes

The future of mixed-signal, memory, and microprocessor technologies are dependent on ever increasing analog and digital integration, higher cell densities, and demand for more processing power. As a result MOSFET device dimensions continue to shrink to meet these demands. A side effect of device scaling is increased variability at each technological node which affects both analog and digital circuits in terms of decreased yields, performance, and noise margins.

At deep sub-micron dimensions the Low-Frequency Noise (LFN) of the MOSFET is dominated by the influence of one or more active traps capturing and emitting charge to and from the oxide creating wide variations in the LFN from otherwise identical devices. Additionally, the random position of dopant atoms near the Si/SiO_2 interface create a potential landscape that induces regions of high and low conductivity which in turn causes a situation where the current is no longer uniform in

the device, but consist of individual current paths or percolating currents. The coupling between the random variation of the percolation current and active traps in the oxide are responsible for the large spread (> 3 orders of magnitude) in the noise characteristics observed in deep sub-micron MOSFET devices. The compact LFN model presented here accounts for the action of traps on percolating currents in deep-sub-micron and nano-scale MOSFETs.

Two schemes for reduction of LFN are studied based on the smoothing of the surface potential. First, noise reduction is demonstrated with measurements on sub-micron MOSFETs with forward substrate bias. Secondly, the model is further verified through the reduction of noise by the removal of dopant atoms near the Si/SiO_2 interface of the device. Both schemes result in a lower noise and threshold device.

Finally, these experimental findings are applied to a 2.2μm 2 MP CMOS image sensor. From the temporal noise measurements on threshold implant process splits, the image sensor noise has been significantly reduced as a direct result of fundamentals described by this MOSFET LFN model and further proves the validity of these findings.

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Random Dopants and Low-Frequency Noise Reduction in Deep-Submicron MOSFET Technology

by

Drake A. Miller

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented March 7, 2011
Commencement June 2011

Doctor of Philosophy dissertation of Drake A. Miller presented on March 7, 2011.

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Drake A. Miller, Author

ACKNOWLEDGEMENTS

The love and support from my wife, Jenaye, has been the fuel to continue in this most difficult of pursuits. She has so graciously put her own life goals on hold to care for and raise our three children. I am forever in her debt for the sacrifices that she has made on this long journey. I love you and will never forget what you have done for us.

My most sincere appreciation goes to Professor Leonard Forbes. His expertise and guidance have taught me a great deal. Through the years we have worked on a number of projects and I am always amazed at his reduction of complex problems to their most simplest of parts. It is this ability that I continually strive for and will take into my professional career with great gratitude. I hope that I will have the opportunity to work with Len for many years to come.

None of this would have been possible without the continued support from my parents and grandparents. They never questioned this direction I have taken and have always been a source of encouragement through the toughest of times. Finally, a special thank you, to my good friend and colleague, David Zier, who has always been there as source of reason and inspiration.

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For my wife

Jenaye Ryann Miller

Random Dopants and Low-Frequency Noise Reduction in Deep-Submicron MOSFET Technology

1 Introduction

Electronic noise and in particular 1/*f* noise has been a fundamental limit to engineers who attempt to measure and control increasingly smaller currents and voltages. A prime example of a technology where noise places severe limitations and a practical example of this research is in CMOS image sensor (CIS) technology. At a minimum a CIS device consists of an array of photodiodes, analog readout circuits, and pixel clocking circuits. Each block of the CIS chip is made up of many MOSFET devices. These devices form the circuits used to convert the optical signal to an electrical signal and for driving the pixel timing signals.

The photodiode sensor and the following analog and analog-to-digital conversion circuitry each place limits on the smallest optical signal capable of being sensed. The most fundamental of the noise limits is that of the photon shot noise, however, before a CIS can be considered as "photon shot noise limited" the readout circuitry must not add considerable noise to the signal. In the readout circuitry, the flicker noise or 1/*f* noise is a dominant noise source. The CIS readout path is an example where noise from a number of sources in the signal chain combines, and in most cases the noise is dominated by one of the circuit elements in the chain. In practice the readout circuitry commonly places the noise limitation on the device; however, the random telegraph signal present in deep-submicron MOSFETs used in the pixel array places an additional noise limitation especially in small pixel pitches less than 2μm and under low-light conditions.

Semiconductor materials and devices have proliferated consumer electronics and have changed the shape of information sharing and dissemination like no other technology has in human history. Solid-state technology has allowed man to explore space, create the world-wide web, and made cell phones accessible to an ever increasing portion of the world-wide population. Fundamentally all of this was made capable through the advent of one particular device, the solid-state transistor. The most desirable characteristic of a transistor is in the ability of the device to convert a small input voltage to a large current. Passing a current through a large resistor creates amplification where the small input voltage is much easier to sense and manipulate. Probably the most common use, in sheer numbers, of transistors today is for digital applications. In digital systems a transistor is simply thought of as a switch with an on or off state or high and low state. With these two states and millions of transistors logic is performed and data is added, multiplied, divided, read, and stored.

Transistors are used widely in analog systems as well. The physical world around us is innately analog. Temperature, sound, and light are examples of measureable analog quantities. Analog signals are separated from digital signal because analog signals represent continuous time quantities while digital signals are defined at discrete values for discrete time intervals. To sense an analog signal an appropriate transducer must be used to transform the physical quantity to a change in a measureable electrical quantity (i.e. current or voltage). In order to make this

transition, electronic circuits make use of transistors to provide amplification in order to measure the signal of interest.

Noise has continually been a concern in circuit and system design as noise poses a lower limit that a signal can be accurately sensed. Sources of noise come from a variety of places and each source of noise has to be investigated and handled separately as they often come from different mechanisms. In this thesis the focus in on a fundamental noise source due to physical phenomena in the transistor. Other sources of noise may be the result of the operation of the circuit and the position of components. Power supply noise is one such noise source and is generally the result from ground loops which cause spurious signals to appear on the ground or supply planes that are then coupled into the transistors that are performing the sensing operations.

With the demand for decreased power supply voltages for low-power applications and the shrinking of transistor dimensions for higher integration, noise presents a bigger challenge for analog circuit designers. In general the noise of the system becomes more difficult to mitigate as supply voltages decrease, bandwidth requirements increase, and especially when the signal of interest is small. Shrinking supply voltages poses a constraint because more and more of the available voltage is consumed by noise. High bandwidth systems will innately have noise due to the fact that in most cases the root-mean squared (RMS) of the noise is proportional to the square root of the bandwidth. When a signal is large compared to the system

noise then noise poses little problem; however, as the signal of interest becomes comparable to the noise it is increasingly difficult to distinguish between the signal and the noise and the noise in the system becomes a strict design criteria. An important metric of a circuit's small signal performance is the Signal-to-Noise Ratio (SNR). SNR is found by:

$$SNR = 20\log\left(\frac{V_s^{RMS}}{v_n^{RMS}}\right) \tag{1.1}$$

In this case the numerator is the RMS signal voltage and the denominator is the RMS voltage of the noise. This expression calculates the margin, in decibels, between the input signal and the noise of the circuit. The larger the ratio the less the signal will be corrupted by the noise.

Today, technology allows the fabrication of MOS transistors with 32nm dimensions now in high volume manufacture. It will be shown that at these delicate sizes the noise is due to:

1. the effect of the random position of dopant atoms in the active region,
2. the few number of active traps in the oxide and,
3. the small number of carriers in the channel.

These properties are the primary source of the large noise levels observed in modern MOSFET technologies. Doping concentrations have increased as a necessity to maintain the threshold voltage of the transistor to an operational level;

consequentially, due to the small dimensions the total number of dopant atoms near the surface in the channel region is small. These atoms are positioned at random in the channel and create a potential landscape with peaks and valleys of high and low potential with rivers of current flowing through the valleys of the lowest barriers. Also, in and near the interface between the silicon and the gate oxide traps exist which can capture and later emit charge. This capture and emission modulates the current flowing through the channel of the device. This modulation is the low-frequency noise found in deep-submicron MOSFETs.

Low-frequency noise (LFN) is the region of noise below the corner frequency of either shot noise or thermal noise. Below the corner frequency the noise in large device dimensions is often found to increase like $1/f$. This work develops a model which accounts for the physical source behind the LFN in deep submicron MOSFET devices. The central goal of the model is to provide a means to predictably reduce the noise in deep submicron and nanoscale MOSFET technology. Specifically, the noise as being effected by both random dopants and the substrate bias are taken into account. Ultimately, to keep noise levels low the dopant atoms near the surface must be minimized.

1.1 Organization of the Dissertation

The prime motivation behind this work is based upon the reduction of low-frequency noise in MOSFET devices. To accomplish this, a compact model which

approximates the fundamental physical nature of the low-frequency noise in MOSFETS devices is developed. The model is verified with practical applications which demonstrate a large noise reduction, not previously discovered, in both MOSFET devices and in CIS devices. The dissertation is structured as follows.

Chapter 2 provides a brief overview of noise theory in electronics. Focus will be on those noise sources that are most commonly encountered in semiconductor devices. These sources include thermal, shot, generation-recombination, $1/f$, and RTS noise. Circuit implications of LFN noise in systems which employ MOS technology is discussed. These include digital systems, memories consisting of flash cells, sense amplifiers, and analog systems.

Chapter 3 discusses the methods and techniques for measuring the LFN of the MOS devices used to develop the model created in this research. Measurements of sub-micron MOSFETs will demonstrate and elucidate the reasoning behind the necessity for understanding and remediating this noise source.

Chapter 4 develops a semi-empirical compact noise model for describing those noise properties observed in Chapter 3. This noise model is presented in context of the fundamental physical mechanisms, specifically oxide traps and percolation currents, which are capable of creating the necessary fluctuations of the drain current.

Chapter 5 discusses and demonstrates two low-frequency noise reduction methods. A few methods will be briefly discussed namely switched bias. The first

noise reduction scheme that will be demonstrated is the application of substrate bias. The substrate bias is studied in a number of devices and the noise reduction of this technique is proven. Secondly, low-frequency noise reduction through decreased substrate dopant is shown in both large and small MOSFET devices.

Chapter 6 is a case study demonstrating the model resulting from this work as applied to a CMOS image sensor. This real-world application demonstrates the learning's found through the course of this research; the results of which have solved a fundamental noise issue previously not understood. With the understanding of the noise source and the application of a noise reduction technique used in Chapter 5, a scheme was adopted which significantly impacted the performance of the product resulting in a superior performing image sensor.

Chapter 7 summarizes the information provided in the dissertation and comments on those future device architectures capable of having more favorable noise performance in context of the model developed herein.

2 Semiconductor Noise

Noise in electronics has been a concern for design engineers and a research interest since the conception of electrical systems. Noise in electronics is a voltage or current variation about some mean value. Thermal, shot, $1/f$, and generation-recombination (GR) noise appear with a Gaussian distribution while random-telegraph noise (RTS) noise is found to be Non-Gaussian. Physical device noise is generated through processes such as the random motion, trapping, or random arrival of charge carriers. What makes understanding noise so important is that noise sets a lower limit on the capability of any particular device or circuit to reliably detect small signals.

Most often a Gaussian noise source is one that is generalized by a single parameter with no frequency dependence. Another term that can be used to qualify this type of noise is to say that it is “white” noise. White noise is characterized by the standard deviation that is in the strictest sense constant across all frequencies. The amplitude distribution of such a noise source will have a normal probability distribution.

The focus of this research is primarily on the low-frequency noise characteristics of sub-micron metal-oxide-semiconductor field effect transistors (MOSFETs). MOSFET devices serve as the work horse for most all modern

electronic devices in manufacture today. The devices are used in both digital and analog systems and it is the analog domain where noise is of utmost concern.

There are four noise sources that are important in semiconductors [1]. These noise sources are thermal, shot, GR, and $1/f$ noise. RTS will also be introduced as a noise source; it will be shown that it is a constituent of $1/f$ noise. The following sections will briefly discuss these common noise sources encountered in semiconductor devices. Emphasis is placed on the low-frequency noise in MOSFET devices.

2.1 Johnson-Nyquist (Thermal) Noise

Thermal noise was measured and modeled early in the infancy of electronics [2, 3]. Thermal noise is the most familiar of noise sources as it is found in all electronic devices. Thermal noise is measured as a random voltage across a resistor or in a current when passed through a resistor. It is due to the random collision of carriers with the atoms in the material. As the current moves through the resistive material, multiple collisions with the atoms of the material cause the carriers to randomly arrive at the electrodes. Thermal noise exists even in the absence of DC current. Unlike the other noise sources that will be discussed thermal noise is present at all times. The thermal noise power is expressed as:

$$i_n^2 = \frac{4kT}{R}\Delta f \qquad (2.1)$$

for the current noise or for voltage noise as:

$$v_n^2 = 4kTR\Delta f \qquad (2.2)$$

where k is the Boltzman constant, T the temperature in Kelvin, R the resistance of the structure or device, Δf is the bandwidth of the measurement.

From these equations it is seen that the noise is proportional to the resistance in the case of voltage noise and the inverse of the resistance in the case of current noise. Depending on the application the noise can be minimized by appropriate design of the resistances in the circuit.

2.2 Shot Noise

Walter Schottky discovered the existence of shot noise in his experiments with vacuum tubes. He discovered that electrons arrived at the cathode at different times resulting in very fast burst of current. Shot noise has been observed since the vacuum tube and is the result of discrete charge packets arriving at a point at different times.

As an example shot noise is seen in photodiodes in two forms. One, the noise due to the random arrival of photons is characterized as a shot noise process.

Two, the dark current in the device contributes shot noise since these dark current carriers are traversing the reverse bias junction and contributing to the noise fluctuation.

In bipolar junction transistors (BJT) shot noise is the dominate noise source. As in the case with the vacuum tube, a BJT has a base region where minority carriers are injected from the emitter and extracted by the collector. These minority carriers will arrive at the collector at random intervals giving rise to discrete pulses of current. At typical biases these carriers arrive in vast numbers so the time domain picture looks like the typical fuzz seen on the oscilloscope.

The equation that describes the shot noise in an electronic device is:

$$i_n^2 = 2qI \tag{2.3}$$

where q is the electron charge, 1.602e-19 and I is the DC current flowing through the device.

2.3 Generation-Recombination Noise

Deep levels in semiconductors are capable of causing a fluctuation in the generation, recombination, and trapping rates of charge which results in a fluctuation of the charge density [4]. This fluctuation is detected as a change in conductivity and sensed either as a current or voltage. This type of fluctuation is

called Generation-Recombination (GR) noise. This type of noise is found in the channel of JFET's, photoconductors, and semiconductor resistors [5]. For the energy level to act as a GR noise source the characteristic energy must lie relatively deep in the band gap of the semiconductor.

These deep levels can capture electrons for a time which is characteristic of the energy of the trap. During the time that the carrier remains in the trap is does not participate in conduction. A couple of events can happen while this carrier is held at the trapping site. One is that the carrier is released and in this case a current increase would result when these traps emit electrons. A second event is that the trapped carrier recombines and in effect is forever removed from conduction. At the electrodes the carriers arrive and are collected and when carriers are released there is a surge of carriers and when they are captured there is a reduction in carriers arriving at the electrodes. This generation-recombination process is described by the power spectral density:

$$S_I(f) = \frac{I_0^2}{N_0^2} S_N(f) = 4 \frac{I_0^2}{N_0^2} \overline{\Delta N^2} \frac{\tau}{1 + \omega^2 \tau^2} \tag{2.4}$$

Below is the ideal power spectrum for a single time constant GR noise source.

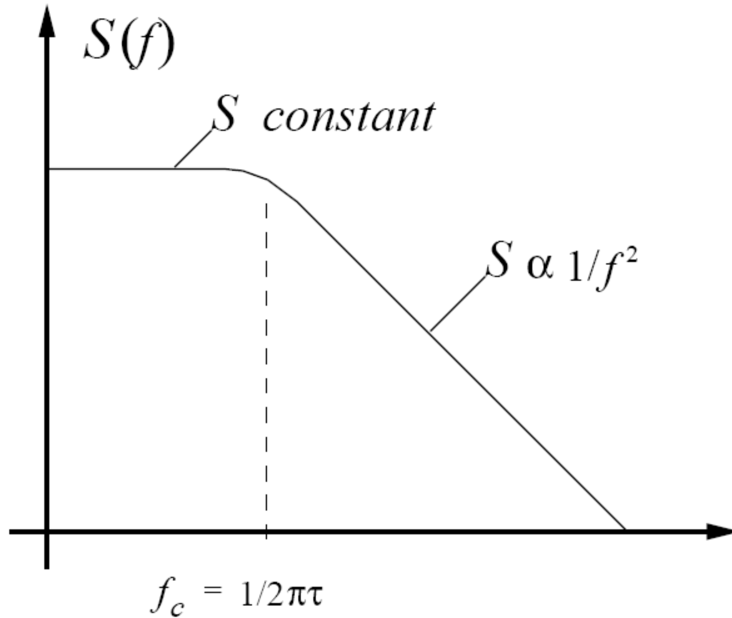


Figure 2.1 Ideal GR Noise spectrum from a single time constant

$$\tau = \frac{1}{\tau_e} + \frac{1}{\tau_c} \quad (2.5)$$

τ is the time constant of the system. The time a carrier is held in the trap is called the time-to-emission, τ_e. The time that the carrier remains free is the time-to-capture, τ_c. Figure 2.2 shows actual device measurements from a photoconductive sensor. The characteristics of GR noise are evident from the shape of the curve specifically the typical plateau region and the corner frequency is readily observable in the noise power spectrum.

From Figure 2.1 and 2.2, at low frequencies below the cut-off frequency, f_c, there is a plateau where the noise level is invariant with frequency. At frequencies above f_c

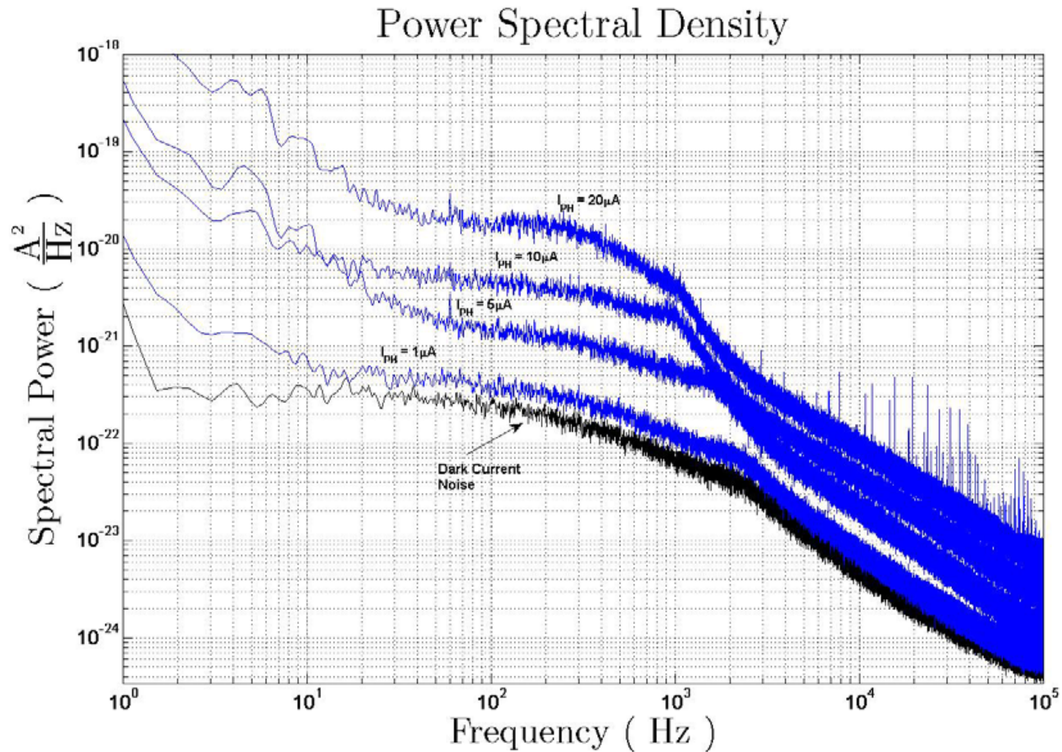


Figure 2.2 GR Noise Spectrum of Photoconductive Device

the noise power rolls off with a $1/f^2$ slope. f_c is dependent on the system time constant, equation 2.2, and the corner frequency is defined as:

$$f_c = \frac{1}{2\pi\tau} \tag{2.6}$$

The behavior and spectral shape of GR noise is very similar to that of an individual RTS as will be shown.

2.4 1/*f* Noise

1/*f* noise is found to exist in a number of physical processes and electronic systems. In general the power spectrum of 1/*f* noise is, as the name implies, proportional to the inverse of frequency [6, 7]:

$$S(f) = \frac{constant}{f} \tag{2.7}$$

Especially in semiconductors there remains controversy as to the fundamental origins of 1/*f* noise. There are two schools of thought which contributed the noise to separate mechanisms. McWhorter theorized in the middle of the 20th century that 1/*f* noise in surface dominated devices, where the current flows near the interface of an oxide-semiconductor interface, is the result of many individual trapping events that modulate the current [9]. Hooge on the other hand claims that pure or fundamental 1/*f* noise is a bulk phenomenon generated from lattice or impurity scattering causing mobility fluctuations of the charge carriers [7].

The general consensus is that 1/*f* is the result of conductivity fluctuations. 1/*f* noise in semiconductors is taken as being an instantaneous change in the conductivity of the material either through number or mobility fluctuations [1, 6].

The definition of the conductivity of a material is:

$$\sigma = q\mu n \tag{2.8}$$

where q is the elementary charge, μ is the carrier mobility, and n is the number of free carriers. In this equation are both elements that can contribute to the measured conductivity fluctuation, number and mobility. The two schools of thought as to the absolute source of 1/*f* noise derive the existence of the noise from one of these two physical parameters. Whatever school of thought is adopted the generally accepted empirical formula for 1/*f* noise is [9]:

$$\frac{S_G}{G^2} = \frac{\alpha}{Nf} \tag{2.9}$$

Here α is a fitting parameter called the Hooge parameter, N the number of charge carriers in the sample, and f the frequency. This equation serves as a basis for comparing devices of different shapes and types. All models of 1/*f* noise generally start from this most basic empirical equation. For instance, it will be shown that from equation 2.9 the SPICE MOSFET 1/*f* noise model is directly derived through substitution of the device equations.

2.5 Random Telegraph Signal (RTS) Noise

The source of much academic interest over the past couple decades is the random telegraph signal (RTS) seen in microstructures. RTS noise has a very similar power

spectrum in most respects to GR noise. RTS has also been named burst or popcorn noise and fundamentally does not differ as to the origin of the noise except that RTS is considered a fundamental phenomenon while burst noise was most often associated with poor device quality. It is pretty well accepted now that the behavior of RTS is due to the capture and emission of traps near a current carrying region where the field setup by the trapped charge causes a change in the local conductivity and/or mobility. RTS has been categorized with $1/f$ noise due to the theoretical treatments by McWhorter and later many others that proved rather conclusively with measurement data, that a $1/f$ spectrum can be generated from the random capture and emission of several fluctuating traps [12-14]. Measurements performed in this research show that a $1/f$ spectrum is closely approximated when several RTS fluctuations are averaged together simulating what would be seen in a larger device, Figure 2.3.

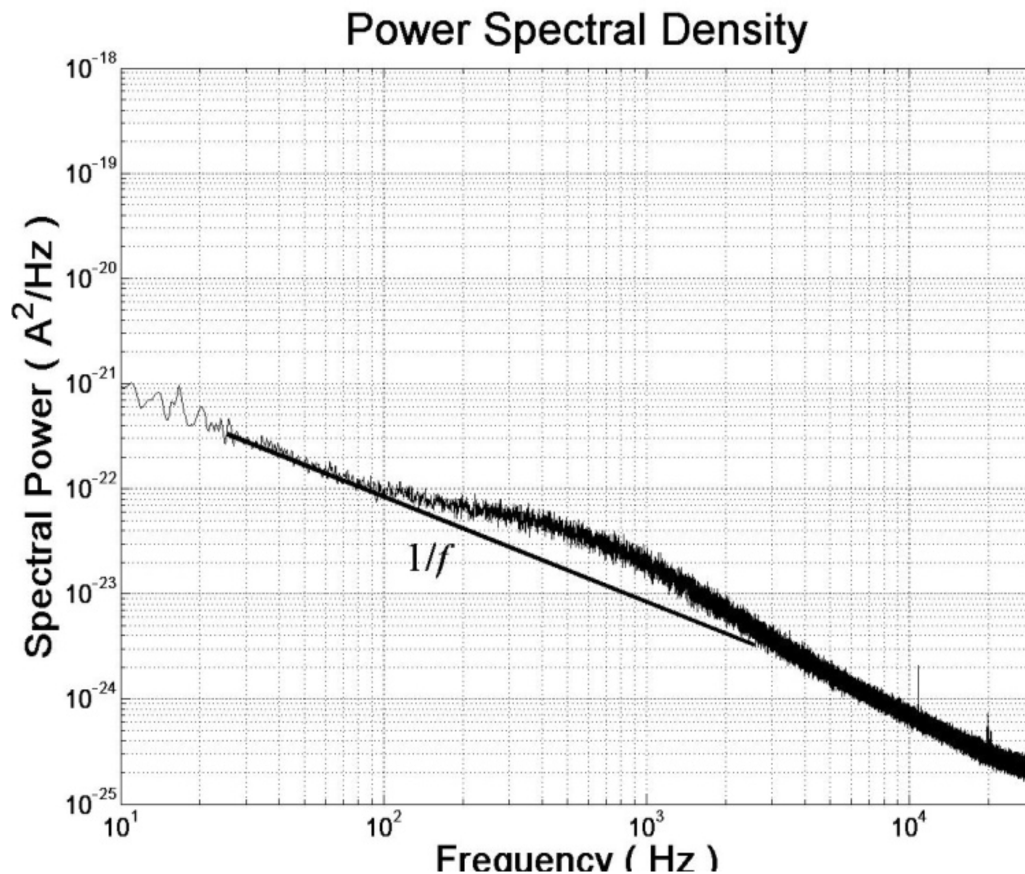


Figure 2.3 1/*f* noise from summation of several RTS waveforms from 10 submicron devices

From measurement, RTS is observed as a two level fluctuation that transitions back and forth from one discrete state to another during some characteristic amount of time. The characteristic times here will be taken as the average time spent in a high or low state, τ_h and τ_l respectively. Figure 2.4, on the next page, shows the high and low state of this theoretical signal.

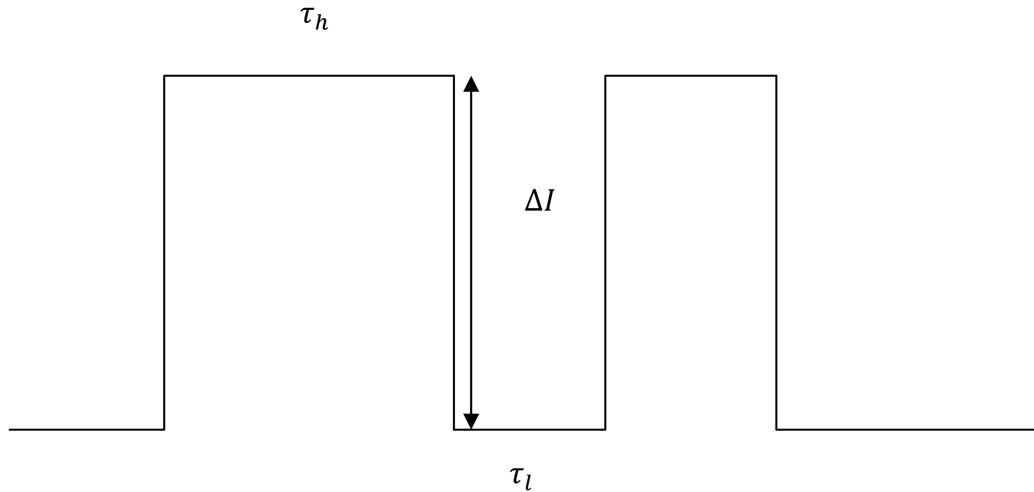


Figure 2.4 Idealized random telegraph signal

Machlup modeled the theoretical nature of a two-state fluctuation and derived that the power spectral density of this fluctuation has the form [16, 17]:

$$S(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_0 + \bar{\tau}_1)\left[\left({}^{1}/_{\bar{\tau}_0} + {}^{1}/_{\bar{\tau}_1}\right)^2 + (2\pi f)^2\right]} \qquad 2.11$$

This is a classical Lorentzian spectrum as also seen in GR noise, see Figure 2.1.

2.6 Low-Frequency Noise in MOSFETs

Low-frequency noise in metal-oxide semiconductor devices is categorized into two groups: 1/*f* and random telegraph noise (RTN). In the first case a measurement of the noise results in a noise power spectrum which has a 1/*f* slope that continues to

low frequencies. RTN on the other hand has a very different character as compared to $1/f$. RTN appears with a Lorentzian shape similar to GR noise, see Figure 2.1, spectrum with a plateau and a roll off of $1/f^{\alpha}$ with $\alpha = 2$. The fundamental noise mechanism behind the low-frequency noise in metal-oxide-semiconductor structures was first theorized by A.L. McWhorter [9]. McWhorter postulated that the source of the low-frequency noise was due to the interaction of surface charge with slow traps in the oxide near the interface. These interface traps had a sufficient spread in energy such that the summation of these traps spanned many decades of time constants and could account for a $1/f$ slope spanning many decades of frequency.

While today there remains little doubt as to the origin of $1/f$ noise in MOSFET devices; other theories as to the origin of $1/f$ noise in other semiconductor devices revolve around mobility fluctuations. These theories are primarily the result of work by F.N. Hooge [10].

2.6.1 1/*f* Noise in MOS Devices

It is well understood now that the source of $1/f$ noise in n-MOSFETs is due to number and mobility fluctuations [11, 15]. The number fluctuation is measured as a change in the number of carriers flowing through the device. The mobility fluctuation is taken into account in a unified model to describe the Coulombic scattering by the trapped carriers.

The SPICE NLEV=0 noise model is derived by substituting the MOSFET device equations into equation (2.9) and recognizing that $S_G/G^2 = S_i/I^2$ in:

$$S_i = \frac{K_f \mu W \left(V_{gs} - V_t\right)^2}{2L^3 f} \tag{2.12}$$

where K_f is a fitting parameter, μ the carrier mobility, W and L the width and length of the MOSFT, $\left(V_{gs} - V_t\right)$ the excess gate voltage above threshold. A more accurate model for the flicker noise in MOSFET's is the unified flicker noise model as developed by Hung. It is called a unified model because it brings together the correlated number and mobility fluctuations to describe the drain current modulation as [15]:

$$\frac{\Delta I_d}{I_d} = -\left(\frac{1}{\Delta N_{inv}} \frac{\delta \Delta N_{inv}}{\delta \Delta N_{it}} \pm \frac{1}{\mu_{eff}} \frac{\delta \mu_{eff}}{\delta \Delta N_{it}}\right) \delta \Delta N_{it} \tag{2.13}$$

The first term in 2.13 describes the number fluctuation while the second term describes the mobility fluctuations. In the linear region of operation at low drain bias the power spectral density of the drain current becomes:

$$S_{I_d} = \frac{kTI^2}{\gamma f W L}\left(\frac{1}{N} + \alpha\mu\right)^2 N_t\left(E_{fn}\right) \tag{2.14}$$

Equation 2.14 describes the noise in the drain current of a MOSFET due to oxide traps at a particular quasi-Fermi level, $N_t(E_{fn})$. The theory presented in this research will taken a different approach then considering mobility degradation but instead consider the effects of the modulation of percolation currents due to the localized conductivity modulation from the field of trapped charge in the oxide.

2.6.2 RTS Noise in MOS Devices

RTS noise in MOS devices has provided an interesting tool for studying the behavior of traps and poses interesting engineering challenges. It is well established now that RTS in MOS devices is the result of the capture and emission of minority charge carriers in the gate oxide of the device. There has been extensive work in modeling and understanding the mechanisms at play [13 - 24]. The action and behavior of traps is well understood, so much of the modeling has revolved around understanding the large modulation of the current that is observed in the measurements [25-28].

In general the behavior or capture and emission rates of traps are taken from considering Shockley-Reed-Hall (SRH) statistics and assuming a tunneling capture mechanism. These rates are expressed as the mean time-to-capture, τ_c, and the mean time-to-emission, τ_e as:

$$\tau_c = \frac{1}{n_s \sigma_n v_{th}} \tag{2.12}$$

where n_s is the density of carriers in the vicinity of the trap, σ_n is the capture cross section, and v_{th} is the thermal velocity of the carriers.

and

$$\tau_e = \frac{1}{\sigma_0 g \eta T^2} exp\left[\frac{\Delta E_B - \Delta E_T}{kT}\right] \tag{2.13}$$

σ_0 is the capture cross section, g is the degeneracy fact, η is a device specific fitting parameter, and T the temperature in Kelvin.

These are the basic relationships that describe the trapping times and in general adequately model the behavior of the high and low time constants observed in MOSFET RTS.

Two approaches have been taken to model the RTS amplitudes. One, approach is to model the effect that a trapped charge has as imaged to the parasitic capacitances mainly those between the oxide capacitance, C_{ox}, the inversion charge capacitance, C_i, or equivalently $q^2 N_i/kT$, and the depletion region capacitance, C_D. Assuming a number fluctuation model the drain current modulation due to the trapping of a single charge is described as:

$$\frac{\Delta I_d}{I_d} = \frac{1}{A}\frac{q\beta}{(C_{ox} + C_D + C_i)} \tag{2.14}$$

where A is the device area, and β is q/kT.

In the second approach a cored out area of low conductivity due to the trapped charge reduces the carrier number in the channel by an amount equal to this reduced device area. In this approach the field setup by the trapped charge creates an exclusion zone depending on the depth of the trap into the oxide and the level of inversion charge in the channel. The model for this is:

$$\frac{\Delta I_d}{I_d} = \frac{L_t}{W} \tag{2.15}$$

where L_t is the effective radius of this trapped charge field. This second approach is the foundation for model described here in Section 5. The model described in Section 5 merges both concepts to also include the non-uniform current distribution due to the effect of ionized dopant charge in the channel and bias dependence of the induced field.

2.7 1/*f* and RTS in Circuits

The following sections provide examples from published research on the impact of RTS noise in circuits. These specific examples highlight the importance of understanding this noise mechanism as it applies to MOSFET subthreshold device leakage and to bit-error rates (BER) in dynamic-random access memory (DRAM) architectures. These examples show that RTS noise plays an integral role on the performance of high density memories where noise can cause unacceptable errors if device optimizations for noise are not considered.

2.7.1 Subthreshold Leakage Due to 1/*f* and RTS Noise

Noise signals can be represented in either the frequency domain or the time domain. The modeling in the frequency domain using the SPICE model gives the mean square noise of a transistor as:

$$i_n^2 = \frac{K_f {I_{ds}}^{\alpha_f}}{C_{ox} {L_{eff}}^2 f^{e_f}} \qquad (2.16)$$

where K_f is the l/*f* noise parameter, L_{eff} the length, and W the width of the transistor channel, μ the mobility, (V_{gs}-V_t) the excess of gate voltage above threshold, and e_f, α_f are fitting parameters. The modeling of the RTS or l/*f* noise of nanoscale devices

that is easiest to understand is that done in the time domain. The capture and emission of a single electron in a nanoscale NMOS transistor of size W/L can be equated to a change in threshold voltage, V_T, as:

$$\Delta V_T = \frac{q}{C_{ox}WL} \tag{2.17}$$

where q is the electronic charge, and C_{ox} is the gate capacitance. This fluctuation of the threshold voltage can modulate the surface potential causing high subthreshold leakage states.

Modern devices are now small enough that we can see RTS noise signals associated with single electron trapping. RTS type traps, with single electronic charge fluctuations, are easily observable on minimum size devices which show discrete switching events in the time domain signal, Figure 2.5.

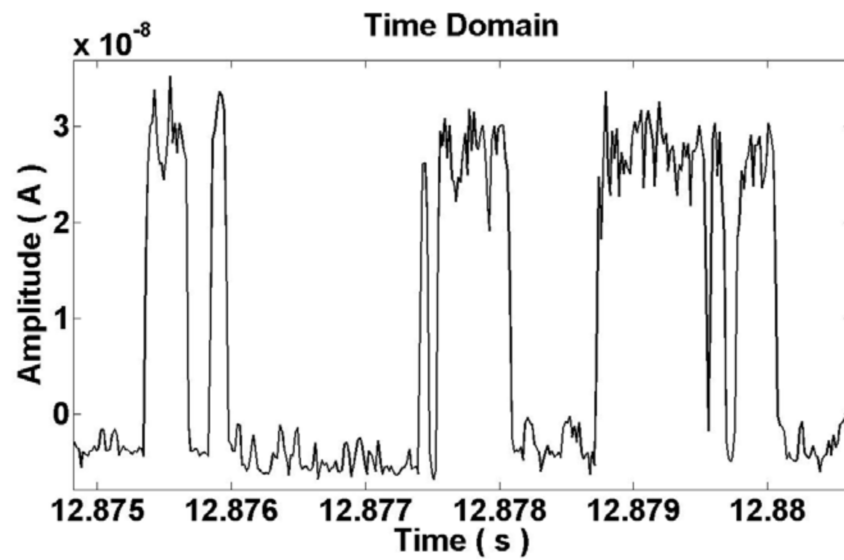


Figure 2.5 Single Electron RTS

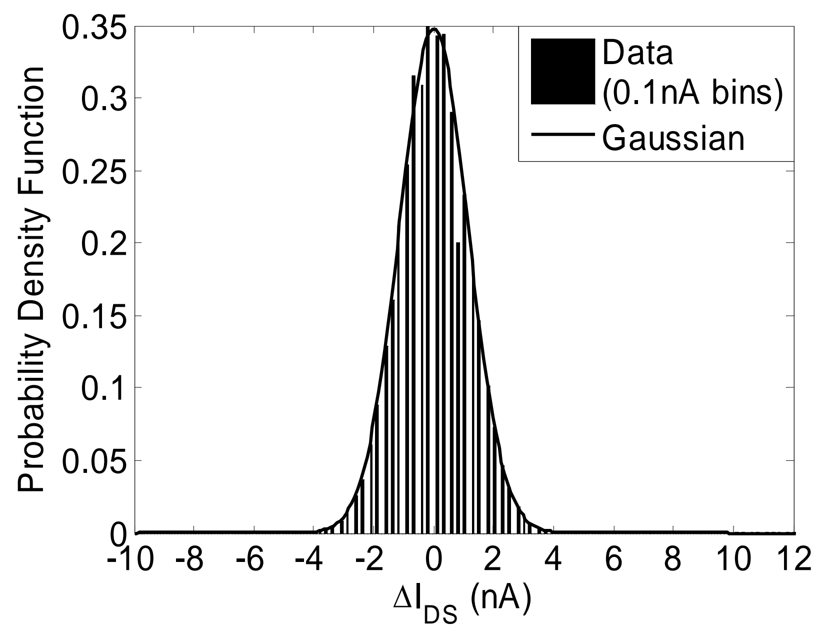
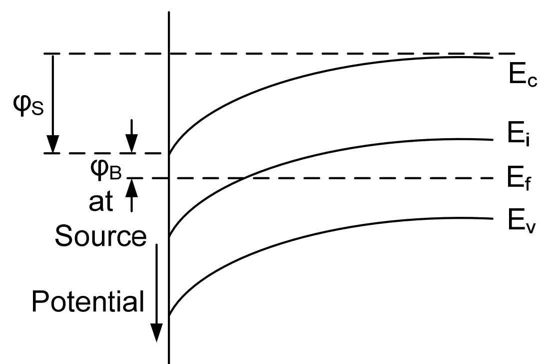
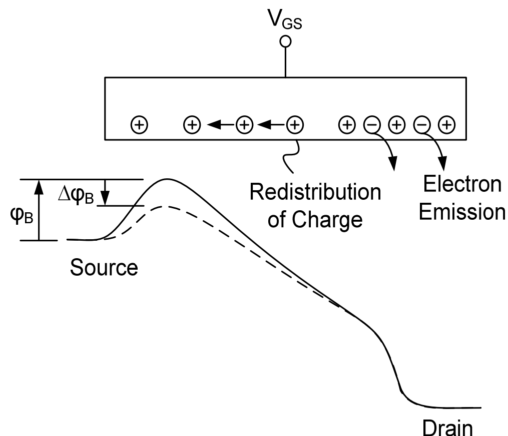


Figure 2.6 Histogram of l/*f* noise from a large device

In wider devices, with dimensions greater than 1µm, a large number of these individual RTS signals combine to give a Gaussian or Normal distribution in 1/*f* noise amplitudes and drain current variations, Figure 2.6. A simple estimate shows that one of these RTS traps changing charge state in the channel will modulate the subthreshold leakage as shown in Figure 2.7.



(a) Energy band diagram at the source.



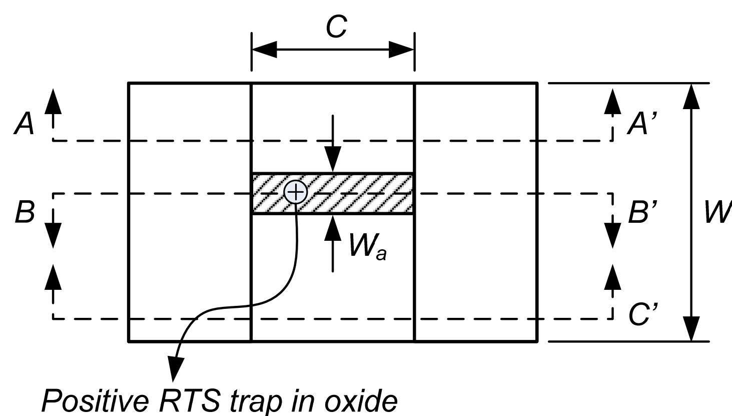
(a) Charge redistribution on gate.

Figure 2.7 RTS due to traps in the channel region

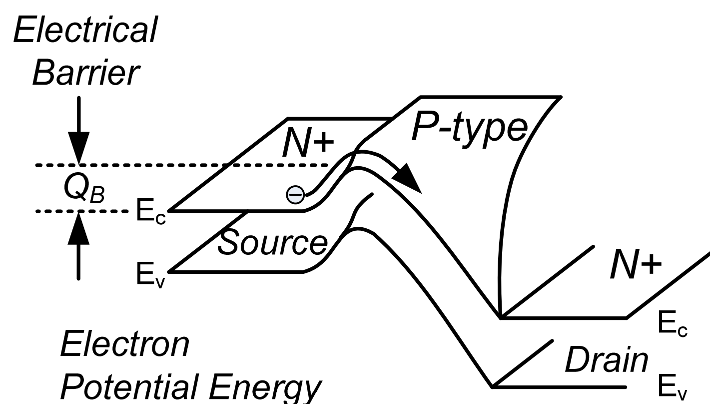
This change in oxide charge will cause a redistribution of charge on the gate and a uniform change in threshold voltage. It should be noted from [28] to quote “in Eq. 6 the subthreshold current exhibits an exponential dependence on the oxide charge. A small variation in the oxide charge can cause a significant subthreshold current transient." The subthreshold current varies as $e^{\varphi_s/kT}$ and if there is a threshold voltage variation then as $e^{\varphi_s/kT}\ e^{V_T/kT}$ or exponentially on the oxide charge or threshold voltage. This change in threshold voltage will result in a uniform change in the current distribution across the width of the gate and source. There can and will however be a distribution in possible magnitudes of the threshold voltage change, this is a Gaussian distribution on large devices, Figure 2.5(b). This noise current will result in a widening of the Gaussian distribution and the symmetrical wings on the bottom of the distribution as shown in Figure 2.8.

A trap near the source will be most effective in modulating the subthreshold leakage since only the surface potential near the source determines the number of carriers in the subthreshold equation. A local change in the surface potential barrier at the source could easily cause a large modulation in the localized subthreshold leakage. Figure 2.7(a) demonstrates a strip model with a positive oxide trap. The current flow through this strip can be fully or partially modulated by the capture and emission of charge at the trap site. Outside of the strip the surface potential is determined by the barrier at the source due to the doping of the channel and the charge on the gate. Figure 2.7(b) shows an increased barrier as compared to Figure

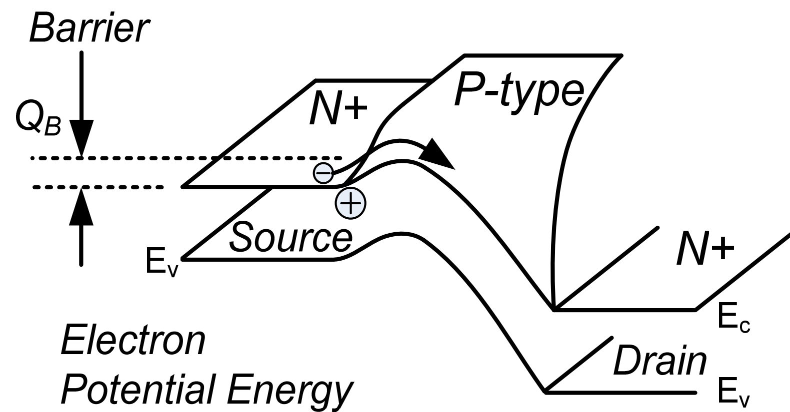
2.7(c). In Figure 2.7(c) the barrier is reduced by the positively charged trap in the gate oxide. This reduced barrier causes an exponential increase in the current under the gate until a carrier is captured which increases the local potential barrier and instantaneously reduces the current flow. The localized conduction channels are the cause of large amplitude subthreshold current changes and distort the Gaussian distribution.



(a) Strip model of MOSFET channel region



(b) Cross section A-A' and C-C'



(c) Cross section B-B'.

Figure 2.8 RTS model for subthreshold leakage

In the case of submicron size devices subthreshold leakage is critical in determining the retention time of DRAM's. Published results show a nominal RTS threshold voltage threshold voltage step of 10mV on a minimum size device in a 90 nm technology with 9nm gate oxides [29]. For 50 nm technology with 2 nm gate oxides and a transistor size of W/L = 0.5μ/0.5μ this translates into a similar threshold voltage distribution if we assume the l/*f* noise varies according to the SPICE noise level 0 model. Most minimum size 50 nm x 50 nm will have on the average four traps. The probability of a RTS trap near the source is low. However, if a single electron RTS trap near the source changes charge state to a more positive charge state this in turn modulates the local surface potential barrier near the source as shown in Figure 2.8. This changes the subthreshold leakage exponentially in the local region. The resulting localized channel or percolation channel can result in a large current change and an asymmetrical distortion of the distribution, Figure 2.9.

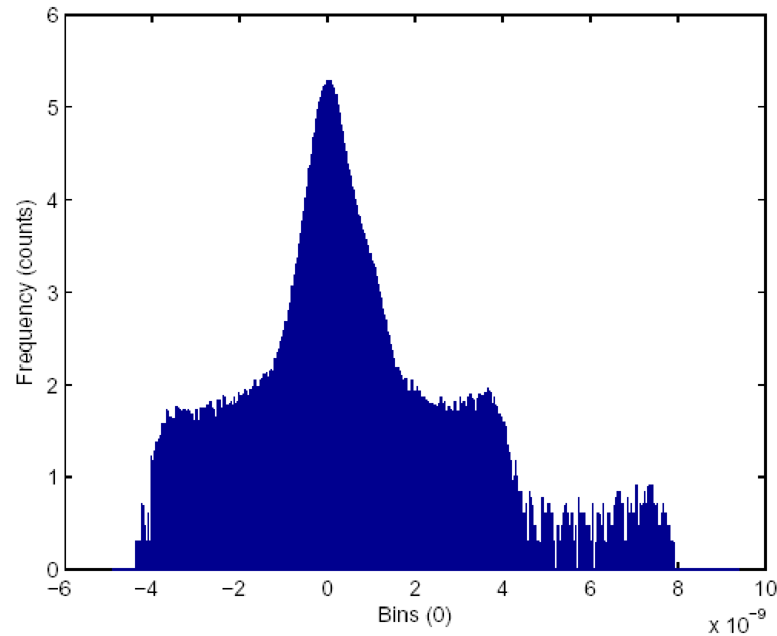


Figure 2.9 Drain current distributions on a nanoscale 0.2um transistor

In Figure 2.9 there is a low but finite probability of 8 nA current pulses About 1/100,000 RTS noise signals will be a multiple electron event resulting in a large leakage current pulse about forty times the amplitude of the RMS variation. Even larger subthreshold current pulses will occur but at a lower probability. The magnitude in Figure 2.9 suggest a percolation channel a few Angstoms wide.

A random and variable error occurring in the transfer device due to subthreshold leakage from RTS or l/*f* noise can cause errors or variable retention time in memory cells. There is a low but finite probability of large amplitude current pulses in the subthreshold leakage of nanoscale transistors which assuredly will cause errors in reading the small voltage levels in high-density memories.

2.8 RTS Noise in MOSFET circuits

2.8.1 RTS Noise in Sense Amplifiers

An analysis has previously been made of the increasing portion of the threshold voltage being occupied by thermal noise levels and the bit error rates in digital logic [30] and memory circuits [31-33]. No consideration was, however, given to the errors that might be caused by l/*f* noise or random telegraph signals.

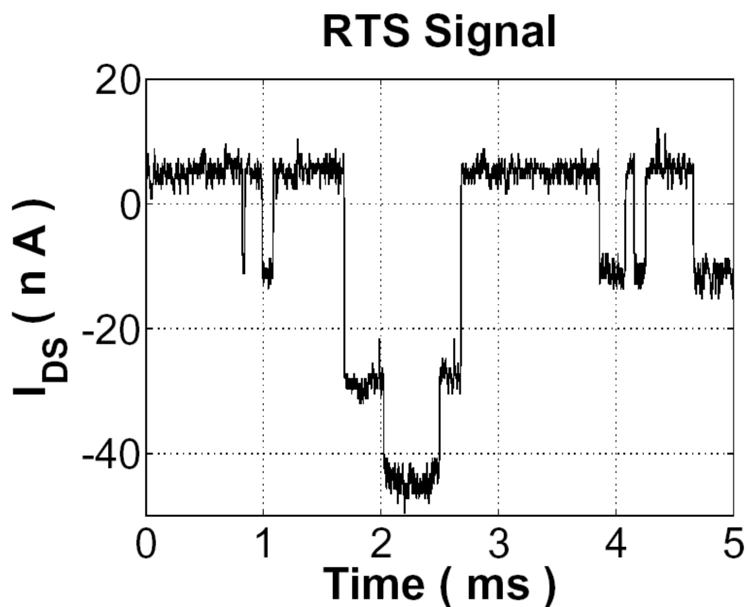


Figure 2.10 RTS signal due to trapping and emission of multiple electrons in a nanoscale n-channel CMOS transistor.

2.8.2 1/*f* Noise

1/*f* noise signals are typically modeled in the frequency domain. The SPICE noise level 0 model for a device in saturation, gives the mean square noise current of the read transistor as shown in (2.18) below:

$$i_n^2 = K_f \mu W \left(V_{gs} - V_T\right)^2 / (2L^3 f) \tag{2.18}$$

where, K_f is a 1/*f* noise fitting parameter mostly dependent on process, L is the length, W the device width and, μ the mobility. The voltage read error due to the 1/*f* noise current in (2.18) of a sense amplifier transistor can be expressed as:

$$\Delta V = \frac{\sqrt{\int_{f_l}^{f_h} i_n^2 df \, \Delta t}}{C_{bit}} \tag{2.19}$$

and substituting equation 2.18 into 2.19 results in the read error voltage for a particular device size and process conditions.

$$\Delta V = \frac{\left(\left(\frac{K_f W \mu}{2L^3}\right) ln\left(\frac{f_h}{f_l}\right)\right)^{1/2} (V_{gs} - V_t)\Delta t}{C_{bit}} \tag{2.20}$$

where f_l and f_h are the low and high frequency bandwidth limits, Δt is the access time of the signal at the sense amplifier, and C_{bit} the bit line capacitance. This average or mean error signal will be small of the order mV. This however is the mean read error voltage; there is small but finite probabilities of much larger read errors, such as tens of mV, see Figure 2.11.

The probability that there will be a coincidence of occurrence of a number of

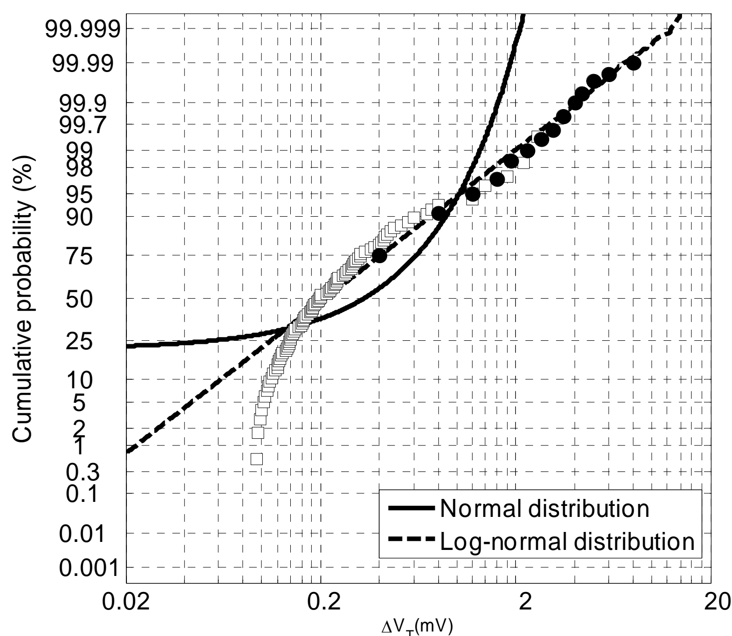


Figure 2.11 Calculated threshold voltage distributions on a 50nm transistor with a 2nm gate oxide and gate width, W=2500 nm or W=2.5μm, a very wide device, data taken from [29].

electrons contributing to a large change in threshold voltage and causing an error has been found to be described by a log-normal distribution. In a log-normal distribution the probability of a large value is of the order $e^{(-x)}$.

Figure 2.12 shows a simplified representation of a sense amplifier in a dynamic random access memory (DRAM). The charge stored on the storage capacitor is discharged on to the bit line when the word line is activated. This causes a signal to be applied to the cross coupled sense amplifier. This signal appears as a differential signal and causes an imbalance in the sense amplifier which is amplified.

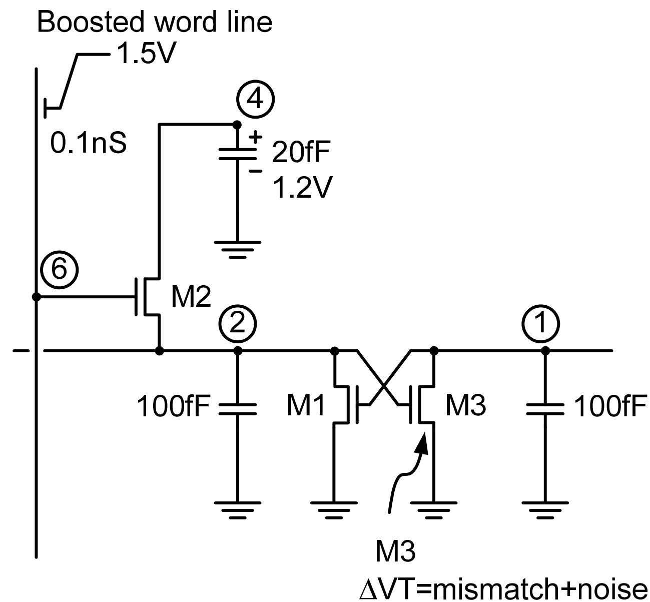


Figure 2.12 Circuit diagram of a simplified sense amplifier.

RTS noise signals also, however, appear as an offset causing an imbalance in the sense amplifier. If these two signals have opposite polarities than the noise signal can be dominant causing an upset of the sense amplifier and erroneous output. Figure 2.13 illustrates the sensitivity of the sense amplifier to noise signals and gives the change in threshold voltage caused by noise which will upset the sense amplifier causing an error [35-37].

The sensitivity of the sense amplifier is affected by the time delay over which the noise has had an opportunity to determine the output state. A representative value is that about a 20 mV threshold voltage offset is sufficient to cause an error if this delay is 100 ps.

Figure 2.11 shows there is about a 0.001% probability, or 10^{-5} probability of an 8mV threshold shift in the transistors due to RTS noise. A 20mV threshold voltage shift causing an error will occur with a probability of about 10^{-11}. This is still a high error rate for modern high-density memories so that a proper design would require larger device widths to reduce the error rate. Similar calculations can be made for other device sizes or width to length ratios.

If a DRAM sense amplifier is upset by a threshold voltage mismatch of ΔV_T then Figure 2.13 shows the calculated error rate. In reality there may not be an error or variable retention time in the memory cell but rather a random and variable error occurring in the sense amplifier due to RTS or l/*f* noise. This could happen as often as every time a Gbit DRAM is read without proper design and consideration of RTS noise.

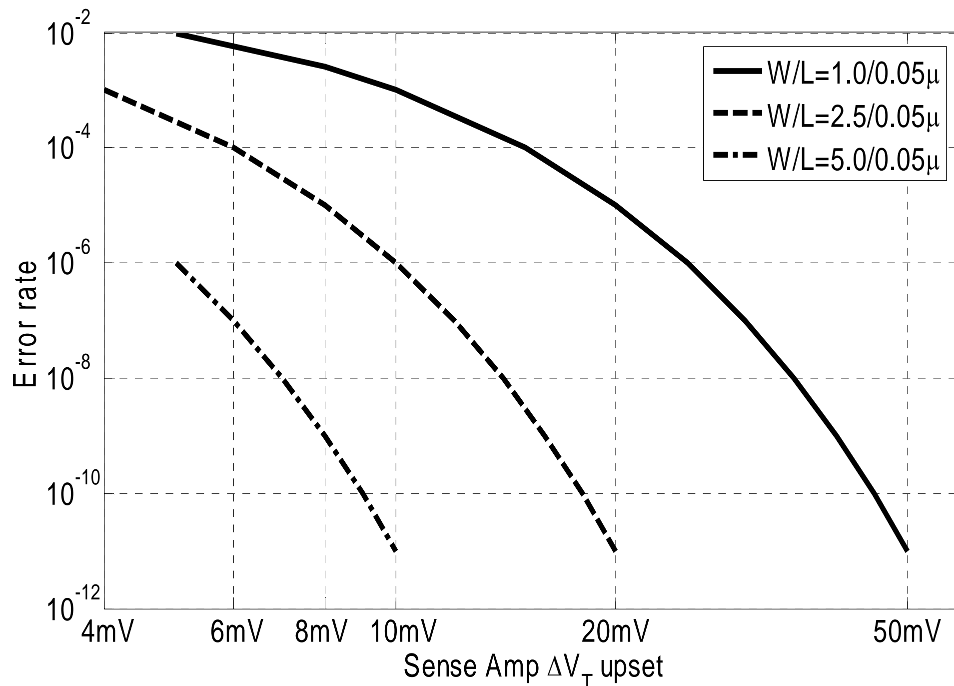


Figure 2.13 Error rate on a DRAM sense amplifier due to upset by V_T mismatch for different W/L values.

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3 RTS Noise Measurement Methods

Interesting information about the traps that exists in the MOSFET system is readily obtained through RTS noise analysis. Especially with large RTS swings the ability to capture these events is not difficult. RTS noise analysis on deep-submicron devices first requires a noise measurement system with sufficient bandwidth and gain to capture the transitions of the random telegraph signal above the background noise, or noise floor, of the test system. A system bandwidth of 30 kHz is most often sufficient to accomplish this as well as a system noise floor of 1×10^{-25} A^2/Hz. The highest possible bandwidth and a noise floor below that of the device under test is a basic requirement for any noise measurement system.

The MOSFET devices used during the course of this study were acquired from MagnaChip Semiconductor of America. These devices are manufactured using a 0.11μ CMOS process. The process followed a standard twin-well CMOS flow. A twin well process is such that each device type is fabricated in a well of dopant which raises the doping level of the substrate higher than what is found in the bulk substrate. The well implant raises the background doping level from 1×10^{15} #/cm^3 to 1×10^{17} #/cm3. After the well has been formed there are two additional implants which serve as the anti-punch through and the threshold adjustment. The primary focus was on the devices that are used in the pixel of a CMOS image sensor (CIS) and in particular the source follower transistor. For the

noise measurements the devices were biased in a manner representative of typical operation. The typical bias currents for these devices ranged from 1µA - 5 µA.

3.1 Noise Test System

The primary concern in the design of a noise test system is that the system be capable of measuring the low-level fluctuations which are usually buried in a dc current or voltage level and have sufficient bandwidth to characterize the noise over some span of frequencies. For the noise study carried out in this research a basic low noise system was constructed which consisted of a battery powered bias circuit, sense resistor, PAR 113 low-noise amplifier, 16-bit analog-to-digital converter, and finally a PC to capture and record the data to disk for later post-processing. In some instances a transimpedance amplifier circuit was also used to measure the noise current through the device. The bias circuit was fabricated on a custom printed circuit board (PCB). Figure 3.1 is a schematic of the circuit used for the biasing of the DUT. Fast diodes are used to protect the gate of the DUT for both positive and negative voltages as well as from electrostatic discharge. The current noise of the DUT is measured across the sense resistor, RL, at the node Vn. The noise signal is then fed into the low-noise amplifier (LNA). The LNA is capable of providing gain and bandwitdth limits to the input signal. The output of the amplifier drives a 16-bit National Instruments USB-6251 Data Acquisition System. Inside the PC the data is

captured and stored for post processing to include statistical analysis and noise power spectrum generation.

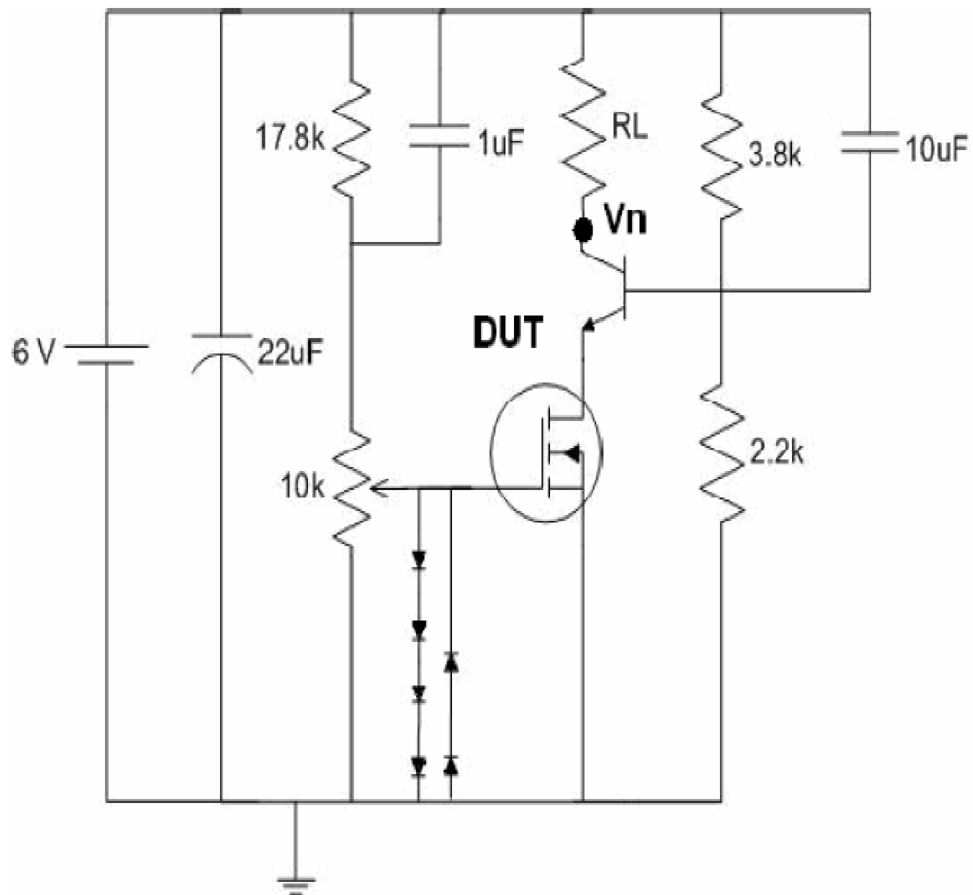

Figure 3.1 DUT bias circuit schematic

At the time of measuring the noise of the device the magnitude of the device noise is unknown, so one approaches the characterization of the test system by first measuring the noise floor of the system using a known quantity or standard with confidence. A good standard is a resistor, typically a wire wound or metal film, or a

reverse biased diode that has been independently measured. The standard is then placed in the signal chain in place of the DUT. This research made use of resistor measurements to determine both the noise floor and signal bandwidth of the overall

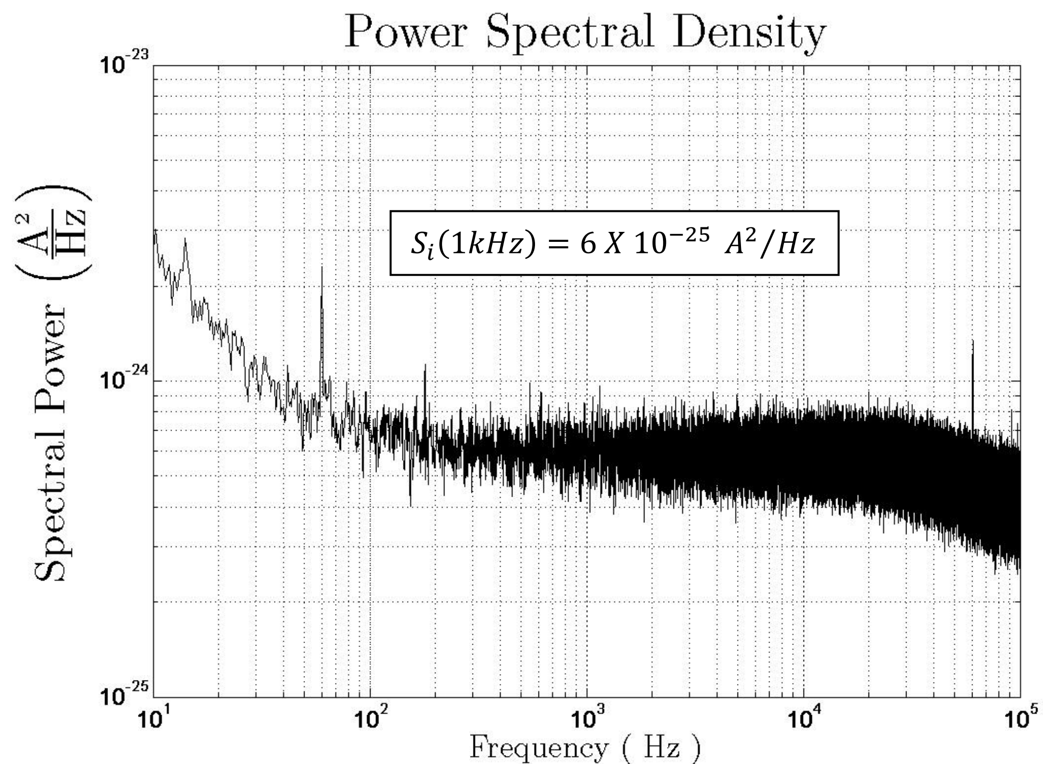

Figure 3.2 Measure background noise using a 100kΩ metal film resistor in place of device and a 100kΩ biased at 5µA.

test system. The background noise was measured with a 100kΩ resistor in place of the DUT as shown in Figure 3.2. Upon analysis of the noise it is found that the noise of the system is 2X higher than expected from the measurement of a 100kΩ resistor alone; however, this has shown to be more than sufficient for detection of

RTS signals. The sense resistor contributes additive noise to the measurement. Combining the two thermal noise sources total expected noise is:

$$S_i = 2i_n^{thermal} = 2(1.66 X 10^{-25}) = 3.33 X 10^{-25}\ A^2/Hz \quad (3.1)$$

From the noise spectral plot of Figure 3.2, the high frequency bandwidth of the system can is deduced from the -3dB point to be 30 kHz. The bandwidth of the system was also verified through frequency sweep analysis to be 30 kHz when a 100kΩ sense resistor is used in place of the device.

The DUTs were all mounted in 24-pin Dual In-line Packages (DIP). The DIP package was seated into a 24-pin zero-insertion force (ZIF) socket for connection to the PCB bias circuitry. The ZIF socket allowed the easy removal of devices for testing of multiple packages.

3.2 Device Under Test

The devices that were tested during the course of this research primarily consisted of those transistors found in the array of 4T CMOS image sensor pixel architecture, specifically the source follower. The 4T architecture consists of a photodiode, transfer gate, reset, source follower amplifier, and row select transistors. The source follower is the transistor that performs the charge to voltage conversion and will be further described in section 6. A large majority of the noise testing focused around

the characterization of the source follower transistors. In a typical 4T CIS process the array and periphery use different devices. The primary difference between the pixel array transistors and those found in the periphery is an implant into the sidewall of the shallow trench isolation (STI) region; see Figure 3.3(b). This implant which is known as a channel-stop implant (CST) which effectively raises the threshold voltage for that region is for suppressing any parasitic MOSFET which might form under the trench. Another primary benefit of this implant is that the dark current, which may be generated by defects at the silicon-oxide interface, is reduced increasing the overall SNR and dark current of the pixel. One other important difference is the thickness of the gate oxide. The array transistors were manufactured with a 65 angstrom effective gate oxide while the periphery used a 32 angstrom effective gate oxide thickness. This difference in the gate oxides stems from the voltage requirements on the array which allows the use of up to 3.6V while the logic core uses a much lower supply voltages of 1.8V for the digital functionality of the device.

The test structures measured for this research contained the individual transistors which came from a number of locations across the wafer. The current baseline for the array design utilized a 0.36µ x 0.36µ sized devices. This particular transistor size was of interest, so the majority of the experimental results come from these transistors sizes. Figure 3.3, on the next page, shows the general device structure. In this process the shallow-trench isolation (STI) is formed first, followed

by the NCST implant and deep p-well implants. The STI is then filled with oxide and a sacrificial oxide is grown. Next anti-punch through and threshold implants are performed. The sacrificial oxide is then removed and the gate oxides are grown. Finally, poly is deposited and implanted to form the gate metal.

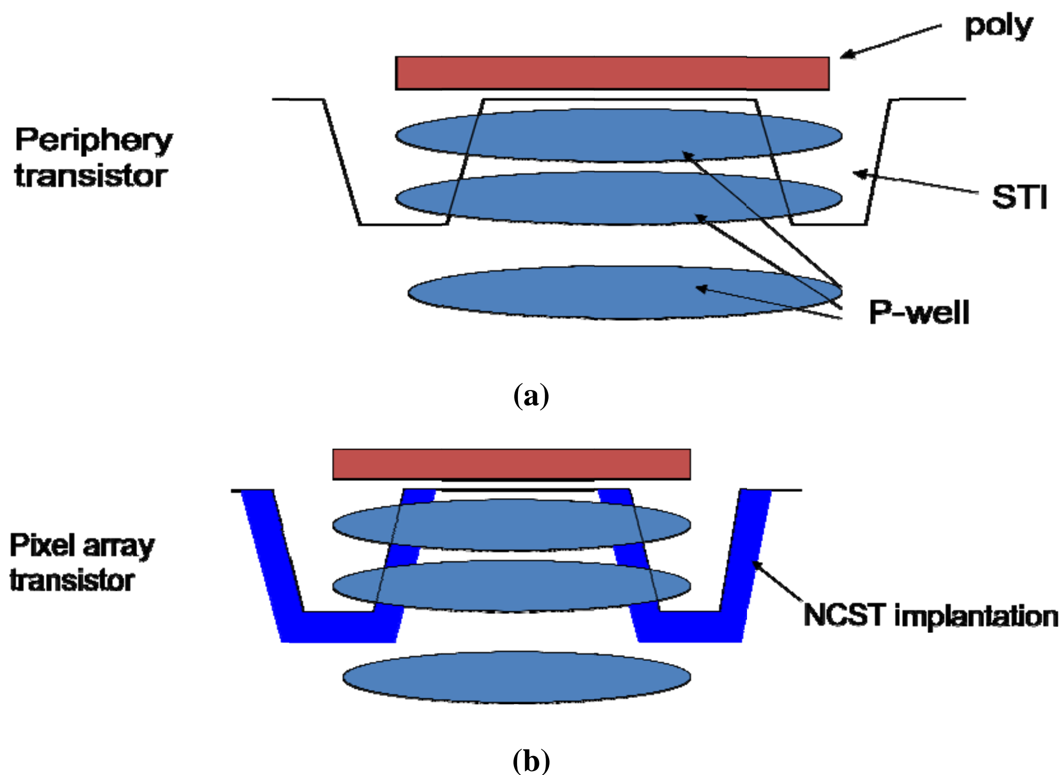

Figure 3.3 Implant Profile for: (a) Periphery transistor and (b) Pixel transistor.

3.3 Time Domain Noise

The drain current of a DC biased submicron MOSFET transistor exhibits discrete switching events as seen in Figures 3.4 and 3.5, on the next page. Each of these

signals shows the existence of multiple active trapping signals. These noise signals show the action of traps with sub-millisecond as well as long many millisecond time constants. These noise signals were captured using the system described previously.

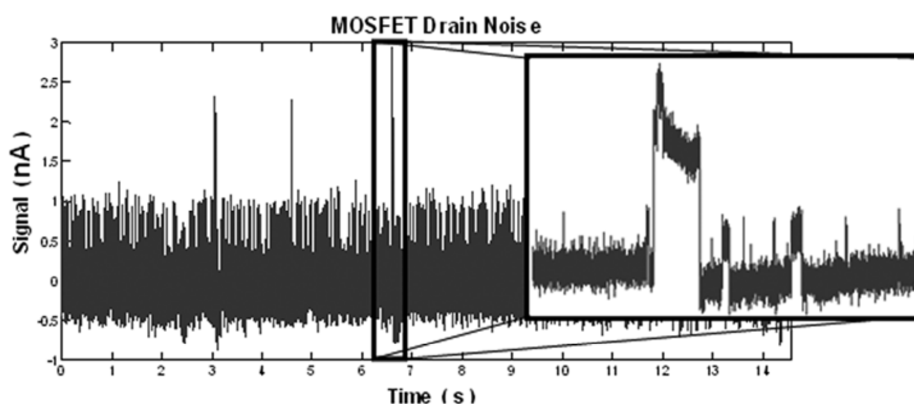

Figure 3.4 Noise signal trace of a DC biased MOSFET with W, L = 0.35µm. The inset of the figure shows a zoomed-in picture of the recorded data demonstrating the discrete current fluctuations.

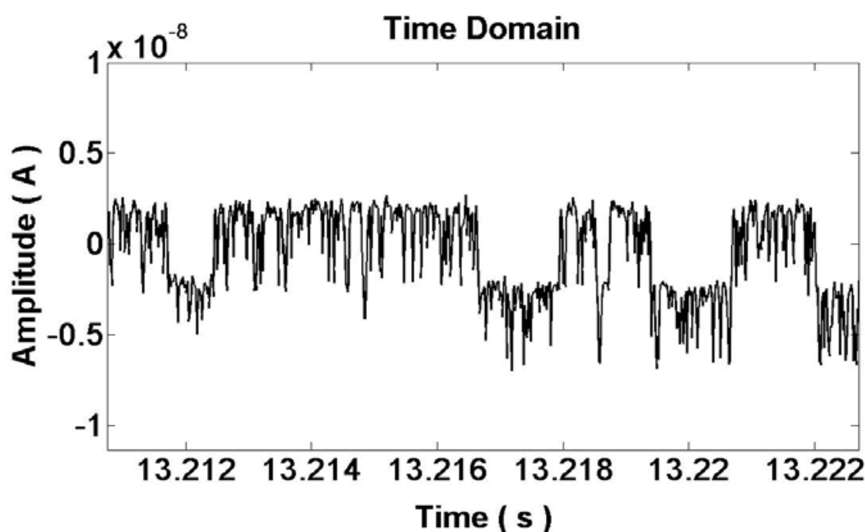

Figure 3.5 Drain current noise signal showing multiple active traps

3.4 Trap Histogram Analysis

Probably the most basic statistical analysis performed on the time domain RTS signal is generating the histogram of the measured signal amplitudes. As basic as it may be, these histograms are powerful visualization tools for understanding the behavior of the RTS present in the signal. Often times the number of traps can be distinguished very easily by simply looking at the histogram and counting the number of peaks. When discrete peaks are present the number of traps is simply $\log_2(N)$ where N is the number of observed peaks. Other times there are so many traps that all the RTS signal merge together and the distinction of the individual trap signals becomes much more of a challenge.

The histogram is the basis for distinguishing a trapping signal with a clear threshold between a high and low signal state. Having a clear separation between high and low signal state allows one to set a threshold for counting the number of times the trap captures and releases the carrier. Figure 3.5 is a classic example of a signal that can be characterized for its trap location. Without this clear distinction between the high and low state it is very difficult to carry out the trap location analysis as demonstrated in Section 3.5. In some instances the signal will start out at a particular gate voltage with a clear single RTS and after changing the gate bias additional traps are activated and make separation of the two signals nearly impossible.

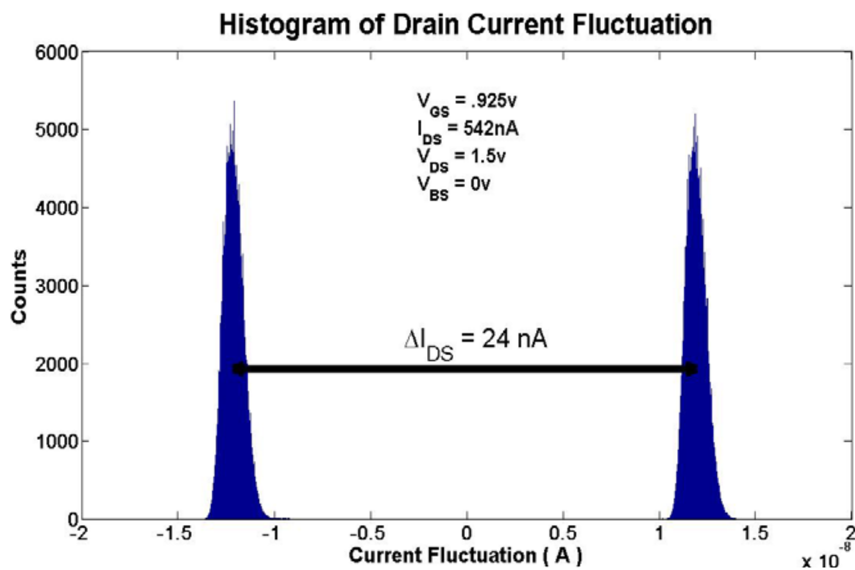

Figure 3.6 Histogram of a single RTS trapping signal

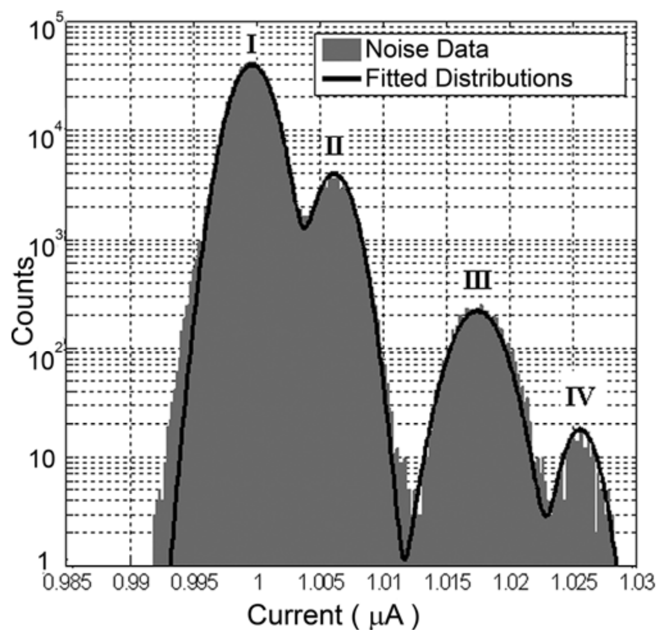

Figure 3.7 Histogram of recorded signal of MOSFET drain noise. Two traps are readily seen as 4 peaks in the data. Peaks I and III are one trap and peaks II and IV are a second trap.

3.5 RTS Noise Spectrum Analysis

Following the histogram the next level of sophistication of RTS analysis is generating the noise power spectrum. This can be done in a number of ways; however, in this research the primary method is to use a non-parametric periodogram smoothing algorithm called the Welch method. The details of the Welch method are described in Appendix A. In summary the Welch method breaks the data into a number of equally sized segments and applies a windowing function to each of the data sections, calculates the power spectrum for each segment, and finally averages the individual spectrums together. With this method the segment size and data overlap are tailored to get high-resolution noise spectral plots while at the same time minimizing the variance in the plot. With the proper choice of parameters the result is a much smoother plot than what is expected from just using a pure Fast Fourier Transform.

3.6 Trap Analysis

Locating the position of a trap in the oxide is a powerful use of the RTS signal waveform. This technique estimates the location of the trap in the oxide by changing either the gate or drain voltage and observing the change in the RTS signal. In most cases the RTS signal waveform changes behavior when the gate or drain voltages are modified. The general equation that describes the ratio of the capture and emission times is shown below:

$$\frac{\bar{\tau}_c}{\bar{\tau}_e} = \gamma e^{-(E_T - E_F)/kT} \tag{3.2}$$

From this equation the depth of the traps can be extracted by expanding (3.2) above resulting in:

$$ln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right) = -\frac{1}{kT}\Big[(E_{Cox} - E_T) - (E_C - E_F) - \chi_0 + \psi_s + q\frac{x_T}{T_{ox}}\left(V_{gs} - V_{FB} - \psi_s\right)\Big] \tag{3.3}$$

and finally differentiating equation (3.3) with respect to V_{gs} results in:

$$\frac{dln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right)}{dV_{gs}} = -\frac{q}{kT}\frac{x_T}{T_{ox}} \tag{3.4}$$

Rearranging (3.4) results in the trap location as:

$$x_T = -\frac{kT}{q} T_{ox} \frac{dln\left(\frac{\bar{\tau}_c}{\bar{\tau}_e}\right)}{dV_{gs}} \tag{3.5}$$

This equation has been applied to measurements performed on RTS signals in deep submicron MOSFETs here and elsewhere [2-4]. Below in Figure 3.8 is the trapping

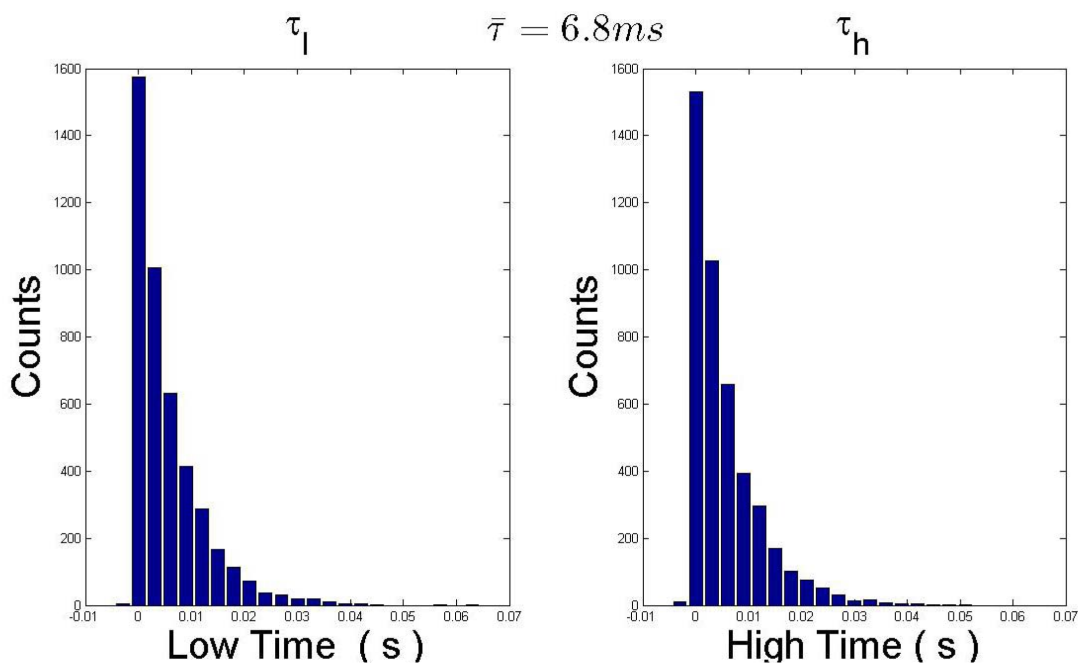

Figure 3.8 Trapping time distribution in the high and low state from signal in Figure 3.6

and emission times for the trap signal shown in the histogram of Figure 3.6. At this bias condition that trapping times are nearly symmetric and there is an equal probability of the trap being in either state as also seen in the histogram. Figure 3.9 shows the typical dependence that gate oxide traps have with gate bias. This shows that the time-to-emission has a weaker gate bias dependence as compared to the time-to-capture.

From equation 3.2 it was shown that the time-to-capture has a negative exponential dependence on the difference in the trap and Fermi energy levels. Figures 3.9 and 3.10 show the trap depth extraction technique for a pure gate oxide device and Figure 3.10 and 3.11 shows the same technique as applied to a plasma nitride gate.

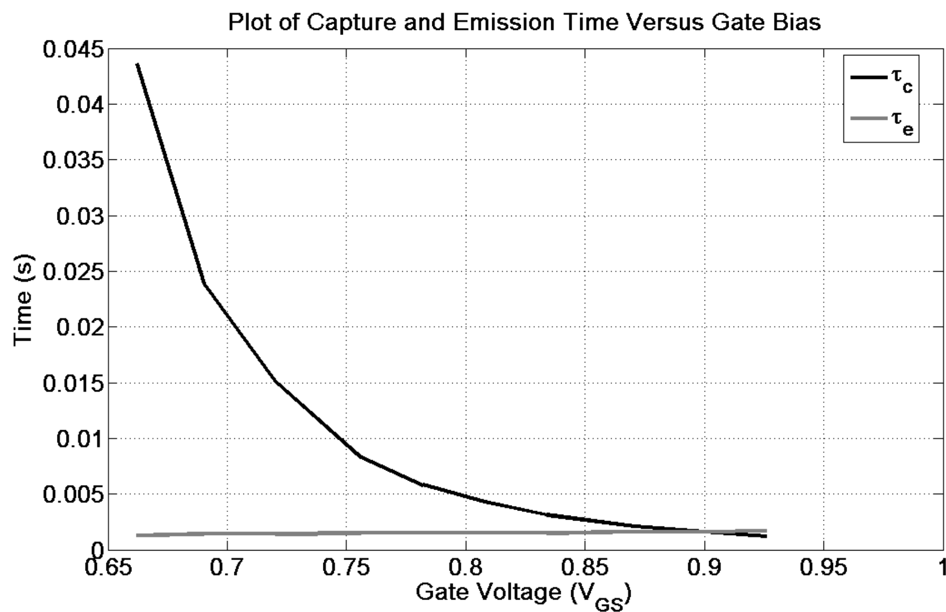

Figure 3.9 Plot of capture and emission times versus gate voltage for a pure oxide MOSFET

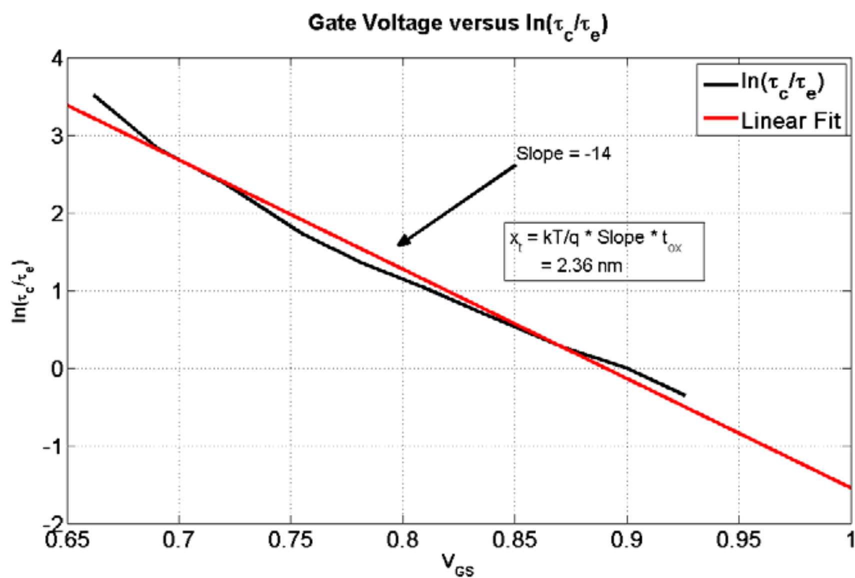

Figure 3.10 Trap location analysis of a pure oxide gate MOSFET W/L = 0.36/0.36 micron, t_{ox} = 65 Angstroms

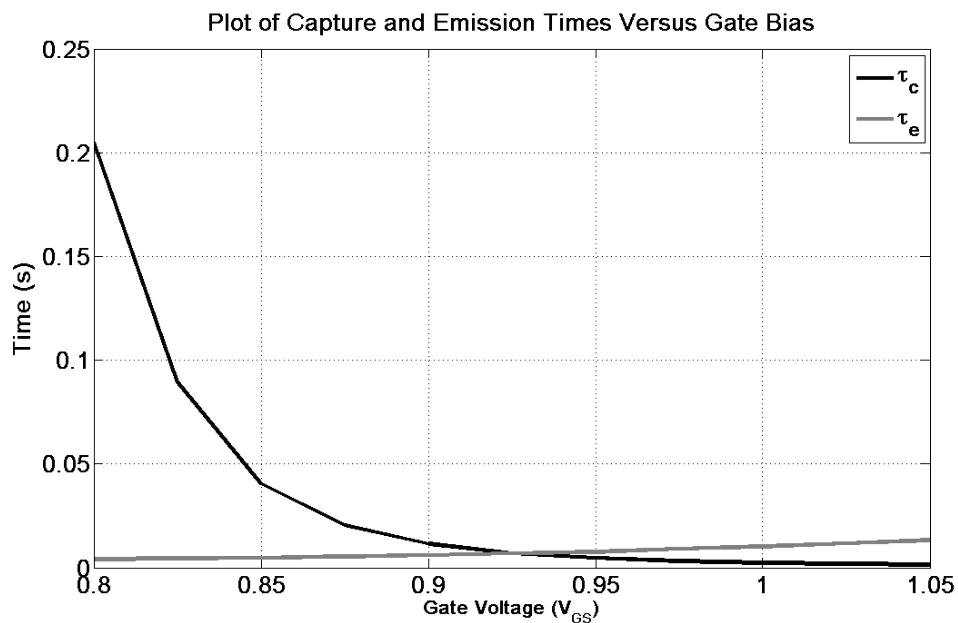

Figure 3.11 Capture and emission times versus gate voltage for a plasma nitride gate MOSFET

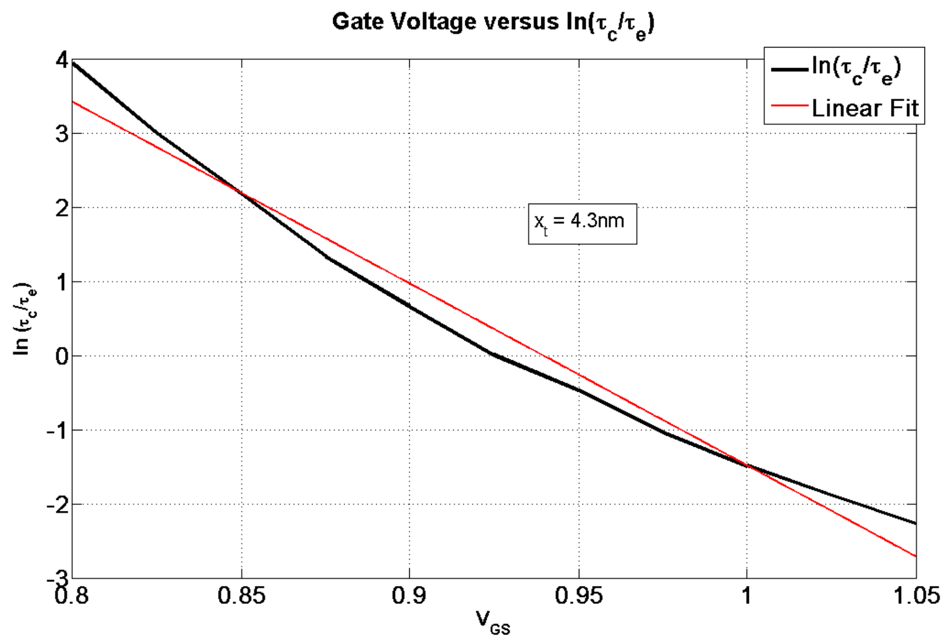

Figure 3.12 Trap location analysis for plasma nitrided gate W/L = .36/.36 micron, Tox = 65 Angstroms

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[2] Zeynep Celik-Butler, Petr Vasina, and Nuditha Vibhavie Amarasinghe, "A Method for Locating the Position of Oxide Traps Responsible for Random Telegraph Signals in Submicron MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 3, March 2000.

[3] Nuditha Vibhavie Amarasinghe, Zeynep Celik-Butler, Petr Vasina,"Characterization of Oxide Traps in 0.15 μm^2 MOSFETs Using Random Telegraph Signals," Microelectronics Reliability, vol. 40, pp. 1875-1881, 2000.

[4] E. Simoen, C. Claeys, "Random Telegraph Signal: A Local Probe for Single Point Defect Studies in Solid-State Devices," Material Science and Engineering, vol. B91, no. 92, pp. 136-143, 2002.

4 Deep-submicron MOSFET RTS Noise Model

The foundations of random telegraph signal in MOSFETs result from the non-idealities that are present due to process variations and fundamental physical phenomena. Process variations are those that result from the conditions of the processing of the device and no two processes are alike. For MOSFETs, process variations typically are some sort of non-uniformity either within the particular devices or across the wafer. Non-uniform gate oxide thickness, gate size, and dopant variation are prime examples of physical device properties that can introduce variation from device-to-device and locally within a device [1]. Physical phenomena are more elusive and often times difficult to characterize. In this case the physical process that is of most interest is the carrier trapping sites at the interface and deeper into the gate oxide. These carrier trapping sites will capture transiting carriers from the channel and hold the carrier for a time characteristic of the trap energy and trap depth into the gate oxide. A second significant physical phenomenon is that of the variation of the implanted dopant species. This may not appear at first to be physical phenomena, but aside from variation caused by the implant tool itself, the variation of the number of dopant atoms follows a Gaussian distribution and accounts for 60% of the variation found in small area MOSFET devices [1, 2]. The RTS model demonstrated here is the result of the fundamental

physical mechanisms of oxide trap interaction with the channel carriers and the discrete random nature of the implanted dopant atoms.

4.1 Random Dopants

Charge in the MOS system determines the surface potential and the conductivity of the device. Of these charges there are fixed and mobile charges in the oxide as well as traps in the oxide which are capable of the capture and emission of carriers. Process technology has matured to the point where the charge and defects in the oxide are to the point where only one or a few traps are active and capable of trapping charge from the channel. Early on before deep submicron devices became commonplace the discrete dopants in the channel were theorized as being a source of high variability in the MOSFET device [3].

The charge in the bulk of the device from doping of the substrate is a major contributor to determining the conductivity of the device. The bulk charge is a contributor to determining the surface potential of the device. Surface potential in turn defines the conductivity of the device. Equations 5.1 and 4.2 show the relationship between the surface potential and the conductivity of the sample [4, 5]:

$$\sigma = qn\mu \tag{4.1}$$

$$n = n_i e^{(q\varphi_s/kT)} \tag{4.2}$$

One of the most important steps in the fabrication of MOS devices is in the introduction of dopant atoms into the substrate. For this discussion Silicon will be assumed as the substrate. To introduce a dopant into the substrate requires that the dopant atoms be physically forced under the surface of the material. This is accomplished in three ways. One, the dopants are introduced during the formation of the single crystal ingot this is a standard technique for doping the starting substrate. Two, the dopants are introduced using a diffusion process by which the dopants are evaporated onto the surface then driven into the Si by high temperature. Third, modern process technology regularly employs an ion implanter to accelerate and forcefully drive the dopant atoms to required depths into the substrate. This step is followed by a high temperature step for activation of the dopant species. The implantation method is the most widely used method for introducing dopant atoms into Silicon in modern process technology as it allows precise placement of atoms at required depths for device performance optimization.

The impurities in the depletion region of the MOSFET play an integral role in determining the threshold voltage of a MOSFET. This is seen in the following equation [3]:

$$V_T = V_{FB} + 2\phi_B + \frac{Q_B}{C_{OX}} \quad (V) \tag{4.3}$$

where V_{FB} is the flat-band voltage, ϕ_B is the potential difference between the intrinsic and Fermi level in the bulk, Q_B is the bulk charge in the depletion region in coulombs, and C_{ox} is the oxide capacitance given as $\kappa_{ox}\epsilon_0 A/t_{ox}$. This relationship only takes into account the bulk (average) numbers of the doping concentration under the gate. It was experimentally confirmed that the dopant number variation can be described as a Gaussian random variable when a large enough number of devices are taken into account. The deviation in the dopant number from the intended doping concentration has been experimentally confirmed, see Figure 4.1. This variation in the dopant number from the average is on the order of $\sqrt{\bar{n}_a}$ where $\bar{n}_a$ is given as $\bar{N}_A W_d W_{eff} L_{eff}$ where $\bar{N}_A$ the average dopant concentration is, W_d the depletion width, W_{eff} and L_{eff} the effective device width and length.

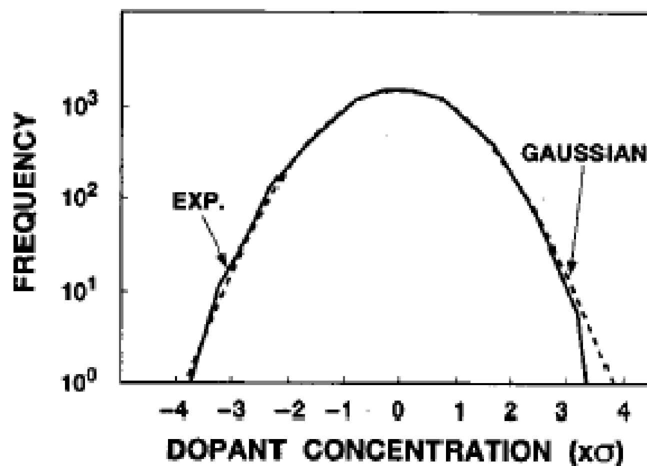

Figure 4.1 Channel dopant distribution from 8k-MOSFET array. Shows fit to Gaussian distribution for average N_a of 7.1 X 10^{16} cm^{-3} at 0 and standard deviation of 1.7 X 10^{15} cm^{-3} [2].

The electric field due to dopants in the channel affects the state of the surface potential. This bulk charge, as has been shown in (4.3), determines the threshold voltage and the conductivity of the channel for a given gate voltage. In deep-submicron MOSFETs the problem lies when the number of dopants near the surface in the channel become very small (< 100 atoms) and so the variation in the number the dopants in the device fluctuates with the square root of the number from device-to-device. This causes V_T variations and the standard deviation is described by [6]:

$$\sigma_{V_T} = \left(\frac{\sqrt[4]{4q^3\varepsilon_{Si}}}{2}\right)\frac{T_{ox}}{\varepsilon_{ox}}\frac{\sqrt[4]{N}}{\sqrt{W_{eff}L_{eff}}} \tag{4.4}$$

Simulations have shown that the dopants within 1 nm of the surface play the most critical role in determining the V_T variation of the MOSFET [7, 8]. It is within this region that the dopants contribute roughly 50% of the V_T variation because the atoms create the largest perturbation of the surface potential resulting in regions of high and low threshold voltages. The dopant also has a lateral field which extends in the direction parallel to the Si/SiO_2 interface. This is schematically shown in Figure 4.2.

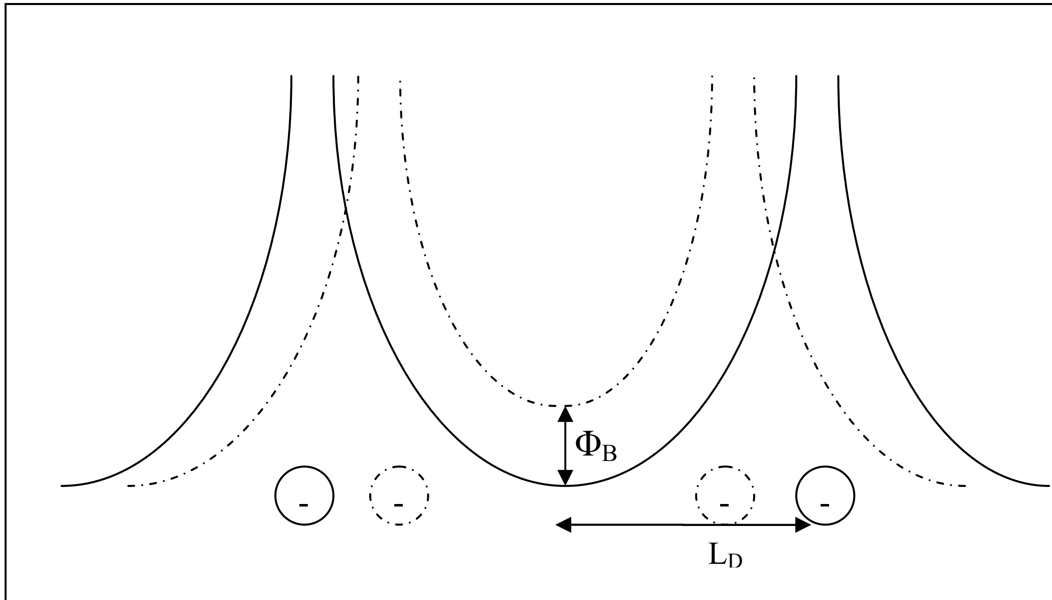

Figure 4.2 Schematic of dopant field effects. Demonstrates that as dopants are closer together this presents an increased barrier, ΦB, to electrons.

This problem was solved in [7] and the correlation length is of the form:

$$L_D^2 = \frac{2}{9}\frac{\kappa_{ox}d + \kappa_{sc}w}{\bar{\kappa}(q_s + Q_s)} + \frac{2w^2}{5} \quad (cm) \tag{4.5}$$

where Q_s the geometrical screening wave vector is defined as:

$$Q_s = \frac{\kappa_{ox}/d + \kappa_{sc}/w}{\kappa_{ox} + \kappa_{sc}} = \frac{C_{ox} + C_{sc}}{2\epsilon_0\bar{k}} \tag{4.5.1}$$

and q_s the inversion charge screening wave vector

$$q_s = (q^2/2\epsilon_0 k)(N_i/2k_B T) \quad (4.5.2)$$

where d is the oxide thickness in cm, w the depletion width in cm, κ_{ox} the dielectric constant of the oxide, κ_{sc} the dielectric constant of the semiconductor, and $\bar{\kappa}$ is the average dielectric constant, C_{ox} the oxide capacitance in Farads, C_{sc} the depletion capacitance in Farads.

This discussion on the aspects of random dopants will be applied to the compact model to estimate the effects of the random dopants and oxide traps on the RTS noise in deep-submicron devices. 3D simulation studies have shown that the random placements of dopants have the effect of causing large changes in the drain current due to the trapping of charge in low V_T regions [8]. These low V_T regions are those where there is a lower dopant concentration than the surroundings such that there is more inversion charge to be effected by the trapped charge.

4.2 MOSFET Two-State Random Fluctuation Model

The behavior of any random telegraph signal can be modeled in its most basic form as a two-state random fluctuation. This model was developed in the 1950's before researchers could measure a discrete trapped charge as we can today in sub-micron MOSFETs [3]. It was hypothesized that the current dependent noise in MOS devices was due to the interaction of the charge with traps. This model lays the ground work for the development of the sub-micron MOSFET RTS Noise model.

A two-state random fluctuation has been modeled by Machlup as an uncorrelated random process [4]. This model was developed considering only a single trap where the trap dynamics are not dependent on whether or not other traps are emptied or filled. In the case of MOSFET RTS model the above base model by Machlup serves as a template for MOSFET specific and trap specific data. Based on the previous discussion on the source of random potential the compact model is developed starting with the basic equation for a single RTS [5, 6]:

$$S_I = \frac{4(\Delta I_{DS})^2}{(\bar{\tau}_e + \bar{\tau}_c)[(1/\bar{\tau}_e + 1/\bar{\tau}_c)^2 + (2\pi f)^2]} \qquad (A^2/Hz) \tag{4.6}$$

There are two variables in (4.6) that need to be addressed and will be considered separately in the following sections. The first variable, ΔI_{DS}, is the drain current fluctuation amplitude. ΔI_{DS} is a measure of how effectively the trapped charge modulates the drain current. Secondly, the trap time constants consist of the ratio, β, and the corner frequency, ω_c. These parameters capture the on-off behavior of the trap which determines where the corner frequency happens.

4.3 Percolation Current Modulation

The drain current modulation, ΔI_{DS}, takes into account the existence of percolation currents and the geometrical positioning of the trap over the current

filament. 3D simulations of discrete dopants have demonstrated that the surface potential of the MOSFET containing ionized dopant atoms near the surface creates

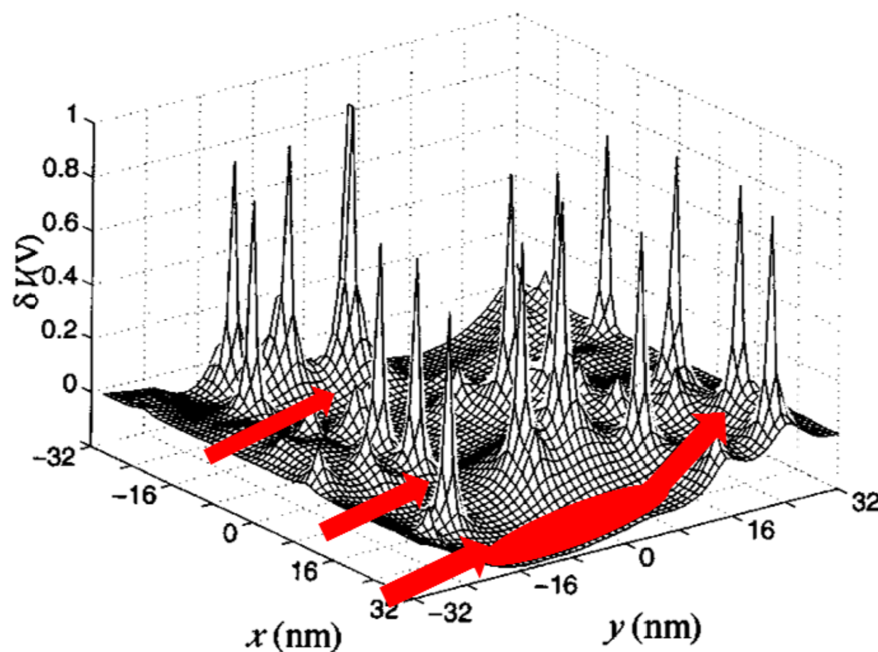

Figure 4.3 Surface potential simulation of nano-scale MOSFET [7].

peak and valleys of high and low potential presenting barriers to carriers at random positions in the channel depending on the particular arrangement of the dopant atoms. Figure 4.3 demonstrates this “potential roughness” or localized variation due to random dopant positioning. As can be seen from Figure 4.3 there are localized positions where charge can pool and flow in between the potential peaks. During the course of this research a simple atomistic potential simulator was created using Matlab and PSPICE. Matlab was used to create the netlist file which was then

simulated using the PSPICE simulator. The result is a similar view of the potential landscape as demonstrated by other groups [7] and as seen in the previous Figure 4.3. Below in Figure 4.4, is a potential simulation of 10 dopant atoms and the resulting potential profile of this fixed charge at and near the oxide interface.

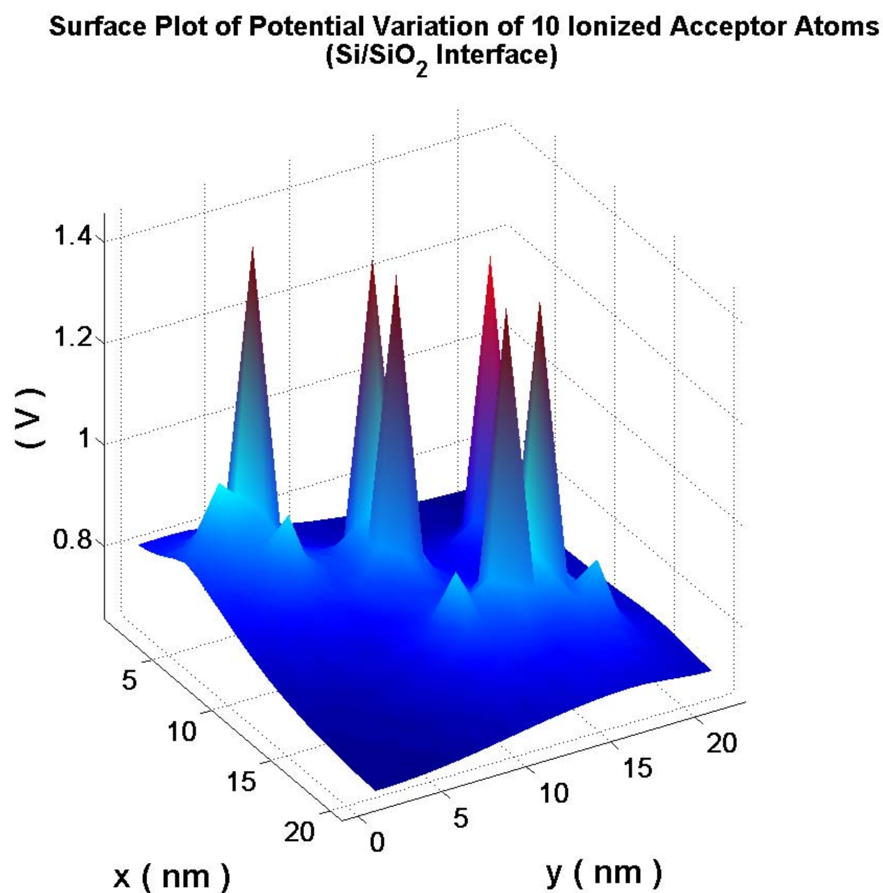

Figure 4.4 Simple potential simulator result for 10 discrete dopant atoms at the Si/SiO2 interface

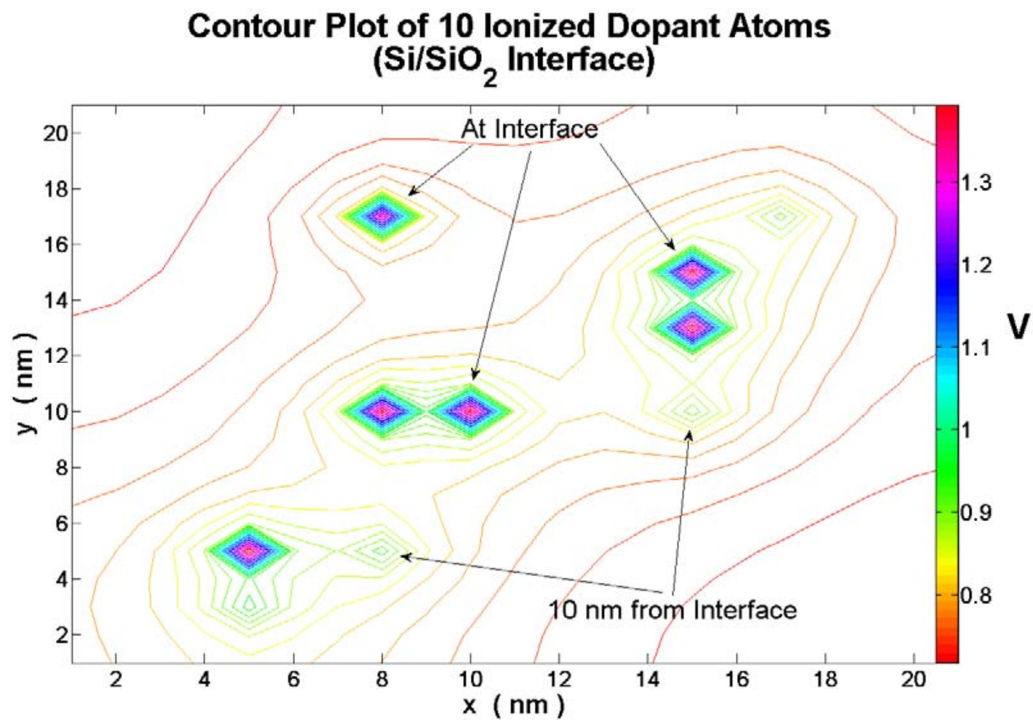

Figure 4.5 Contour map of Figure 4.4 through a slice at the interface

The contour map of Figure 4.5 shows that the dopant electric field is stongly reduced by those dopants deeper into the Silicon or away from the Si/SiO2 interface. This result is in accordance with findings in [7,8].

In this model an ideal arrangement of dopant atoms is assumed as seen in Figure 4.5. From Figure 4.5 the current flows in strips between the parallel arrangements of the impurity atoms in the channel. Based on this model the drain current is made up of a number of percolation channels.

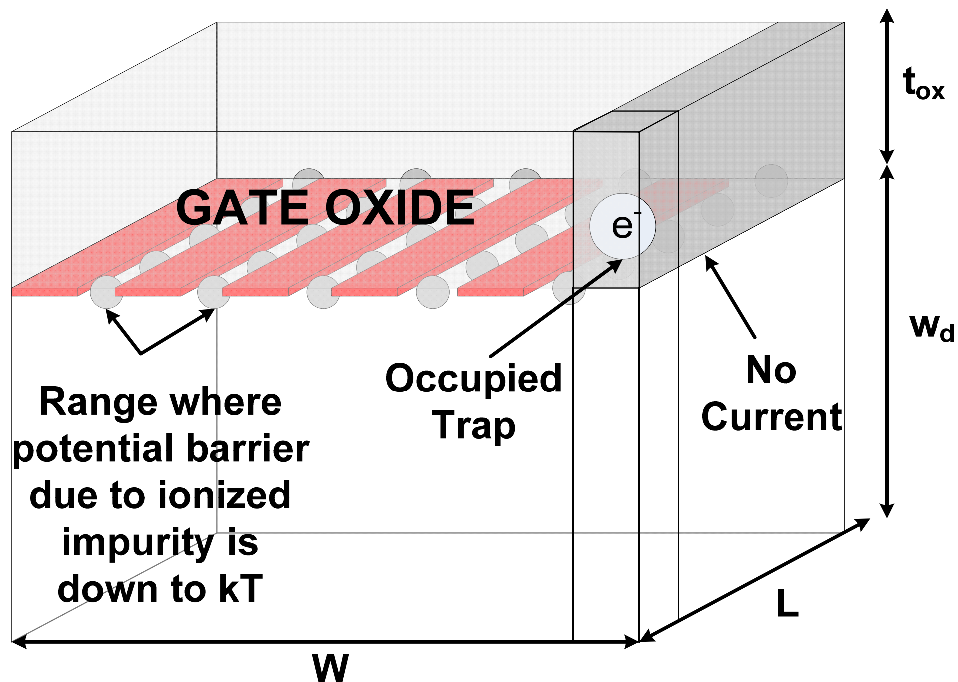

Figure 4.5 3-D pictorial view of perfect dopant arrangement and percolation currents

The modulation of the drain current is given as:

$$\Delta I_{DS} = \frac{I_{DS}}{N_d}\eta \quad (A) \tag{4.7}$$

$$N_d = \sqrt{N_D W L w_d} \tag{4.8}$$

where N_D is the average number of dopants atoms per cm^3, W and L the length and width of the device. N_d is the average number of dopant atoms along the source

within 1nm of the surface, w_d. As was discussed previously, 1 nm is chosen as this has been shown through rigorous simulation to be the distance that represents the majority of the surface potential fluctuation.

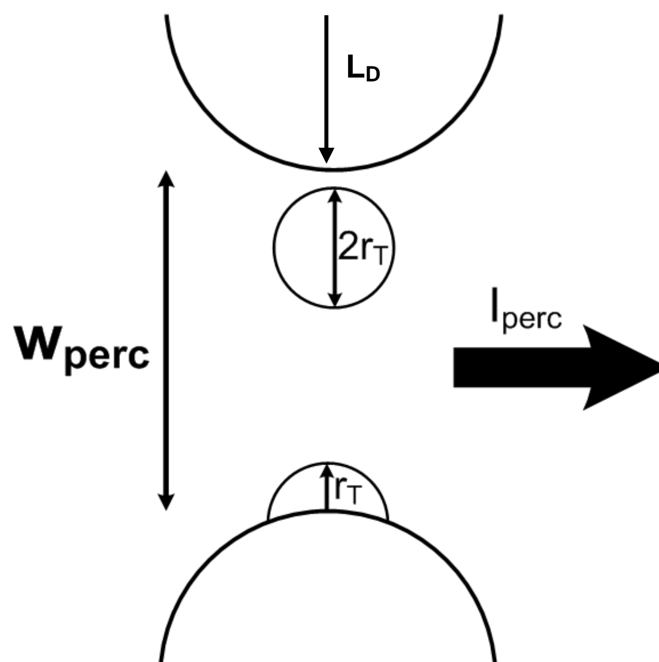

Figure 4.6 2-D schematic of single percolation path

The η term captures the fractional change in the percolation current due to the effect of the coulomb blockade on the underlying channel filament and the bias conditions for gate/substrate image charge. From Figure 4.6 the fractional change in the percolation current can be written as:

$$\eta = \frac{2\alpha r_T}{w_{perc}} \tag{4.9}$$

where r_T is the effective trap radius, w_{perc} is the width of an individual percolation channel, and α is how well the trap is centered over the percolation channel width. With α=1 the situation is as seen in the solid circle of radius, r_T, in Figure 4.6, and α < 1 is shown as the broken circle. A basic equation for r_T from (4.9) is estimated by finding the distance where the interaction energy of the trapped charge is down to kT [7]:

$$r_T = \frac{1}{\frac{4\pi\varepsilon_s kT}{2q^2} + \frac{qQ_i}{2\sqrt{2}\varepsilon_s kT}} \quad (cm) \tag{4.10}$$

The first term in the denominator describes the length scale where the potential due to a separation of charge in a dielectric medium is down to a kT. The second term in the denominator is the result of inversion charge screening. The effect of carrier screening is brought into the picture as an additional term which effectively reduces the trapped charge interaction length due to carrier screening as the channel carriers, Q_i, increases. The value of r_T is the point is where the field from the trapped charge has virtually no effect on the channel carrier concentration.

The average width of the percolation channel can be found using the following equation and the dopant field length (4.5) and not considering percolation channels along the edge of the device:

$$w_{perc} = \frac{2N_d L_D - W}{N_d - 1} \quad (cm) \tag{4.11}$$

Discussed next is the influence of the trap radius and the radius due to ionized acceptor atoms. Figure 4.6 shows pictorially how the percolation widths are affected by the bias conditions. Increasing the gate voltage increases the channel carriers which screens the field due to the ionized acceptors, as seen from Figure 4.7.

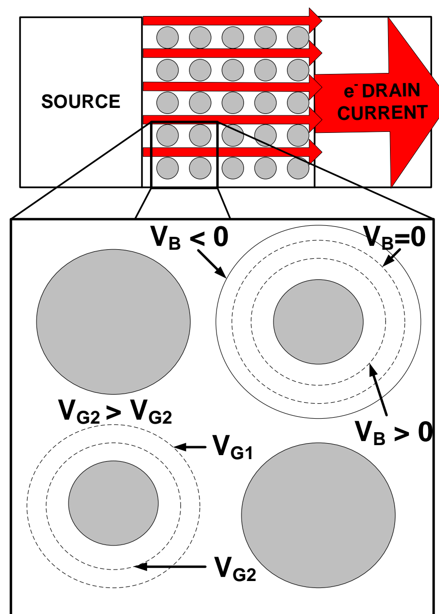

Figure 4.7 Bias influences on dopant field

On the other hand, increasing the substrate bias shrinks the depletion region and the ionized dopants will have increased coupling to the edge of the depletion region reducing the effective radius at the interface and hence widening the percolation channels and reducing the effect of the trapped charge on the overall current flow. Experimental results will be shown in the next section which brings further evidence that this effect will also cause a decrease in the measured low-frequency noise of the device.

4.4 Trap Time Constants

The trap time constants are related to the depth in the oxide, the carrier concentration, and the field across the oxide. The basic equation that relates the capture and emission times to physical quantities is [8, 9]:

$$\bar{\tau}_c = \bar{\tau}_e e^{\left(\frac{E_T - E_F}{kT}\right)} \tag{4.12}$$

$E_T - E_F$ is the difference between the quasi-Fermi level at the interface and the trap energy in the oxide. Equation 4.11 can be expanded to include bias conditions as [8]:

$$\beta(V_{gs}) = \frac{\bar{\tau}_c}{\bar{\tau}_e} = e^{-1/kT\left(K + q\psi_s + q\frac{x_T}{T_{ox}}(V_{gs} - V_{FB} - \psi_s)\right)} \tag{4.13}$$

K is a constant and the other terms retain the usual meaning. Equation 4.12 can be used to find the ratio factor, β, and the corner frequency, ω_c, of the traps for use in (4.1).

4.5 Model Predictions

The proposed model is implemented in Matlab for analysis of the validity of the model. Figure 4.8 demonstrates the model predictions for a range of dopant values and the resulting relative drain current fluctuation, $\Delta I_{DS} / I_{DS}$ for a fixed current of 1μA.

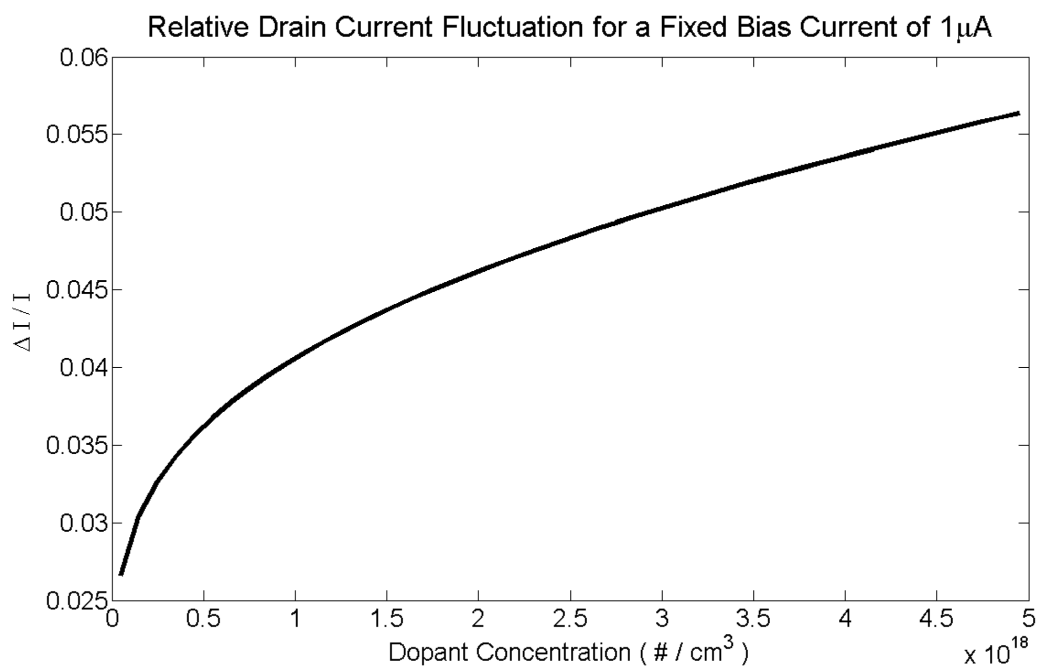

Figure 4.8 Relative drain current fluctuation versus dopant concentration

Figure 4.8 predicts that as the dopant concentration is reduced there is an accompanying reduction in the drain current noise fluctuation. This concept serves as the basis for work in reduction of the threshold voltage and the population of the dopant atoms in the channel.

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5 Low-Frequency Noise Reduction Techniques in MOSFETs

How to controllably affect the noise of a device in a predictable manner is an important tool in improving the noise performance of any electronic device, circuit, and system. Since MOSFETs are major constituents of any modern electronic system it is highly beneficial to have techniques for reducing the noise of these devices. One such technique is through the application of switched bias. By cycling the MOSFET from accumulation to inversion the noise of the device has been shown to reduce [1, 2]. The noise reduction is a result of the inability of some traps that do not capture immediately, but instead take some time to reach steady state [3-8]. Also, measurements performed on large switched bias MOSFETs show a long-term transient [9-12]. These long term transients demonstrate that there exist traps in the oxide with very long time-to-capture. This is one method that is based on the interruption of the trapping/detrapping behavior; however, more applicable to the model presented in this research is the reduction of noise through the manipulation of the ionized dopant electric field variation on the surface potential of the MOSFET. It is the potential field variation and resulting percolation current channels which are the culprit behind the large drain current modulations. When the current channels in the device are made wider the influence of the trapped charge is lessened due to the decrease in the charge density in the vicinity of the field setup by the trapped charge. Two methods for reducing the potential variation in the

device are one, through the application of a forward substrate bias and, two through the engineering of the substrate dopant.

5.1 Substrate Bias

Previous works have demonstrated that a reduction in low-frequency noise is possible through the application of a forward substrate bias [13,14]. Forward substrate bias also has the added benefit of decreasing the V_T which has advantages in low-power design. In addition, measurements on RTS parameters have also shown a reduction in the drain current modulation, ΔI_{DS}, as a result of the forward bias of the substrate source junction and an increase in ΔI_{DS} when the junction is reverse biased [14]. These observations are also predicted in terms of the percolation model presented here and measurements on submicron devices. For an nMOSFET this means that a positive voltage is applied to the substrate or p-well of the transistor and a negative voltage in the case of a pMOSFET device. Here it is proposed that through the application of a source/body forward bias the reduction in the low-frequency noise is a result of the decrease in the RTS component of the noise in deep-submicron MOSFETs. This reduction comes as a result of the decrease in the filament current flow or a smoothing of the surface potential in the channel where the ionized impurities couple to the substrate depletion edge more effectively as opposed to the gate.

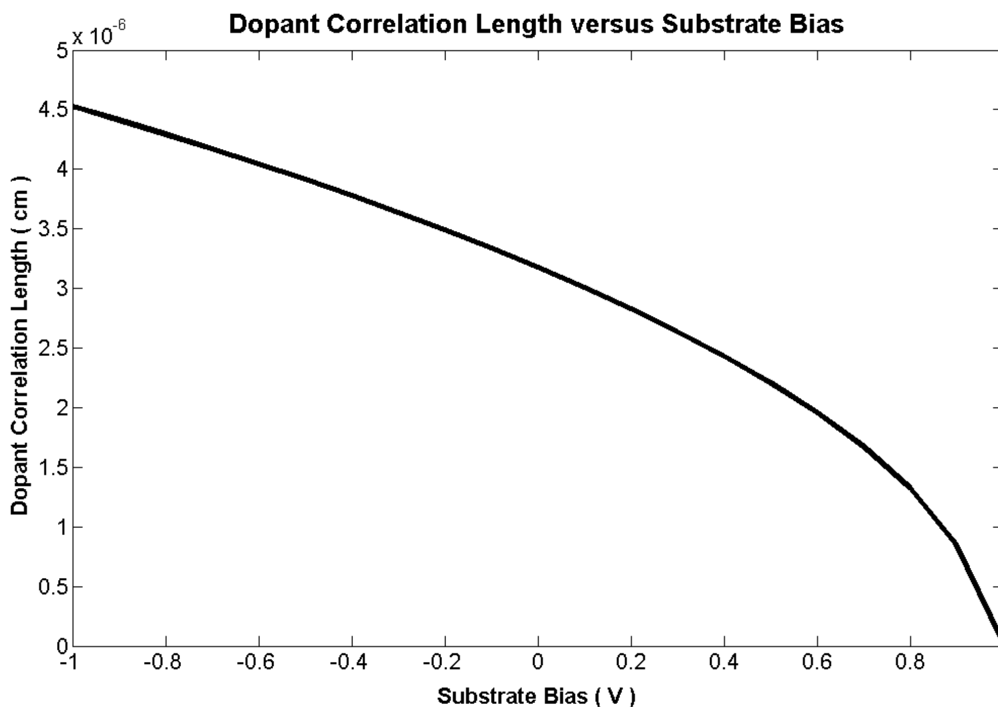

Figure 5.1 Substrate bias versus the dopant potential correlation length for an n-channel MOSFET.

This coupling to the depletion edge reduces the field imposed at the interface and in effect widens the individual current paths decreasing the local charge density and lessening the effect trapped charge has on the overall current. Additionally, with the decrease in the local charge density there is an additional reduction in the trapping activity since carrier trapping rate, τ_c, is proportional to the inverse of the local charge density, n_s.

Measurements have been performed on a number of sub-micron MOSFET transistors. For the noisiest of devices there is a strong reduction in the noise with application of a forward substrate bias. This reduction based on the measurements is due to the decrease in the measure drain current modulation, ΔI_{DS}, and a reduction in the trapping/detrapping activity. This effect is demonstrated in measurements from several sub-micron MOSFETs with W and L of 0.36μm. Figures 5.1 – 5.5 show the noise power at 100Hz versus the substrate bias. In almost every measurement the noise has been reduced. In the case where the noise has not reduced, Figures 5.3and 5.5, the noise is still lower than the noisiest of the devices. What is important about this data is that the devices with the highest noise see the greatest improvement at 100 Hz, see Figures 5.2 and 5.4.

The improvement in the noise with substrate bias is a result of the widening of the percolation channels in the device. In almost all of the measurements it can be seen that the noise actually has a small peak before it falls off. In other cases, Figure 5.3 and 5.6 the noise actually begins to increase. The cases where the noise has peaks are examples where trapping has been activated in a newly formed percolation channel. This new channel has a higher V_T than the rest of the channel and as a result of the decrease in the V_T due to substrate bias this new channel is carrying current in the vicinity of an oxide trap. This channel is also much smaller than the main current carrying path. In this path the current is fully switched on and off by the Coulombic interaction with the trapped charge. Assuming that the current

is effectively completely blocked during the capture of charge, the current level of these atomic-scale percolation paths can be deduced directly from the measured noise fluctuation. For instance, the peak at 0.1V in Figure 5.4 in the saturation current shows

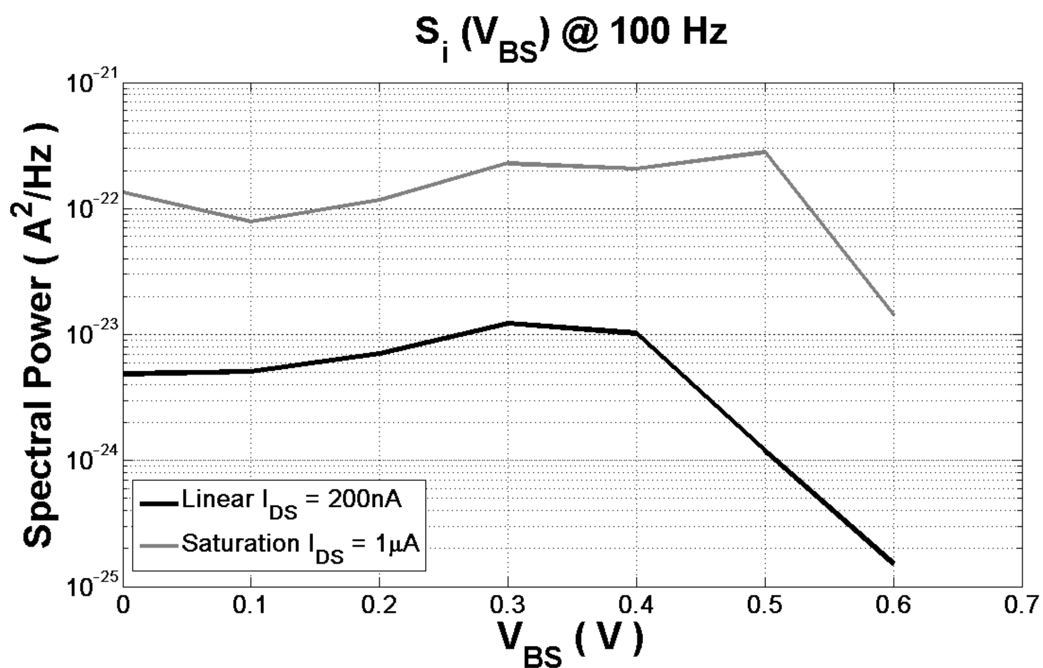

Figure 5.2 Device 4 Noise versus Substrate Bias

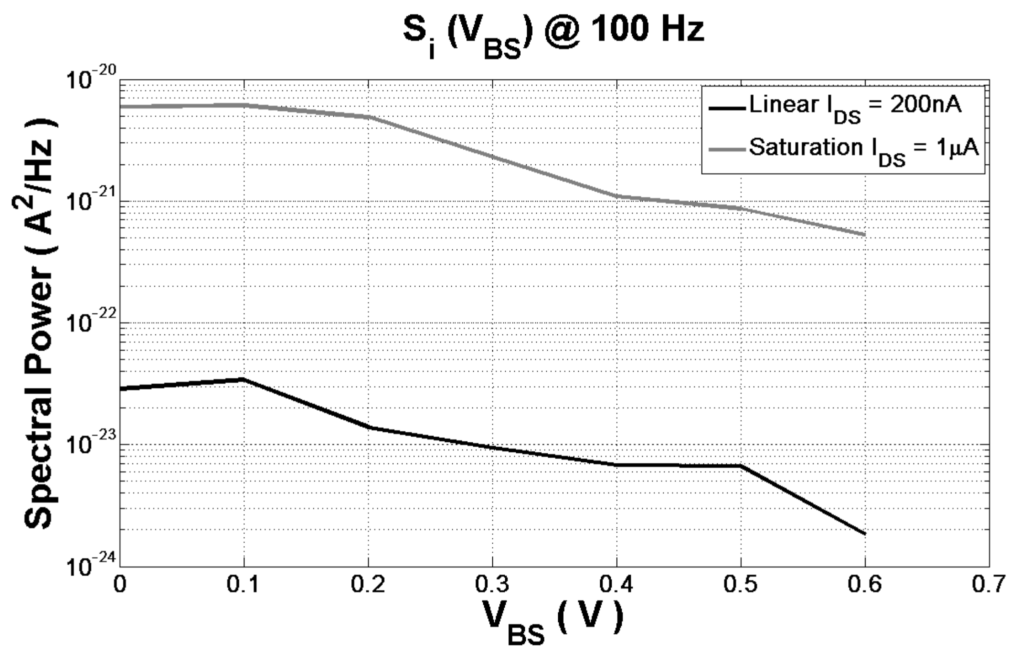

Figure 5.3 Device 8 Noise versus Substrate Bias

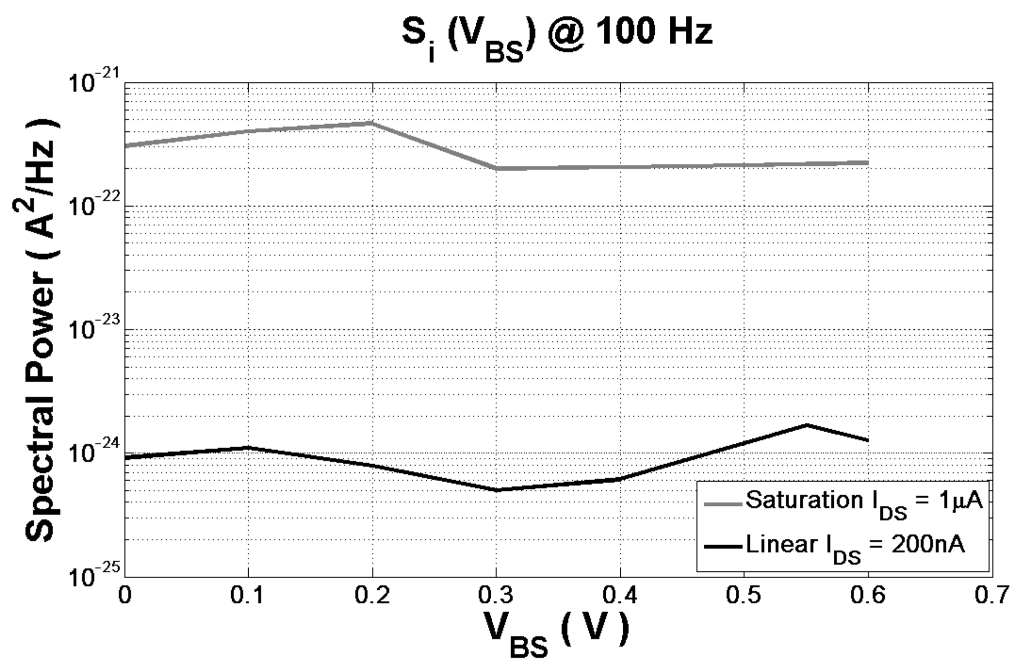

Figure 5.4 Device 11 Noise versus Substrate Bias

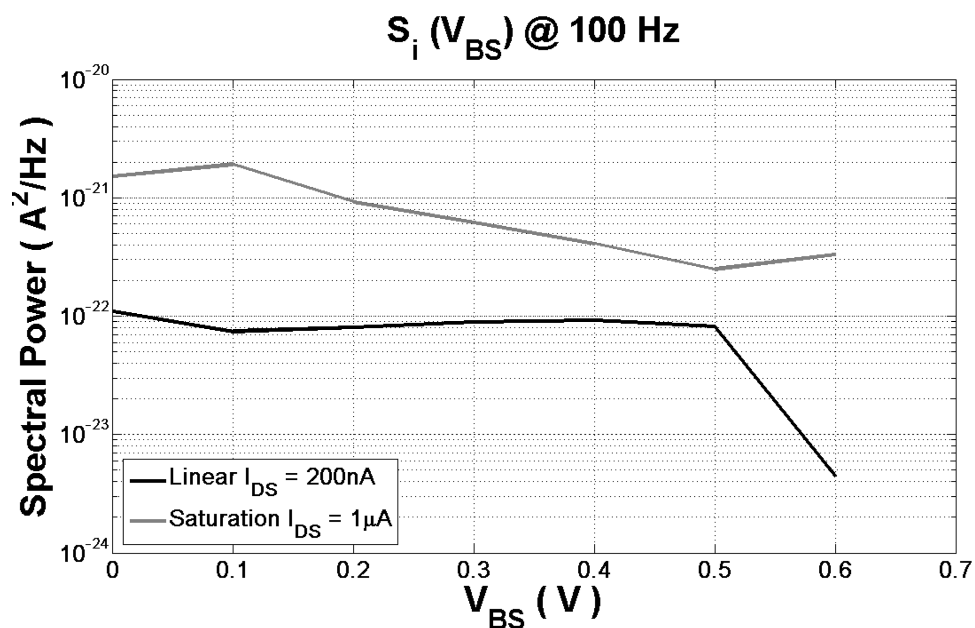

Figure 5.5 Device 14 Noise versus Substrate Bias

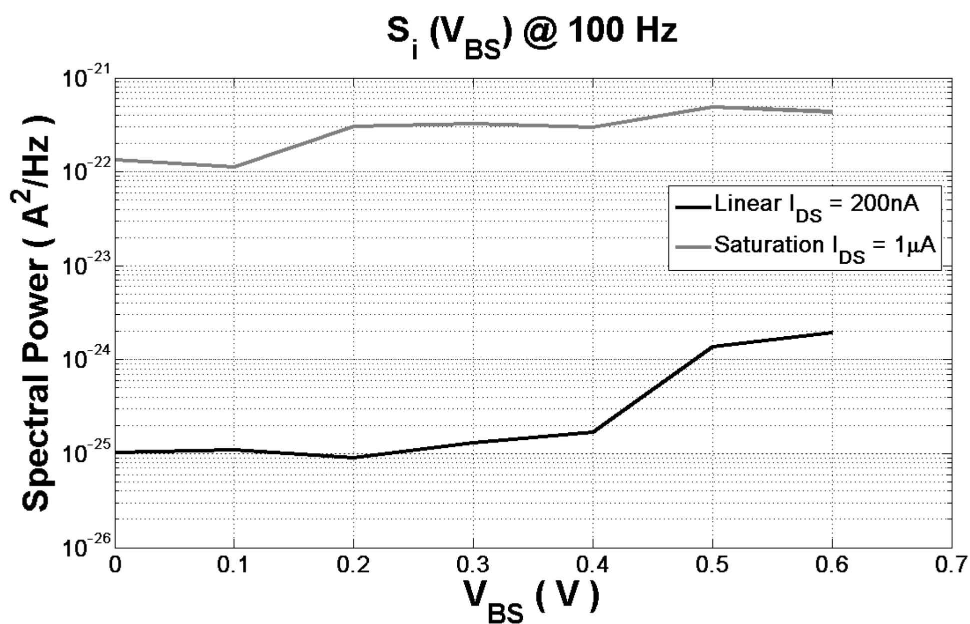

Figure 5.6 Device 17 Noise versus Substrate Bias

5.2 Channel Engineering

The model presented in the previous section states that the surface potential variations in the channel of submicron MOSFETs determine the noise properties of the device. This is due to the presence of percolation currents as a result of the non uniform surface potential due to the field of the ionized dopant atoms in the channel. Channel engineering techniques, such as ground planes behind the channel during epitaxial growth or retrograde implants, have been predicted to be useful to reduce V_T variation and increase device matching specifically targeted at reducing surface potential variation while minimizing short-channel effects [16, 17]. Demonstrated in this work is the lowering of the V_T and the substantially reduction in RTS and 1/*f* noise of the MOSFET device. There is no reference to this behavior in the literature and this appears to be the first reporting of such a noise lowering mechanism. The reason is that with reduced doping in the channel there is in fact less spatial variation in the dopant distribution, hence, a widening in the percolating flow of the current through the device. Less spatial variation is simply due to the fact that there are fewer dopant atoms and as a result the space between atoms is on average much wider than in a more highly doped device of identical dimensions. In essence the device behaves more like an ideal transistor with uniform current flow under the gate.

Simulation on nano-scale MOSFETs have shown that V_T variation can be reduced while maintaining device performance through engineering of a delta

doped region under the gate [16]. While this reduces V_T variations between devices this technique is also capable of reducing the surface potential variations in the channel of the device.

A practical example covered in more detail in section 7 shows that V_T engineering for noise can reduce the read noise of a CMOS image sensor. As shown in the power spectral plots, Figures 5.7 and 5.9, the noise is reduced by not

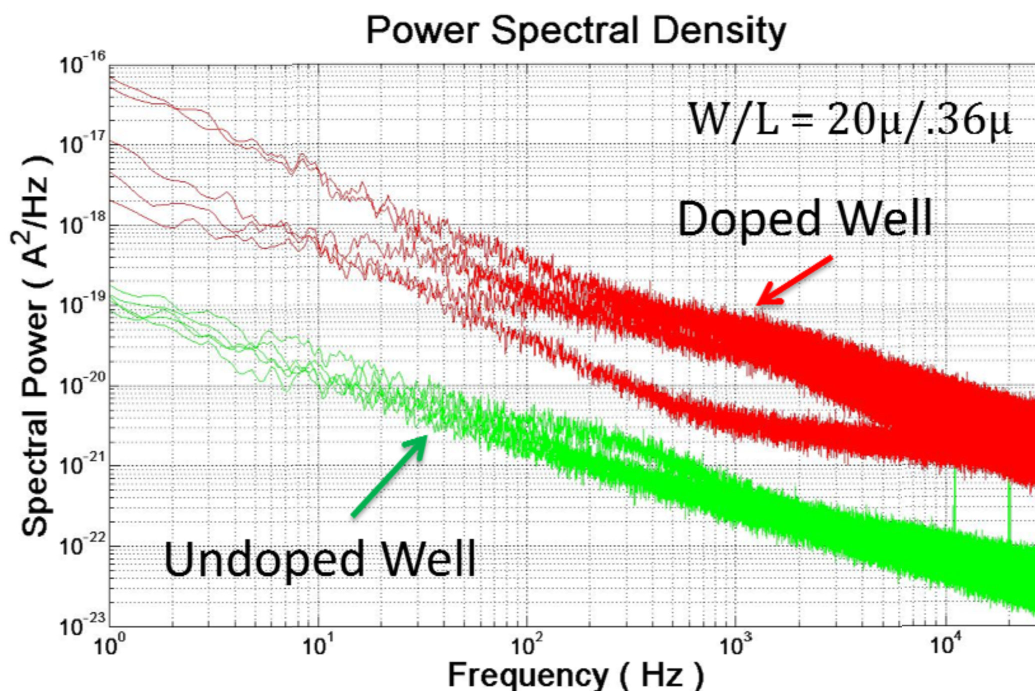

Figure 5.7 Low-Frequency Noise in a 20μm wide MOSFET

performing the p-well implant for these nMOSFETs. As shown in Figure 5.7,

each of the larger devices has seen a significant noise reduction. Also, the device to device noise variation has been reduced which is evident visually from the spectral and box plots of Figures 5.7 and 5.8.

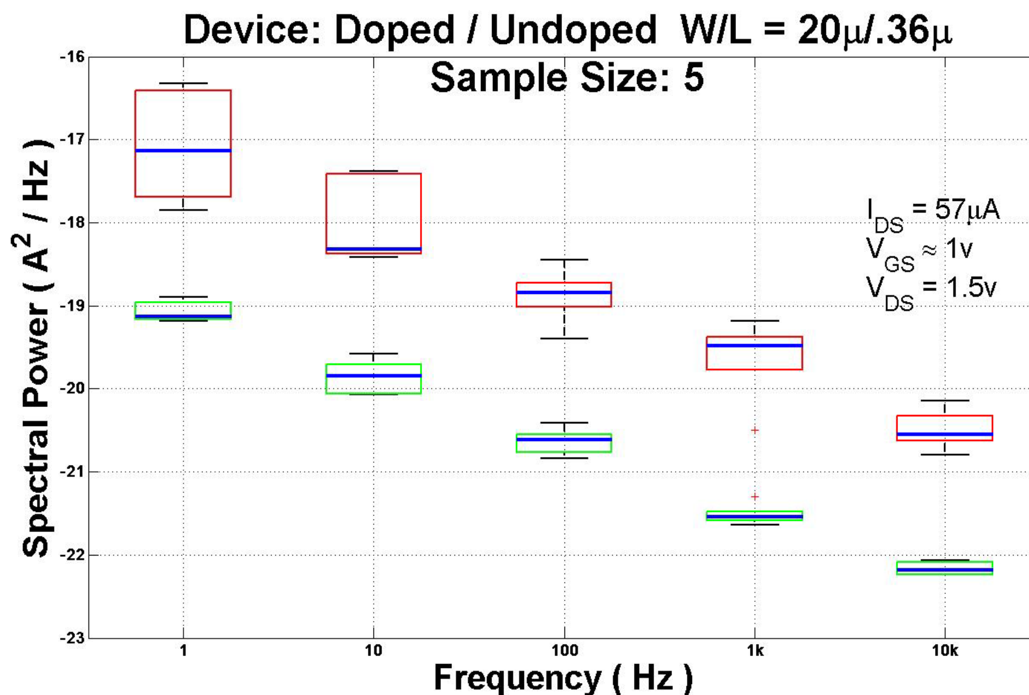

Figure 5.8 Box plot of power spectral data. Green (Light) boxes are undoped and Red (Dark) boxes are doped devices.

Looking at the average values of the box plots the noise has been reduced by substantial 20 dB across all frequencies.

In the smaller dimension devices, the noise has also been impacted positively by the lowered doping in the channel. The results are not as impressive as for the larger device; however, the average trend still holds for these MOSFETs too.

From Figure 5.9 the variation in the distribution has not been improved as was seen in the larger devices although the average has shifted down from the highly doped.

Figure 5.9 Low-frequency noise in a narrow (0.36μm) MOSFET

Again the average noise across the measurement frequencies demonstrates a significant, greater than 20 dB at 1 Hz, improvement in the noise properties between the doped and undoped device types. The box plots of Figure 5.10, on the next page, show both the average and the device variation has been improved in the lower frequencies.

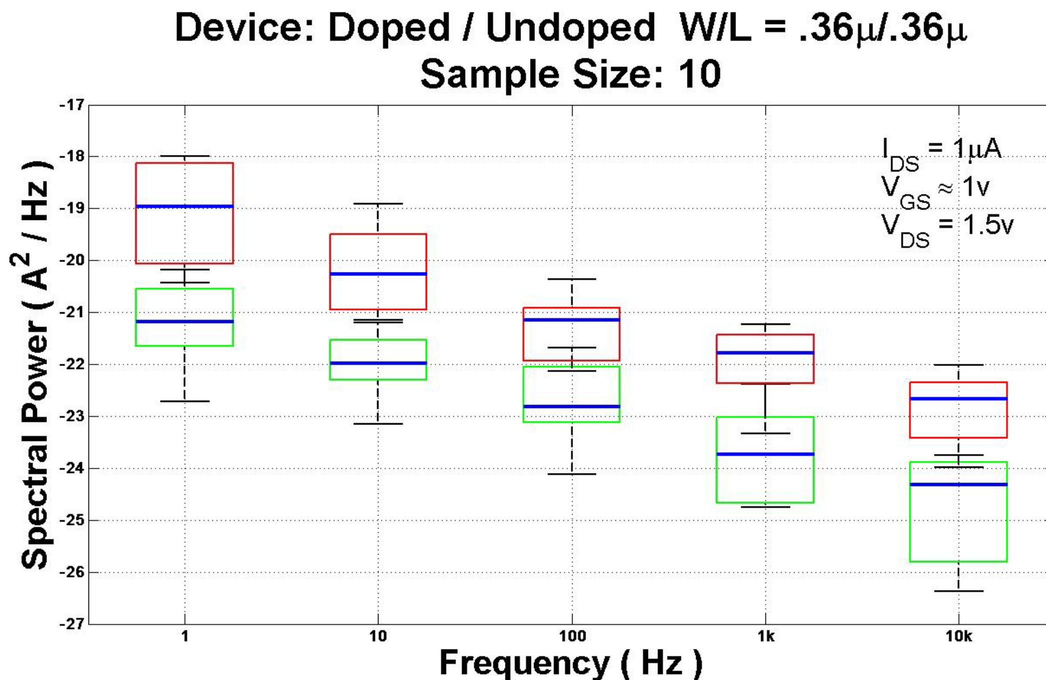

Figure 5.10 Statistics of the noise of Figure 5.8. Green (Light) boxes are undoped and Red (Dark) boxes are doped devices.

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6 Case Study: Noise Reduction in a CMOS Image Sensor

This case study is an investigation of the individual transistor and pixel-level noise impacts of various processes conditions applied to the source follower (SF) of a 4T 2.2μm 2MP CMOS image sensor (CIS). First, individual SF transistor noise was characterized through measurements of the noise power spectrum of the sampled DC current with the transistor biased at typical operating currents using the noise test setup presented in Section 4. Secondly, a series of splits were run to verify the impact of the measurement observations on CIS noise parameters namely the temporal noise of the imager. The process splits came as a result of the model and understanding of the noise source developed in Section 5 and measurements which confirmed the predictions provided by the model. Ultimately, it was discovered that the temporal noise performance is dramatically improved using the same bias currents, but lowering the threshold voltage of the SF device.

The CIS is named so because it makes use of standard CMOS process technology in the manufacture of the sensor and read-out electronics. This level of integration allows CIS parts to take up a much smaller footprint as compared to a CCD imager which requires several peripheral electronic devices for operation. Similar to that seen in microprocessor technology, CIS technology also drives to shrink the pixel for a number of reasons; first, increase pixel count for higher resolution imaging in the same die size; second, to decrease die size to get more die

per wafer. This device shrink has required that the transistors in the pixel also shrink in order to increase or maintain the fill factor. The fill factor is a measure pixels open photodiode area to the pitch of the pixel. As pixels get smaller it becomes difficult to design devices for low noise which require large W and L.

Techniques such as shallow-trench isolation, ion implantation, gate oxide growth are common process modules used in the creation of a CIS product just as they are in typical CMOS integrated circuit (IC) devices. The only real difference comes from the fabrication details of the image sensor array; however, this is simply a difference in the masking steps that separate the pixel-level electronics from the digital and analog processing electronics. The CIS product can be considered a mixed-signal IC because it combines analog sensing capability with digital processing electronics. Before an optical signal is transformed to its digital representation and reaches the periphery of the chip it has been amplified, digitized, and most often the digital data post-processed. With every function performed on the original optical signal an amount of noise is added to the signal which increases the uncertainty in the actual measurement.

6.1 Noise in CMOS Image Sensors

Noise sources in a CIS stem from a number of sources as shown in equation 6.1. The SNR of the image sensor can be calculated as the following:

$$SNR = \frac{i_{sig}}{\sqrt{{i_{ph}}^2 + {i_{dk}}^2 + {i_{SF}}^2 + {i_{rd}}^2}} \tag{6.1}$$

where i_{sig} is the signal amplitude, i_{ph} is the photon shot noise, i_{dk} is the dark current shot noise, i_{SF} is the source follower noise, and i_{rd} is the noise of the readout electronics. The first source of noise to consider is the photon shot noise from the incident photons. Arrival of the photons on the sensor obeys Poisson statistics where the standard deviation is equivalent to the square root of the number of photons impinging on the surface [1]. The photons are absorbed in the silicon and create electron-hole pairs that are collected by the diode. These carriers give rise to shot noise in the photodiode. The transfer gate is activated and the collected carriers flow out of the diode onto a capacitive node called the floating diffusion. The charge storage on the floating diffusion results in a fluctuation of kTC reset noise and dark current noise. The kTC noise of the floating diffusion is mostly removed through the correlated-double sampling (CDS) operation. Next the noise of the source follower is added to the signal and the signal is now driven onto the column line. From there the signal is amplified by a programmable-gain amplifier and output amplifiers where additional noise is added to the signal and finally driven off chip.

The most typical types of noise encountered in the characterization of a CIS are temporal and fixed-pattern of both row and column. Temporal noise is the

variation of the pixel or amplifier output with time. In the case of an RTS pixel, this pixel will appear to blink from a high or low value above some mean signal. Fixed-pattern noise is named so because the pixels which demonstrate large deviations from the average, either dark or bright, are in fixed locations usually along a

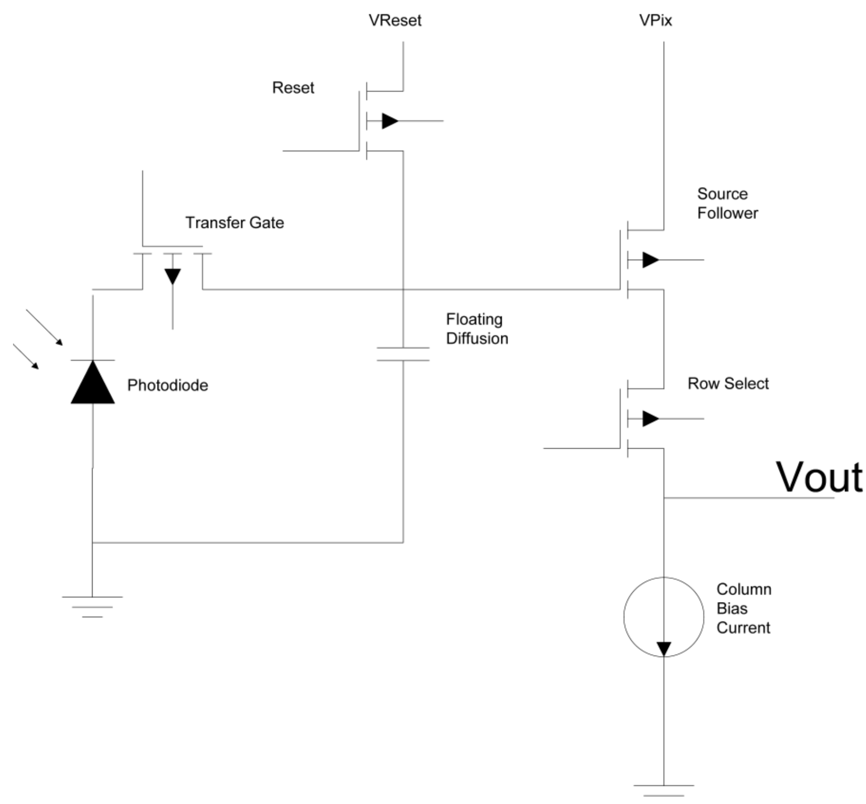

Figure 6.1 4 transistor (4T) active pixel circuit schematic

column or row, and do not change with time or exposure. The equations for calculating the noise properties of an image sensor are shown in Appendix B.

6.2 RTS Noise in CMOS Image Sensors

The low-frequency noise in the source follower of the CIS device has become a major challenge to the scaling of pixel when submicron transistors are necessary in the array [2-3]. The source follower is the device which converts the charge stored on the floating diffusion to a column output voltage. So the source follower is a major component of the signal path from diode to the column amplifiers. While the $1/f$ noise is always a concern, the deep submicron devices made today typically exhibit RTS behavior. RTS appeared as a major hurdle in CMOS image sensors at the 2.2um pixel node where it is required to have submicron transistor sizes in the pixel. Researchers have attributed RTS like pixel behavior to the reset gate as the cause, but the general consensus is that the source follower is the dominant contributor to high temporal noise [4]. The problem really arises at low-light levels where the signal coming from the photodiode is small on the order of 10 electrons [5]. At these signal levels RTS can appear as a fictitious signal since it also appears with a signal magnitudes on the order of 10 or more electrons as will be shown in the following imager RTS characterization.

Discussed and demonstrated in the following data is a noise reduction implementation in a 4T CIS through modification of the doping levels in the source follower. As noise places a fundamental limit on the performance of any image sensor understanding and optimizing the pixel readout circuitry for the lowest noise is paramount. Others have used techniques to reduce the noise of the source

follower through engineering a buried channel device and through optimization of the length and width of the transistor [6, 7].

From the model presented in this research it makes sense that a buried channel device would show a lower noise due to the fact that the carriers in the channel of the MOSFET are not confined close to the surface, but instead the current flows away from the interface and are not capable of being trapped in the gate oxide.

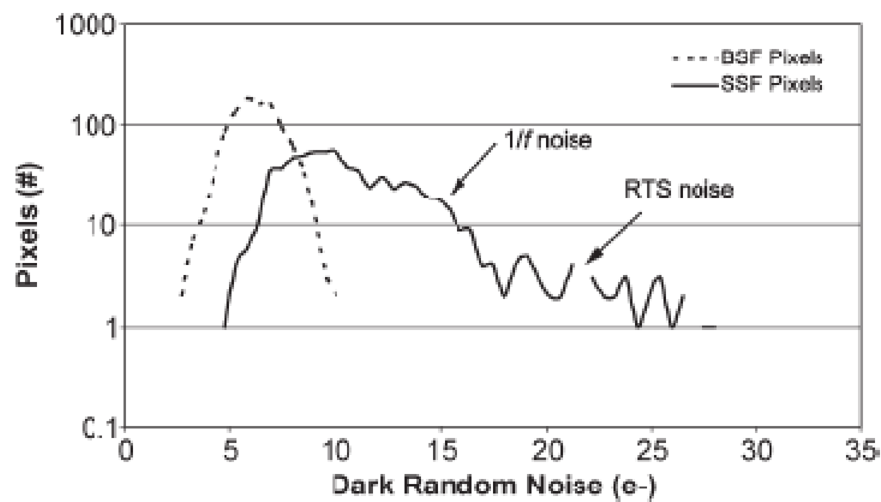

Figure 6.2 Comparison of the dark read noise of a surface SF and buried channel SF [6].

Figure 6.2 shows this improvement in the temporal noise between a surface mode device and a buried channel devices [6].

6.3 Source Follower Transistor Measurements

Test structures containing various transistor sizes and process conditions were used for characterization of the low-frequency noise. The noise test system and analysis that was used for this study is the same as described in Section 3. In short this test system consisted of a battery powered biasing testing fixture, a low-noise amplifier, and finally a 16-bit analog-to-digital converter. The sampled signal was captured by a PC through the USB port. Post-processing of the recorded noise signal was performed using time domain and frequency analysis techniques developed and run inside MATLAB software.

Each of these pixel transistor test structures were individually characterized by measuring the noise at a bias that would be typical of operation in the actual imager sensor. The bias current in this case was 1µA. Measurements of the pixel MOSFET devices highlight the primary issue of RTS noise in sub-micron MOSFETs. Primarily this noise is seen as highly variable from device to device, see Figure 6.3. These high noise levels and variability degrades the key image sensor parameters namely temporal noise. This type of noise manifests in the image as blinking pixels. Blinking pixels are those that continuously transition from light to dark from one frame to the next.

The noise PSDs of Figure 6.3 demonstrates the high variability from one device to the next from different locations on the wafer. From the plots it can be seen that the noise power at 10 Hz spans two orders of magnitude. This is the root

of the problem. Below is shown the corresponding time domain, histogram, and noise PSD of the data from a device shown in Figure 6.3.

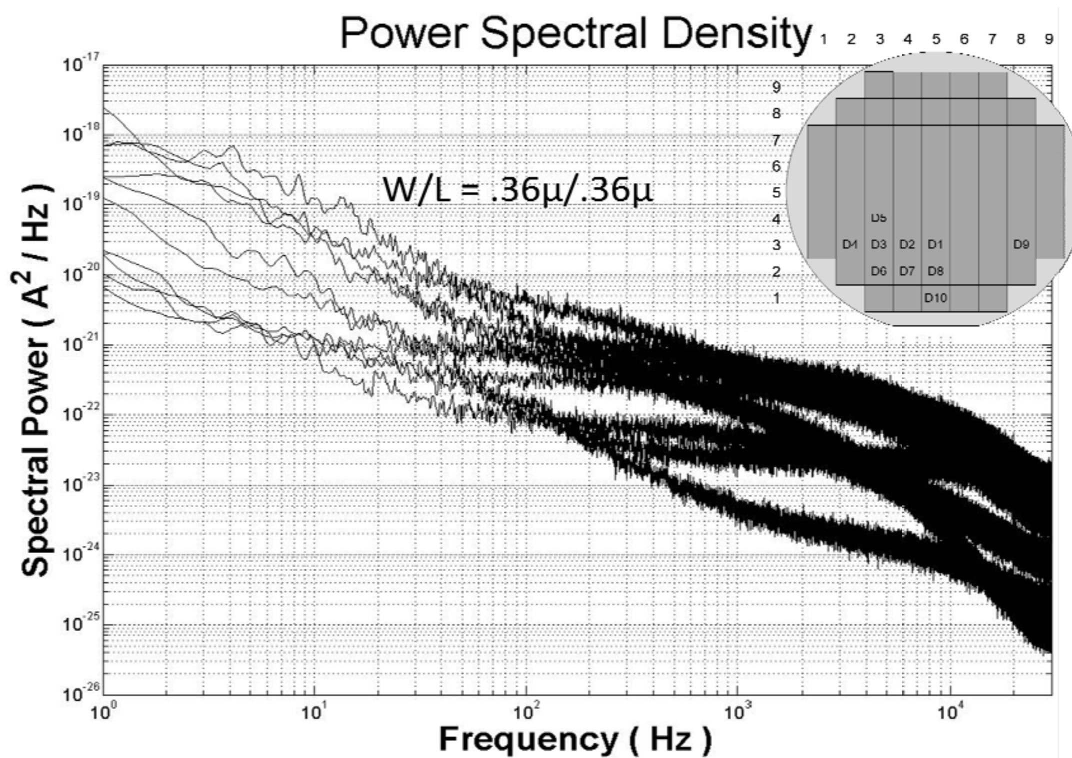

Figure 6.3 Noise spectral power plots of 10 devices taken from 10 different locations across the wafer (see inset).

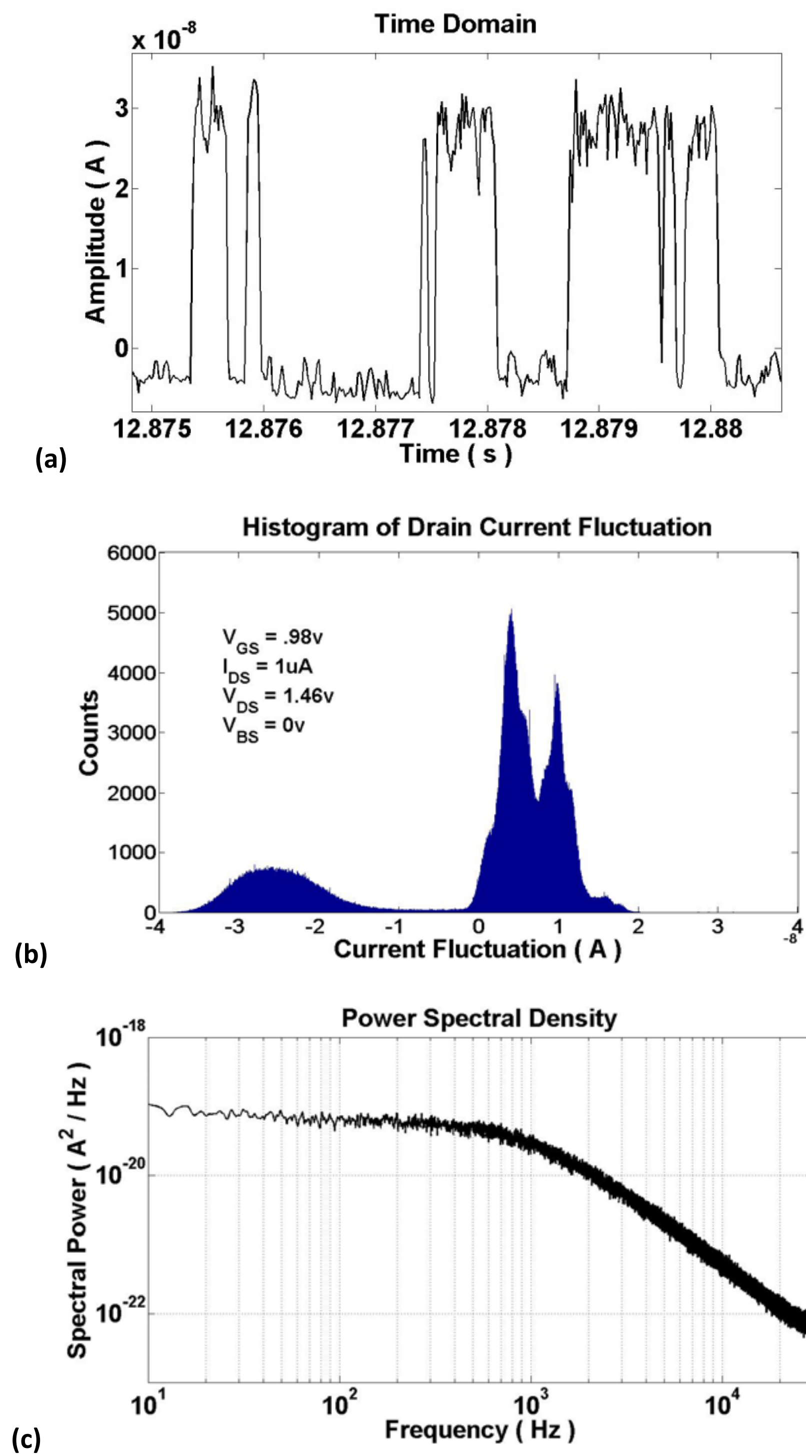

Figure 6.4 (a) Time domain RTS waveform (b) amplitude distribution (c) power spectral density of RTS signal

The measurements seen in Figure 6.4 are typical device characteristics for the noisiest of the devices that were implemented as the source follower of the pixel for the baseline process conditions. As part of the test pattern there are also devices that are considered native transistors. The native transistors had a lower threshold voltage due to the fact that they did not receive the p-well implant. This p-well

Figure 6.5 Power spectral density of sub-micron (W, L = 0.36μm) source follower transistors

implant raised the background doping of the substrate under the gate and hence the V_T. These native devices showed a significant reduction in the low-frequency noise and more importantly the absence of large RTS signals. These signals appeared to be suppressed due to the lower doping in the channel. This is in accordance with the model which suggests that a “smoothing” of the surface potential variation in the

channel region which effectively widens the percolation channels and reduces the impact that a trap can have on modulating the total current in the device.

Figures 6.5 and 6.6 demonstrate the impact that reducing the doping has on the low-frequency noise of the source follower MOSFET. The box plot shows that statistically for these samples the mean noise has been reduced across the measurement frequencies.

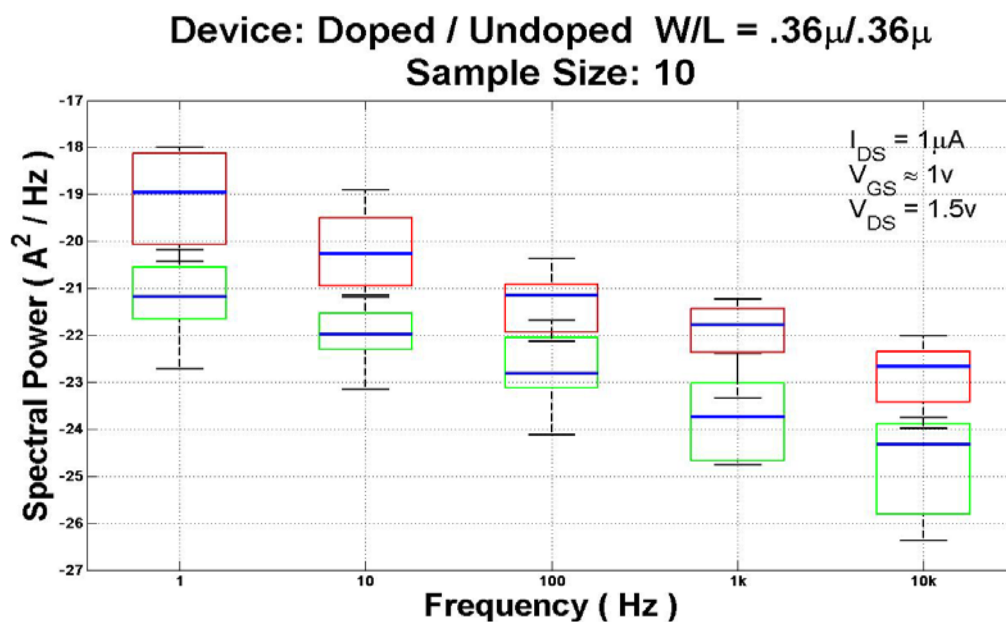

Figure 6.6 Box plots of source follower noise power spectrum plots from Figure 6.5. Red (Dark) boxes are doped devices. Green (Light) boxes are undoped “native” transistors.

6.4 Noise Reduction Process Splits

The CIS image sensors used in this study were manufactured at MagnaChip Semiconductor in Korea. The splits that were used to test the theory discussed in this work are outlined in Table 6.1, below.

Table 6.1 Split conditions for threshold voltage lowering study

SF implant	**20 keV 1.3E12 /cm^2**	**20 keV 1.0E12 /cm^2**	**20 keV 0.7E12 /cm^2**	**20 keV 0.4E12 /cm^2**	**Skip**	**20 keV 0.7E12 /cm^2**
SX implant	**30 keV 4.0E12 /cm^2**	**30 keV 3.0E12 /cm^2**	**30 keV 2.5E12 /cm^2**	**30 keV 2.0E12 /cm^2**	**Skip**	**Skip**
SF V_T	0.883V	0.807V	0.705V	0.594V	0.308V	0.707V
SX V_T	0.427V	0.453V	0.398V	0.327V	0.324V	0.717V
Splits	BL	S1	S2	S3	S4	S7

The process splits included a variation in the implant dose for the row select and source follower transistor. The source follower V_T was set between 0.883V for the baseline process conditions down to 0.308V for split 4 which did not receive the threshold implant.

6.5 Imager Temporal Noise Characterization

The experimental image sensors were characterized using a bench-top characterization setup. This characterization system consists of sensor bias circuitry, FPGA for pixel signaling, analog-to-digital converter (ADC), and a frame capture port. The sensor bias circuitry provides the necessary currents and voltages necessary for biasing the columns and internal amplifiers. The FPGA provides the pixel clocking and control signals to the chip. The ADC converts the analog output of the imager to digital for forming an image. The frame capture port receives the digital data for capture and displaying the image on the PC.

The bench characterization confirmed that the noise had been in fact reduced through the reduction of the V_T implant of the source follower transistor. This fact is in line with the individual MOSFET noise characterization data where a reduction in the noise power was observed, Figure 6.5. The details of the implant conditions and resulting V_T for the sensor is shown in Table 6.1.

Two metrics that are typically used to evaluate image sensor noise performance on a macroscopic level are the pixel temporal or read noise and the total temporal noise. The read noise of the image sensor is computed by reading the signal from each pixel of the sensor in the dark with a short integration time over a successive number of frames. Dark conditions are used so that there was no additional noise from the photon shot noise. A short integration time is used to reduce the dark current noise generated in the photodiode so that this noise source

can be neglected. Typically several hundred frames are captured for the temporal noise calculations in order to gather enough statistics from each pixel. The equation for calculating the pixel temporal noise is:

$$\sigma_{temporal}(x,y) = \left[\frac{1}{(N-1)}\sum_{n=1}^{N}(p_n(x,y) - \bar{p}(x,y))^2\right]^{1/2} \tag{6.2}$$

where $\bar{p}$ is the pixel mean, $p_n(x,y)$ is the n_{th} value of pixel x, y. N is the total number of frames. The total temporal noise is computed taking the mean value of each individual pixel temporal noise. The total temporal noise equation is:

$$\sigma_{total\ temporal} = \frac{1}{X \cdot Y}\sum_{x=1}^{X}\sum_{y=1}^{Y}\sigma_{temporal}(x,y) \tag{6.3}$$

where X and Y is the width and height of the region of interest.

The image sensor splits were characterized at the fabrication facility in Korea and again in the United States at the MagnaChip Advanced Pixel Research Center. The RTS noise of the image sensor was measured from 5 die from each of the split conditions. For the read noise of the sensor one die was measured from each split condition. The condition by which the noise of the sensor was measured and calculated is shown below in Table 6.2. The RTS measurements were taken with an analog gain of 8X with a digital gain of zero and the read noise was

measured with an analog gain of 4X and a digital gain of 2X. All other measurement conditions are those listed in Table 6.2. The pixel level RTS noise data is shown in Figures 6.7 – 6.10 on the following pages.

Table 6.2 Image Sensor characterization settings and conditions

Test Conditions	
Hardware:	Denali Demo Camera
Data Processing:	500 frames raw Bayer
	ROI: 1604 X 1200 820 X 600 each color plane Conversion Gain: 69 µV/e^-
	Dark Image, Room Temp
	Matlab RTS Noise Analysis
Sensor Settings:	By-pass all ISP
	Disable BPC/Black Sun
	Analog Gain 4X, 8X Digital Gain 2X

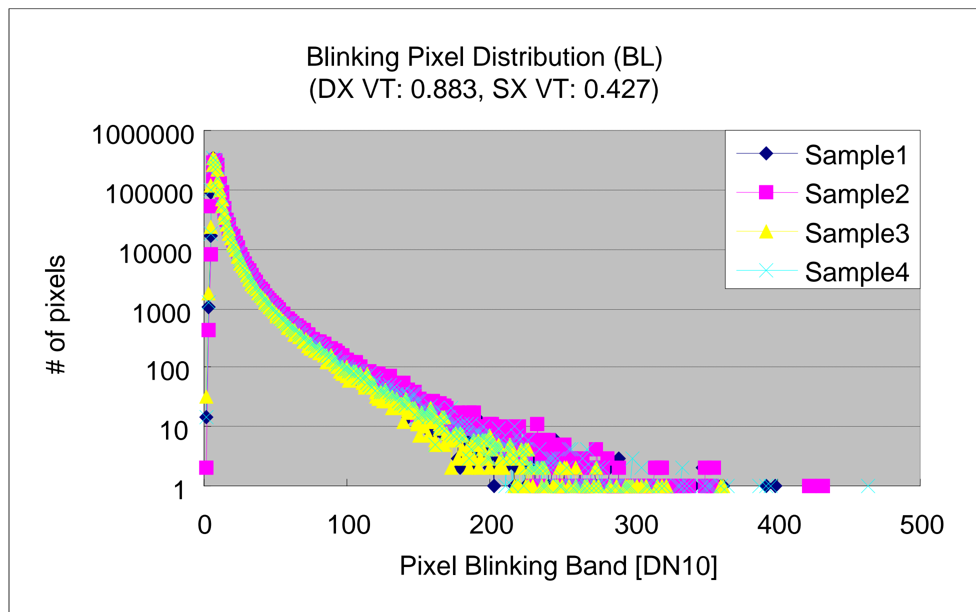

Figure 6.7 RTS pixel distribution from baseline process conditions

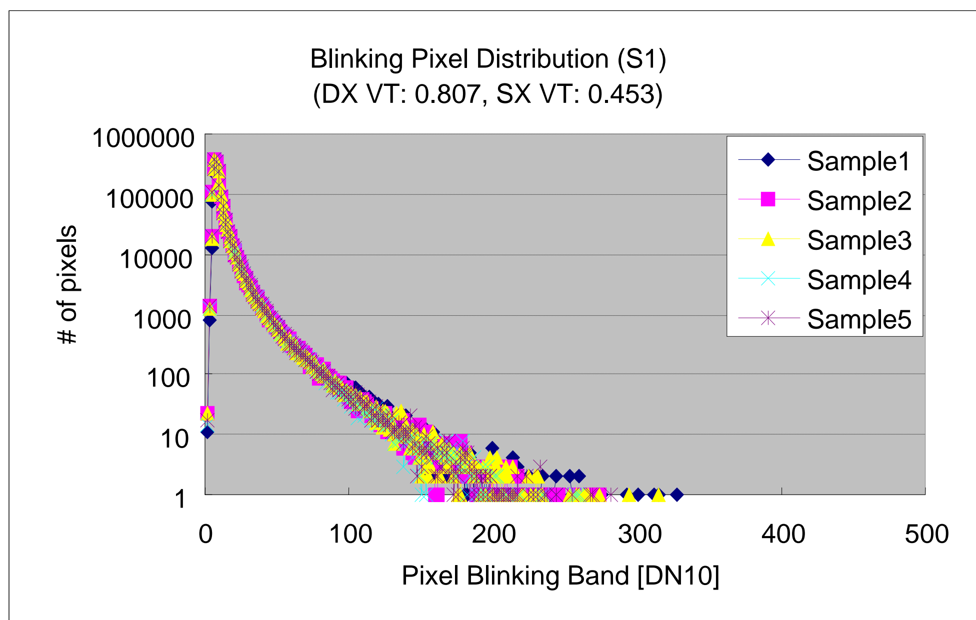

Figure 6.8 RTS pixel distribution for split #1

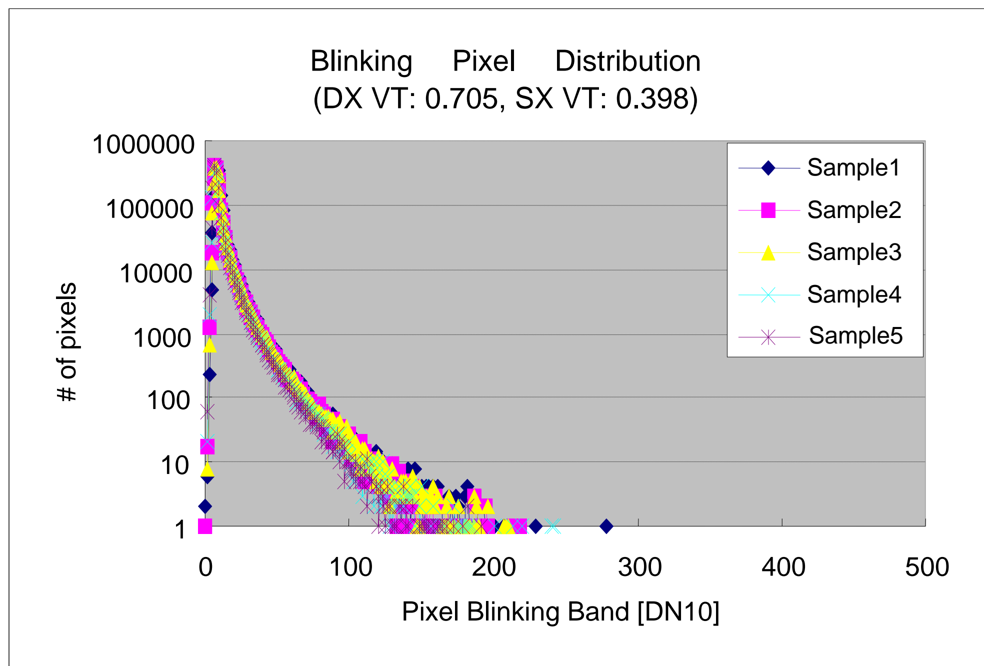

Figure 6.9 RTS pixel distribution for split #2

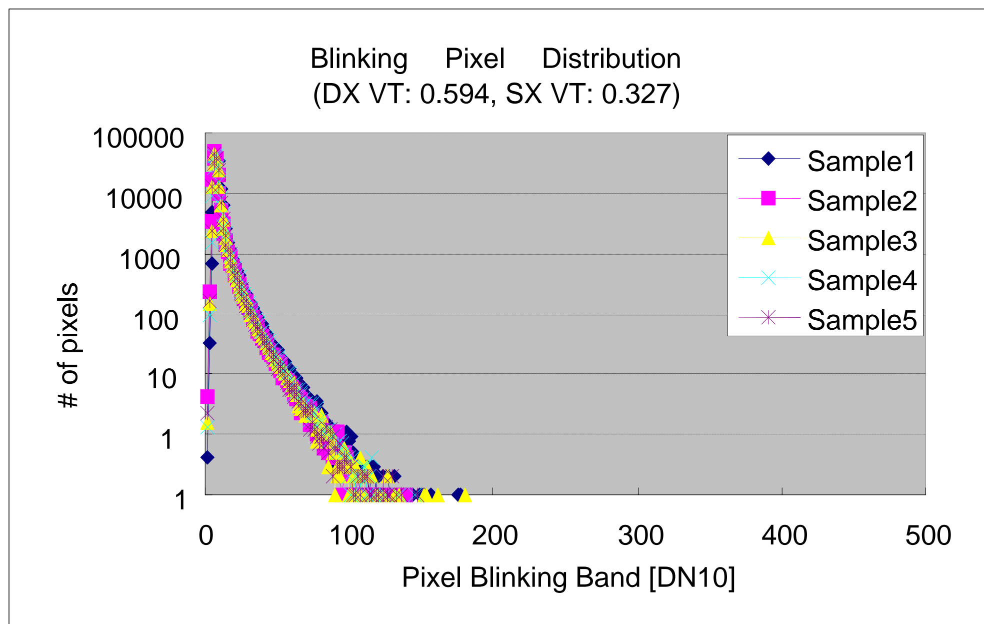

Figure 6.10 RTS pixel distribution for split #3

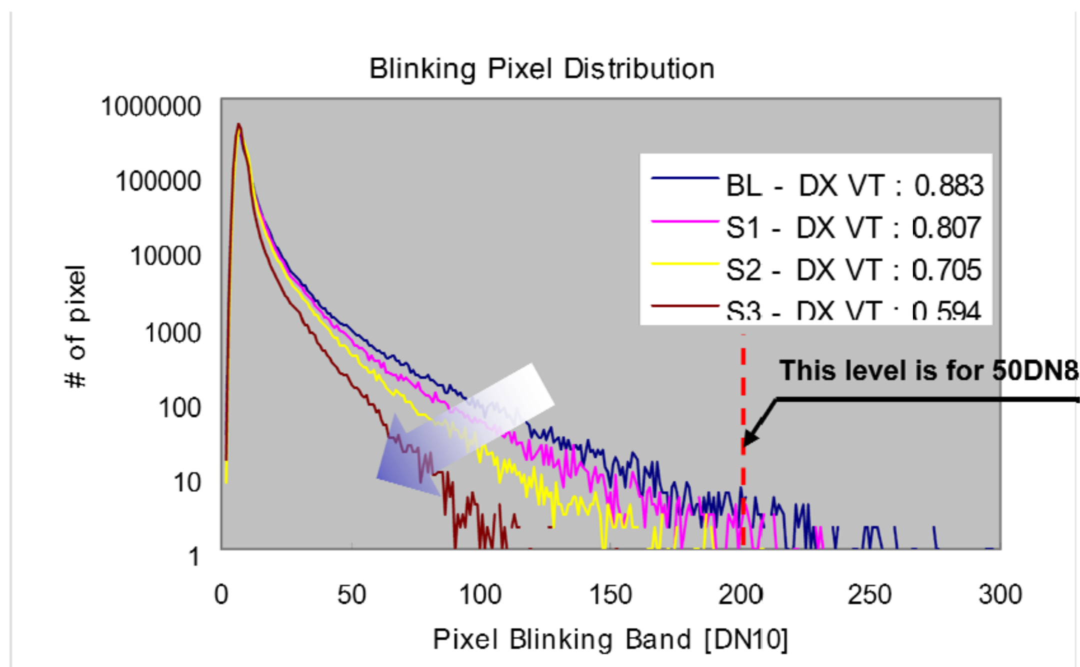

Figure 6.11 RTS pixel distribution from mean samples taken from each process split condition

It is very clear from Figure 6.11 that the RTS blinking pixels had been significantly reduced as a result of the decrease in the doping concentration. Above in Figure 6.11, is plotted the read noise of the average of the samples measured for temporal noise characterization, Figures 6.7 – 6.10. What is important to observe from Figure 6.11 is the tail in the distributions. Going from baseline to split 3 the tail in the distribution has observably decreased. This tail in the distribution results in poor image quality since this is a measure of the noisiest of the pixels in the sensor. Reducing the tail in the distribution is a goal for all image sensor designs. Further characterization of the temporal noise also came to the same conclusion. In

Figure 6.12 below, the noise is converted from digital number to a noise voltage. This is done by taking the 12 bits of the ADC over the 1 volt span of the output signal which results in 244μV/LSB.

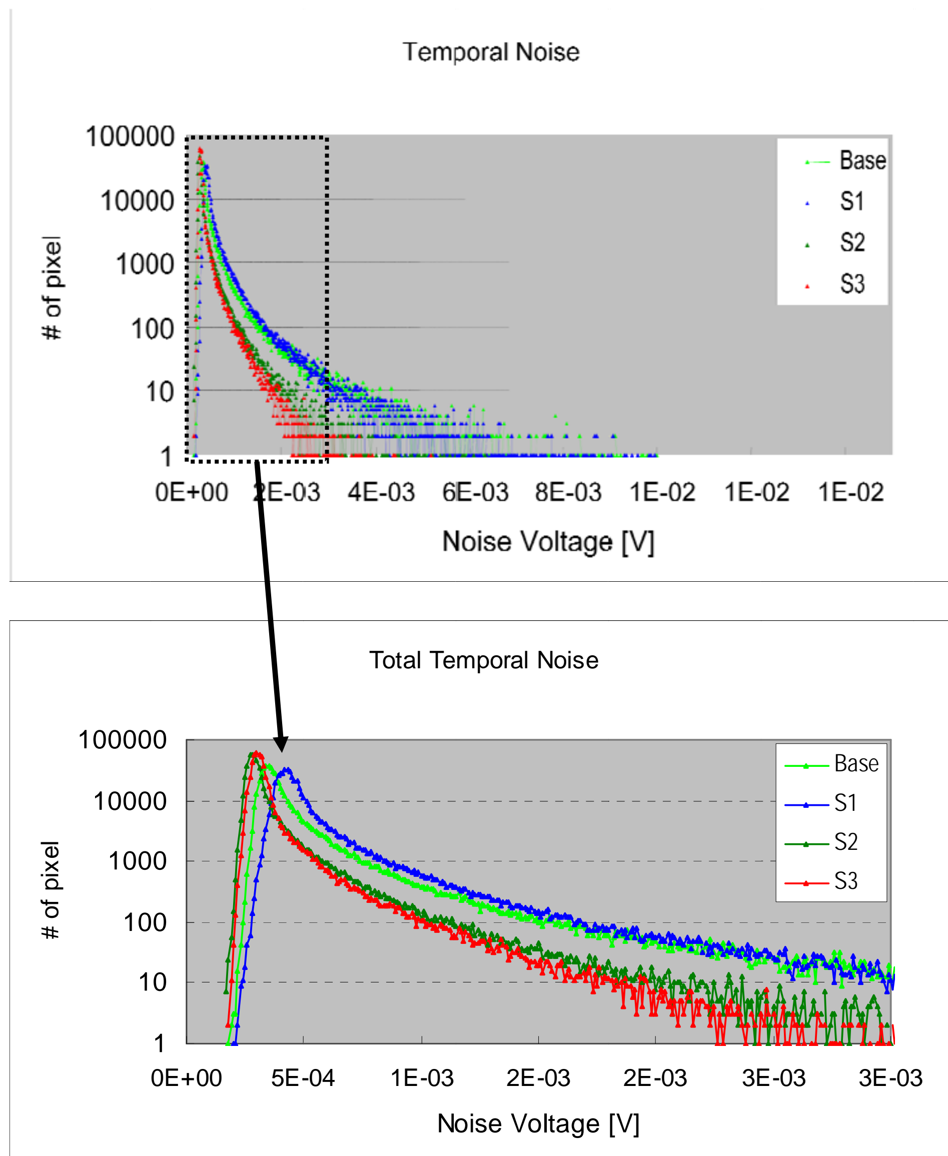

Figure 6.12 Temporal noise distributions

Table 6.3 Total Temporal Noise from process splits baseline, 1, 2, 3

	Total Noise [e-]	**Analog Total Noise [e-]**	**Pixel Total Noise [e-]**
Base	6.54	3.45	5.40
Split 1	7.18	4.32	5.49
Split 2	4.25	2.90	2.88
Split 3	4.11	3.08	2.41

The Table 6.3 shows the result of the total temporal noise. The baseline process conditions show a total temporal noise of 5.4 e-. As a result of the lower doping and threshold voltage of the device the noise is reduced by over 50% to 2.41 e- for Split #3.

The read noise of the image sensor was also characterized at the Advanced Pixel Research Center in Portland, OR. The results confirmed what was previously measured at the Korean facility. The read noise of the imager was again measured and calculated by taking 500 frames of data and computing the individual pixel temporal noise. Figure 6.13 is the result of these measurements. In the Figure 6.13 are the typical device characteristics for each of the split conditions. In this data is one additional split and that is the native device. As in the case with individual MOSFET noise measurements, the source follower of the image sensor was

processed with no additional implant for the threshold adjustment. This results in a V_T of approximately 0.4v.

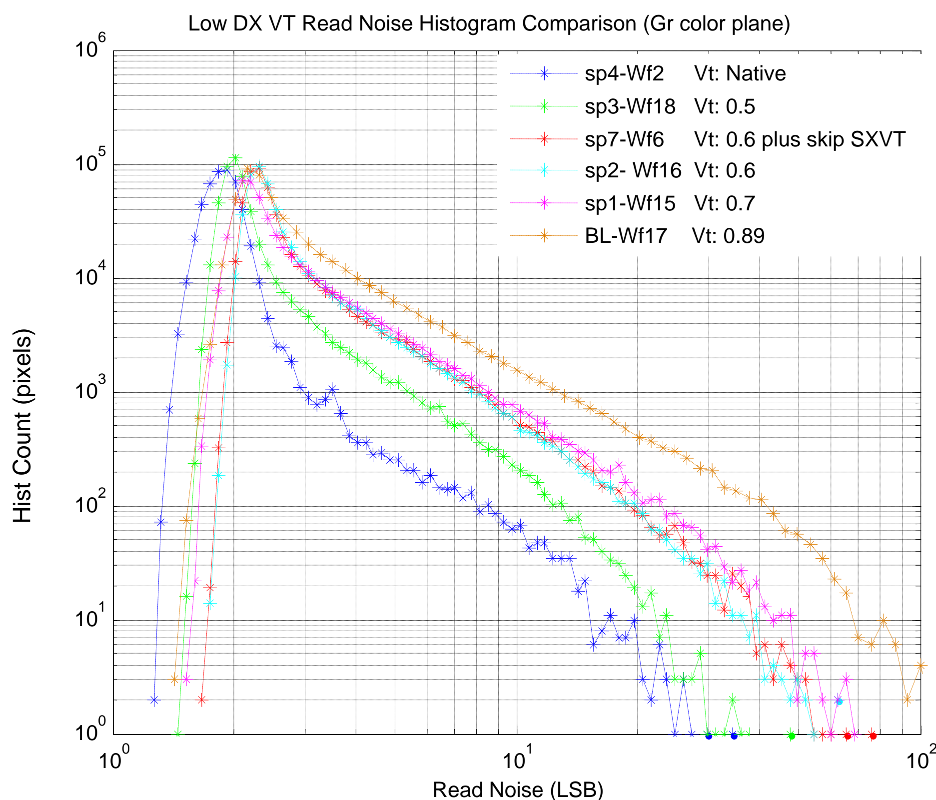

Figure 6.13 Read noise of the process splits

The cumulative distribution plot of Figure 6.14 also highlights the improvement gained by the decrease in the doping density. From Figure 6.14 the probability distribution of pixel exhibiting noise greater than 2 e- has gone from almost 1 down less than 0.02. This represents a large low-light performance increase for the improved image sensor as will be shown in the read noise maps.

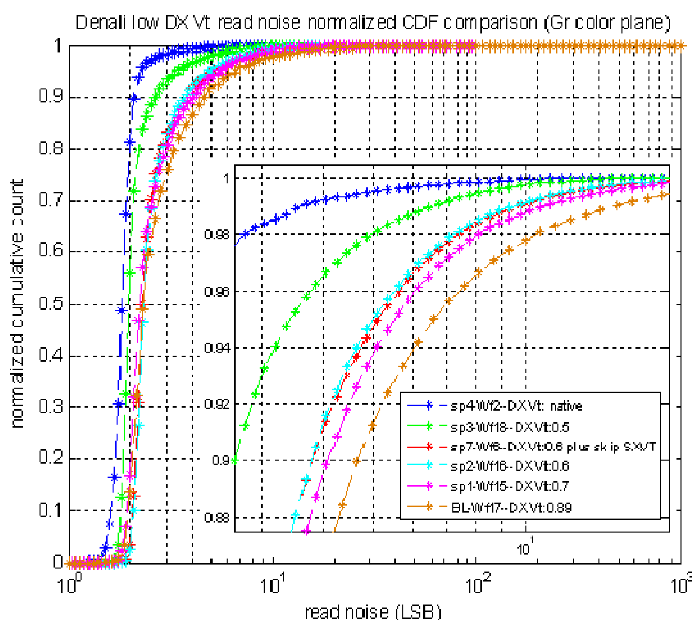

Figure 6.14 Cumulative distribution function of the read noise

On the next page, Figure 6.15, are read noise maps of the individual pixels. The brightness of the pixel shown in the image is a measure of the relative noise of the corresponding pixel. This noise will also manifest as poor image quality especially in low-light conditions. For instance a pixel which is black virtually has no additional noise above the mean pixel value. These maps serve as a visual representation of the data shown in Figures 6.13 and 6.14. Again these maps also demonstrate clearly that through reduction of the threshold voltage there is a clear improvement in the uniformity and reduction in high (bright) RTS pixels. With the decrease in the noise other issues in the imager design are able to be seen such as

the column wise fixed-pattern noise which was almost masked by the high level of RTS pixels in the BL, 1, and 2 process splits.

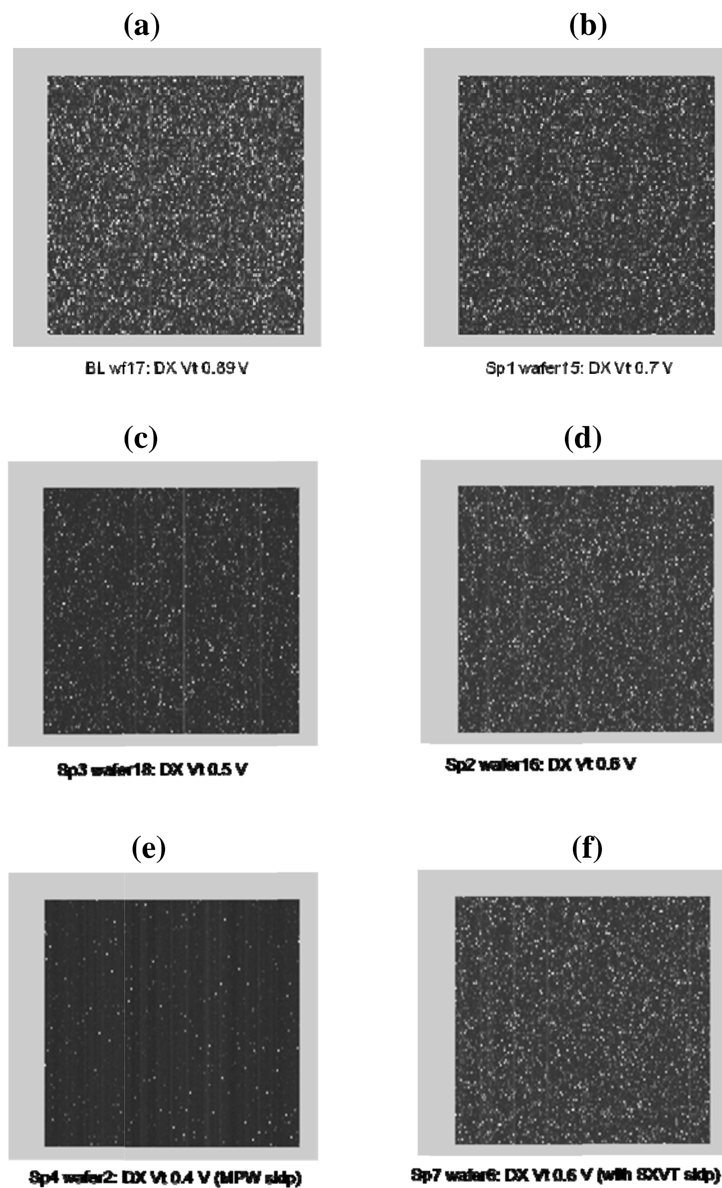

Figure 6.15 Read noise maps for pixel splits (a) – (f) represent various implant splits

6.6 Imager RTS Noise Characterization (Time Domain)

In order to characterize the RTS noise of the CIS device a number of frames of data were taken in order to gain the necessary statistics required to accurately calculate the noise. When looking at RTS the sequence and timing of these frames is important in order to capture the behavior of the particular RTS signature. As shown previously, the RTS signature is a signal which contains discrete steps to one or many repeatable levels. These steps are characteristic of the trapping effect on the drain current of the SF transistor. As discussed the RTS noise seen in CMOS image sensors manifest as blinking pixels.

The following data will provide further insight into the blinking pixel behavior. For the following data and discussion a blinking pixel is categorized as outlined in Table 6.4. The table describes three types of blinking or RTS pixels. The first, RTS, has a symmetric behavior where the signal swings to levels above and below the mean signal value. Figure 6.16 demonstrates exactly what the data looks like from a sequence of 100 frames. Each of these frames represents the signal level at that instant in time. In this case it can be seen that the pixel value swings from a relatively high value at frame twenty to zero two frames later. The signal remained in both of these states for two frames before returning to the mean signal level. This is an excellent example of the negative impact that RTS has on image quality for a 4T pixel such as this. The second category of RTS pixel, from Table 6.4, is the bright RTS pixel. Similar to the RTS symmetric pixel, the bright RTS pixel blinks

between the mean signal and a high signal, as shown in Figure 6.17. This time the signal is never seen going much lower than the mean value. What is interesting from Figure 6.17 is the additional RTS signal that is at a lower magnitude showing that there are additional RTS traps that effect much less of the source follower current or are due to a separate noise mechanism.

Table 6.4 RTS blinker type definitions

Blinker Type	**Definition**
RTS (Symmetric)	If pixel signal is 30 LSBs above its mean and 30 LSBs below its mean at least one time, this pixel will be count as RTS blinker. If this pixel is also a hot pixel (mean is 50 LSB above whole frame mean), it will NOT be count as a RTS blinker.
Bright (Asymmetric High)	If pixel signal is 30 LSBs above its mean and 30 LSBs below its mean at least one time, this pixel will be count as RTS blinker. If this pixel is also a hot pixel (mean is 50 LSB above whole frame mean), it will NOT be count as a RTS blinker.
Dark (Asymmetric Low)	If pixel signal is never 30 LSBs above its mean and is 30 LSBs below its mean at least one time, this pixel will be count as dark blinker. If this pixel is also a hot pixel (mean is 50 LSB above whole frame mean), it will NOT be count as a dark blinker.

In this case it can be seen that the pixel value swings from a relatively high value at frame twenty to zero over fifty frames later. The signal remained in both of these states for two frames before returning to the mean signal level.

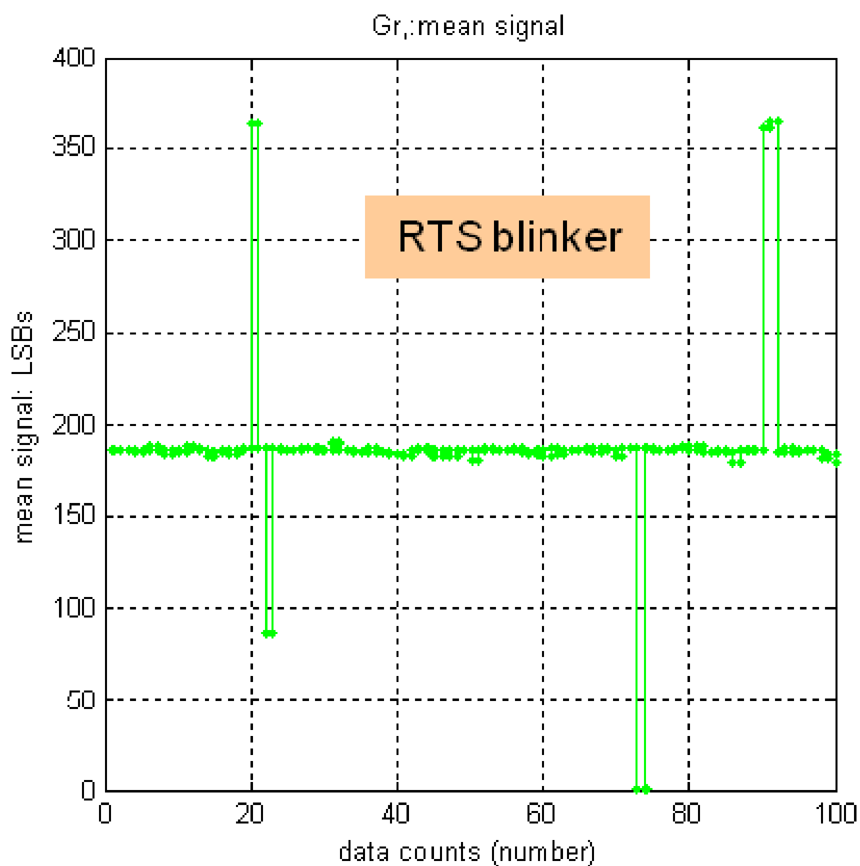

Figure 6.16 RTS Blinker

The second category of RTS pixel from Table 6.4 is the bright RTS pixel. Again, as with the RTS symmetric noise, this pixel blinks between the mean signal and a high signal. In this case, however, the signal is never seen going much lower than the mean value.

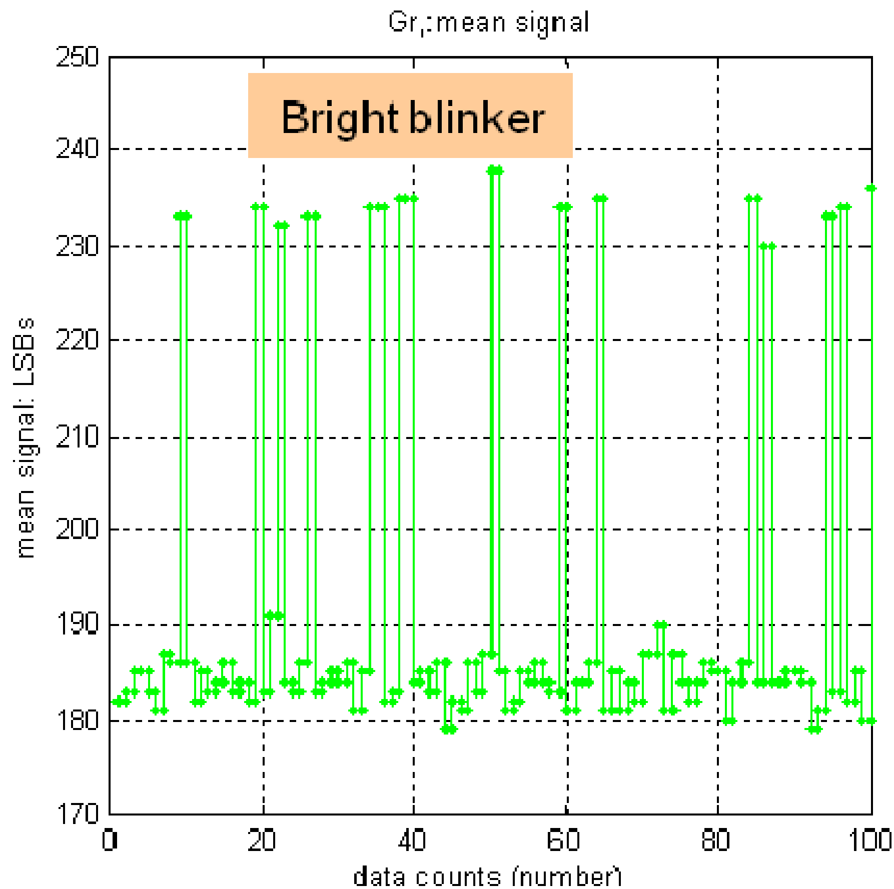

Figure 6.17 Bright blinking pixel

The third RTS pixel is the dark RTS pixel and this type of noise is opposite that seen in the bright pixel. In this case the dark RTS pixel tends to contain only lower values below the mean of the number of RTS pixels seen in each of the color planes of the imager. From this it is readily apparent that the improvement from the lower implant dose reduced the number of detected RTS pixels. Interestingly there is a large difference in the detected number of RTS symmetric versus the bright and dark RTS pixel types. This is also coincidental with noise measurements from source follower transistors. In these transistors there are cases when the noise signal

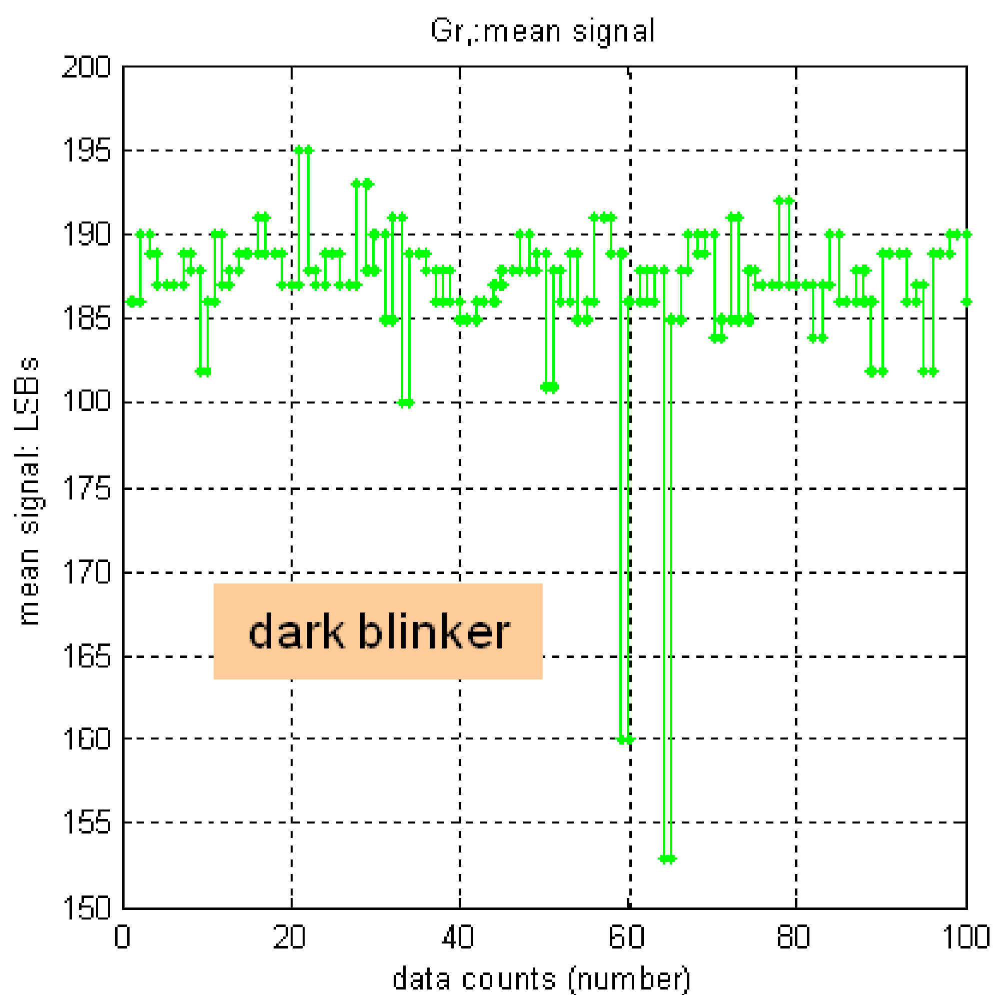

Figure 6.18 Dark blinking pixel.

tends to higher values and those to lower. This high-low behavior is strictly dependent on the depth of the trap in the oxide and the local charge density.

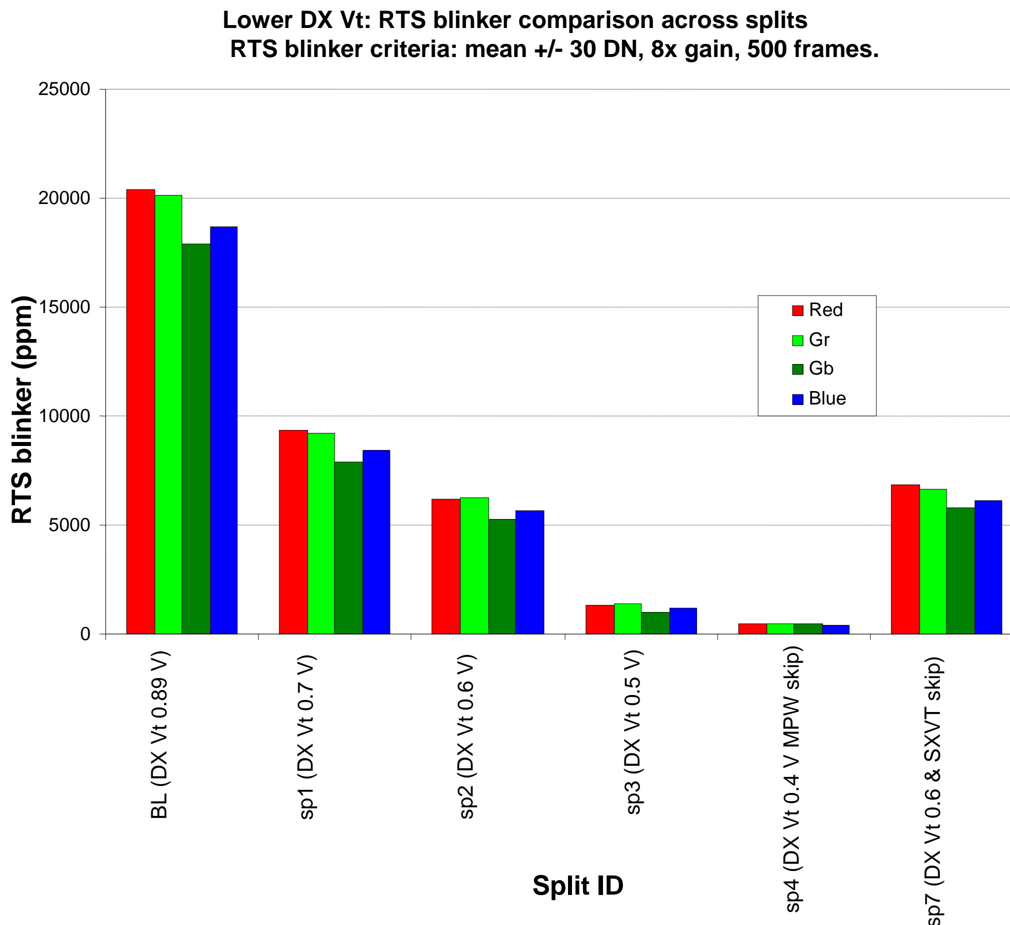

Figure 6.19 Comparison of RTS blinking pixels

The RTS blinking pixel is really just a mixture of the bright and dark blinking pixels. In this case both behaviors are observed in the same pixel. For the baseline conditions the RTS pixel is the most common. For the lower V_T devices there is little difference between the RTS types. Additional analysis techniques were investigated in an attempt to discover the number of RTS pixels in the image. This analysis technique was threshold based and counted the number of pixel above or

below a preset threshold. This technique requires up to 500 frames of data in order to capture all the RTS pixel in the image. This type of analysis would be too costly to be used in a manufacturing test process; however, it does demonstrate the difficulty in adequately quantifying all the RTS pixels in the image.

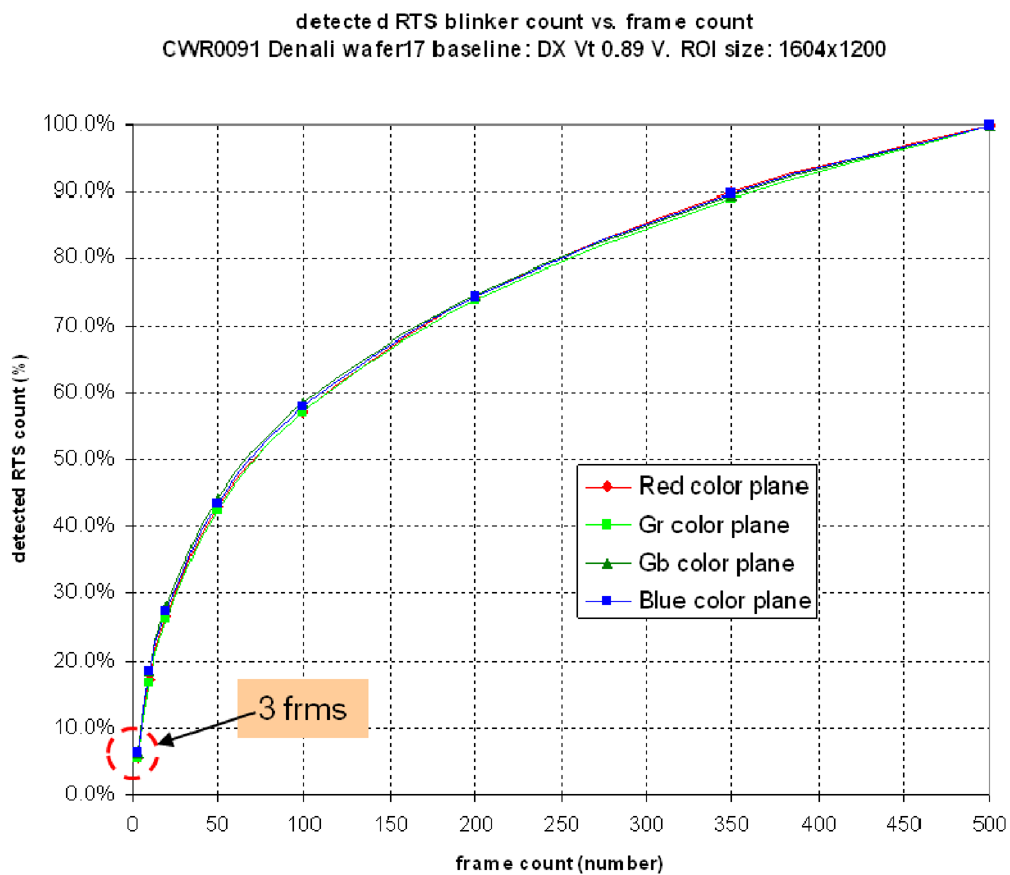

Figure 6.20 Normalized detection probability of RTS blinking pixels

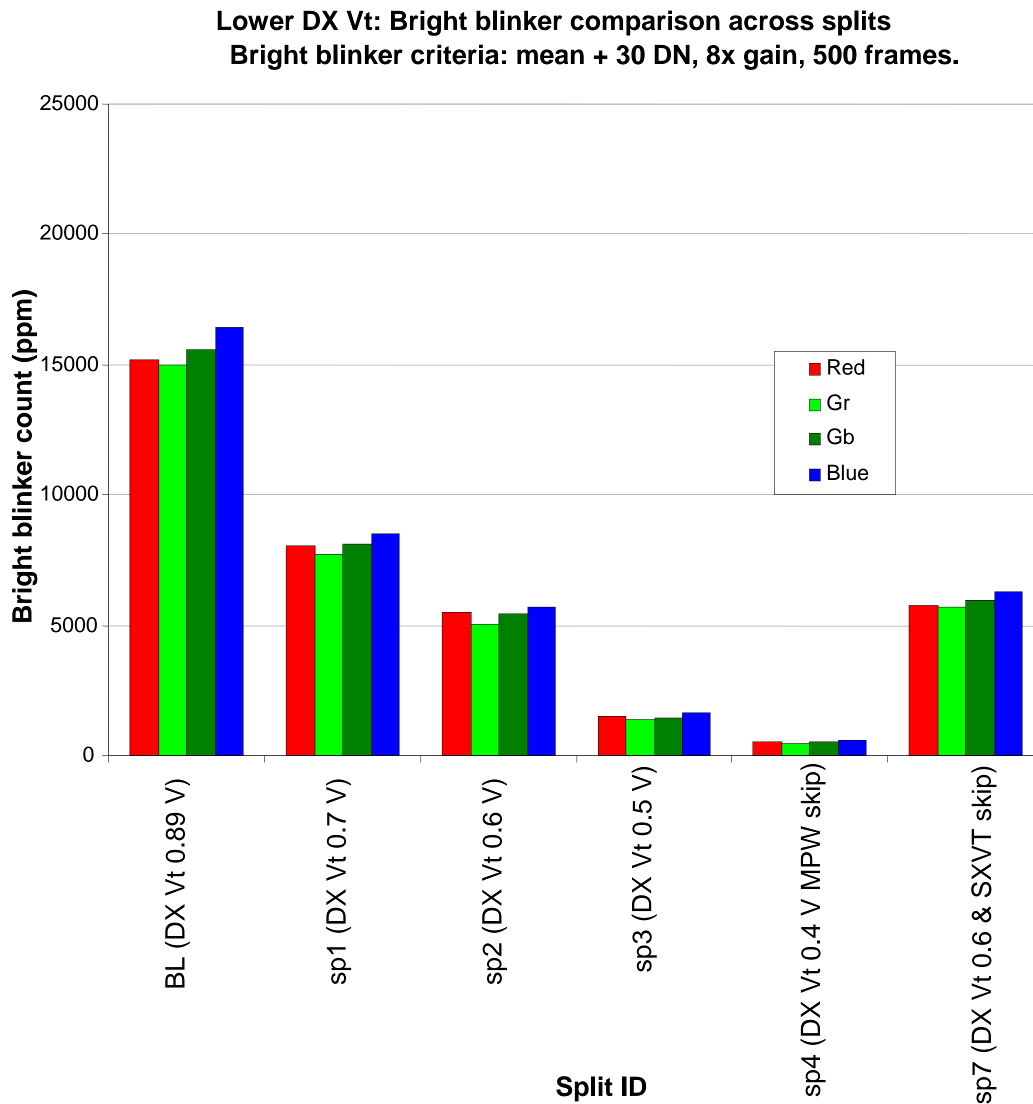

Figure 6.21 Comparison of bright blinking pixels

The bright blinking pixels are characterized by values that increase above the mean signal. For the baseline process, this RTS type is found in lower concentrations as compared to the RTS blinker type by 33%.

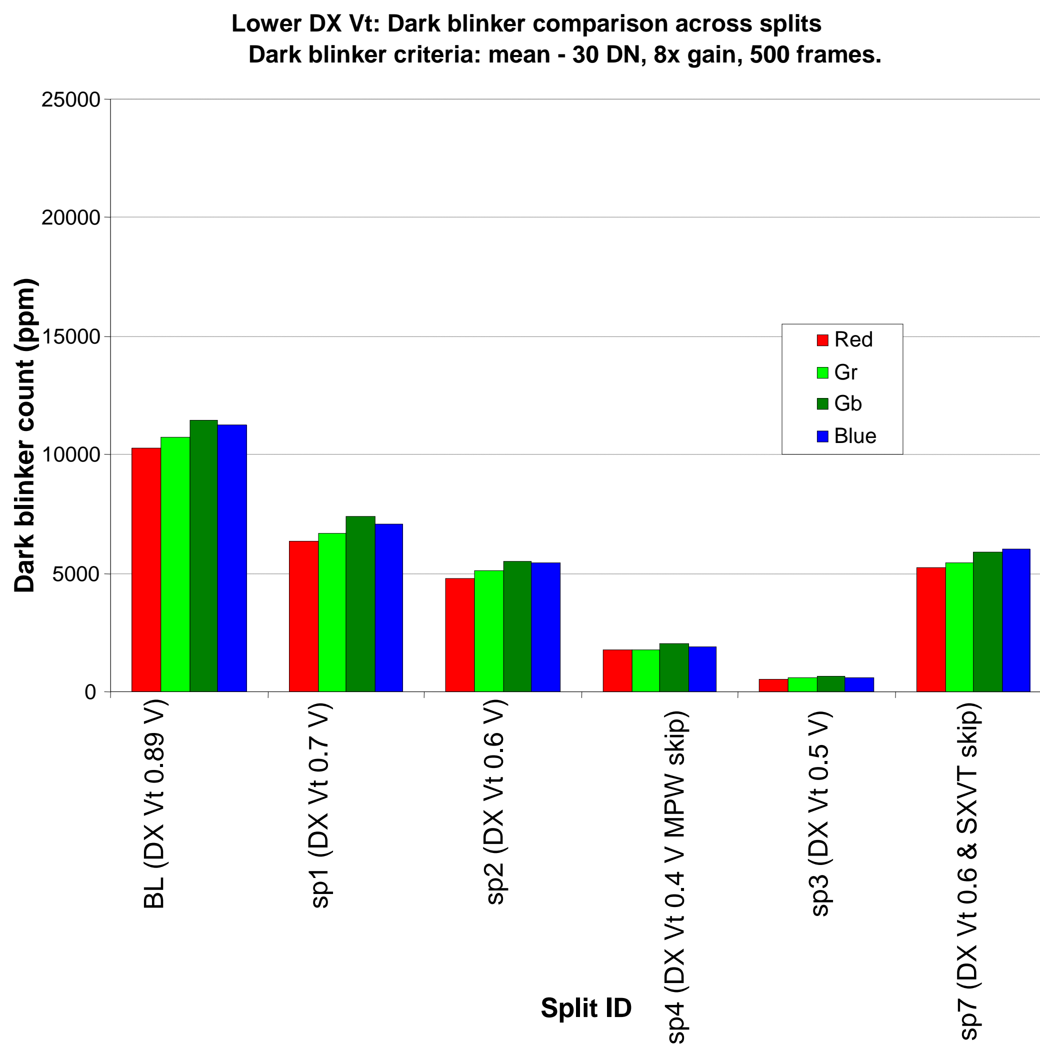

Figure 6.22 Comparison of dark blinking pixels

Figure 6.22 shows that the occurrence of dark blinking pixels is also reduced across the process splits. This type of RTS pixel occurs in lower numbers as compared to the bright blinking pixels by 33%.

6.7 Case Study Conclusion

This study performed on the CMOS image sensor demonstrated that a strong correlation exist between the doping of the source follower MOSFET and the noise in the image. This relationship is described as being due to the percolation currents in the channel of the device and the traps in the oxide which modulate these percolation currents. As a result of this understanding experiments were performed on a 2.2µm pixel 2MP CMOS image sensor where the threshold voltage doping was adjusted and the resulting noise of the image sensor characterized. The image sensor characterization showed what was also predicted from the percolation model and that was that the noise would be nearly cut in half. In this case the total temporal noise between the baseline and Split #3 condition fell from 5.4 e- to 2.41e- as a result of the lower doping concentration.

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7 Conclusion

Random-telegraph signal (RTS) serves as the basis for the observed low-frequency noise seen in MOSFETs and has been a focus of both technological and academic interest for over 30 years. Technologically RTS poses some challenging problems that present fundamental physical barriers that limit device performance especially for highly demanding analog and digital applications. In applications such as DRAM and flash memories it is required that error rates be incredibly low and yet memory densities continue to increase further requiring that devices become smaller and smaller. This shrink has a huge impact on the device variability and noise properties of these systems. As demonstrated here with CMOS image sensors the noise of analog circuits are also severely impacted by this RTS noise. In the image sensor the low-light performance of the sensor is the concern and the result is a grainy image under these conditions.

Not understanding the physical mechanisms or properties of the noise source presents challenges to the device and circuit designer. At their disposal are empirical models which often perform well, but these models can break down leading to poor performance if the noise source is not fully understood. It is always better to have a thorough understanding of the noise mechanism and behavior. In the case of thermal and shot noise these noise sources are well known and characterized to the point that these noise sources can be reliably predicted. This is

a prime example of the fact that once the noise mechanism is understood, one is capable of identifying methods to push the noise floor lower creating all new sensing capabilities.

In the case of this research it was shown that once the noise source and mechanism was understood necessary steps could be taken to reduce the source of the noise. Two examples shown here are the impact of substrate bias and modification of the doping levels. Substrate biasing is a relatively straight forward approach to reducing the noise and has been show here to have this repeatable effect. With additional understanding of the percolation currents modification of the channel dopant profile can serve as an additional means for device noise improvement. Once understood, these relatively easy steps, as in the case of reducing the implant dose in the channel, verified the theory and model developed during this research and resulted in a superior performing CMOS image sensor product.

Future work into the lowering of MOSFET noise should lead one to focus on these fundamental elements of doping and bias architectures which are capable of reducing both device-to-device variability, but also the overall noise of the system. Some of these architectures would be delta doping under the channel. This delta doping has the possibility of reducing the surface potential variation and also the noise. The problem is that in the n-MOSFET this doping is most often done with Boron and Boron is a fast diffuser during the subsequent thermal cycles typical

of modern CMOS process. Future work should focus on other dopant species that are less diffusive and can provide a reasonable activation to maintain device performance. Like Arsenic, Gallium and Indium that are heavier atoms and thus are less prone to diffusing. These would be interesting atoms in terms of creating this delta doped region. Future work on the doping species dependence of noise in n-MOSFETs should focus on these two elements.

Some device structures are already in existence that would also be interesting to look at from a noise perspective. In particular double gated MOSFETs with intrinsic channels would be interesting candidates for future work. These devices have little to no dopant in the channel region and rely on the field of the double gate structure for operation. With the absence of dopant in this type of device there would be less of chance for percolation currents to form and the associated large swing in the resulting low-frequency noise signal.

The noise source as describe here has provided an insightful look into the nano scale operation of a MOSFET. Whether the device is much larger than a micron or made at the nanometer regime, percolation currents are always present. As long as there is an oxide there will always be traps capable of capturing carriers. These two phenomena will continue to dominate the low-frequency noise behavior of MOSFETs. Presented here are two methods to reduce this noise source and push the noise limits of MOSFET technology to new lows.

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APPENDICES

Appendix A Spectral Estimation

It is often desirable and more efficient to look at and to perform manipulations on data in the frequency domain. The frequency characteristics of a set of data are important in understanding the components of a signal that are not readily apparent from time domain data.

The Welch spectral estimation method uses a smoothing technique for reducing the variance in the resulting spectrum. This is accomplished by breaking the data record into multiple segments. The segments can then be overlapped and averaged with the original data record creating a situation of creator averaging for a given set of data. A window is applied to each of the segments in order to reduce the error resulting from a rectangular window. This method allows one to the tailor of the spectral estimate by trading off resolution for reduced variance or vice versa. For a data record consisting of N samples

The process by which the Welch method is carried out is described by first windowing the first data segment [2]:

$$x^{(p)}[n] = w[n]x[n + pS] \tag{A.1}$$

where $x^{(p)}[n]$ is the windowed data of the pth segment, $w[n]$ is the discrete window function, and $x[n + pS]$ is the sampled data in of the pth segment. The pth segment power spectrum is then calculated as:

$$P_{xx}^{(p)}(f) = \frac{1}{UDT} X^{(p)}(f)\left[X^{(p)}(f)\right]^{*} = \frac{1}{UDT}\left|X^{(p)}(f)\right|^{2} \quad \text{(A.2)}$$

where T is the sample period and $X^{(p)}(f)$ is the discrete-time Fourier transform of the pth segment as:

$$X^{(p)}(f) = T\sum_{n=0}^{D-1} x^{(p)}[n]e^{-j2\pi fnT} \quad \text{(A.3)}$$

and U is the window power correction factor given by:

$$U = \left|\frac{1}{D}\sum_{n=0}^{D-1} w[n]\right|^{2} \quad \text{(A.4)}$$

Finally, the Welch power spectrum is calculated by averaging the individual segment spectrums:

$$P_{W}(f) = \frac{1}{P}\sum_{p=0}^{P-1} P_{xx}^{(p)}(f) \quad \text{(A.5)}$$

On the next page is the Matlab program that was used in this research for calculating the power spectrum of the random-telegraph signals.

```
function psd=welch_psd(num_psd,window,overlap,seg_size,T,x,y)

% Classical periodogram auto/cross power spectral density estimate
by Welch
% procedure, eqs. (5.39),(5.40),(5.43).
%
%    Auto:   psd=welch_psd(num_psd,window,overlap,seg_size,T,x)
%    Cross:  psd=welch_psd(num_psd,window,overlap,seg_size,T,x,y)
%
% num_psd  -- number of psd vector elements (must be power of 2);
%                      frequency spacing between elements is F =
1/(num_psd*T)
%              Hz, with psd(1) corresponding to frequency  -1/(2*T)
%              Hz, psd(num_psd/2 + 1) corresponding to  0  Hz, and
%              psd(num_psd) corresponding to 1/(2*T) - F  Hz.
%  window    -- window selection: 0 -- none, 1 -- Hamming, 2 --
Nuttall
% overlap  -- number of overlap samples between segments
% seg_size -- number of samples per segment (must be even)
% T        -- sample interval in seconds
% x        -- vector of data samples
% y        -- vector of data samples (cross PSD only);
%                  note that length(y) must equal length(x)
% psd      -- vector of num_psd auto/cross PSD values

if nargin == 7
    if length(x) ~= length(y)
        error('The input data vectors are not of equal lengths.')
    end
end
if seg_size > num_psd
    error(['Seg_size cannot exceed num_psd = ',int2str(num_psd)])
end
if (overlap < 0) | (overlap >= seg_size)
    error(['Out of range: 0 <= overlap <',int2str(seg_size)])
end
shift = seg_size - overlap;
num_segs = fix(( length(x) - seg_size )/shift) + 1;
psd = zeros(num_psd,1);
range = 1:seg_size;
s = seg_size - 1;
ph = 2*pi*(0:s)/s;

if     window == 0  wind = ones(seg_size,1);          % rectangular
(aka boxcar)
```

```
elseif  window  ==  1    wind  =  (.53836  -  .46164*cos(ph))';
% Hamming
elseif window == 2  wind=(.42323-.49755*cos(ph)+.07922*cos(2*ph))';
% Nuttall
else
    error('Window selection number is invalid.')
end
% Wind  could also be specified as one of the following from the
MATLAB Signal
% Processing Toolbox:
%   wind = barlett(seg_size);
%   wind = blackman(seg_size);
%   wind = chebwin(seg_size,sidelobe level in db);
%   wind = hanning(seg_size);
%   wind = kaiser(seg_size,0.1102*(sidelobe level in db - 8.7));
%   wind = triang(seg_size);

for k=1:num_segs
    z = T*fft(wind.*x(range),num_psd);
    if nargin < 7
        psd = psd + real(z).^2 + imag(z).^2;
    else
        psd = psd + z.*(T*conj(fft(wind.*y(range),num_psd)));
    end
    range = range + shift;
end
pow_wind = sum(wind.^2)/seg_size;          % adjustment in gain for
window power
psd = (1/(num_segs*pow_wind*seg_size*T))*fftshift(psd);
%
```

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Appendix B Imager Sensor Noise Equations

The purpose of image sensor noise characterization is to quantify and indentify the sources of noise and variation present in the image sensor design. The various noise components of the sensor are what set each design and product apart within a company's product line or between competing products. Some of the sources of noise are at the pixel level (i.e. transfer gate, reset, source follower) while other sources of noise is due to the column readout electronics consisting of the sampling circuits, programmable gain amplifiers, and output amplifiers. Through careful test design each of these noise sources can be measured and the results provide insight and guidance to future design optimizations.

Below are the typical metrics and algorithms for collecting and calculating the key imager noise sources.

Mean signal:

$$\bar{p} = \frac{1}{N \cdot X \cdot Y} \sum_{n=1}^{N} \sum_{x=1}^{X} \sum_{y=1}^{Y} p_n(x, y) \tag{B.1}$$

Total noise:

$$\sigma_{total} = \left[\frac{1}{N \cdot X \cdot Y} \sum_{n=1}^{N} \sum_{x=1}^{X} \sum_{y=1}^{Y} (p_n(x, y) - \bar{p})^2 \right]^{1/2} \tag{B.2}$$

Total temporal noise:

$$\overline{p_n}(x,y) = \frac{1}{N}\sum_{n=1}^{N} p_n(x,y) \tag{B.3}$$

$$\sigma_{temporal}(x,y) = \left[\frac{1}{(N-1)}\sum_{n=1}^{N}(p_n(x,y) - \bar{p}(x,y))^2\right]^{1/2} \tag{B.4}$$

$$\sigma_{temporal} = \left[\frac{1}{X \cdot Y}\sum_{x=1}^{X}\sum_{y=1}^{Y}\left(\sigma_{temporal}(x,y)\right)^2\right]^{1/2} \tag{B.5}$$

$$\sigma_{temporal} = \frac{1}{X \cdot Y}\sum_{x=1}^{X}\sum_{y=1}^{Y}\sigma_{temporal}(x,y) \tag{B.6}$$

Row temporal noise:

$$\bar{p}_n(y) = \frac{1}{X}\sum_{x=1}^{X} p_n(x,y) \tag{B.7}$$

$$\sigma_{temporal}(y) = \left[\frac{1}{N-1}\sum_{n=1}^{N}\left(\left(\bar{p}_n(y)\right) - \frac{1}{N}\sum_{n=1}^{N}\bar{p}_n(y)\right)^2\right]^{1/2} \tag{B.8}$$

$$\sigma_{row\ temporal} = \left[\frac{1}{Y}\sum_{y=1}^{Y}\left(\sigma_{temporal}(y)\right)^2\right]^{1/2} \tag{B.9}$$

Column temporal noise:

$$\bar{p}_n(x) = \frac{1}{Y}\sum_{y=1}^{Y} p_n(x,y) \tag{B.10}$$

$$\sigma_{temporal}(x) = \left[\frac{1}{N-1}\sum_{n=1}^{N}\left(\left(\bar{p}_n(x)\right) - \frac{1}{N}\sum_{n=1}^{N}\bar{p}_n(x)\right)^2\right]^{1/2} \tag{B.11}$$

$$\sigma_{row\ temporal} = \left[\frac{1}{X}\sum_{x=1}^{X}\left(\sigma_{temporal}(\ x)\right)^2\right]^{1/2} \tag{B.12}$$

Frame flicker noise:

$$\bar{p} = \frac{1}{N \cdot X \cdot Y}\sum_{n=1}^{N}\ \sum_{x=1}^{X}\ \sum_{y=1}^{Y} p_n(x,y) \tag{B.13}$$

$$\overline{p_n}(x,y) = \frac{1}{X \cdot Y}\sum_{x=1}^{X}\ \sum_{y=1}^{Y} p_n(x,y) \tag{B.14}$$

$$\sigma_{frame\ flicker}(x) = \left[\frac{1}{(N-1)}\sum_{n=1}^{N}(\bar{p}_n - \ \bar{p}\ )^2\right]^{1/2} \tag{B.15}$$

Pixel temporal noise:

$$\sigma_{pixel\ temporal} = \left[\left(\sigma_{temporal}\right)^2 - \left(\sigma_{row\ temporal}\right)^2 - \left(\sigma_{col\ temporal}\right)^2 + \ \left(\sigma_{frm\ flicker}\right)^2\right]^{1/2} \tag{B.16}$$

Total fixed-pattern-noise (FPN):

$$\overline{p_n}(x,y) = \frac{1}{N}\sum_{n=1}^{N} p_n(x,y) \tag{B.17}$$

$$\bar{p} = \frac{1}{N \cdot X \cdot Y} \sum_{n=1}^{N} \sum_{x=1}^{X} \sum_{y=1}^{Y} p_n(x, y) \tag{B.18}$$

$$\sigma_{total\ FPN} = \left[\frac{1}{(XY - 1)} \sum_{x=1}^{X} \sum_{y=1}^{Y} (\bar{p}(x, y) - \bar{p}\ )^2 \right]^{1/2} \tag{B.19}$$

Row FPN:

$$\bar{p}(x, y) = \frac{1}{N} \sum_{n=1}^{N} p_n(x, y) \tag{B.20}$$

$$\bar{p}(\ y) = \frac{1}{X} \sum_{x=1}^{X} \overline{p_n}(x, y) \tag{B.21}$$

$$\bar{p} = \frac{1}{N \cdot X \cdot Y} \sum_{n=1}^{N} \sum_{x=1}^{X} \sum_{y=1}^{Y} p_n(x, y) \tag{B.22}$$

$$\sigma_{Row\ FPN} = \left[\frac{1}{(Y - 1)} \sum_{y=1}^{Y} (\bar{p}(y) - \bar{p}\ )^2 \right]^{1/2} \tag{B.23}$$

Column FPN:

$$\bar{p}(x, y) = \frac{1}{N} \sum_{n=1}^{N} p_n(x, y) \tag{B.24}$$

$$\bar{p}(\ x) = \frac{1}{Y} \sum_{y=1}^{Y} \overline{p_n}(x, y) \tag{B.25}$$

$$\bar{p} = \frac{1}{N \cdot X \cdot Y} \sum_{n=1}^{N} \sum_{x=1}^{X} \sum_{y=1}^{Y} p_n(x, y) \tag{B.26}$$

$$\sigma_{Row\ FPN} = \left[\frac{1}{(X-1)} \sum_{x=1}^{X} (\bar{p}(x) - \bar{p})^2 \right]^{1/2} \tag{B.27}$$

Pixel FPN:

$$\sigma_{pixel\ FPN} = [(\sigma_{total\ FPN})^2 - (\sigma_{row\ FPN})^2 - (\sigma_{col\ FPN})^2]^{1/2} \tag{B.28}$$