AN ABSTRACT OF THE DISSERTATION OF

Kevin A. Stewart for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on August 22, 2017.

Title: Assessment of High Mobility Oxide Thin-Film Transistors

Abstract approved: _____

John F. Wager

The trend towards higher resolution, faster refresh rate active-matrix liquid-crystal displays (AMLCDs) as well as the emergence of active-matrix organic light-emitting diode (AMOLED) displays is driving the demand for amorphous oxide semiconductor thin-film transistors (AOS TFTs) with higher mobility. A physics-based model for carrier transport in an amorphous semiconductor is developed to estimate the mobility limits of an AOS TFT to be 71 $cm^2V^{-1}s^{-1}$. Only the effective mass and band tail state density need to be specified, relating to the disorder in the amorphous semiconductor. Three ways are identified to achieve a mobility higher than that of quaternary amorphous indium gallium zinc oxide (a-IGZO) with a cation ratio of 1:1:1. i) Quaternary systems with a higher indium ratio; ii) lower disorder ternary oxides (e.g., boron indium oxide); iii) dual active layer (DAL) TFTs. ITO-IGZO DAL TFTs are directly compared with a-IGZO TFTs. The ITO-IGZO DAL TFT exhibits significantly improved performance with mean mobility of 31 $cm^2V^{-1}s^{-1}$, threshold voltage of -3.6 V, sub-threshold swing of 175 mV/dec, minimal hysteresis, and good

bias temperature stress stability. Technology computer aided design (TCAD) simulation is used to elucidate the density of states (DOS) of various types of AOS TFTs. A mapping technique is introduced to relate experimental transfer characteristics to the sub-bandgap DOS model.

Assessment of High Mobility Oxide Thin-Film Transistors

by

Kevin A. Stewart

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented August 22, 2017
Commencement June 2018

Doctor of Philosophy dissertation of Kevin A. Stewart presented on August 22, 2017.

APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Kevin A. Stewart, Author

ACKNOWLEDGEMENTS

I would like to thank my major advisor Dr. John Wager for giving me the opportunity to work on this project and for the continued support and guidance during my graduate education.

The work on novel AOS materials would not have been possible without my project partner Vasily Goulioukin the Chemistry Department. I would like to thank Vasily for the fabrication of the sputter targets, training me on the x-ray diffractometer, and working together to create a presentation of the research results every month. Thanks to Dr. Douglas Keszler for being the co-advisor on the project and bringing in new, innovative ideas.

Thank you to everyone from the Wager group for their technical contributions to this work as well as making this a pleasant environment to work in. The same is true for the other folks who work in the office and labs. No mention of the lab can go without giving a special thanks to Chris Tasker and Rick Presley for bringing up new tools, keeping the existing tools running, and their great hands-on training.

Finally, I would like to thank Dr. Robert Manley of Thin Films Research, Corning Incorporated for the support of this project.

This work was funded by Corning Incorporated.

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CHAPTER 1: INTRODUCTION

An amorphous solid exhibits short range order but no long range order on the atomic scale. In other words, the structure beyond first or second nearest-neighbor atoms is random. People have been using and preparing amorphous solids, e.g., silicate glasses for thousands of years. However, amorphous semiconductors for (opto-)electronics applications are a much more recent discovery. The subject of amorphous semiconductors has rapidly evolved from academic curiosity [15] in the 1950s to the principal semiconductor in large-area electronics today. This is mostly due to the discovery of how to use hydrogen to passivate dangling bonds in amorphous silicon, which greatly reduces its defect density [16]. Hydrogenated amorphous silicon (a-Si:H) has been employed in solar cells and is still the dominant semiconductor in active-matrix liquid crystal displays (AMLCDs). In AMLCDs, a-Si:H is the active layer in the thin-film transistor (TFT) that is associated with every pixel. Furthermore, amorphous semiconductors lack grain boundaries and are ultra-smooth, which makes them very suitable for deposition over large areas.

In 1996, a new class of amorphous materials was discovered [17]. These were later named amorphous oxide semiconductors (AOSs), or sometimes just 'oxides' [5]. AOSs are remarkable in that AOS electron mobility is hardly reduced compared to its crystalline counterpart. The most widely employed AOS today is amorphous indium gallium zinc oxide (a-IGZO). The electron mobility of a-IGZO is 10 to 20 times greater than that of a-Si:H. Additionally, AOSs have a wide band gap of approximately 3 eV which makes them transparent in the visible regime and AOSs can be

easily deposited via sputtering at low temperatures. All of this makes oxides a prime candidate to replace a-Si:H in existing applications and to enable next-generation flat-panel displays as well as transparent, flexible, and wearable electronics. To realize these new applications, a lot of interest is directed towards finding AOSs with even higher electron mobility.

The research presented herein assesses high mobility oxide TFTs from both an experimental and modeling standpoint. Oxide TFTs are fabricated at the Materials Synthesis and Characterization laboratory at Oregon State University. Theoretical models are developed using both fundamental physics considerations as well as commercial 2-dimensional device simulation software.

This dissertation is structured as follows. Chapter 2 provides the necessary background information and a review of the current literature. Chapter 3 proposes a model to assess the upper limit of mobility in an amorphous semiconductor. Chapter 4 introduces the experimental methods used in this work. Chapter 5 presents the results of boron indium oxide TFTs. Chapter 6 investigates dual active layer TFTs as a means to further increase oxide TFT performance. Finally, Chapter 7 presents conclusions and recommendations for future work.

CHAPTER 2: BACKGROUND AND LITERATURE REVIEW

This chapter provides a background on TFTs and their application. The fundamental physics of AOSs are briefly summarized as it pertains to the discussion in this thesis. Lastly, the literature on high mobility oxide TFTs is reviewed.

2.1 Flat-Panel Displays

2.1.1 Major Display Milestones

Active-matrix, TFT-based flat-panel displays (FPDs) were first widely adopted in laptop screens around 1995. Not long after that, AMLCDs started to replace the bulky cathode ray tube (CRT) computer monitors. Nowadays, AMLCDs are ubiquitous in our everyday life. Figure 2.1 gives a brief historical overview of the most important TFT-based FPD applications. In large-screen TVs, smartphones, and tablets the display is arguably the most important component. FPDs also find new applications in infotainment systems, automotive, and household appliances. The latest displays offer a larger diameter screen, higher resolution, faster refresh rates, higher color accuracy, thinner form factor, and narrow bezel striving for the most immersive viewing experience. New material innovation is driven by head-mounted displays for virtual reality applications requiring very high pixel density (pixel per inch, ppi). AMOLED displays also require a higher performance TFT beyond that of an a-Si:H-based backplane.

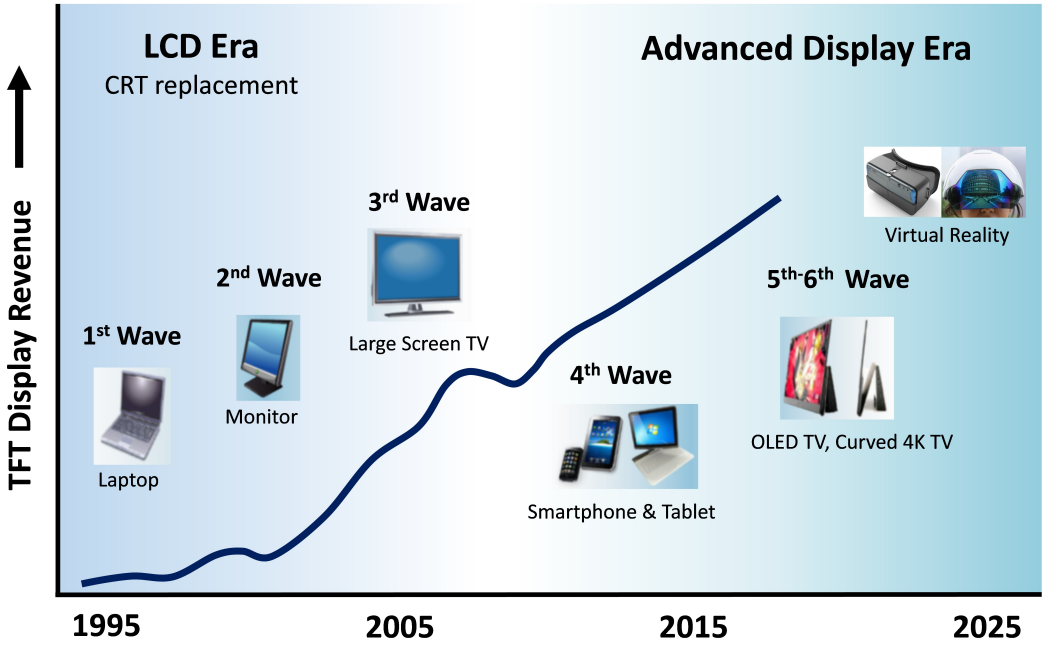

Figure 2.1: Timeline of TFT-based flat-panel display technologies at point of widespread adoption. With data from IHS DisplaySearch, Applied Materials, and Intel.

2.1.2 Pixel Circuit

TFTs are employed in the pixel circuit of the AMLCD backplane. Additionally, in the latest AMLCDs TFTs are sometimes used for the peripheral drive circuit using a so-called *gate driver on array* technology. In an AMLCD pixel circuit, the TFT adjusts the brightness of the RGB sub-pixel by controlling the orientation of the liquid-crystal which transmits light from the backlight. In contrast, in an AMOLED display the TFT adjusts the brightness of the sub-pixel by controlling the current passing through the OLED. Attached to each sub-pixel is a pixel circuit. One of the simplest circuits for an AMOLED pixel consisting of 2 transistors and 1 capacitor (2T1C) is shown in Fig. 2.2.

A circuit with the fewest devices and lines is almost always desired as it takes up

less area and is essential for achieving higher ppi. However, frequently more complex circuits must be used to compensate for non-uniformity and degradation of the TFT. The driving TFT in an AMOLED display is particularly sensitive to non-uniformity and degradation. A shift in the turn-on voltage can make a significant impact on the resulting drain current that is then supplied to the OLED. With a lower current the luminescence of the OLED is reduced, which results in brightness variation across the display.

In contrast, AMLCD operation involves a voltage-controlled technology so that no driving TFT is required in the pixel circuit. The requirements for uniformity and stability are not as stringent in an AMLCD as in an AMOLED display.

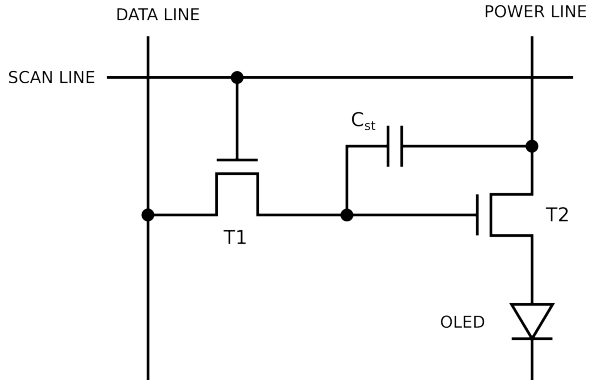

Figure 2.2: A simple pixel circuit for an AMOLED display. $T1$ is a switching transistor, $T2$ is a driving transistor, and C_{st} is a storage capacitor. Figure reproduced from Ref. [1].

2.1.3 Current TFT Semiconductors

The dominant TFT backplane material is a-Si:H. In 2012, the total TFT production capacity was approximately 210×10^6 m^2 and LTPS and Oxide technologies only contributed about 5 % (or 10×10^6 m^2) [18]. In recent years, LTPS and Oxide have

increased their market share. A summary of approximate application range for a-Si:H, LTPS and Oxide (a-IGZO) is given in Fig. 2.3. Excimer laser annealed (ELA) LTPS can provide the highest mobility and the option of CMOS circuitry, however, a-IGZO exhibits a lower OFF-current and is cheaper to fabricate than LTPS. New displays require an ever higher TFT mobility which is indicated by the dashed lines in Fig. 2.3 and described in the following.

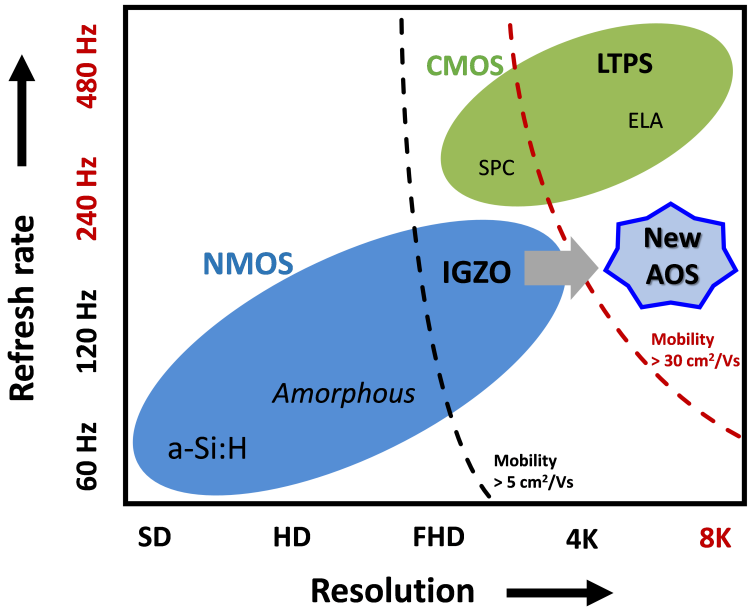

Figure 2.3: Current TFT semiconductors used in mass-production are a-Si:H, LTPS, and a-IGZO. Required mobility increases with refresh rate and resolution. Adapted from Kwon and Jeong [2].

One of the key parameters of a TFT is its carrier mobility. The general *square-law* relation describing the drain current of a FET is equal to

$$I_{DS} = \mu \frac{W}{L} C_{OX} (V_{GS} - V_{ON}) V_{DS} - \frac{V_{DS}^2}{2}, \tag{2.1}$$

where μ is the carrier mobility, W is the width of the channel, L is the gate length,

C_{OX} is the gate oxide capacitance per unit area, V_{GS} is the gate-source voltage, V_{ON} is the turn-on voltage of the TFT, and V_{DS} is the drain-source voltage.

The on-current I_{ON} is defined as the value of I_{DS} in a fully biased/fully-on state. A higher I_{ON} is always desired. The basic parameters for increasing I_{ON} are indicated in Eq. 2.1. Namely, for a given operating voltage (V_{GS} and V_{DS}) a higher I_{ON} can be achieved by increasing μ, or by increasing the W/L ratio.

To motivate the need for a higher mobility two scenarios are described in the following. First, the TFT has a higher mobility with all other parameters remaining unchanged. This results in a higher I_{ON} which in turn results in faster switching (charging of capacitances) and, finally, enables faster refresh rates of the display. Second, the TFT has a high mobility, and hence, I_{ON} is sufficiently large. Therefore, W can be reduced. This allows the manufacturer to make the TFT smaller which (a) is a prerequisite step for increasing the resolution of the display, or (b) results in the TFT taking up less area in the sub-pixel (higher aperture ratio, meaning less shadowing by the black matrix) which results in a wider viewing angle and increases the brightness of the sub-pixel. If the higher brightness is not desired, one can in turn dim the backlight or reduce the supply voltage to the OLED for an AMLCD and AMOLED display, respectively, effectively reducing power consumption.

2.2 Thin-Film Transistors

In the following, commonly used device structures and the general operation of a TFT are described. TFTs belong to the class of field-effect transistors (FET). They are three terminal devices. Namely, the three electrodes are gate, source, and drain. Additionally, a TFT needs a semiconducting channel layer and a substrate (typically

silicon or glass) to build the device upon. A current flowing from source to drain can be controlled by biasing the gate electrode (voltage control).

2.2.1 Device Structure

The four basic possible structures of a TFT are staggered top gate, coplanar top gate, staggered bottom gate, and coplanar bottom gate, shown in Fig. 2.4. The naming scheme refers to the position of the gate electrode (top/bottom) and the plane of the source and drain regions in reference to the channel (coplanar/staggered). The two bottom gate structures are sometimes referred to as inverted staggered and inverted coplanar TFT, respectively.

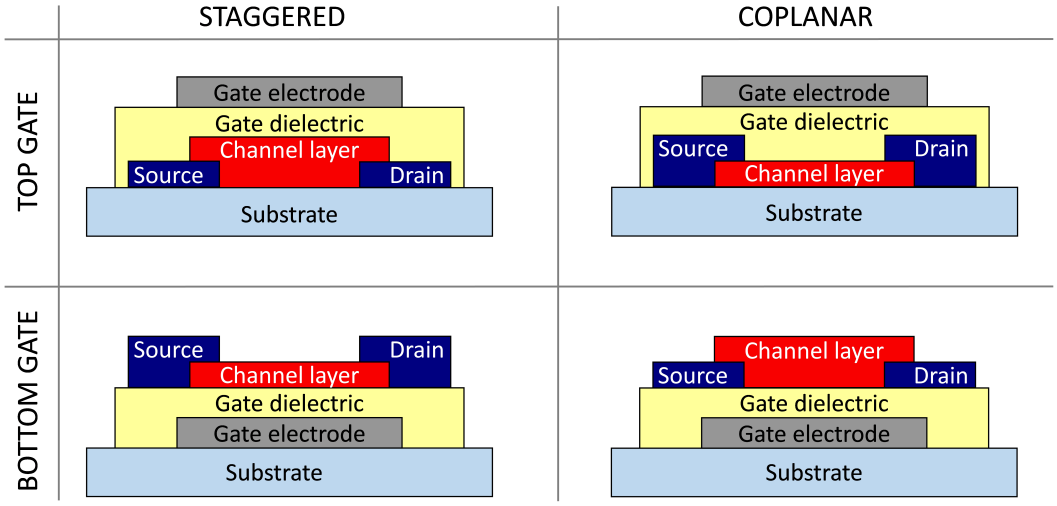

Figure 2.4: Staggered top gate, coplanar top gate, staggered bottom gate, and coplanar bottom gate device structures.

Each structure has its own advantages and disadvantages. The bottom gate structures need fewer mask steps and therefore, are easier and cheaper to fabricate. In a coplanar or staggered bottom gate structure the gate or the gate and source/drain

electrodes, respectively, are already deposited and patterned before the potentially delicate channel layer is deposited. This avoids exposure of the channel material to any of the previous processing steps, e.g., the use of certain etchants, energetic plasmas, and/or elevated temperatures. Furthermore, the channel is not in direct contact with the glass substrate. Therefore, any negative impact the substrate might have on device characteristics, e.g., any surface roughness or out-diffusion of elements like sodium which is used during the glass substrate manufacturing, is mitigated. Typically, a nitride/oxide buffer layer is used as a barrier between the substrate and the TFT [19]. Additionally for the case of oxide TFTs, no source/drain doping is required. However, the parasitic gate-source/drain overlap capacitances are higher in the bottom gate structure.

In a top gate device the channel layer is exposed on a planar surface. This is helpful for excimer laser annealing and source/drain doping via ion-implantation which is why the coplanar top gate structure is typically used for LTPS TFTs.

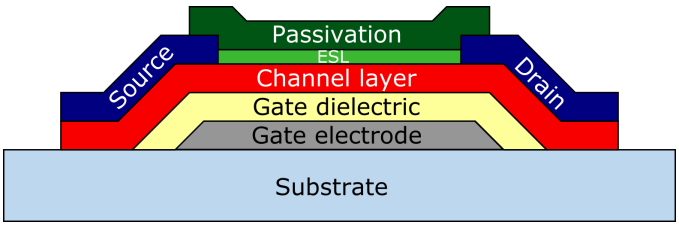

Figure 2.5: Staggered bottom gate TFT structure typically used in mass-production.

For mass-manufacturing, where reproducibility and reliability are crucial, several changes need to be made to the basic TFT structure. A staggered bottom gate TFT with an etch stop layer is shown in Fig. 2.5. It has tapered sidewalls for better step coverage [20], and a passivation layer to reduce degradation of the channel due to ambient conditions (e.g., gas adsorption). The AOS channel layer can be very

sensitive to etchants. The etch stop layer (ESL) aids in protecting the channel during source/drain patterning [21]. Fabrication without an ESL is called a back channel etch (BCE) type process.

2.2.2 Operation

TFTs are accumulation-mode devices meaning the conducting channel is formed by majority carriers, in contrast to the ubiquitous metal-oxide-semiconductor field-effect transistor (MOSFET) which forms an inversion channel (minority carriers). Commonly, the desired TFT behavior for application in the display backplane is enhancement-mode (normally-off) operation. The idealized enhancement-mode operation with flat-band conditions is described in the following and the corresponding energy band diagrams are shown in Fig. 2.6.

By applying a positive bias ($V_{GS} > 0$) electrons are accumulated at the insulator-semiconductor interface and a thin, conducting accumulation region forms in the semiconductor. Is a bias applied at the drain terminal simultaneously ($V_{DS} > 0$), then electrons get injected from the source contact, travel across the channel layer, and get extracted at the drain contact. As a consequence, current can flow from source to drain and the transistor is in the ON-state (Fig. 2.6(b)). In the OFF-state ($V_{GS} \leq 0$) the channel is non-conducting and no current (ideally) can flow between source and drain (Fig 2.6 (a) and (c)).

For a small applied drain voltage, an increase in V_{DS} results in a linear increase in I_{DS} (pre-saturation). With a further increase in V_{DS} beyond $V_{GS} - V_T$, the channel is *pinched-off* at the drain and I_{DS} saturates (saturation region).

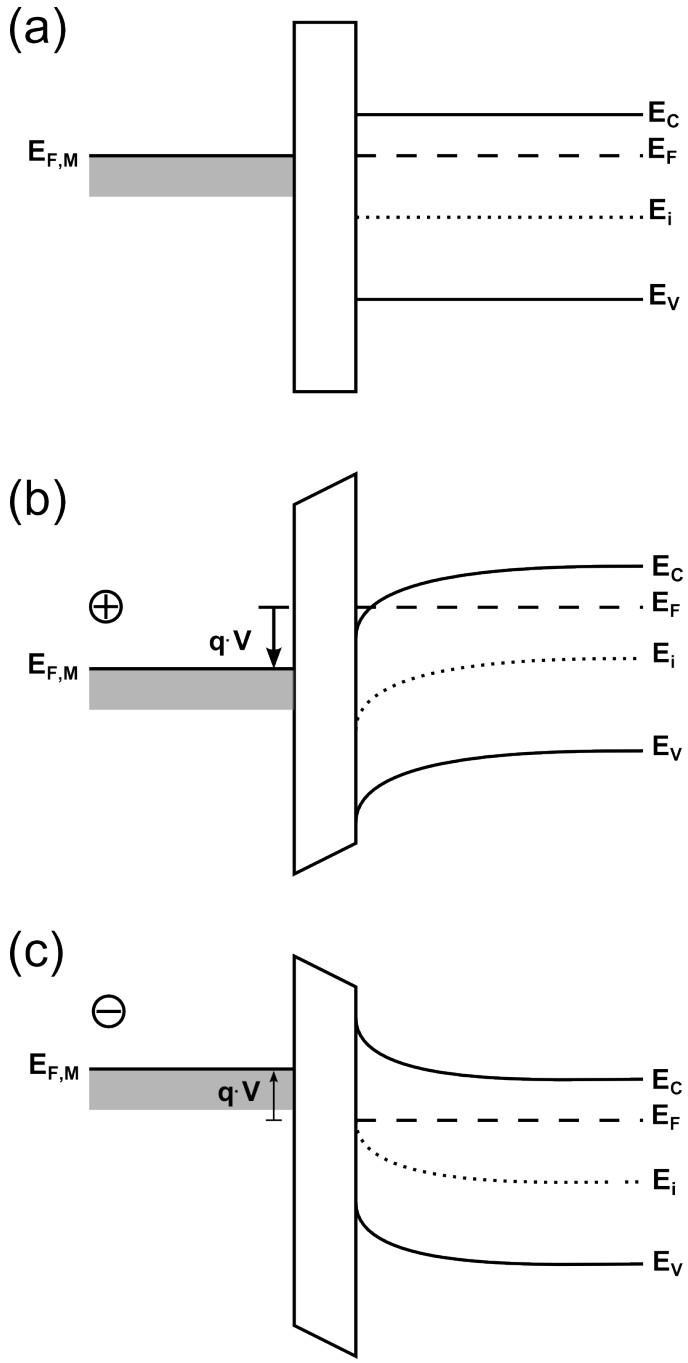

Figure 2.6: Energy band diagrams for a metal-insulator-semiconductor (M-I-S) capacitor. The n-type semiconductor is in (a) equilibrium when no bias is applied, (b) accumulation when a positive bias is applied, and (c) depletion when a negative bias is applied.

2.3 Amorphous Oxide Semiconductors

The first report on AOSs was published by Hosono et al. in 1996 [17]. The amorphous oxides $AgSbO_3$, Cd_2GeO_4, and Cd_2PbO_4 were investigated. It was found that these materials exhibited a relatively large Hall mobility, $\mu_{Hall} \approx 10$ cm^{2}V^{-1}s^{-1}. TCOs are closely related to AOSs and had been reported more than a decade earlier [22]. The difference is that TCOs like In_2O_3:Sn (ITO) are typically polycrystalline and have too many mobile carriers to be used as a semiconducting channel layer for a TFT. A part of the periodic table of elements was suggested for selecting cations for the design of an AOS, as shown in Fig. 2.7. These are elements with an $(n-1)d^{10}ns^0$ $(n \geq 4)$ electronic configuration.

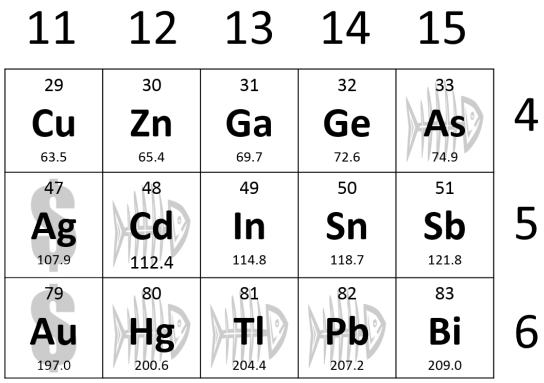

Figure 2.7: The portion of the periodic table proposed for selecting AOS cations. As, Cd, Hg, Tl, and Pb are usually not used due to their toxicity. Ag and Au are costly. Figure adapted from Refs. [3, 4].

An amorphous phase can be achieved by selecting two ore more cations having different oxide crystal structures, thereby resulting in a frustration of the lattice. Three typically used binary oxides are indium oxide (In_2O_3), zinc oxide (ZnO), and tin oxide (SnO_2) which are commonly found in the crystal structures of cubic mineral

bixbyite, hexagonal wurtzite, and tetragonal rutile [23]. The amorphous phase is metastable. AOSs remain amorphous until around 500 °C to 700 °C depending on the specific system. Beyond that temperature, crystallization and/or phase separation occurs.

In 2004, the first amorphous IGZO TFT was reported by the Hosono group [24]. The TFTs were fabricated on a flexible substrate (polyethylene terephthalate, PET), the IGZO channel layer was deposited by pulsed laser deposition, and a 140 nm thick Y_2O_3 layer was used as a gate insulator. The devices exhibited an on-to-off ratio of $I_D^{ON-OFF} \approx 10^3$, a mobility of $\mu_{FE} \approx 6$ cm^{2}V^{-1}s^{-1}, and a threshold voltage of $V_T = 1.6$ V.

The electrical characteristics of IGZO depend on the ratio of In_2O_3 to Ga_2O_3 to ZnO. The most common IGZO composition is $InGaZnO_4$, having a molar ratio of $In_2O_3/Ga_2O_3/ZnO$ of 1:1:2. The effect of varying the IGZO composition on the Hall mobility and carrier concentration is shown in Fig. 2.8. The mobility and carrier concentration tend to increase with higher In content. Going from the center point of the triangle of Fig. 2.8 to the bottom right corner (pure In_2O_3) the mobility increases by a factor of 3.8× while the carrier concentration increases by an enormous 100×.

AOSs have larger mobilities than that historically expected from an amorphous semiconductor. This expectation stems mainly from comparison to silicon, the most prominent semiconductor. The electron mobility of silicon decreases from ~1500 to ~1 cm^{2}V^{-1}s^{-1} when going from single crystal silicon to hydrogenated amorphous silicon. Silicon forms covalent bonds. These bonds are formed with highly directional sp^3 orbitals. For silicon precise orbital overlap is only possible in an ordered or, more specifically, in a crystalline structure [6], as indicated in Fig. 2.9(a),(b).

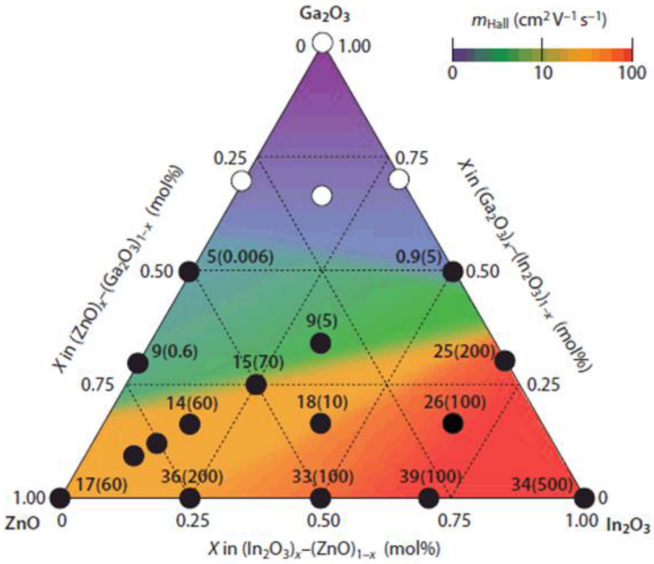

Figure 2.8: Hall mobility and carrier concentration of the In_2O_3-Ga_2O_3-ZnO system. The Hall mobility is in units of $cm^2V^{-1}s^{-1}$ and the carrier concentration (in parentheses) is in units of 10^{18} cm^{-3} [5].

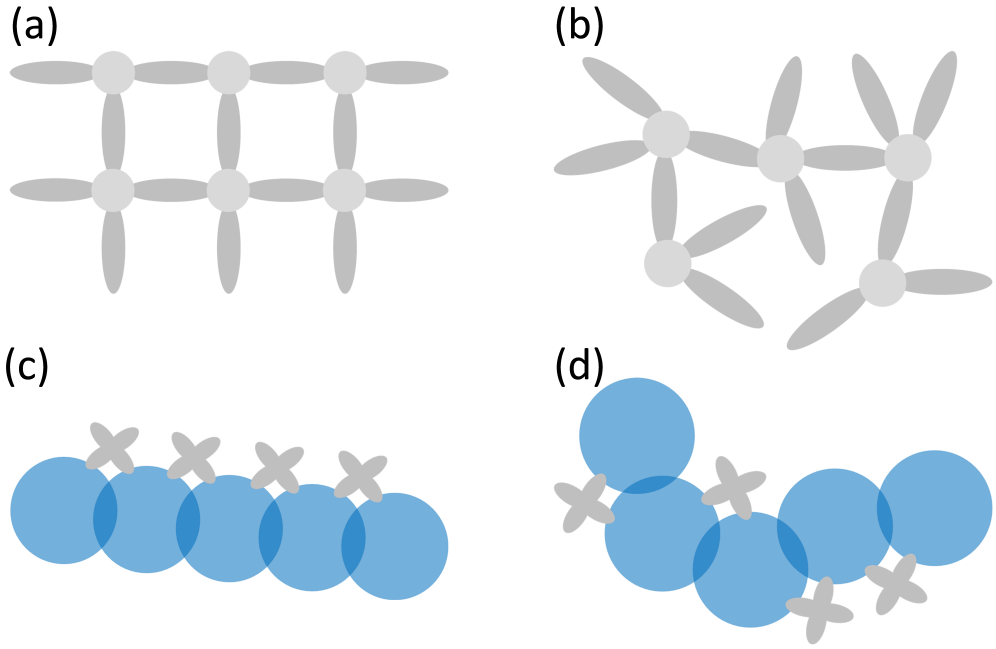

Figure 2.9: Schematic illustration of orbitals for (a) crystalline covalent, (b) amorphous covalent, (c) crystalline ionic, and (d) amorphous ionic semiconductors.

An AOS forms ionic bonds. Its conduction band is derived from large spherical metal s-orbitals. Directional order is not needed to have sufficient overlap between orbitals since the ionic radius of constituent cations is relatively large. Bonding in an ionic semiconductor is illustrated in Fig. 2.9(c),(d). Hence, AOSs are relatively insensitive to directional (bond angle and bond length) disorder. This gives rise to a fundamental difference in the sub-gap density of states (DOS) between a covalent and ionic amorphous semiconductor. The topic of amorphous semiconductor DOS and how it relates to the electron conduction is briefly introduced in the next section and is further discussed in Chapter 3.

2.3.1 Density of States

The type of bonding of the amorphous semiconductor directly influences the DOS. Moreover, the DOS profile determines the electrical and optical behavior of the semiconductor. The localized conduction and valance band band-tail states follow an exponential distribution and are defined according to the following equations

$$g_{TA}(E) = N_{TA} \exp\left(\frac{E - E_C}{W_{TA}}\right) \tag{2.2}$$

and

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_V - E}{W_{TD}}\right), \tag{2.3}$$

where g_{TA} (g_{TD}) is the total conduction (valence) band band-tail state density, N_{TA} (N_{TD}) is the peak density of acceptor (donor) band-tail states, and W_{TA} (W_{TD}) is

the conduction (valence) band Urbach energy. Common Urbach values for a-Si:H and a-IGZO are summarized in Fig. 2.10.

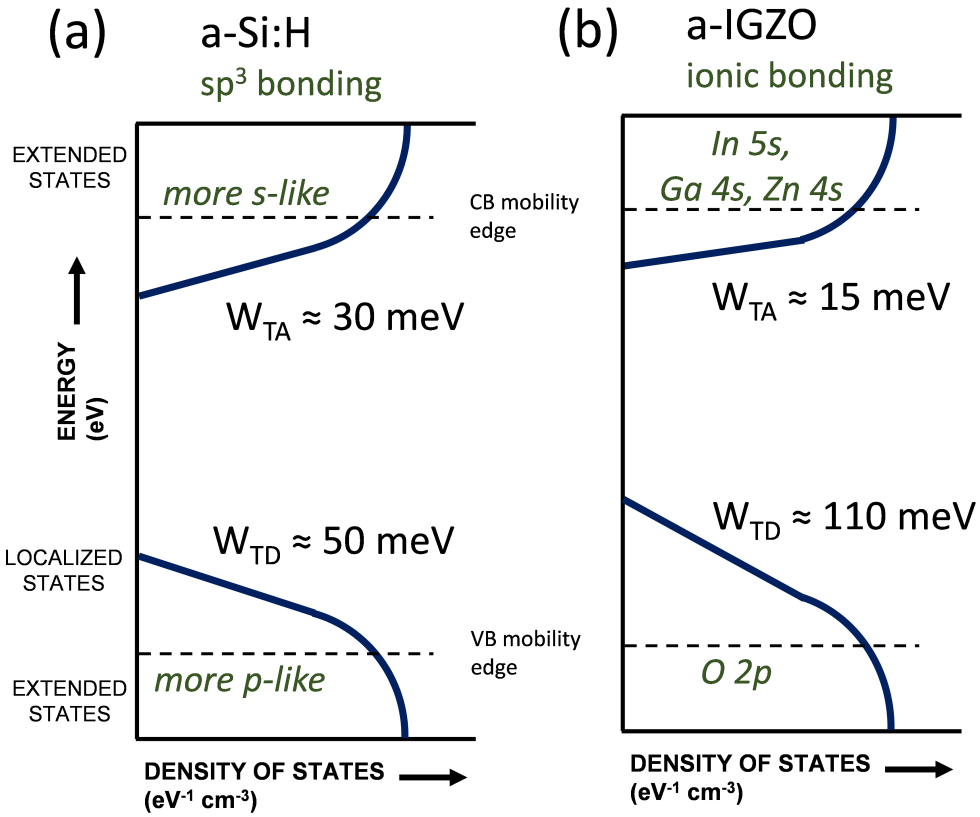

Figure 2.10: (a) a-Si:H and (b) a-IGZO band-tail state Urbach energy influenced by bonding type.

Knowledge about the DOS is crucial for complete understanding of device behavior and for use in AOS TCAD simulations. However, the DOS is very difficult to measure experimentally and several analytical techniques need to be combined to even attempt creating a complete DOS profile. As a result, the DOS of a-IGZO is still not completely understood, particularly the existence and shape of sub-gap states besides the band-tail states are highly debated. Two attempts at a complete experimental characterization of an AOS DOS are shown in Fig. 2.11.

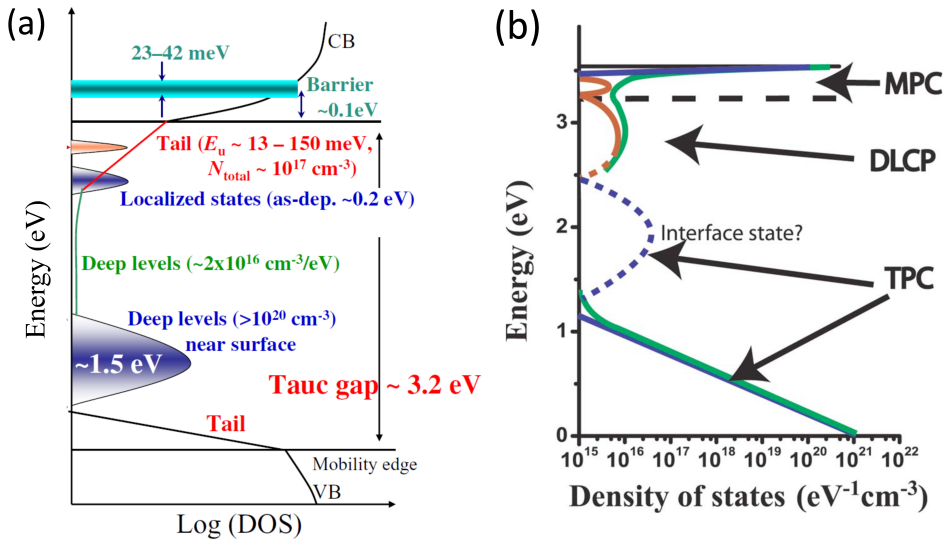

Figure 2.11: Proposed AOS DOS model for (a) a-IGZO [6, 7] and (b) a-ZTO [8].

The a-IGZO DOS in Fig. 2.11(a) was developed from C-V and TFT characterization, optical and hard X-ray photoemission spectroscopy, and density functional theory calculations. Three gaussian-like sub-gap features are indicated in this model. On the other hand, the amorphous zinc tin oxide (a-ZTO) DOS was determined from modulated photocurrent spectroscopy (MPC), drive level capacitance profiling (DLCP), and transient photocapitance (TPC) measurements performed on relatively thick, sputtered a-ZTO thin films. Comparing the zero-order a-IGZO DOS profile from Fig. 2.10(b) with the more complete DOS from Fig. 2.11(a), they match the band-tail states which are intrinsic to an amorphous semiconductor and relatively easy to explain, however, a multitude of other, extrinsic (gaussian) defect states are also possible as indicated in Fig. 2.11(a).

2.3.2 Free Carriers and Mobility

Amorphous IGZO and all AOSs that have been discovered to date are wide band gap, unipolar n-type semiconductors. No inversion, and no hole conduction and p-type doping in general has been achieved in a-IGZO. This is not too surprising considering the large defect density near the valence band mobility edge. Rather, a-IGZO is intrinsically n-type.

Experimentally it is possible to reduce the carrier concentration by increasing the oxygen partial pressure during the deposition process (or vice versa). Furthermore, gallium-rich IGZO compositions have a lower carrier concentration than indium-rich compositions (shown in Fig. 2.8) and thus, gallium seems to act as a carrier suppressor. Gallium bonds to oxygen more strongly than indium or zinc and may aid in reducing oxygen vacancies. Because of this experimental evidence, it is commonly postulated that oxygen vacancies act as a carrier generation site (donor state). Defect creation of an oxygen vacancy can be expressed as,

$$O_O^{\times} \rightleftharpoons V_O^{\cdot\cdot} + 2e^{'} + \frac{1}{2}O_2(g), \tag{2.4}$$

where $O_O^{\times}$ is a neutrally charged oxygen on an oxygen lattice site, $V_O^{\cdot\cdot}$ is a doubly positive charged vacancy on an oxygen site, $2e^{'}$ are two mobile electrons, and $\frac{1}{2}O_2(g)$ is a gaseous oxygen molecule stemming from the now unoccupied lattice site (vacancy). Hence, every oxygen vacancy donates two free electrons according to this model. Revisiting the DOS profile in Fig. 2.11(a), the deep levels near the valence band are often said to be the origin of oxygen vacancies, however, those levels seem too deep to act as an electron donor.

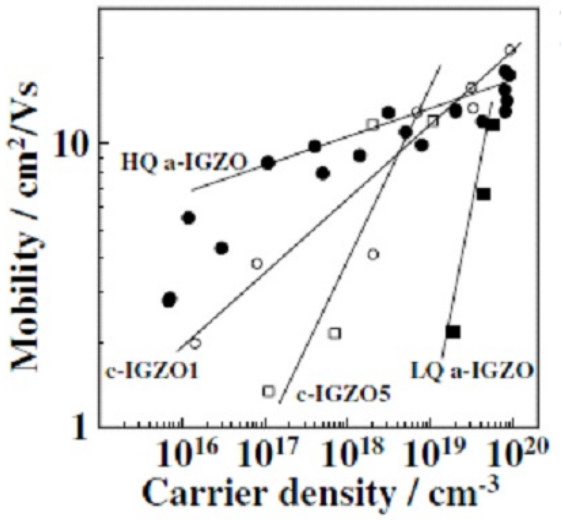

Figure 2.12: Hall mobility versus carrier concentration for crystalline and amorphous IGZO with varying deposition conditions [7].

The mobility and carrier concentration are strongly connected, as can be seen in Figs. 2.8 and 2.12. The mobility tends to increase with increasing carrier concentration. This is likely because of trap filling. For this, consider that the drift mobility in an amorphous semiconductor is often written as [16, 25, 26, 27]

$$\mu_{\text{drift}} = \left(\frac{n}{n + n_T}\right) \mu_0, \tag{2.5}$$

where n is the free electron concentration, n_T is the trapped electron concentration, and μ_0 is the trap-free drift mobility. However, the carrier concentration cannot be arbitrarily chosen. Rather, the carrier concentration in an AOS channel layer needs to be tightly controlled because it strongly influences the turn-on voltage of the TFT. Trapping in band-tail states and how it affects mobility is discussed in detail in Chapter 3.

2.4 High Mobility Reports

Hundreds of journal articles on the topic of AOSs have been published since 2003. An attempt was made to identify the reports claiming the highest electron mobilities from fabricated TFTs.

2.4.1 Single Active Layer TFTs

Figure 2.13 gives a summary of reported mobilities for single active layer (SAL) oxide TFTs, this includes AOSs such as a-IGZO as well as polycrystalline ZnO and In_2O_3. The field-effect or saturation mobility (whichever was given), the semiconductor used for the channel layer and its deposition method, the gate insulator, a comment (if applicable), and affiliation of the main authors of those 29 publications is tabulated in Table 2.1.

The majority of channel layers were deposited via sputtering and utilize a staggered bottom gate structure. A remarkable result are the sputtered In-Zn-O TFTs with top gate structure reported by Samsung Advanced Institute of Technology in 2009 and 2013 exhibiting a mobility of 115 [28] and 157 $cm^2V^{-1}s^{-1}$ [29], respectively.

Distinguishing between amorphous and polycrystalline reported experimental mobilities is difficult since adequate experimental evidence of a true amorphous phase is often not provided. Many of the reported channel layers likely lie in a grey area of nanocrystalline microstructures with grain sizes of ~2 to 5 nm. Even the polycrystalline channel layers still have relatively small grains < 50 nm.

Note that a high mobility result can be a consequence of measurement artifacts associated with employing a leaky gate insulator (GI), not properly accounting for

hysteresis, peripheral current flow in an unpatterned-channel TFT, depletion-mode operation, and/or simple incorrect calculation of the mobility [30, 31, 32, 33, 34]. A gate insulator of thermally oxidized silicon of 100 to 200 nm thickness is typically of very high quality and gate leakage current can be ruled out as a potential artifact to influence the apparent mobility. The double stack of PECVD Si_3N_4/SiO_2 often used in industry is also of high quality especially since the total insulator thickness is often $\geq$ 300 nm. Low temperature deposited (low-T.) or solution-processed insulators are frequently of lower quality. Unpatterned channel layers were an issue particularly in the early days of AOS research.

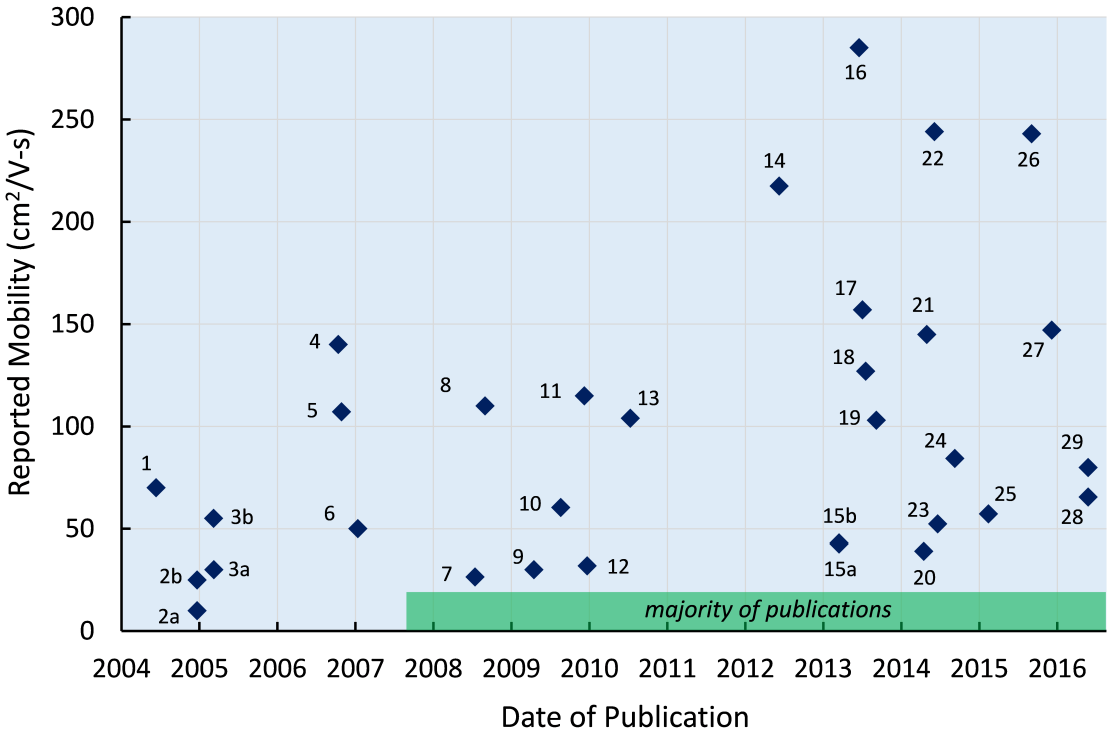

Figure 2.13: High mobility reports of SAL oxide TFTs. Numbers correspond to the ID column in Table 2.1.

Table 2.1: High mobility reports of SAL oxide TFTs.

ID	$\mu_{FE,sat}$ cm^2/Vs	Channel Layer	Dep. Method	Gate Insulator	Comment	Affiliation [Ref.]
1	70	Zn-O	sputt.[1]	therm. SiO_2	unpatterned	U. Lisbon [35]
2a	10	Zn-Sn-O	sputt.[1]	220 nm ATO[2]	E-mode	OSU (ECE) [36]
2b	25	Zn-Sn-O	sputt.[1]	220 nm ATO[2]	D-mode	OSU (ECE) [36]
3a	30	In-Zn-O	sputt.[1]	220 nm ATO[2]	E-mode	OSU (ECE) [37]
3b	55	In-Zn-O	sputt.[1]	220 nm ATO[2]	D-mode	OSU (ECE) [37]
4	140	In-O	IAD[3]	organic	leaky GI?	Northwestern [38]
5	107	In-Zn-O	sputt.[1]	220 nm ATO[2]	unpatterned?	U. Lisbon [39]
6	50	Zn-O	sputt.[1]	PECVD Si_3N_4	top gate	Kochi/Casio [40]
7	27	In-Zn-O	sputt.[1]	therm. SiO_2	-	Tokyo Tech. [41]
8	110	Zn-O	PLD[4]	PECVD SiO_2	-	AFRL [42]
9	30	In-Zn-Sn-O	sol.[5]	therm. SiO_2	unpatterned	OSU (ChE) [43]
10	60	Zn-O	sputt.[1]	100 nm Ta_2O_5	unpatterned	Shanghai [44]
11	115	In-Zn-O	sputt.[1]	PECVD SiO_2	top gate	Samsung [28]
12	32	Al-Sn-Zn-In-O	sputt.[1]	185 nm Al_2O_3	-	ETRI [45]
13	104	In-Zn-Sn-O	sol.[5]	organic	leaky GI	Northwestern [46]
14	218	In-Ga-Zn-O	sputt.[1]	PECVD Si_3N_4	Si cap	Chiao-T. U. [47]
15a	43	Zn-O-N	sputt.[1]	Si_3N_4/SiO_2	bottom gate	Samsung [48]
15b	44	In-Zn-O	sputt.[1]	Si_3N_4/SiO_2	bottom gate	Samsung [48]
16	285	Al-Zn-O	sputt.[1]	low-T. SiO_2	unp.+GI?	Peking U. [49]
17	157	In-Zn-O	sputt.[1]	PECVD SiO_2	top gate	Samsung [29]
18	127	In-O	sol.[5]	sol.[5] Al_2O_3	unp.+GI	KAUST [50]
19	103	Zn-O	sputt.[1]	150 nm Ta_2O_5	unpatterned	Manchester [51]
20	39	In-W-O	sputt.[1]	therm. SiO_2	-	NIMS [52]
21	145	Al-Zn-Sn-O	sputt.[1]	low-T. SiO_2	unp.?+GI?	Peking U. [53]
22	244	Hf-Zn-O	sputt.[1]	low-T. SiO_2	unp.+GI?	Peking U. [54]
23	52	In-Zn-Sn-O	sputt.[1]	PECVD SiO_2	-	Inha/Sam. [55]
24	84	In-Ga-Zn-O	sol.[5]	sol.[5] Al_2O_3	lower I_{GS}	UCLA [56]
25	57	In-O	sol.[5]	sol.[5] Al_2O_3	higher I_{GS}	CUHK [57]
26	243	In-O	MOCVD[6]	therm. SiO_2	-	Yat-sen [58]
27	147	Sn-O	PVD[7]	40 nm HfO_2	-	Chiao-T. U. [59]
28	66	CAAC-IGZO[8]	sputt.[1]	unspecified	top gate	SEL/Sharp [60]
29	80	MOx[9]	sputt.[1]	PECVD Si_3N_4	-	Cbrite [61]

[1]RF magnetron sputtering. [2]Superlattice of AlO_x and TiO_x. [3]Ion-assisted deposition. [4]Pulsed laser deposition. [5]Solution processing (typically spin-coating or ink-jet printing). [6]Metal-organic chemical vapour deposition. [7]Unspecified PVD method. [8]C-axis aligned crystalline In-Ga-Zn-O. [9]Unspecified oxide semiconductor.

2.4.2 Dual Active Layer TFTs

A dual active layer (DAL) TFT has a channel comprised of an interface layer adjacent to the gate insulator and a second (typically thicker) "bulk" layer, as illustrated in Fig. 2.14.

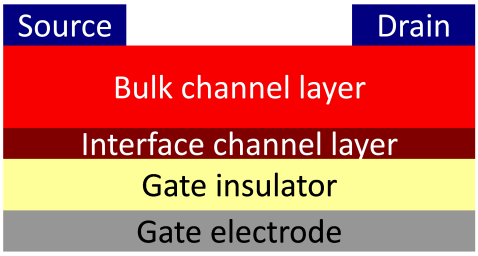

Figure 2.14: Dual active layer structure.

For the interface layer, a semiconductor is used which has a high mobility. The high mobility is often caused by a high carrier concentration (see Section 2.3.2). A TFT channel layer comprised of entirely this material would create a TFT that only turns-off at a very negative gate voltage or does not turn-off at all. To circumvent this issue, the high mobility material is combined with a material which has a modest mobility but has a sufficiently low carrier concentration to create an enhancement-mode TFT. The accumulation layer, where the majority of electron transport occurs, is very thin. Hence, the interface layer can be of similar thickness, typically ~5 nm, and still gain most of the benefits of the high mobility transport.

The interface and bulk layer can be comprised of different oxides, e.g., In-Sn-O and In-Ga-Zn-O for the interface and bulk layer, respectively, or of the same material. In the latter case, the carrier concentration and hence, mobility can be enhanced by, for example, adjusting the oxygen partial pressure during deposition. It is very desirable to deposit both layers without breaking vacuum to avoid any defects or contamination

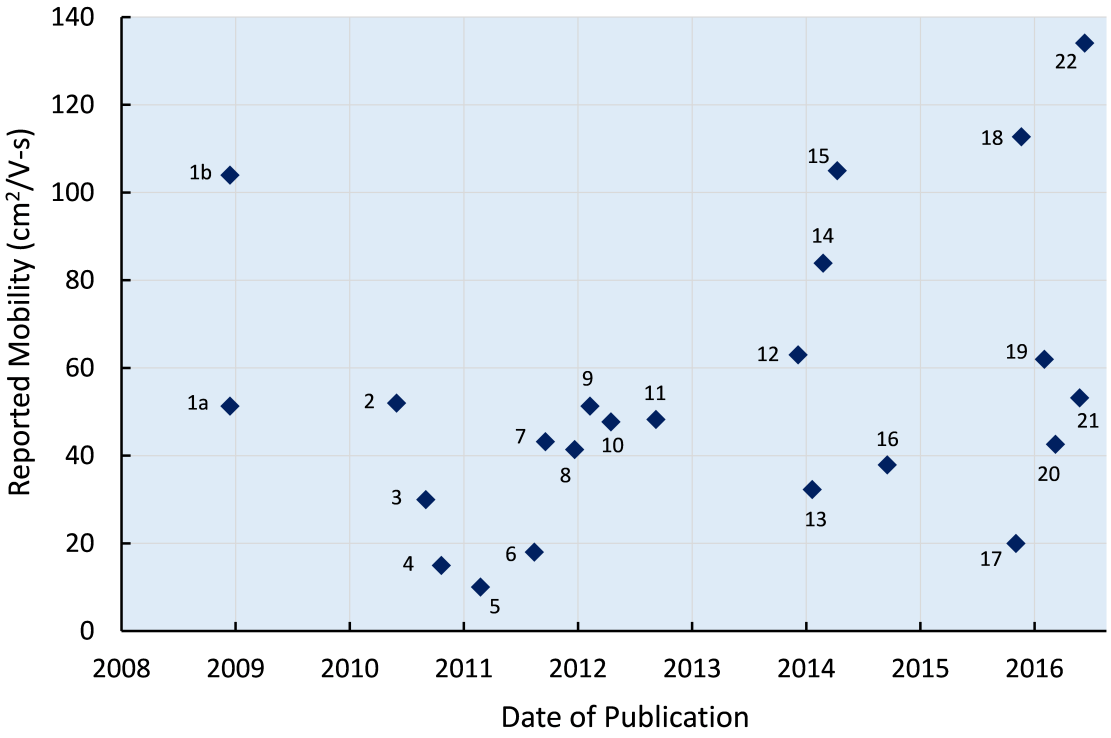

Figure 2.15: Reported mobility of sputtered DAL oxide TFTs. Numbers correspond to the ID column in Table 2.2.

at the interface between both layers.

A summary of reported mobilities for sputtered DAL oxide TFTs is shown in Fig. 2.15. Note that unlike the summary of SAL devices, which only included the devices with the highest mobilities, this is a complete list of reports on DAL oxide TFTs (to my best knowledge). Overall, the median mobility reported for DAL devices is much higher than that of SAL devices across all published results. Most of the reported DAL results seem reliable. The highest reported DAL mobility is smaller than the highest claimed SAL mobility.

Indium-rich oxides such as In-Sn-O and In-Zn-O are the most common choice for the interface layer and a-IGZO is favored for the bulk layer, as tabulated in Table 2.2.

Sputtering was identified early as the deposition method of choice and still produces the highest performance channel layers compared to other PVD methods as well as CVD techniques and solution processing. A chart detailing the deposition method of the channel layer for both the SAL and DAL literature is given in Appendix A.1.

Table 2.2: Summary of sputtered DAL oxide TFTs reported in the literature.

ID	$\mu_{FE,sat}$ **cm^2/Vs**	**Channel Layer I**	**Channel Layer B**	**Gate Insulator**	**Comment**	**Affiliation [Ref.]**
1a	51	In-Zn-O	In-Ga-Zn-O	PECVD SiO_2	-	Samsung [62]
1b	104	In-Sn-O	In-Ga-Zn-O	PECVD SiO_2	-	Samsung [62]
2	52	In-Sn-O	Zn-Sn-O	PECVD SiO_2	unpatt.	Hitachi [63]
3	30	In-Zn-O	In-Ga-Zn-O	PECVD SiO_2	-	Samsung [64]
4	15	Hf-In-Zn-O[1]	Hf-In-Zn-O[1]	Si_3N_4/SiO_2	-	Samsung [65]
5	10	Ga-Zn-O	In-Ga-Zn-O	therm. SiO_2	-	KIST [66]
6	18	In-Zn-O	In-Ga-Zn-O	PECVD SiO_2	-	ASU [67]
7	43	In-Sn-O	Zn-Sn-O	PECVD SiO_2	-	Inha/LG [68]
8	41	In-Zn-O	Hf-In-Zn-O	therm. SiO_2	D-mode	KIST [69]
9	51	In-O	Ga-O	ALD HfO_2	very thin	N. Taiwan [70]
10	48	In-Zn-O	In-Ga-Zn-O	PECVD SiO_2	-	Yonsei U. [71]
11	48	In-Zn-O	Hf-In-Zn-O	Si_3N_4/SiO_2	-	Samsung [72]
12	63	In-Ga-Zn-O	Ti-In-Ga-Zn-O	56 nm HfO_2	leaky GI?	Chiao-T. U. [73]
13	32	In-Zn-O	Zn-Sn-O	PECVD SiO_2	-	Inha/LG [74]
14	84	In-Ga-Zn-O[2]	In-Ga-Zn-O[2]	low-T. SiO_2	unp.+GI?	Peking U. [75]
15	105[3]	In-Sn-O	Zn-Sn-O	low-T. SiO_2	unp.+GI?	Peking U. [76]
16	38	In-O	In-Sn-O	sol.[5] Zr-O	-	Qingdao U. [77]
17	20	CAAC-IGZO[4]	In-Ga-Zn-O	therm. SiO_2	-	Cornell U. [78]
18	113	Al-Sn-Zn-O[2]	Al-Sn-Zn-O[2]	low-T. SiO_2	unp.+GI?	Peking U. [78]
19	62	In-Zn-O	In-Ga-Zn-O	unspecified	-	AMAT [79]
20	43	Zn-O:H	Zn-O	therm. SiO_2	-	Wuhan U. [80]
21	53	In-Zn-O	Al-In-Zn-Sn-O	PECVD SiO_2	-	ETRI [81]
22	134	Al-Sn-Zn-O	Al-Sn-Zn-O	low-T. SiO_2	leaky GI?	Peking U. [82]

[1]Varied Hafnium content. [2]Varied O_2 partial pressure. [3]A μ_{sat} of 292 $cm^2V^{-1}s^{-1}$ is also reported. [4]C-axis aligned crystalline In-Ga-Zn-O. [5]Solution processing.

CHAPTER 3: MOBILITY LIMITS CONSIDERATIONS

In this chapter, the mobility limiting scattering mechanisms for amorphous semiconductors and polar polycrystalline semiconductors are studied in the context of developing new high-performance TFT channel layer materials for large-area electronics. A physics-based model for electron and hole transport in an amorphous semiconductor is developed to estimate the mobility limits of amorphous semiconductor TFTs. The model involves band-tail state trapping of a diffusive mobility. Simulation reveals a strong dependence on the band-tail density of states. Employing this model leads to a predicted maximum mobility of ~71 $cm^2V^{-1}s^{-1}$ (~16 $cm^2V^{-1}s^{-1}$) for electrons (holes). A non-elemental, polar crystalline semiconductor may offer a higher mobility, but is fundamentally limited by polar optical phonon scattering. Any crystalline TFT channel layer for practical large-area applications will not be a single crystal but polycrystalline and, therefore, grain size and grain boundary dependent scattering will further degrade the transport properties.

This research is also discussed in the following publications:

K. A. Stewart, B.-S. Yeh, J. F. Wager, "Amorphous semiconductor mobility limits," *Journal of Non-Crystalline Solids* **432**, 196-199 (2016)

and

K. A. Stewart, J. F. Wager, "Thin-film transistor mobility limits considerations," *Journal of the Society for Information Display* **24**, 386-393 (2016).

3.1 Amorphous Semiconductor Mobility Limits

A main distinction between an amorphous and a crystalline material is that only a crystalline lattice exhibits long range order (atomic periodicity). However, both crystalline and amorphous materials have short range order. In an amorphous material, much insight can be gained from the chemical bonding of atoms, looking at nearest and next-nearest neighbor atoms (short range order). For example, a-Si:H has the same average coordination number, bond angle, and bond length values as single crystal silicon [16]. The key difference is the disorder of the amorphous phase giving rise to a distribution of coordination numbers, bond angles, and bond lengths.

The variability in bond angles and bond lengths give rise to band-tail states. It has been shown empirically that band-tails exhibit an exponential distribution of states. The slope of the exponential distribution is called the Urbach energy [83]. A density of states (DOS) distribution for a generic amorphous semiconductor is shown in Fig. 3.1. $g_C(E)$ and $g_V(E)$ are the conduction and valence band DOS, respectively. Band-tail states are acceptor-like for the conduction band [$g_{TA}(E)$] and donor-like for the valence band [$g_{TD}(E)$]. Band-tail states trap free carriers, which degrades the transport performance, as discussed in the following.

The drift mobility of an n-type amorphous semiconductor is often written as, [16, 25, 26, 27]

$$\mu_{\text{drift}} = \left(\frac{n}{n + n_T}\right) \mu_0, \tag{3.1}$$

where n is the free electron concentration, n_T is the trapped electron concentration, and μ_0 is the trap-free drift mobility.

If μ_0 is envisaged as a diffusive mobility in which *"It would be more accurate to de-*

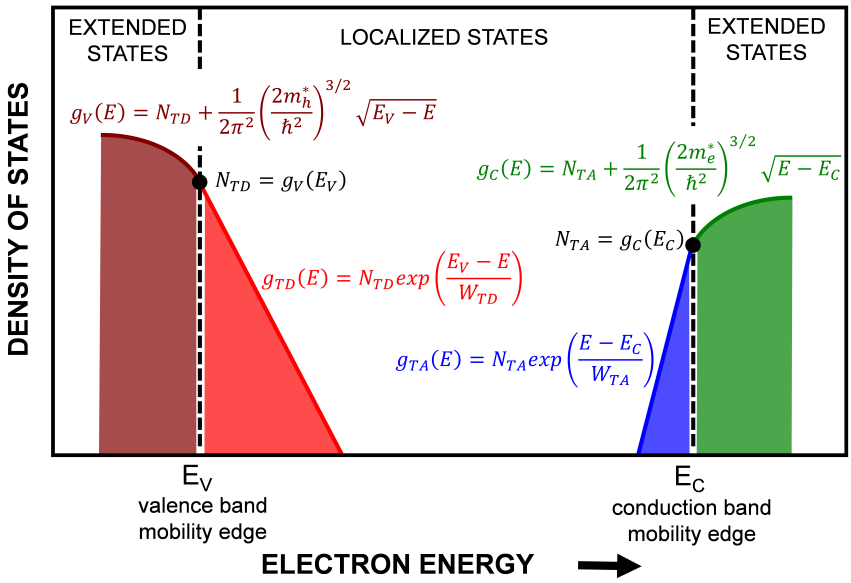

Figure 3.1: Amorphous semiconductor density of states distribution and defining equations.

scribe the carriers as almost continuously under the influence of the scattering centers so that their motion would be more like Brownian motion than wave propagation."[84] then μ_0 may be derived from, [16, 26, 27]

$$\mu_0 = \frac{qD}{k_B T}, \tag{3.2}$$

where the diffusion constant, D, is given by

$$D = \frac{\hbar}{6m_e^*}. \tag{3.3}$$

This results in

$$\mu_0 = \frac{q\hbar}{6m_e^* k_B T}, \tag{3.4}$$

where q is the elementary charge, $\hbar$ is the reduced Planck constant, k_B is the Boltz-

mann constant, m_e^* is the electron effective mass, and T is the temperature. Note that due to the complicated nature of electron motion near the mobility edge, Eq. 3.4 is only valid for transport near room temperature (T = 300 K). Figure 3.2 shows the effect of the effective mass assumption on the resulting diffusive mobility, μ_0. The range of typical effective mass values from the literature for a-Si:H, a-IGZO and a best-case semiconductor (explained below) are indicated in Fig. 3.2 and tabulated in Table 3.2.

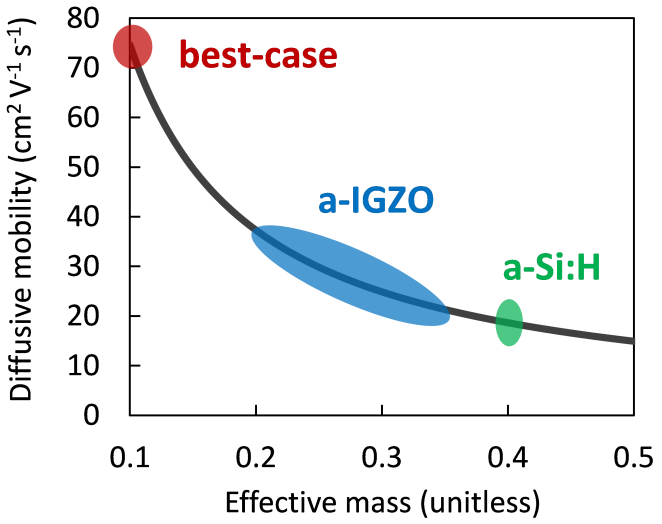

Figure 3.2: Diffusive mobility, μ_0, as a function of effective mass, m_e^*, at room temperature (T = 300 K).

Next, to evaluate the μ_{drift} expression given in Eq. 3.1, the free and trapped electron concentrations can be obtained via,

$$n = \int_{E_C}^{\infty} g_C(E) f(E) dE, \tag{3.5}$$

and

$$n_T = \int_{E_V}^{E_C} g_{TA}(E) f(E) dE, \tag{3.6}$$

respectively, where E_C and E_V are the conduction and valence band mobility edges, respectively, and f is the Fermi-Dirac occupancy function.

Equation 3.1 is appropriate for describing electron conduction in the accumulation layer of a TFT operating at a gate voltage above threshold, where the channel current is dominated by drift, but is not appropriate at sub-threshold gate voltages since diffusion dominates [3]. Thus, by introducing a diffusion mobility given by,

$$\mu_{\text{diff}} = \mu_{\text{drift}} \frac{n}{N_C}, \tag{3.7}$$

where N_C is the conduction band effective density of states,

$$N_C = 2 \left(\frac{2\pi m_e^* k_B T}{h^2} \right)^{\frac{3}{2}}, \tag{3.8}$$

the amorphous semiconductor electron mobility arising from drift and/or diffusion is equal to

$$\mu^{-1} = \mu_{\text{drift}}^{-1} + \mu_{\text{diff}}^{-1}. \tag{3.9}$$

To obtain the gate voltage dependence of the mobility, we employ a charge-sheet model in which the number of induced carriers is given by

$$n_{\text{ind}} = n + n_T = \left(\frac{C_{\text{OX}} V_{\text{G}}}{q} \right)^{3/2}, \tag{3.10}$$

where C_{OX} is the gate insulator capacitance density and V_G is the applied gate voltage. For the simulation shown herein, C_{OX} is equal to 34.5 nF/cm^2, which corresponds to a gate insulator of 100 nm of silicon dioxide.

The n-type amorphous semiconductor mobility transport model is summarized in

Table 3.1: Amorphous semiconductor mobility assessment (n-type case).

SUMMARY OF TRANSPORT MODEL EQUATIONS	
(i)	$\mu_{\text{drift}} = \left(\frac{n}{n+n_T}\right)\mu_0$
(ii)	$\mu_0 = \frac{q\hbar}{6m_e^* k_B T}$
(iii)	$n = \int_{E_C}^{\infty} g_C(E) f(E) dE$ and $n_T = \int_{E_V}^{E_C} g_{TA}(E) f(E) dE$
(iv)	$g_{TA}(E) = N_{TA} \exp\left(\frac{E-E_C}{W_{TA}}\right)$
(v)	$g_C(E) = N_{TA} + \frac{1}{2\pi^2}\left(\frac{2m_e^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E-E_C}$
(vi)	$\mu_{\text{diff}} = \mu_{\text{drift}}\frac{n}{N_C}$
(vii)	$N_C = 2\left(\frac{2\pi m_e^* k_B T}{h^2}\right)^{\frac{3}{2}}$
(vii)	$\mu^{-1} = \mu_{\text{drift}}^{-1} + \mu_{\text{diff}}^{-1}$
(ix)	$n + n_T = \left(\frac{C_{\text{OX}} V_{\text{G}}}{q}\right)^{3/2}$

Table 3.1. An analogous set of equations involving p, p_T, m_h^*, E_V, g_{TD}, N_{TD}, W_{TD}, and N_V is developed to describe hole transport in a p-type amorphous semiconductor, where the subscript TD denotes an exponential distribution of donor-like valence band-tail states [3].

First considering the electron (n-type) case, Fig. 3.3 shows mobility trends for three channel layers. The three semiconductors considered are a-Si:H, a-IGZO, and a best-case material that is our estimate of the upper limit of AOS mobility. Note that these semiconductor transport curves are determined by specifying only the temperature, $T = 300$ K, and three material parameters, the electron effective mass, m_e^*, the peak density of acceptor-like band-tail states, N_{TA}, and the conduction band-tail slope, W_{TA} (n-type case). The m_e^*, N_{TA}, and W_{TA} values employed to generate the curves shown in Fig. 3.3 are summarized in Table 3.2.

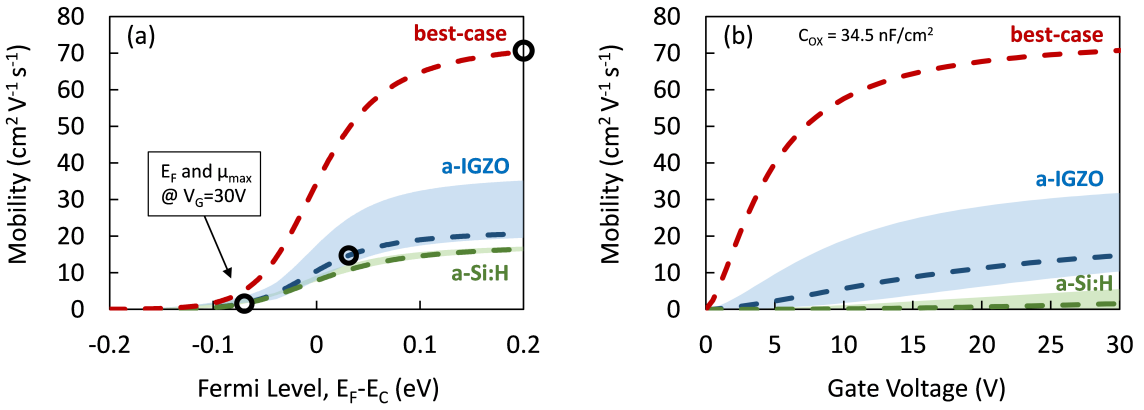

Figure 3.3: Electron (n-type) mobility as a function of (a) Fermi level position and (b) gate voltage. The dashed line corresponds to the typical values specified in Table 3.2 and the shaded areas bound the low/best range values.

In the mobility vs. Fermi level curve (Fig. 3.3(a)) we assume that the Fermi level can be freely positioned beyond the conduction band mobility edge into the extended states. However, in a real device this is not necessarily the case. The Fermi level

is modulated by the applied gate voltage and the extent of the Fermi level shift is determined by band-tail trapping. As a consequence, while in Fig. 3.3(a) a-Si:H and a-IGZO have comparable maximum mobilities (for the dashed line typical cases), in Fig. 3.3(b) there is a significant difference. Amorphous IGZO is superior to a-Si:H partly because the Fermi level can be modulated into the extended states (see black circles shown in Fig. 3.3(a)). For the best-case amorphous semiconductor, trap-related mobility degradation is greatly reduced and the Fermi level moves far beyond the mobility edge (see black circle to the far right shown in Fig. 3.3(a)).

The quality of the model clearly depends on the accuracy of the three input parameters. Amorphous silicon has been researched for decades and as a result the values for m_e^*, N_{TA}, and W_{TA} appear to be fairly well established. This is indicated by the narrow shaded areas in Figs. 3.2 - 3.4, which cover an upper and lower boundary of values commonly reported in the literature, as tabulated in Table 3.2. The uncertainty of the estimate for a-IGZO mainly originates from the variation in the effective mass, as shown in Fig. 3.2, whereas the given lower/typical/upper values in the band-tail trap density (N_{TA} and W_{TA}) have a comparatively small effect on the difference of lower/upper bounds of mobility for a-IGZO. The typical maximum mobility (at $V_G = 30$V) of ~1 and ~15 $\mathrm{cm^2V^{-1}s^{-1}}$ for a-Si:H and a-IGZO, respectively, agrees well with experimental results.

The material parameters for the best-case estimate are certainly difficult to predict. However, we think that a value of 0.1 for the effective mass truly is an optimistic best-case estimate. Hautier et al. [85] conducted an exhaustive computational screening study of binary and ternary oxides from the periodic table, identifying $BaSnO_3$ as the oxide with the smallest theoretical relative effective mass of 0.13. They also note

that the primary AOS/TCO candidates based on In_2O_3, ZnO, and SnO_2 already have remarkably small effective masses and, therefore, it is unlikely to find an oxide with a significantly smaller effective mass. It has been reported that perfect, defect-free single crystal semiconductors have an Urbach energy on the order of 5-10 meV caused by thermal disorder in the lattice [86, 87, 88]. Hence, our lower estimate of 10 meV for W_{TA} is based on the fact that even if compositional and spatial disorder are extraordinarily small, thermal disorder will yield a non-negligible band-tail slope. Values for N_{TA} are difficult to obtain experimentally and as a result are rarely reported. We assume a best-case estimate of $N_{TA} = 10^{19}\text{cm}^{-3}\text{eV}^{-1}$ which is smaller than what is commonly reported in the literature. We also note that a smaller (larger) N_{TA} tends to primarily increase (decrease) the slope of the mobility curve in Fig. 3.3(b) rather than affecting the peak mobility.

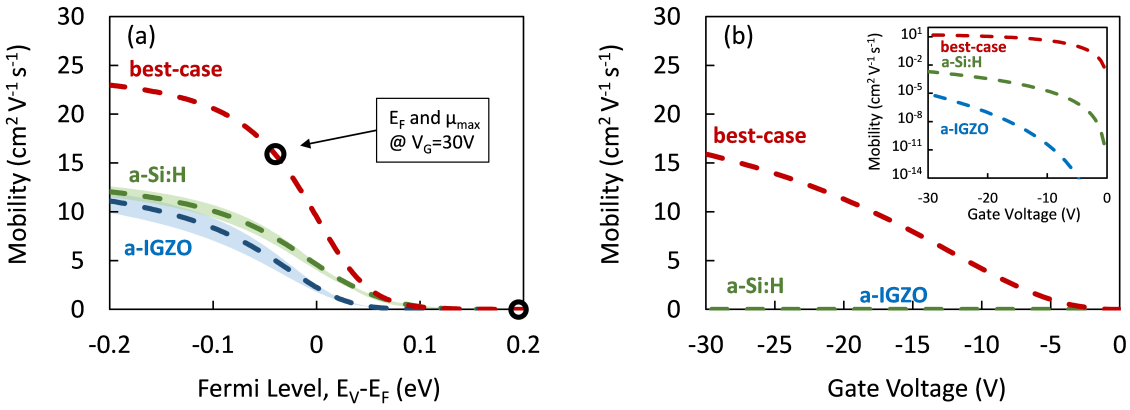

Figure 3.4: Hole (p-type) mobility as a function of (a) Fermi level position and (b) gate voltage. The dashed line corresponds to the typical values specified in Table 3.2 and the shaded areas bound the low/best range values. Inset shows mobility on a log-scale (low/best range bound omitted for clarity).

Next considering the hole (p-type) case, Fig. 3.4 shows the mobility in terms of the hole effective mass, the peak density of donor-like band-tail states, N_{TD}, and the

valence band-tail slope, W_{TD}. Amorphous IGZO has a large valence band Urbach energy of 110 meV. This means that even at a large applied gate voltage of 30 V, the Fermi level is still far from the mobility edge (see black circle to the far right, as shown in Fig. 3.4(a)). Hence, the hole mobility for a-IGZO is abysmal. For the best-case amorphous semiconductor estimate, extended state transport is achieved. However, keep in mind that $m_h^* = 0.3$ and $W_{TD} = 30$ meV (from Table 3.2) is extremely optimistic and actual material development may never achieve this.

The conduction and valence band for a-Si:H are derived from sp^3 hybridized orbitals. AOS s-orbitals forming the conduction band are large, spherically symmetrical, and relatively insensitive to disorder compared to p-orbitals which are highly directional. Note that disorder increases with increasing p-bonding character and the Urbach energy increases with increasing disorder. In fact, the magnitude of the Urbach energy is a good indicator of the amount of disorder in an amorphous semiconductor (see Section 3.1.1). Coming back to a-Si:H bonding, the conduction band has slightly more s-like character, resulting in a smaller Urbach energy compared to that of the valence band. For a-IGZO this disorder asymmetry is much more pronounced as the conduction band is derived from In 5s, Ga 4s, and Zn 4s metal cations, resulting in a very small conduction band Urbach energy. However, the valence band is derived from oxygen 2p orbitals, giving rise to a very large valence band Urbach energy and a very low hole mobility, as shown in the transport simulation of Fig. 3.4.

It now becomes apparent why all oxide semiconductors with O 2p orbital derived valence bands have a very low hole mobility; the band-tail trap density is simply too large. Very few oxides have valence bands that are not based on O 2p orbitals [89]. Stannous oxide, SnO, and cuprous oxide, Cu_2O, have Sn 5s/O 2p hybridized and

mostly Cu 3d-derived valence bands, respectively [90]. However, while large Hall mobilities for Cu_2O have been reported (see Table 3.4), the TFT mobilities for Cu_2O and SnO are still quite low [91, 92]. In addition, their band gaps are too small (0.7 and 2.3 eV, respectively [93]) to provide the very low OFF-current that is so highly valued in an AOS TFT.

Concluding this section, a physics-based model for mobility in an amorphous semiconductor is developed. The mobility is strongly degraded by band-tail trapping. Specifically comparing a-Si:H and a-IGZO, they have similar values of m^* and, therefore, similar values for the trap-free diffusive mobility μ_0 (see Fig. 3.2 and Table 3.2). However, the maximum TFT (gate voltage-dependent) mobility is strongly influenced by the band-tail trap density, resulting in a much lower mobility for n-type a-Si:H. Lastly, an oxide-based CMOS-like technology seems very challenging due to poor p-type performance.

Table 3.2: Amorphous semiconductor transport parameters. ~ indicates that this value is not based on a value reported in the literature; rather, it is a crude estimate.

Semiconductor	**Range**	$\mathbf{m^*_{e,h}}$ (m_0)	$\mathbf{N_{TA,D}}$ ($cm^{-3}eV^{-1}$)	$\mathbf{W_{TA,D}}$ (meV)	μ_0 ($cm^2V^{-1}s^{-1}$)	$\mu_{\mathbf{max\ @\ 30\ V}}$ ($cm^2V^{-1}s^{-1}$)	$\mathbf{E_{F,max\ @\ 30\ V}}$ (eV)
ELECTRONS							
a-Si:H	best	0.4 [16]	1.0×10^{21} [94]	20 [95]	18.7	5.5	$E_C - 0.03$
a-Si:H	typical	0.4 [16]	2.0×10^{21} [96]	30 [97]	18.7	1.6	$E_C - 0.07$
a-Si:H	low	0.4 [16]	5.0×10^{22} [97]	35 [98]	18.7	0.05	$E_C - 0.20$
a-IGZO	best	0.20 [99]	4.23×10^{19} [100]	11 [100]	37.3	31.8	$E_C + 0.09$
a-IGZO	typical	0.34 [101]	1.55×10^{20} [102]	13 [102]	22.0	14.7	$E_C + 0.03$
a-IGZO	low	0.35 [103]	$\sim 2.0 \times 10^{20}$	~30	21.3	10.4	$E_C + 0.02$
best-case	-	~0.1	$\sim 1.0 \times 10^{19}$	~10	74.6	70.7	$E_C + 0.21$
HOLES							
a-Si:H	best	~0.5	2.0×10^{21} [96]	45 [98]	14.9	0.13	$E_V + 0.10$
a-Si:H	typical	~0.5	1.0×10^{22} [97]	50 [97]	14.9	2.1×10^{-3}	$E_V + 0.20$
a-Si:H	low	~0.5	$\sim 5.0 \times 10^{22}$	~60	14.9	1.2×10^{-6}	$E_V + 0.33$
a-IGZO	best	~0.5	5.0×10^{20} [103]	~100	14.9	3.6×10^{-3}	$E_V + 0.12$
a-IGZO	typical	~0.5	9.3×10^{20} [103]	110 [8]	14.9	8.8×10^{-6}	$E_V + 0.21$
a-IGZO	low	~0.5	1.6×10^{21} [103]	~140	14.9	7.2×10^{-11}	$E_V + 0.37$
best-case	-	~0.3	$\sim 1.0 \times 10^{20}$	~30	24.8	15.9	$E_V - 0.04$

3.1.1 Quantifying Amorphous Semiconductor Disorder

The magnitude of the Urbach energy is a measure of disorder in an amorphous semiconductor [16, 26, 27]. Soukoulis et al. [104] show that (for acceptor-like conduction band-tail states) the disorder potential variability, W^2, is given by,

$$W^2 \approx 8\pi \frac{\hbar^2}{mL^2} W_{TA} \approx 0.03\ W_{TA}\ (\text{meV}), \tag{3.11}$$

where m is the electron rest mass and L is a disorder potential correlation factor on the order of atomic dimensions, $L \approx 0.25$ nm, an average inter-atomic distance. A tabulation of W, the disorder potential standard deviation, for the three discussed semiconductors a:Si:H, a-IGZO, and best-case, is given in Table 3.3. Note that W_{TA} and W are two different but related parameters for estimating the extent of disorder in an amorphous semiconductor.

An alternative new method to quantify amorphous semiconductor disorder is to calculate the total band-tail trap density, n_{total}, in the sub-bandgap region. For electron transport, n_{total} is equal to

$$n_{\text{total}} = \int_{E_V}^{E_C} g_{TA}(E) dE = N_{TA} W_{TA}. \tag{3.12}$$

As summarized in Table 3.3, the mobility significantly improves for disorder values smaller than ~0.9 eV and ~$1 \times 10^{19}\text{cm}^{-3}$ for W and n_{total}, respectively.

Both methods, Eqs. 3.11 and 3.12, depend on the Urbach energy, W_{TA}, emphasizing the key role of the Urbach energy in assessing amorphous semiconductor transport. Figure 3.5 shows the trend of decreasing mobility with increasing Urbach energy using the simulation program.

Table 3.3: Summary of amorphous semiconductor disorder parameters and resulting mobility where W and n_{total} are the disorder potential standard deviation and the total band-tail trap concentration, respectively. The values given for $\text{N}_{\text{TA,D}}$ and $\text{W}_{\text{TA,D}}$ correspond to the *typical* range as tabulated in Table 3.2.

Semiconductor	$\mathbf{N_{TA,D}}$ ($\text{cm}^{-3}\text{eV}^{-1}$)	$\mathbf{W_{TA,D}}$ (meV)	**W** (eV)	n_{total} (cm^{-3})	$\mu_{\text{max @ 30 V}}$ ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)
ELECTRONS					
a-Si:H	2.0×10^{21}	30	0.95	6×10^{19}	1.6
a-IGZO	1.55×10^{20}	13	0.62	2×10^{18}	14.7
best-case	1.0×10^{19}	10	0.55	1×10^{17}	70.7
HOLES					
a-Si:H	1.0×10^{22}	50	1.2	5×10^{20}	2.1×10^{-3}
a-IGZO	9.3×10^{20}	110	1.8	1×10^{20}	8.8×10^{-6}
best-case	1.0×10^{20}	30	0.95	3×10^{18}	15.9

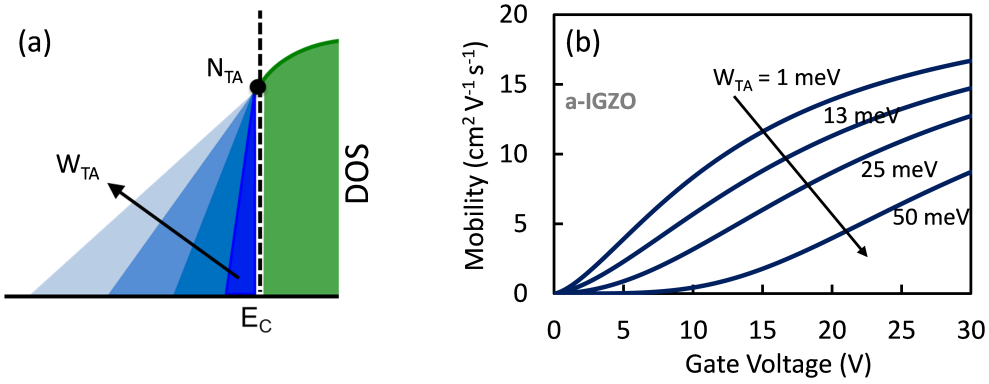

Figure 3.5: (a) Increasing conduction band Urbach energy trend and (b) simulation of a-IGZO mobility while varying the Urbach energy.

3.1.2 Interactive Simulation Program

The mathematical software program MATLAB was used to numerically solve the device physics equations of Table 3.1. An interactive tool of the amorphous semiconductor transport simulation was published on nanoHUB. The tool allows the user to input custom material parameters and calculates the mobility as a function of Fermi level position or gate voltage as well as the disorder parameters of Section 3.1.1. A graphical user interface (GUI) was developed to facilitate the use of the amorphous semiconductor transport model. The GUI was created using the Rappture Toolkit [105] which is provided by nanoHUB and a screenshot of the simulator is shown in Fig. 3.6. The Rappture Builder program can generate code to interface with several programming languages such as C, Python, and MATLAB. As of July 2016, the tool has been used for 296 simulations and the program code can be freely downloaded [9].

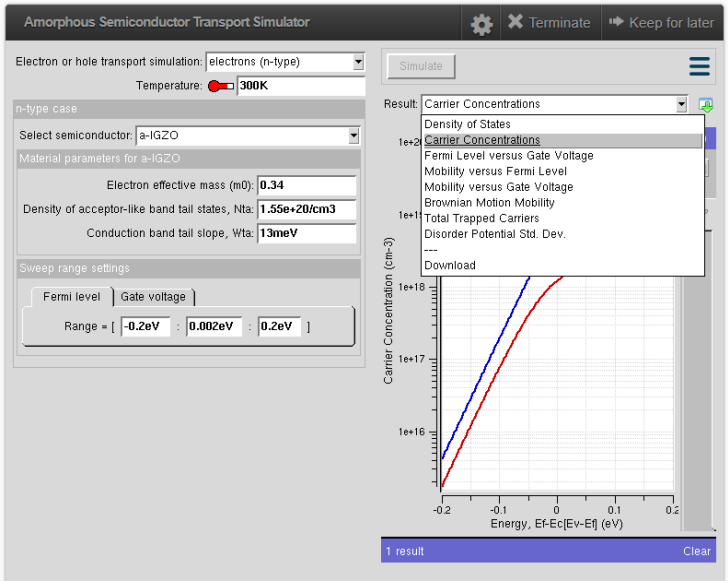

Figure 3.6: Screenshot of the Amorphous Semiconductor Transport Simulator deployed on nanoHUB [9].

3.2 Single-Crystal Polar Semiconductor Mobility Limits

As discussed in Section 3.1, the mobility limits of an amorphous semiconductor are estimated to be ~71 $cm^2V^{-1}s^{-1}$ (~16 $cm^2V^{-1}s^{-1}$) for electrons (holes). If a display-based, large-area electronics application requires a semiconductor mobility exceeding these limits, a crystalline semiconductor must be employed. The obvious present-day choice is low-temperature polycrystalline silicon (LTPS). However, suppose that a project of exploratory development was to be undertaken to search for a new type of high-performance semiconductor. Moreover, suppose that this search was constrained to exclude the use of elemental semiconductors (e.g., Si or Ge). The following considerations in this section, as well as Section 3.3, pertain to this proposed project.

All non-elemental semiconductors have some ionic bonding character and, therefore, are considered polar. Polar optical phonon (POP) scattering typically determines the upper limit in mobility in a polar semiconductor at room temperature [106]. This assumes that the semiconductor is intrinsic (unintentionally doped). The POP-determined upper mobility limit for a given material can be estimated by knowing four material properties: the conductivity effective mass, the low-frequency (static) and high-frequency (optical) dielectric constants, and the optical phonon energy.

The POP momentum relaxation time is defined as [106]

$$\tau_{\mathrm{m}}(E) = \left(\frac{q^2 \omega_0 \left(\frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_S} \right)}{4\pi\epsilon_S \hbar \sqrt{2[E/m^*]}} \left[N_0 \sqrt{1 + \frac{\hbar\omega_0}{E}} + (N_0 + 1)\sqrt{1 - \frac{\hbar\omega_0}{E}} - \right. \right. \\ \left. \left. \frac{\hbar\omega_0 N_0}{E} \sinh^{-1}\left(\frac{E}{\hbar\omega_0} \right)^{1/2} + \frac{\hbar\omega_0 (N_0 + 1)}{E} \sinh^{-1}\left(\frac{E}{\hbar\omega_0} - 1 \right)^{1/2} \right] \right)^{-1}, \tag{3.13}$$

where q is electronic charge, ω_0 is the optical phonon angular frequency, ϵ_∞ is the

high-frequency (optical) dielectric constant, ϵ_S is the low-frequency (static) dielectric constant, m^* is the conductivity effective mass, and N_0 is the phonon density as calculated using the Bose-Einstein occupation function. For a nondegenerate semiconductor with spherical constant energy surfaces, the average momentum relaxation time can be calculated via [107]

$$< \tau_m >= \frac{\int_0^\infty \tau_m E^{3/2} \exp[-E/k_B T] dE}{\int_0^\infty E^{3/2} \exp[-E/k_B T] dE}. \tag{3.14}$$

Finally, the average momentum relaxation time, $< \tau_m >$, is then employed in

$$\mu_{POP} = \frac{q < \tau_m >}{m^*} \tag{3.15}$$

to calculate the POP scattering mobility limit. Table 3.4 summarizes the four POP input parameters for several n-and p-type semiconductors. Figure 3.7 shows that there is a close relation between the POP mobility limit and the maximum reported intrinsic mobility of several selected semiconductors. The slope of the fit to the data (0.874) is a bit less than one, suggesting that the POP scattering model tends to slightly underestimate the intrinsic mobility. Overall, Fig. 3.7 shows rather good agreement with the assumption that the intrinsic mobility is limited by POP scattering for a wide range of polar semiconductors.

Note the dramatic difference in Table 3.4 in POP mobility of ~10 and ~240 $cm^2V^{-1}s^{-1}$ for SnO and Cu_2O, respectively. This clearly makes Cu_2O the more promising candidate for a p-type TFT channel layer, at least from the perspective of the POP mobility model. However, keep in mind that a single crystal phase as assumed in Table 3.4 is not attainable on large glass substrates such as those used in

flat-panel display manufacturing using conventional PVD equipment.

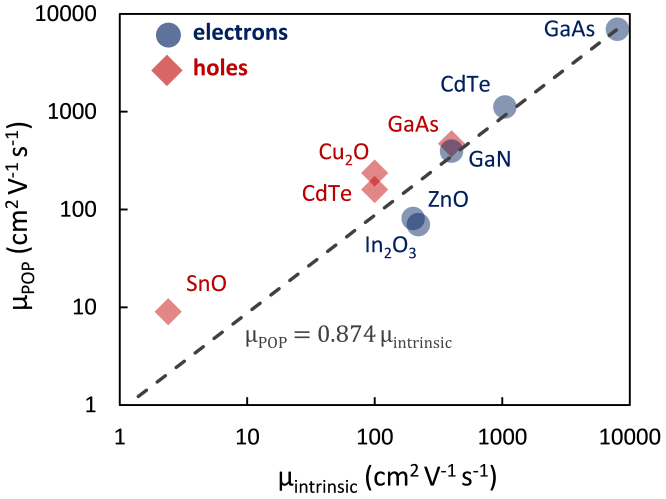

Figure 3.7: POP mobility limit, μ_{POP}, versus intrinsic mobility, $\mu_{intrinsic}$.

Assessing polar optical phonon scattering using Eqs. 3.13 - 3.15 is a bit complicated. It turns out that POP mobility trends are often dominated by the Eq. 3.13 prefactor, such that a unitless polar (Fröhlich) coupling constant can be defined as,

$$\alpha = \frac{q^2}{4\pi\epsilon_0\hbar}\sqrt{\frac{m^*}{2\hbar\omega_0}}\left[\frac{1}{\epsilon_{\infty R}} - \frac{1}{\epsilon_{SR}}\right], \tag{3.16}$$

where ϵ_0 is the dielectric constant of free space while $\epsilon_{\infty R}$ and ϵ_{SR} are the low-frequency (static) and high-frequency (optical) relative dielectric constants, respectively. It is found from Table 3.4 that α(n-type) = 0.07 (GaAs), 0.35 (CdTe), 0.41 (GaN), 1.2 (In_2O_3), 1.0 (ZnO) and α(p-type) = 0.17 (GaAs), 0.67 (CdTe), 0.28 (Cu_2O), and 4.0 (SnO). Figure 3.8(a) shows that $\mu_{\text{intrinsic}}$ and α are strongly correlated. The dissimilar electron and hole slopes of the fit to the data are primarily due to effective mass differences. The last term in the square brackets of Eq. 3.16, involving the reciprocal difference of the high- and low-frequency relative dielectric

constants, appears to be a dominant contributor to α. Thus, a unitless POP coupling parameter is defined as the inverse of the reciprocal difference of $\epsilon_{\infty R}$ and ϵ_{SR}, as indicated in Fig. 3.9. A plot of POP_{CP} versus band gap, E_G, is given in Fig. 3.9 for 107 inorganic semiconductors and insulators [93]. POP_{CP} decreases with increasing band gap. Thus, mobility decreases with increasing band gap due to POP scattering. This leads to a display backplane materials dilemma in which a high ON-current (high mobility) and a low OFF-current (wide band gap) are difficult to achieve at the same time.

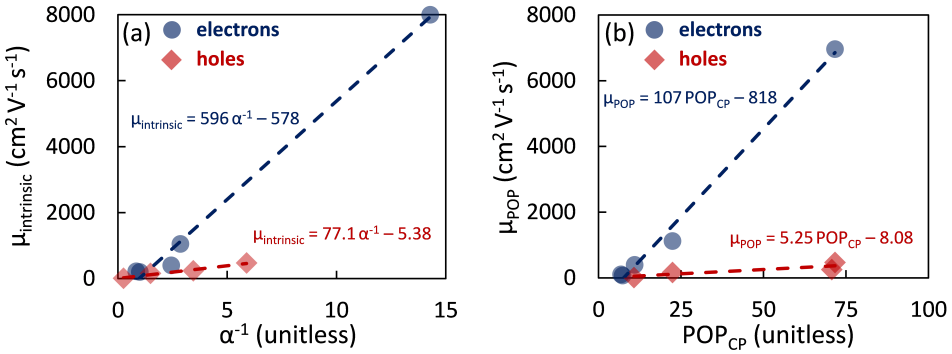

Figure 3.8: (a) Intrinsic mobility as a function of the inverse Fröhlich coupling constant and (b) POP mobility as a function of the POP coupling parameter.

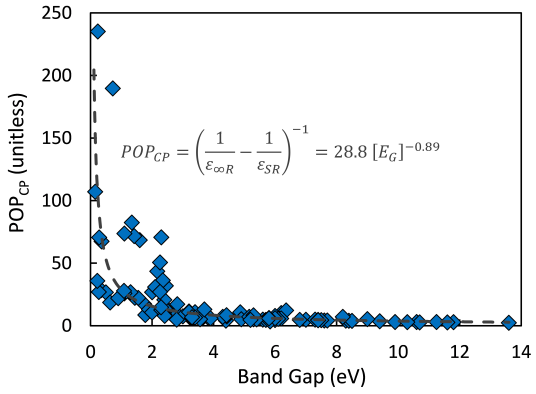

Figure 3.9: POP coupling parameter versus band gap trend for 107 inorganic semiconductors and insulators.

Table 3.4: Single crystal semiconductor POP model parameters, calculated POP mobility, and reported intrinsic mobility.

Semiconductor	$\mathbf{m^*_{e,h}}$ (unitless)	$\epsilon_{\infty R}$ (unitless)	ϵ_{SR} (unitless)	$\hbar\omega_0$ (meV)	$\mu_{\mathbf{POP}}$ ($cm^2V^{-1}s^{-1}$)	$\mu_{\mathbf{intrinsic}}$ ($cm^2V^{-1}s^{-1}$)
ELECTRONS						
GaAs	0.063 [108]	10.86 [93]	12.8 [93]	35 [109]	6960	8000 [108]
CdTe	0.096 [110]	7.1 [93]	10.4 [93]	21.3 [111]	1120	1050 [108]
GaN	0.13 [112]	5.2 [93]	9.95 [98]	87.3 [112]	395	400 [108]
In_2O_3	0.30 [12]	4.0 [12]	8.9 [12]	50 [12]	70	220 [12]
ZnO	0.23 [113]	3.73 [93]	8.28 [93]	73.1 [114]	103	200 [108]
HOLES						
GaAs	0.38 [108]	10.86 [93]	12.8 [93]	35 [109]	470	400 [108]
CdTe	0.35 [110]	7.1 [93]	10.4 [93]	21.3 [111]	160	100 [108]
Cu_2O	0.58 [115]	6.46 [93]	7.11 [93]	19 [116]	236	100 [117]
SnO	1.5 [118]	6.25 [93]	15 [118]	15.1 [119]	9	2.4 [92]

3.3 Doping and Polycrystalline Considerations

As mentioned previously, the single crystal mobility considerations presented in Section 3.2 are not the final word on the utility of a newly identified semiconductor for display-based, large-area electronics applications since use of an intrinsic, single crystal semiconductor is impractical. In practice, the single crystal mobility of a new, high-performance semiconductor will be degraded by ionized impurity scattering and grain boundary issues. These issues are briefly discussed in the following. Our treatment is not original or exhaustive. Rather, our purpose here is to warn the would-be researcher undertaking this hypothetical exploratory development project that there are other mobility challenges to overcome even if a new high-performance single crystal semiconductor has been successfully discovered. Ionized impurity scattering can reduce the mobility in a doped semiconductor. For a non-degenerate semiconductor, the ionized impurity scattering limited mobility is inversely proportional to the doping concentration, N_{II}, as given by the following equation [114]

$$\mu_{\mathrm{II}} = \frac{128\sqrt{2\pi}\epsilon_S^2 \left(k_B T\right)^{3/2}}{q^3 N_{\mathrm{II}} \sqrt{m^*} \left[\ln\left(\frac{24 m^* \epsilon_S (k_B T)^2}{q^2 N_{\mathrm{II}} \hbar^2}\right)\right]}. \tag{3.17}$$

A magnetron sputtered thin film of, e.g., zinc oxide on a glass substrate typically results in a polycrystalline phase, which introduces grain boundaries. Carriers can get scattered or trapped at a grain boundary. If the mean free path in the single crystal is much larger than the size of the grains in the polycrystalline thin film, then one can assume that the mean free path (MFP) is equal to the grain size, l_G [120]. The average momentum relaxation time for grain size scattering (GSS) can then be

estimated as

$$< \tau_m >_{\text{GSS}} = \frac{l_G}{v_{th}} = \frac{l_G}{\sqrt{\frac{8k_BT}{\pi m_e^*}}}. \tag{3.18}$$

A GSS limited mobility can then be written as

$$\mu_{\text{GSS}} = \frac{ql_G}{\sqrt{\frac{9}{\pi}m_e^* k_B T}}. \tag{3.19}$$

The transition from amorphous to polycrystalline transport is likely to be continuous. The minimum grain size in the polycrystalline phase should then be equal to the MFP in the amorphous phase. Hence, using Eq. 3.4 and 3.19, a 'minimum grain size' for an amorphous material can be defined as

$$l_{G,min} = \sqrt{\frac{2\hbar^2}{8\pi m_e^* k_B T}}, \tag{3.20}$$

and corresponds to where the transition between amorphous diffusive transport and grain size limited polycrystalline transport occurs. The 'minimum grain size' is typically on the order of one nanometer.

Using Eqs. 3.15, 3.17 and 3.19, a polycrystalline mobility for a doped semiconductor can be formulated as follows

$$\mu_{\text{polycrystalline}} = \left(\frac{1}{\mu_{\text{POP}}} + \frac{1}{\mu_{\text{II}}} + \frac{1}{\mu_{\text{GSS}}}\right)^{-1}. \tag{3.21}$$

Figure 3.10 illustrates mobility trends as a function of grain size for the three scattering mechanisms included in Eq. 3.21 for a polar polycrystalline semiconductor, using zinc oxide as an example. The 'minimum grain size' in this case is 0.95 nm. Note from Fig. 3.10 that an ionized impurity of 1×10^{17} cm^{-3} is of negligible importance in

this simulation. Grain size scattering is found to be significant only for grain sizes less than 10 nm. Figure 3.10 suggests that an improvement in mobility seems possible when going from an amorphous to a polycrystalline channel layer. However, mobility degradation due to an energy barrier introduced by a grain boundary has not been taken into account yet. The Seto model [121] states that a grain boundary introduces trap states that tend to deplete a semiconductor near a grain boundary. This leads to an energy barrier at the grain boundary. Mobility is reduced in a polycrystalline semiconductor with grain boundary barriers since carriers must surmount energy barriers. Finally, a polycrystalline semiconductor is more prone to defect creation and compensation than a single crystal semiconductor. In summary, more issues need to be considered with a polycrystalline semiconductor compared to an amorphous semiconductor, in terms of non-ideal transport behavior, as well as scaling to large areas.

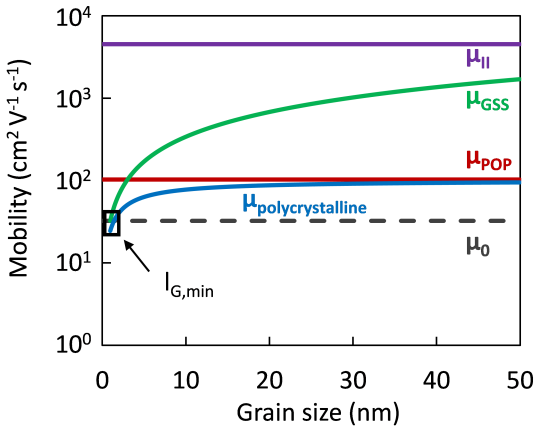

Figure 3.10: Mobility as a function of grain size for the case of zinc oxide (see Table 3.4 for material parameters). Ionized impurity concentration is assumed to be 1×10^{17} cm^{-3}.

3.4 Conclusion

The objective of this chapter was to provide a framework for the development of new high-performance TFT channel layer materials for large-area electronics applications, specifically display backplanes. A physics-based model is presented which predicts a maximum amorphous semiconductor mobility of ~71 $cm^2V^{-1}s^{-1}$ (~16 $cm^2V^{-1}s^{-1}$) for electrons (holes). If a semiconductor mobility exceeding these limits is required, a crystalline semiconductor must be employed. Polar optical phonon scattering seems to establish an approximate upper mobility limit for single crystal polar semiconductors. However, a single crystal semiconductor is impractical for large-area electronics. Practical deposited semiconductors for large-area electronics applications will be either amorphous or polycrystalline. However, when going to a polycrystalline channel layer, grain size scattering and energy barriers introduced by grain boundaries impede carrier transport, as will an increased defect density, compensation, and carrier trapping.

CHAPTER 4: EXPERIMENTAL METHODS

Thin films and TFTs in this work are fabricated in a cleanroom environment at the Materials Synthesis and Characterization (MaSC) laboratory at Oregon State University. The layer stack of the TFTs is deposited by means of physical vapor deposition (PVD) techniques. The channel layer and source/drain contacts are deposited via radio frequency (RF) magnetron sputtering and thermal evaporation, respectively. These PVD processes are conducted under a vacuum atmosphere. Thus, a basic understanding of the characteristics of a vacuum and the basic functioning of a vacuum system are very helpful.

The BIO work (Chapter 5) utilized a Circuits Processing Apparatus (CPA) sputtering system and a Veeco thermal evaporator. The DAL work (Chapter 6) employed, for the majority, an AJA Orion 5 sputtering system and a Polaron thermal evaporator. The advantages of the Orion 5 system over the CPA tool are a lower base pressure (turpo pump instead of diffusion pump), a high vacuum load lock (instead of a medium vacuum load lock), and two power supplies for co-sputtering capabilities.

Analysis of the semiconductor thin film can provide invaluable insights and complements the information gathered from device testing. One primary characterization technique used is x-ray diffraction (XRD) and x-ray reflectivity (XRR) which can provide information about the film crystal structure, or lack thereof, and film thickness. Another useful technique is a Hall measurement which gives carrier concentration and mobility of the semiconductor.

The fabrication of a TFT is followed by electrical testing. Different test setups

and settings of the tools used (e.g., the semiconductor parameter analyzer) can influence the measurement. Several key parameters (figures of merit) are calculated to assess the device performance and to judge the capability of a novel material. When comparing various results within the OSU group and across research groups internationally the testing methods must be known. As a consequence, the testing setup and the basic equations for extracting carrier mobility, drain current on-to-off ratio, sub-threshold swing, as well as turn-on and threshold voltage are described in this chapter.

4.1 Fundamentals of Vacuum Technology

4.1.1 Characteristics of a Vacuum

The term vacuum describes a volume void of matter. Even the most advanced vacuum technology cannot evacuate an enclosed space to complete emptiness. Typically, the term vacuum refers to any gas pressure below the atmospheric level. PVD methods such as magnetron sputtering and thermal evaporation are vacuum processes. At atmospheric pressure the source or target material would not reach the substrate, because there are too many collisions with gas molecules from the air. Furthermore, atmospheric gas is a potential source of contamination. Deposition under vacuum results in a much purer film.

There are several causes that limit the lowest achievable pressure in a real vacuum chamber, illustrated in Fig. 4.1. Permeation, diffusion, and desorption (outgassing) are physical mechanisms. All three are sometimes collectively referred to as *outgassing* in a general sense. During desorption gas detaches from the chamber walls that

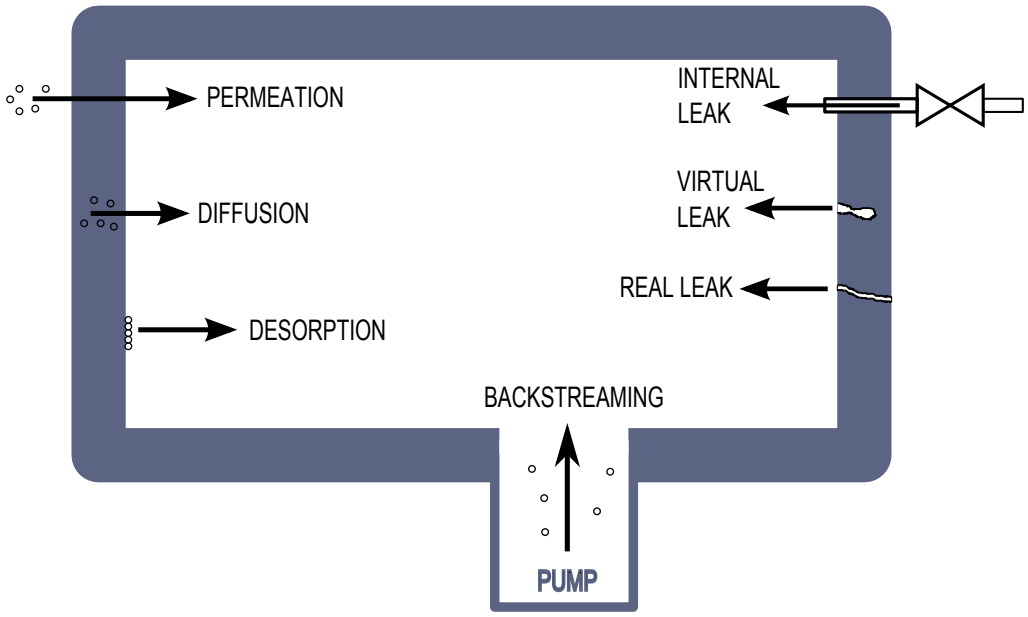

Figure 4.1: Physical mechanisms that increase gas pressure in the system are permeation, diffusion, and desorption. Leaks are categorized into internal leaks, virtual leaks, and real leaks. Figure created with data from Ref. [10].

was previously adsorbed on the surface, thus increasing the pressure of the system. Diffusion involves diffusion of gas through a material (chamber wall), followed by desorption. Permeation is a three-stage process that consists of adsorption of a gas molecule on the exterior (high pressure) side, diffusion through the chamber wall, and finally, desorption from the interior wall [122]. Furthermore, there are leaks which can be categorized into internal leaks, virtual leaks, and real leaks. An internal leak can be caused by a pressure differential across an imperfect valve. Gas trapped in, e.g., a screw thread can result in it being slowly released (virtual leak). Lastly, there is the possibility of particles moving the opposite direction, from the pump into the chamber (backstreaming).

Different gas loads tend to dominate during the pumpdown process, as is schematically shown in Fig. 4.2. Initially, the pressure decays quickly while the gas volume

is pumped out. From there on, desorption and diffusion dominate the gas load and, finally, the lowest pressure is limited by permeation, leaks and type of pump. Hence, materials for vacuum applications are carefully chosen after evaluation of their outgassing and gas permissibility properties.

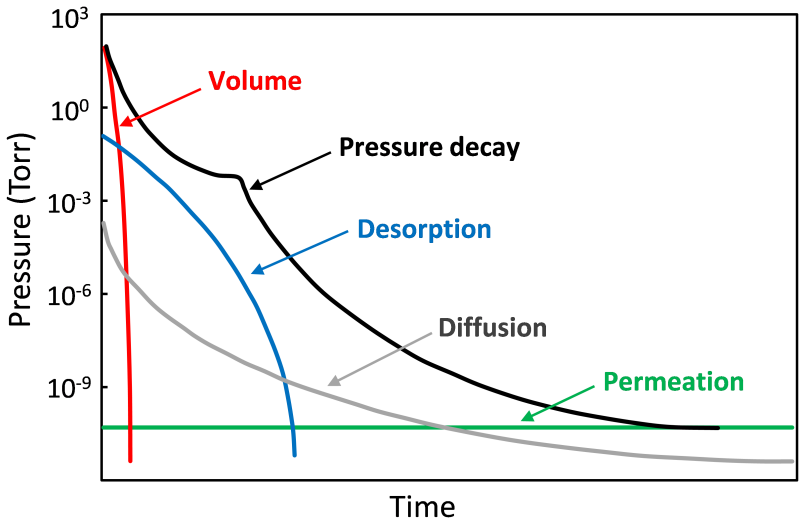

Figure 4.2: The various gas loads during pumpdown. Figure adapted from Ref. [10].

A vacuum is categorized into pressure ranges of low (rough), medium, high (sometimes subdivided into high/very-high), and ultra-high vacuum. Frequently, vacuum equipment such as pumps and pressure gauges can only cover one or two of the former mentioned vacuum levels, making it necessary to employ more than one type of pump/gauge to cover the full range of working and base pressures for a certain application. The working pressure refers to the pressure at which the deposition takes place whereas the base pressure is the lowest pressure achieved in the deposition chamber after loading the sample and pumping down for a reasonable amount of time.

Characteristic properties of a certain vacuum pressure are the mean free path (MFP), monolayer (ML) formation time, flow regime, gas composition and dominat-

ing physical mechanism limiting pumpdown. The mean free path is the characteristic length a particle moves between two consecutive scattering events. The MFP for air at room temperature can be approximated by, [10]

$$MFP = \frac{1}{\sqrt{2} \cdot \pi \cdot d^2 \cdot n} \approx \frac{5.1 \times 10^{-3}(cm)}{P(Torr)}. \tag{4.1}$$

The MFP at a typical sputter deposition pressure of 5 mTorr is approximately 1 cm. This means at a target-to-substrate distance (throw distance) of 10.2 cm (4 inches) an ejected target atom undergoes, on average, 10 collisions before reaching the substrate.

The monolayer formation time is the time it takes one ML to form on a pristine surface. It is closely related to the impingement rate [123]. A layer can form either on the chamber walls which slows down the pumpdown process or on the substrate and act as a source of contamination. Therefore, it is often advantageous to increase the deposition rate allowing less time for foreign atoms to be incorporated into the film. Table 4.1 shows different ML formation times in dependence of pressure assuming a sticking coefficient of one (every impinging particle sticks to the surface).

Table 4.1: MFP, ML formation time, and corresponding vacuum level, range, and flow regime for three different pressures. The chosen values of 760, 1×10^{-3}, and 1×10^{-7} Torr equate to approximately atmospheric pressure, working pressure, and base pressure, respectively.

Pressure	MFP	ML formation	Vacuum level	Range	Flow regime
760 Torr	0.67 nm	2.9 ns	Low (Rough)	760 to 1 Torr	Viscous
1×10^{-3} Torr	5.1 cm	2.2 ms	Medium	1 to 10^{-3}	Knudson
1×10^{-7} Torr	510 m	22 s	High	10^{-3} to 10^{-7}	Molecular

Several different flow regimes exist in a vacuum system. The gas can be in a viscous, intermediate, or molecular state depending on the chamber or pipe diameter

and on the MFP. The length of the MFP in turn depends on the type of gas, temperature, and, especially, pressure [124]. The three flows can be distinguished by the relation $\frac{D}{MFP}$, where D is the diameter of the pipe. Frequently, the relation $\frac{D}{MFP}$ and the intermediate state are referred to as the Knudson number and the Knudson flow, respectively. A Knudson number above 100, between 1 and 100, and smaller than 1 corresponds to the viscous, Knudson, and molecular flow regime, respectively [10]. As can be seen from the Knudson number, in the viscous regime there are many more collisions among particles compared to the molecular flow, where the MFP is large and particles dominantly interact with the chamber walls.

Not only does the flow regime change during pumpdown from atmosphere to high vacuum, but the composition of the gas changes as well. A vacuum system can be equipped with a residual gas analyzer (RGA) to gather information about the gas species present. At low vacuum the composition is mostly unaltered from atmosphere. Going to high vacuum the gas contains an increasing amount of water vapor, up to between 70 and 90 %, coming from exposed surfaces/chamber walls [124]. In ultra-high vacuum, hydrogen is the dominant species. The discussed characteristics of a vacuum: MFP, ML formation time, and flow regime are summarized in Table 4.1.

4.1.2 Vacuum Systems

A vacuum system consists of several components. These core components tend to be very similar across a wide range of physical vapor deposition (PVD) and chemical vapor deposition (CVD) tools. A block diagram of a typical PVD system is shown in Fig. 4.3. The heart of the system is the main (or deposition) chamber where the deposition takes place. Attached to the main chamber is a high vacuum pump separated

by a high vacuum isolation valve which also acts as a throttle valve. The throttle valve modulates the throughput of the pump and is thus effectively controlling the pressure in the chamber. Additionally, the working pressure is controlled by regulating the flow rate of any process gas admitted into the chamber. The high vacuum pump will typically fail if the exhaust is at atmospheric pressure. Therefore, it is backed by a medium vacuum pump connected via the foreline. The second, smaller chamber is the load lock which can be equipped to achieve a medium vacuum or high vacuum. It is then directly connected to a medium vacuum pump via the roughing line or set up equivalently to the high vacuum main chamber with a set of two pumps. The load lock acts as a double door entry to the main chamber and prevents particles and contaminants from getting into the main chamber from atmosphere. Furthermore, its smaller volume allows it to be pumped down to medium/high vacuum much more efficiently after the loading of samples at atmospheric pressure. Meanwhile, the main chamber can stay at medium/high vacuum except for occurrences such as maintenance, change of target material, etc.

Another essential piece of equipment is the pressure gauge. Typically, the main chamber has three pressure gauges, one gauge which covers the range from atmospheric pressure to medium vacuum, one that covers the range from medium vacuum to high vacuum, and a third one that allows the precise pressure measurement at the working pressure range during the deposition. Furthermore, a number of gauges are placed at important locations, i.e., at the load lock and foreline to monitor the state of the system.

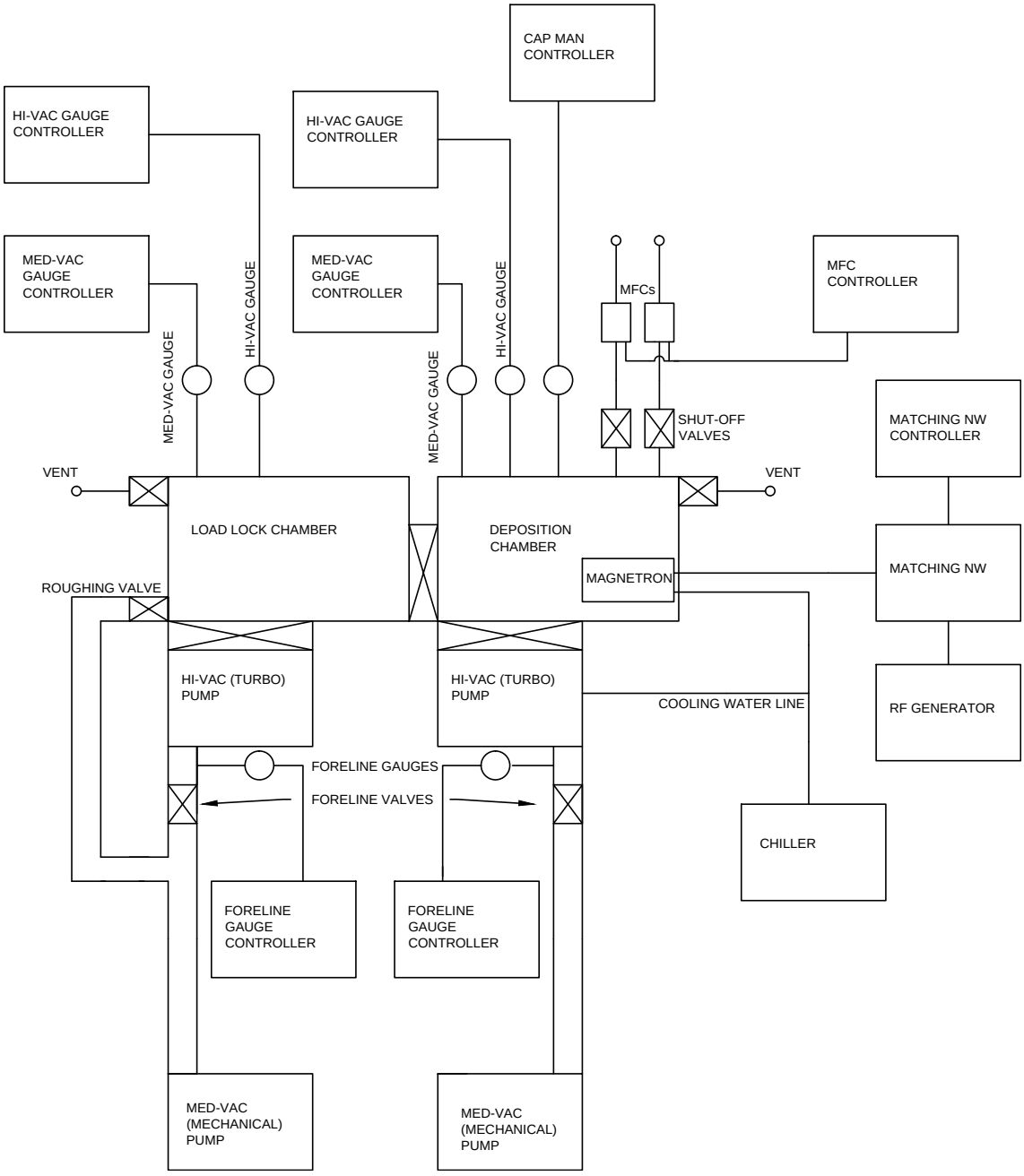

Figure 4.3: Block diagram of a load-locked high vacuum system. The main chamber is typically equipped with a single gun and corresponding RF generator/power supply for a sputtering system.

4.2 Thin Film Deposition and Analysis

4.2.1 RF Magnetron Sputtering

Sputtering is a thin film deposition technique and belongs to the class of physical vapor deposition (PVD) methods [125]. Energetic argon ions (Ar^+) are accelerated toward a target. The ions hit the target and physically remove target atoms. The ejected atoms travel away from the target and deposit on the substrate and chamber walls. The process is depicted in Fig. 4.4(a). The argon ions are generated by a type of plasma called glow discharge. A plasma consists of positive charges (ions), negative charges (electrons), and neutral gas particles. If a free electron has sufficient kinetic energy it can ionize or excite an Ar atom. In the event of ionization, an Ar^+ ion and a second electron are generated. The two free electrons can ionize additional Ar atoms causing a cascading effect. If the energy transferred by the collision between electron and Ar atom is less than the ionization potential, it will cause a temporarily excited state of the Ar. When the Ar atom relaxes, it emits a photon. The emitted photon is the cause of the characteristic glow of the plasma.

The target acts as the cathode and the substrate/chamber walls as the anode. When a direct current (DC) bias is applied between the target and substrate, the positively charged ions are accelerated toward the target by an electric field. The electrons are attracted by the anode. The collection of electrons at the anode completes the circuit. More electrons need to be generated at the cathode to sustain the current flow and therefore the plasma. If a metallic target is used, the secondary electrons are produced during the ion bombardment of the target.

Most of the voltage is dropped across the cathode sheath. The location of the

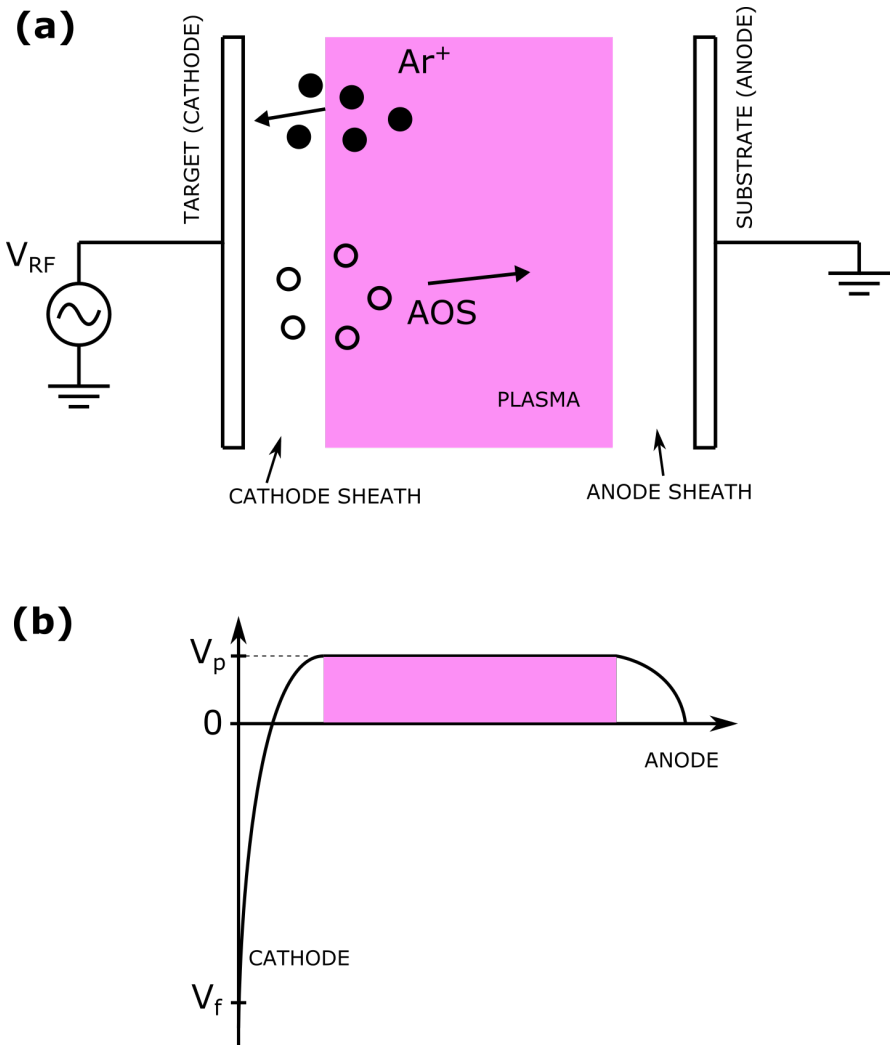

Figure 4.4: (a) Basic mechanism of the sputtering process and (b) a typical voltage distribution from cathode to anode (V_p is the plasma potential).

sheaths is shown in Fig. 4.4. An electron, which has a light mass, is quickly accelerated away from the cathode, whereas a much heavier ion is accelerated comparatively slowly towards the target. Thus, the cathode sheath (or dark space) is predominantly made up of ions and is positively charged. Due to the large electric field in the sheath the electrons gain kinetic energy more quickly and are more likely to ionize an Ar atom than to excite it. Therefore, there is very little glow in the sheath explaining the synonymous term *dark space*.

Simple DC sputtering is suitable for conducting (metallic) target materials, but usually not used for semiconducting or insulating targets [125]. DC sputtering with an insulating target causes charge to build up. Ions hitting the target recombine with an electron to return to the neutral state. In a conducting target a missing electron can be easily replenished. However, for an insulating target this is not the case and the missing electrons lead to positively charging the target surface. The positive charge on the cathode (target) increases until the potential difference between the cathode and anode is too small to sustain the glow discharge. In addition, the charge build up can cause arcing from a charge island/particle to an uncharged region on the target surface or from the target to ground (e.g., dark space shield) [126].

The solution to deposit semiconducting materials is RF sputtering from a ceramic target or reactive sputtering with a metallic target. The RF sputtering technique is employed in this work. During one half of the RF cycle the target has opposite polarity and electrons attracted by the target diminish any positive charge build up. Only the electrons can move quickly enough to follow the RF signal. The ions in contrast, because of their larger mass, remain relatively stationary. This causes a negative *self-bias* voltage on the target and the sputtering process occurs as described previously.

An impedance matching network is required to efficiently couple the power from the RF generator to the cathode/glow discharge. The industry standard for RF sputtering is a frequency of 13.56 MHz. Disadvantages of RF sputtering are a lower deposition rate compared to DC [127] and the more complex and expensive RF equipment.

The addition of a magnetron significantly improves the sputtering process. A magnetron target is shown in Fig. 4.5. Magnets are placed behind the target. The magnetic field confines/traps electrons close to the target surface. The higher electron density greatly increases the ionization rate. As a result, the working pressure can be reduced by about one order of magnitude, improving the transport of the sputtered species (longer MFP), and greatly increasing the deposition rate.

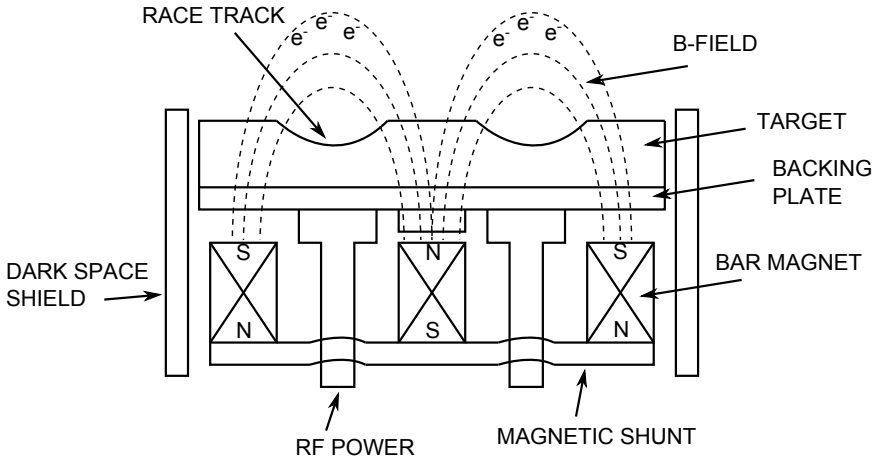

Figure 4.5: Cross section of a magnetron sputter target.

Areas of preferential sputtering exist due to the confinement of the electrons. This circular erosion path is called racetrack. The racetrack can cause film thickness non-uniformity and limits target utilization. The target has to be replaced before all the material is used up. Planar targets with a scanning magnet and cylindrical, rotary magnetron and target technologies have been developed to increase target

utilization [128].

A dark space shield is placed in close proximity around the target to avoid sputtering surfaces beside the front side of the target, shown in Fig. 4.5. The dark space shield is grounded (at anode potential) and at a distance less than the sheath region, thereby preventing a glow discharge to form between the shield and the to be protected area.

It is important to remove the excess heat from the target that develops during sputtering. A thermally conductive backing plate is needed in particular for a non metallic target. In this work an AOS target is bound to an aluminum backing plate with a silver epoxy that is electrically and thermally conductive. The target/backing plate combination is held in place with a magnetic keeper. Thermal paste facilitates the conductivity between backing plate and sputter gun. The RF power connectors and the backside of the target/backing plate are cooled by a water cooling system.

4.2.2 X-Ray Diffraction

X-ray diffraction (XRD) is used to characterize the structural order of a thin film. In an XRD measurement, x-rays scatter on the atoms in the thin film and at certain angles constructive interference occurs according to Bragg's Law, $2d \sin\theta = n\lambda$, where d is the spacing between diffracting planes, θ is the incident angle, and λ is the wavelength of the x-ray source ($\lambda = 0.15$ nm). Detecting the diffracted x-rays across a range of angles produces a diffraction pattern. In a grazing incidence x-ray diffraction (GI-XRD) measurement the incident x-rays are kept at a small, constant angle ($\omega = 0.35°$ in this work) while the 2θ angle of the detector side is swept from 10 to 90°, as shown in Fig. 4.6. GI-XRD is better suited to thin film measurements than a regular

θ-2θ scan because the small incident angle reduces the influence of the substrate. In this work, GI-XRD is mainly used to determine the temperature for phase transitions from an amorphous to crystalline structure. Figure 4.7 shows the diffraction pattern for amorphous and crystalline IGZO.

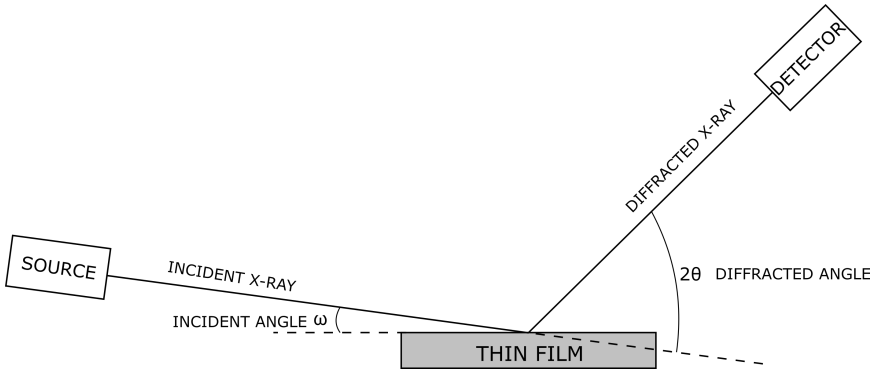

Figure 4.6: Definition of angles for a GI-XRD measurement.

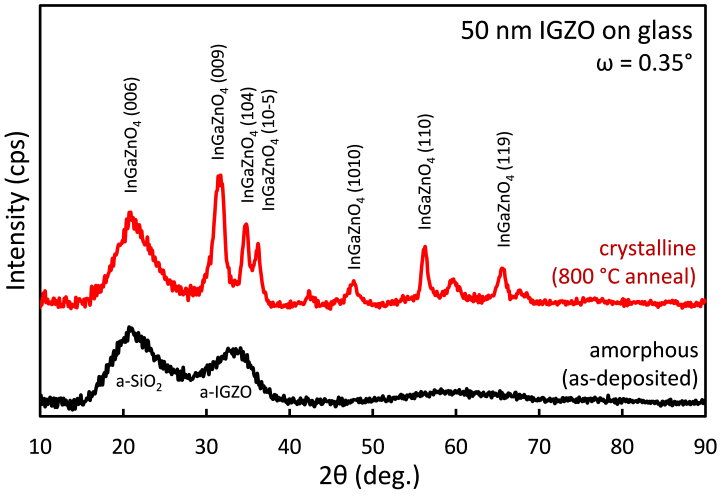

Figure 4.7: Diffraction pattern of amorphous and crystalline IGZO thin films on fused silica.

4.2.3 X-Ray Reflectivity

X-ray reflectivity (XRR) is closely related to XRD and the same Rigaku Ultima IV diffraction system is used. Instead of detection of diffracted x-rays, the reflection of x-rays from the thin film surface is observed. Via a computer modeling approach XRR provides quantitative information about the film thickness (for ~2 to 100 nm thick films), film density, and surface roughness. Additionally, a qualitative assessment can be made by directly comparing the XRR spectra of the thin films studied. The general trends to interpret density, thickness, and roughness from an XRR measurement are indicated in Fig. 4.8(a). Figure 4.8(b) highlights the increasing number of oscillations with increasing film thickness for three ITO samples.

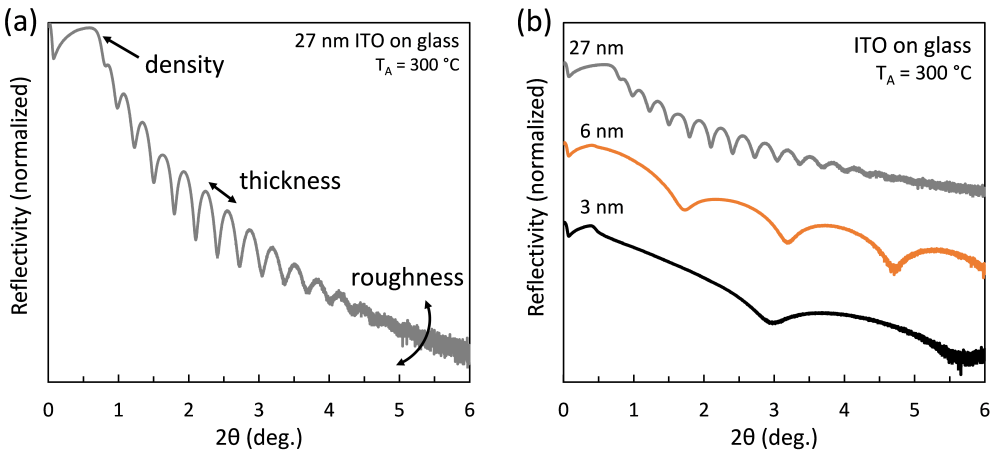

Figure 4.8: (a) General trends of an XRR spectrum and (b) XRR measurement of ITO films with varying thickness.

4.2.4 Optical Spectroscopy

When shining light on a semiconductor parts of the incident light get transmitted, reflected, and absorbed, accordingly T + R + A = 1. In reality, another fraction of the incident light is lost due to other scattering mechanisms. Figure 4.9(a) shows the transmission, reflectance, and corrected transmission of an a-IGZO thin film. The optical absorption coefficient, α, can then be calculated as,

$$\alpha = -\frac{1}{d} \ln \left[\frac{T}{(1-R)} \right], \tag{4.2}$$

where d is the thickness of the film. The resulting absorption plot is shown in Fig. 4.9(b). Note that calculating α without correcting for reflectance (α_{T} curve in Fig. 4.9(b)) severely overestimates the sub-gap absorption as well as the onset and slope of absorption. However, further analysis revealed that the absorption below ~3 eV shown in the $a_{\mathrm{T/(1\text{-}R)}}$ curve is also an artifact and determined that this apparent absorption of ~5000 cm^{-1} is the detection limit (noise floor) of the measurement system. In fact, simple calculation shows that a 1% uncertainty in the '$T/(1-R)$' term in Eq. 4.2 results in an error of $\alpha = 3000$ cm^{-1} for a 30 nm thick film.

The band gap can be estimated from a Tauc plot [129] by plotting '$(\alpha h\nu)^{1/\mathrm{n}}$ vs. $h\nu$', as shown in Fig. 4.9(b), and turns out to be $\mathrm{E_G} \approx 3.2$ eV for a-IGZO. An index of n = 1/2 or 2 is used for a direct or indirect electron transition, respectively. Some controversy exists in the literature about which value of n is appropriate for an amorphous semiconductor since the meaning of *k-space* is lost in a disordered material. N = 2 is used in this work as employed by Tauc [129] and Mott&Davis [26] for an amorphous semiconductor.

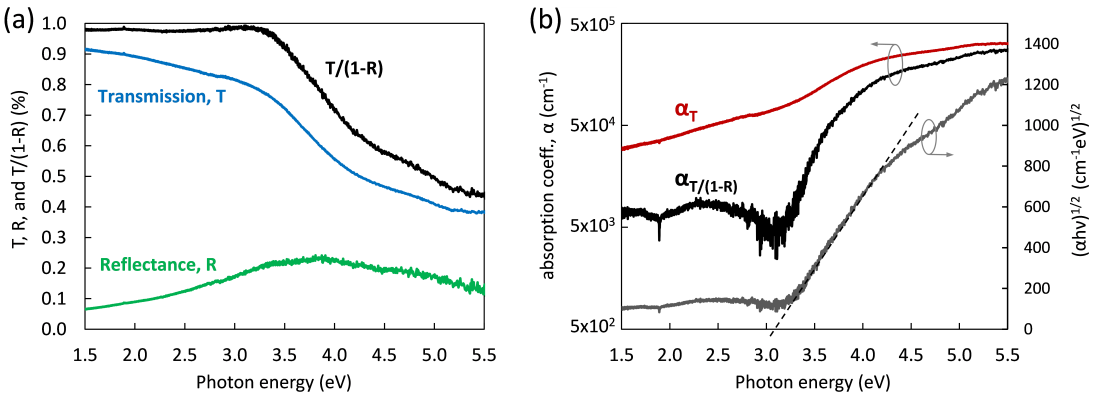

Figure 4.9: Optical spectroscopy of 30 nm a-IGZO on fused silica. (a) Transmission, reflectance, and corrected transmission and (b) absorption coefficient, α, and Tauc plot.

Lastly, the Urbach energy (characteristic slope) of the exponential absorption-tail can be evaluated with the following equation,

$$\alpha = \alpha_0 \exp\left(\frac{h\nu}{E_0}\right), \tag{4.3}$$

where α_0 is an absorption pre-factor and E_0 is the Urbach energy. Note that E_0 differs from the $W_{TA,D}$ Urbach energy discussed in Chapters 2 and 3 in that it describes the joint DOS of valence and conduction band according to the optical absorption theory. As discussed in Chapter 2, it is known that the valence band Urbach energy is much larger than the conduction band Urbach energy for a-IGZO. Hence, the Urbach energy of $E_0 \approx 115$ to 170 meV that is extracted here from the optical spectroscopy can be mainly attributed to the character of the valence band.

4.2.5 Hall Effect

Running a current through a semiconductor and applying a magnetic field perpendicular to it causes a voltage difference transverse to the current, this is called the Hall effect. A Hall measurement allows disentangling the semiconductor conductivity product, $\sigma = qn\mu$, into its individual terms of carrier concentration and mobility. The experimental set-up is shown in Fig. 4.10.

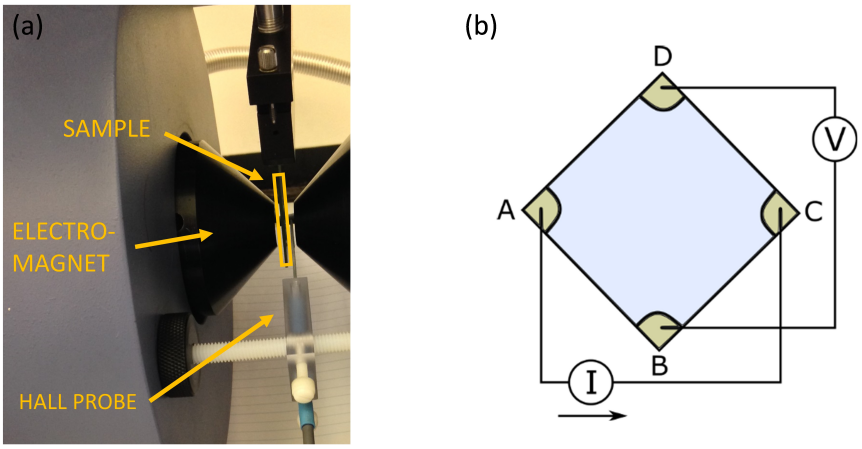

Figure 4.10: (a) Picture of sample mounted between Hall pole magnets and (b) electrodes placed in the *Van der Pauw* configuration.

The complete derivation of the Hall effect is omitted herein and is discussed in, e.g., Ref [130]. However, care must be taken when discussing the Hall mobility. For real thin films the Hall constant, R_H, depends on the carrier concentration, n, with an additional Hall scattering factor, r_H, according to

$$R_H = -\frac{r_H}{qn}. \tag{4.4}$$

As a result, the relationship between Hall mobility, μ_H, and the conductivity mobility of the carriers, μ_{drift}, is $\mu_H = r_H \times \mu_{\text{drift}}$. The Hall scattering factor depends primarily

on the dominant type of scattering the carriers encounter. For example in indium oxide r_H varies between 1.05 and 1.45 depending on the carrier concentration in the thin film [12]. Because the exact value of r_H is usually unknown for novel materials, the value for μ_H is reported in this work when discussing Hall measurements. Additionally, in a Hall measurement the Fermi level is not modulated by a gate voltage (and moves toward the conduction band) as is the case in the operation of a TFT, which could explain why the Hall mobility is typically smaller than the field-effect mobility extracted from a TFT.

4.3 Device Fabrication and Electrical Characterization

This section discusses device fabrication, the methods used for testing the TFT, and extraction of TFT figure of merits. The devices are tested in a dark box Karl Suss probe station with a gold plated chuck (common gate contact) and two probes/micromanipulators to make contact to the source and drain of the TFT. An Agilent 4155C seminconductor parameter analyzer (SPA) is used. Based on past work the typical SPA settings used in this work are 0.1 or 0.2 V step in gate voltage, 0.1 seconds delay time, 1 second hold time, and medium integration time.

4.3.1 Device Fabrication

Fabrication of a TFT involves the following steps: cleaning of the substrate, sputtering of the channel layer, thermal furnace annealing, and evaporation of the S/D contacts. The substrate is a p-type Si wafer with 100 nm thermally grown silicon dioxide acting as the gate insulator. The layer stack and optical microscope image of the staggered

bottom gate device are shown in Fig. 4.11. The p-type substrates acts as the gate and is coated with a chromium/gold layer for lower contact resistance. Devices are fabricated on 10×15 mm^2 coupons and the channel and S/D contacts are patterned via shadow masks. The process sequence is as follows.

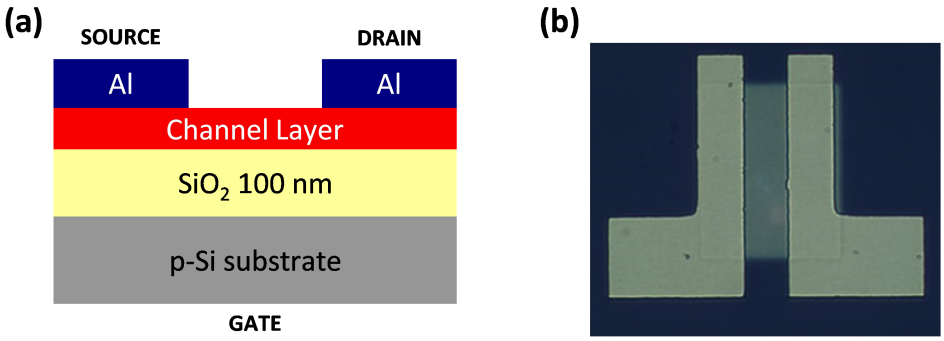

Figure 4.11: (a) Schematic diagram of the TFT structure (cross-section) and (b) optical microscope image of AOS device (top view).

First, the substrate is cleaned in a sequence of rinses of acetone-isopropanol-DI water (AID) followed by nitrogen blow gun drying and dehydration on a hot plate at 200 °C for 30 minutes. Subsequently, the channel layer is deposited via sputtering and then annealed in air in a Neytech Qex furnace. For the BIO work (Chapter 5) an annealing temperature profile of 2 °C/min ramp up - 2 hour hold at target temperature (e.g., 300 °C) - 2 °C/min ramp down is used. For the remaining work a profile of 10 °C/min ramp up - 1 hour hold - 10 °C/min ramp down is used. No significant difference was observed between the two settings.

The S/D contacts are formed by evaporation of aluminum in the Veeco or Polaron thermal evaporators. For the thermal evaporation process a couple of aluminum clips are placed in a wire basket and evaporated via resistive heating under a vacuum atmosphere.

4.3.2 Transfer Curve Assessment

A transfer curve is defined as the plot of drain current versus gate voltage, shown in Fig. 4.12. The main performance metrics of a TFT are turn-on voltage (V_{ON}) or threshold voltage (V_{TH}), mobility (μ), sub-threshold swing (S), drain current on-to-off ratio ($I_D^{ON\text{-}OFF}$), and hysteresis.

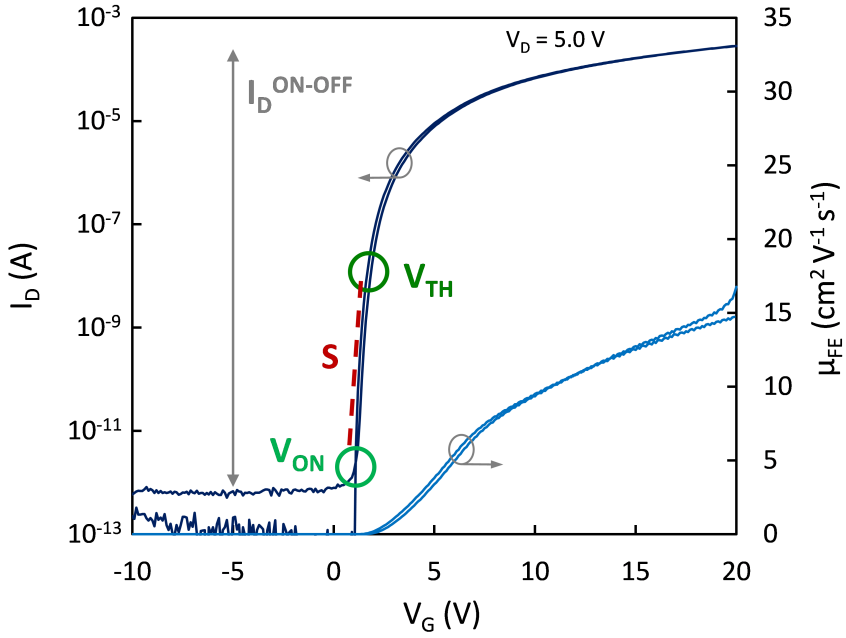

Figure 4.12: Amorphous IGZO transfer curve with illustrations of V_{ON}, V_{TH}, S, I_D^{ON-OFF}, and μ_{FE}.

The turn-on voltage is defined as the applied gate bias at which the first onset of conduction above the off-state leakage current occurs. This is approximately at '$I_D = 1 \times 10^{-11}$ A'. In contrast, several definitions for V_{TH} exists. In this work V_{TH} is defined as the voltage at '$I_D = W/L \times 10^{-9}$ A' with a W/L ratio of 10.

The carrier mobility is an important performance metric as discussed in section 2.1.2. Several methods for extracting the carrier mobility exist and are summarized in

Table 4.2: Summary of incremental, average, field-effect, effective, and saturation mobility equations.

Name	**Equation**	**Notes**
Incremental	$\mu_{INC}(V_{GS}) = \left.\frac{\frac{\partial g_d(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}C_{OX}}\right\|_{V_{DS}\to 0}$	Hoffman model [131]
Average	$\mu_{AVG}(V_{GS}) = \left.\frac{g_d(V_{GS})}{\frac{W}{L}C_{OX}(V_{GS}-V_{ON})}\right\|_{V_{DS}\to 0}$	Hoffman model [131]
Field-Effect	$\mu_{FE}(V_{GS}) = \left.\frac{g_m(V_{GS})}{\frac{W}{L}C_{OX}V_{DS}}\right\|_{V_{DS}\to 0}$	Very common
Effective	$\mu_{EFF}(V_{GS}) = \left.\frac{g_d(V_{GS})}{\frac{W}{L}C_{OX}(V_{GS}-V_T)}\right\|_{V_{DS}\to 0}$	Common
Saturation	$\mu_{SAT}(V_{GS}) = \frac{\left(\frac{\partial\sqrt{I_{DS}}}{\partial(V_{GS}-V_T)}\right)^2}{\frac{1}{2}\frac{W}{L}C_{OX}}$	Common; with $V_{GS} > V_T$ and $V_{DS} > (V_{GS} - V_T)$

Table 4.2. Incremental (μ_{INC}) describes the incremental mobility of carriers injected into the channel. Average (μ_{AVG}) is the average mobility of all carriers in the channel. Notably, incremental, average, field-effect, and effective mobility are calculated from the linear region, in contrast to saturation mobility which is extracted from the saturation region.

The sub-threshold swing S is the inverse of the slope in the sub-threshold region. S is a measure of the steepness of the turn-on and defined as [108]

$$S = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}}\right)^{-1}. \tag{4.5}$$

A small value of S is desired, because it results in more abrupt switching from the OFF to the ON-state and allows scaling of the supply voltage. In a Si MOSFET the sub-threshold current is based on diffusion. Hence, the fundamental lower value of S is limited by thermionic emission across a potential barrier. Initially, only a

small number of carriers, those with high kinetic energy, in the exponential tail of the Maxwell-Boltzmann distribution contribute to the drain current. The lower limit of S can be derived from [108],

$$S = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{OX}}\right) \text{ with T = 300 K and } \frac{C_d}{C_{OX}} \to 0, \tag{4.6}$$

so that

$$S \approx 60 \text{ mV/dec.} \tag{4.7}$$

To first order, this limit still holds true for an AOS TFT (i.e., conduction is not dominated by tunneling) even though the potential barrier is not formed by a pn-junction and there is extensive carrier trapping.

The drain current on-to-off ratio (I_D^{ON-OFF}) is defined as the ratio between the current flow in the OFF-state and the ON-state. The ratio is extracted from a transfer curve with V_{DS} biased in the saturation region.

Finally, the magnitude of hysteresis is defined (in this work) as the V_{TH} difference between reverse and forward sweep. A positive value denotes clockwise and a negative value counter-clockwise hysteresis. For example, the hysteresis of the transfer curve in Fig. 4.12 can be calculated via '$H = V_{TH,\text{rev}} - V_{TH,\text{fwd}} = 1.82 \text{ V} - 1.64 \text{ V} = +0.18 \text{ V}$.'

4.3.3 Output Curve Assessment

An output curve is defined as a plot of drain current versus drain voltage. Typically, a family of curves with constant steps in gate voltage is shown, such as the output curve in Fig. 4.13. The output curve shows good saturation, meaning I_D becoming independent of drain voltage at $V_D > V_{DSAT}$. Additionally, there is a near quadratic

increase of I_{DSAT} with increase in gate voltage showing the desired long-channel *square-law* behavior. The output curve can be used to asess if the device performance is degraded due to series resistance (e.g., a large contact resistance). In the output curve shown in Fig. 4.13 this is not the case as there is a linear (ohmic) increase in I_D at small drain voltages.

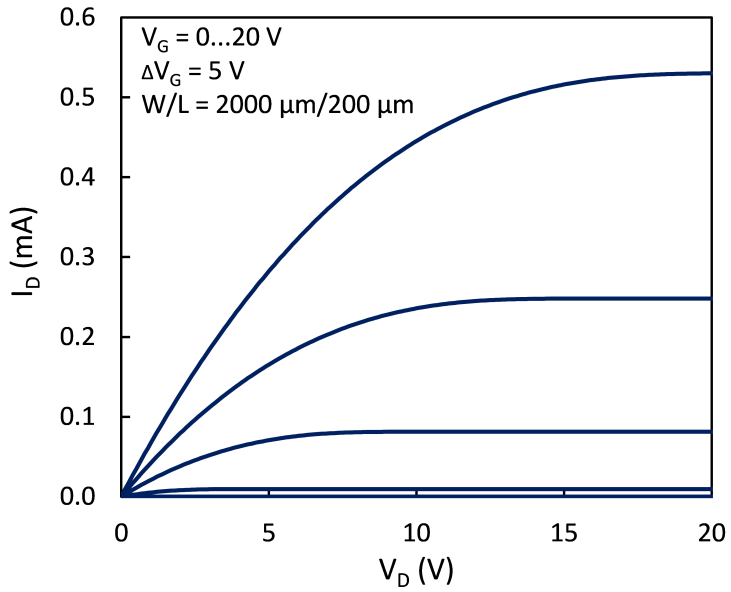

Figure 4.13: Output curve of an AOS TFT fabricated in this work (corresponding transfer curve shown in Fig. 4.12).

CHAPTER 5: BORON INDIUM OXIDE THIN-FILM TRANSISTORS

Boron indium oxide (BIO) is studied for thin-film transistor (TFT) channel layer applications. Sputtered BIO thin films exhibit an amorphous phase over a wide range of B_2O_3/In_2O_3 ratios and remains amorphous up to 500 °C. The band gap decreases linearly with decreasing boron content, whereas device performance generally improves with decreasing boron content. The best amorphous BIO TFT exhibits a field-effect mobility of 10 $cm^2V^{-1}s^{-1}$, turn-on voltage of 2.5 V, and sub-threshold swing of 0.72 V/dec. Decreasing the boron content to 12.5% leads to a polycrystalline phase, but further increases the mobility up to 20-40 $cm^2V^{-1}s^{-1}$. TCAD simulation results suggest that the reason for higher performance after increasing the anneal temperature from 200 to 400 °C is due to a lower defect density in the sub-bandgap region of the BIO channel layer.

This research is also discussed in the following publication:
K. A. Stewart, V. Goulioukk, D. A. Keszler, J. F. Wager, "Sputtered Boron Indium Oxide Thin-Film Transistors," accepted in *Solid State Electronics* (2017).

5.1 Introduction

Boron bonds to oxygen very strongly compared to other cations commonly used in the design of AOSs such as Al, Ga, or Zn. The bond strength for selected metal-oxides is summarized in Table 5.1. A high carrier concentration, which is undesirable for use as a channel layer, is usually attributed to oxygen vacancies in the AOS. Due to its

Table 5.1: Comparison of boron with commonly used cations in the design of an AOS. With data from Ref. [14].

Metal oxide	**Bond dissociation energy (eV)**	**Atomic radius of cation (pm)**	**Band gap (eV)**
B-O	8.4	86	8.0
Al-O	5.3	143	7.5
Ga-O	3.0	135	4.5
In-O	3.7	167	2.9
Sn-O	5.7	151	3.6
Zn-O	2.9	134	3.3

high oxygen bond strength boron should work very well at reducing oxygen vacancies in the In-O system and, hence, act as a carrier suppressor. Gallium is commonly thought of as a carrier suppressor in a-IGZO, however, it also reduces the mobility (as discussed in Section 2.3). The hypothesis is that a smaller size cation will not greatly impact the electron transport among In-In s-orbitals. Boron is a very small element compared to Ga or any of the other relevant AOS cations, see atomic radii in Table 5.1, which potentially could lead to a high mobility of BIO. Boron oxide also has a large band gap of ~8 eV [132] which will aid in increasing the overall band gap of the boron-doped In-O system.

Targets from high purity B_2O_3 and In_2O_3 powders are prepared as follows.

1. Grind binaries with extra 3 mol % of B_2O_3 (due to volatility)
2. Mechanically press into pellets with 1.9 cm diameter
3. React at 1200 °C in air for 4 hours with 10 °C/min ramp up/down
4. Grind in auto-grinder for 2 hours
5. Mechanically press target with 5 cm diameter (load of 10 tons)

6. Sinter at 1100 °C in air for 24 hours with 2 °C/min ramp up/down

7. Bind to roughened aluminum backing plate with silver epoxy

8. Anneal at 60 °C for 24 hours

The melting point of $InBO_3$ is 1610 °C [133]. Reacting at temperatures below or above 1200 °C lead to low density and cracked or brittle pellets. The listed steps are the optimized recipe. High density, ceramic targets are prepared with a fixed stoichiometry of 50/50, 25/75, 17.5/82.5, and 12.5/87.5 mol % B_2O_3/In_2O_3 from here on referred to as 50BIO, 25BIO, 17.5BIO, and 12.5BIO, respectively.

5.2 Thin Film Characterization

Thin films are deposited on fused silica substrates via RF sputtering. Figure 5.1 shows that 50BIO, 25BIO, and 17.5BIO thin films remain amorphous even after an anneal at 500 °C, characterized by the broad peaks in the diffraction pattern. Further GI-XRD analysis shows that the 50BIO, 25BIO, and 17.5BIO thin films are amorphous up to 550, 525 and 515 °C, respectively. The trend of amorphous phase stability versus boron content is summarized in Fig. 5.4(a). The 12.5BIO thin film is polycrystalline as-deposited. The peaks in the GI-XRD pattern of the 12.5BIO thin film, as shown in Fig. 5.1(a), can be referenced to bixbyite In_2O_3. This suggests that the 12.5BIO sample phase segregates into polycrystalline In_2O_3 and amorphous B_2O_3. At this low boron composition the B_2O_3 content in the BIO system is too small to sustain an amorphous phase. Overall, B_2O_3 seems to be quite effective as an amorphous phase stabilizer in the In-O system. This was not necessarily expected considering the small size of boron.

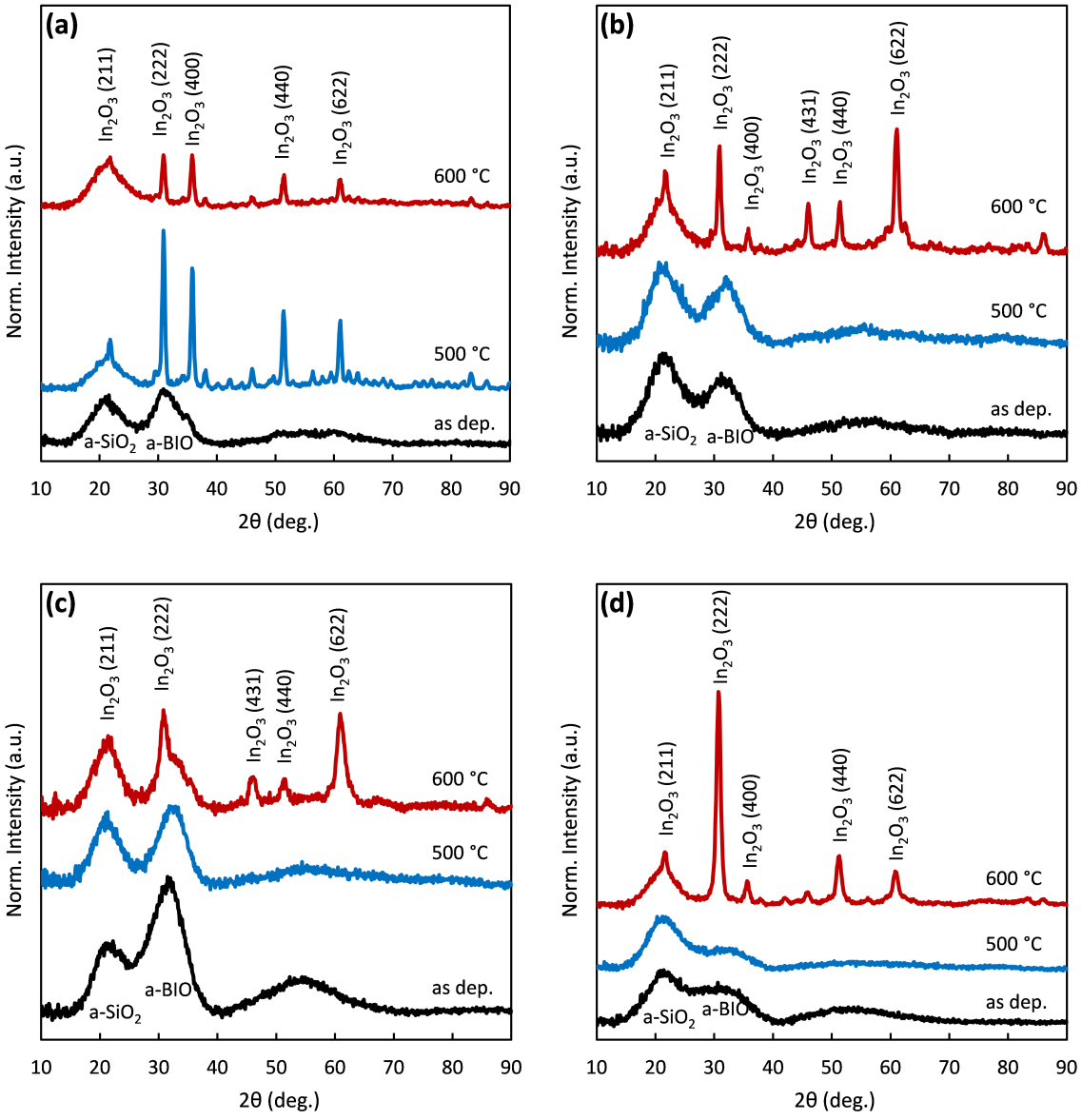

Figure 5.1: GI-XRD patterns of (a) 12.5BIO, (b) 17.5BIO, (c) 25BIO, and (d) 50BIO thin films on fused silica substrates.

Of the investigated compositions, the thin film with the lowest boron content to still be amorphous as-deposited is the 17.5BIO sample. Scanning transmission electron microscopy (STEM) selective-area electron diffraction (SAED) of the 17.5BIO thin film is conducted to further verify the amorphous phase. The STEM image in Fig. 5.2(a) shows that a smooth and homogeneous film is achieved. The sample is then heated in-situ to 400 °C (the maximum temperature of the instrument before drift occurred) and a SAED measurement is performed, as shown in Fig. 5.2(b). The absence of a crystalline diffraction pattern further confirms the amorphous nature of the 17.5BIO thin film even after heating to elevated temperatures.

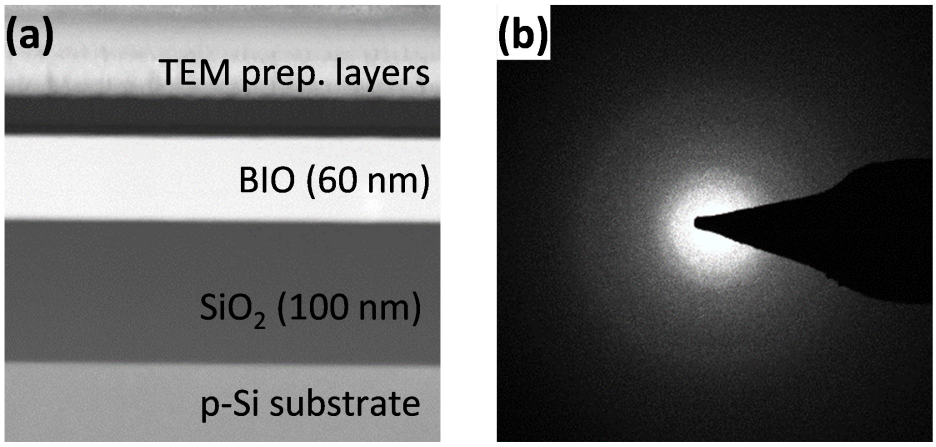

Figure 5.2: (a) Cross-sectional STEM high-angle annular dark-field (HAADF) image of as-deposited 17.5BIO thin film and (b) SAED pattern of BIO layer after in-situ heating to 400 °C, showing an amorphous phase.

The band gap is analyzed from optical spectroscopy using a Tauc plot [129], as shown in Fig. 5.3. The 50BIO thin film exhibits a large band gap of 4.44 eV. The band gap decreases gradually with decreasing boron content. The band gap of the 25BIO, 17.5BIO, and 12.5BIO thin films is 3.46, 3.19, and 2.97 eV, respectively. The trend of band gap versus boron content is summarized in Fig. 5.4(a). The polycrystalline

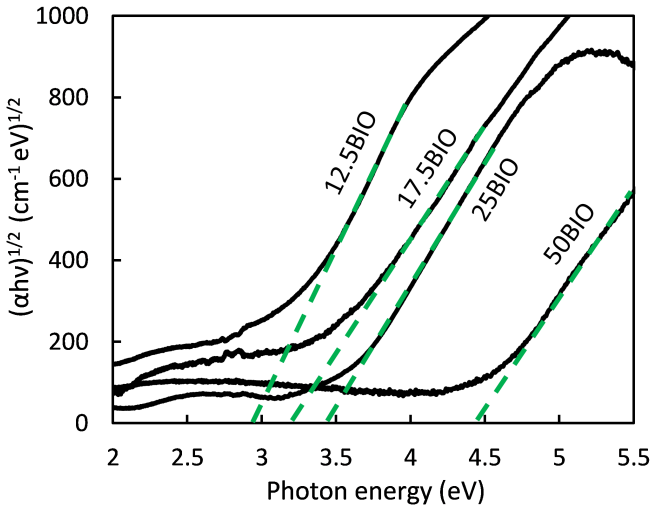

Figure 5.3: Tauc plot of optical absorption of BIO thin films as-deposited.

12.5BIO thin film has a band gap which is very similar to the band gap of 2.9 eV for In_2O_3 [134]. This suggests that the 12.5BIO band gap is determined by the polycrystalline In_2O_3 phase. Note that the amorphous phase stability and band gap as a function of boron content follow two distinctly different trends. The amorphous phase stability is near constant at ~500 °C over a wide range of BIO compositions (50BIO to 17.5BIO) and then abruptly decreases to below 100 °C (*threshold* behavior). On the other hand, the band gap decreases almost linearly with decreasing boron content.

5.3 Device Characterization

Staggered, bottom gate BIO TFTs with a channel thickness (t_{ch}) of 50 nm and an O_2 partial pressure of 10 % are fabricated for each composition. The sputtering time for the BIO channel layer is adjusted for each composition as the deposition rate significantly decreases with increasing boron content. This suggests that the target

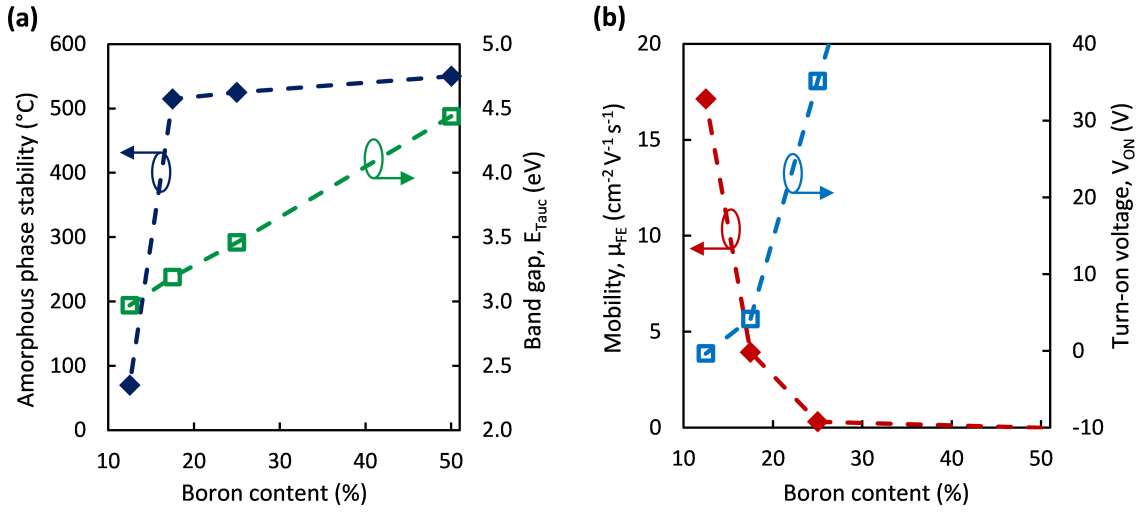

Figure 5.4: Summary of trends with decreasing boron content for (a) amorphous phase stability and optical band gap of thin films; and (b) field-effect mobility and turn-on voltage of devices annealed at 400 °C.

becomes more insulating at higher boron content which also agrees with the trend of increasing band gap as discussed before. Furthermore, no TFT behavior is observed for 50BIO devices indicating a very small free carrier concentration.

The extracted μ_{FE} and V_{ON} performance metrics for the other three BIO compositions are shown in Fig. 5.5. The error bars in Fig. 5.5 indicate the standard deviation of three devices tested for each condition. While there is a moderate amount of variation, overall, μ_{FE} increases with increasing anneal temperature (T_A). Mobility also increases with reduced boron content. At the same time V_{ON} tends to decrease with increasing T_A, as shown in Fig. 5.5(b), and this is further discussed in Section 5.4.

For the T_A = 400 °C data, μ_{FE} and V_{ON} are plotted as a function of boron content in Fig. 5.4(b). V_{ON} decreases with decreasing boron content. This suggests an increase in carrier concentration as well as an increase in the number of oxygen vacancies with lower boron content, and thus, confirms the proposed role of boron as

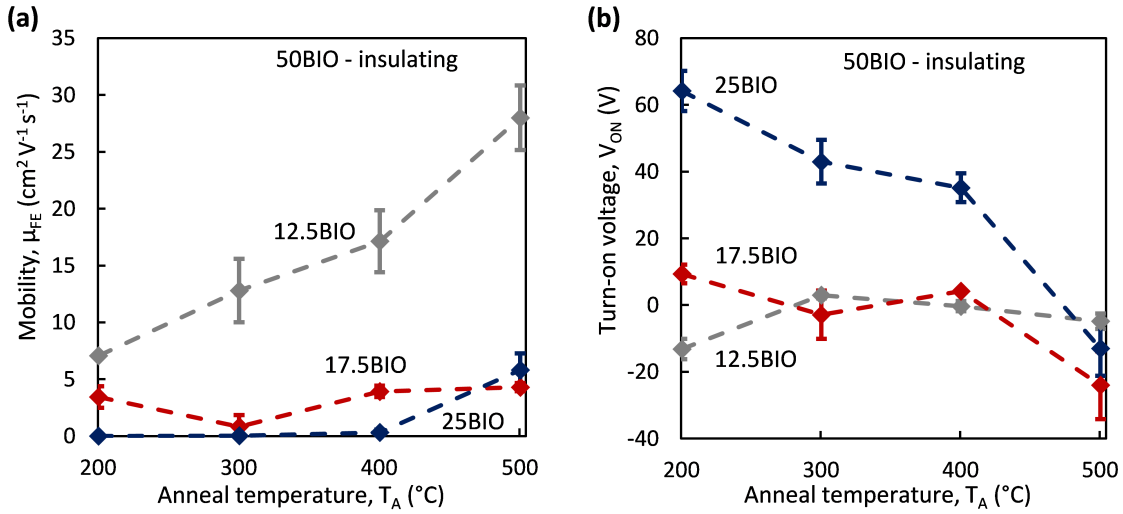

Figure 5.5: (a) Field-effect mobility and (b) turn-on voltage as a function of anneal temperature for BIO TFTs.

a carrier suppressor. The best amorphous BIO device with a good trade-off between high mobility but V_{ON} near zero is the 17.5BIO device at 400 °C with μ_{FE} around 4 $cm^2V^{-1}s^{-1}$. A further improvement in mobility is achieved by reducing the O_2 partial pressure during sputtering from 10 to 5 %. The transfer curve of this amorphous BIO device is shown in Fig. 5.6(a). The extracted device metrics are μ_{FE} of 10 $cm^2V^{-1}s^{-1}$, V_{ON} of 2.5 V, and sub-threshold swing (SS) of 0.72 V/dec. Thus, amorphous 17.5BIO offers a similar performance to that of a-IGZO under the same process conditions [135]. An even higher mobility surpassing that of a IGZO could only be achieved by further reducing the boron content, while at the same time losing the amorphous phase. The polycrystalline 12.5BIO devices exhibit the highest mobility in this study, as shown in Fig. 5.5(a), regardless of annealing temperature. However, 12.5BIO devices also generally have a negative V_{ON}. The process is further optimized by decreasing t_{ch} which moves V_{ON} closer to zero. Of these optimized 12.5BIO devices with ultra-thin channel layer and low maximum process temperature

of 200 °C, a representative device is shown in Fig. 5.6(b). This device exhibits μ_{FE} of 21 $cm^2V^{-1}s^{-1}$, V_{ON} of 2.6 V, and SS of 0.57 V/dec. Finally, the highest mobility device with μ_{FE} of ~40 $cm^2V^{-1}s^{-1}$ is achieved by annealing at a high temperature of 500 °C, as shown in Fig. 5.6(c). However, while achieving a high mobility, other characteristics are degraded, as indicated by significant hysteresis and larger sub-threshold swing.

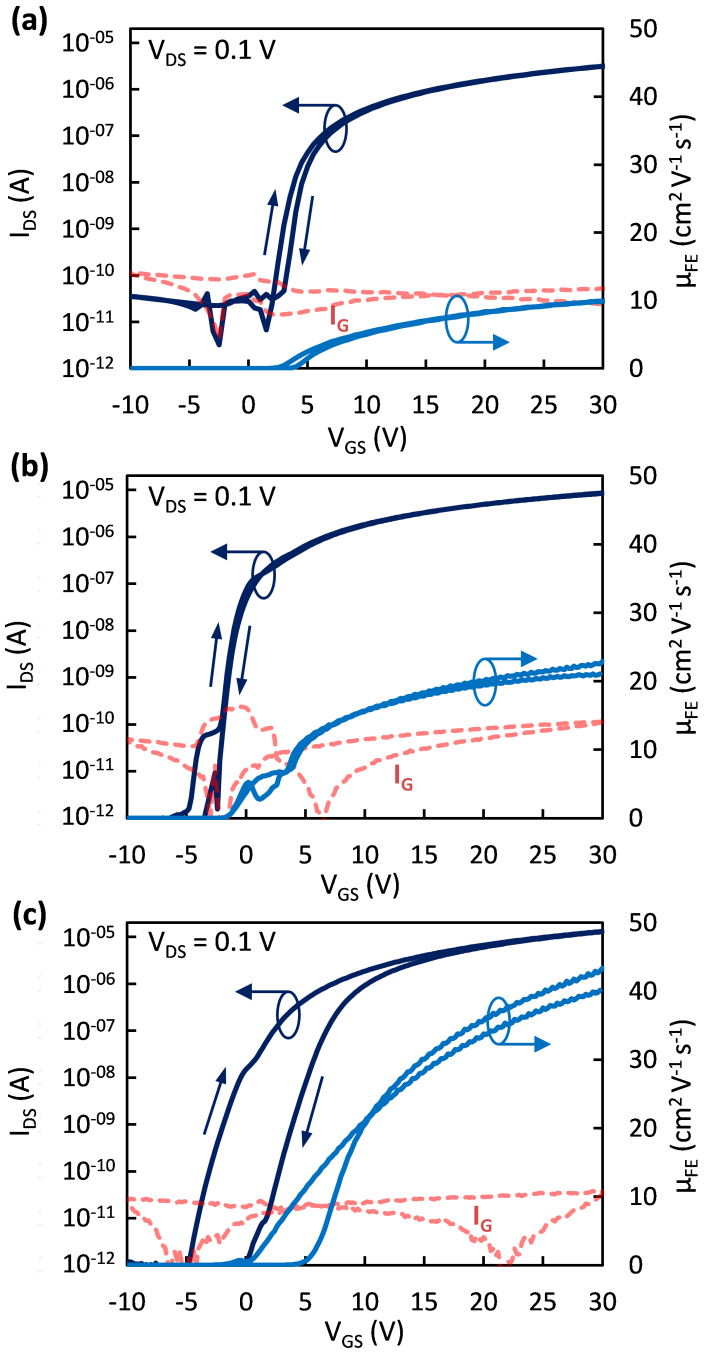

Figure 5.6: Transfer characteristics with optimized process of (a) amorphous 17.5BIO device (t_{ch} = 50 nm, T_A = 400 °C, O_2 = 5 %), (b) polycrystalline 12.5BIO device (t_{ch} = 10 nm, T_A = 200 °C, O_2 = 10 %), and (c) ultra-thin polycrystalline 12.5BIO device (t_{ch} = 5 nm, T_A = 500 °C, O_2 = 10 %).

5.4 TCAD Simulation

The Silvaco ATLAS 2D device simulation software is used to investigate the improved performance at higher T_A. Fig. 5.7 shows the transfer characteristics of two 17.5BIO devices after anneal at 200 and 400 °C (t_{ch} = 50 nm, O_2 = 10 %). The TCAD simulation (solid lines) agrees well with the experimental data (squares), as shown in Fig. 5.7(a). The shift in the transfer curve can be explained with a change in the BIO density of states (DOS), as shown in Fig. 5.7(b). The DOS profile is the only parameter that is adjusted in going from the 200 °C device to the 400 °C device simulation. The gaussian shallow donor states decrease from $N_{GD} = 4.0 \times 10^{18}$ to 1.6×10^{18} $cm^{-3}eV^{-1}$ which can be correlated to a steeper subthreshold swing in the transfer characteristics. The conduction band band-tail states are critical for the electron transport performance [3, 34]. The simulation suggests that the peak density of acceptor band-tail states increases from $N_{TA} = 4.0 \times 10^{20}$ to 1.2×10^{21} $cm^{-3}eV^{-1}$ but that the Urbach energy decreases from $W_{TA} = 57$ to 20 meV. Furthermore, the gaussian deep acceptor state density decreases from $N_{GA} = 5.6 \times 10^{18}$ to 2.0×10^{18} $cm^{-3}eV^{-1}$. The physical origin of the deep acceptor state still needs to be conclusively determined. One suggested explanation involves interface states at the gate insulator/channel interface [8]. The deep acceptor state is needed in the simulation to achieve charge-balance and match the V_{ON} of the experimental data. Billah et al. [136] have successfully used a similar DOS distribution of a gaussian shallow donor state and a slightly deeper gaussian acceptor state for their TCAD simulation of oxide TFTs. In summary, the TCAD simulation results indicate that the improved performance at a higher annealing temperature is due to a lower defect density in the sub-bandgap region of the BIO channel layer. The simulation input

files for both cases are provided in Appendix C.

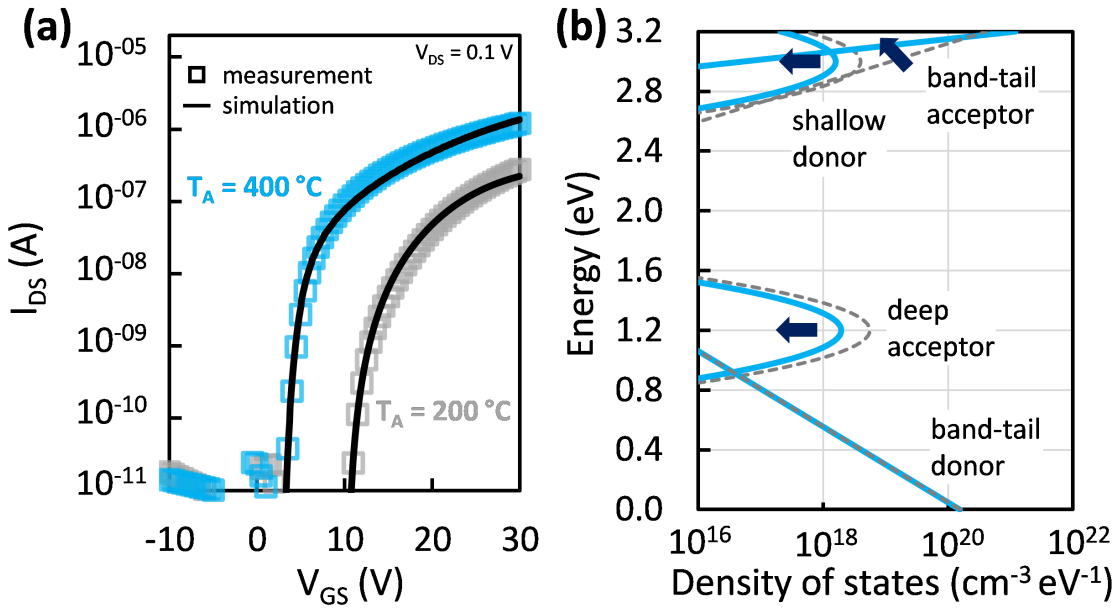

Figure 5.7: (a) Experimental transfer characteristics of 200 and 400 °C annealed 17.5BIO devices and comparison with TCAD simulation. (b) BIO DOS for the 200 °C device (dashed lines) and 400 °C device (solid lines) as inferred from the TCAD simulation.

5.5 Conclusion

Boron indium oxide is investigated over a wide range of B_2O_3/In_2O_3 ratios. Even with a low boron concentration, 17.5BIO remains amorphous up to above 500 °C. As hypothesized in the beginning of this investigation, boron indeed acts as a carrier suppressor and an amorphous phase stabilizer in In-O. A mobility of ~10 and ~20 – 40 $cm^2V^{-1}s^{-1}$ is achieved for amorphous and polycrystalline BIO TFTs, respectively. The results for T_X, E_G, and μ_{FE} are summarized in Table 5.2.

Very recently, ultra-wide band gap (UWB) AOSs have attracted attention due to

Table 5.2: Phase separation temperature, T_X, band gap, E_G, and field-effect mobility, μ_{FE}, as a function of increasing boron content.

% B	**12.5**	**17.5**	**25**	**50**
T_X (°C)	70	515	525	550
E_G (eV)	2.97	3.19	3.46	4.44
μ_{FE} ($cm^2V^{-1}s^{-1}$)	20-40	10	7	-

their excellent negative bias illumination stress (NBIS) stability. It is reported that an UWB AOS requires a band gap of around ~3.8 eV [137, 138]. As an avenue for future research, an UWB BIO device seems possible with a predicted boron content of 34 % from a linear fit of the band gap data shown Fig. 5.4.

CHAPTER 6: DUAL ACTIVE LAYER THIN-FILM TRANSISTORS

Dual active layer (DAL) TFTs are a promising technology to increase the performance compared to single active layer (SAL) devices such as an a-IGZO TFT. SAL and DAL TFTs comprised of a-IGZO and ITO-IGZO are fabricated using the same process conditions and compared side-by-side. TCAD simulation is used to investigate the SAL and DAL device performance. A mapping technique is used to directly correlate the transfer characteristics to the sub-bandgap density of states. The simulation suggests that the improved performance of the DAL is due to an improved gate insulator/channel interface with an approximately one order of magnitude lower interface trap density. Additionally, a novel DAL TFT with a crystalline/amorphous channel is investigated.

Part of the research in this chapter is also discussed in the following publication:
K. A. Stewart, V. Goulioukk, J. M. McGlone, J. F. Wager, "Side-By-Side Comparison of Single and Dual Active Layer Oxide TFTs: Experiment and TCAD Simulation," accepted in *IEEE Transactions on Electron Devices* (2017).

6.1 Introduction

A DAL oxide TFT was first reported in 2008 by Kim et al. [62] as a way to increase the mobility compared to that of a conventional SAL TFT. The general idea of the DAL TFT is to match a high mobility (but undesirably high carrier concentration) semiconductor such as ITO with a low carrier concentration AOS such as a-IGZO

to achieve both high mobility and reasonable threshold voltage. This concept is similar to the traditional silicon MOSFET, where the channel has various regions with different carrier concentrations (doping implants) to improve the performance.

The optimum thickness of the high mobility interface layer (*I-layer*) was found to be between 3 and 6 nm when matched with a thicker low carrier concentration layer (*B-layer*) of around 30 nm [68, 74, 67]. This agrees with the experimental results in this work. In general, a trade-off exists where a thicker I-layer results in a higher mobility but also a more negative threshold voltage (data shown in Appendix B.1).

Figure 6.1 shows transfer curves for three DAL TFTs (straight lines) with stacks of ITO-AITO, BIO-AITO, and ITO-IGZO, respectively. Additionally, transfer curves are shown of TFTs fabricated with the respective single layers of the DAL stack (dotted lines). All channel layers are deposited via sputtering and annealed at 200 or 300 °C. Detailed information of the AITO AOS can be found in Ref. [139]. Overall, the transfer curve of the DAL TFT tends to lie between the two respective SAL TFTs. However, the mobility of the DAL TFT is much closer to the mobility of the SAL TFT which is used as the I-layer in the DAL stack, as depicted in Fig. 6.2. This is explained by the fact that the accumulation layer is formed in the I-layer (at the gate insulator/channel interface) where the majority of carrier transport occurs.

The next part of this chapter is devoted to the characterization and discussion of the ITO-IGZO DAL stack.

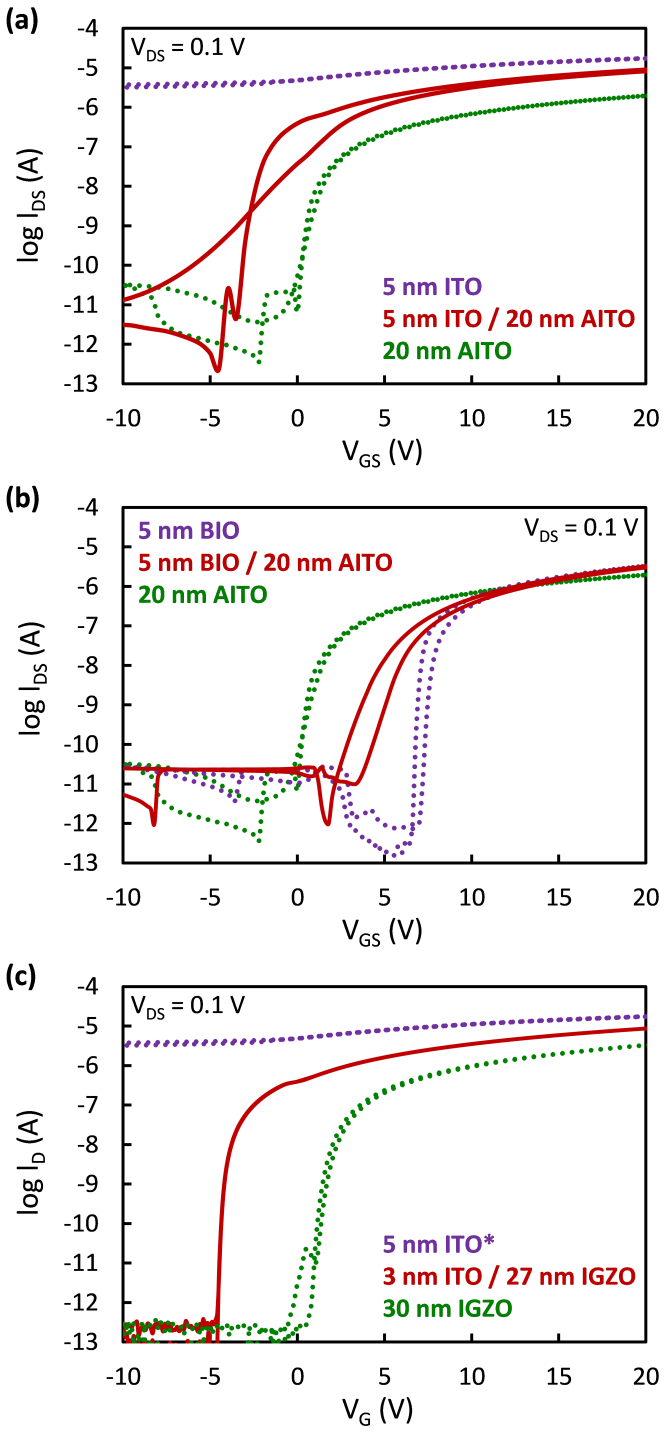

Figure 6.1: Transfer curves of SAL and DAL TFTs for (a) ITO-AITO, (b) BIO-AITO, and (c) ITO-IGZO channel layers. W/L = 1000 μm/200 μm for all devices.

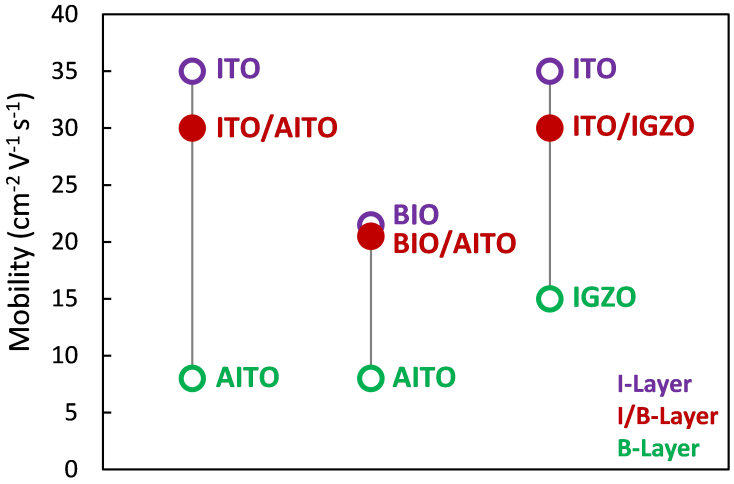

Figure 6.2: Summary of field-effect mobility for SAL and DAL TFTs.

6.2 Thin Film Characterization

Thin films are deposited via RF sputtering. Sputtering conditions for both the ITO (10 wt. % tin oxide doped indium oxide) and a-IGZO are kept the same and are as follows: pressure of 5 mTorr, applied RF power density of 3.82 W cm^{-2}, and a process gas ratio of $O_2/(Ar+O_2)$ = 10 %. For the DAL stack ITO and a-IGZO are deposited subsequently without delay nor breaking vacuum. No intentional heating is used during sputtering. A post-deposition anneal of 300 °C for one hour is performed in air.

The device characteristics strongly depend on the thickness of the ITO (I-layer). Therefore, the thickness of the ITO layer and to a lesser degree of the a-IGZO must be known precisely. The XRR measurement results of ITO and a-IGZO thin films are shown in Fig. 6.3. For the deposition conditions used in this study, the ITO and a-IGZO process exhibit a deposition rate of 3.0±0.2 nm/min and 2.0±0.2 nm/min, respectively.

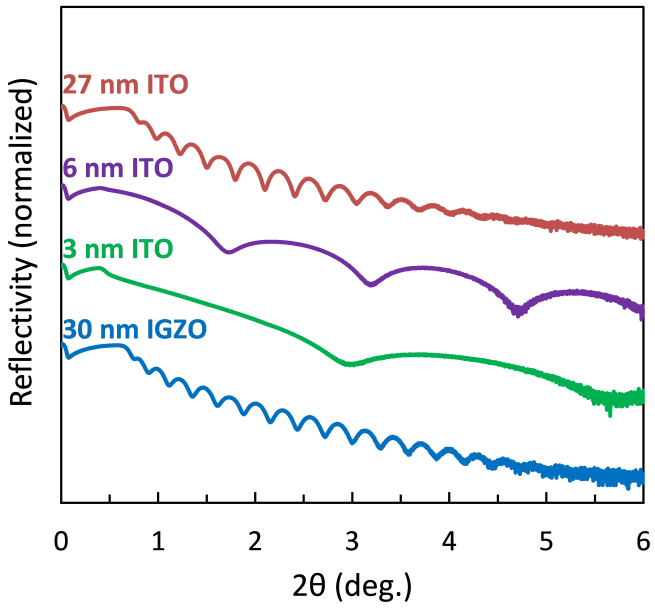

Figure 6.3: XRR measurement of ITO and a-IGZO thin films on glass substrates.

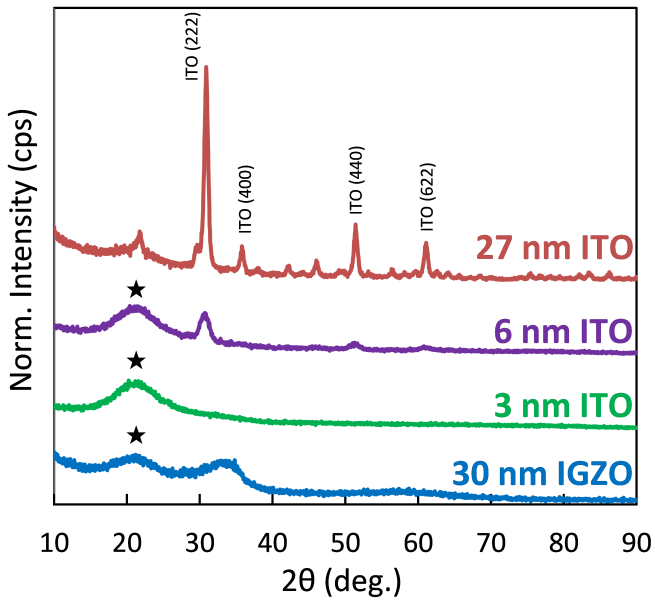

Figure 6.4: GI-XRD measurement of ITO and a-IGZO thin films on glass substrates.

GI-XRD results of the same thin films are shown in Fig. 6.4. IGZO is known to be amorphous below 600 °C and this is verified by GI-XRD measurement, characterized by the broad amorphous hump and absence of any diffraction peaks. Thicker ITO films are typically polycrystalline, as shown by the ITO film with a thickness of 27 nm in Fig. 6.4. A nano-/polycrystalline morphology is observed in the GI-XRD pattern of the 6 nm thin ITO layer. No crystalline peaks are detected in the GI-XRD pattern of the 3 nm ITO film. However, 3 nm is at or slightly below the minimum film thickness required for a reliable GI-XRD measurement. Therefore, the surface roughness is analyzed to verify the result using an Asylum Research MFP-3D atomic force microscope (AFM) in contact mode. AFM of the 3 nm ITO shows a continuous and smooth surface with an RMS roughness of 0.24 nm, as depicted in Fig. 6.5(b). Surface roughness increases from 0.18 nm (near the noise floor) for a-IGZO to 0.46 nm for polycrystalline ITO with a thickness of 27 nm. An amorphous nucleation layer is often observed in polycrystalline oxide thin films before grain growth occurs [140]. In the DAL case, the ITO layer consists entirely of the amorphous nucleation layer because it is ultra thin. An amorphous DOS model is used in the simulation for both the ITO and a-IGZO layers.

The band gap is obtained from optical spectroscopy using a Tauc plot, as shown in Fig. 6.6. The band gap is approximately 3.2 eV for both ITO and a-IGZO.

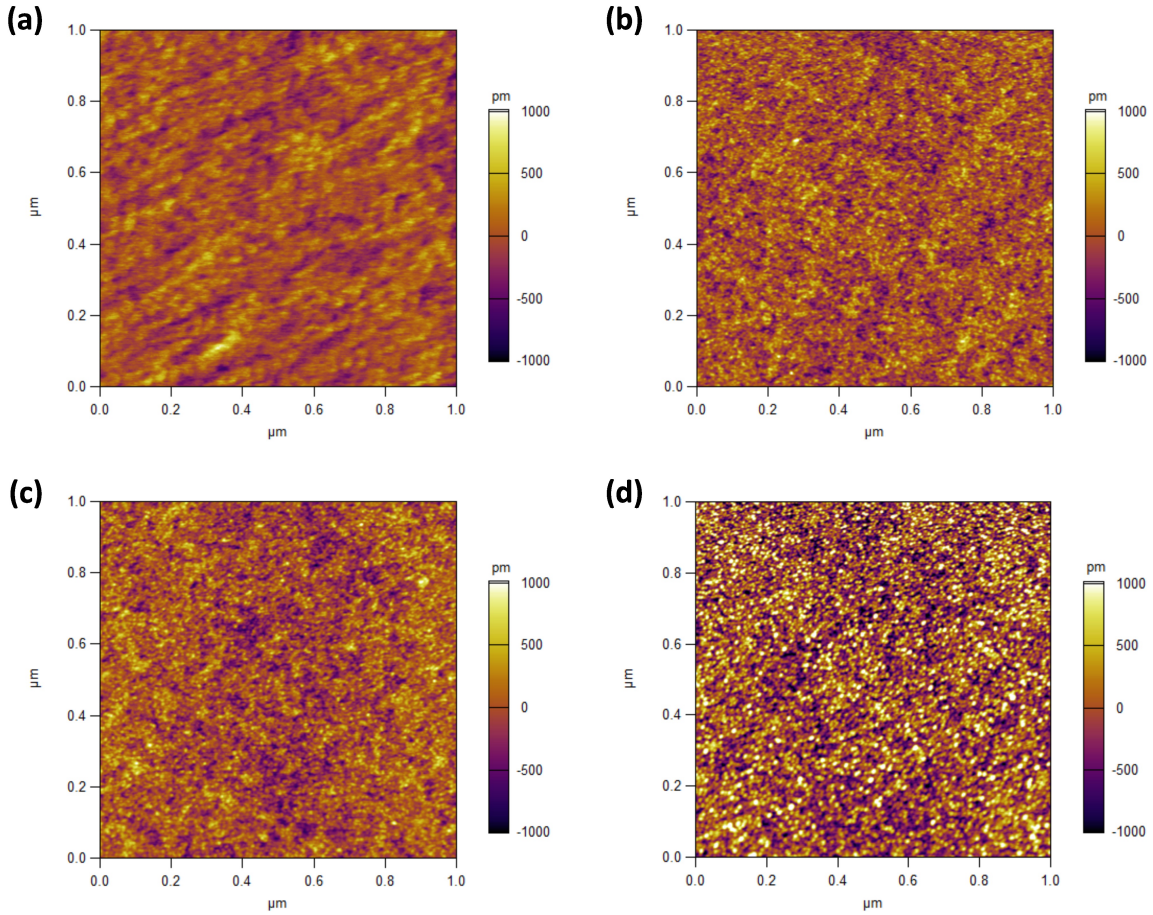

Figure 6.5: Atomic force microscopy measurement on thermal oxide/silicon substrates of (a) 30 nm a-IGZO, (b) 3 nm ITO, (c) 6 nm ITO, and (d) 27 nm ITO thin films.

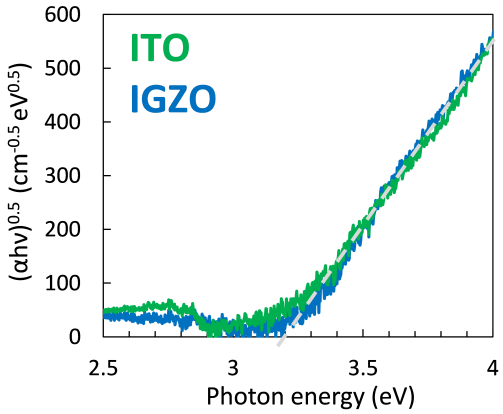

Figure 6.6: Optical spectroscopy of ITO and a-IGZO thin films on glass substrates.

6.3 Device Characterization

Staggered, bottom-gate TFTs are fabricated on p-type Si substrates with a Cr/Au coated back side to act as the gate electrode. The gate insulator (GI) is composed of 100 nm thermal silicon oxide. The channel layer is processed using the same conditions as the thin films. The SAL channel is comprised of 30 nm of a-IGZO and the DAL channel of 3 nm ITO/27 nm a-IGZO. After the post-deposition anneal, source/drain contacts are formed by thermal evaporation of aluminum. The channel layer and source/drain areas are patterned via shadow mask. The final device has dimensions of width/length (W/L) = 2000 µm/200 µm.

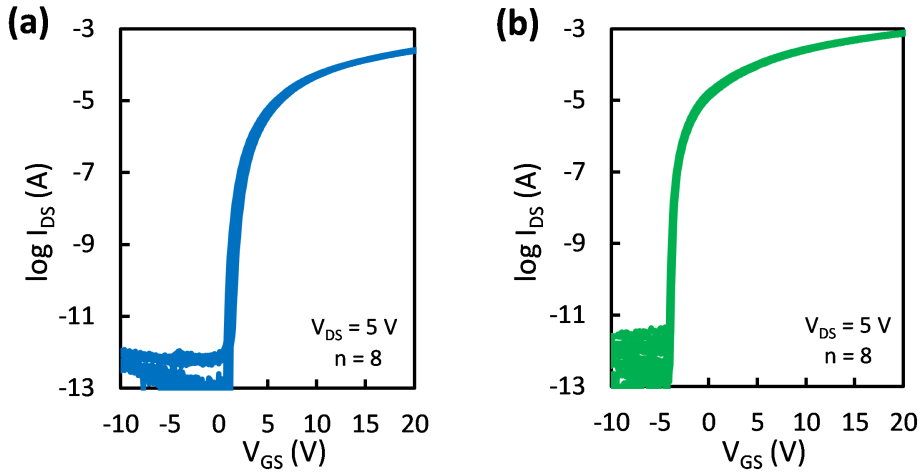

Figure 6.7: Transfer characteristics (forward and reverse sweep) of (a) single active layer (SAL) and (b) dual active layer (DAL) devices.

Figure 6.7(a) shows the transfer characteristics (forward and reverse sweep) of eight SAL devices. They exhibit a mean V_{TH} of 1.78 V, μ_{FE} of 13.3 $cm^2V^{-1}s^{-1}$, I_{ON} of 110 nA/µm, S of 350 mV/dec, hysteresis of 302 mV, and excellent uniformity. The device parameters are summarized in Table 6.1. Mean values are given with the standard deviation in parentheses (n = 8). The transfer characteristics of eight DAL

Table 6.1: Device parameters for SAL and DAL TFTs.

Parameter	**SAL**	**DAL**
V_{TH} (V)	1.78 (± 0.13)	-3.63 (± 0.10)
μ_{FE} ($cm^2V^{-1}s^{-1}$)	13.3 (± 0.2)	31.6 (± 0.8)
I_{ON} (nA/μm)	110 (± 3)	345 (± 11)
S (mV/dec)	350 (± 9)	175 (± 8)
Hyst. (mV)	302 (± 18)	32 (± 11)

devices are shown in Fig. 6.7(b). Mean mobility increased twofold, I_{ON} by a factor of 3, devices are twice as steep, and hysteresis decreased by one order of magnitude.

An overlay, i.e., transfer curves are parallel shifted to exhibit matching turn-on, for a representative SAL and DAL device is shown in Fig. 6.8(a). The overlay clearly shows the smaller sub-threshold swing for the DAL device as well as the higher mobility at the same gate overvoltage. The sub-threshold swing as a function of drain current for both forward and reverse sweep is shown in Fig. 6.8(c). The DAL TFT exhibits an improved sub-threshold swing throughout the whole sub-threshold region with a minimum value reaching 73 mV/dec which is an excellent result for an oxide TFT. A sub-threshold swing below 80 mV/dec for an oxide TFT was also reported by Asami et al. [141]. However, their gate insulator was comprised of a much smaller equivalent oxide thickness (EOT) of 9.3 nm. The higher mobility of the DAL device also results in an increased drain current as is apparent in the output characteristics shown in Figs. 6.8(b) and (d). As expected, both SAL and DAL devices exhibit good saturation.

Next, the stability of the devices is investigated. SAL and DAL TFTs are subjected to positive bias temperature stress (PBTS) of $V_{GS} = +20$ V and temperature of 60 °C for 60 minutes. The evolution of transfer characteristics with increasing stress time

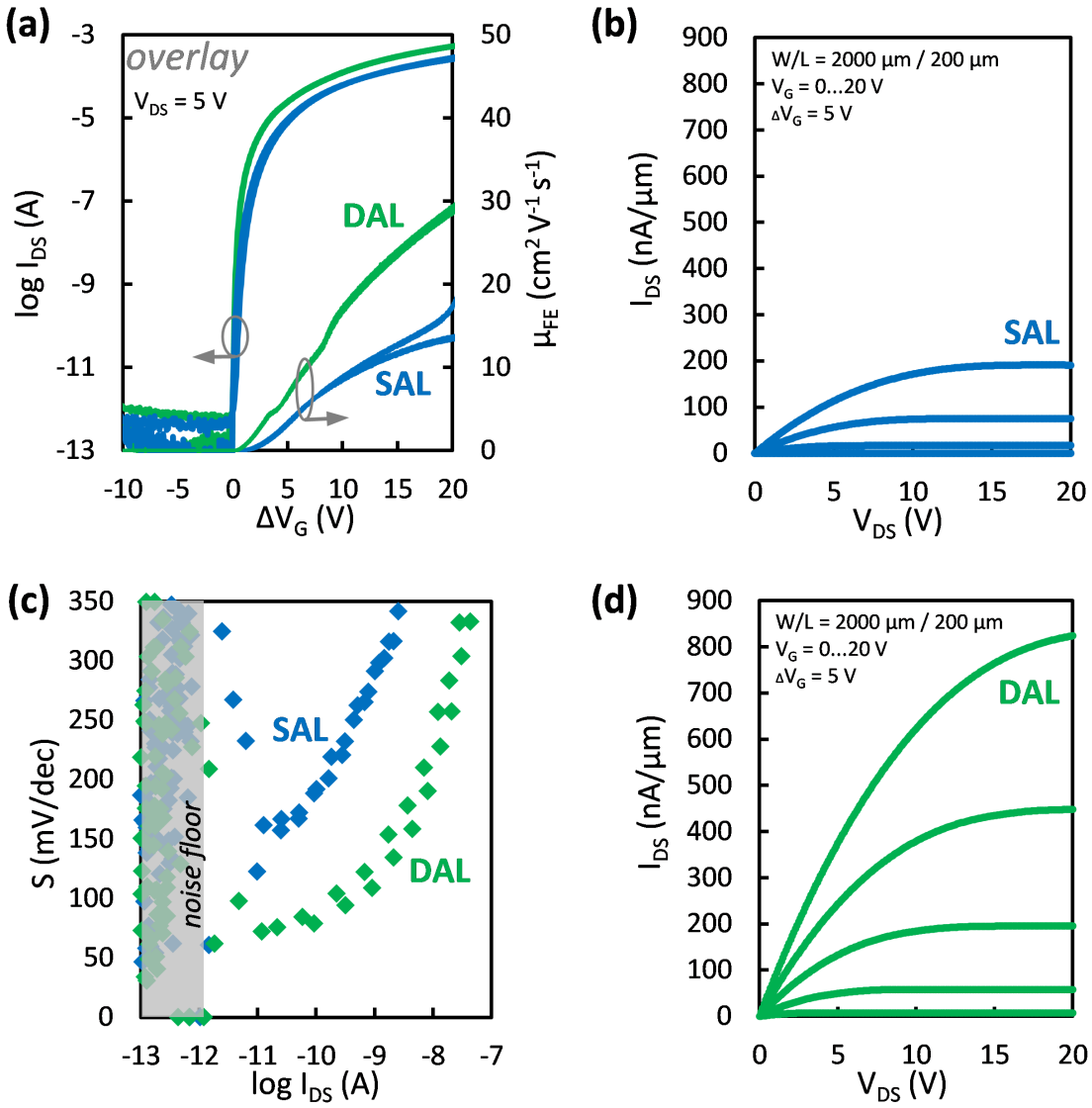

Figure 6.8: (a) Overlay of transfer characteristics of SAL and DAL device, (b) output characteristics of DAL device, (c) comparison of sub-threshold swing of SAL and DAL device, and (d) output characteristics of DAL device.

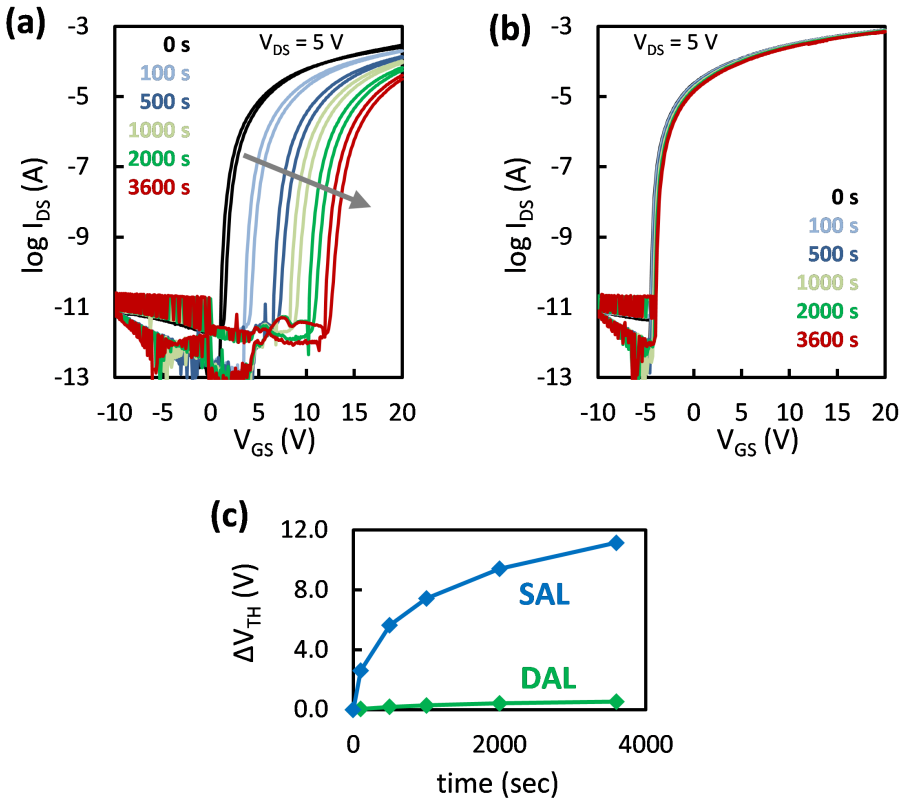

Figure 6.9: Evolution of transfer characteristics for (a) SAL and (b) DAL device with increasing PBTS time and (c) shift of threshold voltage with increasing PBTS time.

for the SAL and DAL device is shown in Fig. 6.9(a) and 6.9(b), respectively. The SAL device shows a large V_{TH} shift of 11.2 V, as summarized in Fig. 6.9(c). In comparison, the DAL device shows a dramatically improved stability with a shift of only 0.5 V after 60 minutes.

Both SAL and DAL TFTs exhibit negligible threshold voltage shift (less than 1 V) after 60 minutes of negative bias temperature stress (NBTS) with V_{GS} = -20 V and 60 °C. This changes when SAL and DAL TFTs are subjected to negative bias temperature illumination stress (NBTIS) with V_{GS} = -20 V, 60 °C, and employing a white light source. Both SAL and DAL devices show significant threshold voltage

shift after 60 minutes of NBTIS, as shown in Fig. 6.10. Interestingly, the stressed SAL device develops a *kink*-behavior (more severe in the reverse sweep), which also degrades the sub-threshold swing. In comparison, the stressed DAL device exhibits a more constant sub-threshold swing degradation throughout the whole sub-threshold region (more severe in the forward sweep) and without any obvious kink. These differing phenomena could give insight into the type of defect creation/carrier trapping and their location with respect to location and energy that likely occur during stress. Understanding the fundamental reason for these instability mechanisms is a topic of ongoing research.

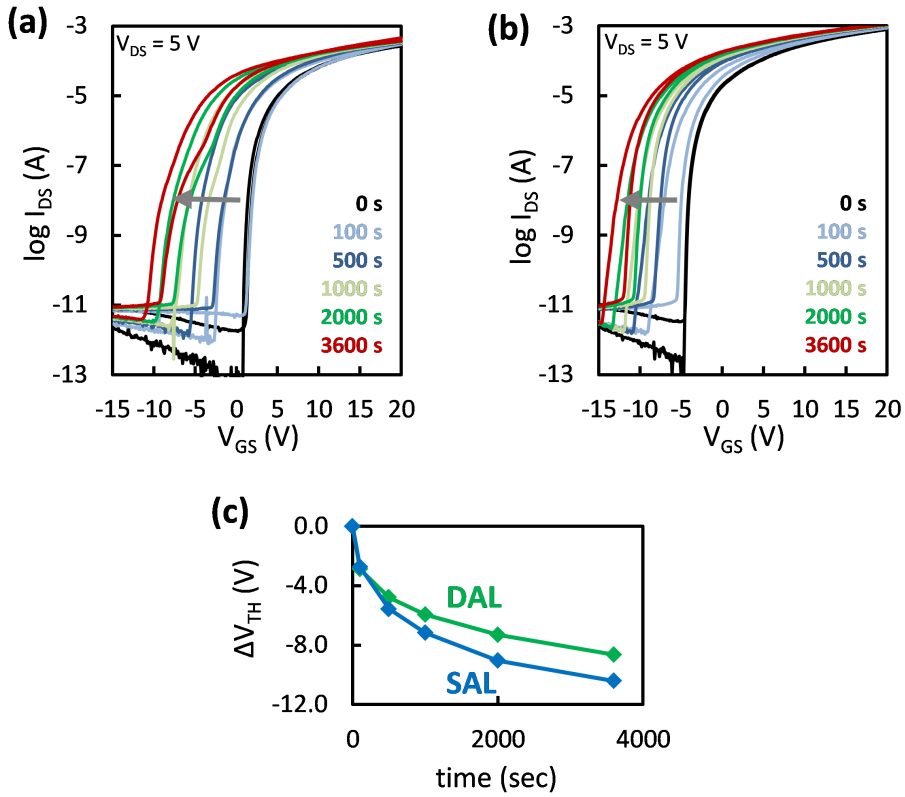

Figure 6.10: Evolution of transfer characteristics for (a) SAL and (b) DAL device with increasing NBTIS time and (c) shift of threshold voltage with increasing NBTIS time.

6.4 TCAD Simulation

Silvaco Atlas 2D device simulation is used to investigate the SAL and DAL devices, particularly the difference in the DOS. The simulation is supported with parameters from as many physical measurements as possible.

6.4.1 Mapping Technique

Fit of transfer characteristics is accomplished using the following procedure. First, known physical parameters are set in the simulation model, summarized in Table 6.2, and remain unchanged.

Table 6.2: General simulation parameters.

Parameter	**ITO**	**IGZO**
Effective mass, electrons (m_0)	0.30 [12]	0.34 [101]
CB effective DOS (cm^{-3})	4.1×10^{18}	5.0×10^{18}
Band gap (eV)	3.2	3.2
Electron affinity (eV)	4.16	4.16
Rel. permittivity (unitless)	9 [12]	10 [102]
Band mobility ($cm^2V^{-1}s^{-1}$)	35	15
Carrier concentration (cm^{-3})	3.63×10^{18}	-

Second, the DOS profile is adjusted until the simulation and experiment converge. To achieve this a mapping technique is used, as shown in Fig. 6.11. In the simulation, the Fermi level position is continuously probed while the bias is ramped. The virtual probe is located at the accumulation layer (near gate insulator/channel interface) and centered along the channel width. As a result, both drain current and Fermi level position are known as a function of gate voltage. Accordingly, any part of the Fermi

level curve and, hence, transfer curve can be mapped to a corresponding energy in the DOS profile. In Figs. 6.11(b) and 6.11(c) the valence band mobility edge (E_V) is located at 0 eV and the conduction band mobility edge (E_C) at 3.2 eV.

For easier visualization, the transfer curve in Fig. 6.11(a) is divided into five sections. Each numbered and colored section has a corresponding region in the Fermi level vs. gate voltage (Fig. 6.11(b)) and energy vs. DOS (Fig. 6.11(c)) plots.

In section I the device is negatively biased and in the off-state. As a result, the Fermi level is positioned below mid-gap.

In section II, around $V_{GS} = 0$ V, the Fermi level experiences a low defect density with respect to energy. Thus, little change in gate voltage is required to move the Fermi level abruptly towards the conduction band, as depicted in Figs. 6.11(b) and 6.11(c). The TFT turns on at $V_{GS} = 1$ V. At this point, the Fermi level is at ~2.8 eV (or ~0.4 eV below E_C).

Section III encompasses the sub-threshold region of the device. In this region, the Fermi level again reaches a higher density of defects near the conduction band and further modulation of the Fermi level requires application of a larger gate voltage, as shown in Fig. 6.11(b).

Examining section III in Fig. 6.11(c), it becomes clear that the sub-threshold behavior is dominated by the shallow donor states around 2.95 eV (or 0.25 eV below the conduction band). An increase (decrease) of these shallow donor states results in an increase (decrease) of the sub-threshold swing in the simulated transfer curve.

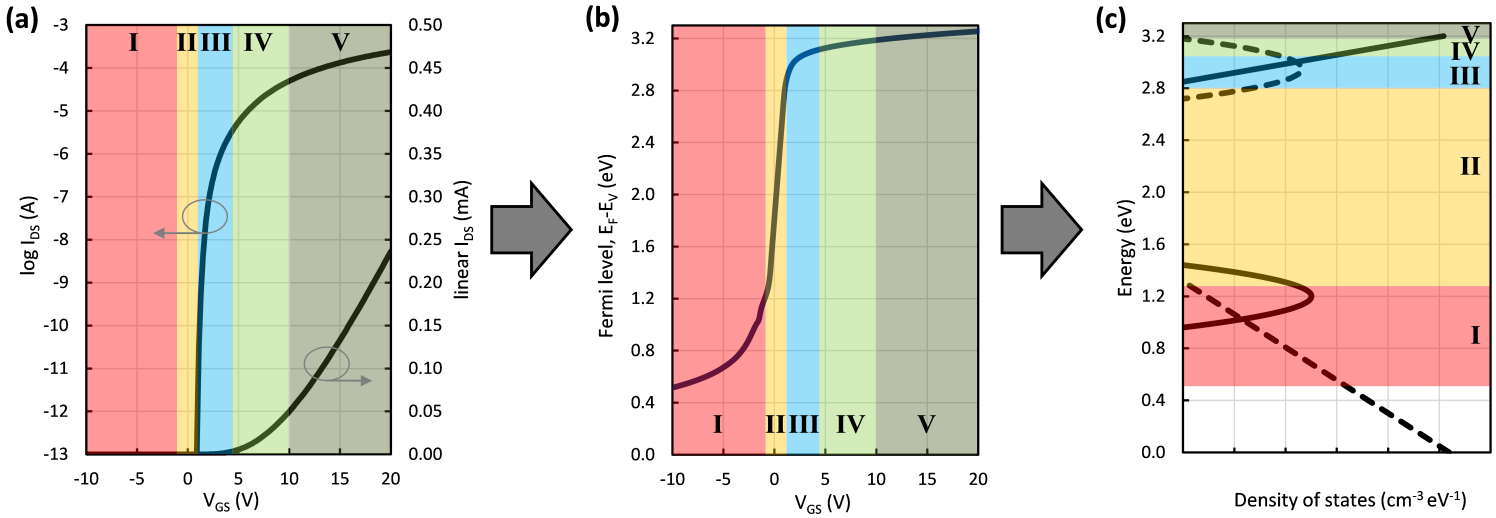

Figure 6.11: Mapping electrical I-V characteristics to sub-bandgap density of states via (a) drain current as a function of gate voltage to (b) Fermi level position as a function of gate voltage to (c) energy as a function of density of states.

In section IV and V, the TFT is in the on-state. Focusing on the linear plot of the transfer characteristics in Fig. 6.11(a) and the upper part of Fig. 6.11(c), the TCAD simulation suggests that from a DOS perspective the on-current is dominated by the conduction band Urbach energy and the peak density of conduction band band-tail states, N_{TA}. This agrees well with previous assessments of amorphous semiconductor transport modeling (Ref. [3] and Chapter 3). At $V_{GS} = 10$ V (at the transition of section IV and V), the Fermi level moves above the conduction band mobility edge according to the simulation.

6.4.2 Simulation Discussion

The sub-bandgap state nomenclature employed in Fig. 6.13 and Table 6.3 is as follows. The acceptor band-tail (TA) states are defined by the peak density, N_{TA}, and the Urbach energy (slope), W_{TA}. The shallow gaussian donor (GD) states are defined by the peak density, N_{GD}, the characteristic decay energy (i.e., the standard deviation of the gaussian distribution), W_{GD}, and the peak energy, E_{GD}. The gaussian deep acceptor (GA) states are defined by the peak density, N_{GA}, the characteristic decay energy, W_{GA}, and the peak energy, E_{GA}. The donor band-tail (TD) states are defined by the peak density, N_{TD}, and the Urbach energy (slope), W_{TD}.

Figure 6.12(a) shows the experimental and simulated transfer characteristics of the SAL device for $V_{DS} = 0.5$ and 5 V both on a log and linear scale. Similarly, Figure 6.12(b) shows the transfer characteristics of the DAL device. Excellent agreement between experiment and simulation is achieved.

To first order, GI/channel interface states and bulk states are interchangeable in the simulation. Magnitude and units are easily converted by multiplying/dividing

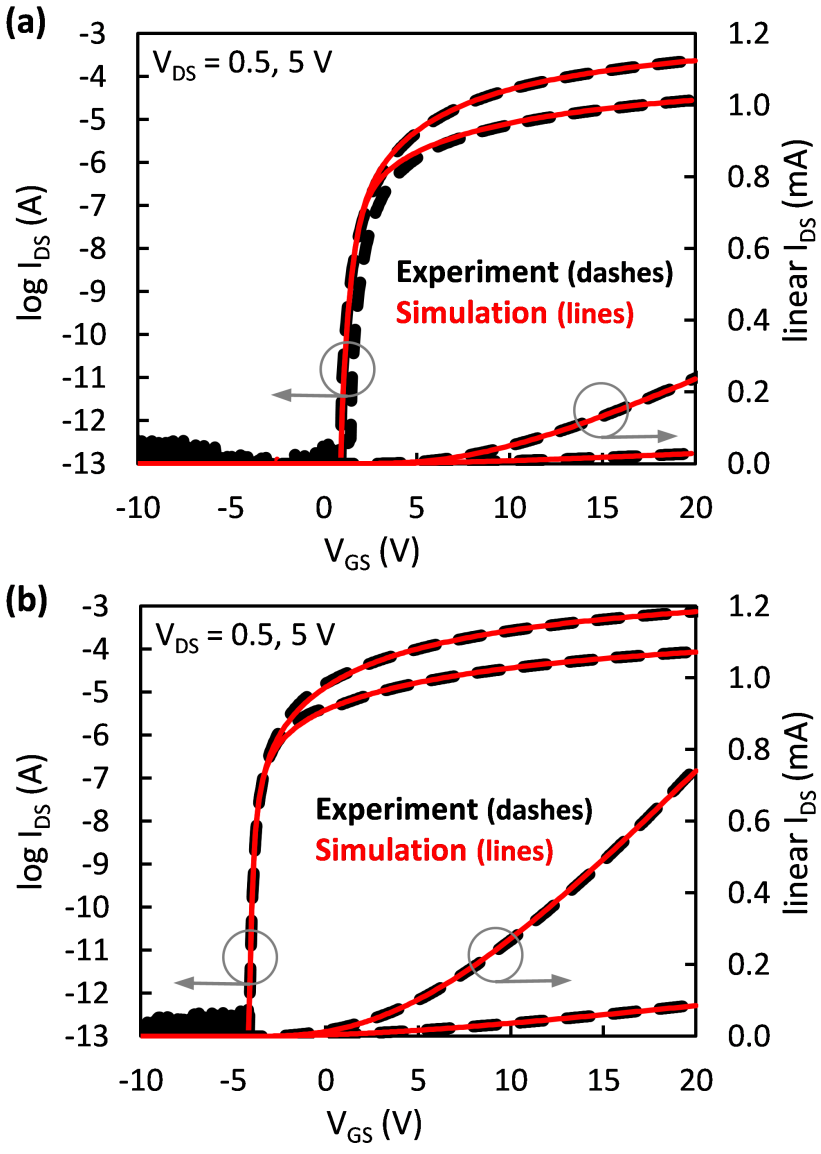

Figure 6.12: Comparison of experimental and simulated transfer characteristics of (a) SAL and (b) DAL device.

Table 6.3: Simulation DOS parameters.

Parameter	**ITO**	**IGZO**
N_{TA} ($cm^{-3}eV^{-1}$)	2.20×10^{20}	1.21×10^{20}
W_{TA} (meV)	18	30
N_{GA} ($cm^{-3}eV^{-1}$)	-	3.20×10^{17}
W_{GA} (eV)	-	0.1
E_{GA} (eV)	-	1.2
N_{TD} ($cm^{-3}eV^{-1}$)	1.55×10^{20}	1.55×10^{20}
W_{TD} (meV)	110	110
N_{GD} ($cm^{-3}eV^{-1}$)	-	1.60×10^{16}
W_{GD} (eV)	-	0.1
E_{GD} (eV)	-	2.95
D_{IT} ($cm^{-2}eV^{-1}$)	$< 6.0 \times 10^{10}$	6.0×10^{11}

by channel thickness. Hence, interface and bulk defect states which are otherwise identical, i.e., with respect to magnitude and energy distribution, are nearly indistinguishable in the simulation. However, the a-IGZO layer for both the SAL and DAL device is processed identically. Therefore, the bulk DOS of a-IGZO should be the same in both cases. As a result, interface traps (D_{IT}) of 6.0×10^{11} $cm^{-2}eV^{-1}$ are introduced in the SAL case in order to achieve agreement between experiment and simulation. The a-IGZO bulk DOS and interface trap distribution are depicted in Fig. 6.13(a) and summarized in Table 6.3. The interface traps have the same characteristic decay energy of 0.1 eV and the same peak energy of 2.95 eV as the shallow donor bulk states.

The interface trap density is at least one order of magnitude smaller in the DAL case, at which point the observational error margin of our simulation is reached. Pristine thermal silicon oxide on silicon, which is the best known gate insulator interface,

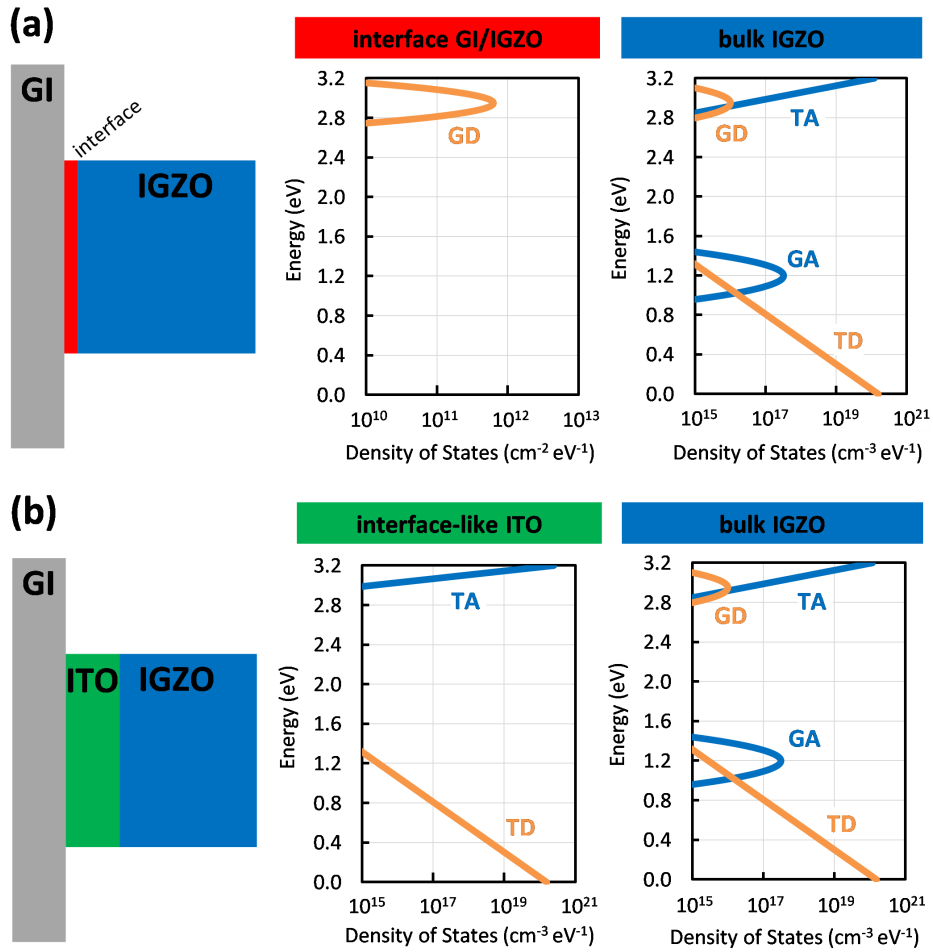

Figure 6.13: DOS of interface and channel layer for (a) SAL device and (b) DAL device.

has a defect density of low-10^{10} $cm^{-2}eV^{-1}$ [108] and this is likely the lower limit. Hence, for the DAL case, the D_{IT} value can be bound between 1×10^{10} and 6×10^{10} $cm^{-2}eV^{-1}$. This small interface trap density in the DAL device could be a result of the high carrier concentration of the ITO, which is extracted to 3.63×10^{18} cm^{-3}. Essentially the traps at the interface are filled/neutralized(passivated) by the high density of free carriers in the ITO. As a result, the DAL TFT has a significantly

improved sub-threshold swing, mobility and hysteresis compared to the SAL TFT.

Besides the small D_{IT}, the following consideration may also contribute to the improved performance of the DAL device. ITO and a-IGZO both have an oxygen anion derived valence band. This means that the ionization potential for both ITO and a-IGZO will be approximately the same, based on the solid state energy scale [142]. Furthermore, using the described process conditions, ITO and a-IGZO exhibit the same band gap of ~3.2 eV. Therefore, the junction between ITO and a-IGZO is modeled as a homojunction. This is different than the model for an ITZO-IGZO DAL TFT proposed by Rim et al. [56] where their band alignment results in a conduction band offset between interface and bulk channel layer, similar to a heterojunction field-effect transistor (HFET). That being said, the higher carrier concentration in the ITO compared to a-IGZO creates a similar band bending effect in the conduction band for the ITO-IGZO DAL. Figure 6.14 depicts the simulated potential of the ITO-IGZO channel as well as the energy band bending across the channel in equilibrium ($V_S = V_D = V_G = 0$ V). Cutline ① shows the energy band diagram at the source electrode where a band bending of 0.06 eV is observed from the ITO to the maximum height, roughly half-way along the channel. Cutline ② shows the energy band diagram at the center of the channel where band bending of 0.11 eV is observed from the ITO to the maximum height at the backside of the channel. Note that the potential variation across the channel is also caused by the different work functions of the Al source/drain (4.16 eV), p-type Si gate (5.25 eV), and ITO/IGZO electron affinity (4.16 eV).

The simulation code for both SAL and DAL cases is provided in Appendix D.

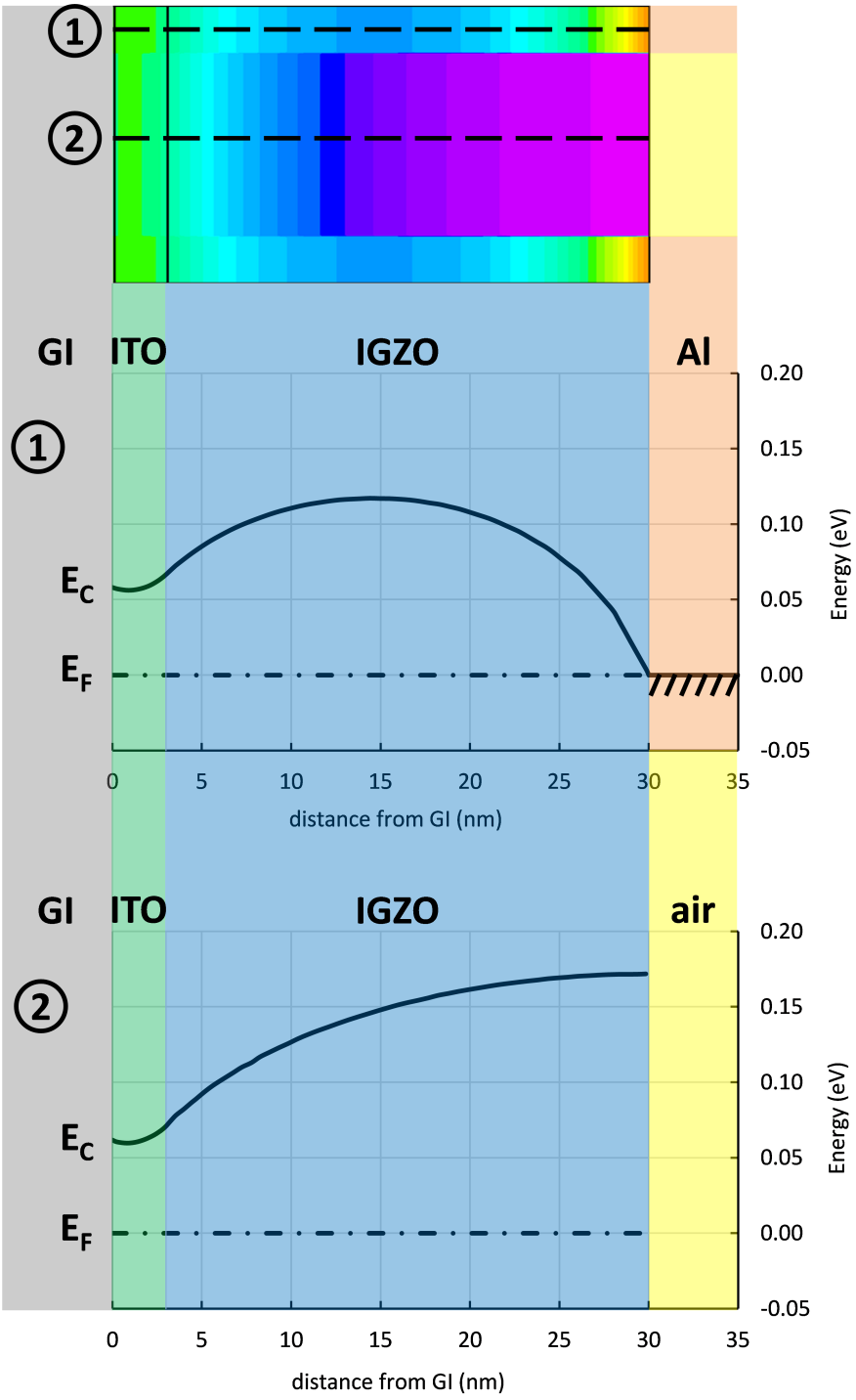

Figure 6.14: Energy band diagram of ITO-IGZO channel layer in equilibrium. Cutline ① is at the source Al metal electrode and cutline ② at the center of the channel.

6.5 A Novel DAL TFT Concept

The results from the previous section clearly demonstrate that a DAL TFT has improved mobility compared to an a-IGZO SAL TFT. What if an even higher mobility than that is required? As described in Chapter 3, the upper limit to amorphous semiconductor mobility is ultimately limited by carrier trapping in band-tail states, which are intrinsic to an amorphous microstructure.

The goal here is to investigate whether a crystalline semiconductor can be employed for the interface layer in a DAL TFT, as depicted in Fig. 6.15, while at the same time using a fabrication process that is suitable for large-area manufacturing. First, the dual layer stack of I-layer (low crystallization temperature, T_X) and B-layer (high T_X) is deposited. Then, with a single post-deposition anneal, the I-layer is (further) crystallized while the B-layer remains amorphous. The aim is to achieve a *controlled morphology* because the I-layer is crystallized while it is capped with an amorphous layer.

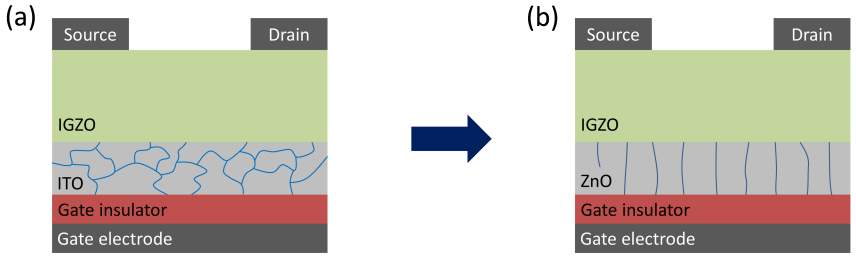

Figure 6.15: (a) Conventional DAL TFT with amorphous/nanocrystalline ITO interface layer and (b) proposed DAL TFT with (poly)crystalline ZnO interface layer.

Single-crystal ZnO and In_2O_3 both exhibit a large Hall mobility of ~200 $cm^2V^{-1}s^{-1}$ at low carrier concentrations, as shown in Fig. 6.16(a). Therefore, both ZnO and In_2O_3 seem to be suitable candidate semiconductors for use as the interface layer.

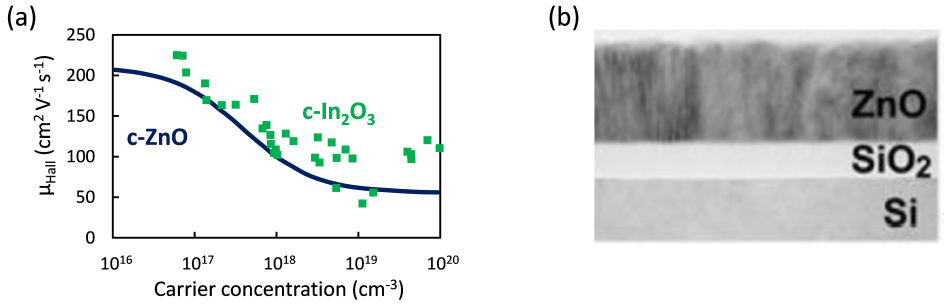

Figure 6.16: (a) Hall mobility data from the literature of single-crystal ZnO [11] and single-crystal In_2O_3 [12] and (b) TEM image of c-axis aligned ZnO [13].

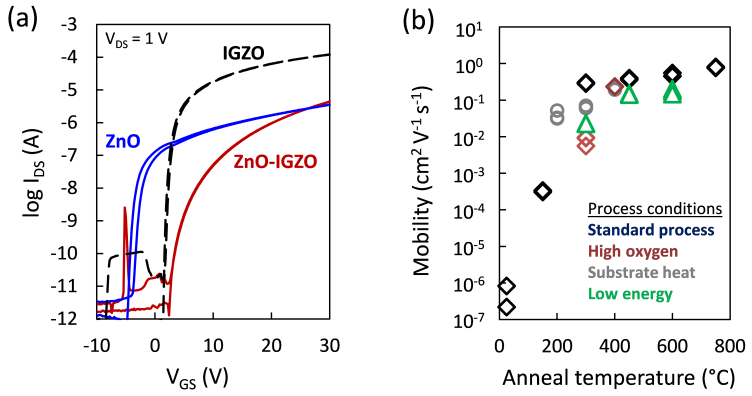

Figure 6.17: (a) Summary of field-effect mobility of ZnO TFTs with varying process conditions and (b) transfer characteristics of ZnO, a-IGZO, and ZnO-IGZO TFTs.

ZnO was chosen due to its larger natural abundance and lower cost. Reports in the literature have demonstrated that ZnO thin films deposited via sputtering can create well-ordered, c-axis aligned columnar grains, as shown in Fig. 6.16(b).

ZnO-IGZO TFTs fabricated in this work with a DAL stack of 5 nm ZnO and 25 nm a-IGZO exhibit a very small mobility of ~0.5 $cm^2V^{-1}s^{-1}$ compared to ~15 $cm^2V^{-1}s^{-1}$ for the 30 nm IGZO 'control' TFT (both annealed at 300 °C). The corresponding transfer curves are shown in Fig. 6.17(a). The poor performance of the ZnO-IGZO TFTs is attributed to the ZnO interface layer. This is confirmed by fabrication of

ZnO SAL TFTs. The mobility of the ZnO TFTs is consistently below 1 $cm^2V^{-1}s^{-1}$, as summarized in Fig. 6.17(b). The various sputtering conditions used are as follows: 'standard process' = 5 mTorr, 75 W, 10 % O_2 flow, room temperature (RT); 'high oxygen' = 5 mTorr, 75 W, 20 % O_2 flow, RT; 'substrate heat' = 5 mTorr, 75 W, 10 % O_2 flow, 300 °C substrate heating; 'low energy' = 8 mTorr, 50 W, 10 % O_2 flow, RT. A representative ZnO TFT transfer curve is also shown in Fig. 6.17(a) ('standard process', 450 °C anneal).

Materials analysis via XRD shows that the ZnO thin films exhibit the desired (002) c-axis phase but also a secondary (103) phase, as depicted in Fig. 6.18. In this work, substrate heating does not result in higher c-axis alignment, contrary to literature reports [40, 42]. Additionally, c-axis alignment does not significantly improve with increasing O_2 flow (shown in Fig. 6.18(b)), type of substrate (glass substrate, Si wafer, thermally oxidized Si wafer), or film thickness (50 to 500 nm). Scherrer analysis estimates grain sizes of approximately 10 nm, independent of anneal temperature.

Next, zinc chloride ($ZnCl_2$) is investigated as a *crystallization catalyst* to enhance the crystallinity and, ideally, the c-axis alignment of the ZnO thin films. Two different experiments are undertaken, a) ZnO is deposited on top of a $ZnCl_2$ thin film and b) the $ZnCl_2$ is 'sandwiched' between two ZnO thin films. The ZnO thin film is deposited via sputtering and $ZnCl_2$ thin film is deposited via solution-processing. However, $ZnCl_2$ formed a very acidic solution (possibly forming HCl) and visibly etching the ZnO thin film. Furthermore, the c-axis alignment of the ZnO stack is not enhanced. Still, the idea of incorporating a crystallization catalyst is promising and Hwang et al. (2016) published a report with a very similar goal although using a different approach [143].

They deposited tantalum metal on the channel backside, aiming to crystallize the amorphous ZTO channel and thus to increase the TFT mobility.

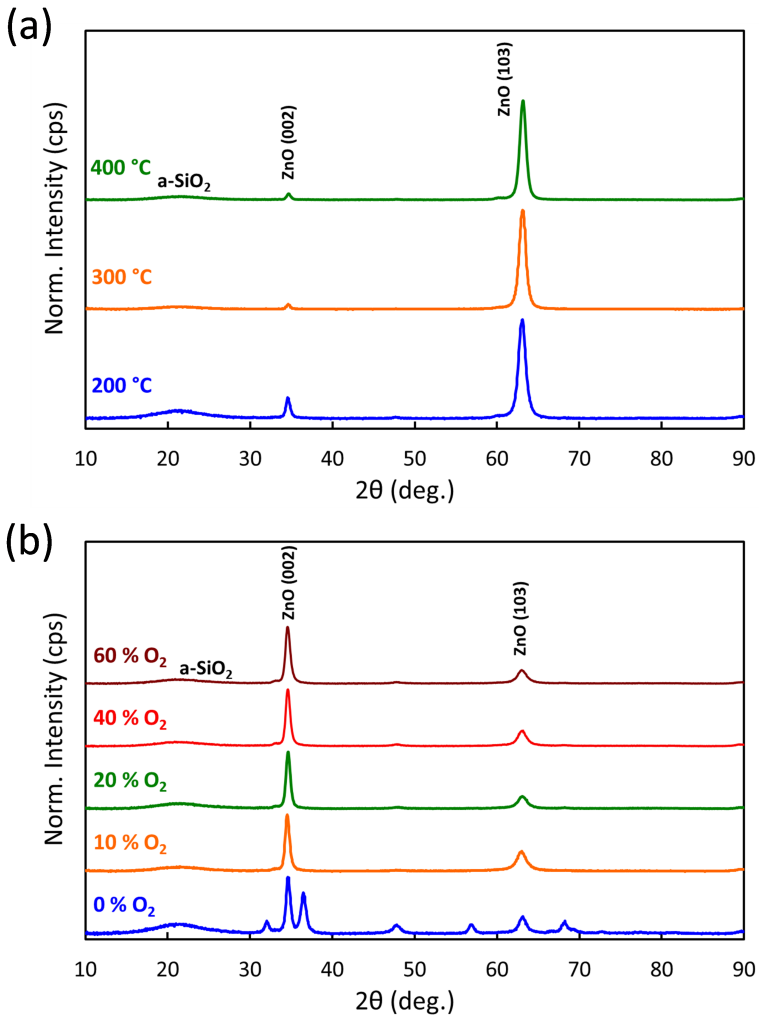

Figure 6.18: (a) GI-XRD data of ZnO thin films on glass substrates for (a) varying deposition temperature (10 % O_2) and (b) varying O_2 flow during deposition (at room temperature).

6.6 Conclusion

In summary, DAL TFTs of ITO-AITO, BIO-AITO, ITO-IGZO, and ZnO-IGZO are fabricated. The ITO-IGZO DAL TFT is extensively characterized and exhibits significantly improved performance compared to an a-IGZO SAL TFT with mobility of 31 $cm^2V^{-1}s^{-1}$, sub-threshold swing of 175 mV/dec, minimal hysteresis, and good PBTS stability. Excellent agreement between experiment and physically-based TCAD simulation is achieved. A mapping technique is introduced to relate experimental transfer characteristics to the sub-bandgap DOS model. Simulation suggests that the DAL TFT has a much smaller interface trap density, presumably due to the large free carrier concentration of the ITO, leading to a reduced number of participating interface traps during TFT operation. The root-cause for the low mobility of the ZnO and, therefore, of the ZnO-IGZO DAL TFT is believed to be because of insufficient c-axis alignment.

CHAPTER 7: CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusions

The goal of the research presented is to assess the maximum mobility in amorphous semiconductors and to fabricate high mobility oxide TFTs using novel channel layers.

First, a framework is provided for the development of new high-performance TFT channel layer materials. A physics-based model is presented which predicts a maximum amorphous semiconductor mobility of ~71 $cm^2V^{-1}s^{-1}$ (~16 $cm^2V^{-1}s^{-1}$) for electrons (holes). The model shows that amorphous semiconductor mobility is ultimately limited by carrier trapping in band tail states which are intrinsic to amorphous semiconductors. If a semiconductor mobility exceeding these limits is required, a crystalline semiconductor must be employed. Polar optical phonon scattering seems to establish an approximate upper mobility limit for single crystal polar semiconductors. However, when going to a polycrystalline channel layer, grain size scattering and energy barriers introduced by grain boundaries impede carrier transport, as does an increased defect density, compensation, and carrier trapping.

Second, one possible way to achieve a mobility beyond that of a-IGZO is to reduce the number of cations and to increase the fraction of mobility-boosting indium oxide. A novel cation, boron, is investigated. Boron is compelling because of its strong affinity for bonding to oxygen and its small size. Boron indium oxide (BIO) is designed with these considerations in mind and is experimentally characterized. As

hypothesized, boron indeed acts as carrier suppressor and as a surprisingly effective amorphous phase stabilizer in indium oxide. BIO remains amorphous up to 515 °C at a boron content of only 17.5 mol%. A mobility of 10 and 20-40 $cm^2V^{-1}s^{-1}$ is achieved for amorphous and polycrystalline BIO TFTs, respectively.

Third, dual active layers (DALs) are another promising approach to further increase TFT mobility. DAL TFTs of ITO-AITO, BIO-AITO, ITO-IGZO, and ZnO-IGZO are fabricated. ITO-IGZO DAL TFTs are extensively characterized and compared side-by-side with a-IGZO SAL TFTs. The ITO-IGZO DAL TFT exhibits significantly improved performance with mean mobility of 31 $cm^2V^{-1}s^{-1}$, threshold voltage of -3.6 V, sub-threshold swing of 175 mV/dec, minimal hysteresis, and good PBTS stability. However, V_{TH} shift of -8.6 V after 60 min of NBTIS is still significant (compared to a V_{TH} shift of -10.4 V for a-IGZO SAL TFT). The optimum DAL thickness is found to be 3 nm ITO/27 nm a-IGZO.

Fourth, TCAD simulation is used to elucidate the density of states (DOS) of BIO, a-IGZO, and ITO-IGZO TFTs. A mapping technique is introduced to relate experimental transfer characteristics to the sub-bandgap DOS model. Simulation suggests that the ITO-IGZO DAL TFT has a much smaller interface trap density, presumably due to the large free carrier concentration of the ITO, leading to a reduced density of participating interface traps during TFT operation.

7.2 Recommendations For Future Work

AOS density of states. Today, the range of values reported in the literature for AOS band tail states spans several orders of magnitude. Reliable characterization of the AOS sub-bandgap DOS will involve a combination of measurement techniques such

as capacitance-voltage (C-V), photo-excited charge-collection spectroscopy (PECCS), technology computer aided design (TCAD) simulation, and density functional theory (DFT). Note that device-level measurement techniques are generally preferred. However, results must be carefully analyzed in order to avoid parasitic effects. Accurate knowledge of the AOS DOS will aid in solving the V_{TH} instability issue and further increasing oxide TFT performance.

AOS instability mechanisms. Threshold voltage shift of an AOS TFT is arguably the most important issue that could limit continued commercialization of oxide technology. Understanding the fundamental physics of this V_{TH} shift, which is most severe during positive bias temperature stress (PBTS) and negative bias temperature illumination stress (NBTIS), is of great interest. A meaningful study would involve a TFT that is very similar to the industrial manufacturing process, i.e., glass substrate, patterned gate electrode, PECVD gate insulator, and passivation layer in a back-channel etch or etch-stop layer type process. Additionally, for NBTIS a light source is needed with known, and ideally adjustable, spectral irradiance (photon flux and energy spectrum).

Crystalline/amorphous DAL TFT. The idea of a crystalline/amorphous DAL TFT is to merge the best of both worlds, i.e., high-performance of a crystalline semiconductor and large-area manufacturability of an amorphous material. Can a crystalline semiconductor layer be grown with a *controlled morphology* on large glass substrates because it is capped with an amorphous layer? This was attempted (unsuccessfully) for a ZnO-IGZO stack, as described in Section 6.5. More work is needed to thoroughly evaluate this approach. Perhaps, a more suitable material system and/or synthesis strategy can be identified.

APPENDICES

Appendix A: Additional Literature Data

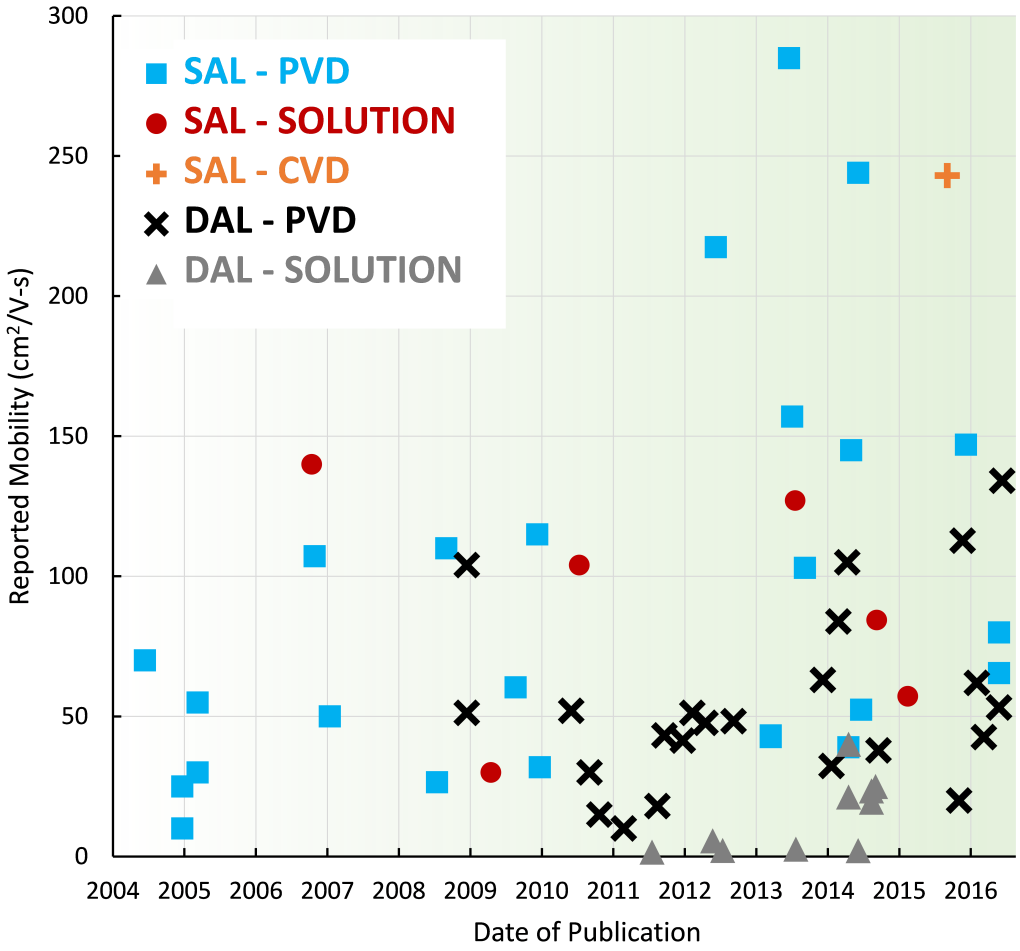

Figure A.1: Mobility of selected reports for single active layer (SAL) physical vapor deposited (PVD) TFTs [square], SAL solution processed TFTs [circle], SAL chemical vapor deposited (CVD) TFT [cross], dual active layer (DAL) PVD TFTs [multiplication sign], and DAL solution processed TFTs [triangle].

Appendix B: Additional Experimental Data

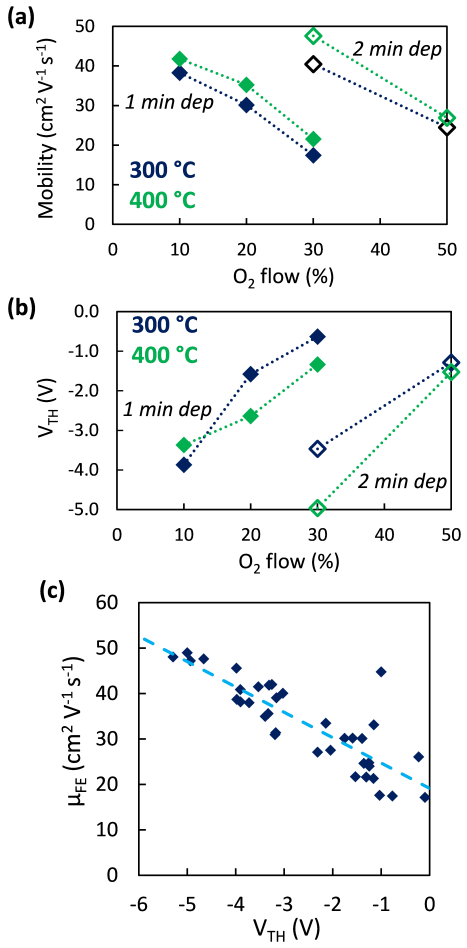

Figure B.1: (a) Field-effect mobility and (b) threshold voltage as a function of oxygen partial pressure during ITO (I-layer) deposition and ITO thickness (one minute deposition corresponds to 3 nm ITO at 10 % O_2 flow). Amorphous IGZO (B-layer) process conditions are fixed at 10 % O_2 flow and 30 nm thickness. (c) Mobility as a function of threshold voltage for 36 ITO-IGZO DAL TFTs.

Appendix C: Boron Indium Oxide TCAD Simulation Code

C.1 17.5BIO 200 °C anneal device (t_{ch} = 50 nm, O_2 = 10 %)

```
# 50 nm BIO TFT
# 200 C anneal device
go atlas simflags="-P 8"
# simulated device was scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=100 outf=tft_BIO.str master.out
x.m l=0   s=1
x.m l=4   s=0.1
x.m l=26  s=0.1
x.m l=30  s=1
y.m l=0    s=0.002
y.m l=0.05 s=0.002
y.m l=0.15 s=0.010
region num=1 material=igzo y.min=0    y.max=0.05
region num=2 material=sio2 y.min=0.05 y.max=0.15
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0  x.max=5
elec num=3 name=drain  y.max=0.0 x.min=25 x.max=30
# p-Si gate
contact num=1 p.poly
# Al source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16
# set BIO band gap and band mobility
material material=igzo eg300=3.2 mun=12 print
models fermi
# BIO bulk DOS
defects nta=4e20 ntd=1.55e20 wta=0.057 wtd=0.110 \
ngd=4e18 egd=3.00 wgd=0.14 \
```

```
nga=5.57e18 ega=2.0 wga=0.14 \
sigtae=1e-15 sigtah=1e-15 sigtde=1e-15 sigtdh=1e-15 \
siggae=1e-15 siggah=1e-15 siggde=1e-15 siggdh=1e-15 \
dfile=BIO_don.dat afile=BIO_acc.dat continuous numa=200 numd=200
# Simulate transfer curve
solve init
solve vdrain=0.1
save outf=tft_BIO_D01V.str
log outf=tft_BIO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-10 name=gate
log off
load inf=tft_BIO_D01V.str master
solve prev
log outf=tft_BIO_pos.log
solve vstep=0.1 vfinal=30 name=gate
save outf=tft_BIO_G30V.str
log off
exit
```

C.2 17.5BIO 400 °C anneal device (t_{ch} = 50 nm, O_2 = 10 %)

```
# 50 nm BIO TFT
# 400 C anneal device
go atlas simflags="-P 8"
# simulated device was scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=100 outf=tft_BIO.str master.out
x.m l=0   s=1
x.m l=4   s=0.1
x.m l=26  s=0.1
x.m l=30  s=1
y.m l=0    s=0.002
y.m l=0.05 s=0.002
y.m l=0.15 s=0.010
region num=1 material=igzo y.min=0    y.max=0.05
region num=2 material=sio2 y.min=0.05 y.max=0.15
```

```
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0  x.max=5
elec num=3 name=drain  y.max=0.0 x.min=25 x.max=30
# p-Si gate
contact num=1 p.poly
# Al source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16
# set BIO band gap and band mobility
material material=igzo eg300=3.2 mun=12 print
models fermi
# BIO bulk DOS
defects nta=1.2e21 ntd=1.55e20 wta=0.020 wtd=0.110 \
ngd=1.6e18 egd=3.00 wgd=0.14 \
nga=1.96e18 ega=2.0 wga=0.14 \
sigtae=1e-15 sigtah=1e-15 sigtde=1e-15 sigtdh=1e-15 \
siggae=1e-15 siggah=1e-15 siggde=1e-15 siggdh=1e-15 \
dfile=tftex10_don.dat afile=tftex10_acc.dat continuous numa=200 numd=200
# Simulate transfer curve
solve init
solve vdrain=0.1
save outf=tft_BIO_D01V.str
log outf=tft_BIO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-10 name=gate
log off
load inf=tft_BIO_D01V.str master
solve prev
log outf=tft_BIO_pos.log
solve vstep=0.1 vfinal=30 name=gate
save outf=tft_BIO_G30V.str
log off
exit
```

Appendix D: Dual Active Layer TCAD Simulation Code

D.1 Simulation of SAL TFT

```
# 30 nm IGZO SAL TFT with interface traps
#
go atlas simflags="-P 8"
# Simulated device is scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=200 outf=tft_IGZO.str master.out
x.m l=0 s=1
x.m l=4 s=0.1
x.m l=26 s=0.1
x.m l=30 s=1
y.m l=0 s=0.002
y.m l=0.03 s=0.0005
y.m l=0.13 s=0.010
# IGZO layer
region num=1 material=igzo y.min=0.000 y.max=0.030
# GI
region num=2 material=sio2 y.min=0.030 y.max=0.130
# Electrodes
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5
elec num=3 name=drain y.max=0.0 x.min=25 x.max=30
# Gate
contact num=1 p.poly
# Source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16
# Set IGZO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=1 eg300=3.20 mun=15 affinity=4.16 permit=10 nc300=5e18 nv300=3e19 print
# Use Fermi statistics
```

```
models fermi
# IGZO bulk DOS
defects nta=1.21e20 ntd=1.55e20 wta=0.030 wtd=0.110 \
ngd=1e16 egd=2.95 wgd=0.1 \
nga=3.2e17 ega=2.0 wga=0.1 \
dfile=IGZO_bulk_don.dat afile=IGZO_bulk_acc.dat continuous numa=200 numd=200
# IGZO interface DOS
intdefects intnumber=1/2 nta=0 ntd=0 wta=0 wtd=0 \
ngd=6.0e11 egd=2.95 wgd=0.1 nga=0 ega=0 wga=0 \
dfile=IGZO_int_don.dat afile=IGZO_int_acc.dat continuous numa=200 numd=200
# Probe Fermi level position
output con.band val.band
probe name=my_fermi_front x=15 y=0.0298 QFN
probe name=my_con_front x=15 y=0.0298 CON.BAND
probe name=my_con_back x=15 y=0.0 CON.BAND
# Simulate transfer curve
solve init
save outf=tftIGZO_init.str
# Ramp drain bias
solve vdrain=0 vstep=0.1 vfinal=0.5 name=drain
save outf=tftIGZO_D05V.str
# Ramp gate bias
log outf=tftIGZO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-5 name=gate
solve vstep=-0.2 vfinal=-10 name=gate
save outf=tftIGZO_negG10V.str
log off
load inf=tftIGZO_D05V.str master
solve prev
log outf=tftIGZO_pos.log
solve vstep=0.1 vfinal=5 name=gate
solve vstep=0.2 vfinal=20 name=gate
save outf=tftIGZO_G20V.str
log off
exit
```

D.2 Simulation of DAL TFT

```
# 3 nm ITO / 27nm IGZO DAL TFT
#
go atlas simflags="-P 8"
# Simulated device is scaled in x-z direction
# by 0.1x relative to real device (for finer mesh)
mesh width=200 outf=tft_IGZO.str master.out
x.m l=0 s=1
x.m l=4 s=0.1
x.m l=26 s=0.1
x.m l=30 s=1
y.m l=0.000 s=0.002
y.m l=0.027 s=0.0005
y.m l=0.030 s=0.0005
y.m l=0.130 s=0.010
# IGZO layer
region num=1 material=igzo y.min=0.000 y.max=0.027
# ITO layer
region num=3 material=igzo y.min=0.027 y.max=0.030
# GI
region num=2 material=sio2 y.min=0.030 y.max=0.130
# Electrodes
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5
elec num=3 name=drain y.max=0.0 x.min=25 x.max=30
# Gate
contact num=1 p.poly
# Source/drain
contact num=2 workf=4.16
contact num=3 workf=4.16
# Set IGZO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=1 eg300=3.20 mun=15 affinity=4.16 permit=10 nc300=5e18 nv300=3e19 print
# Set ITO band gap, mobility, electron affinity, rel. permittivity, and effective CB/VB DOS
material region=3 eg300=3.20 mun=35 affinity=4.16 permit=9 nc300=4.1e18 nv300=3e19 print
# ITO carrier concentration
doping region=3 uniform n.type concentration=3.63e18
```

```
# Use Fermi statistics
models fermi
# IGZO bulk DOS
defects number=1 nta=1.21e20 ntd=1.55e20 wta=0.030 wtd=0.110 \
ngd=1e16 egd=2.95 wgd=0.1 \
nga=3.2e17 ega=2.0 wga=0.1 \
dfile=IGZO_bulk_don.dat afile=IGZO_bulk_acc.dat continuous numa=200 numd=200
# ITO bulk DOS
defects number=3 nta=2.2e20 ntd=1.55e20 wta=0.018 wtd=0.110 \
ngd=0 egd=2.95 wgd=0.1 \
nga=0 ega=2.0 wga=0.1 \
dfile=ITO_bulk_don.dat afile=ITO_bulk_acc.dat continuous numa=200 numd=200
# Probe Fermi level position
output con.band val.band
probe name=my_fermi_front x=15 y=0.0298 QFN
probe name=my_con_front x=15 y=0.0298 CON.BAND
probe name=my_con_back x=15 y=0.0 CON.BAND
# Simulate transfer curve
solve init
save outf=tftIGZO_init.str
# Ramp drain bias
solve vdrain=0 vstep=0.1 vfinal=0.5 name=drain
save outf=tftIGZO_D05V.str
# Ramp gate bias
log outf=tftIGZO_neg.log
solve vgate=0 vstep=-0.1 vfinal=-5 name=gate
solve vstep=-0.2 vfinal=-10 name=gate
save outf=tftIGZO_negG10V.str
log off
load inf=tftIGZO_D05V.str master
solve prev
log outf=tftIGZO_pos.log
solve vstep=0.1 vfinal=5 name=gate
solve vstep=0.2 vfinal=20 name=gate
save outf=tftIGZO_G20V.str
log off
exit
```

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