AN ABSTRACT OF THE DISSERTATION OF

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Title: Scalable Array Transceivers with Wide Frequency Tuning Range for Next Generation Radios

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Arun S. Natarajan

Scalable array transceivers with wide frequency tuning range are attractive for next-generation radios. Key challenges for such radios include generation of LO signals with wide frequency tuning range, scalable synchronization between multiple array unit cells and tolerance to in-band and out-of-band interferers. This thesis presents approaches to address these challenges in commercial CMOS technologies.

The first part focuses on a series resonant mode-switching VCO architecture that achieves both state-of-art area and power efficiency with an octave frequency tuning range from 6.4-14 GHz achieved 186-dB-188-dB Figure-of-Merit (FoM) in 65 nm CMOS technology. The scalability of this approach towards achieving even larger FTR is also demonstrated by a triple-mode 2.2 GHz to 8.7 GHz (119% FTR) CMOS VCO.

In the second part a scalable, single-wire coupled-PLL architecture for RF/mm-wave arrays is presented. The proposed architecture preserves the simplicity of a daisy-chained

LO distribution, compensates for phase offset due to interconnect, and provides phase noise improvement commensurate to the number of coupled PLLs. Measurements on a 28 GHz CMOS prototype demonstrate the feasibility of this scheme.

The third part of this thesis presents filtering techniques for in-band blocker suppression. A spatial/spectral notch filter design for MIMO/digital beam forming arrays is proposed to relax the ADC dynamic range requirement. Orthogonal properties of Walsh functions incorporated into passive N-path approach enables reconfigurable notches at multiple frequencies and angles-of-incidence. A 0.3 GHz-1.4 GHz four-element array prototype implemented in 65 nm CMOS achieves $>$ 15-dB notch filtering at RF input for two blockers while causing $<$ 3-dB NF degradation.

Finally, a code-domain N-path receiver (RX) is proposed based on pseudo-random (PN) code-modulated LO pulses for simultaneous transmission and reception (STAR) applications. A combination of Walsh-Function and PN sequence is proposed to create code-domain matched filter at the RF frontend which reflects unknown in-band blockers and rejects known in-band TX self-interference (SI) by using orthogonal codes at RX input thereby maximizing the SNR of the received signals. The resulting prototype in 65 nm is functional from 0.3 GHz-1.4 GHz with 35 dB gain and concurrently receives two code-modulated signals. Proposed transmitter (TX) SI mitigation approach results in 38.5 dB rejection for -11.8 dBm 1.46 Mb/s QPSK modulated SI at RX input. The RX achieves 23.7 dBm OP1dB for in-band SI, while consuming $\sim$35 mW and occupies 0.31 mm^2.

Scalable Array Transceivers with Wide Frequency Tuning Range for Next Generation Radios

by

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Abhishek Agrawal, Author

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Chapter 1: Introduction

1.1 Introduction

In the last decade, data transfered wirelessly has increased by more than 100 times and is expected to reach 300 exabytes by 2020 [4]. This demand for higher data rate has led to growing interest in 5G technology. With efforts from both industry and academia, the deployment of upcoming 5G technology is expected to begin in 2020 with an estimated annual revenue of more than $250 billion by 2025 [5]. Potential applications of 5G networks (shown in Fig. 1.1) include cloud service, virtual reality, driver-less cars, smart grid real-time traffic control and Internet of things (IoT). Recently, the radio communication sector of International Telecommunication Union (ITU) has set the specification for 5G networks to meet the performance required by above applications as shown in Fig. 1.2.

The front-runner technologies to meet 5G requirements are massive multiple input and multiple output (massive MIMO) arrays operating at RF and millimeter-wave frequencies respectively. Massive MIMO includes hundreds of physically small, non-directive and scalable antenna arrays at the base station to transmit data simultaneously to multiple users, with user transceivers consisting of single antenna system [6]. This approach is optimized to minimize interference from other users while sending desired data to intended user. The array size can be scaled up to provide increased throughput, improved

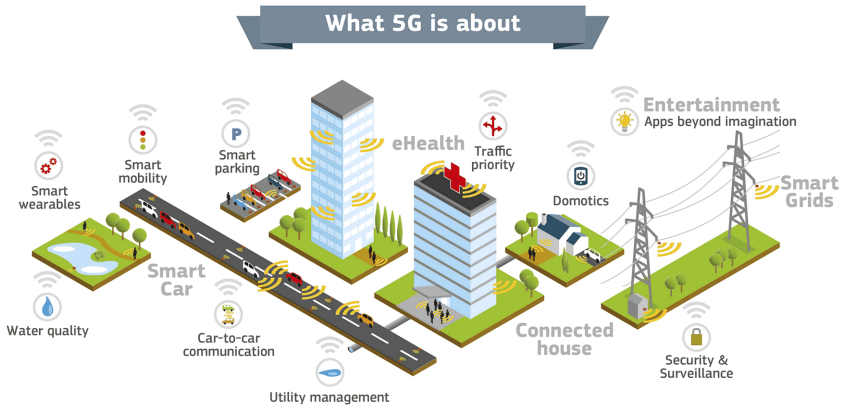


Figure 1.1: European commissions vision of 5G from [1].

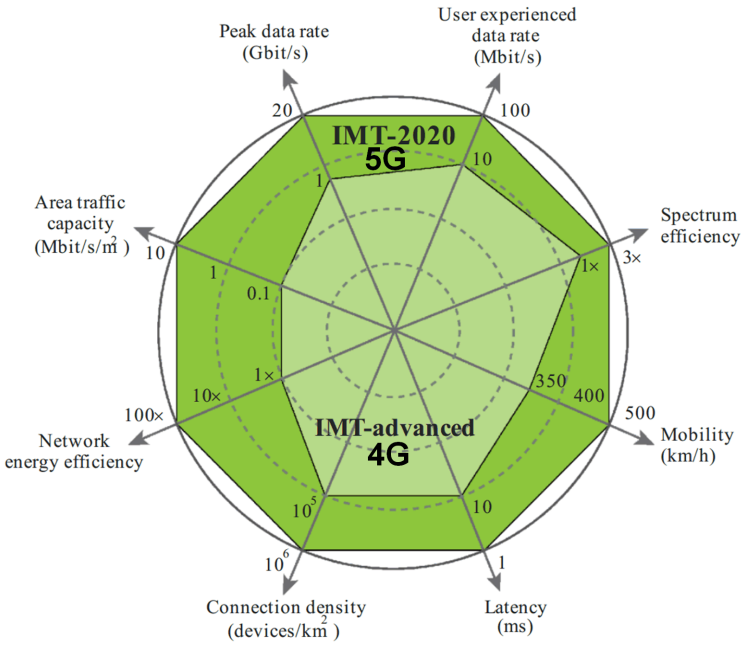


Figure 1.2: 5G system requirements from [2].

power efficiency and simplified signal processing requirement at baseband. Thus, massive MIMO enables increased number of user with enhanced spectrum efficiency [6].

mm-Wave technology operates at 30-300 GHz frequency range with 1-10 mm wavelengths providing higher channel bandwidth and utilizing large amount of unused spectrum. Key reasons for under utilization of mm-wave frequencies are (a) path loss caused by smaller antenna aperture size and (b) high cost of transmitters and receivers. With the advancement in CMOS and SiGe integration technology, the cost of large-scale arrays at mm-wave frequency has been reduced and tens to hundreds of elements can be integrated [7, 8, 9, 10, 11, 12, 13, 14] to overcome path loss by realizing larger aperture size using antenna arrays.

Recently, several prototypes consisting of hundreds of elements has been demonstrated for both RF and mm-wave large scale arrays [15, 16]. For commercial viability the arrays are typically implemented using a tile-based approach, wherein a unit cell is replicated to achieve a large-scale array. Some of the key challenges in such a scalable array includes frequency generation using minimum number of VCOs, distributing coherent reference clocks across hundreds of antennas and ensuring blocker tolerance to reduce ADC dynamic range requirement. This dissertation explores scalable solutions that can be incorporated in the design of large-scale arrays.

1.2 Organization

Frequency generation to cover from several hundreds to $<$6 GHz$-$often called "beachfront spectrum"$-$ using single VCO is challenging for RF massive MIMO system.

An area and power efficient octave frequency tuning range (FTR) LC VCO operating at 14 GHz is presented in Chapter 2. A quantitative description of the trade-offs between tuning range and phase noise of conventional inductor and capacitor switching is derived in Section 2.2 to understand the limitation of wide-FTR VCO. A series resonator mode-switching VCO design [17, 18] is elaborated in Section 2.3 ensuring high quality factor, Q, across the entire FTR. The proposed technique is extended to a triple-mode VCO achieving 2.2 GHz to 8.7 GHz FTR in Section 2.4. Measurement results are presented in Section 2.5, concluded with discussion on Figures-of-Merit to compare the performance across FTR and area of conventional VCO.

The strength of MIMO receivers lies in coherent processing of signal through multiple channels. The key challenges in such system is co-phasing antenna array to steer the signal beam in any direction and to attenuate the interferer by null formation, both requiring coherent clock distribution scheme. Chapter 3 explores a coherent clock distribution scheme for scalable arrays. Section 3.2 evaluates the performance of array in the presence of incoherent clock distribution for beamforming and massive MIMO application. Section 3.3 discusses the shortcomings of conventional clock distribution approaches and presents a scalable single wire bidirectional type-II coupled-PLL architecture to generate coherent clock. Noise and stability of four coupled-PLL placed on different tiles is analyzed in Section 3.4. The implementation of 28 GHz coherent clock generation is presented in Section 3.5 and concluded with its measurement results are presented in Section 3.6.

The next three chapters are dedicated to blocker-tolerant scalable receiver array design to attenuate both in-band and out-of-band blockers using passive mixer approach

reducing the required ADC dynamic range. Walsh function sequence (WF-seq) based passive notch mixer implementation is proposed in Chapter 4. The theoretical analysis of WF-seq based passive mixer using a signal space approach is presented in Section 4.2. Its equivalence to the N-path passive mixer is also elaborated. Section 4.3 describes the design and implementation of the proposed filter with its measurement results discussed in Section 4.4. Further, the above approach is extended to concurrent bandpass filters in Section 4.5 to investigate concurrent dual frequency signal reception.

Chapter 5 extends the WF-seq based notch filter to suppress in-band spatial blockers in a MIMO system. Section 5.2 describes the implementation of concurrent dual-frequency /angle-of-incidence (AoI) spatio-spectral notch filter. Measurement results are presented in Section 5.3 achieving $>$20 dB spatio-spectral attenuation of interferer at RF input for one frequency/AoI notch and $\sim$15 dB rejection at two independent frequencies/AoI.

While Chapter 4 and Chapter 5 study the passive notch filter concept, a more complex full duplex transceiver is implemented using code domain modulation in the presence of self-interference from its own transmitter. Chapter 6 extends the WF-seq based notch filter to design the code domain receiver that implements matched filter at RF for spread spectrum system. Section 6.2 provides the background and system level requirements for code modulated receiver in the presence of in-band jammer. Section 6.3 extends the N-path mixer architecture to code domain. In Section 6.3.4 schematic implementation is presented followed by measurements in Section 6.4.

Chapter 2: Series Resonator Mode-Switching for Area-Efficient Octave Tuning-Range LC Oscillators

2.1 Introduction

The emergence of cellular, wireless LAN, GPS and low-power wireless applications has led to the pursuit of the software-defined radio (SDR) in CMOS. Such a SDR would support a wide range of transmit-receive frequencies and standards, enabling lower bill-of-materials and higher integration[19, 20, 21, 22]. A wide tuning-range oscillator is required to provide all the local-oscillator (LO) frequencies for signal upconversion and downconversion in SDR transceivers as well as for providing a clock for other on-chip circuits. Octave frequency tuning range (FTR) in an oscillator implies that all frequencies up to the highest oscillation frequency can be synthesized in the PLL if multiplexers are used [23, 24, 25, 26, 27]. Additionally, many transceiver architectures require quadrature LO signals even at RF [28], which can be generated effectively with commonly-used frequency dividers as shown in Fig. 2.1. Therefore, VCO operating at twice the highest frequency of interest are very useful. Since most standards of interest occupy "beach-front" spectrum up to 6 GHz an octave-FTR oscillator with > 12-GHz oscillation frequency is relevant for multi-standard quadrature transceivers up to 6 GHz.

Octave FTR can be achieved by dividing the tuning range among two or more VCOs with overlapping frequency bands followed by multiplexers as shown in Fig. 2.2(a)

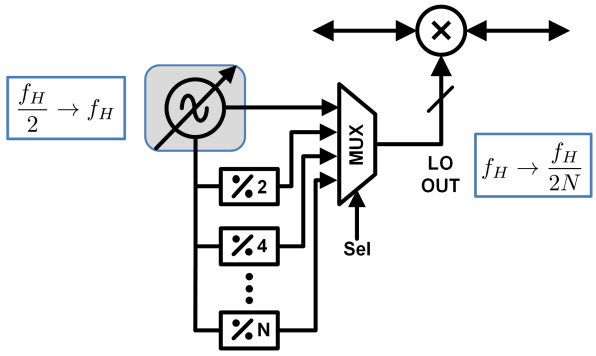
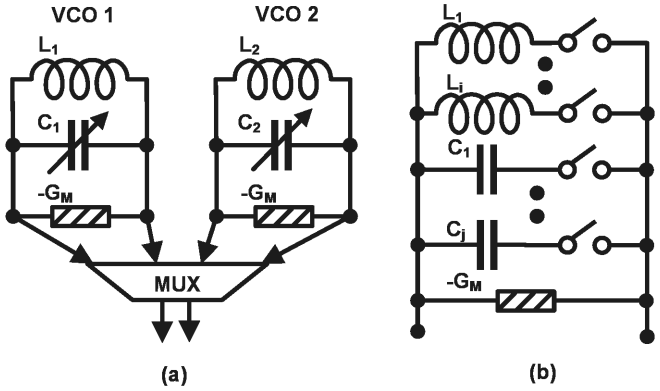


Figure 2.1: Motivation for octave FTR VCOs - all frequencies below highest oscillation frequency can be generated by a combination of multiplexers and frequency dividers



	Two VCOs	One VCO
Power Consumption	Higher FoM	Lower FoM
Tuning Range	Lower FTR →better PN	Higher FTR → poor PN
Area	Lower FoMA (2 Inductors)	Improved FoMA

Figure 2.2: Required wide tuning-range can be achieved by (a) dividing tuning range among multiple oscillators, each of which are power efficient (b) or by providing wide tuning range in the resonator of a single oscillator by varying one or both of the resonator inductor and capacitor.

[29, 21], or by designing a single VCO to cover the entire FTR as shown in Fig. 2.2(b). At the system-level, the two approaches must be compared on the basis of power and area efficiency. Dividing the wide FTR among multiple narrow tuning-range VCOs allows each of the VCOs to achieve better phase noise for the same power consumption, i.e., a higher VCO Figure-of-Merit (FoM)[30]. Therefore, the two/multi-VCO approach can be power efficient. However, this requires an inductor in each resonator leading to larger area as compared to a single VCO. Given the inherent trade-offs between FTR and power efficiency derived in Section 2.2, single VCO must be area efficient to be preferred to a multi-VCO solution as summarized in Fig. 2.2.

In [17, 18], an area-efficient octave-FTR VCO from 6.4 GHz to 14 GHz was demonstrated using a series resonator mode-switching approach. In this Chapter, a quantitative description of the trade-offs between tuning range and phase noise is derived in Section 2.2 to understand wide-FTR VCO limits across resonator topologies. Given the limitations of conventional inductor and capacitor switching derived in Section 2.2, a series resonator mode-switching VCO introduced in [17, 18] is described in further detail in Section 2.3, emphasizing the design of a mode-switching resonator that ensures high quality factor, Q, across the entire FTR. The proposed approach is also contrasted with other resonator mode-switching techniques. An extension of the proposed technique to a triple-mode VCO achieving 2.2 GHz to 8.7 GHz FTR is detailed in Section 2.4. Measurement results are detailed in Section 2.5, along with a discussion on conventional VCO Figures-of-Merit that compare performance across FTR and area.

2.2 Impact of wide frequency tuning range on resonator Q

Resonators with switched capacitor banks are widely used for VCO frequency tuning[31, 32, 33, 23]. Techniques to improve capacitor-variation ratios in such switched banks without degrading Q have been studied[27, 34]. Alternate topologies with switches in series with inductors or across transformers have been proposed for wide-FTR VCOs[35, 36, 37, 38, 39, 40]. The above approaches generally achieve wide FTR by relying upon transistor switches and are limited by switch losses. While technology scaling improves CMOS switch performance, even state-of-the-art CMOS switches significantly degrade resonator Q and phase noise at frequencies $>$ 10 GHz[25]. Competing capacitor or inductor switching approaches can provide phase-noise advantages under different operating frequency and fixed parasitics scenarios[40]. While there have been some efforts to understand trade-offs across tuning range and power consumption[41], there has been no systematic approach to quantify relative merits. In the following, we introduce a generalized two-port network approach that can be used as a framework for understanding performance limits. We derive Q and FTR trade-offs assuming narrow FTR and wide FTR highlighting the relative performance of different topologies. The impact of Q and FTR on VCO figures-of-merit is discussed in Section 2.5.3.

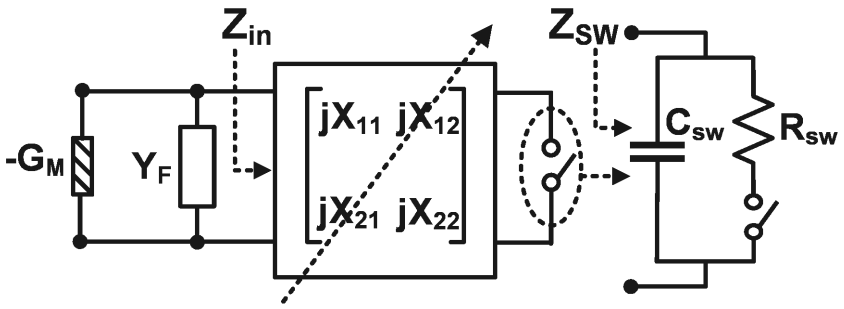


Figure 2.3: A generalized two-port Z-parameter network quantifies resonator trade-off between Q and FTR.

2.2.1 Generalized Two-Port Network Models for FTR and Phase Noise Analysis

The lossy resonator with switched capacitor/inductor banks in Fig. 2.2(b) uses switches to change effective resonance frequency. For each switch in Fig. 2.2(b), the resonator can be modeled using the approach in Fig. 2.3. Here, the resonator is modeled as a fixed admittance Y_F, with a quality factor, Q_F, and a loss-less two-port network terminated by the switch impedance, Z_{SW}, which is equal to resistance, R_{SW}, in the ON state and $\frac{1}{jC_{SW}}$ in the OFF state, where R_{SW} and C_{SW} are the switch resistance and capacitance respectively. The input impedance, Z_{in}, at port 1 resonates Y_F at the oscillation frequency, ω_0, and is given by,

$$Z_{in} = jX_{11} - \frac{jX_{21}jX_{12}}{jX_{22} + Z_{SW}} \tag{2.1}$$

Based on the definition in [42], resonator quality factor, Q_T, at ω_0 for resonator

impedance, $Z_t = 1/Y_F \parallel Z_{in}$, is given by,

$$Q_T = \frac{\omega_0}{2} \left| \frac{\frac{dZ_t}{d\omega}}{Z_t} \right| \tag{2.2}$$

In order to simplify the following analysis, we assume that Z_{in} and Y_F are primarily capacitive or inductive,

$$\omega_0 \cdot |imag\left(Z'_{in}\left(\omega_0\right)\right)| \approx |imag\left(Z_{in}\left(\omega_0\right)\right)|$$
$$\omega_0 \cdot |imag\left(Y'_{F}\left(\omega_0\right)\right)| \approx |imag\left(Y_{F}\left(\omega_0\right)\right)|$$

This assumption is valid in the case of typical oscillators where an inductor (representing Y_F) is resonated with a switched capacitor bank, or a capacitor is resonated with switched inductors. In this case, individual components are operating at frequencies lower than their self-resonance frequency, and are primarily inductive or capacitive [43]. Under this assumption, when the switch in Port 2 is in the on-state, Q_T is approximately,

$$Q_T \approx Q_F \parallel Q_{SW,ON} \tag{2.3}$$

where,

$$Q_{SW,ON} = \left| \frac{im\left(Z_{IN,ON}\right)}{re\left(Z_{IN,ON}\right)} \right| \tag{2.4}$$

For narrow frequency tuning, we can assume that changing the state of the switch in Port 2 (Fig. 2.3) results in small fractional change, $\Delta\omega$, at ω_0. In this case, the fractional

$FTR = \frac{\Delta\omega}{\omega_0}$, can be shown to be,

$$FTR = \frac{\Delta\omega}{\omega_0} \approx \frac{1}{2}\frac{im\left(\Delta Z_{in}\right)}{im\left(Z_{in,ON}\right)} \tag{2.5}$$

Further assuming that i) $|X_{22}| > R_{SW}$, and ii) $jX_{ij,ON} \approx jX_{ij,OFF}$, since $\Delta\omega$ is small, the two-port network Z_{in} in the on and off states are given by,

$$Z_{in,ON} = \frac{R_{SW}X_{12}X_{21}}{X_{22}^2} + jX_{11} - \frac{jX_{21}jX_{12}}{jX_{22}} \tag{2.6}$$

$$Z_{in,OFF} = jX_{11} - \frac{jX_{21}jX_{12}}{jX_{22} + 1/j\omega C_{SW}} \tag{2.7}$$

Hence, it can be shown based on (2.4) - (2.7), that

$$Q_{SW,ON}\left|\frac{\Delta\omega}{\omega_0}\right| = \left|\frac{1}{2\omega_0 R_{SW}C_{SW}\{1 - \frac{1}{\omega_0 C_{SW}(X_{22})}\}}\right| \tag{2.8}$$

The term $\frac{1}{\omega_0 C_{SW}X_{22}}$ is the network parameter which makes the $Q_{SW,ON}\cdot FTR$ product topology dependent. Notably, the trade-off between $Q_{SW,ON}$ and FTR is present in any topology and impacts VCO phase noise, power consumption and FTR, as will be shown in the following. The well-known VCO phase-noise FoM is given by [44, 45, 46],

$$\begin{aligned} FoM &= -PN + 10\log\left\{\left(\frac{f_0}{\Delta f}\right)^2\left(\frac{1mW}{P_{dc}}\right)\right\} \\ &= 10\log\left(\frac{2Q_T^2 P_{TANK}}{kTFP_{dc}}\right) - 30 \end{aligned} \tag{2.9}$$

where P_{dc} is the oscillator dc power consumption, P_{TANK} is the power dissipated

in the tank, and F is an oscillator-topology dependent constant. As shown in (2.9), for a given topology and class of operation, VCO FoM is determined by Q_T. However, (2.8) shows the fundamental trade-off between $Q_{SW,ON}$ (and hence, Q_T) and FTR. Therefore, simultaneously achieving high FoM and FTR is challenging, particularly at high frequencies since the $Q_{SW,ON} \cdot FTR$ product is inversely proportional to oscillation frequency.

It can also be seen from (2.8), that $Q_{SW,ON} \cdot FTR$ product is inversely proportional to the switch $R_{SW}C_{SW}$ constant which is technology dependent. Device scaling which reduces $R_{SW}C_{SW}$ improves this trade-off and will make it easier to achieve high FTR and VCO FoM in more advanced technology nodes. A similar derivation is presented in Appendix A with two-port Y-parameter models, which can be convenient for analyzing certain resonator topologies as shown in the following sections.

2.2.2 Resonator with Switched Capacitor Banks

The generalized two-port approach in Section 2.2.1 can be used to compare different topologies. A typical switched capacitor bank to vary resonance frequency is shown in Fig. 2.4(a). For this topology, the generalized two-port Y-parameter network in (A.2) provides simplified analysis. Therefore, in the case of narrow tuning range, $Q_{SW,ON}$ is related to fractional frequency change $\frac{\Delta\omega}{\omega_0}$ by,

$$Q_{SW,ON}\left|\frac{\Delta\omega}{\omega_0}\right| = \left|\frac{1}{2\omega_0 R_{SW}C_{SW}\{1+\frac{C}{C_{SW}}\}}\right| \tag{2.10}$$

This result is similar to that derived in [31] through an analysis of the actual capacitor

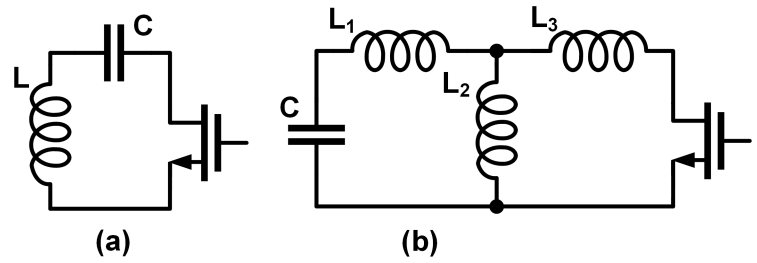


Figure 2.4: Resonator with (a) switched capacitor bank used in analysis in Section 2.2.2, (b) switched inductor/transformer used in analysis in Section 2.2.3

network without a generalized approach. The wide FTR case can be evaluated by considering a switched capacitor bank as shown in Fig. 2.4(a). The capacitance in ON and OFF state are C and $\frac{CC_{SW}}{C+C_{SW}}$ respectively, leading to a difference in capacitance between ON and OFF state, $\Delta C = \frac{C^2}{C+C_{SW}}$. Since the capacitance Q in ON state is given by,

$$Q_{SW,ON} = \frac{1}{\omega_{ON} R_{SW} C} \tag{2.11}$$

this implies,

$$Q_{SW,ON} \left| \frac{\Delta C}{C} \right| = \left| \frac{1}{\omega_{ON} R_{SW} C_{SW} \{1 + \frac{C}{C_{SW}}\}} \right| \tag{2.12}$$

Again, achieving a large FTR requires a large ΔC which degrades Q. This is compared to the inductor switching in the following section.

2.2.3 Resonator with Switched Inductor/Transformer Banks

Switched tank inductance as opposed to capacitance in the resonator has been proposed to overcome $Q \cdot FTR$ limitations [47, 48, 49]. Switched inductors [50, 38, 47]

and switched transformer approaches [36, 39, 49] can be analyzed jointly with the circuit in Fig. 2.4(b). The narrow FTR tuning approximation in Section 2.2.1 leads to Q and FTR for this topology being related by,

$$Q_{SW,ON}\left|\frac{\Delta\omega}{\omega_0}\right| = \left|\frac{1}{2\omega_0 R_{SW}C_{SW}\left(1-\frac{\omega_Z^2}{\omega_0^2}\right)}\right| \tag{2.13}$$

where, $\omega_Z = 1/\sqrt{(L_2+L_3)\,C_{SW}}$. The circuit in Fig. 2.4(b) and the analysis in (2.13) reduces to a pure inductor switching case when $L_3 = 0$ and can include switched transformers when $L_3 \neq 0$. The ω_z term in the (2.13) can improve the Q for a given FTR by lowering the effective $R_{SW}C_{SW}$ product in (2.13). In the wide FTR case without the narrow-band assumptions (detailed derivation in Appendix B),

$$Q_{SW,ON}\left|\frac{\Delta L}{L_{OFF}}\right| = \frac{\omega_{OFF}}{\omega_{ON}}\left|\frac{1}{\omega_{OFF}R_{SW}C_{SW}\left(1-\frac{\omega_Z^2}{\omega_{OFF}^2}\right)}\right| \tag{2.14}$$

Therefore, appropriate choice of ω_Z can provide benefit as illustrated in Fig. 2.5, which considers two cases (a) 6.4 GHz to 14 GHz tuning range and (b) 9 GHz to 14 GHz tuning range in a technology with $R_{SW}C_{SW} = 1\ ps$ and assuming $L_3 = 0$. Note that in the inductive switching case, ($\omega_{OFF} = \omega_{LO}; \omega_{ON} = \omega_{HI}$) where ω_{HI} and ω_{LO} represent the high and low frequency limits respectively. In the capacitive switching case, this is reversed - higher oscillation frequency occurs when switch is OFF. As expected from (2.8), smaller FTR implies that the Q achieved by 9-GHz to 14-GHz resonator is higher than that achieved by the 6.4-GHz to 14-GHz resonator for both capacitive and inductive switching schemes. Also, inductive switching can be better or worse than

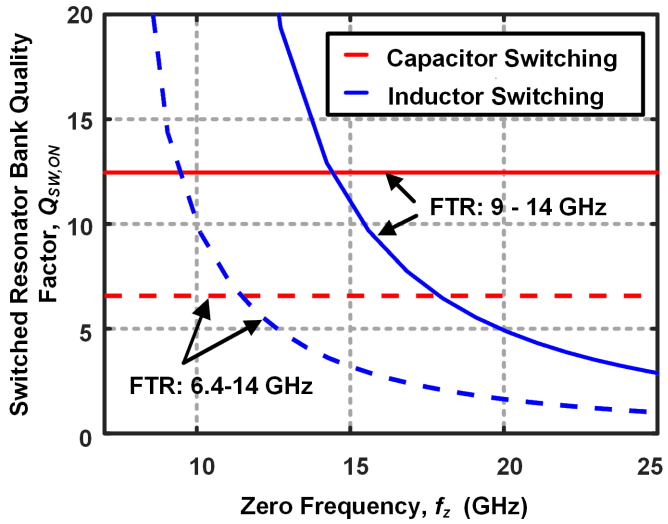


Figure 2.5: Quantitative comparison of inductor/capacitor bank switching approaches in Fig. 2.4 demonstrates relative merits of such approaches for targeted FTR for 6.4 GHz to 14 GHz and 9 GHz to 14 GHz. Wider FTR leads to lower Q - inductor switching can help but even f_z =10 GHz limits Q to 10.

capacitive switching depending upon ω_Z. While lower ω_Z leads to better resonator Q for inductor-switching schemes, it should be also noted that it leads to a higher secondary peak (from the fourth-order resonator) which may lead to oscillation at undesirable frequencies. From Fig 2.5, the Q for 6.4-GHz to 14-GHz FTR is < 10 even for inductor switching with f_z = 10 GHz. In the following section, we discuss architectures that break the $Q \cdot FTR$ trade-off in resonator bank switching approaches by employing lossless resonator mode-switching.

2.3 Series Resonator Mode-Switching VCO

Lossless resonator mode-switching approaches that overcome the Q and FTR tradeoffs have been proposed [51, 52]. Impedances across modes are equalized in a transformer-based mode-switching VCO in [25]. This approach leads to relatively uniform impedance across the resonator modes and therefore achieves good phase noise and FoM across the entire octave FTR up to 5.6 GHz. It also ensures low area overhead by placing one transformer coil inside another - however, this negatively impacts overall Q due to the presence of the inner coil, inter-metal crossings and mutual coupling. The inner transformer approach and loading of G_m cells limit performance for higher frequency of operation. An extension of such an approach to three resonant modes is proposed in [53] in order to achieve octave FTR at higher oscillation frequency ($\sim$13 GHz). This requires controlled coupling between three inductors, with two of the inductors placed inside an outer inductor. This layout approach also leads to lower Q due to internal metal crossings.

Parallel resonator mode-switching approaches that avoid inductor Q degradation are proposed in [26],[54]. While octave FTR up to 8.45 GHz is demonstrated in [26], this approach utilizes four inductors, each with an inductance of L_T (570 pH) with the parallel mode-switching resulting in L_T/4 and L_T/2 inductances. Since inductor Q is proportional to $\sqrt{Area}$ [55], for the same Q, parallel mode-switching approach uses a much larger area. Hence, the use of multiple parallel inductors to achieve smaller inductance reduces the area benefits of using a single wide-FTR LC VCO.

2.3.1 Series Resonator Mode-Switching Approach

The proposed series resonator mode-switching scheme, shown in Fig. 2.6, maintains high impedance across the entire FTR as well as area efficiency. The resonator has two inductors of inductance, L, each connected in series and has two modes of operation, referred to as high-band (HB) and low-band (LB) modes in the following. The modes are enforced by activating or deactivating the corresponding G_M cells in Fig. 2.6.

In the high-band mode, the G_M-cells create a mode of operation with the voltage polarity at different points on the resonator as shown in Fig. 2.6(a). This mode can be considered as two tightly-coupled oscillators with optimal FoM in parallel. The equivalent model for the resonator consists of an inductance, $L = L_{HB}$, in parallel with capacitance, C_D with the corresponding resonance frequency,

$$\omega_{HB} = \frac{1}{\sqrt{L_{HB}C_D}} \tag{2.15}$$

Since the doubling of power compared to a single VCO is accompanied by a corresponding reduction in phase noise in a tightly-coupled oscillator, the VCO phase-noise FoM stays the same. Fig. 2.6(b) shows the resonator in low-band mode with the voltage polarity forced by $G_{M,LB}$. Therefore, this can be viewed as a single oscillator with a resonator consisting of $L_{LB} = 2L\,(1 + k)$ in parallel with a capacitance, $C_D/2 + C_{LB}$, where k represents the coupling between sections, S_1 and S_2. The resonance frequency in LB mode is given by,

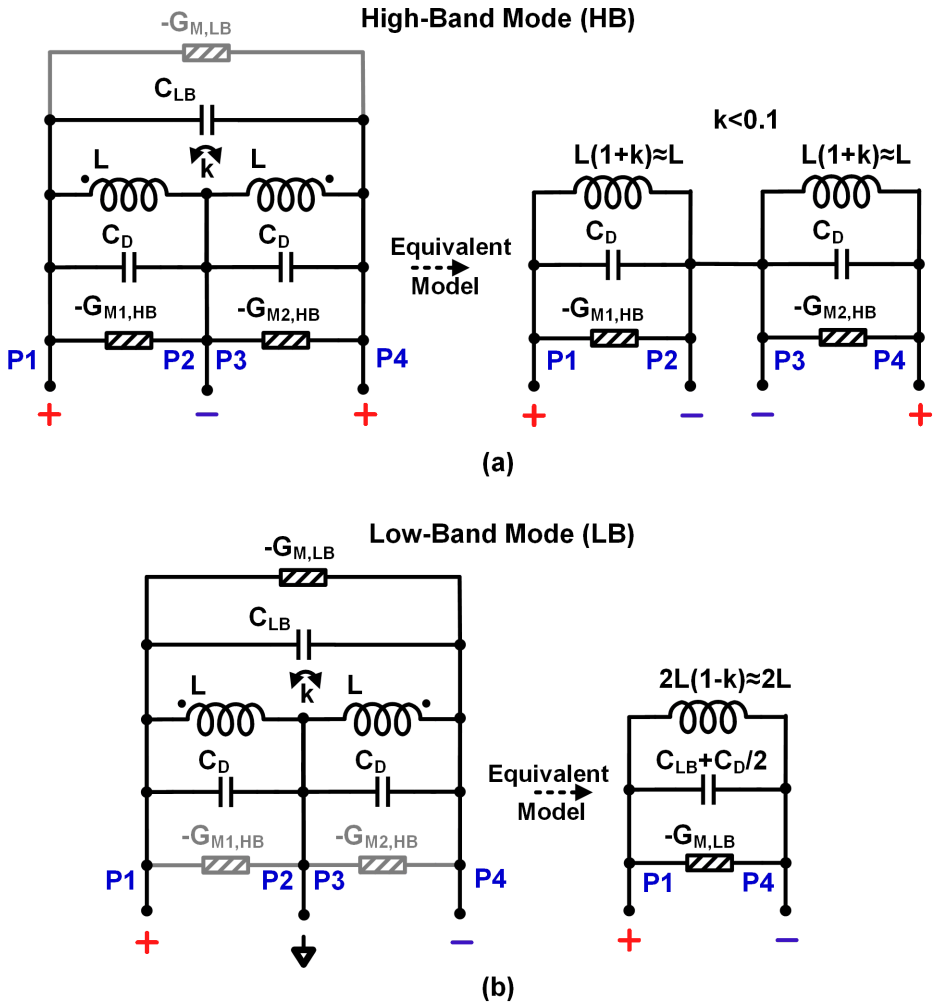


Figure 2.6: Voltage polarities across the resonator in proposed series resonator mode-switching approach: (a) High-band (HB) mode, (b) Low-band (LB) mode.

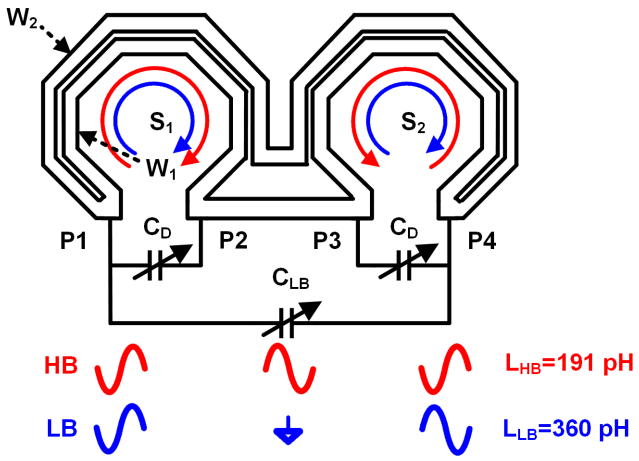


Figure 2.7: Resonator structure and current flow direction in HB and LB modes for implementation of proposed approach.

$$\omega_{LB} = \frac{1}{\sqrt{L_{LB}\left(\frac{C_D}{2} + C_{LB}\right)}} \tag{2.16}$$

From (7) and (8), it is evident that $\omega_{LB} < \omega_{HB}$. Effective inductance values for the resonator structure in the two modes for the 6.4-GHz to 14-GHz operation in this work are shown in Fig. 2.7. Thus, tank inductance goes from L_{HB} =191 pH in HB mode to $L_{LB} \approx 2L_{HB}$ =360 pH in LB mode. The mutual coupling between S_1 and S_2 is negligible ($k < 0.1$) which is confirmed by the near-doubling in inductance between modes.

It must be noted that the two inductors are in series in the LB mode. The small coupling between the inductors implies that they achieve the Q that would be achieved by an inductor with inductance, L_{LB}, occupying the same area. Therefore,area wastage is minimized in LB mode. Frequency tuning within LB and HB modes is achieved by varying C_D and C_{LB}. Notably, when going from HB to LB modes, both inductance and

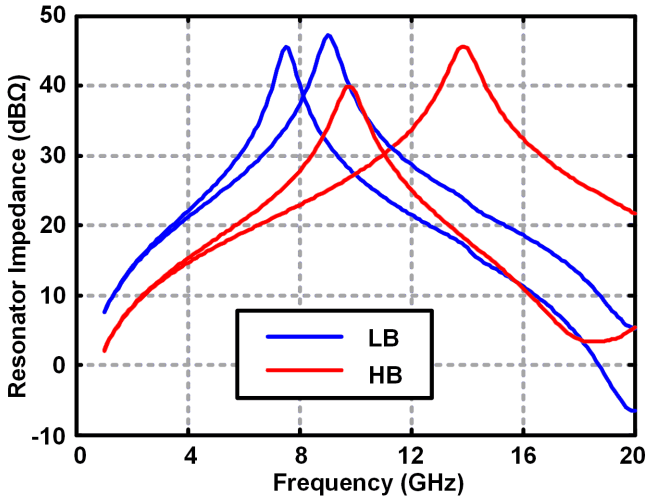


Figure 2.8: Simulated resonator impedance in HB and LB modes demonstrates the effectiveness of series resonator mode switching in maintaining high impedance across entire FTR.

the capacitance increase implying constant impedance. The ∼2x increase in inductance in LB mode leads to high resonator impedance even at the low end of the FTR as shown in Fig. 2.8, ensuring low power consumption across FTR. Performance is limited by the Q of the capacitor bank utilized for tuning within each mode.

In the HB mode, the two tightly-coupled oscillators reduce phase noise by 3 dB. In the LB mode, an inductance of $2L$ is achieved without degradation in inductor Q or VCO FoM. This implies effective area utilization in both modes. The proposed approach can also be viewed as a merging of two oscillators that achieve optimal FoM in a given area with one oscillator operating in HB mode and the other operating in LB mode.

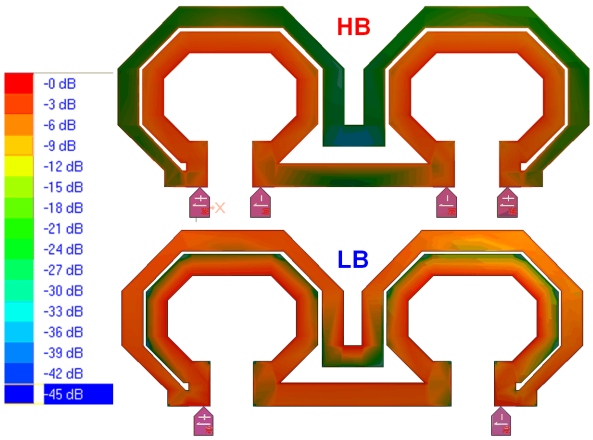


Figure 2.9: Current distribution in inductor structure from EM simulations[3] - W_2 carries less current than W_1 in HB Mode, while the effective width is W_1 + W_2 in LB mode.

2.3.2 Design of Resonator with High Q across Octave FTR

While the approach proposed in Section 2.3.1 ensures effective area utilization, avoids Q degradation due to mode switching, and provides high impedance across FTR, the trade-offs between substrate and resistive losses lead to a peak-Q frequency for the inductor. This intrinsic variation in inductor Q across frequency represents a key design challenge for wide-FTR VCOs. Wider metal width is preferred for inductors at low frequencies while narrower widths are desirable at high frequencies to reduce substrate losses. In this work, a two-wire approach, shown in Fig. 2.7, is adopted to overcome this trade-off by leveraging voltage polarities to change effective inductor width across resonator modes. Each of the two inductor sections S_1 and S_2 consists of two wires, W_1 and W_2 as shown in Fig. 2.7. In this implementation, $W_1 = W_2 = 20$ μm with spacing of 2 μm between the two wires. In the LB mode, $G_{M,LB}$ enforces the voltage polarities corresponding to current flow in the inductor as indicated in Fig. 2.7 in black. Similarly,

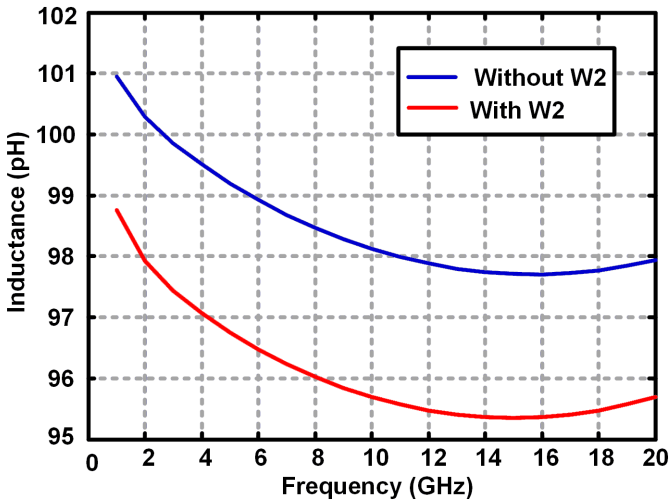


Figure 2.10: Inductance in HB mode simulated in the presence and absence of wire, W_2, to demonstrate minimal influence in HB mode.

in the HB mode, the $G_{M,HB}$ cells enforce the polarities shown in red. EM simulations, shown in Fig. 2.9, confirm that in HB mode, identical voltages at $P1$ and $P4$ result in small current through W_2. Therefore, the effective inductor width in HB mode is W_1. However in LB mode, the two wires W_1 and W_2 operate in parallel with an effective width of $W_1 + W_2$. In addition to the current distribution outlined in Fig. 2.9, the change in effective width can be understood by simulating the inductor structure in Fig. 2.7 in HB mode in the presence and absence of wire, W_2. The minimal change in inductance shown in Fig. 2.10 demonstrates that wire, W_2, has minimal impact in HB mode. The change in effective inductor width from $W_1 + W_2 = 40$ μm in LB mode to $W_1 = 20$ μm in HB mode causes a desirable shift in the peak inductor Q frequency across the two modes, as shown in Fig. 2.11. Hence, the proposed switching scheme can ensure high Q across the entire FTR, addressing the problem of inductor Q variation in wide-FTR

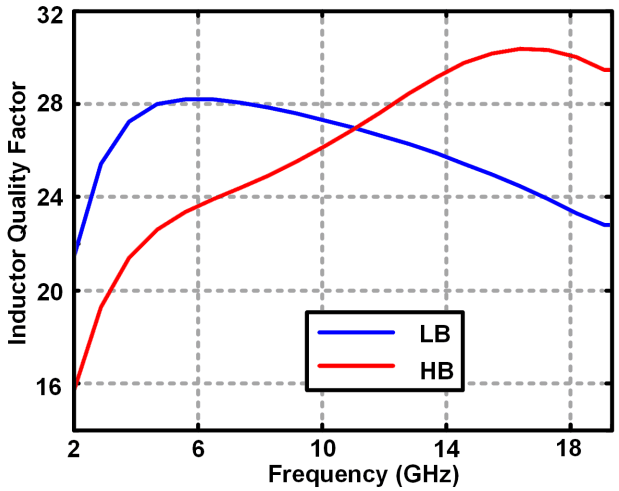


Figure 2.11: Simulated inductor Q in LB and HB modes demonstrating shift in peak-Q frequency.

VCOs.

2.3.3 6.4-GHz to 14-GHz VCO in 65-nm CMOS

Fig. 2.12 shows the schematic of the proposed dual-mode series resonator mode-switching CMOS VCO that achieves 6.39 GHz to 14 GHz FTR (74%). The cross-coupled G_M cells ($G_{M,LB}$, $G_{M1,HB}$ & $G_{M2,HB}$) are designed with enable switches at the source of the cross-coupled pair. The G_M cell can be activated by enabling these switches, thereby enabling a particular oscillation mode. In the ON state, the switches degenerate the cross-coupled pair - however, a small on-resistance minimizes noise impact, particularly since these switches are at the source of the cross-coupled pair. When the G_M cells are de-activated by disabling the switches, the high source impedance ensures that the disabled cross-coupled pair does not degrade the tank quality factor even in the presence

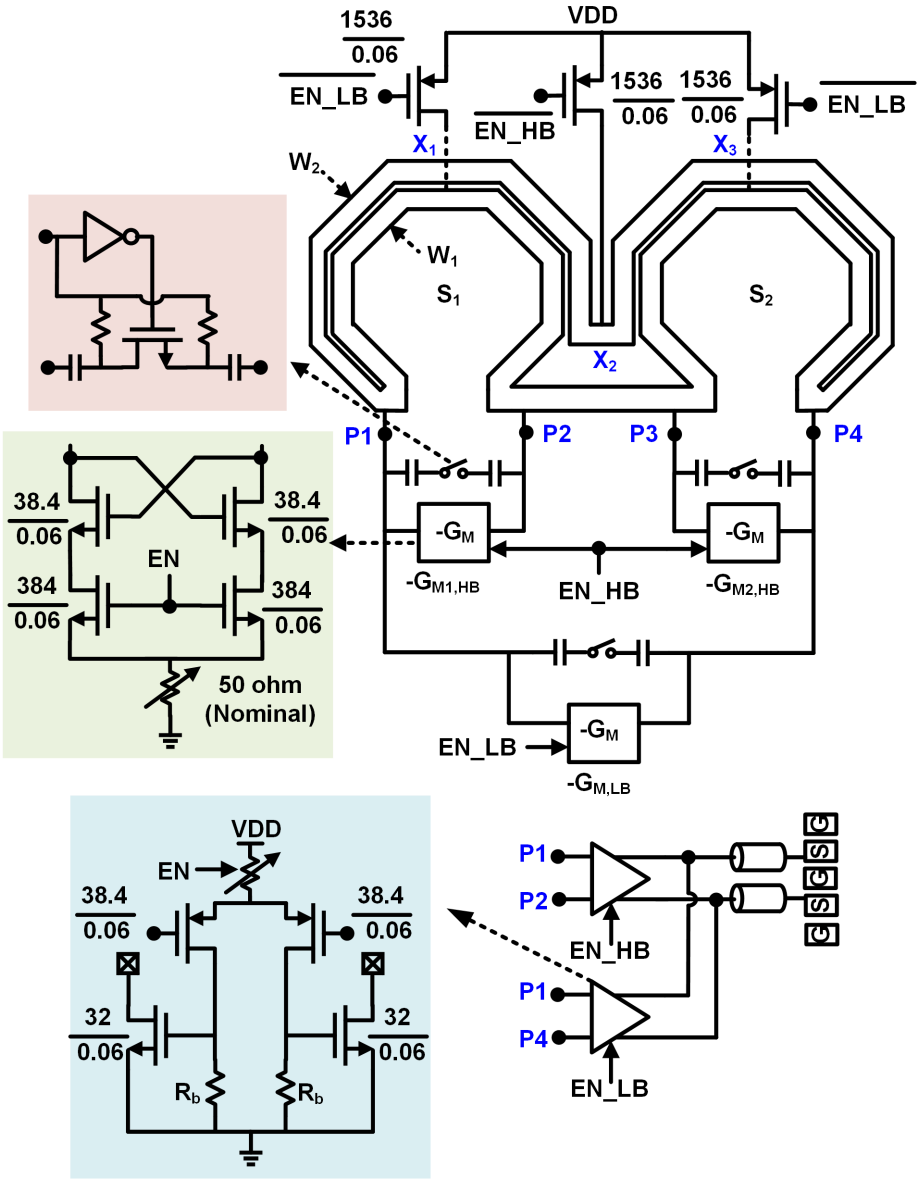


Figure 2.12: Schematic and core layout of proposed series resonator mode-switching CMOS VCO with octave tuning range (6.39 GHz to 14 GHz).

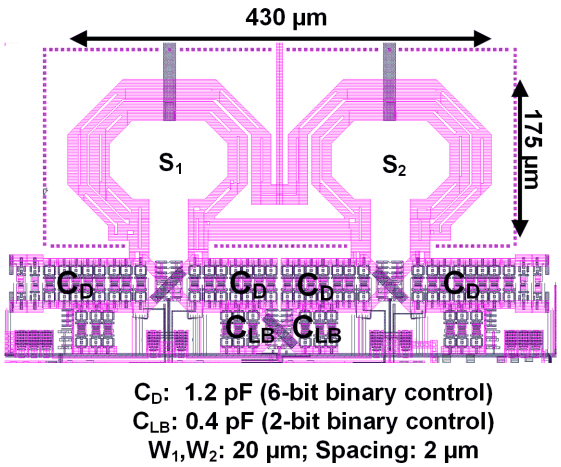


Figure 2.13: Parasitic-aware layout of switched capacitance bank minimizes associated inductance and resistive losses.

of voltage swing at the drain and gate nodes. Bias control is provided by a programmable tail bias resistor (Fig. 2.12). Notably, the inductor center tap-point or virtual ground is now mode dependent as detailed in the following. In this implementation, the supply voltage is provided to the G_M cells by applying it to the appropriate virtual ground nodes in each mode through PMOS switches (Fig. 2.12).

Frequency tuning within LB and HB modes is achieved by a 6-bit digitally-switched capacitor bank, C_D, with an NMOS varactor providing frequency overlap (Fig. 2.7). Switched capacitors, C_{LB}, provides additional two bits of tuning in LB mode. Parasitic-aware layout of the switched capacitors minimizes inductance and resistance due to routing (Fig. 2.13). VCO outputs drive two-stage buffers that are controlled by enable signals that select appropriate buffer in each mode.

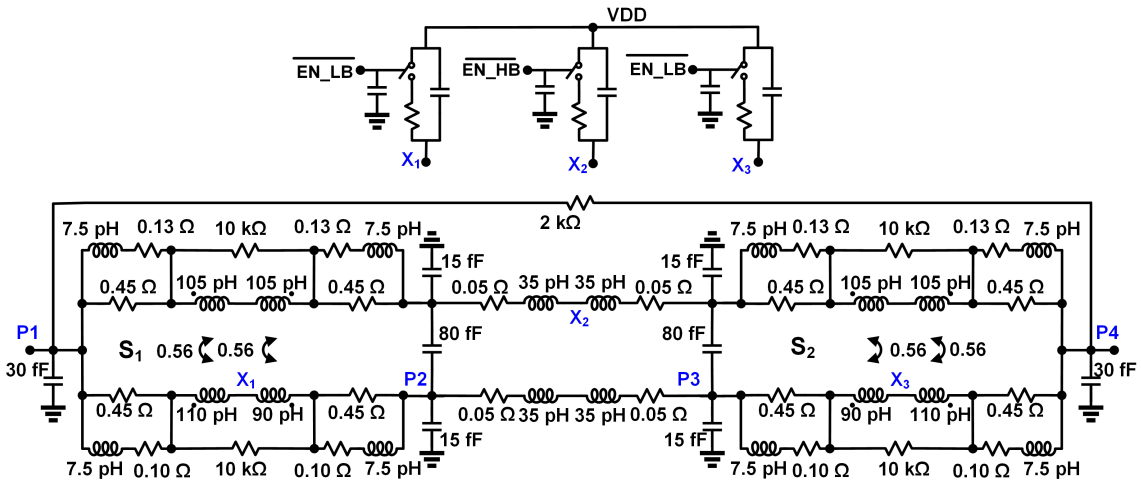


Figure 2.14: Broadband inductor model is necessary for transient simulations, phase-noise optimization and studying impact of supply-switching schemes.

2.3.4 Inductor Modeling

A broadband model for the inductor structure in Fig. 2.7 is necessary for practical phase-noise optimization based on transient simulations and to study the impact of supply switch parasitics in the VCO (Fig. 2.14). This broadband model is developed by relying on the symmetry of the inductor structure in Fig. 2.9 and by using EM simulations that assume excitations, representative of oscillations in the LB mode and in the HB mode. Due to the wide FTR, frequency dependence of losses is modeled using the parallel R and L networks in Fig. 2.14. In LB mode, the center of the inductor structures, X_2, acts as virtual ground and therefore supply for -$G_{M,LB}$ is connected to X_2. The virtual ground shifts to X_1 and X_3 in HB mode and therefore supply for -$G_{M,HB1}$ and -$G_{M,HB1}$ is provided through those nodes. Therefore, the supply switch should be sized while considering the trade-off between increased phase noise due to high on-resistance and the

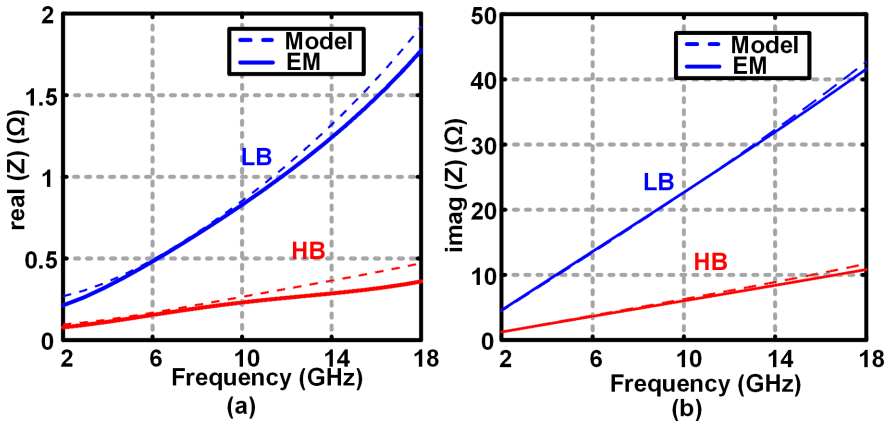
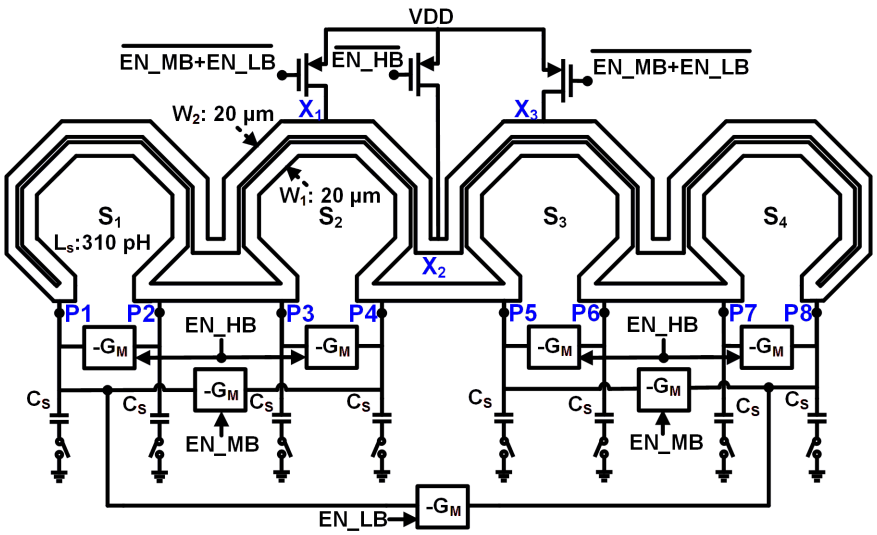


Figure 2.15: Comparison of broadband model and EM simulations of inductor structure for z-parameters.

capacitive loading associated with large switch size, which affects LB mode operation. The broad-band model captures the impact of capacitive coupling between W_1 and W_2 as well as mutual coupling between inductance sections. Fig. 2.15 shows comparison between the broadband inductor model and EM simulations of the structure in Fig. 2.7. Subsequent simulations based on the model in Fig. 2.14 show $<$ 1 dB degradation in phase noise due to supply switch parasitics. Notably, a simpler supply scheme can be adopted in the case of complementary cross-coupled VCO topologies at the cost of increased device parasitics.

2.4 Resonator mode-switching with higher number of modes

The series resonator mode-switching approach can be extended to higher number of modes to achieve wider FTR or to distribute octave FTR among multiple modes. Fig. 2.16 shows the schematic of a triple-mode 2.2 GHz to 8.7 GHz (120% FTR) VCO



	P1	P2	P3	P4	P5	P6	P7	P8
HB	+	−	−	+	+	−	−	+
MB	+	↓	↓	−	−	↓	↓	+
LB	+			↓	↓			−

C_s: 5.17 pF (6-bit binary control)
W_1,W_2: 20 µm; Spacing: 2 µm

Figure 2.16: Schematic of a 2.2 GHz-8.7 GHz VCO that extends the proposed series resonator mode-switching approach to three modes.

that can switch between high-band (HB), mid-band (MB) and low-band (LB) resonator modes. The voltage polarities enforced by the G_M cells at nodes P_1 thru P_8 in HB, MB, and LB modes are shown in Fig. 2.16. Extension to higher number of modes requires a more complex scheme to provide supply voltage to the G_M cells (Fig. 2.16). Assuming that each section ($S_1, S_2, S_3,$ and S_4) has an inductance, L_S, resonance frequencies corresponding to the three modes can be derived as,

$$\omega_{HB} = \frac{1}{\sqrt{L_s(C_s/2)}} \approx \frac{1.41}{\sqrt{L_s C_s}} \tag{2.17}$$

$$\omega_{MB} = \frac{1}{\sqrt{(2L_s)(C_s/2)}} = \frac{1}{\sqrt{L_s C_s}} \tag{2.18}$$

$$\omega_{LB} = \frac{1}{\sqrt{\frac{\sqrt{2}}{1-\sqrt{2}} L_s C_s}} \approx \frac{0.54}{\sqrt{L_s C_s}} \tag{2.19}$$

The three modes provide $\sim$120% FTR in the VCO. Additional, frequency tuning within each mode is provided by implementing C_S as a switched capacitor bank. The scaling of resonance frequencies demonstrates that inductance scales across multiple modes ensuring area efficiency. Additional capacitors can be added across the G_M cells (similar to C_D in Fig. 2.7 for dual-mode VCO) to enhance FTR. However, this was not required for targeted triple-mode FTR VCO.

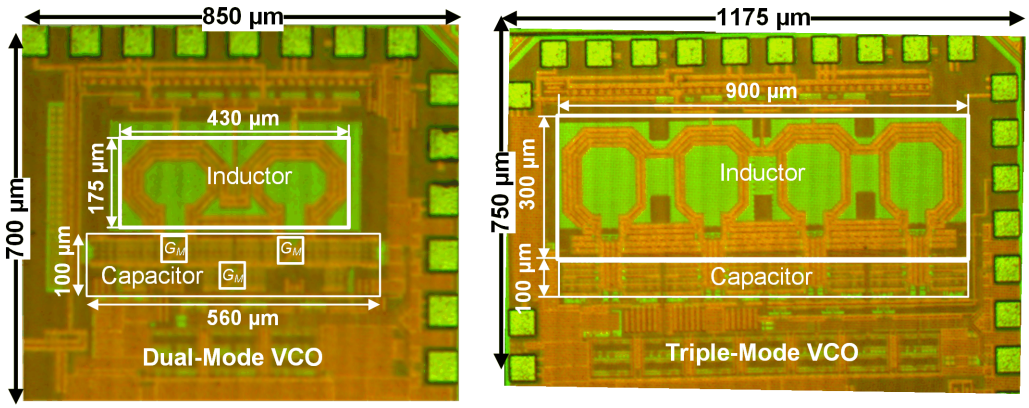


Figure 2.17: Die photo of dual-mode (6.4 GHz-14 GHz) and triple-mode (2.2 GHz-8.7 GHz) CMOS VCO in 65nm CMOS.

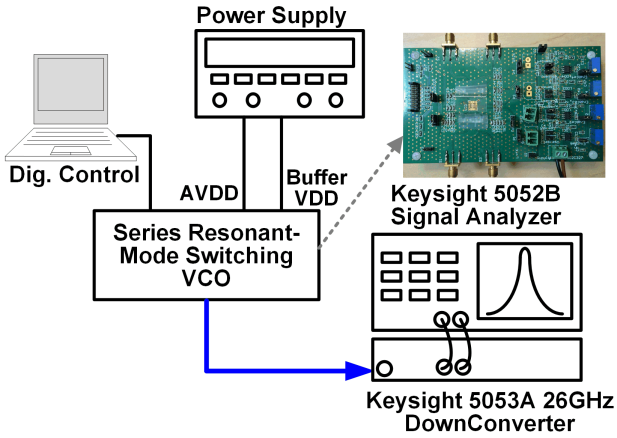


Figure 2.18: Test setup for dual-mode and triple-mode VCO phase-noise measurements.

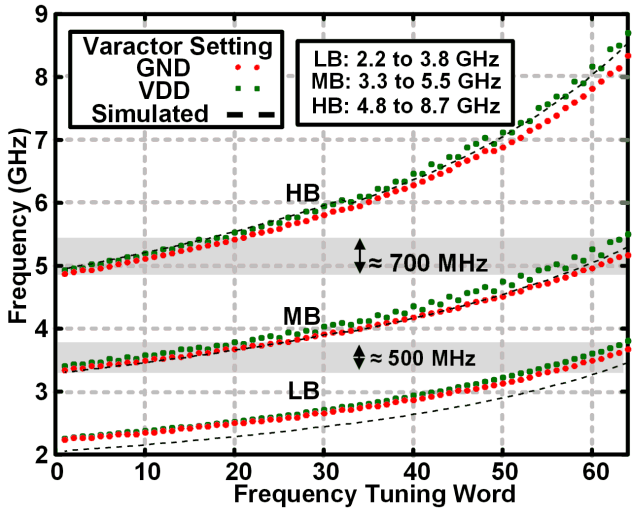


Figure 2.19: Measured triple-mode VCO with $\sim$4$\times$ FTR (>500 MHz overlap).

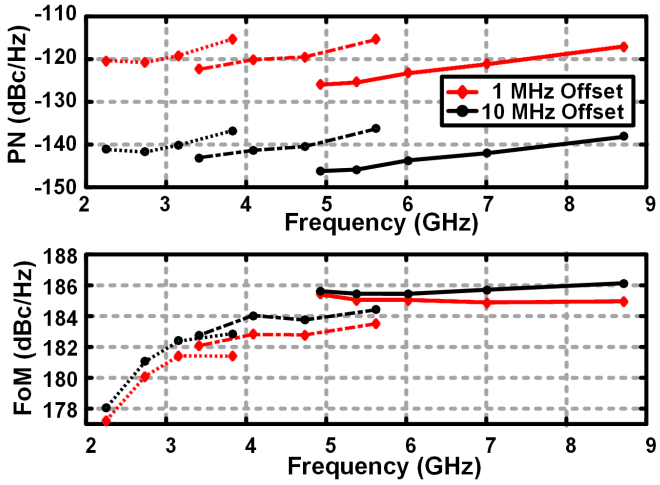


Figure 2.20: Measured triple-mode VCO phase noise and FoM across modes and FTR.

2.5 Measured Performance

The dual-mode and triple-mode VCOs are implemented in a 9-metal 65-nm CMOS process with 3.4-μm thick top metal layer (Fig. 2.17)[17]. Metal density and cheesing rules are followed for wide inductors. VCO phase noise is measured using a Keysight 5052B/5053A Signal Analyzer (Fig. 2.18).

2.5.1 Triple-mode VCO:

The triple-mode VCO achieves an overall 2.2-GHz to 8.7-GHz FTR across the three modes as shown in Fig. 2.19 (2.2 GHz to 3.8 GHz in LB mode, 3.3 GHz to 5.5 GHz in MB mode, 4.9 GHz to 8.7 GHz in HB mode). The $>$ 500MHz overlap between frequency modes and the overlap in each capacitor step within each mode ensures robustness to process variations. The triple-mode VCO consumes 10.3 mW in the LB mode, 12.5 mW in the MB mode, and 32 mW in the HB mode - the supply voltage is varied between 0.5 V and 0.7 V in the frequency and phase noise measurements. The phase noise varies from -136 to -146 dBc/Hz (at 10 MHz offset) across the FTR (Fig. 2.20). The triple-mode VCO FoM matches expectations in high band but phase noise is poorer in the low-band and mid-band due to the loading of the biasing network in Fig. 2.16 in these modes. However, the VCO still achieves $>$182 dB phase-noise FoM from 3.5 GHz to 8.7 GHz (Fig. 2.20). FoM degradation in the low frequency mode because of the supply-switching scheme loading the resonator can be avoided by the use of a complementary cross-coupled G_M-cells topology.

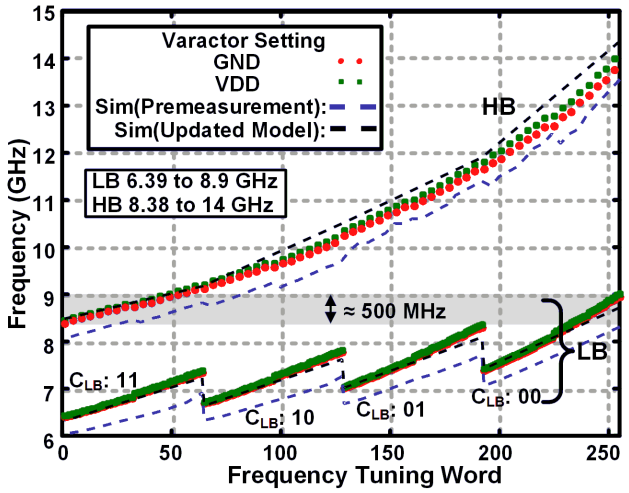


Figure 2.21: Measured dual-mode VCO with octave FTR ($\sim$500 MHz overlap).

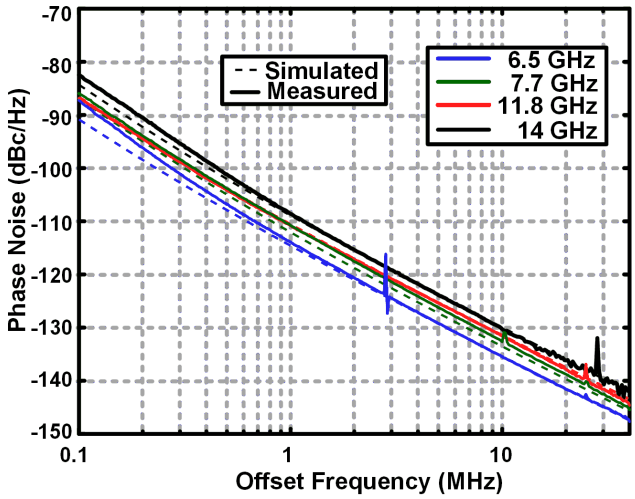


Figure 2.22: Measured dual-mode VCO phase noise across offset frequency for four different oscillation frequencies (data captured from 5052B).

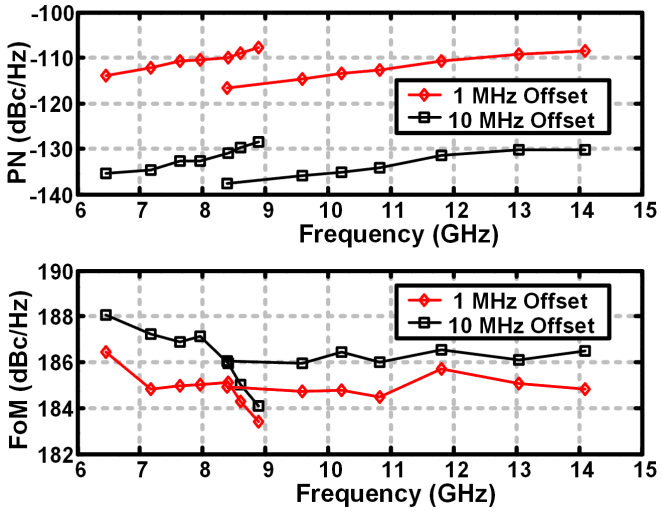


Figure 2.23: Measured dual-mode VCO phase noise and FoM across modes and FTR.

2.5.2 Dual-mode VCO:

The dual-mode VCO operates with a supply voltage of 0.45 V to 0.6 V and consumes 2.2 mW in LB mode and 10 mW in the HB mode. The measured VCO FTR of 6.4 GHz to 14 GHz with 6.4 GHz to 8.9 GHz in the LB mode and 8.38 GHz to 14 GHz in the HB mode are shown in Fig. 2.21. Comparison to simulations demonstrates that the inductor model shown in Fig. 2.14, resulted in $\sim$6% lower oscillation frequency - updating the model post-VCO measurement achieves close match between measured and simulated performance. The $\sim$500 MHz overlap between LB and HB modes again ensures sufficient FTR across process variations. Fig. 2.22 plots the measured phase noise across offset frequencies at four different VCO frequencies and Fig. 2.23 plots the measured dual-mode VCO phase noise and FoM at 1 MHz and 10 MHz offset frequencies. The simulated phase noise agrees with measurements at higher offset frequencies ($>$

Table 2.1: Measured Octave-FTR VCO performance summary and comparison to state-of-the-art wide-FTR VCO.

	Freq. (GHz)	Power (mW)	Area (mm^2)	PN (dBc/Hz)	Δf (MHz)	FoM (dBc/Hz)	FoMT (dBc/Hz)	FoMA (dBc/Hz)	CMOS Tech.
This Work	6.4-14	2.2-10.3	0.126	-130.3/-137.7	10	188-186	205-203	197-195	65 nm
This Work	2.2-8.7	3.5-31.7	0.36	-136/-146	10	178-186	200-208	182-190	65 nm
[24]	2.4-5.3	4.4-6	0.253	-149/-139	10	187-189	205-207	193-195	65 nm
[25]	2.5-5.6	9.8-14.2	0.294	-156.6/-151.7	20	187.7-192.7	205-210	193-198	65 nm
[57]	2.7-6.2	5.8-9.4	0.35	-129/-118	1	184-188.2	201-206	189-193	65 nm
[26]	3.2-8.5	20	0.324	-150.2/-144.4	10	188.6-189.3	208	194-194	40 nm
[53]	5.1-12.9	5-10	0.33	-122.9/-122	1	184.5-189.7	204-208	190-195	180 nm

1 MHz) but is higher than simulated at lower offsets that are dominated by flicker noise. The dual-mode VCO phase noise varies from -130 dBc/Hz to -137 dBc/Hz at 10 MHz offset frequencies and the measured 186-188 dB FoM is comparable to that achieved by VCOs at lower frequencies (Table I), particularly when the lower Q of the capacitor switch bank at $\sim$2.5x higher frequency is considered. As described in Section 2.3, the series resonator mode-switching scheme is area efficient and hence shows state-of-the-art FoM-Area (FoMA) which normalizes VCO area [56].

2.5.3 Discussion on FoMA vs FoMT as metrics for wide FTR VCOs

Wide FTR VCOs are often compared on the basis of three figures-of-merit: VCO phase-noise FoM, FoM normalized to tuning range, FoMT, and FoM normalized to area, FoMA. The VCO FoM is defined in (2.9), and FoMT is defined as,

$$FoMT = FoM + 20\log\left(\frac{FTR\,(\%)}{10}\right) \tag{2.20}$$

Even with narrow FTR assumption, using (2.9) and (2.10),

$$FoMT = 10\log\left(\frac{2P_{TANK}}{kTFP_{dc}}\right) + 20\log\left(\frac{1}{2\omega R_{SW}C_{SW}\left(1+\frac{C}{C_{SW}}\right)}\right) - 10 \quad (2.21)$$

FoM is limited by resonator Q (2.9), and hence serves to compare resonator Q across oscillators. FoMT attempts to normalize the Q degradation due to FTR. However, as shown in (2.8), $Q_{SW,ON} \cdot FTR$ is inversely proportional to oscillation frequency, ω_0. This degrades overall resonator Q. Hence, FoMT, as defined in (2.21), does not capture the difficulty of achieving the same FTR at a higher frequency, and is biased towards lower frequency implementations. Therefore, comparison using FoMT across different topologies are only appropriate for similar oscillation frequencies. On the other hand, FoMA is defined as follows,

$$\begin{aligned} FoMA &= FoM - 10\log\left(\frac{Area}{1mm^2}\right) \\ &= 10\log\left(\frac{2Q^2P_{TANK}}{kTFP_{dc}}\right) - 30 - 10\log\left(\frac{Area}{1mm^2}\right) \end{aligned} \quad (2.22)$$

Hence, FoMA assumes that resonator Q trades off against VCO area such that $Q \propto \sqrt{Area}$. While this assumption is valid if inductor area dominates both VCO area and resonator Q, it is generally not true in the case of high-frequency wide-FTR VCOs where both capacitor *and* inductor Q impact phase noise as well as area. Additionally, FoMA does not normalize resonator impedance (which also affects area) and hence is more suitable for comparing oscillators with similar impedances[55]. The performance of

the dual-mode and triple-mode VCO are compared to state-of-the-art in Table I. Notably, the dual-mode VCO achieves state-of-the-art FoM for octave tuning range VCOs $>$ 10GHz and improves upon FoMA while also occupying the smallest absolute area. This can be intuitively understood - the dual-mode VCO can be viewed as a *merger/overlap* of two VCOs with optimal FoM that together provide octave FTR.

Chapter 3: Coupled-PLL with Single-Wire Synchronization for Large-Scale 5G mm-Wave Arrays

3.1 Introduction

Wideband massive MIMO has emerged as key enabler for wide range of 5G applications by utilizing large-scale arrays with more > 50 low performance inexpensive transceivers [58, 6, 59, 4, 2, 60]. These large array utilizes beamforming and spatial diversity technique to increase the data rate with reliable communication link while improving the overall energy efficiency of system. As the performance of such array depends heavily on coherent processing of signals through multiple channels, coherent clock generation and distribution scheme is required for up/down-conversion of signals and generating sampling clock for ADC.

In the following section, the performance of array in the presence of asynchronous clock distribution is discussed for beamforming and massive MIMO application. Section 3.3 elaborates the shortcomings of conventional clock distribution approaches and presents a scalable architecture of single-wire bidirectional coupled-PLL to generate coherent clock. The noise and stability of four coupled-PLL placed on different tiles is analyzed in Section 3.4 while the implementation details of 28 GHz coherent clock generation is presented Section 3.5. Section 3.6 concludes with measurement results.

3.2 Importance of Coherent clock generation in MIMO systems

3.2.1 Beamforming

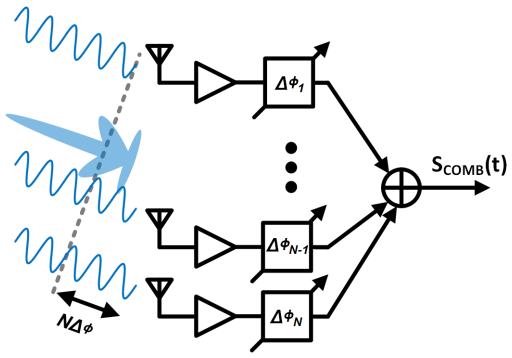


Figure 3.1: Beamforming in MIMO system.

Beamforming is used in MIMO system to form narrow spatial beam using multiple antennas as shown in Fig. 3.1 [58]. The antenna array can transmit or receive signal in a given direction if driven by coherent clock. In the transmitter, the desired signal are phase shifted and radiated coherently in a particular direction while the received signal are added coherently forming a phased array in the receiver. Additionally, spatial null can be employed to suppress signal reception in the interferer direction.

The effect of clock phase noise has been studied in [61] and its effect on desired signal and null formation is illustrated in Fig. 3.2 using two element array for simplicity. The desired signal is passed through mixer driven by incoherent clock (Fig. 3.2(a)) and coherent clock (Fig. 3.2(c)). The incoherent clock is generated from two independent sources while the coherent clock is generated by coupling these two sources resulting in 3 dB lower phase noise. Thus, the effective signal to noise ratio for the desired signal

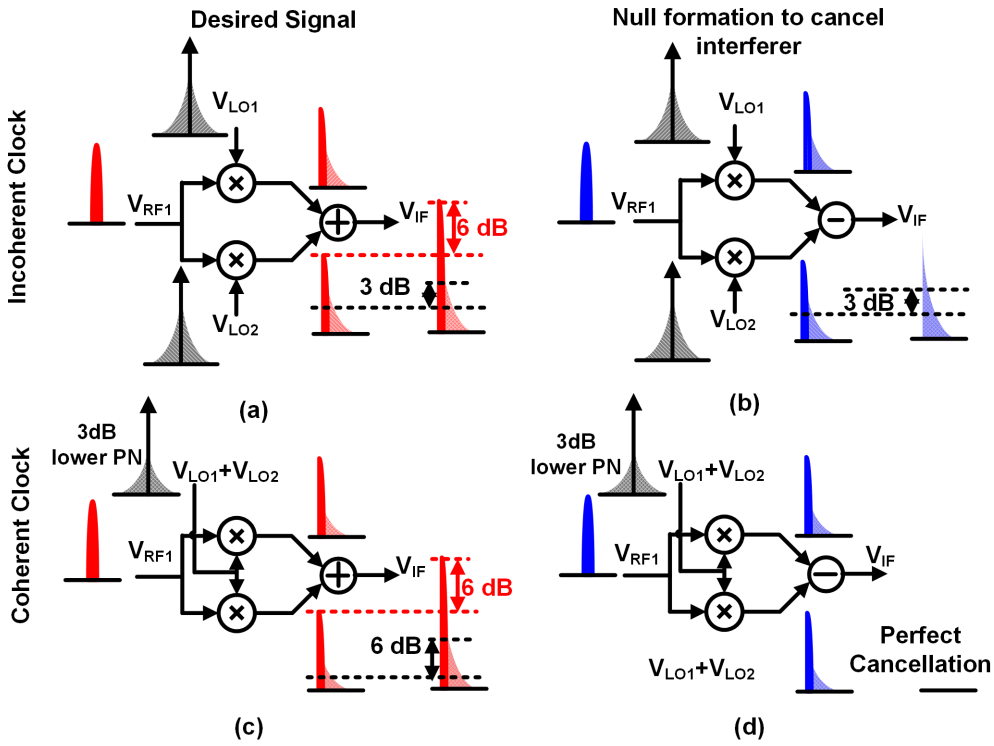


Figure 3.2: Effect of coherent/incoherent processing on desired signal/interferer received through multiple receiver.

is same for the above two cases. On the other hand, null can be formed by subtracting the signals at the mixer output to suppress interferer. Mixers driven by incoherent clock results in imperfect cancellation (Fig. 3.2(d)) compared to when coherent clock (Fig. 3.2(b)) source is used.

3.2.2 MIMO Receiver

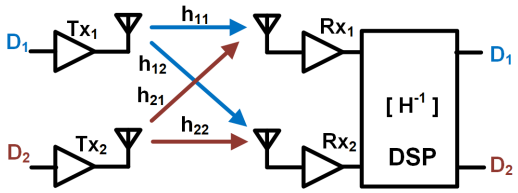


Figure 3.3: MIMO system creating multiple spatial data channels using space-time coding.

MIMO system increases the data rate by taking advantage of multi-path nature of wireless propagation using space-time coding technique. The data from transmitter array passes through channel with channel impulse response constituting of matrix H to receiver input as shown in Fig. 3.3. Multiple data stream can be established by inverting the channel coherently at the receiver baseband. In particular, multi-user massive MIMO system, uses hundreds of antennas to ensure interference free communication while supporting multiple users, increases the capacity of channel with increase in the array size. However, its performance is limited by synchronization across the array.

Similar to null formation in beamforming, any synchronization error creates unattenuated interference [62, 63, 64] and limits the scalability of the array. Additionally, the uncorrelated phase noise from incoherent clock generation leads to loss of orthogonality

[65, 66, 67, 68, 69, 70] between the sub-carriers in OFDM modulation used in massive MIMO system.

3.3 Clock Distribution Approaches

3.3.1 Unidirectional Clock Distribution

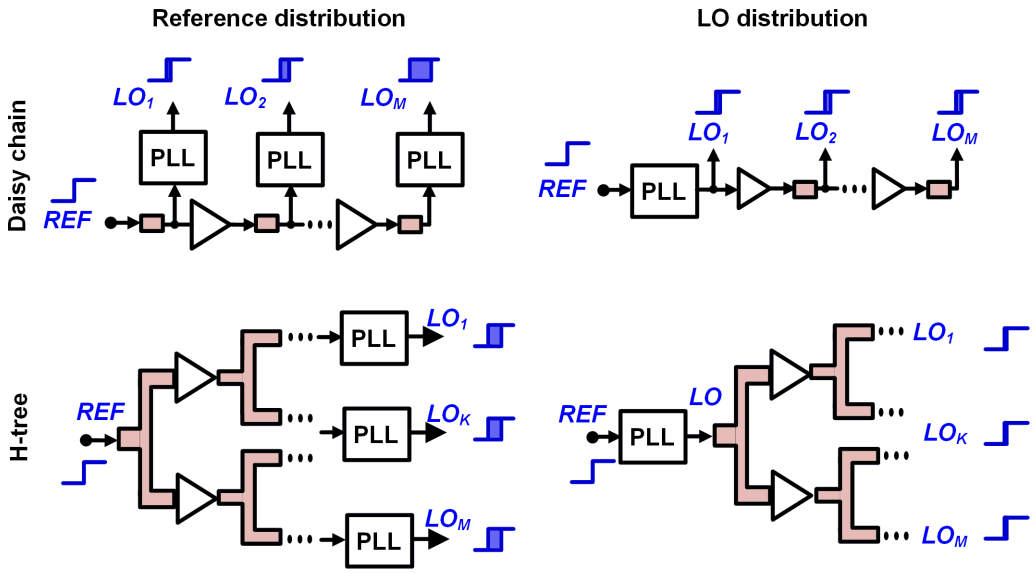


Figure 3.4: Conventional clock distribution approaches using daisy chain and H-tree.

Synchronization across tiles can be achieved by distributing the clock using daisy chain or symmetric H-tree distribution topology as shown in Fig. 3.4. A daisy chain presents a scalable approach which easily allows for an increase in the number of elements. On the other hand, a symmetric H-tree can reduce the number of buffer stages between root and leaves of the distribution tree. It has limited scalability and

reconfigurability as compared to the daisy chain. Further, low frequency reference clock REF (in MHz) or the high frequency LO (in GHz) can be used in the above clock distribution topologies. Reference clock distribution generates the high frequency LO (Fig. 3.4) by using individual PLLs placed on different tiles whereas a common high frequency LO is distributed in the LO distribution scheme. As the low frequency REF is used, the reference clock distribution consumes lesser power compared to the LO distribution. The performance of the clock distribution can be evaluated based on scalability, phase noise and power consumption.

The relative phase coherence LO_i(Fig. 3.4) at each elements are affected due to noise arising from the reference clock, PLL and the clock distribution buffers. The reference frequency generated using crystal oscillator is very precise and stable while its noise appears directly across each element without affecting the coherency of relative LO_i phases. The PLL noise in the LO distribution is common to each element and thus does not affect the relative phases. On the other hand, the PLL noise in each tile are uncorrelated and creates incoherent phases in the reference distribution. Its performance can be improved by using higher frequency REF allowing higher PLL loop bandwidth to suppress the PLL noise. The buffer in clock distribution network also causes relative phase error. As the clock propagates through the daisy-chain, its quality worsens due to accumulation of uncorrelated buffer noise. For instance, the accumulated buffer noise in a N elements daisy chain is proportional to $\sqrt{N}$. On the other hand, the accumulated noise is proportional to $\sqrt{logN}$ in H-tree. The buffer noise can be reduced by increasing the power consumption. The performance of distribution network is summarized in Table 3.1.

Table 3.1: Performance of conventional clock distribution

	Scalability	**Phase Drift/Skew**	**Phase Noise**
REF Daisy Chain	✓✓✓	✗✗✗	✗✗✗
REF H-Tree	✓✓	✗	✗✗
LO Daisy Chain	✓	✗✗	✗
LO H-Tree	✗✗✗	✓✓	✓✓

Low frequency REF distribution suffers from random phase mismatch and phase drift[71, 72, 73] through the interconnects. For instance, a phase mismatch in 0.1^o at 10 MHz reference translates to 280^o phase mismatch at 28 GHz frequency. Additonally, the temperature dependent expansion of the copper trace can cause random phase drift while the thermal gradient can cause phase mismatch due to asymmetric expansion of two same length wires. Assuming the thermal expansion coefficient of copper is 17×10^{-6} K^{-1}, two traces with routing length of 10 cm on PCB with 10^o K temperature difference can cause 1.2^o phase mismatch at 28 GHz frequency.

3.3.2 Bidirectional Clock Distribution

As opposed to an unidirectional daisy chain or a symmetric H-tree distribution, a bidirectional daisy chain (Fig. 3.5) can be adopted where the clock signals are sent back and forth across neighboring elements forming coupled-PLL [74, 75, 76, 77]. As the noise performance of an oscillator can be improved by coupling multiple identical oscillators [78, 79], the bidirectional coupling between PLLs results in lower phase noise [75, 80] with an increase in power consumption and array size. Similarly, random phase

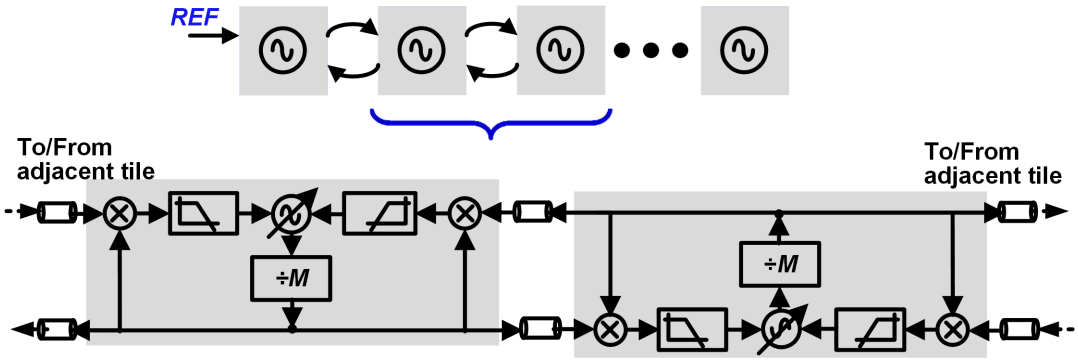


Figure 3.5: Conventional Bidirectional coupled-PLLs.

drift and phase offset through interconnects and distribution buffers are averaged out with an increase in number of PLLs. On the contrary, unidirectional clocking is suboptimal as phase noise degrades with an increase in overall power consumption. Hence, the figure of merit (FoM) of PLL [81], that relates phase noise or jitter to overall power consumption, worsens as number of elements is increased in the unidirectional clocking.

Similar to the coupled-PLL, the clock distribution using coupled injection-locked oscillators [77, 82] can be used to generate coherent clock with improved phase noise as the array size increases. However, a practical array requires that the frequency must be well defined with respect to reference frequency which is generated using a type-II PLL.

Although the bidirectional coupled-PLL generates coherent clock, resultant increase in number of IO pads is undesirable compared to unidirectional clock distribution. Additionally, the phase-shift through the two wires are uncorrelated [83] causing phase drift between the PLL outputs.

3.3.3 Proposed Clock Distribution

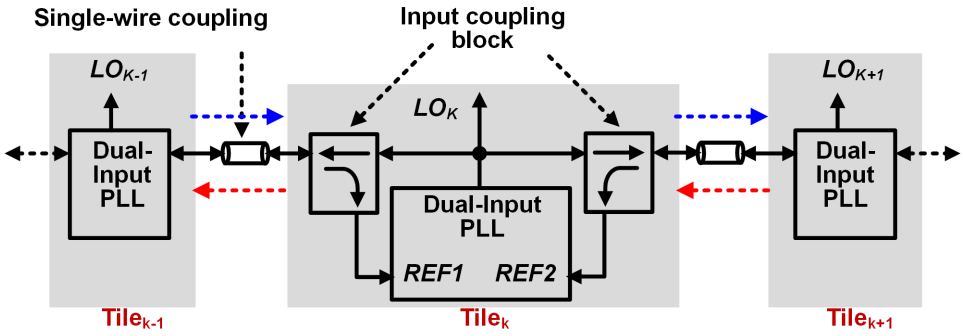


Figure 3.6: Proposed single-wire bidirectional coupled-PLL.

A single-wire bidirectional coupling approach is proposed [84] that preserves the simplicity and scalability of daisy chain while providing phase noise benefits of coupled-PLL with increasing number of elements. As shown in Fig. 3.6, the coupling is accomplished by implementing dual input PLLs where the VCO is controlled by reference signals coming from the neighboring tiles. An input-coupling block works as a circulator and distinguishes between incoming and outgoing signals from the tile. Coupling between the PLL ensures that the phase noise scales as $1/N$ within the coupling bandwidth. A 28 GHz coupled-PLL is implemented for 5G application while the VCO divided by 8 (3.5 GHz) frequency is used to establish the coupling between the neighboring PLLs.

While the bidirectional coupling ensures phase coherence between the tiles, interconnect phase shift can cause phase skew between the PLL outputs LO_i as the type-II PLL is implemented as shown in Fig. 3.7. Phase error at the input of both the phase detectors

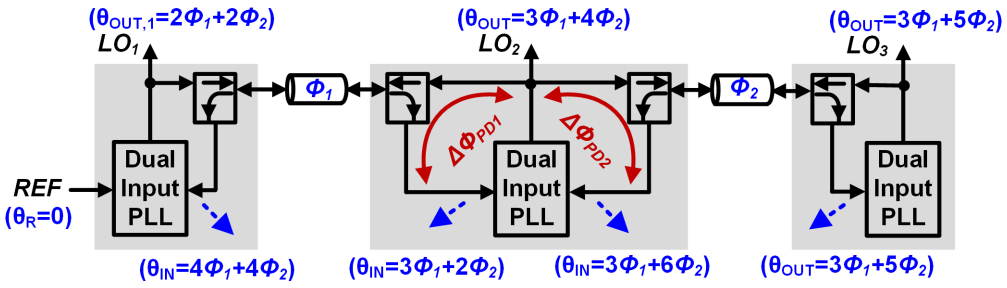


Figure 3.7: Phase offset resulting from arbitrary interconnect delay in type-II PLL.

are related by

$$\Delta\phi_{PD1} = -\Delta\phi_{PD2} \tag{3.1}$$

For an arbitrary interconnect phase shift of ϕ_1 and ϕ_2, the relative phases of LO outputs in the three coupled-PLL is shown in Fig. 3.7 and is dependent on the phase shift through the interconnects. As a single wire is used for bidirectional coupling, the phase shift through the interconnect in both directions is same even in the presence of thermal gradient. Thus, the single wire approach eliminates the random phase drift due to interconnects while the systematic DC phase skew still exists.

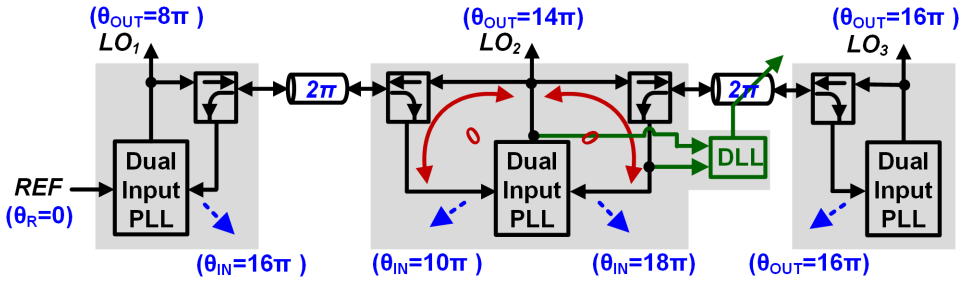


Figure 3.8: Interconnect delay is compensated using DLL to integral multiple of 2π.

However, this skew can be eliminated if the effective interconnect phase shift is an integral multiple of 2π. In order to achieve this condition for an arbitrary interconnect length, on-chip delay lock loop (DLL) is used as shown in Fig. 3.8 with sufficient variable delay to compensate for interconnect phase offset. DLL measures the phase difference between one of the reference paths and the VCO and drives the phase error to zero eliminating the clock skew due to interconnect. The bandwidth of the DLL is chosen sufficiently low to avoid any interference with the PLL locking behavior.

A key limitation of the bidirectional coupling approach is the coupling bandwidth and its impact on stability and noise. In the following section, a framework to analyze noise and stability of the coupled-PLL is discussed which can be extended to higher number of elements.

3.4 Noise and Stability Analysis of Coupled-PLLs

The stability of coupled-PLLs in the presence of delay has been studied [76, 85, 86, 87, 75, 77] using network theory for clock distribution. The proposed coupled-PLL can be represented as a MIMO control system [74, 85, 77] with single reference clock REF as input and N PLL outputs LO_i as shown in Fig. 3.9. The individual PLLs are physically placed on different tiles with T_d delay.

The MIMO model consists of N reference phase detectors in the reference path and N coupled phase detectors in the coupled path. Phase error in the reference and coupled path are

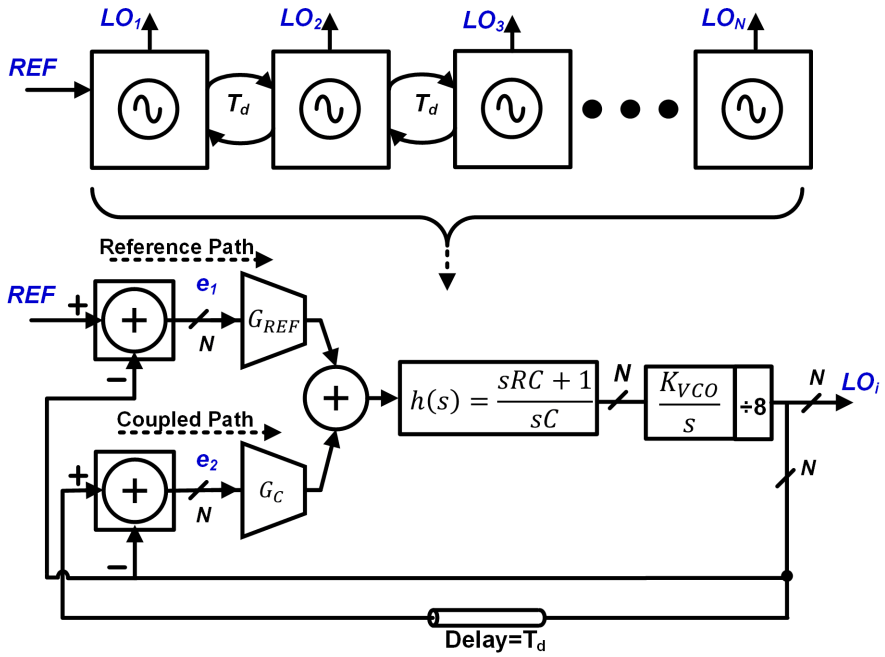


Figure 3.9: MIMO representation of coupled-PLL system in the presence of interconnect delay.

$$e_1 = A_{r1}LO + A_{r2}REF \tag{3.2}$$

$$e_2 = A_c LO \tag{3.3}$$

Where A_{r1}, A_{r2} are the gain from the feedback signal LO_i and the reference clock REF respectively in the reference path. In the coupled path, gain is represented as A_c. For instance, in a cascaded four coupled-PLLs, the gain matrices are

$$A_{r1} = \begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.4}$$

$$A_{r2} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.5}$$

$$A_c = \begin{bmatrix} -1 & e^{-sT_d} & 0 & 0 \\ e^{-sT_d} & -2 & e^{-sT_d} & 0 \\ 0 & e^{-sT_d} & -2 & e^{-sT_d} \\ 0 & 0 & e^{-sT_d} & -1 \end{bmatrix} \tag{3.6}$$

As it can be seen from the gain matrices, a cascaded four coupled-PLL has asymmetry since the first and last PLL has only single neighbors for coupling as well as reference clock is provided to the first PLL. The output of $2N$ phase detectors are followed by transconductors G_{REF} and G_C in the reference and coupled path respectively. The

resultant output currents are summed and passed through the N type-II loop filters with transfer function $h(s)$. The loop filter consists of proportional path resistor R and integral path capacitor C_z and is followed by a VCO with gain K_{VCO}. The interconnect delay T_d between the PLLs is modeled to analyze the stability of the system.

Assuming a type-II PLL, loop bandwidth with respect to the reference path $\omega_{UGB,REF}$ and the coupled path $\omega_{UGB,C}$ can be defined as,

$$\omega_{UGB,REF} = G_{REF} R K_{VCO} \tag{3.7}$$

$$\omega_{UGB,C} = G_C R K_{VCO} \tag{3.8}$$

which are the key loop parameters used in next subsection to analyze the noise transfer function (NTF) and stability of coupled-PLL.

3.4.1 Noise Analysis

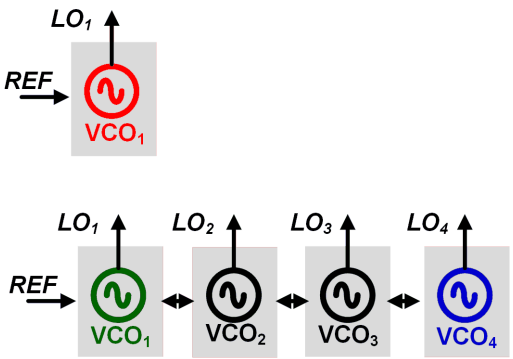


Figure 3.10: Simplified schematic of single PLL and four coupled-PLL showing REF input and LO output.

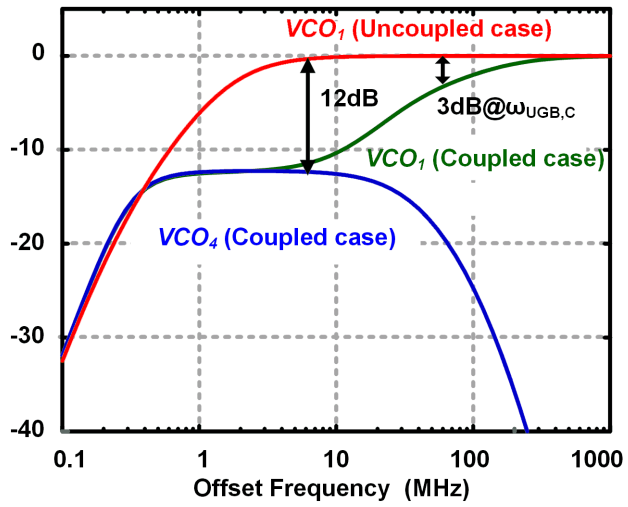


Figure 3.11: NTF of VCO noise in single PLL compared with noise from VCO_1 and VCO_4 to LO_1 output in four coupled-PLLs.

The noise transfer function of the VCO to the coupled-PLL outputs NTF_{VCO} is a matrix transfer function and is,

$$NTF_{VCO} = \left(I - (A_c G_c + A_{r1} G_{REF}) h(s) \frac{K_{VCO}}{s} \right)^{-1} \tag{3.9}$$

$$\tag{3.10}$$

where I is a $N \times N$ identity matrix. The resultant matrix NTF_{VCO} considers the impact of noise from each VCO_i to each PLL output LO_i shown in Fig. 3.10. Additionally, the NTF in a single PLL is compared to coupled-PLL while keeping the same loop parameters such as the gain of loop filter, VCO and phase detector.

The NTF of VCO noise in the single PLL and coupled-PLL is shown in Fig. 3.11.

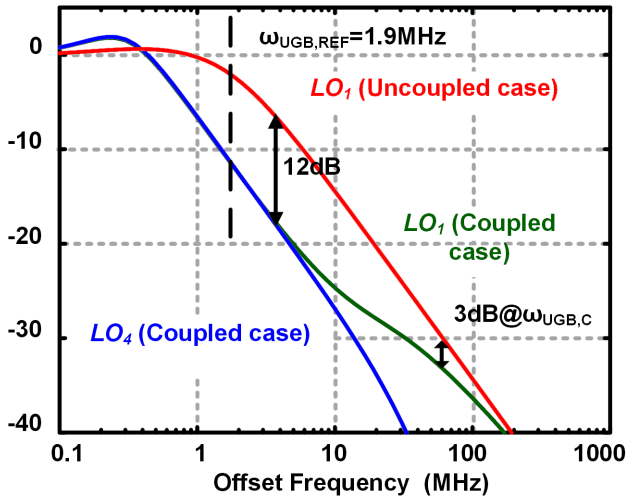


Figure 3.12: NTF from reference to PLL output in uncoupled case is compared to LO_1 and LO_4 in four coupled-PLL.

In single PLL, the NTF of VCO_1 is a high pass filter with 3 dB cut-off frequency set by the PLL reference loop bandwidth. In four coupled-PLL, each of the four VCOs contributes towards noise to each outputs LO_i. The NTF from VCO_1 and VCO_4 at LO_1 output is also compared. Within the coupling bandwidth, the NTF from VCO_1 is lowered by 12 dB whereas NTF from VCO_4 contributes at $LO1$ output and does not contribute outside the coupling bandwidth. Similarly, the NTF from VCO_2 and VCO_3 at output $LO1$ contributes within the coupling bandwidth only. Hence, the overall phase noise decreases by 6 dB or $10\log_{10}N$ within the coupling bandwidth.

A similar analysis is performed for the noise from reference clock to coupled-PLL outputs and is given by,

$$NTF_{REF} = \left(I - (A_c G_c + A_{r1} G_{REF}) h(s) \frac{K_{VCO}}{s} \right)^{-1} A_{r2} G_{REF} h(s) \tag{3.11}$$

which is plotted in Fig. 3.12. Notably, if the individual loop parameters are kept constant for a single PLL and the four PLL, the effective reference loop bandwidth is reduced by a factor of 4. Additionally, there is some asymmetry in the noise transfer function from REF to LO_1 and to LO_4 since the reference is only provided to first PLL.

3.4.2 Stability of Coupled-PLL

Stability of the coupled-PLL is determined by delay T_d between tiles which limits the maximum coupling bandwidth. Fig. 3.13 shows the impact of delay in a four cascaded coupled-PLL. The delay comparable to coupling bandwidth results in peaking in the NTF and can cause instability. Stability can be analyzed formally using generalized Nyquist stability criteria [88, 89] for a MIMO system. Further, the stability is also evaluated in terms of step response of the NTF as shown in Fig. 3.14. An excessive delay T_d relative to the coupling bandwidth causes ringing in the step response. For a practical array size , the tiles can be placed 30 cm apart (corresponding to 1 ns delay) to achieve 10s of MHz of coupling bandwidth.

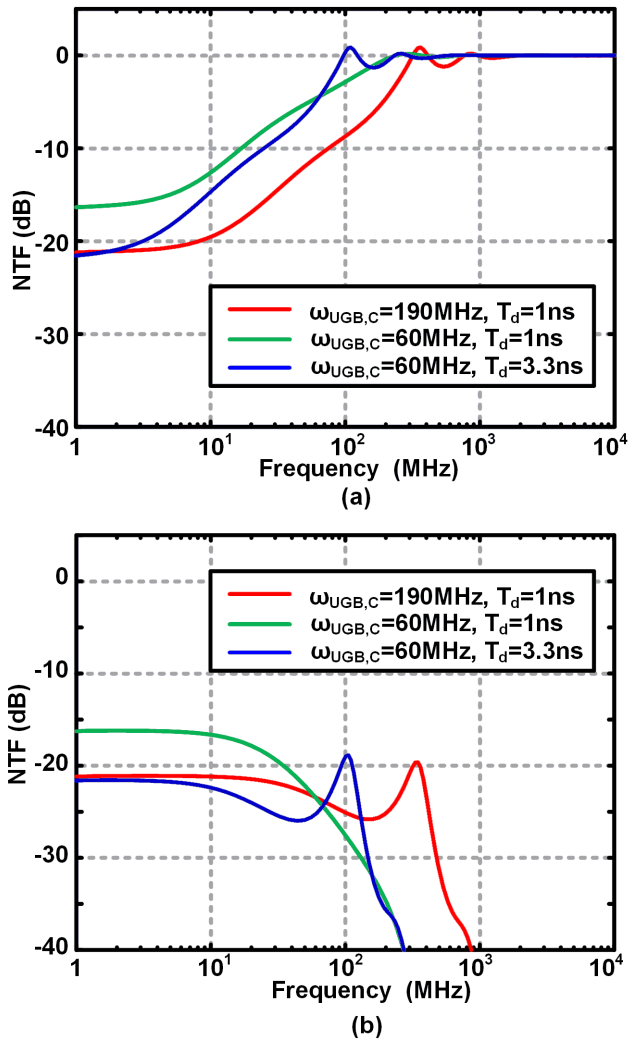


Figure 3.13: Stability degradation from peaking in NTF from (a) VCO and (b) reference when interconnect delay is comparable to coupling bandwidth $\omega_{UGB,C}$.

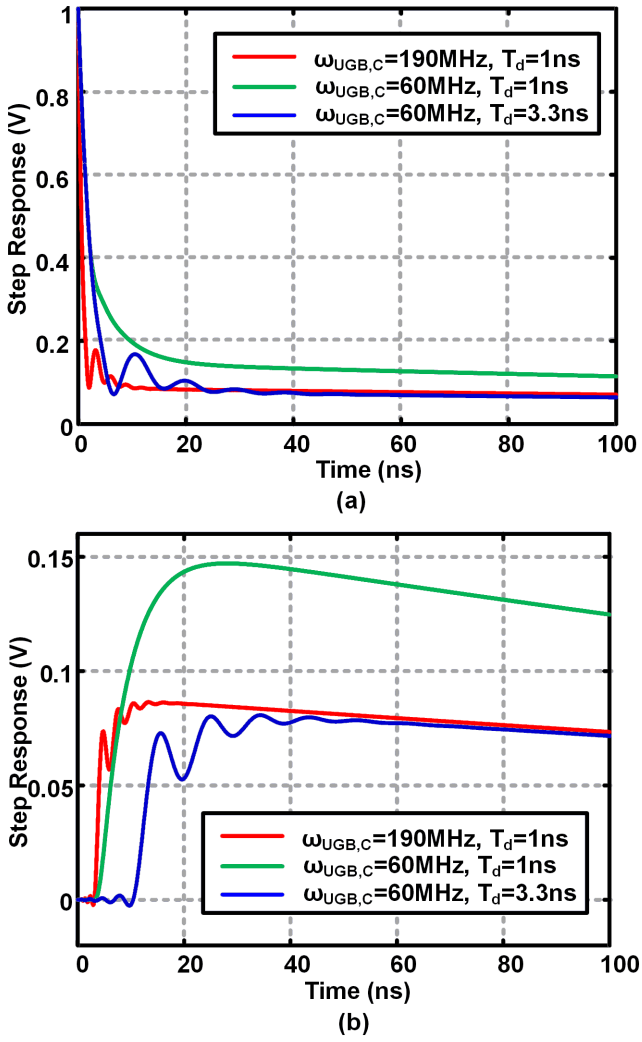


Figure 3.14: Stability of coupled-PLL is illustrated using step response of NTF from (a) VCO and (b) reference.

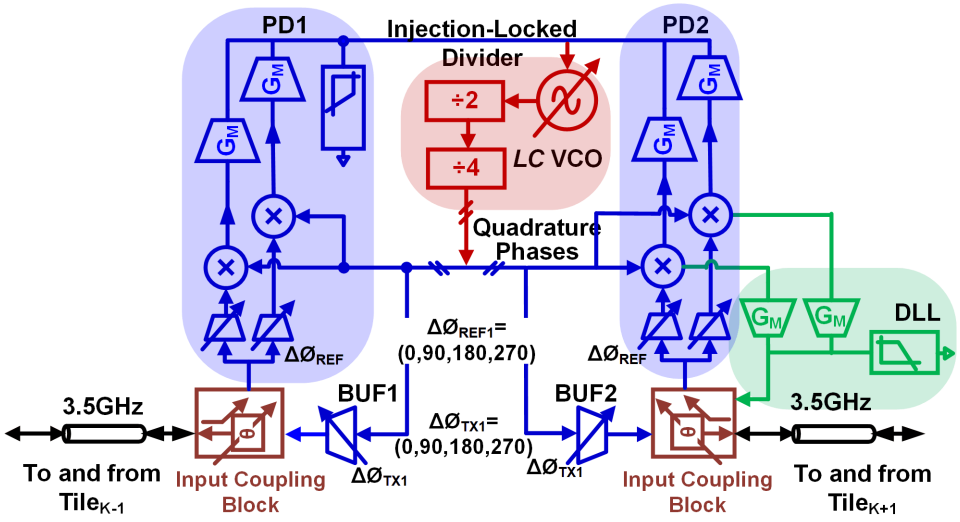


Figure 3.15: Block level architecture of 28 GHz single-wire bidirectional coupled-PLL.

3.5 Bidirectional Coupled-PLL Implementation

3.5.1 PLL

The architecture of 28 GHz bidirectional coupled-PLL is shown in Fig. 3.15. The PLL consists of a differential type-II loop filter, mixer based phase detector, LC VCO, input coupling block and DLL with programmable digital interface. Although mixer based phase detectors are used for simplicity, other phase detector topologies can also be used. Loop filter is implemented using both on-chip and off-chip capacitor with programmable zero frequency. DLL can accommodate arbitrary interconnect phase shift by using continuous voltage controlled delay line and coarse phase-shifters distributed across multiple blocks.

The reference signals from adjacent tiles and divided VCO signal exist on the same

wire which are distinguished using input-coupling block functioning as a directional coupler. Any leakage from divider output to phase detector input via input coupling block creates the phase offset since the divided signal is present at both inputs of the phase detector in a type-II PLL.

The clock distribution frequency represents a trade-off between power consumption, coupling bandwidth, phase noise and die area. Low frequency distribution limits the achievable coupling bandwidth and increases the die area while reducing power consumption. This implementation uses VCO frequency divided by 8 ($\sim$3.5 GHz) clock to establish coupling across the tiles.

3.5.2 VCO and Divider

A cross coupled LC VCO is designed to operate between 25.3 GHz to 30.4 GHz using 3-bit coarse frequency tuning and a varactor based continuous tuning. The VCO output is divided by 2 using an injection locked frequency divider (ILFD) [90] that includes switched capacitor banks to ensure sufficient locking range. The ILFD output drives current mode logic (CML) divider that divides the frequency by four to generate quadrature signal at 3.5 GHz. This signal serves as the feedback signal to both phase detectors as well as the reference signal to adjacent tiles.

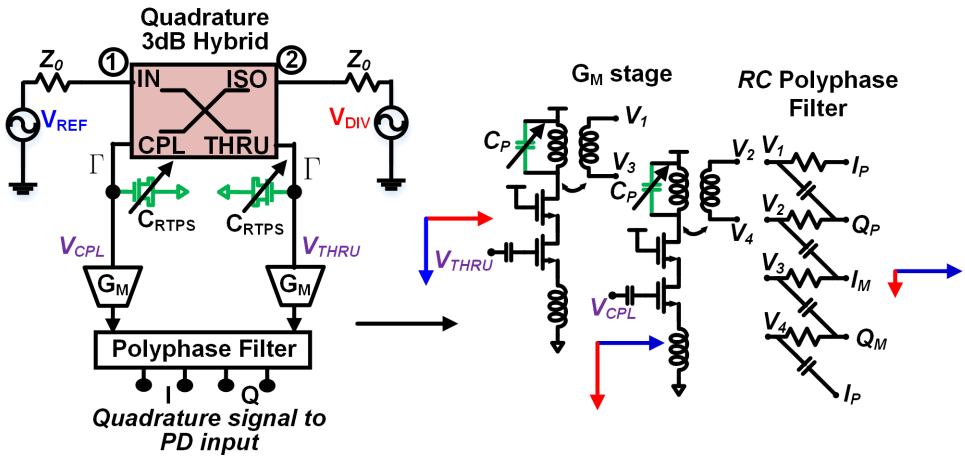


Figure 3.16: Input coupling block separates reference signal from the single wire while providing both discrete coarse and continuous phase shift.

3.5.3 Input Coupling Block

The input-coupling block (Fig. 3.16) consists of a 3 dB hybrid coupler while its through and coupled ports are terminated with high impedance. The signal from divider V_{DIV} drives the isolated port while the reference signal V_{REF} from an adjacent tile drives the input port. The signals V_{CPL} and V_{THRU} are

$$V_{CPL} = 0.7\,(V_{REF} - jV_{DIV}) \tag{3.12}$$

$$V_{THRU} = 0.7\,(-jV_{REF} + V_{DIV}) \tag{3.13}$$

V_{REF} and V_{DIV} appears with quadrature phases at both coupled and through ports with V_{REF} phase leading at coupled port relative to through port while V_{DIV} phase is lagging at coupled port.

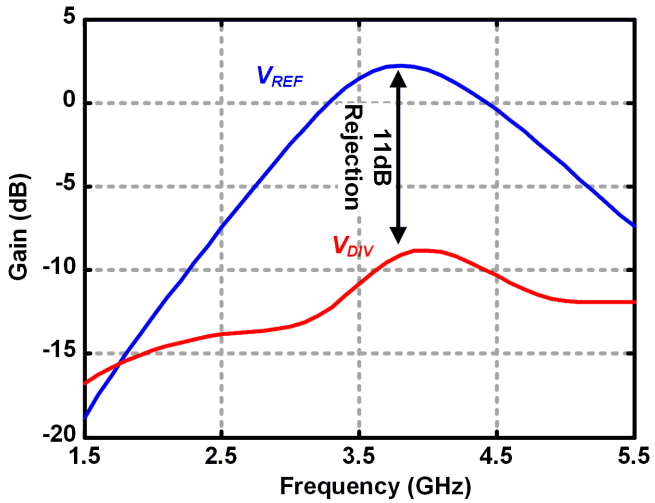


Figure 3.17: Simulated gain from V_{REF} and V_{DIV} to the polyphase filter output.

A RC polyphase filter is implemented at 3.5 GHz to distinguish between two phase progressions at coupled and through ports. Thus, V_{DIV} is attenuated while V_{REF} is unaffected at the filter output as the signals pass through polyphase filter. The polyphase filter is driven by transconductance cells which provides a high capacitive impedance at the coupled and through ports. Simulated performance of the input coupling block including bond wire model is shown in Fig. 3.17 demonstrating rejection of V_{DIV} signal by $\sim$11 dB.

Further, the polyphase filter output have quadrature phases which can be used to suppress any leakage signal from V_{DIV} at the filter output. This suppression is possible because the leakage signal has opposite phase progression compared to reference signal V_{REF}. Therefore, a quadrature phase detector is implemented with little overhead to further ensure low leakage in the PLL.

Additionally, input coupling block provides both discrete coarse phase shift and

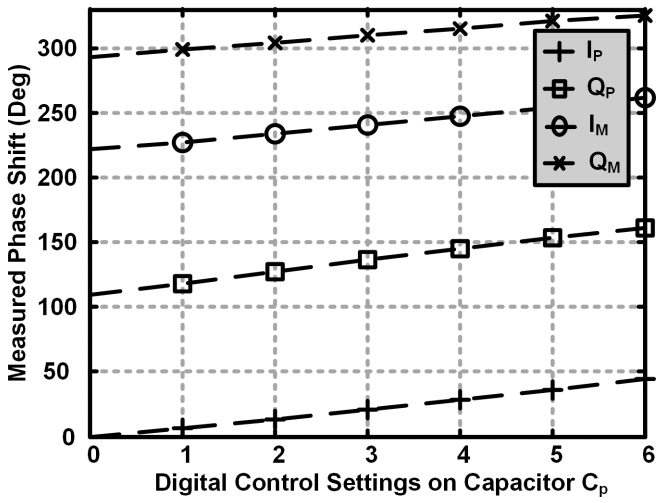


Figure 3.18: Measured coarse phase shift from input coupling block.

continuous phase shift which is being used as a part of DLL. Coarse phase shift of 90^o step size is realized by using quadrature phases at the polyphase filter output while finer discrete phase shift range of $\sim 45^o$ is implemented by varying resonance tank capacitor C_p at the transconductance stage. Fig. 3.18 shows the measured phase shift from input coupling block across discrete setting. Moreover, the hybrid coupler behaves as reflection type phase shifter (RTPS) [91, 92] providing continuous phase shift of $\sim 45^o$ using varactors C_{RTPS} as shown in Fig. 3.16. DLL controls the delay of RTPS by varying bias voltage across the load varactors connected at both coupled and through port of the coupler.

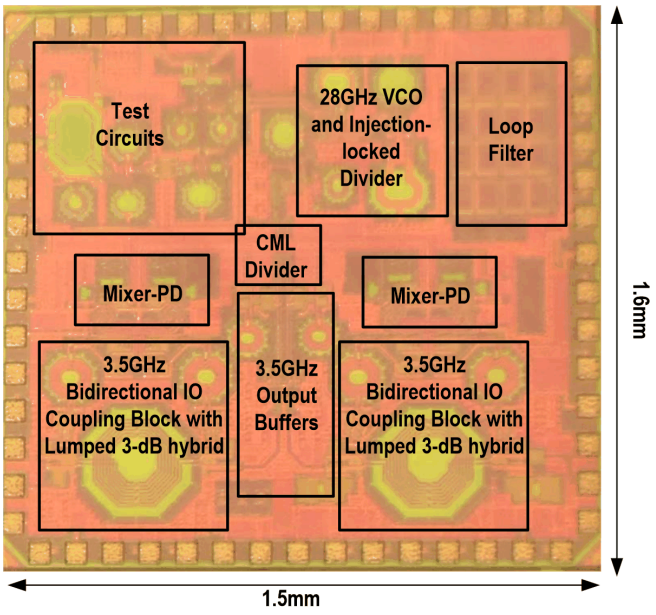


Figure 3.19: Die photo of 28 GHz single-wire coupled-PLL.

3.5.4 DLL

DLL loop senses phase difference at the inputs of mixer based phase detector $PD2$ and varies on-chip phase shifters to lock with quadrature phase difference. The DLL loop bandwidth is set to very low value (in the order of kHz) so that it does not interfere with the PLL dynamics. The continuous DLL voltage drives the RTPS phase shifter while the remaining phase shifts are coarse and preprogrammed using serial interface.

3.6 Measured Performance

A prototype PLL is implemented in a 65 nm CMOS process as shown in Fig. 3.19 occupying a die area of 1.5×1.6 mm^2. The die is packaged using a chip-on-board

Table 3.2: Power consumption summary

Block	**Power Consumption (mW)**
VCO	3.9
Buffer	7.9
ILFD	2.9
CML Buffer	29.3
IQ MXPD	10.5
DLL PD	0.1
Polyphase Gm	24.6
Tx	7.7
Total	87

approach and the power consumption of various block is summarized in Table 3.2. VCO operates from 0.5 V supply while all other blocks in the PLL operates from a 1.1 V supply.

The synchronization across tiles is verified by measuring phase noise improvement in coupled-PLLs compared to cascaded-PLL placed on separate PCB boards as shown in Fig 3.20. A 3.5 GHz reference signal is provided from Anritsu MG3694C signal generator that achieves phase noise of -127 dBc/Hz at 1 MHz frequency offset. The phase noise and spectrum were measured at 3.5 GHz frequency using both R&S FSUP26 signal source analyzer and Agilent E4440A PSA spectrum analyzer. PLLs can be programmed to operate in unidirectional cascaded mode by disabling phase detector $PD2$ and output driver $BUF1$ (Fig. 3.15) and vice versa for bidirectional coupled mode using a serial interface.

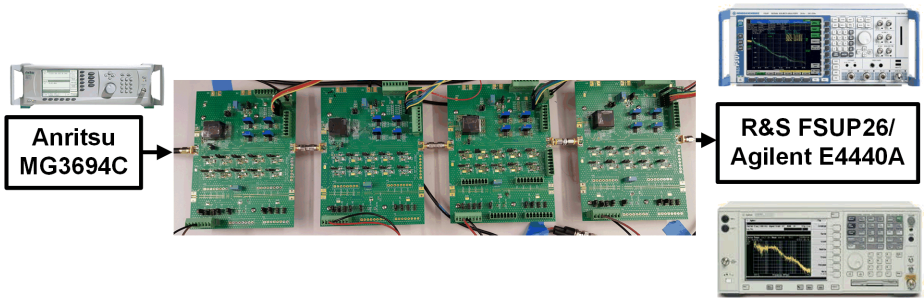


Figure 3.20: Measurement setup to demonstrate performance of four coupled-PLL placed apart on different PCBs.

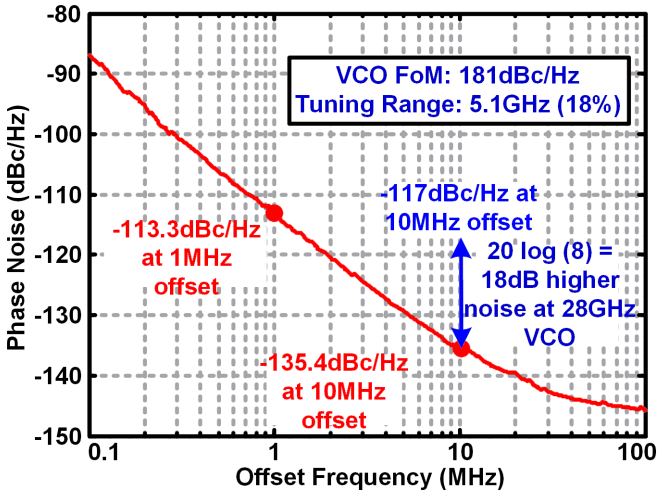


Figure 3.21: Measured phase noise performance of VCO and divider.

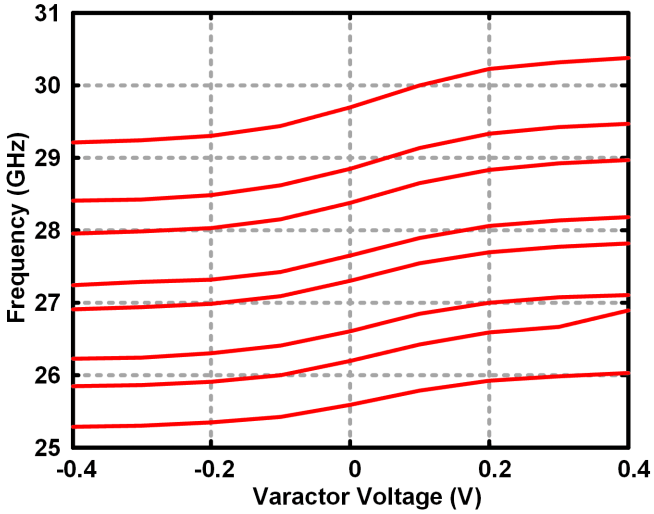


Figure 3.22: Frequency tuning range of VCO.

Fig. 3.21 shows the phase noise of VCO and frequency divider measured at 3.5 GHz divided clock output in an open loop PLL configuration by disabling the phase detectors. VCO is designed using 127 pH tank inductor and consumes 8 mA current from a 0.5 V supply. The VCO and dividers achieved -135.4 dBc/Hz phase noise at 10 MHz offset at 3.5 GHz which translates to -117 dBc/Hz for the 28 GHz oscillation frequency. VCO can be tuned from 25.3 GHz to 30.4 GHz oscillation frequency using 3-bit coarse capacitor bank settings as shown in Fig. 3.22. The VCO achieved 181 dBc/Hz figure-of-merit (FoM) with 18% frequency tuning range at 28 GHz oscillation frequency.

Fig. 3.23 shows the expected performance of coupled-PLL for a constant loop bandwidth across different number of PLLs. The pole frequency of VCO NTF is kept constant by varying the loop parameters to assess improvement in phase noise. With increasing number of PLLs, coupling causes $20logN$ reduction in the NTF of VCO noise whereas the total VCO phase noise increases as $10logN$. Hence, the overall phase

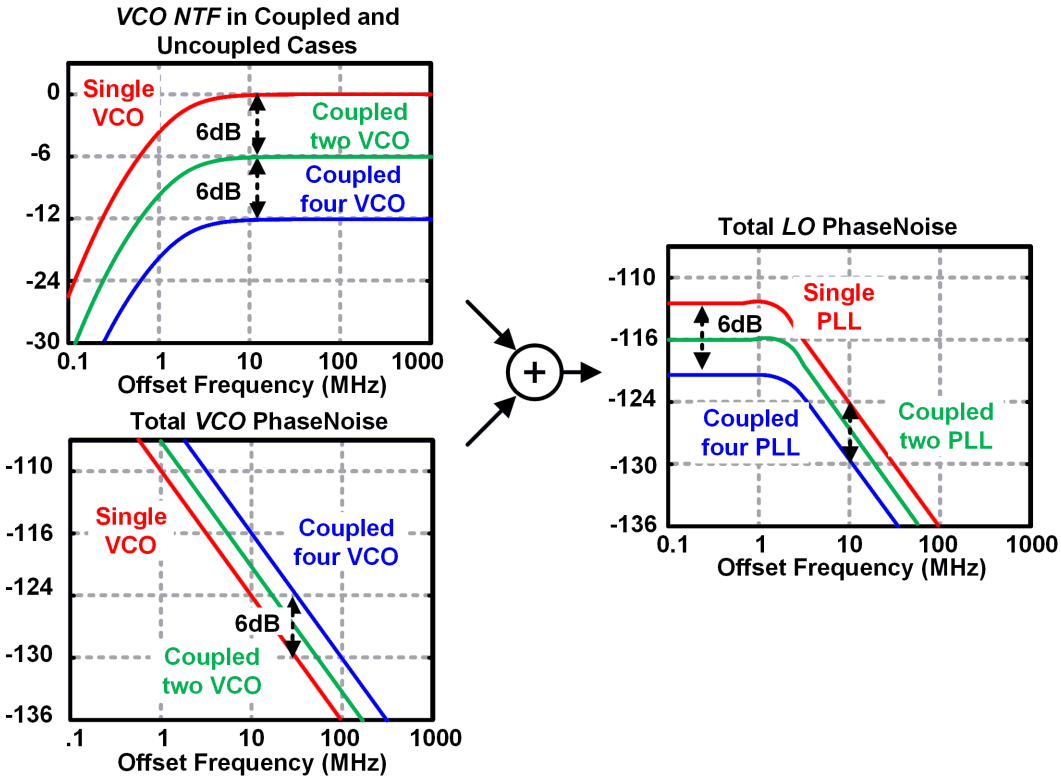


Figure 3.23: Expected reduction in phase noise from VCO due to coupling.

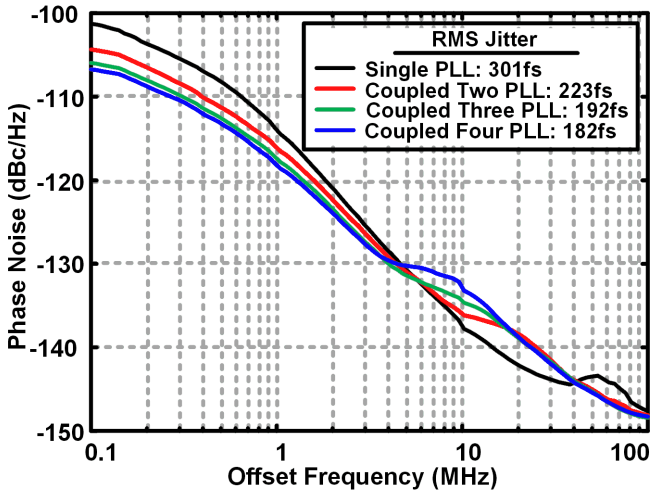


Figure 3.24: Reduction in phase noise with increased in number of coupled-PLL with 1 MHz reference bandwidth.

noise at PLL output is reduced by a factor of $10logN$ provided that the phase noise from reference clock is low.

The measured performance of a stand-alone PLL with a low-noise reference is compared up to four coupled-PLLs as shown in Fig 3.24. Reference loop bandwidth is set to 1 MHz to ensure VCO is the major source of overall phase noise. Results shows a decrease in phase noise within a coupling bandwidth of around 15 MHz. Assuming the jitter contribution from reference is negligible, a decrease in VCO phase noise contribution leads to a decrease in integrated jitter from 300 fs in single PLL to 182 fs in four coupled-PLL.

A similar measurement is carried out upto three coupled PLLs with a reference bandwidth set to 3 MHz. Again, an improvement in phase noise is observed with integrated jitter reduced from 183 fs in single PLL to 103 fs in three coupled-PLL.

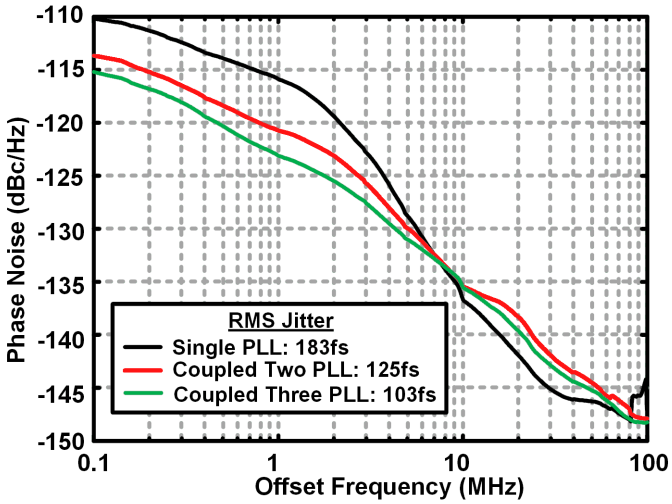


Figure 3.25: Reduction in phase noise with increased in number of coupled-PLL with 3 MHz reference bandwidth.

3.6.1 Performance of DLL

The performance of DLL is measured by inserting phase shifters between the PLLs to model any arbitrary interconnect phase shifts as shown in Fig. 3.26. The phase shifter can provide limited phase shift range from 0^o to 210^o at 3.5 GHz. The continuous phase shift in the DLL comes from the input coupling block while the discrete coarse phase shifts are provided through the output driver and gm-cells. As the interconnect phase shifters setting are varied, the on-chip discrete phase shifters are programmed manually using serial interface whenever DLL exceeds the range of continuous phase shifter. The measured result of DLL is shown in Fig 3.27 demonstrating its ability to lock over wide range of interconnect phase shifts.

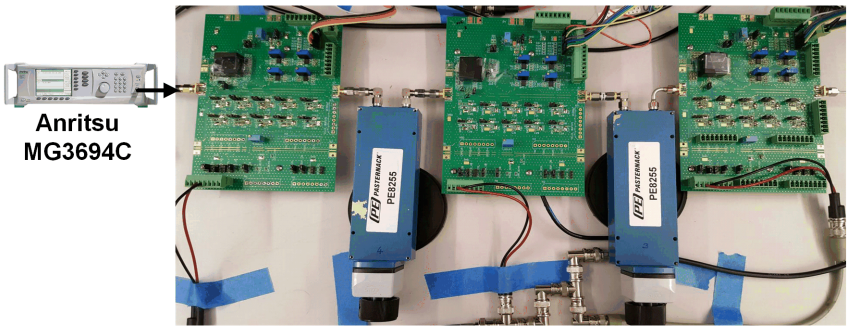


Figure 3.26: Measurement setup demonstrating DLL performance using external phase shifters to model arbitrary interconnect length.

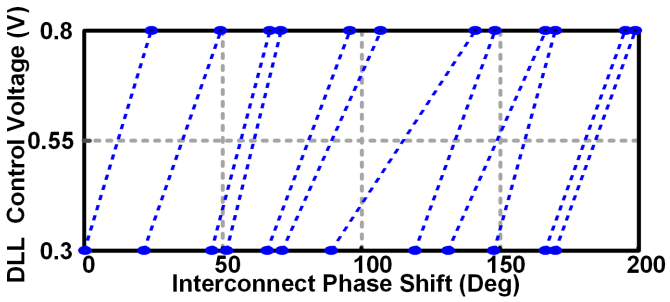


Figure 3.27: Demonstrates DLL's ability to compensate interconnect delay.

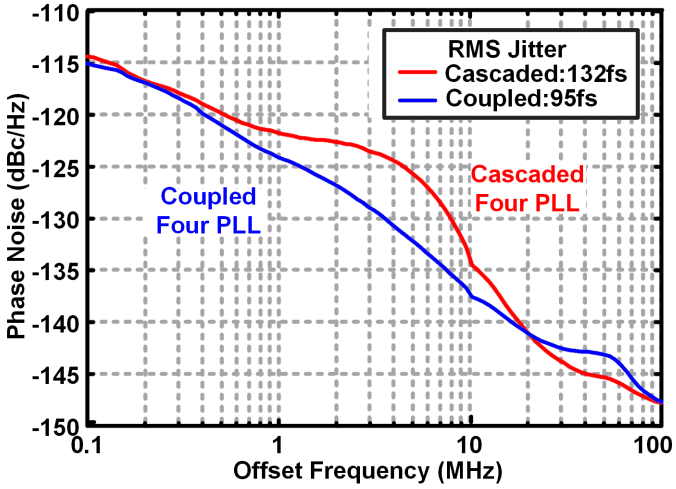


Figure 3.28: Phase noise performance of four cascaded-PLL and coupled-PLL.

3.6.2 Comparison between cascaded and coupled-PLL

Fig. 3.28 compares the phase noise for four cascaded-PLL and four coupled-PLL demonstrating improvement in jitter and phase noise associating with bidirectional coupling as opposed to a cascaded loop for four PLLs. In the cascased PLL, bandwidth of the first PLL is optimized to reduce integrated jitter coming from both reference and VCO while the bandwidth is set to maximum to reduce the VCO noise from all further cascaded stages. On the other hand, the reference loop bandwidth is optimized to reduce overall jitter from both reference and coupled VCOs in coupled-PLL. A similar measurement is carried out to compare three cascaded-PLLs with three coupled-PLLs as shown in Fig. 3.29 demonstrating improvement in PLL figure-of-merit [81]. In the cascaded mode, overall power consumption increases with increasing number of PLLs; however there is no improvement in jitter. On the other hand, bidirectional coupling improves jitter as PLLs are increased without requiring any overhead in IO pads on the

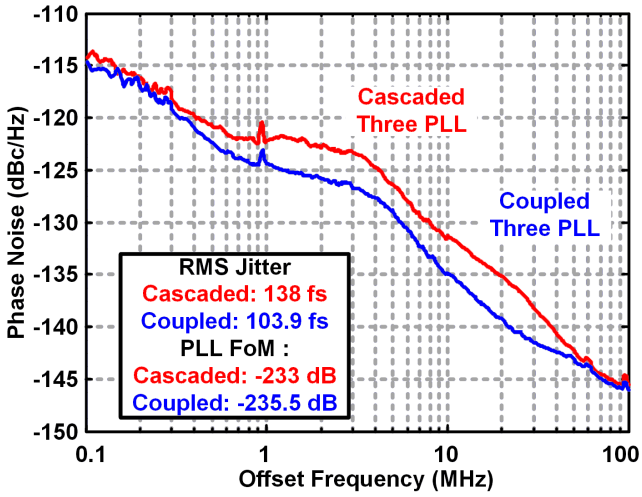


Figure 3.29: Performance comparison of three cascaded-PLL and coupled-PLL.

PCBs. Further, As the number of PLLs increased, the improvement in jitter limited by the reference noise.

3.6.3 Jitter optimization in the presence of noisier reference

PLL is used to filter a noise from both reference clock and VCO while the loop bandwidth is optimized to reduce total integrated jitter [81]. Fig. 3.30 shows the measured performance of the single PLL and coupled-PLL in the presence of a noisier reference. As the number of coupled-PLLs is increased, the effective VCO noise decreases and hence the optimal reference loop bandwidth reduced to filter out more noise from reference clock. The loop parameters for each of single, two and three PLLs were adjusted to achieve optimum jitter, demonstrating the reduction in achievable jitter as PLLs are coupled together.

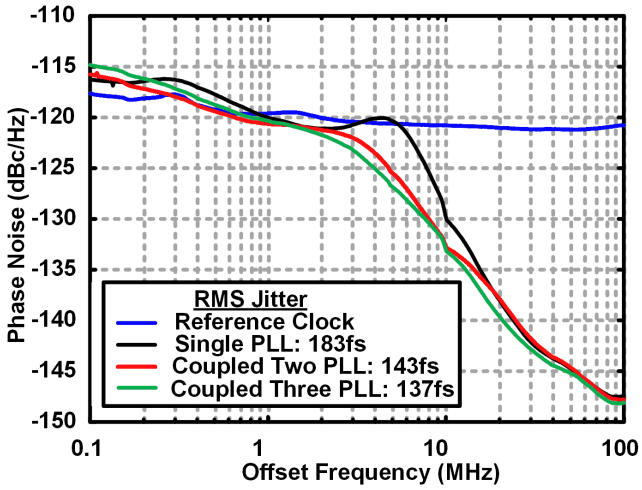


Figure 3.30: Bandwidth optimization of coupled-PLL in the presence of nosier reference.

Chapter 4: Concurrent Dual Frequency Bandstop Filter based on Walsh Function Sequence Mixing

4.1 Introduction

N-path passive mixer (Fig. 4.1) has been shown to achieve high-Q filtering around a LO-defined frequency[93, 94, 95, 96, 97, 98] using the impedance translation property of the mixer. N-path mixers based tunable bandpass[94, 97] and bandstop filters[95] driven by non-overlapping clock pulses (NOP) have been theoretically analyzed in detail and demonstrated in CMOS technologies. In such filters, the center frequency is defined by the LO frequency and the passband/stopband bandwidths are specified by baseband impedances. As shown in Fig. 4.1, bandpass and bandstop filters using the N non-overlapping pulses can be modeled to an equivalent shunt LC networks [95]. Recently, combined approaches have demonstrated higher blocker tolerance which is suitable for tunable SAW-less receiver application[99, 100]. Since the SAW filters are bulky off-chip component working at fixed center frequency, several SAW filters are needed to cover multiple frequency bands. The integrated N-path filter provides alternative cost effective solution with tunable center frequency, high linearity and high selectivity to mitigate large out-of-band blocker.

N-path filters rely on minimal overlap between clock pulses driving the switches. Such overlap causes charge sharing between the filter capacitors which leads to performance

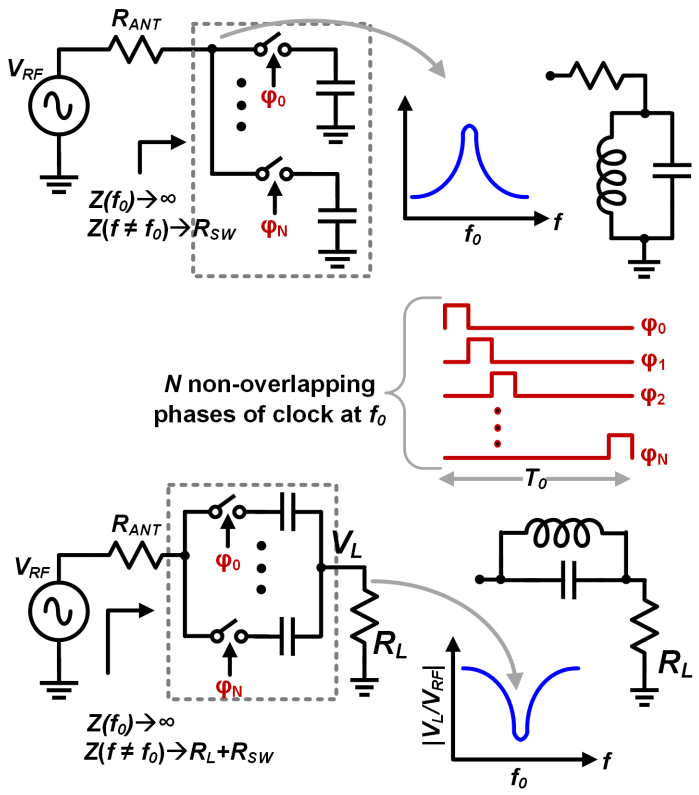


Figure 4.1: N-path passive mixers with non-overlapped LO pulses for (a) bandpass filtering, and (b) bandstop filtering. The filter can be modeled by a parallel LC network.

degradation [101, 97, 102] and limits the ability to reject interferers concurrently at different frequencies by placing two filters in parallel. Moreover, the bandstop filter [95] results in a high input impedance in the stopband causing large voltage swing [99] which is undesirable to ensure reliability of the transistors.

In this chapter, a passive bandstop filtering approach is presented in 65 nm CMOS technology where the passive mixers are driven by Walsh Function (WF) sequences as opposed to NOP. The WF sequence (WF-seq) based mixer enables a reconfigurable bandstop filtering where the filters are placed in parallel to the signal path as opposed to the series approach in [95]. Further, multiple bandstop filters operating at different frequencies are placed in parallel enabling concurrent rejection of two interferers across 0.3 GHz to 1.4 GHz.

The theoretical analysis of WF-seq based passive mixer using a signal space approach is presented in Section 4.2. Its equivalence to the N-path passive mixer is also presented in detail. Section 4.3 describes the design and implementation of the proposed filter and its measurement results are presented in Section 4.4. Further, the above approach is extended to concurrent bandpass filters in Section 4.5.

4.2 Bandstop Filtering with WF Sequence Mixing

Fig. 4.2 illustrates a current driven passive mixer using N-phases of NOP $\varphi_i(t)$ to drive the mixer switches. Assuming 4-phases without loss of generality, for a sinusoidal input at the LO frequency creates steady-state capacitor voltages as shown in Fig. 4.2. A rigorous mathematical analysis of the N-path passive mixers using transient signals

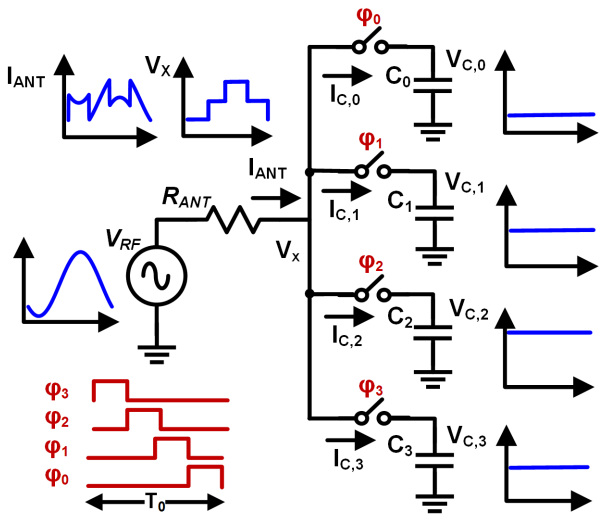


Figure 4.2: Operation of N-path filter.

[93] and linear periodically time variant (LPTV) state space analysis [95, 94] has been already described in literature. In the following subsection, a high-level overview of the operating principle is presented to motivate the equivalence between the WF-seq and NOP based passive mixer.

4.2.1 N-path Mixer as Correlators

The steady-state voltage, $V_{C,i}$ on N-path capacitors, C_i (Fig. 4.2) is only dependent on the $V_{RF}(t)$ when φ_i is high and is independent of $V_{RF}(t)$ when φ_i is low. Using the fact that RC time constant of capacitor at baseband is much larger than period of NOP, for a sinusoidal input signal, the average current through capacitor $I_{C,j}$ is zero as the capacitor have reached to their steady-state voltage. The current $I_{C,j}$ and RF voltage at V_x can be written as,

$$I_{C,j} = \frac{1}{R}\int \left(V_{RF}(t) - \sum_{i=0}^{i=3} V_{C,i}(t)\varphi_i(t) \right) \varphi_j(t)dt = 0 \tag{4.1}$$

$$V_x = \sum_{i=0}^{i=3} V_{C,i}(t)\varphi_i(t) \tag{4.2}$$

Since the NOP functions are orthogonal [103], any two NOP are related as

$$\int_0^{T_0} \varphi_i(t)\varphi_j(t)dt = \delta_{ij} = \begin{cases} 1, & \text{if } i = j \\ 0, & \text{if } i \neq j \end{cases} \tag{4.3}$$

Using (4.3) in (4.1), the steady state voltage across capacitor is

$$V_{C,j} = \int V_{RF}(t)\varphi_j(t)dt \tag{4.4}$$

Thus, $V_{C,i}$ can be interpreted as the dot product of $V_{RF}(t)$ and $\varphi_j(t)$. Therefore, an N-path mixer can be viewed as a bank of parallel correlators, where in each path the signal is correlated to $\varphi_j(t)$, and the result of the correlation is stored in the capacitor voltage. It follows from (4.4) that if the frequency of NOP $f_0 = \frac{1}{T_0}$ is not equal to the signal frequency (f_s), then the resultant dot product is zero. When $f_s = f_0$, the correlation from (4.4) leads to the staircase approximation of input signal (Fig. 4.2) that results in a smaller residual current through the load and a bandstop frequency response is observed at output load current. Increasing the basis set size by increasing the number

of NOP phases decreases the error between the input signal and V_X. This leads to a smaller residual current through the load with reduced harmonic content and improved rejection of load current at bandstop frequency. Notably, since the capacitors store a voltage in response to the RF current, this approach requires non-overlap in addition to orthogonality.

4.2.2 Signal representation using Walsh Functions:

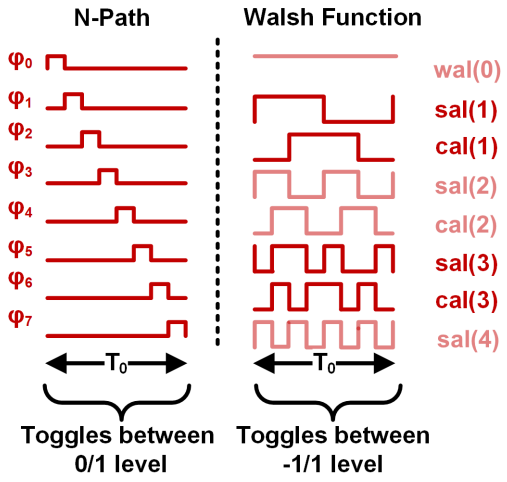


Figure 4.3: 3^{rd}order WF-seq compared to typical N-path non-overlapping clock pulses. Higher order Walsh functions will have higher zero crossings within T_o.

Walsh functions (WF), similar to Fourier transform, represent a complete and orthogonal basis set for representing signals [103]. WF, as shown in Fig. 4.3, are restricted to ± 1, making them compatible with digital implementations. The order of WF-seq can be increased by generating additional sequences with higher number of zero crossings in time period T_0 [103]. This is in contrast to NOP approach where a higher

number of phases require re-generation of the entire NOP set with smaller pulsewidths for each phase. Fig. 4.3 shows a 3^{rd}order WF-seq along with 8-phase NOP with same duration T_0.

Similar to Fourier series, any periodic signal $x\,(t)$ can be represented as sum of the product of WF coefficients c_i [103] and $WF_i(t)$,

$$x(t) = \sum_{i=0}^{\infty} c_i WF_i(t) \tag{4.5}$$

where $WF_i(t)$ represents ith WF-seq. The WF coefficients are computed by,

$$c_i = \int_0^{T_0} x(t) WF_i(t) dt \tag{4.6}$$

For the 2^{nd}order WF, the WF coefficient c_i for sinusoidal signal at frequency f_0 and the correlation with the 4-phase NOP is shown in Fig. 4.4. For a zero-mean sinusoidal signal, the correlation with $wal(0)$, $sal(2)$ are zero (shown as faded waveform in Fig. 4.3 and Fig. 4.4). Therefore, a 2^{nd}order WF representation of the input signal requires only two correlator. Similarly, a 3^{rd}order WF representation requires four correlator: $sal(1)$, $cal(2)$, $sal(3)$ and $cal(3)$. Fig. 4.5 plots the residual signal $s_{res}\,(t)$ which is defined as,

$$s_{res}(t) = x(t) - \sum_{i=0}^{N} c_i WF_i(t) \tag{4.7}$$

Further, $s_{res}(t)$ can be reduced by taking higher order terms from WF-seq similar to Gibbs phenomenon in Fourier series. The fundamental component of $s_{res}(t)$ defines the amount of rejection provided by filter and can be expressed using (4.7) as

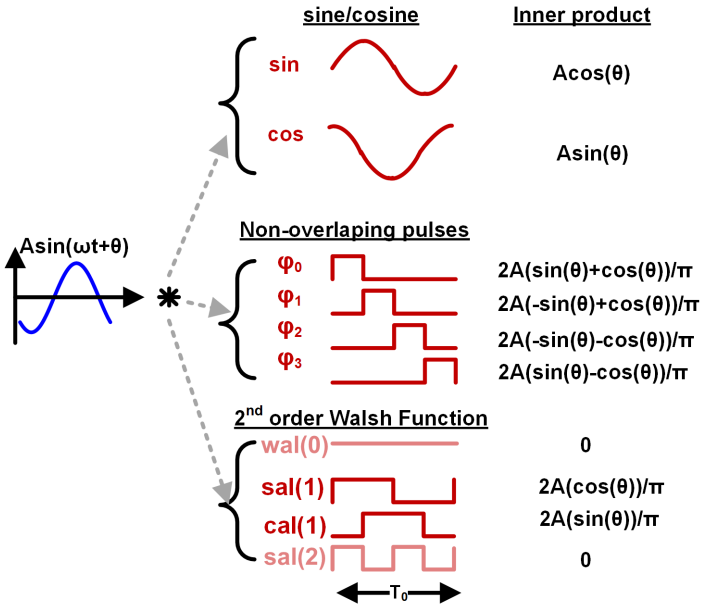


Figure 4.4: Correlation of sinusoidal signal with sinusoid, NOP and WF.

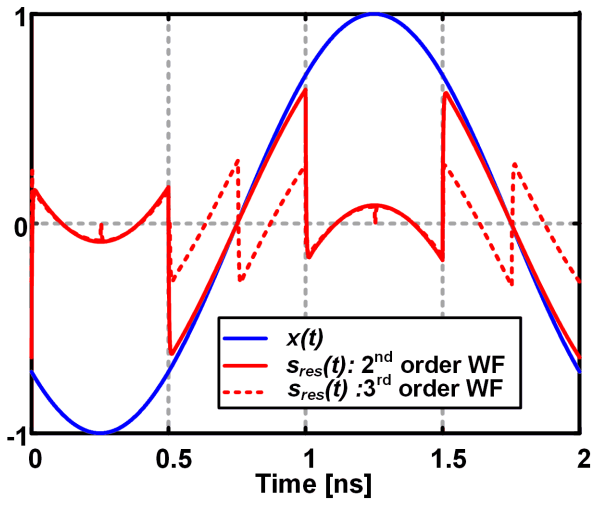


Figure 4.5: The residue between input and staircases approximated signal using Walsh function reduces as order of WF-seq increases.

$$s_{res,fund}(t) = x(t) - \sum_{i=0}^{N} c_i WF_{i,fund}(t)$$
$$= x(t)(1-\alpha) \tag{4.8}$$

where α for 2^{nd}order and 3^{rd}order WF-seq are $\frac{8}{\pi^2}$ and $\frac{16(2-\sqrt{2})}{\pi^2}$ respectively. From (4.8), the residual signal $s_{res,fund}(t)$ is 14.4 dB and 24 dB lower in power compared to the input signal for 2^{nd}order and 3^{rd}order WF respectively which are identical to that computed for 4-phase and 8-phase NOP in [95]. A simplified model of bandstop filter is discussed in the next subsection and a detailed derivation is presented in Appendix C.

4.2.3 Walsh Function based Bandstop Filter

The proposed parallel bandstop filter is shown in Fig. 4.6 where the antenna port is modeled as Norton equivalent current source I_{ANT} with parallel 50 Ω resistor R_{ANT}. The receiver provides broadband matching and modeled as input impedance R_L connected in parallel with notch filter. The filter correlates the input voltage V_x with Walsh Functions WF_i by integrating the baseband voltage on inductors. The resultant feedback output current $I_{FILT,BB,i}$ from parallel inductors are summed at node V_x which creates the staircase approximation of the input RF current source. The baseband current on each inductor, $I_{FILT,BB,i}$, can be determined by

$$I_{FILT,BB,i} = \frac{1}{L}\int V_x(t) WF_i(t) dt \tag{4.9}$$

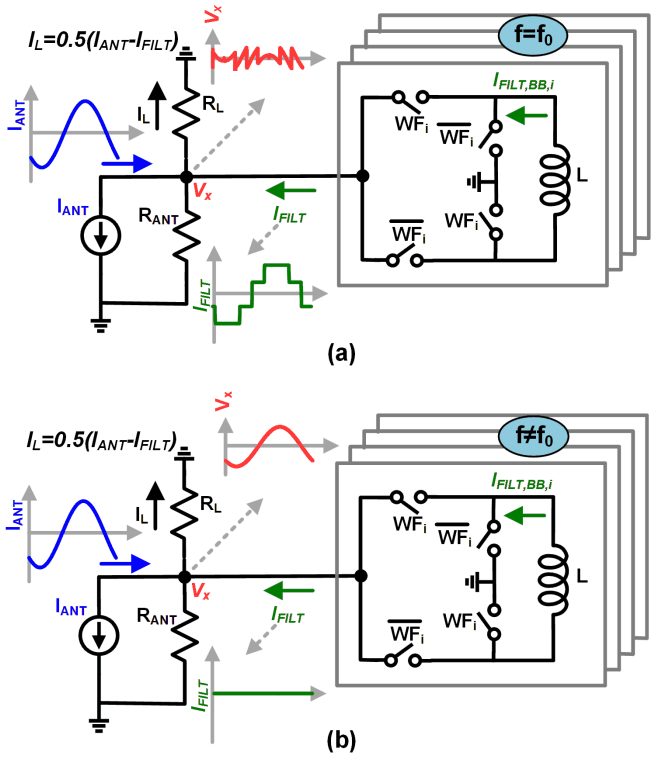


Figure 4.6: Proposed notch filter using Walsh function sequence mixing and impedance translation of passive mixers.

Assuming WF-seq and input signal has same periodicity $T_0 = \frac{1}{f_0}$ (Fig. 4.6(a)), the non-zero baseband current is upconverted to RF input by the passive mixer resulting in small residual leakage current into the load. However, if the input signal frequency and WF-seq are different (Fig. 4.6(b)), the correlation leads to zero baseband current and the filter has no impact at input signal frequency which lead to bandstop behavior. Notably, increasing the number of correlators leads to smaller residual current and hence provide higher attenuation to interferer signal at $f_s = f_0$.

4.2.3.1 2^{nd}order WF-seq based Bandstop Filter:

As discussed in Appendix C, the baseband currents for 2^{nd}order WF-seq can be computed as,

$$I_{BB,sal}(\omega_{IF}) = -\frac{2}{\pi}\frac{R_{ANT}||R_L}{j\omega_{IF}L + R_{ANT}||R_L}Asin(\phi) \tag{4.10}$$

$$I_{BB,cal}(\omega_{IF}) = \frac{2}{\pi}\frac{R_{ANT}||R_L}{j\omega_{IF}L + R_{ANT}||R_L}Acos(\phi) \tag{4.11}$$

and the impedance seen by incident signal from antenna at RF is,

$$Z_{IN} = (R_{ANT}||R_L)|| \left(R_{ser,h} + \frac{j\omega_{IF}L}{\alpha}\right) \tag{4.12}$$

where $\alpha = 8/\pi^2$ and $R_{ser,h} = \frac{(1-\alpha)}{\alpha}(R_{ANT}||R_L)$. As shown in Fig. 4.7, the equivalent RF model at the input can capture the impact of the residual current using a series resistance, $R_{ser,h}$, which is also identical to the harmonic shunt resistance used in NOP

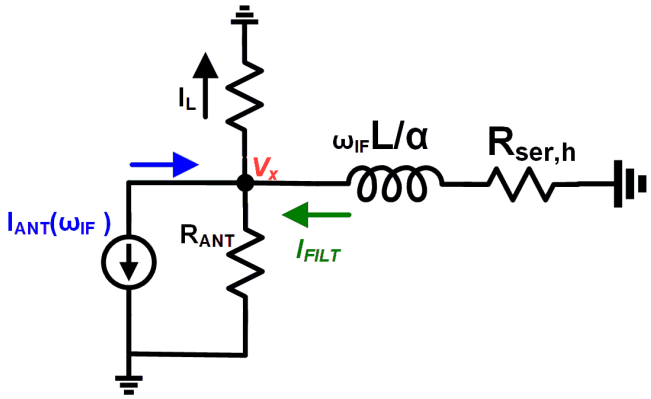


Figure 4.7: Baseband equivalent circuit of notch filter including effect of harmonic down and up conversion.

N-path filter models [93, 94]. Note that similar to 4-phase NOP bandstop filters, 2^{nd}order WF-seq filter leads to harmonic notches.

4.2.3.2 3^{rd}order WF-seq based Bandstop Filter:

Compared to a 2^{nd}order WF-seq correlator, the 3^{rd}order correlator has two additional correlators that correlate with $sal(3)$ and $cal(3)$. The baseband currents in these correlators can be computed from (C.5) (shown in Appendix C),

$$I_{BB,sal(3)}(\omega_{IF}) = -\frac{2(\sqrt{2}-1)}{\pi}\frac{R_a}{j\omega_{IF}L+R_a}Asin(\phi) \tag{4.13}$$

$$I_{BB,cal(3)}(\omega_{IF}) = \frac{2(\sqrt{2}-1)}{\pi}\frac{R_a}{j\omega_{IF}L+R_a}Acos(\phi) \tag{4.14}$$

where $\alpha = 16(2-\sqrt{2})/\pi^2$ with the same model shown in Fig. 4.7. Using additional

correlators, the 3^{rd}order provides better filtering for interferers compared to 2^{nd}order notch filter due to smaller $R_{ser,h}$. For instance, with antenna port impedance R_{ANT} =50 Ω and receiver input impedance R_L =50 Ω, $R_{ser,h}$ is 5.84 Ω and 1.32 Ω for 2^{nd}order and 3^{rd}order WF-seq filters respectively.

The operation of the WF-seq bandstop filter can also be viewed as the impedance translation provided by passive mixers, which translate the high-pass inductor transfer function to RF, creating a bandstop response at LO frequency. The parallel WF-seq and inductor based filter correlates voltage and returns current, unlike the capacitor-based N-path filters that correlate current and store baseband voltage. Voltage correlation implies that the WF-seq bandstop filter is insensitive to overlap between the signals driving parallel bandstop filters. Therefore, multiple WF-seq correlators can be placed in parallel without incurring any penalty except through additional switch parasitics. The insensitivity to overlap implies that the filters can reconfigured. For example, a 3^{rd}order correlator with WF-seq with frequency f_0 can be reconfigured as two 2^{nd}order correlators with WF-seq with frequencies f_0 and f_1, resulting in concurrent bandstop performance at two different frequencies as shown in Fig. 4.8.

Further, the N-path filter [94] have unwanted bandstop filtering at every harmonic frequencies whereas in WF-seq based filter the bandstop notches occurs only at odd harmonics frequencies due to the correlation of incident signals at even harmonics with the used WF-seq ($sal(1)$, $cal(1)$, $sal(3)$ and $cal(3)$) is zero.

The baseband inductor can be replaced by an active gyrator as shown in Fig. 4.9 if on-chip integration is desired. The effective baseband inductance of the gyrator is given

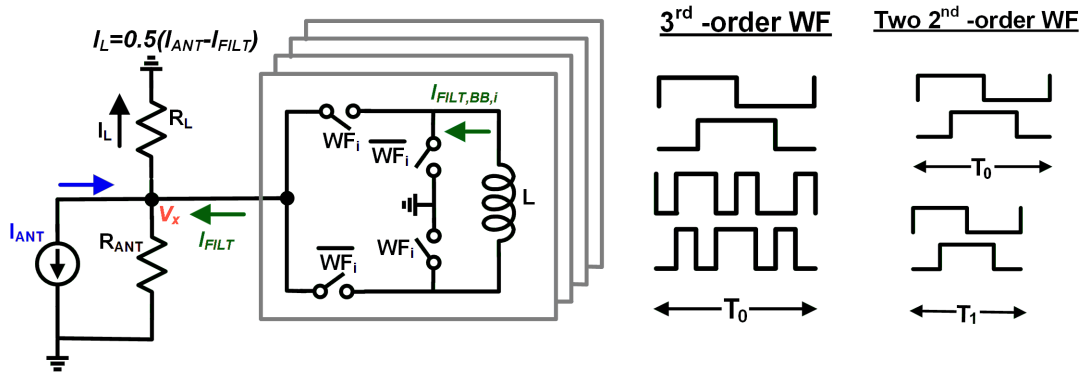


Figure 4.8: Filter can be reconfigurable by changing WF-seq from the single frequency 3^{rd}order filter to the dual frequency 2^{nd}order filter.

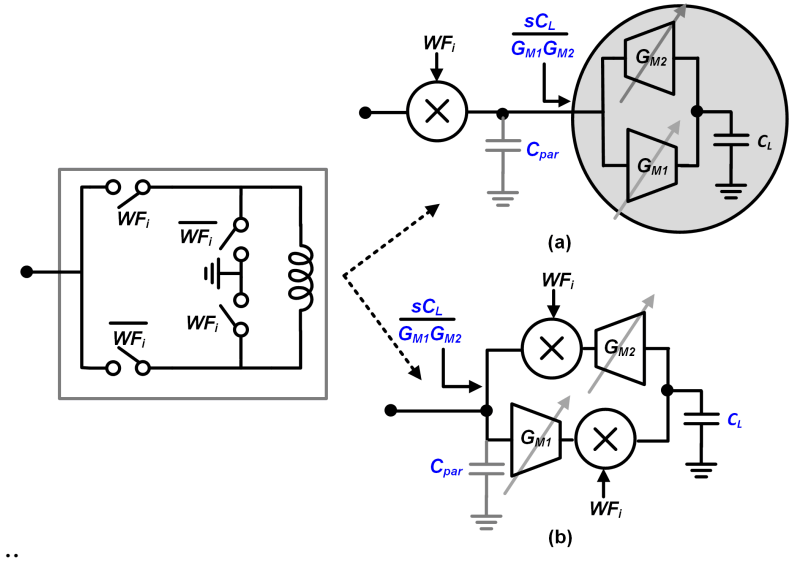


Figure 4.9: Active gyrator based inductor implementation to save off-chip inductor.

by,

$$L_{eff} = \frac{C}{G_{M1}G_{M2}} \tag{4.15}$$

While the gyrator enables integration, the transconductances G_{M1} and G_{M2} introduce noise and non-linearity. Gyrator linearity will be discussed in the context of the implementation in Section 4.3. The out-of-stopband noise is dominated by G_{M2} noise and its contribution referred to input of the bandstop filter which is given by,

$$\overline{V_{n,GM2}^2} = 4KT\gamma G_{M2}(R_L||R_{ANT})^2 \tag{4.16}$$

Assuming the antenna port and receiver impedance of 50 Ω, the noise figure (NF) degradation due to the active gyrator based notch filter is,

$$NF = 1 + \gamma G_{M2} R_{ANT} \tag{4.17}$$

4.3 Dual frequency Bandstop Filter using WF-Seq in 65 nm CMOS

The proposed bandstop filter is implemented in a commercial 65 nm CMOS technology with 9 metal layers option as shown in Fig. 4.10. An active gyrator approach is used for the baseband inductors to achieve high levels of integration. In the gyrator, large transistors are used to reduce flicker noise of G_{M1}. However, the resulting parasitic capacitance at the input increases insertion loss, since the input capacitor is charged and discharged in every RF cycle. Therefore, the gyrator implementation in Fig. 4.9(b) is

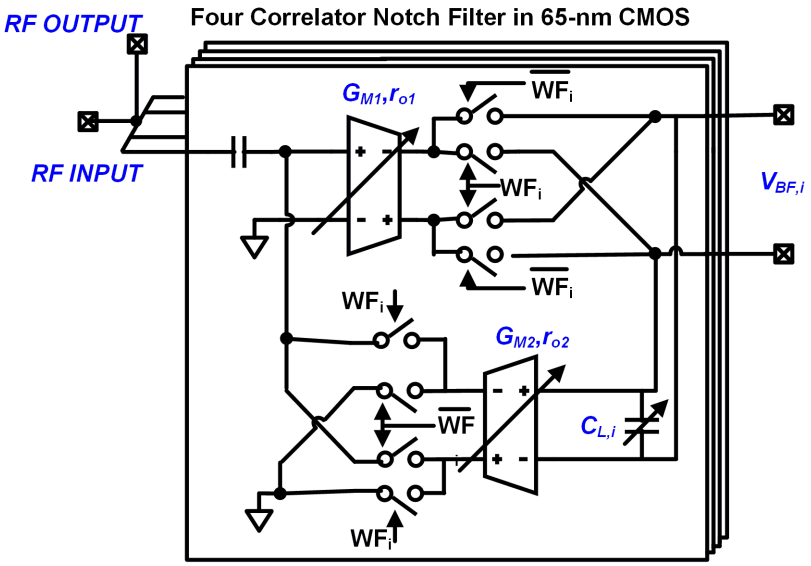


Figure 4.10: Schematic of bandstop filter.

used with G_{M1} implemented at RF and two sets of mixer switches to accomplish the impedance translation.

As described in Section 4.2, the proposed approach leads to a small voltage swing at the RF in the stopband. However, G_{M2} cell must source/sink a current whose magnitude is equal to the RF interferer current. Therefore, the output linearity of G_{M2} limits the overall performance. In this design, 20 dB interference cancellation is achieved with a bias current of 23 mA from supply voltage of 1.8 V to ensure RF cancellation for an -10 dBm input signal. The G_{M1}, G_{M2} and capacitors $C_{L,i}$ are programmable to meet the bandwidth, noise figure, linearity and power consumption specification of the notch filter.

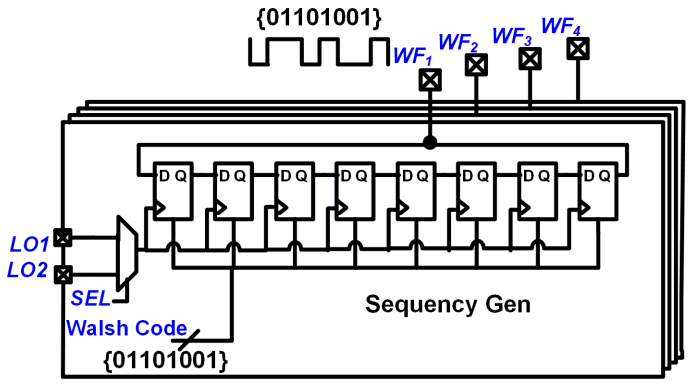


Figure 4.11: A shift register based WF-seq generator output can be programmed by using SPI interface.

4.3.1 WF-seq Generation:

Although the WF-seq can be generated using logical operations on NOP signals or multi-clock phases, a shift-register based approach is adopted for design simplicity in this work. As shown in Fig. 4.11, the shift registers can be programmed with a targeted sequence. Dual-edge flipflops are used to implement shift registers which can work with both the rising and the falling edge of the clock. Thus, an external LO at four-times the signal frequency is used to implement eight phases. Notably, the bandstop filter downconverts and upconverts the RF signal with the same LO. Therefore, the phase noise of the LO signal does not impact performance assuming small delay between the WF-seq to the two mixers as also reported in [95]. Reconfigurability is supported by enabling independent LO to each pair of correlators. Therefore, the bandstop filter can either be configured as a 3^{rd}order bandstop WF-seq at f_1 or as two independent 2^{nd}order WF-seq bandstop filters at f_1 and f_2. Operation frequencies are limited by the insertion loss of the filter and by the used shift register for WF-seq approach.

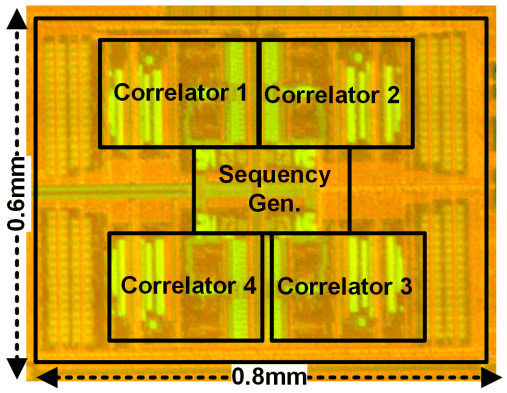


Figure 4.12: Die photograph of the notch filter.

4.4 Measured Performance

The die photo of the implemented filter is shown in Fig. 4.12 occupying 0.48 mm^2 area. The baseband capacitance is made programmable and can be varied from 0.1 pF to 16 pF per correlator while occupying 0.1 mm^2 for four correlators. A gain-boosted N-path receiver [104] is also included to demonstrate the feasibility of the proposed approach to build receivers with LO-defined receive frequency as well as bandstop frequency. Fig. 4.13 illustrates the measurement setup used for s-parameter, noise and linearity measurements. Small signal measurements are carried out using Keysight E4448A specturm analyzer Linearity is measured using four signal sources to generate two external LOs and input signals. A laptop interface is used to program the scan chain using serial interface.

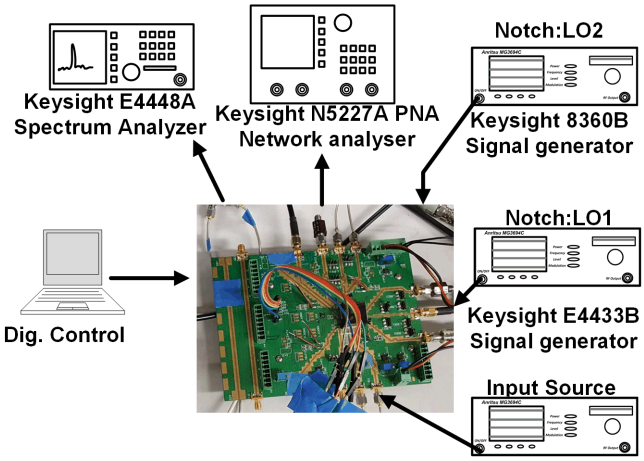


Figure 4.13: Test setup for characterizing the notch filter.

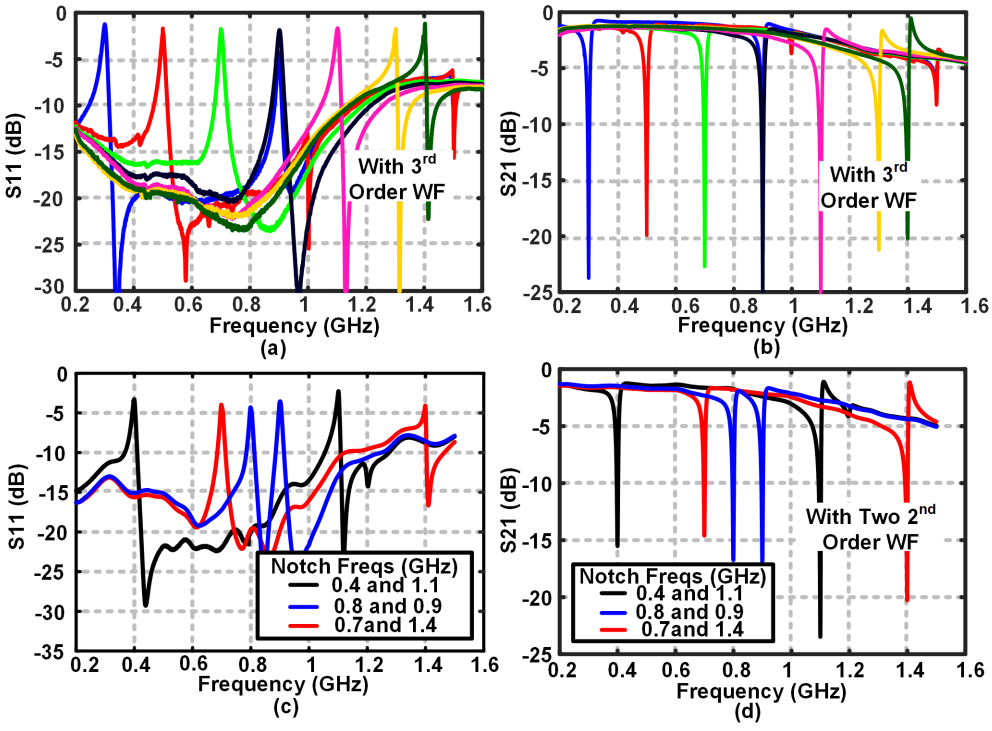


Figure 4.14: Measured s-parameters of filter with 3^{rd}order WF-seq targeting notch at one frequency and 2^{nd}order WF-seq targeting notch at two different frequencies.

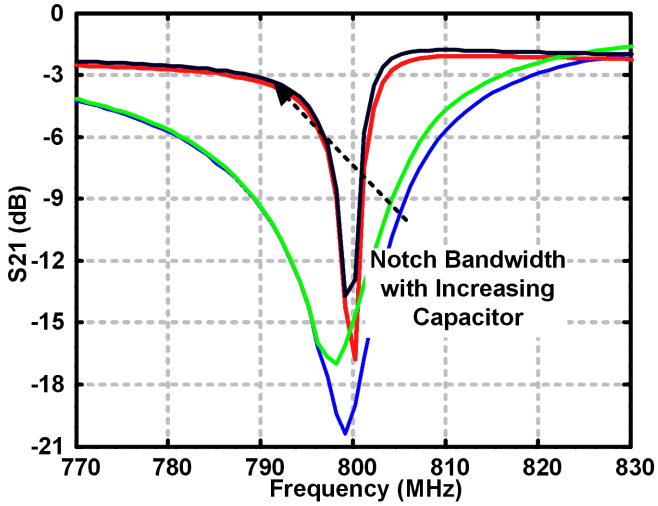


Figure 4.15: Bandwidth of filter are programmable by changing capacitors.

4.4.1 Small Signal Measurements

The measured s-parameters of the filter configured as 3^{rd}order WF-seq at a single frequency are shown in Fig. 4.14(a,b). As shown in Fig. 4.14(b), the input $S21$ shows a frequency tunable bandstop filtering with stopband frequency defined by the period of the WF-seq that demonstrates attenuation of 20 dB from 3^{rd}order notch filter. Parasitic capacitor shown in Fig. 4.9(b) causes $\sim$2 dB insertion loss and is limited by 65 nm CMOS technology. Corresponding $S11$ measurements are shown in Fig. 4.14a demonstrating the reflective impedance at RF input at the stopband frequency. The four-correlator filter can be reconfigured as two 2^{nd}order WF-seq with two different periods operating in parallel. Fig. 4.14(c,d) shows measured s-parameters of the filter configured as dual frequency bandstop filter which is tunable independently from 0.3 GHz to 1.4 GHz.

The stopband bandwidth is determined by baseband $C_{L,i}$, G_{M1} and G_{M2}. Fig. 4.15

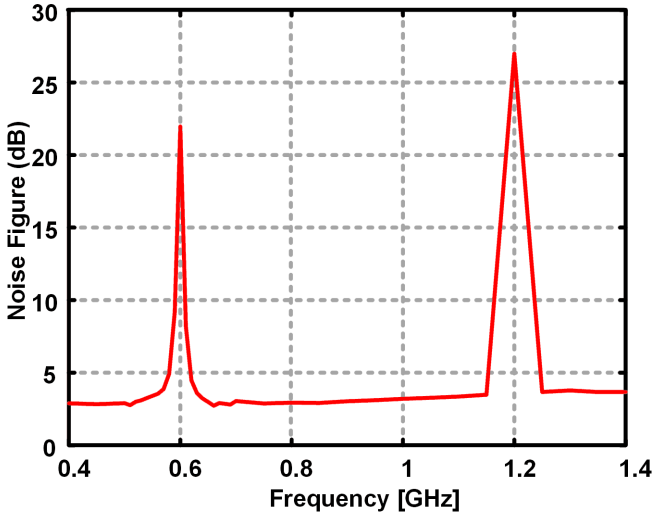


Figure 4.16: Noise figure of stand-alone notch filter operating as 3^{rd}order filter at 600 MHz.

shows measured bandwidth across different capacitor settings demonstrating 10 dB notch bandwidth of $\sim$10 MHz is achievable using this approach.

4.4.2 Noise Figure Measurements

The measured noise figure of standalone notch filter configured as 3^{rd}order WF-seq is shown in Fig. 4.16. It demonstrates out-of-band noise figure of 2.5 dB to 3.5 dB. At frequencies other than notch frequency, the capacitor $C_{L,i}$ act as short and thus, the noise is dominated from G_{M2} transconductor. Lower G_{M2} reduces out-of-band noise contribution but it degrades the filters linearity. At notch frequency, the noise is dominated by G_{M1} and is of lesser concern, since the notch is suppose to attenuate any signal present.

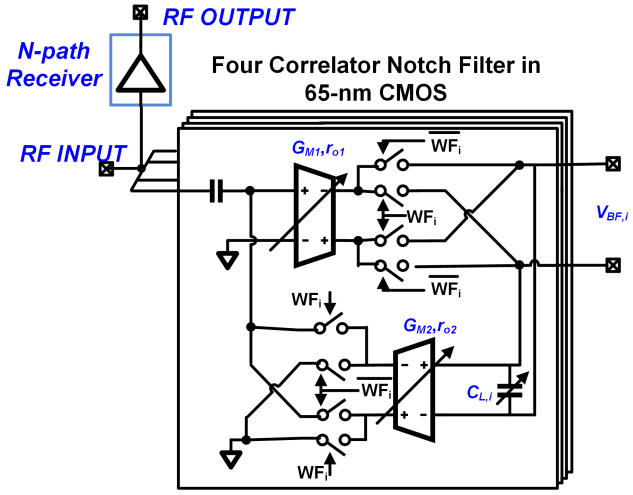


Figure 4.17: A gain-boosted receiver is connected to characterize noise figure degradation due to notch filter.

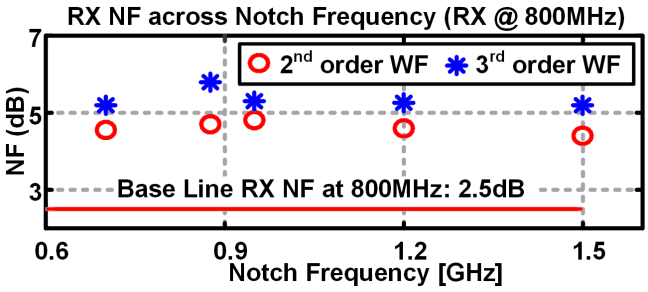


Figure 4.18: Noise figure degradation due to notch filter at receiver output.

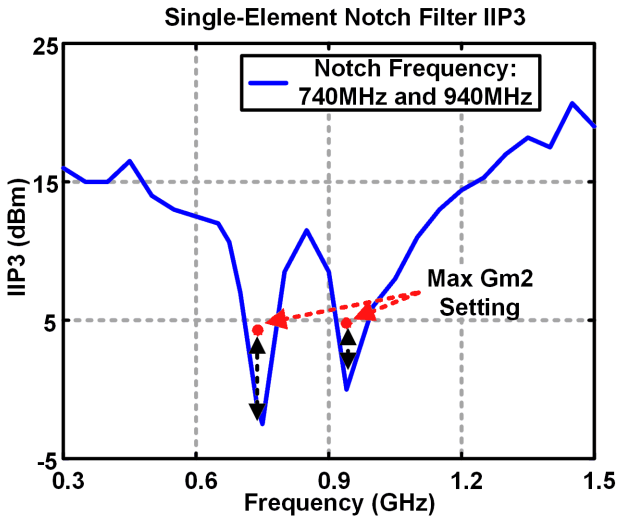


Figure 4.19: Measured IIP3 with filter is configured as dual frequency notch.

Noise figure is also measured at gain boosted receiver output as shown in Fig. 4.17. The gain boosted N-path receiver achieved 2.5 dB noise figure with 43 dB gain in standalone measurement. Fig. 4.18 shows measured noise figure degradation is between 2.5 dB to 3 dB when the filter is configured in dual frequency 2^{nd}order and 3^{rd}order filter.

4.4.3 Linearity Measurements

Linearity of notch filter is strongly dependent on the current canceling capability of G_{M2}. For instance, to cancel 0 dBm blocker, filter need to have atleast 12 mA current driving capability. Hence, G_{M2} cell is made programmable and it achieved a measured IIP3 of -2.5 to $+5$ dBm (Fig. 4.19) in dual frequency notch filter operating at 740 MHz and 940 MHz.

4.4.4 LO leakage to RF port

The spurious LO power leakage to antenna port is a concern in N-path receivers [105, 96] where emission occurs at harmonically related frequencies. The spurious leakage may desensitize nearby receivers operating in the same band. Measured LO spur leakage when notch filter is enabled and disabled while operating at 500 MHz and 700 MHz is shown in Fig. 4.20 and is measured below -60 dBm. When the filter is disabled, spurs of ~ -57 dBm at 4 times the notch frequency (which is provided to the IC) are present at the output due to coupling through traces on board and bondwire.

4.5 Extension to Bandpass Filter using WF-Seq

The bandpass filter can be designed from the notch filter by using duality principle in electrical network. The inductors are replaced with capacitors, parallel filters are replaced by series and Norton equivalent of port (Fig. 4.6) are replaced by Thevinin equivalent in bandpass filter. Fig 4.21 shows the 3^{rd}order bandpass filter based on WF-seq implementation. Similar to N-path filter, the incident RF current is multiplied by the WF and integrated on the capacitor and resultant capacitor voltages are summed in series to create staircase approximation of V_{ANT} at filter output V_{FILT}. Similar to Fig. 4.8, the above approach can be extended to design two frequency receiver by using two 2^{nd}order WF.

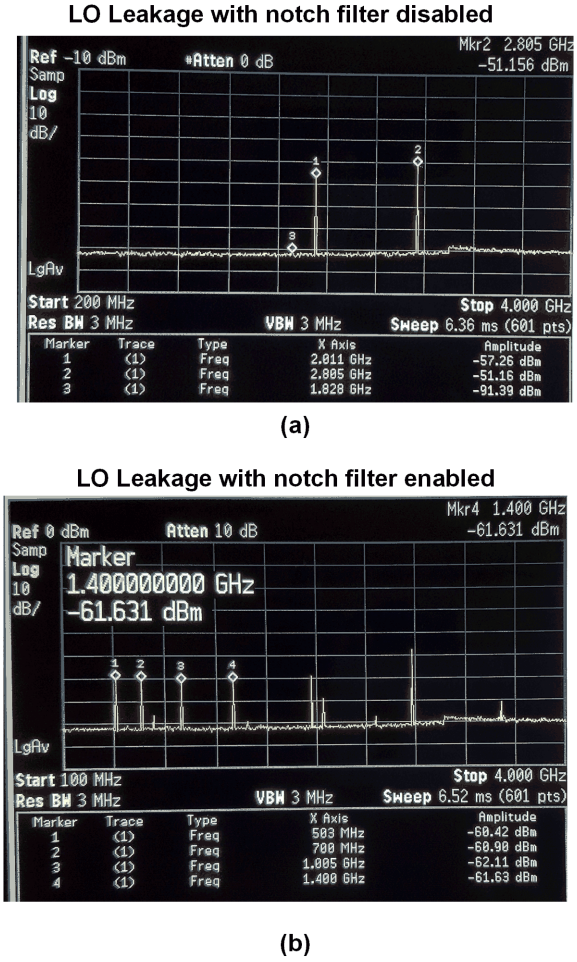


Figure 4.20: Measured LO signals at filter output ports are of the order of ~ -60 dBm.

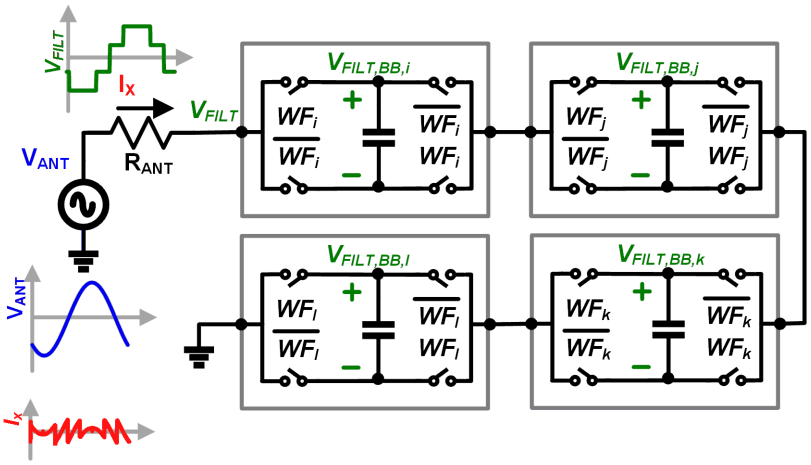


Figure 4.21: Current driven bandpass filter based on WF-seq.

Chapter 5: A Concurrent Dual-Frequency/Angle-of-Incidence Spatio-spectral Notch Filter using Walsh Function Passive Sequence Mixers

5.1 Introduction

Wireless communication systems including IEEE 802.11n (Wi-Fi), IEEE 802.11ac (Wi-Fi), HSPA+ (3G), WiMAX (4G), Long Term Evolution (LTE 4G) standards use multiple-input multiple-output (MIMO) technique[106] to increase the data rate by exploiting the spatial signature of the wireless medium. Recently, large scale massive MIMO systems [58, 59, 4] have drawn a lot of attention in the context of upcoming 5G standard. MIMO employs hundreds of antennas to increase the data rate by thousand times with overall 100x reduced energy consumption [60]. MIMO increases the data rate by aggressively using spatial multiplexing [107] and improves the energy efficiency by focusing the transmitted signal sharply into a very small space. Additionally, spatial diversity is utilized in a MIMO system to reduce the power outage probability. In spatial diversity, the receiver observes several redundant copies of the same signal coming from different paths[108, 109] and hence improves the reliability of the wireless link. However, one of the key challenges faced by a MIMO system is its low resilience to in-band co-channel interferers (CCI).

Spatial beamforming is used to separate CCI from the desired signal. Since both the

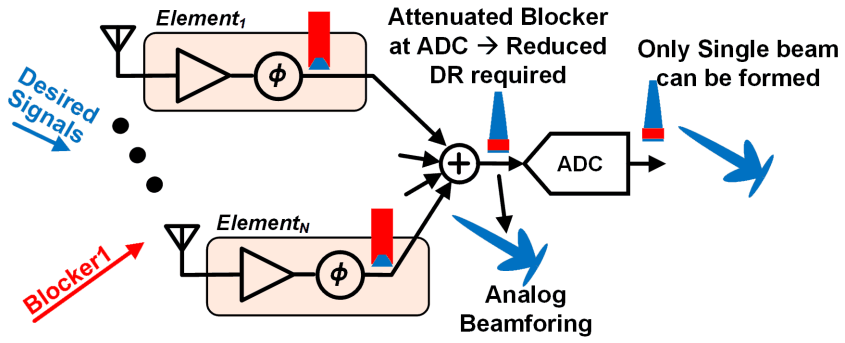


Figure 5.1: ADC linearity specification is relaxed as the CCI is filtered in a linear phased array shown as an analog beamformer.

signal and CCI are very close in frequency, CCI is attenuated by creating spatial nulls in its angle-of-incidence (AoI) while maximizing the gain in the AoI of the desired signal. The resulting array gain due to beamforming improves the signal-to-noise ratio (SNR) for the desired signal by 3 dB for each two-fold increase in array size. Beamforming can be done in the RF/analog domain by employing phased arrays (analog beamforming) or in the digital domain after the signals are quantized by the ADC (digital beamforming).

Many low cost silicon based implementations of analog beamforming have been demonstrated at mm-wave [7, 8, 9, 10, 11, 12, 13, 14] and low GHz frequencies [110, 111, 112] which employ linear phased arrays to add the received analog signal at various antennas with appropriate delays as shown in Fig. 5.1. For a narrow band signal, delays are often approximated by phase and the phase shifters are used to avoid bulky variable delay block. Phase shifting is realized in the RF or LO or IF path. If a desired signal with in-band CCI is present with a different AoI, the interferer gets attenuated due to the array gain while the desired signal gets amplified. This reduces the dynamic range required at the ADC input and results in power savings[113, 114]. Since the phased arrays can only

receive a signal from a single AoI, duplication of hardware is required for simultaneously receiving signals from multiple AoI.

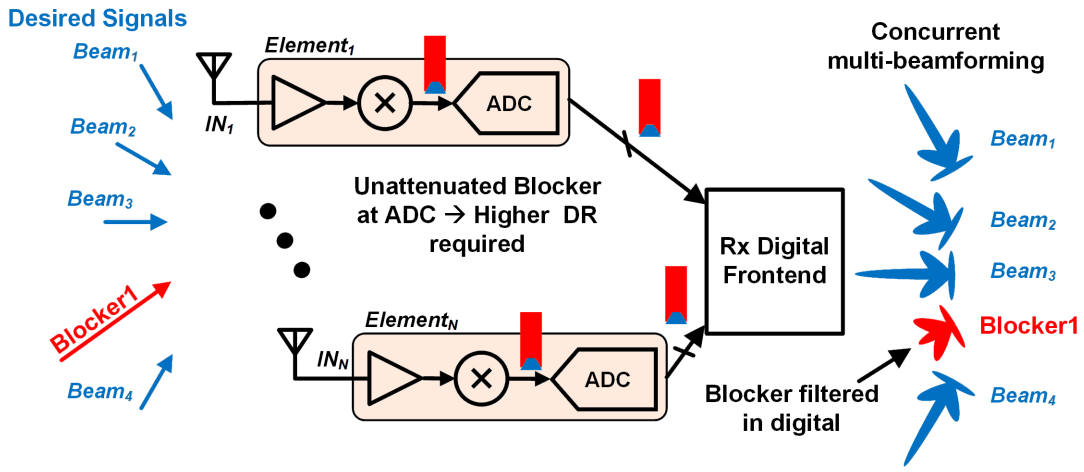


Figure 5.2: MIMO digital beamforming performs spatial filtering at digital baseband while ADC is exposed to unattenuated CCI.

On the other hand, digital beamforming(DBF)[115, 116] (Fig. 5.2) provides a truly MIMO solution with maximum flexibility and in general has a larger digital hardware footprint. It allows simultaneous multi-directional beam formation while supporting single-user MIMO, multi-user MIMO and spatial diversity. Signals received at each antenna pass through the individual receiver chain with ADCs and are processed in the digital domain. Digital signal processing allows formation of more complex spatial filters with programmable spatio nulls that can be placed at any arbitrary interferer AoI. However, as the blocker and desired signal have the same gain, a larger dynamic range is required for the ADC which results in overall increased power consumption [117]. This has led to interest in the development of notched-arrays with spatio-spectral notching of CCI in RF/analog prior to the ADC and DBF.

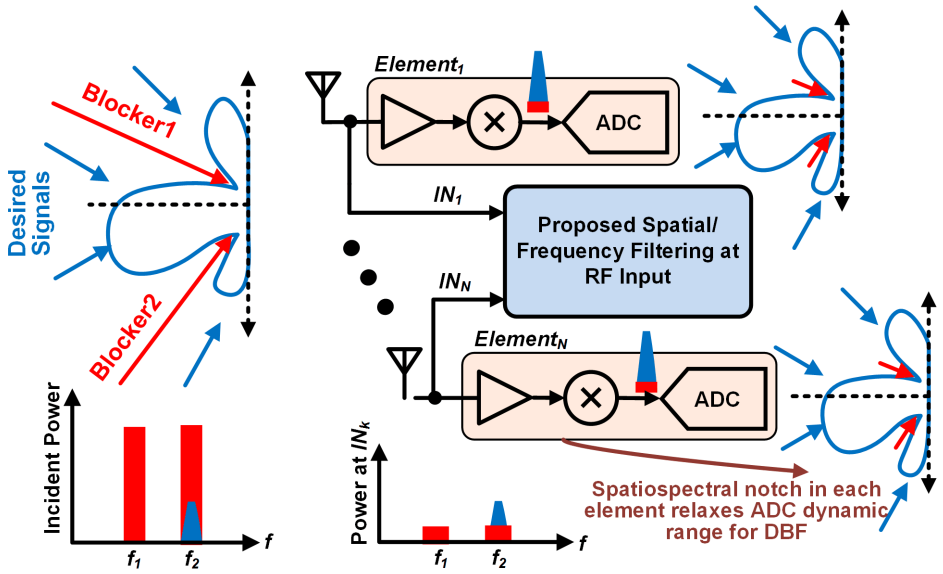


Figure 5.3: Spatio-spectral filtering at RF input to attenuate multiple blockers (both out-of-band and in-band at specific angles of incidence) reduces blocker levels at ADC input enabling subsequent digital beamforming.

Existing spatio-spectral notching approaches include spatio-spectral filtering of one blocker at RF input in an X-band array [118] and spatio-spectral filtering of one blocker using feed-forward cancellation (FFC) at baseband [119]. However, blocker suppression at RF input is critical to address intermod products [120] between blocker and desired signal. In [121, 122], a passive butler matrix based reconfigurable beamforming network inserted at antenna improves linearity is as each receiver along the chain sees signals from only one AoI. However, the butler matrix requires area hungry couplers and has poor noise-figure(NF) due to high insertion loss of the passive components.

In this chapter, spectral notch filter from Chapter 4 is extended to spatial domain. A scalable, reconfigurable RX architecture for parallel spatio-spectral notch filtering (PSNF) [123] is presented in Fig. 5.3 that allows concurrent rejection of two blockers

at each antenna input in a DBF array. It can attenuate two concurrent blockers at a) different frequencies and same AoI, b) same frequency but different AoI and c) arbitrary AoI/frequency. The PSNF can be programmed to create a low impedance for the blocker at the antenna input. Due to impedance mismatch, the blocker gets reflected from antenna. This reduces the dynamic range requirement and saves power consumption in the ADC.

In Section 5.2, a detailed description of the PSNF implementation is presented that uses the orthogonality of Walsh function sequences (WF-seq) [103] and the impedance translation of passive mixers [93] to enable spatial filtering. The measurement results are presented in Section 5.3 confirming $>$20 dB spatio-spectral attenuation at RF input (18 dB higher at RF input than state-of-art [119]) for one frequency/AoI notch and $\sim$15 dB rejection at two independent frequencies/AoI.

5.2 N-path Spatio-spectral Filtering

As discussed in Chapter 4, rejecting multiple frequencies or performing spatial notch filtering using parallel N-path notch filters is infeasible due to capacitor charge sharing when the LO pulses overlap. Additionally, N-path notch filters [95] create a high input impedance at the notch frequency leading to a high blocker voltage swing at the input which might limit the linearity.

Similar to spectral notch filters in Chapter 4, each PSNF element in Fig. 5.4 consists of four correlators that are driven by WF-seq (Fig. 4.8). Each set of switches and baseband gyrator/capacitor in PSNF can be considered to be a correlator that senses the RF voltage and returns a current based on the projection of the RF input voltage on the WF-seq.

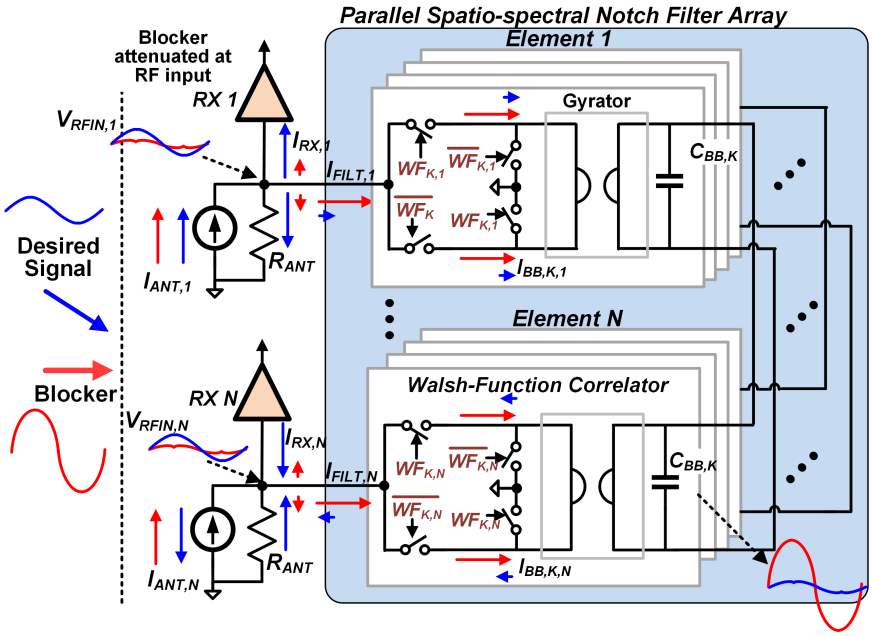


Figure 5.4: Proposed parallel spatio-spectral notch filter (PSNF) array using Walsh function sequence mixing and impedance translation of passive mixers.

Spatio-spectral filtering is achieved by connecting the capacitors corresponding to one set of correlators across each element. For example, if we assume that the WF-seq are in-phase in all elements, a blocker with broadside AoI results in constructive in-phase current addition on $C_{BB,K}$ (in red). The resultant non-zero feedback currents at gyrators output are upconverted as current I_{FILT} which flows through antenna. This causes low RF impedance and blocker notch filtering at input of each element. For the desired signal (in blue) AoI, the current on each baseband capacitor $C_{BB,K}$ cancels out due to the out-of-phase summation, producing smaller voltage swing across the capacitor which results in negligible feedback RF current I_{FILT} flow through the antenna. Thus, the PSNF filter provides higher impedance to the desired signal which is unaffected at each

element. The AoI corresponding to the notch can be steered to different spatial direction by changing the relative phase of the WF-seq applied to correlators in each element.

Importantly, since the correlators in the PSNF correlate input voltage and return current, this approach is not affected by overlap between WF-seq across correlators. The PSNFs insensitivity to overlap between basis functions allows arbitrary WF-seq to be applied at each correlator. For instance, if single-frequency/AoI 3^{rd}order WF-seq (Fig. 4.8) are applied to the four correlators in each array element, a single frequency/AoI notch filter is created which is equivalent to 8-phase NOP filter. On the other hand, a concurrent dual-frequency/AoI notch can be achieved by applying two 2^{nd}order WF-seq at two independent frequencies (Fig. 4.8) to the four correlators in each element. Additionally, in this approach, the baseband capacitors in the gyrators also capture the blocker signal for subsequent FFC.

The CMOS implementation of 4-element 4-correlator notch filter is shown in Fig. 5.5. A gain-boosted N-path receiver [104] is included in one of the element to demonstrate the improvement in the reception of the desired signal in the presence of CCI. The PSNF filter uses WF-seq based LO generation and is discussed in detail in Section 4.3. The relative coarse phase shift of 3 bits across array is achieved by changing the relative phases of the WF-seq in shift registers corresponding to different elements. This architecture also supports the traditional LO-path phase shifting for higher phase resolution.

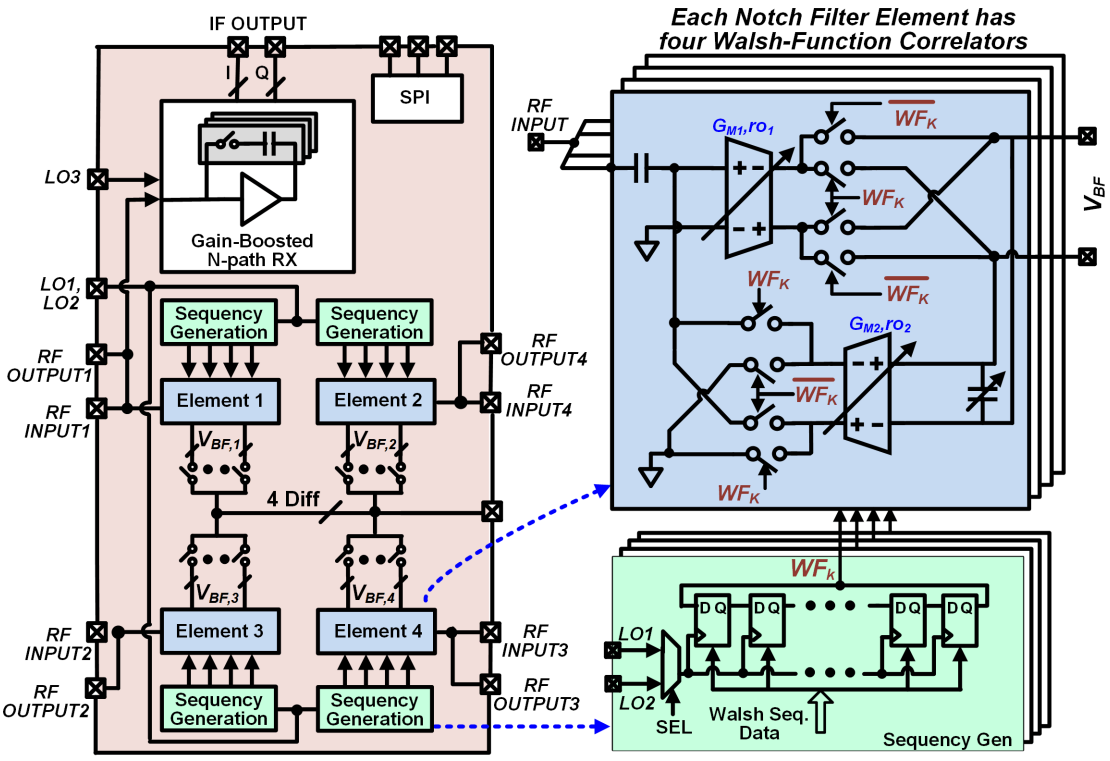


Figure 5.5: Schematic of 65 nm CMOS implementation of four-element PSNF with four correlators in each element operating from 0.3 GHz to 1.4 GHz.

5.3 Measured Performance

The 4-element PSNF is implemented in 9-metal layers 65 nm CMOS with 3.4 μm ultra thick top metal layer option and the die photo is shown in Fig. 5.6. The core element area is 0.48 mm^2. Notably, the IC has extensive programmability in baseband gyrators/capacitors (Fig. 5.5) which increases the die area. The notch filter operates from 0.3 to 1.4 GHz frequency range and consuming overall 170 mW power from 1.8 V supply. The clock generation circuit consumes 16.5 mA per element current from 1.2 V supply while operating as two frequency 2^{nd}order notch filter.

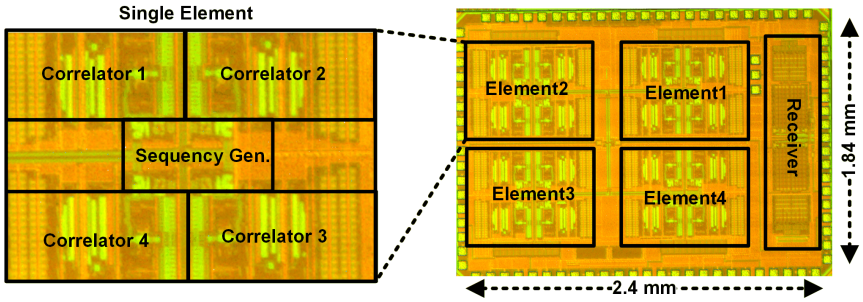


Figure 5.6: Die photo of 4-element PSNF in 65 nm CMOS technology.

5.3.1 Small Signal Measurements

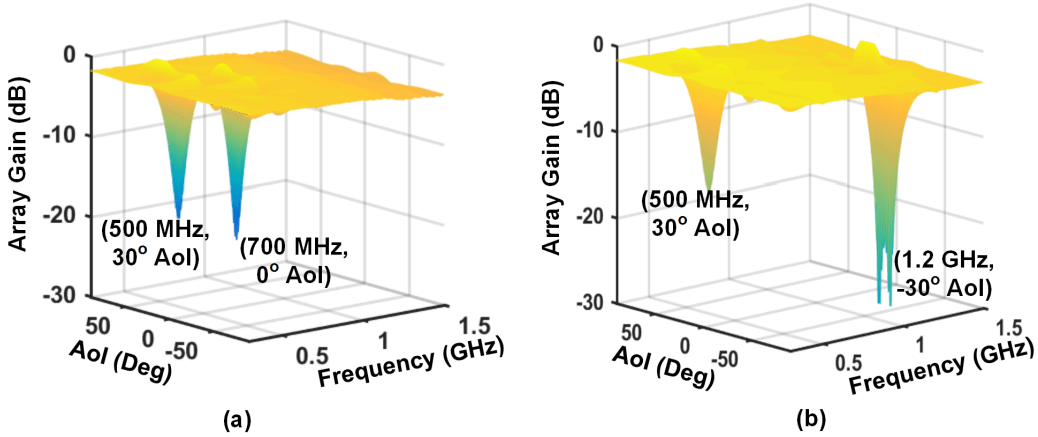


Figure 5.7: Measured array gain for 4-element array for two settings demonstrating concurrent dual frequency/AoI notch filtering

The small signal spatio-spectral filter are measured by using Keysight N5227A PNA Network analyser. Two port s-parameter measurement is carried out between each input and output of 4-element notch filter while terminating all other inputs and outputs with 50 Ω resistor. Subsequently, 3D plot of array gain across AoI and Frequency sweep is obtained from ADS testbench [124] using measured s-paramters at each RF

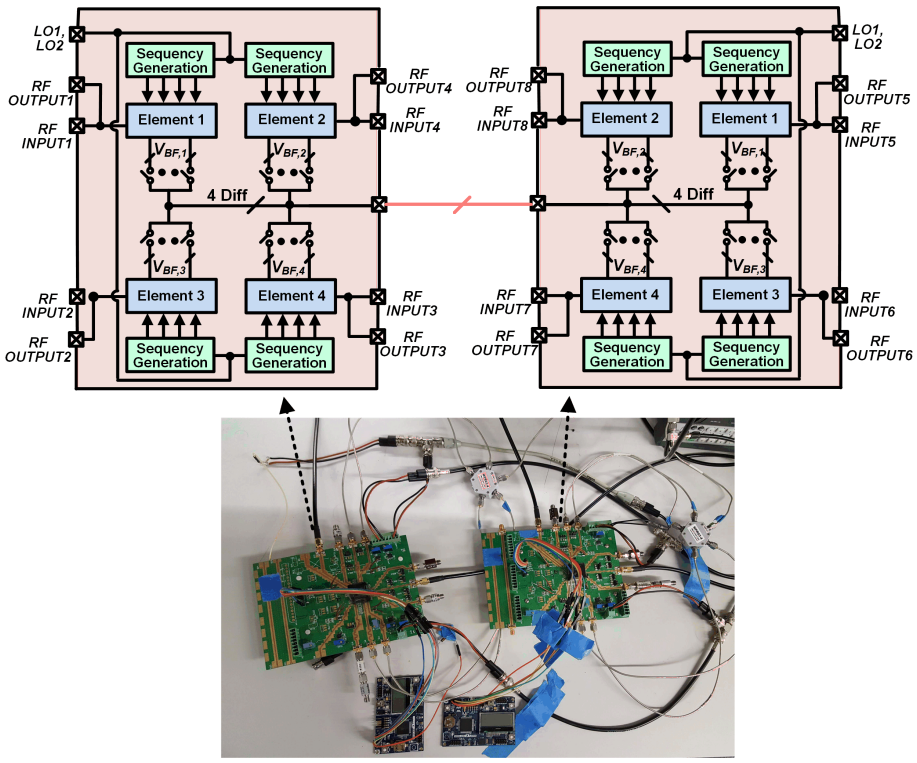


Figure 5.8: Measurement setup with two four-element parallel spatial notch filter array demonstrating scalability to 8 elements by connecting baseband capacitors.

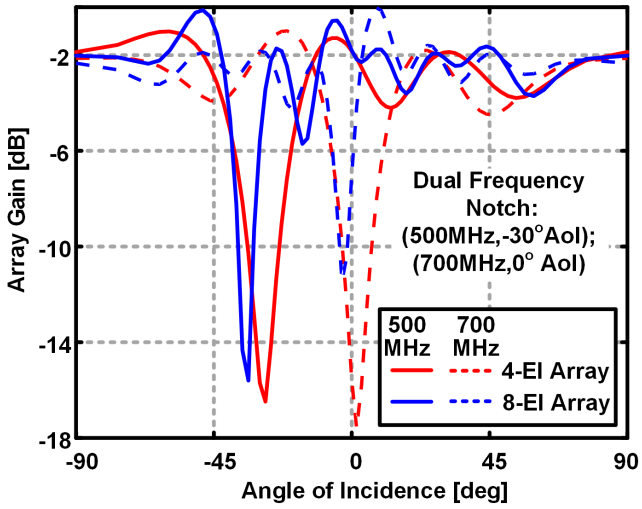


Figure 5.9: 8-element 2^{nd}order WF-seq demonstrating scalable MIMO spatio-spectral filtering

outputs of the filter as shown in Fig. 5.7. It demonstrates concurrent dual-frequency/AoI spatio-spectral notch filtering of more than 14 dB attenuation to spatial/spectral blockers, thereby reducing the dynamic range requirement for the subsequent baseband ADC in the receiver chain.

More often higher element spatio notch filter is desired to achieve much sharper spatial filtering. Scalability of this approach is verified by forming 8-element PSNF array by connecting the baseband nodes of two 4-element notch filters on PCB as shown in Fig. 5.8. The LOs are shared between the ICs and phase shift is achieved by varying the phases of LO in each elements. Measurement result (Fig. 5.9) demonstrates that 8-element notch filter achieves improved spatial resolution compare to 4-element one while creating concurrent dual spatio-spectral notch filter at RF input in DBF arrays.

5.3.2 Linearity Measurements

Two-tone linearity measurements is carried out by exciting the array by uniform phased-shifted input signal. A gain-boosted N-path RX is connected to element 1 in Fig. 5.5 to verify improvement in receiver linearity. The measured gain of the receiver (G_{Rx}) is $\sim$42 dB and noise figure of 2.5 dB to 3.9 dB. The output referred in-band OIP3 can be expressed as

$$OIP3 = IIP3 + G_{Rx} \tag{5.1}$$

and is characterized by measuring the input referred IIP3 of the receiver across AoI of input signal while the PSNF is configured for dual-frequency (500 MHz and 800 MHz)/AoI(0^o) spatio-spectral filter. Fig. 5.10(a) shows the measured in-band OIP3 of the receiver is 28 dBm in the configured notch direction and is improved by 15 dB compared to all other AoI. The above improvement in linearity is expected as the filter attenuates blocker by $\sim$15 dB when configured as dual frequency/AoI notch filter.

The extent of blocker cancellation depends on the available output current from gyrator and thus it trades with power consumption of the gyrator. Both G_{M1} and G_{M2} transconductances are varied and linearity is measured. G_{M1} is varied by changing the bias current of the transconductance stage and G_{M2} is varied by turning ON/OFF the parallel transconductance cells. Measurement (Fig. 5.10(b)) confirms the trade-off between in-band OIP3 and power consumption and it depends mostly on the power consumption in G_{M2} stage.

The blocker 1 dB gain compression of the receiver is measured for desired signal in presence of the blocker signals at 701 MHz and 811 MHz frequencies with AoI of 0^o and

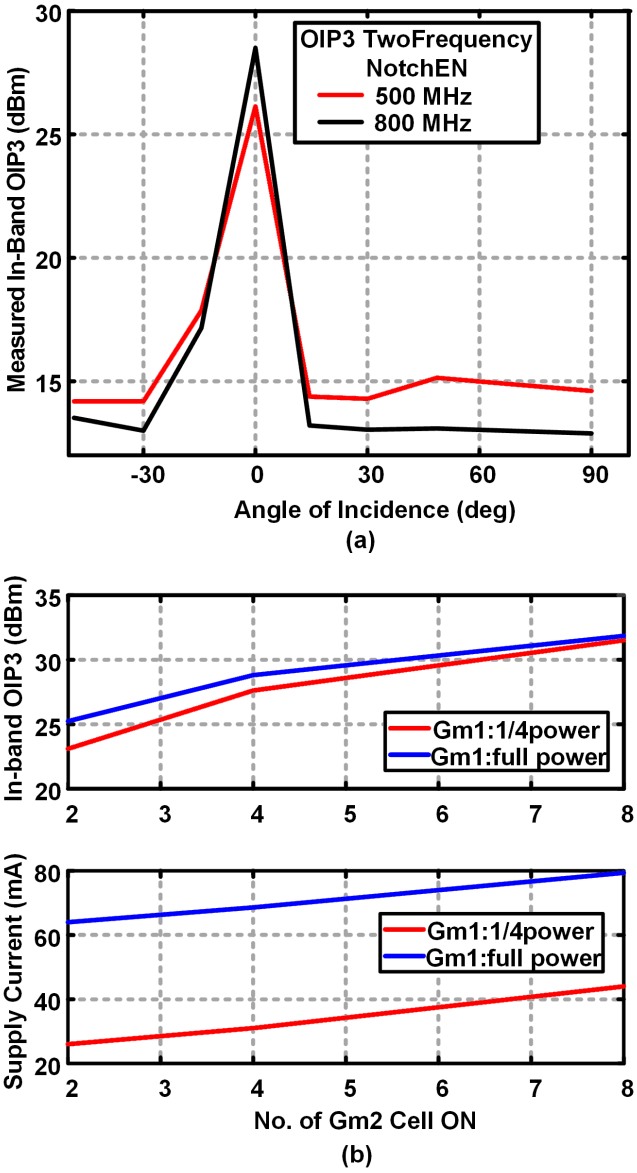


Figure 5.10: (a) In-band OIP3 of the receiver and (b) its trade-off with power consumption.

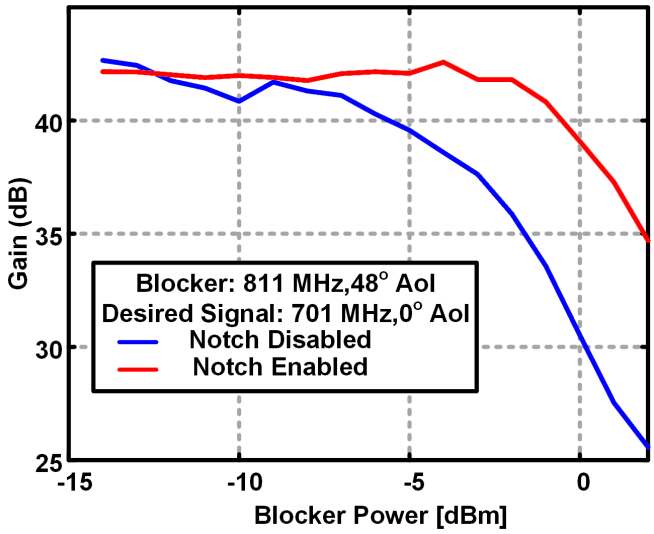


Figure 5.11: Blocker 1-dB gain Compression of the receiver.

48^o respectively. As the blocker power is increased (Fig. 5.11), in the presence of PSNF the 1 dB gain compression of the receiver is improved.

5.3.3 Simulated Noise Figure

As discussed in Chapter 4, noise at the notch frequency is dominated by G_{M1} and at other frequencies it is dominated by G_{M2}. This is because at other frequencies the baseband capacitor $C_{L,i}$ is a short (Fig. 4.10). Similarly, for the spatio-spectral notch filter, the noise from G_{M1} is the dominant source in the notch direction as shown in Fig. 5.12. Since noise current from the G_{M1} in each element is summed on common baseband capacitors (Fig. 5.4) and they beamform in the notch direction. G_{M2} noise degrades the receiver noise figure is in all other directions as shown in Fig. 5.12. Simulated noise figure of notch filter configured as 3^{rd}order WF-seq for 0^o AoI notch direction is shown

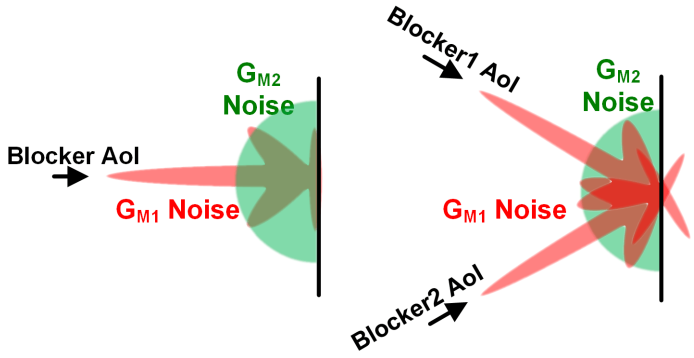


Figure 5.12: (a) Noise of Notch filter configured as single and dual AoI notch filter. Noise due to the G_{M1} is in notch direction while noise due to the G_{M2} degrades noise figure of the MIMO receiver in all direction.

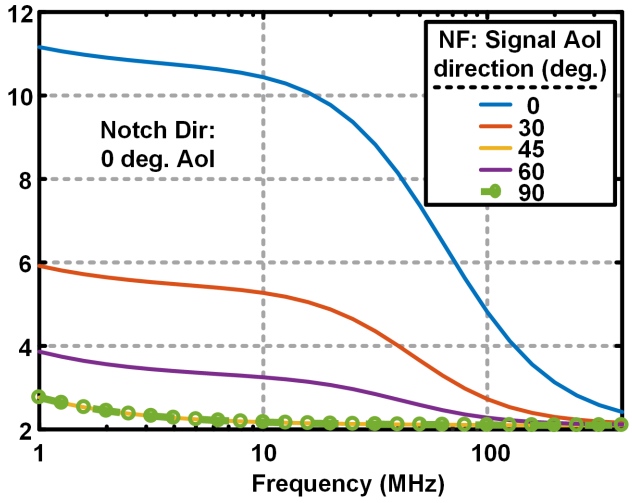


Figure 5.13: Simulated noise figure as a function of spatial angle. Notch filter is configured as 3^{rd}order WF-seq in 0^o direction.

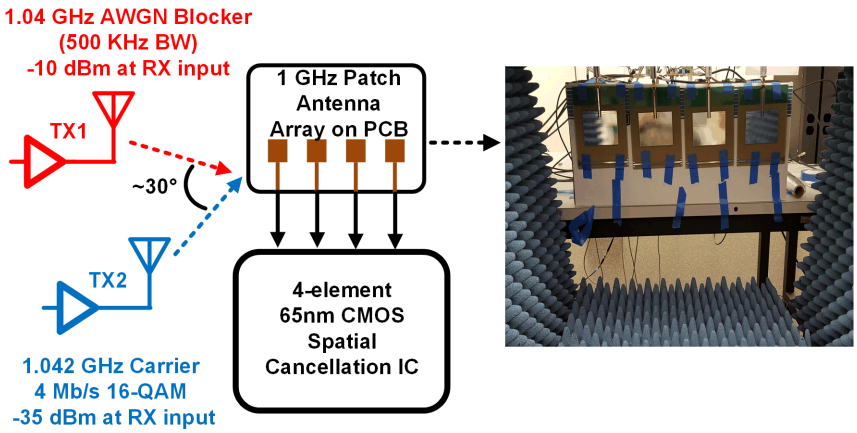


Figure 5.14: Wireless setup (patch antennas connected to packaged IC) with in-band -10 dBm AWGN blocker at RF input.

in Fig. 5.13, confirms that noise from G_{M1} dominates in notch direction and is less of concern for a MIMO system. However, G_{M2} noise degrades the noise figure of receiver and can be reduced by reducing G_{M2} which can be reduced by reducing the current thereby trading off with maximum blocker current that can be notched out at antenna.

5.3.4 Wireless Measurements

A wireless measurement (Fig. 5.14) was carried out with a -10 dBm in-band AWGN blocker and a -35 dBm 16-QAM modulated desired signal incident at the receiver antenna array. A uniformly spaced patch antenna array was designed on standard FR-4 boards with half wavelength spacing between arrays at 1.04 GHz frequency. The constellation before and after the spatial blocker filtering as shown in Fig. 5.15 demonstrates the efficacy of the proposed notch filtering approach. The performance summary of the PSNF is shown in Table 5.1.

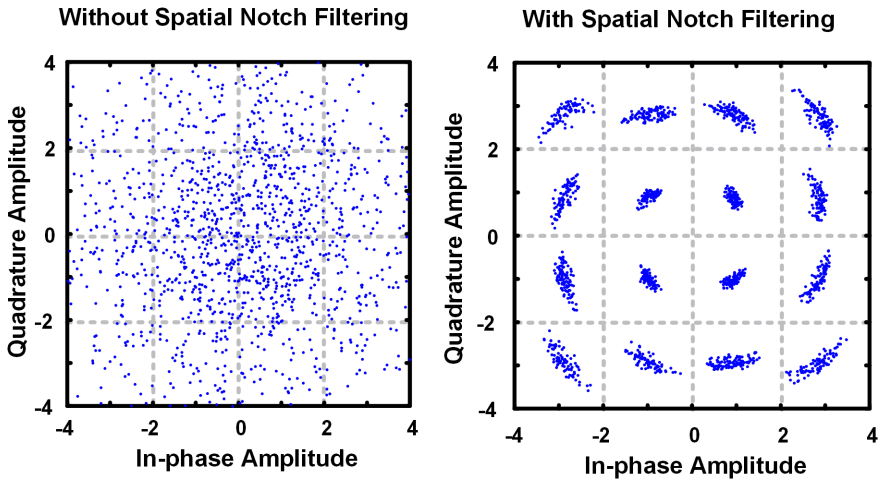


Figure 5.15: Measured constellation without and with notch filtering.

Table 5.1: Performance summary of 4-element spatio-spectral notch filter

Power Consumption	Notch Filter:170 mW, Seq Gen: 80 mW (4-elements) RX: 30 mW/element (1.2 V and 1.8 V supplies)
No. of Inputs/Outputs	4/4
Frequency (GHz)	0.3-1.4
Spatio-spectral Notch	2 independent Freq/AoI Notches
Spatial Notching	25/20 dB at RF input (3^{rd}order WF/2^{nd}order WF)
Eqvt. 1-element NF	2.5-3.9 dB (PSNF off); 5.3-7.5 dB (PSNF enables)
In-band OIP3 (dBm)	26, 28.5 (Two Frequency Notch), 32 (Max Gm2 power)

Chapter 6: A N-path Mixer-based Code-Domain Receiver with Transmitter Self-Interference Rejection

6.1 Introduction

Spread spectrum communication using code modulated receivers are commonplace in both military and consumer electronics. In spread spectrum [125, 106], the signal can be hidden below the thermal noise floor of the medium while providing resistance to the jammer and low probability of interception. Typical commercial applications includes CDMA IS-95, IS-2000, WCDMA mobile telecommunication, WLAN (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g), Bluetooth and GPS. It features enhanced safety, security and ability to withstand the threat of attacker to jam any critical military mission.

In signal processing theory, the matched filters are known to be optimal linear filter with remarkable interferer rejection property in the presence of additive white Gaussian random noise. Matched filter, in spread spectrum, is designed by correlating the desired code with the received signal in digital domain while taking advantage of implementation flexibility in deep sub-micron silicon technologies. Such system can achieve optimal performance if the signals are passed through ideal LNA, mixer and ADC. However, power of the jammer is often so high that the receiver can suffer from limited linearity and saturated RF/analog frontend unless the jammer is rejected earlier in the receiver chain.

This chapter extends the correlator concept presented in the context of WF-seq in Chapter 4 to an N-path mixer based code domain receiver that implements matched filter in RF for spread spectrum system. It uses correlation of the received code-modulated signal with the receiver code to extract information while rejecting in-band self-interference generated from its own transmitter or interferer at the RF frontend. In both military and consumer applications [126, 127], this will enable filtering/cancellation of interference for simultaneous transmit and receive (STAR) applications. Since the interferers are rejected at receiver frontend, the proposed approach relaxes the dynamic range required by both RF blocks and ADC and hence promises better performance compared to digital-filter only implementation. Additionally, the receiver features concurrent dual code reception which could be used to receive two different signals or to implement a RAKE receiver.

Here is the outline of the current chapter. Section 6.2 presents the background and system level requirements for code modulated receiver in the presence of in-band jammer. Section 6.3 extends N-path mixer architecture to code domain. In Section 6.3.4 schematic implementation is presented followed by measurements in Section 6.4.

6.2 In-band Interferer in Code Modulated Receiver

The performance of today's wireless system is limited by interferers generated by various users accessing the same wireless medium simultaneously at same or different frequency bands. The desired signal strength is often too low compared to interferer at receiver input and requires analog filters to attenuate interferer linearly in order to process signal in digital domain. Traditionally, frequency selective filters have been

employed in receiver to remove out-of-band interferer. As discussed in chapter 4, N-path based receiver has demonstrated high linearity and tunable SAW-less reception while rejecting out-of-band blocker. However, the frequency selective filters are ineffective for the in-band blockers as both interferer and the desired signal occupy same frequency band.

The in-band interferer could be categorized into a) self-interferer (SI) generated by its own transmitter and b) externally generated unknown interferer. Self-interference is a key challenge faced in the full duplex (FD) or frequency domain duplex (FDD) system as the receiver has to reject its own transmitted signal. On the other hand, unknown in-band spatial interferers are suppressed in a MIMO system using spatial filters by exploiting spatial signature of the interferer AoI. The spatio-spectral notch filter has already been discussed for MIMO receivers in Chapter 5. The unknown blocker is also attenuated in a CDMA receiver using spreading codes to leverage correlation and processing gain.

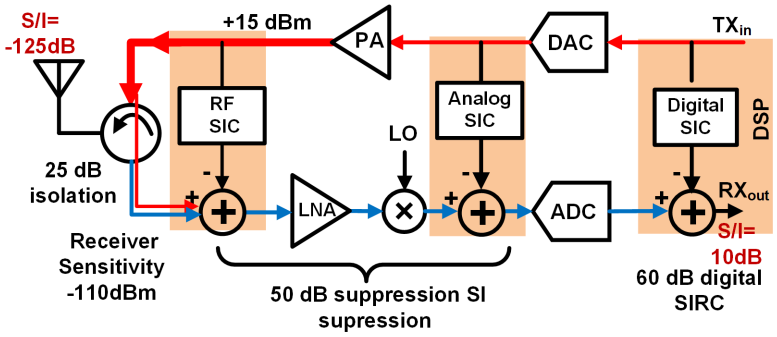


Figure 6.1: SIC distribution in full-duplex system.

Recently, FD system has drawn a lot of attention[128, 129, 130, 131, 132, 133] as it uses same frequency to do both transmission and reception while improving the spectral efficiency of wireless system. These transceivers use self-interference cancellation (SIC)

to suppress SI as the transmitted signal is known at the receiver. Assuming -110 dBm receiver sensitivity, 15 dBm SI leakage from the transmitter and 25 dB isolation between transmitter and receiver port of circulator (Fig. 6.1) in a FD system, more than 110 dB SI cancellation (SIC) is required in both analog and digital domain for interference level to be 10 dB below noise floor at the receiver output. Importantly, SIC must be applied earlier in the receiver chain to enable gain for the desired signal without the in-band SI saturating the receiver. However, SIC suffers from noise figure degradation, area power penalty and limited cancellation linearity [129]. Additionally, SIC is only effective for jammers known prior to the receiver but fails for any unknown in-band interferer.

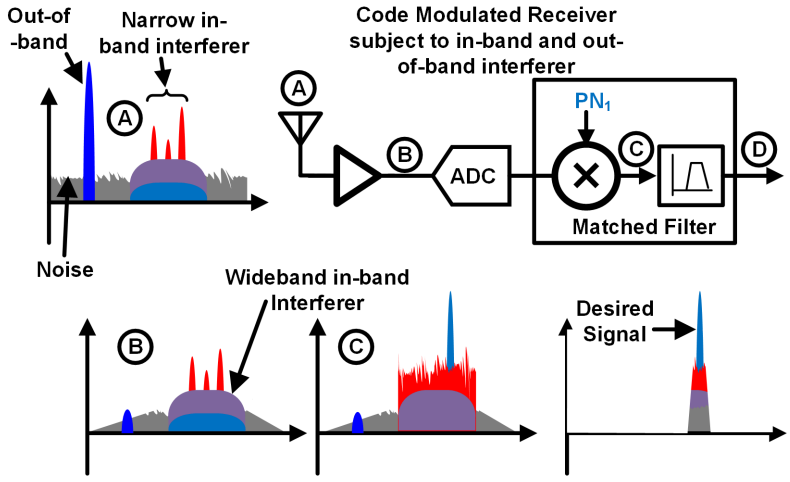


Figure 6.2: Interferer and the desired signal strength as it passes through a code modulated spread spectrum system.

Code modulated receiver can suppress the unknown in-band blocker due to processing gain of code as shown in Fig. 6.2 while reducing the bandwidth of the desired signal by a realted ratio. Out-of band blockers at offset frequencies gets filtered out by RF frontend of the receiver. The desired signal in such system is a wideband spread signal.

Multiplication by despreading code PN_1 in the RX results in a desired narrow band signal. However, the effect of despreading code on the unknown narrow in-band interferer (at node C in Fig. 6.2) is that the power get distributed over the bandwidth of PN_1 code and is subsequently filtered out (node D in Fig. 6.2). Thus, the narrow in-band interferer gets attenuated by processing gain of the code compared to desired signal. However, in the digital implementation, if the interferer signal strength is high enough, the analog frontend will be jammed, saturating the receiver with resulting non-linearity limits processing gain in digital domain. Further, the bandwidth of wideband interferer and thermal noise are unaffected by despreading code and attenuated by the processing gain of code at the lowpass filter output of the receiver.

Commercial CDMA system addresses the SI and known in-band jammer by defining communication standards that uses time division duplex (TDD) or frequency division duplex (FDD) along with power control loops that limits the power of interferer. However, it fails when the unknown jammer is originated from a different standard in an uncontrolled manner. Additionally, to enable STAR operation in spread spectrum system, the transmitted signal is a wideband jammer to the receiver which requires SI rejection/cancellation (SIRC) of $\sim$120 dB for SI to be 10 dB below the noise floor.

In this chapter, a correlator based solution is proposed to attenuate the SI by more than 50 dB at RF frontend by using orthogonal codes [134]. The proposed architecture of the transceiver is shown in Fig. 6.3. A correlator based interferer rejection is advantageous compared to SIC as it can suppress both in-band and out-of-band jammer without degrading the receiver sensitivity while maintaining STAR operation. A specific pair of codes are used in transmitter and receiver ($PN_{WF,1}$ and $PN_{WF,2}$ in Fig. 6.3). At the

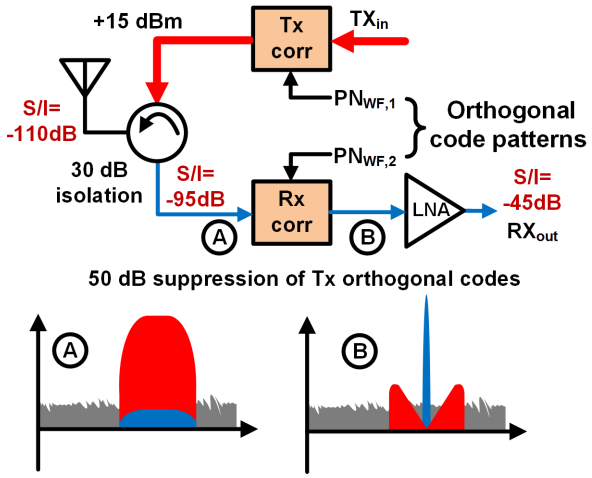


Figure 6.3: SIC in proposed code domain receiver using pseudo random orthogonal codes at transmitter and receiver.

output of correlator in receiver, SI spreading using $PN_{WF,1}$ is de-spreaded with $PN_{WF,2}$ that ideally produces zero at desired signal frequency and can be filtered out using frequency selective filters. Additionally, the correlator attenuates any unknown in-band jammer before the LNA by processing gain and relaxes the dynamic range required for receiver chain. A detailed implementation of N-path based code-modulated receiver is presented in the next section which extends the correlator concepts from Chapter 4 to code domain receivers.

6.3 Code domain N-path Mixer based Receiver

6.3.1 Correlation based Receiver:

The N-path passive mixer driven by non-overlapping LO pulses φ_K is shown in Fig. 6.4. As discussed in Section 4.2, the switch and baseband filter correlate input RF

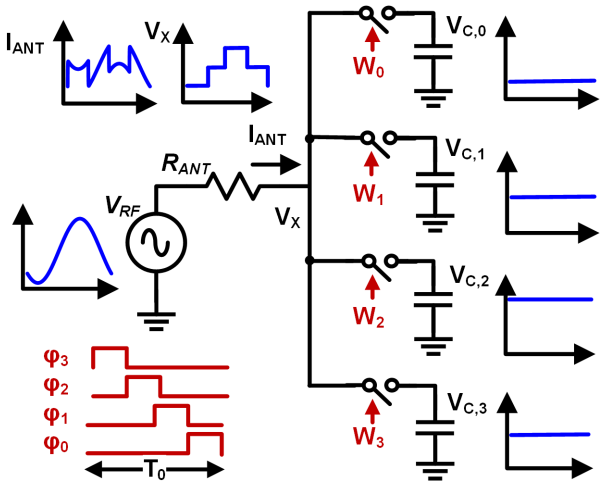


Figure 6.4: N-path mixer based receiver with non-overlapping pulse LO.

current with the LO signal. The baseband voltage, $V_{C,k}\,(t)$ is given by,

$$V_{C,K}\,(t) = \frac{1}{R_A C}\int \left(V_{RF} - \sum_{J=0}^{J=3} V_{C,J} W_J \right) W_K dt \tag{6.1}$$

where $W_J = \varphi_K$; $R_A = R_{ANT} + R_{SW}$, antenna and switch resistance are given by R_{ANT} and R_{SW} respectively. The LO pulses used to drive switches of the mixer are mutually orthogonal basis function. The resultant voltage developed across the baseband capacitor is projection of input signal on these orthogonal basis function. Charge sharing [93] between the baseband capacitors is avoided by using non-overlapping LO pulses. Also, charge sharing occurs if two N-path filters are placed in parallel to receive two different frequencies concurrently and thus making the parallel filter placement infeasible.

Assuming a code modulated desired signal $V_{RF}(t)$ with symbol rate, B_R that is spreaded using a pseudo noise (PN) code, PN_{R1} with a chip rate, $C_R = 1/T_C$, (code

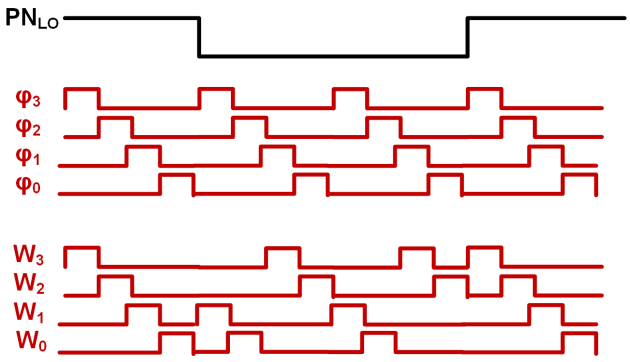


Figure 6.5: LO pulses generation by multiplying pseudo noise code with non-overlapping LO pulses.

length, $M = C_R/B_R$) and translated to center frequency, f_0 is incident to a code modulated N-path receiver. In this case, if the LO signal applied to each switch is generated by multiplying the NOP with period, $T_0 = 1/f_0$, with a pseudo-noise sequence, PN_{LO}, then W_K is given by,

$$W_K = \begin{cases} \varphi_K(t) \text{ for } PN_{LO}(t) = 1 \\ \varphi_K(t + \pi/\omega_0) \text{ for } PN_{LO}(t) = -1 \end{cases} \tag{6.2}$$

As shown in Fig. 6.5, W_K is multiplication of NOP pulses with PN_{LO} and is used to demodulate the code modulated received signal. Thus, the baseband output signal is given by,

$$V_{C,K}(t) = \frac{1}{R_A C} \int \left(V_{RF} PN_{R1} - \sum_{J=0}^{J=3} V_{C,J} W_J \right) W_K dt \tag{6.3}$$

and $V_{C,K}(t)$ depends upon cross-correlation between PN_{LO} and PN_{R1}. Assuming

$PN_{LO} = PN_{R1}$ and perfect synchronization between the PN codes, (6.3) reduces to (6.1) and despreading of the desired signal occurs at baseband capacitors. However, for low cross-correlation between codes PN_{LO} and PN_{R1}, the signal is rejected and the baseband voltage across capacitor is lower value.

Similar to N-path filter, impedance translation occurs for the code domain N-path passive mixer. For the desired coded signal, the baseband voltage across capacitor is upconverted and observed at V_x (Fig. 6.5) which provides impedance matching at antenna whereas for code mismatch, $V_{C,K}(t)$ is small and provide low impedance at RF.

The PN code family can be selected based on auto-correlation for synchronization and cross-correlation for interferer rejection properties. For the known jammer such as self-interference generated from the transmitter, the orthogonal codes are used that ideally produces zero across baseband capacitors. On the other hand, the unknown jammer are uncorrelated to the desired code and produce smaller voltage across capacitor. In the following, a technique to select pairs of PN sequences is proposed that can provide higher SIRC by leveraging a combination of PN and Walsh sequences.

6.3.2 Walsh Functions/PN Sequences for Self-Interference Cancellation:

Walsh function sequences (WF-seq) are orthogonal sequences well suited for digital synthesis[103]. An example of 3^{rd}order WF-seq is shown in Fig. 6.6. Notably, a PN sequence multiplied by a WF-seq is also a PN sequence. For instance, if we consider two

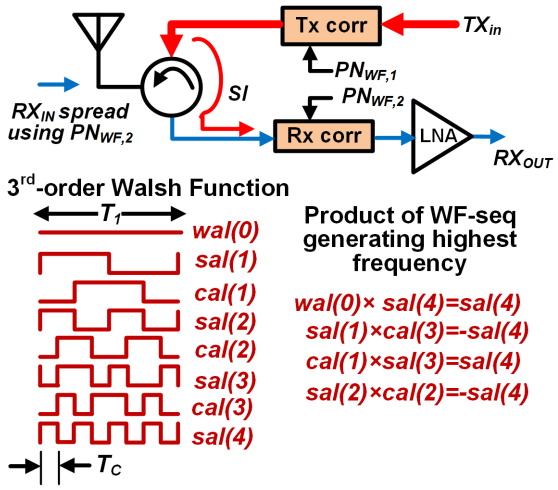


Figure 6.6: 3-rd order Walsh Function sequences (WF-seq)

PN sequences, $PN_{WF,1}$ and $PN_{WF,2}$,

$$PN_{WF,1} = PN_1 \cdot sal(1); PN_{WF,2} = PN_1 \cdot cal(3) \tag{6.4}$$

where $sal(1)$ and $cal(3)$ are shown in Fig. 6.6 and PN_1 is a pseudo-noise sequence with chip rate, $C = 1/T_C$. As shown in Fig. 6.6, $PN_{WF,1}$ and $PN_{WF,2}$ are used as the spreading sequence for the transmitter and the despreading sequence for desired receiver signals respectively. Hence, if W_J applied to the mixers is generated using $PN_{WF,2}$, and assuming that the transmitter is synchronized to the despreading sequence $PN_{WF,2}$, the SI and desired receiver at the baseband output are given by,

$$V_{BB,SI} = V_{TX} \cdot PN_{WF,1}PN_{WF,2} = sal(4) \cdot V_{TX} \tag{6.5}$$

$$V_{BB,RX} = V_{RX} \cdot PN_{WF,2} \cdot PN_{WF,2} = V_{RX} \tag{6.6}$$

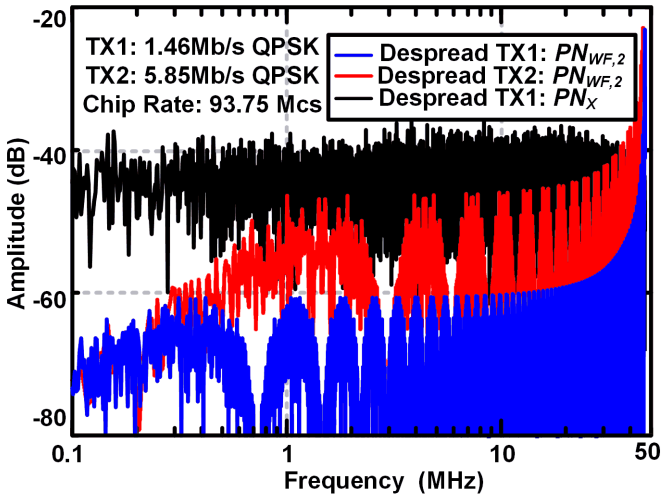


Figure 6.7: SI at N-path receiver output following despreading using PN code and WF-seq/PN code.

From (6.5), SI interaction with receiver despreading code translates SI outside receiver bandwidth, enabling frequency domain filtering in the N-path receiver baseband. While (6.5) was analyzed for one combination of WF-seq, other WF-seq combinations (Fig. 6.6) lead to the same result, with higher order WF-seq providing higher number of pairs.

Fig. 6.7 shows the SI after despreading with code $PN_{WF,2}$ of transmitted signals with a chip rate of 93.75 Mchips/s (Mcs) and spreaded using $PN_{WF,1}$ code for cases: a) 1.46 Mb/s (TX1) and b) 5.85 Mb/s QPSK (TX2). It also compares the improved rejection of SI when orthogonal code $PN_{WF,2}$ is used for spreading compared to the case using completely uncorrelated code PN_X generated using another PN sequence. The SI produced at the receiver output is filtered out as it passes through a lowpass filter with bandwidth 746 KHz. Higher SIRC is achieved when orthogonal code is used compared

to completely uncorrelated code and is 41.7 dB and 17.7 dB for code $PN_{WF,2}$ and PN_X respectively. Additionally, a higher ratio between chip rate and symbol rate produces higher SIRC with 41.7 dBm for TX1 compared to 29.6 dB for TX2 over the integration bandwidth of 5.85 MHz. The synchronization required between the transmitter and receiver spreading codes implies that the transmitter code must be aligned with the desired receiver sequence using pilot signals similar to a CDMA receiver.

6.3.3 Noise Figure Degradation due to Waveform Mismatch:

In a spread spectrum system, the bandwidth of spreaded signals is limited and transmitted chips are shaped using waveform shaping functions such as root-raised cosine, raised cosine etc. In the digital implementation of the matched filters, each chip is passed through matched filter with the impulse response having same waveform shaping function maximizes the signal to noise ratio and any mismatch between the waveform leads to suboptimal SNR at the receiver output [125].

A simplified diagram of the receiver is shown in Fig. 6.8 that consists of an input signal $s(t)$ and the receiving filter with impulse response $g(t)$ in the presence of AWGN channel noise $n(t)$. The energy of a chip with finite duration T can be expressed as

$$\varepsilon_s = \int_0^T s^2(t)dt \tag{6.7}$$

Without loss of generality, if the signal $s(t)$ is normalized to have unit energy, the

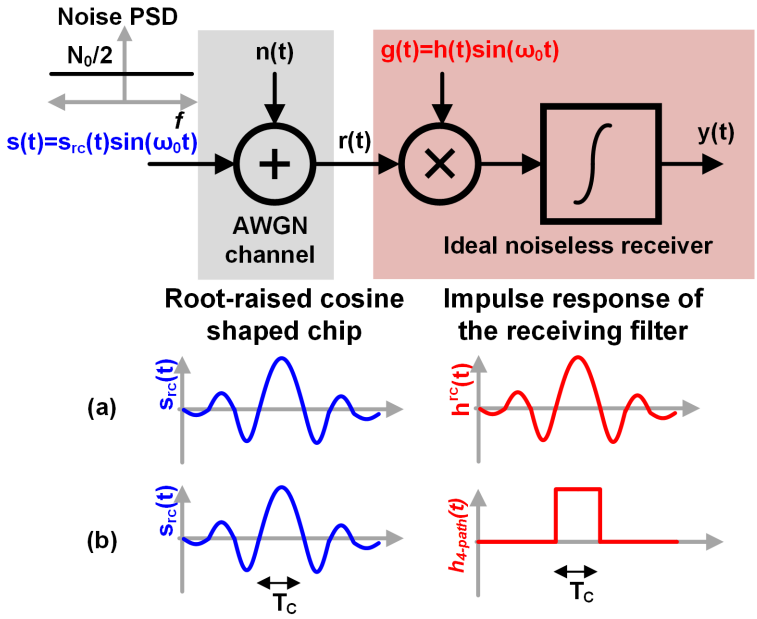


Figure 6.8: Noise figure degradation due to mismatch between waveform shaping of chip and impulse response of receiving filter. (a) Ideal matched filter implementation. (b) Receiving filter that models the code domain N-path Receiver.

SNR of the received signal $y(t)$ at the output of the receiving filter can be calculated as

$$\frac{S}{N} = \frac{2}{N_0} \frac{\left[\int_0^T h(\tau)s(T-\tau)d\tau\right]^2}{\int_0^T h^2(t)dt} = \frac{2}{N_0}\frac{1}{NF} \tag{6.8}$$

where, NF denotes noise figure degradation due to mismatch between the transmitted signal and impulse response of the receiving filter. For instance, when a root-raised cosine shaped input signal (Fig. 6.8(a)) is passed thorough the receiving filter with same impulse response, it forms a matched filter and results in no degradation in noise figure.

However, in the code domain N-path receiver, the impulse response of the receiver filter is a rectangular shaped waveform which degrades the simulated noise figure by

0.9 dB. Additionally, the RF sinusoidal signal is passed through 4-path filter and has theoretical minimum noise figure of 0.9 dB. Thus, the above implementation of code modulated receiver for an input signal with root-raised cosine shaped waveform chips have estimated theoretical noise figure of 1.8 dB compared to a digitally implemented ideal matched filter.

6.3.4 Proposed Code Domain Receiver in 65 nm CMOS

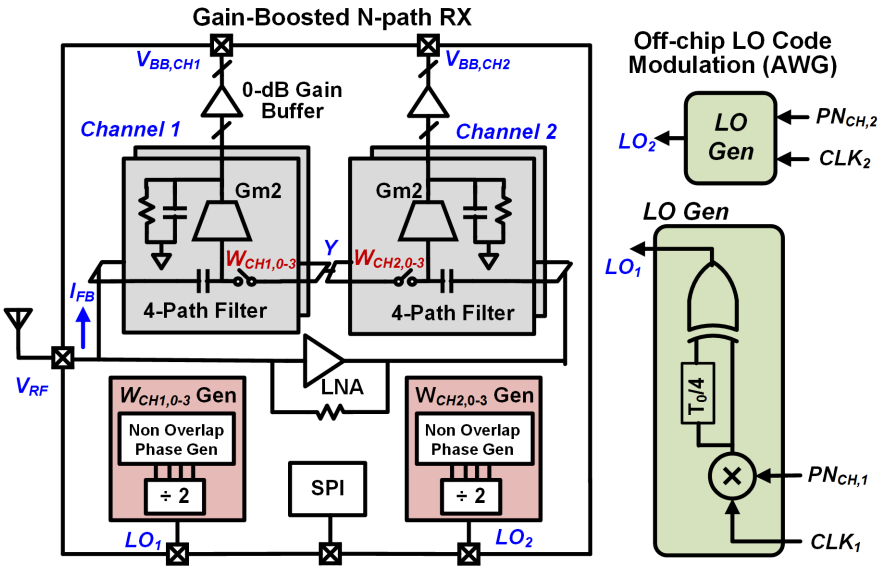


Figure 6.9: Schematic of dual-correlator gain-boosted N-path receiver.

The correlator based receiver is implemented using a gain-boosted N-path receiver [104] as shown in Fig. 6.9. Two correlators (N-path filter) can be placed in series for concurrent reception of two signals as the same RF current I_{FB} in passes through the switches and is available at Y. The correlators in each channel are driven by different

PN sequences, PN_{CH1} and PN_{CH2}. For signals with the code matched to either of despreading codes PN_{CH1} and PN_{CH2} see impedance matching at RF while all other signals are rejected. However, two series correlators in the feedback path increases the effective switch resistance and hence presents trade-offs between noise figure and linearity. Rejection of undesired signals requires equivalent RF current to be sourced by the LNA output. Higher series resistance leads to larger voltage swing at the LNA output, limiting the linearity. Further, increasing the switch size increases the parasitics capacitor that shunt RF current to substrate degrading the high frequency operation.

The receiver achieved $\sim$40 dB gain and the LO frequency can be programmed from 0.3 GHz to 1.4 GHz while having 25 mW power consumption. Two 4-path correlators are implemented in the feedback path followed by a second IF stage and a buffer stage to drive 50 Ω load with 0 dB gain. The bandwidth of the N-path correlators and second IF stages are 5 MHz and 3.4 MHz respectively.

NOP generation is accomplished using on-chip frequency dividers and logic gates. PN code modulated off-chip LO signal is generated (shown in Fig. 6.9) using arbitrary waveform generator in the current work. The chip rate of PN code is 93.75 Mcs and is significantly lower than RF frequency. If on-chip LO code modulation scheme is implemented using digital multipliers, the estimated power consumption of multiplier is $<$ 1 mW from simulation.

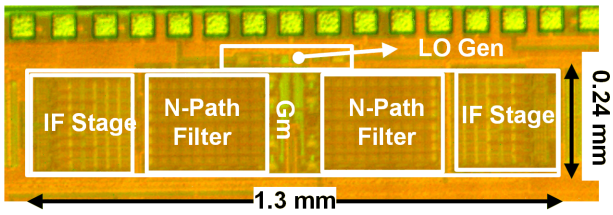


Figure 6.10: Die Photo of 65-nm CMOS N-path receiver.

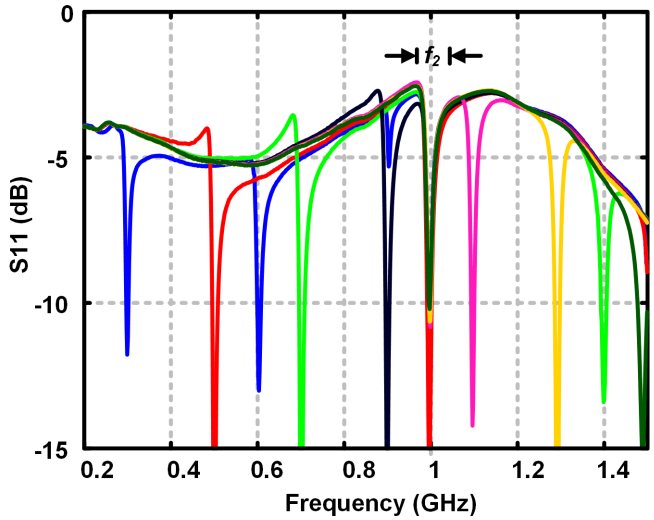


Figure 6.11: Measured S11 with CH2 fixed at 1 GHz while CH1 is varied demonstrating concurrent dual-frequency matching.

6.4 Measured Performance

6.4.1 Small Signal Measurements

The receiver occupies 0.31 mm^2 in a 65 nm CMOS technology as shown in Fig. 6.10. Fig. 6.11 shows the measured S11 when W_{CH1} and W_{CH2} are 4-phase NOP without code modulation at two frequencies, f_1 and f_2. Frequency f_2 is held constant at 1 GHz while f_1 is varied from 300 MHz to 1.4 GHz. While harmonic downconversion in N-path

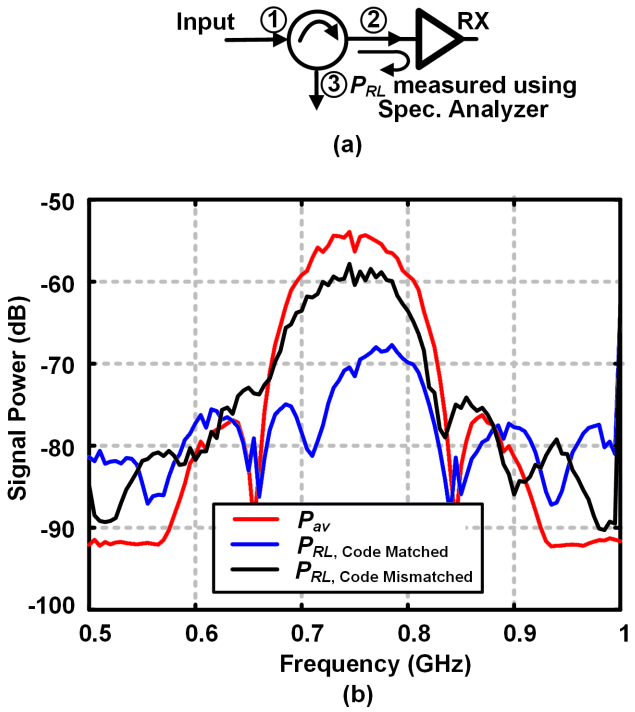


Figure 6.12: (a) Code domain matching measurement setup. (b) Measured available and reflected power for matched and mismatch despreading codes.

mixers precludes harmonic relationship between f_1 and f_2, concurrent LO tunable dual frequency match is observed.

An indirect code domain matching measurement is performed using the circulator based setup as shown in Fig 6.12(a). The measured spectrum of the available power at receiver port 2 is compared to the measured spectrum of the reflected power from the receiver at port 3 when the despreading code in the receiver is same and different from the spreading code for the input signal. A 10 dB higher reflected power at port 3 is measured in Fig 6.12(b) when the codes are mismatched compared to when the codes are matched.

Fig. 6.13 shows the receiver gain and the isolation between the channels CH1 and

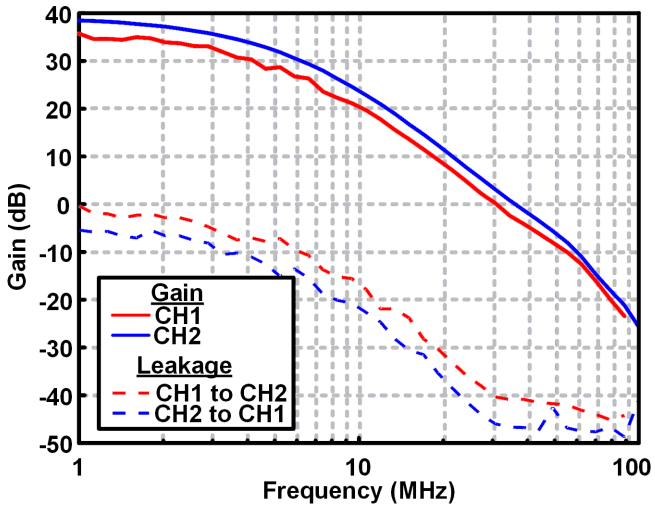


Figure 6.13: Measured receiver gain and isolation between CH1 and CH2.

CH2 by applying 4-phase NOP pulses operating at 1 GHz and 0.6 GHz respectively. The measured gain at CH1 and CH2 is 35.5 dB and 38.5 dB respectively. The asymmetry in the gain is due to the position of two correlators in the feedback path of the gain-boosted LNA. The leakage signal from CH2 to CH1 is measured at the CH1 output when the RF input frequency is close to the CH2 LO frequency and the measured isolation between the channels is 35 dB.

6.4.2 Noise Figure of the Receiver

The measured noise figure of the receiver without code modulation is 2.5 dB to 4 dB for an operating frequency range of 0.3 MHz to 1.4 GHz. The noise figure of the receiver is also compared with code modulation enabled using Y-Factor method in simulation. Fig. 6.14 shows that the noise figure of the receiver configured with and without code

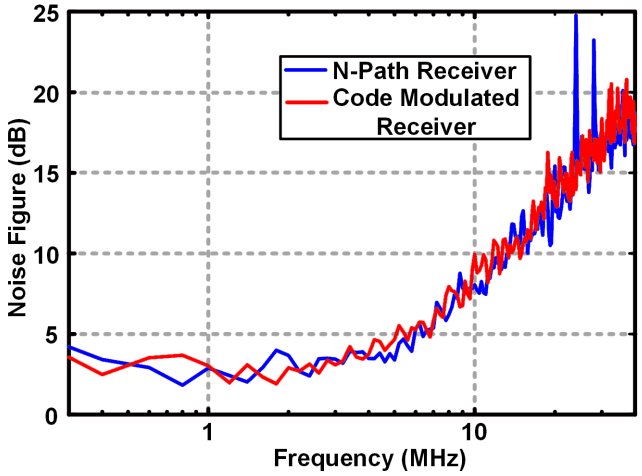


Figure 6.14: Simulated noise figure of the receiver with and without code modulation using Y-Factor method.

modulation is same. However, as discussed in Section 6.3, the mismatch between chip waveform and impulse response of correlator causes an additional 0.9 dB noise figure degradation.

6.4.3 Linearity of Receiver

The in-band IIP3 and OB-IIP3 of the receiver is measured without code modulation. The measured in-band IIP3 of the receiver is -26 dBm. The OB-IIP3 is $+13$ dBm which is measured using two tones at 45 MHz and 91 MHz offset frequencies.

Transmitter SIRC is measured by spreading a two-tone SI at 750 MHz using $PN_{WF,1}$ (Fig. 6.6) followed by despreading at receiver using orthogonal code $PN_{WF,2}$ and uncorrelated code PN_X. Fig. 6.15 demonstrates higher SIRC when $PN_{WF,2}$ is used compared to PN_X. Further, despreading with $PN_{WF,2}$ translates SI to 46.9 MHz

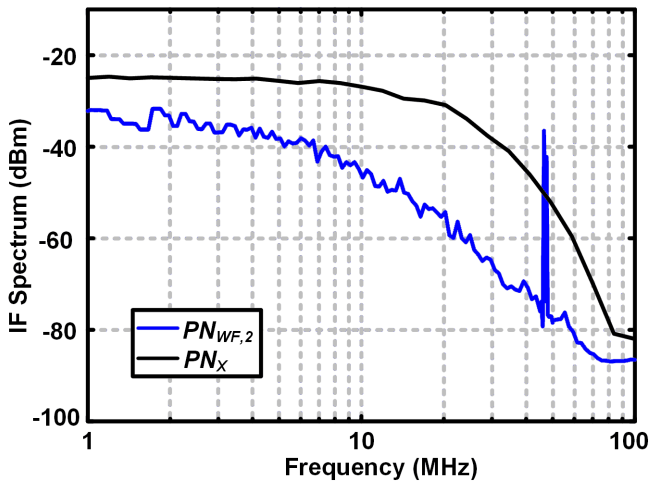


Figure 6.15: Measured two-tone SI at receiver output following spreading and despreading.

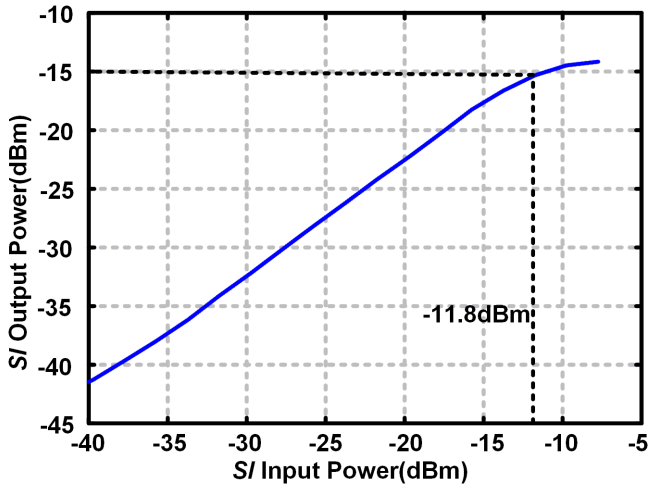


Figure 6.16: Measured integrated in-band receiver output power for modulated SI.

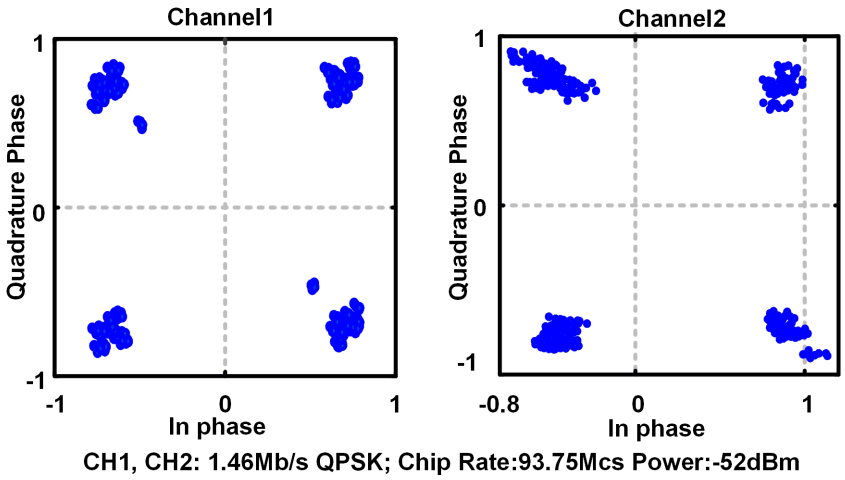


Figure 6.17: Concurrent reception of two code-modulated receiver signals at 750 MHz.

frequency at 93.75 Mcs chip rate. Subsequent lowpass filtering of the despreaded signal can provide higher SI rejection for $PN_{WF,2}$ case.

Fig. 6.16 plots integrated in-band power at receiver output over 1 MHz integration bandwidth as a function of SI power which is modulated as 1.46 Mb/s QPSK. Measurements demonstrate -11.8 dBm input-referred P_{1dB} with respect to SI power at the receiver input which can be translated to 13.2 dBm transmitter output power (assuming 25 dB isolation between transmitter and receiver port of the circulator). Notably, the receiver provides 35.5 dB gain for the desired signal, implying in-band SI rejection of 38.5 dB (from Fig. 6.16) and $+23.7$ dBm OP_{1dB} with respect to SI.

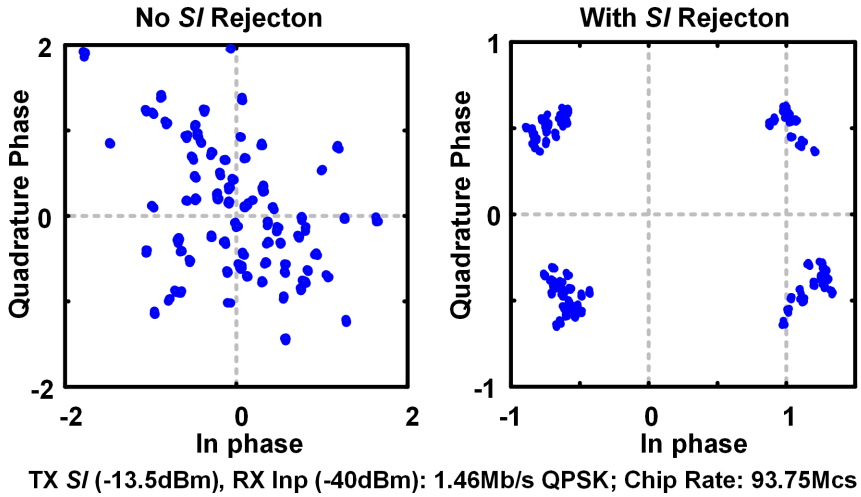


Figure 6.18: Reception of desired 750 MHz receiver signal in the presence of in-band SI following rejection approach.

6.4.4 Measured Constellation at the Receiver Output

Fig. 6.17 shows the measured constellation for two concurrent QPSK modulated signals with data rate 1.46 Mb/s at 750 MHz which is spreaded with different PN codes at chip rate 93.75 Mcs demonstrating concurrent reception. The minimum input power used at antenna is limited by the input-referred noise of the oscilloscope. Fig. 6.18 shows receiver constellation recovery with SIRC for -40 dBm desired input and -13.5 dBm SI (both at 1.46 Mb/s QPSK).

Table 6.1 compares the proposed code domain approach to the existing SIRC approaches. Present work pioneers in the code domain N-path receiver for SIRC achieving low power consumption and NF degradation in a smaller area opening up path for integration of code domain and SIC techniques in STAR application.

Table 6.1: Performance compared to state-of-the-art

	This Work	**Yang [131], JSSC 15**	**Zhou [135], ISSCC 15**	**Broek [133], ISSCC 15**	**Zhou [130], ISSCC 16**
f_c (GHz)	0.3-1.4	0.5-1.5	0.8-1.4	.15-3.5	0.6-0.8
Arch.	Code-domain N-path Mixer	Mixer-First TX/RX	Wideband SIC†	Mixer First VM SI	Circulator +BB SIC
No. of RX O/P	2	1	1	1	1
RX Gain (dB)	35/38	53	27-42	24	42
RX NF (dB)	2.5-4 + *0.9dB Filter mismatch	5-8	4.8	6.3	5.0
SIRC NF Deg (dB)	0	-	0.9/1.3	4-6	5.9*
IB IIP3 (dBm)	-26	-38.7	-20	+9/+19	-33
S/I P1dB (dB)	-11.8	-9.7**	-7.7**	9.3**	-27.7**
SIRC (dB)	38.5	33	25	27	42
BW (MHz)	1	0.6	20	16.25	12*
Power (mW)	LNA: 25.5 LO: 9.5◇ code mod.: ∼1 (sim)	43-56 (incl. TX BB)	107-250 †	23 - 56	160 *
Area (mm^2)	0.31	1.5	4.8	2	1.4

*includes N-path circulator antenna interface; NF degraded by LO PN, **computed from measured IIP3 (this work measured integrated power). † Includes filters to cancel across 9ns of peak delay in antenna interface; power consumption scales with one or two filters enabled. ◇ does not include power required for LO synchronization for code domain filtering.

Chapter 7: Conclusion

The enhancement in performance of wireless system by using hundreds of antenna array in a massive MIMO and millimeter wave system is very attractive. The practical deployment of such system depends upon inventing new circuit techniques such that array can scaled to any size by combining inexpensive transceivers in cost effective manner.

In this dissertation, an state-of-the-art area and power efficient clock generation scheme is presented to provide quadrature phases upto 6 GHz frequency range for 5G applications. A dual mode-switching series resonator is demonstrated to achieve 6.4-GHz to 14-GHz tuning range with 186-dB FoM. Extensions to higher number of modes are also demonstrated with a triple-mode 2.2-GHz to 8.7-GHz CMOS VCO that achieves 119% tuning range. Further, the series resonator mode switching scheme can be to other VCO topologies and classes of operation to increase both area and power efficiencies.

A scalable coherent clock generation and distribution scheme is presented for scalable mm-wave phased array/MIMO applications. Bidirectional coupling over a single-wire preserves simplicity of daisy-chain reference distribution while lowering phase noise. 28 GHz prototype in CMOS demonstrates phase noise and jitter improvement with increasing number of PLLs. Future work includes incorporation of synchronization scheme in a scalable mm-wave array/MIMO transceiver. A digital implementation of fractional PLL along with exhaustive calibration scheme to compensate phase offset can be incorporated in future work.

Further, blocker tolerant scalable parallel spatio-spectral notch filtering architecture is presented to relax the ADC dynamic range for scalable array application. A signal space approach is presented to explain the operation of passive mixer which is much simpler and intuitive compared to the LPTV approach. A bandstop and bandpass filters using orthogonal Walsh function is presented that provides impedance translational property similar to non-overlapping clock pulses based N-path filters with added features such as reconfigurability and insensitivity to clock overlap. A 65 nm CMOS prototype achieves $>$15 dB notch filtering at RF input for two independent frequencies (from 0.3 to 1.4 GHz)/angle-of-incidence defined by the sequence driving the mixers while causing $<$3 dB NF degradation. The approach can be extended to higher frequencies with technology scaling. Future work includes combining feedforward cancellation of jammers/interferers with the proposed architecture for interferer mitigation in MIMO arrays.

An extension of passive filter concept to code domain receiver is realized to enable full duplex communication in a CDMA system. A combination of Walsh-Function and PN sequence is proposed to translate in-band TX self-interference (SI) to out-of-band at N-path RX output enabling frequency filtering for high SI rejection. A 0.3 GHz-1.4 GHz 65-nm CMOS implementation can receives two RX signals concurrently while reflecting unknown in-band blocker at RF interface. Future work includes integration of automatic synchronization spreading code scheme between the transmitter and receiver.

APPENDICES

Appendix A: Frequency Tuning Range Analysis using Generalized Two-port Y-Parameters

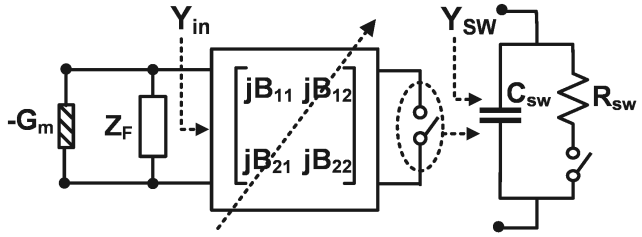


Figure A.1: A generalized two-port Y-parameter-based analysis demonstrates trade-off between resonator Q and FTR.

The impact of switch losses on a resonator can also be analyzed using two-port Y-parameters, similar to the analysis using Z-parameters in Section 2.2.1. The Y-parameter representation is convenient for analyzing certain network topologies, such as the switched capacitor bank in Section 2.2.2. In Fig. A.1, the resonator tank is represented using two-port lossless Y-parameter network terminated with a switch admittance, Y_{SW} at port 2. The input admittance seen at Port 1, Y_{in} must resonate a fixed reactance, Z_f, and can be determined from,

$$Y_{in} = jB_{11} - \frac{jB_{21}jB_{12}}{jB_{22} + Y_{SW}} \tag{A.1}$$

Assuming narrow tuning range, similar to Section 2.2.1, the product of $Q_{SW,ON}$ and

FTR is given by,

$$Q_{SW,ON}\frac{\Delta\omega}{\omega} = \frac{1}{2}\frac{1}{\omega R_{sw}C_{sw}\{1+\frac{B_{22}}{\omega C_{sw}}\}} \tag{A.2}$$

This formulation of the $Q\cdot FTR$ trade-off again captures the challenges of operating at higher frequencies and the significance of the switch technology constant in determining VCO performance.

Appendix B: $Q.FTR$ for Switched Inductor Banks

Based on Fig. 2.4(b), the inductance in the on-state and off-state are given by,

$$L_{ON} = L_1 + L_2 \parallel L_3 \tag{B.1}$$

$$L_{OFF} = L_1 + \frac{L_2(1 - \omega_{OFF}^2 L_3 C_{SW})}{1 - \omega_{OFF}^2 (L_2 + L_3) C_{SW}} \tag{B.2}$$

The change in tank inductance, ΔL is hence,

$$\Delta L = \frac{L_2^2}{(L_2 + L_3)(1 - \omega_{OFF}^2 (L_2 + L_3) C_{SW})} \tag{B.3}$$

The on-state inductor quality factor for the network in Fig. 2.4(b), $Q_{SW,ON}$ is given by,

$$Q_{SW,ON} = \frac{(L_2 + L_3)^2}{L_2^2} \frac{\omega_{ON} \left(L_1 + L_2 \parallel L_3\right)}{R_{SW}} \tag{B.4}$$

Therefore, using (B.1)-(B.4)

$$Q_{SW,ON} \left| \frac{\Delta L}{L_{ON}} \right| = \frac{\omega_{ON}}{\omega_{OFF}} \left| \frac{1}{\omega_{OFF} R_{SW} C_{SW} \left(1 - \frac{\omega_Z^2}{\omega_{OFF}^2}\right)} \right| \tag{B.5}$$

The inductances in the switch on-state and off-state are also related as,

$$\frac{L_{ON}}{L_{OFF}} = \frac{\omega_{OFF}^2}{\omega_{ON}^2} \tag{B.6}$$

Using (B.6) in (B.5)

$$Q_{SW,ON}\left|\frac{\Delta L}{L_{OFF}}\right| = \frac{\omega_{OFF}}{\omega_{ON}}\left|\frac{1}{\omega_{OFF}R_{SW}C_{SW}\left(1-\frac{\omega_Z^2}{\omega_{OFF}^2}\right)}\right| \tag{B.7}$$

Appendix C: Derivation of Input impedance for Notch filter based WF-seq

As discussed in Section 4.2, the notch filter based on WF-seq can be designed with higher order sequence to improve the bandstop rejection of the interferer. Without loss of generality, a 3^{rd}order notch filter is discussed in this Appendix and can be extended to any order filter by following the same steps used for 3^{rd}order filter.

The notch filter based on 3^{rd}order WF-seq can be analyzed using simplified model shown in Fig. C.1. Switches are driven by periodic WF-seq with time period T_0 and are assumed to be ideal. The Norton equivalent of antenna port consists of incident current source I_{ANT} and port resistor R_{ANT}. Further, R_{ANT} and input impedance from receiver R_L are combined and represented as equivalent parallel resistor R_a. Assuming the time constant L_i/R_a of baseband current $I_{BB,i}$ through inductor L_i is relatively large compared to time period T_0, the current stays relatively constant over several RF cycles. Thus, the baseband current $I_{BB,i}$ and RF voltage $V_x(t)$ are

$$I_{BB,i}(t) = \frac{1}{L}\int WF_i(t)V_x(t) \tag{C.1}$$

$$V_x(t) = \left(I_{ANT}(t) - \sum_{i=1}^{i=4} I_{BB,i}(t)WF_i(t)\right)R_a \tag{C.2}$$

where WF_i is Walsh functions and are $sal(1)$, $cal(1)$, $sal(3)$ and $cal(3)$ respectively used for the 3^{rd}order filter. Due to orthogonality of Walsh function, the correlation

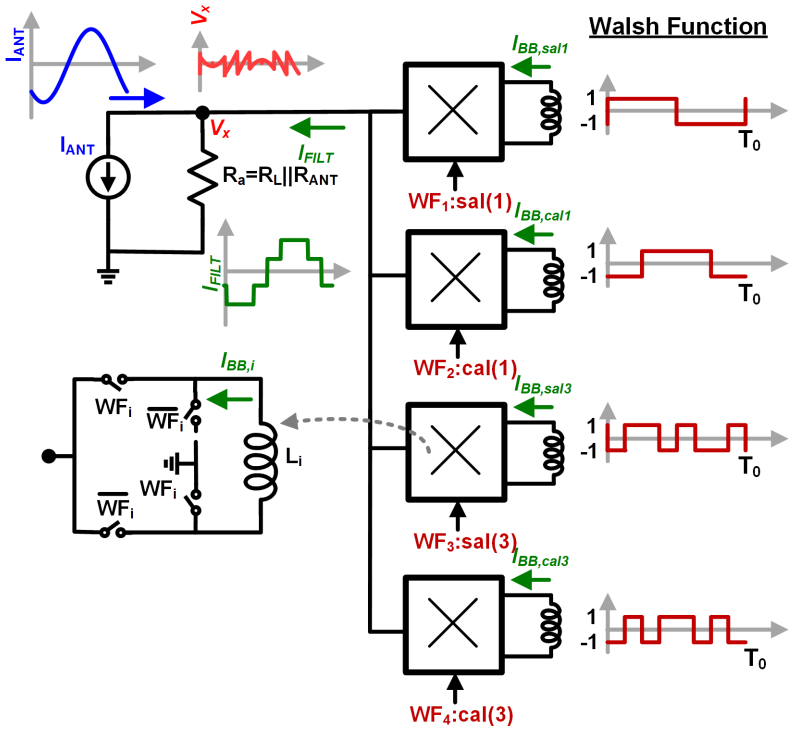


Figure C.1: Bandstop passive filter based on 3^{rd}order Walsh Function sequence.

between any two WF is Kronecker delta function and is

$$\int WF_i(t)WF_i(t)dt = \delta_{ij} = \begin{cases} 1, & \text{if } i = j \\ 0, & \text{if } i \neq j \end{cases} \tag{C.3}$$

Using (C.3), (C.1) and (C.2), the inductor current can be expressed as,

$$\begin{aligned} I_{BB,i}(t) &= \frac{R_a}{L}\left(\int WF_i(t)I_{ANT}(t)dt - \int \sum_{j=1}^{i=4} I_{BB,j}(t)WF_j(t)WF_i(t)dt\right) \\ &= \frac{R_a}{L}\left(\int WF_i(t)I_{ANT}(t)dt - \sum_{j=1}^{i=4} I_{BB,j}(t)\int WF_j(t)WF_i(t)dt\right) \\ &= \frac{R_a}{L}\left(\int WF_i(t)I_{ANT}(t)dt - \int I_{BB,i}(t)dt\right) \end{aligned} \tag{C.4}$$

For the sinusoid input current source $I_{ANT} = Acos((\omega_0 + \omega_{IF})t + \phi)$, the baseband current $I_{BB,i}(\omega)$ can be computed in frequency domain as,

$$I_{BB,i}(\omega) = \frac{R_a}{j\omega L + R_a} c_i(\omega) \tag{C.5}$$

Where c_i is WF coefficient and can be calculated using (4.6). Further, c_i can be represented in frequency domain as,

$$c_0(\omega) = \frac{-2A}{\pi}\left(\frac{e^{j\phi}\delta(\omega+\omega_{IF}) - je^{-j\phi}\delta(\omega-\omega_{IF})}{2}\right) \tag{C.6}$$

$$c_1(\omega) = \frac{2A}{\pi}\left(\frac{e^{j\phi}\delta(\omega+\omega_{IF}) + je^{-j\phi}\delta(\omega-\omega_{IF})}{2}\right) \tag{C.7}$$

$$c_2(\omega) = \frac{-2(2-\sqrt{2})A}{\pi}\left(\frac{e^{j\phi}\delta(\omega+\omega_{IF}) - je^{-j\phi}\delta(\omega-\omega_{IF})}{2}\right) \tag{C.8}$$

$$c_3(\omega) = \frac{2(2-\sqrt{2})A}{\pi}\left(\frac{e^{j\phi}\delta(\omega+\omega_{IF}) + je^{-j\phi}\delta(\omega-\omega_{IF})}{2}\right) \tag{C.9}$$

The impedance seen by the incident signal at fundamental frequency $\omega_0 = 2\pi f_0$ is calculated by determining the voltage V_x at ω_0. Using (C.2) and (4.8), the fundamental component of voltage $V_{x,fund}$ is given by

$$V_{x,fund}(\omega) = R_a\left(I_{ANT}(\omega) - \sum_{i=1}^{i=4}\frac{1}{2\pi}\left(\frac{R_a c_i(\omega)}{j\omega L + R_a} * WF_{i,fund}(\omega)\right)\right) \tag{C.10}$$

where $WF_{i,fund}(t)$ is the fundamental component of WF-seq and are

$$WF_{0,fund}(\omega) = \frac{4}{\pi}\frac{\delta(\omega+\omega_0) - j\delta(\omega-\omega_0)}{2} \tag{C.11}$$

$$WF_{1,fund}(\omega) = \frac{4}{\pi}\frac{\delta(\omega+\omega_0) + \delta(\omega-\omega_0)}{2} \tag{C.12}$$

$$WF_{2,fund}(\omega) = \frac{4(2-\sqrt{2})}{\pi}\frac{\delta(\omega+\omega_0) - j\delta(\omega-\omega_0)}{2} \tag{C.13}$$

$$WF_{3,fund}(\omega) = \frac{4(2-\sqrt{2})}{\pi}\frac{\delta(\omega+\omega_0) + \delta(\omega-\omega_0)}{2} \tag{C.14}$$

Hence, the impedance of 3^{rd}order filter seen at antenna port, calculated by substituting (C.11)-(C.14) and (C.5) into (C.10), is

$$\frac{V_x(\omega_0+\omega_{IF})}{I_{ANT}(\omega_0+\omega_{IF})} = R_a\left(1-\frac{16(2-\sqrt{2})}{\pi^2}\frac{R_a}{j\omega_{IF}L+R_a}\right) \tag{C.15}$$

For the analysis of the 2^{nd}order WF-seq based notch filter, same model can be used with two filters driven by $sal(1)$ and $cal(1)$. Therefore, the impedance of the 2^{nd}order filter is

$$\frac{V_x(\omega_0+\omega_{IF})}{I_{ANT}(\omega_0+\omega_{IF})} = R_a\left(1-\frac{8}{\pi^2}\frac{R_a}{j\omega_{IF}L+R_a}\right) \tag{C.16}$$

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