AN ABSTRACT OF THE THESIS OF

Xin Meng for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on May 22, 2015.

Title: Wideband Discrete-Time Delta-Sigma Analog-to-Digital Converters With Shifted Loop Delays.

Abstract approved:

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Gabor C. Temes

Low-distortion architecture is widely used in wideband discrete-time switched-capacitor delta-sigma ADC design. However, it suffers from the power-hungry active adder and critical timing for quantization and dynamic element matching (DEM). To solve this problem, this dissertation presents a delta-sigma modulator architecture with shifted loop delays. In this project, shifted loop delays (SLD) technique can relax the speed requirements of the quantizer and the dynamic element matching (DEM) block, and eliminate the active adder. An implemented 0.18 um CMOS prototype with the proposed architecture provided 81.6 dB SNDR, 81.8 dB dynamic range, and -95.6 dB THD in a signal bandwidth of 4 MHz. It dissipates 19.2 mW with a 1.6 V power supply. The conventional low-distortion ADC was also implemented on the same chip for comparison. The new circuit has superior performance, and dissipates 25% less power (19.2 mW vs. 24.9 mW) than the conventional one. The figure-of-merit for the ADC with SLD is among the best reported for wideband discrete-time ADCs, and is almost 40% better than that of the conventional ADC.

The second project describes two techniques to enhance the noise shaping function in the proposed low-distortion ΔΣ modulator with shifted loop delays. One is self-noise coupling based on low-distortion ΔΣ structure; the other is noise-coupled

time-interleaved ΔΣ modulator. Both architectures use shifted loop delays to relax the critical timing constraints in the modulator feedback path, then to save power consumption of each block in the modulators. Two ΔΣ ADCs were analyzed and simulated in a 0.18um CMOS technology. The simulation results highly verify the effectiveness of the proposed structure.

The third system describes the design technique for double-sampled wideband ΔΣ ADCs with shifted loop delays (SLD). The added loop delay in the feedback branch relaxes the critical timing for DEM logic. Delay shifting can be combined with such useful techniques as low-distortion circuitry and noise coupling for wideband ΔΣ modulators. The presented techniques relax the timing for inherent quantization delay, reduce the speed requirements for the critical circuit blocks, and achieve power efficiency by replacing the power-hungry blocks normally used in the modulators. Analysis of all architectures allows the choice of the most power-efficient topology for a wideband ΔΣ modulator. The proposed second-order and third-order ΔΣ modulators were designed and simulated to verify the effectiveness of the shifted loop delays techniques.

Wideband Discrete-Time Delta-Sigma Analog-to-Digital Converters With Shifted Loop Delays

by
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Xin Meng, Author

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Wideband Discrete-Time Delta-Sigma Analog-to-Digital Converters With Shifted Loop Delays

CHAPTER 1 . INTRODUCTION

1.1. Motivation

Hearing and seeing are real-time transmissions in the human senses. State-of-art technologies, like Hi-Fi audio system [1], high efficiency video coding and 3D video [2], are utilized to achieve high-quality audios and videos sources. When transmitting the media signal, increasing bandwidth of telecommunication channel has relieves the speed bottleneck of releasing 720p or higher-resolution videos. In the receiving terminals, smart phones, tablets and HDTV offer higher pixel density to match the audios' and videos' resolution. The whole industrial chain of transmitting media signals emphasizes an increasing market on the high-speed high-resolution analog and digital interface circuits, especially data converters.

On the other hand, portable devices are becoming more and more popular in media world because of providing one more freedom by getting rid of electric cables. However, battery-powered mobile devices restrict this unplugging to a limited time usage because of its demand on recharging. It is very common for people to expect longer battery time, which emphasizes low-power property in all electronics chips, including data converters.

Data converters are constructing a bridge between the analog world (the physical world) and digital world (the data world). With down-scaling of transistors' size, data converters, including analog-to-digital converters (ADC) and digital-to-analog converters (DAC), are become a performance bottleneck in an on-chip system. In deep submicrometer CMOS technologies, compared to other ADC counterparts, delta-sigma (ΔΣ) modulators, because of their inherent oversampling and noise shaping, are becoming popular in high-resolution bandwidth application. In this

thesis, we describe some new techniques and architectures to design a high-speed, high-resolution, low-power delta-sigma ADCs.

There are two realizations for ΔΣ modulators: continuous-time (CT) modulators and discrete-time (DT) modulators. CT modulators are becoming more and more popular in wideband applications because of several advantages: 1. easy to drive from external sources; 2. higher permissible frequency; 3. inherently anti-alias filter; 4. integrator operational transconductance amplifiers (OTAs) consume less power than DT counterparts. For 10 MHz or higher signal bandwidth applications, CT modulators have often been used [3]-[10]. However, compared with DT ΔΣ ADCs, the design of CT ΔΣ modulators is complex and challenging. CT ADCs are very sensitive to clock jitter noise; this situation becomes worse when the feedback DAC uses return-to-zero pulses. The loop filter transfer function is suffering from the large coefficient uncertainty due to variations of resistors and capacitors referring to process, voltage and temperature (PVT). The stability of the loop filter is degrading because of the excess feedback loop delay.

So far, most commercial ΔΣ ADCs use traditional DT realization, based on switched capacitor (SC) circuitry. The loop filter of DT ΔΣ modulators can be easily analyzed and designed in z-domain, and the design procedure is well developed [11] [12]. Pole-zero locations of the loop filter are set by precise capacitor ratios, which are highly accurate and insensitive to process variation. DT modulators offer robust operation and are insensitive to clock jitter, as long as complete settling occurs. However, DT modulators require large switched input capacitors to lower kT/C noise, and hence are difficult to drive form external sources. Furthermore, the settling requirements of OTAs have to trade off with the power consumption of OTAs, which is limited by the sampling frequency and bandwidth of DT ΔΣ ADCs. Along with the increasing signal bandwidth, the power dissipation of each integrator increases rapidly. Even so, recently published low-power DT ΔΣ ADCs could achieve 10 to 25 MHz bandwidth [13]-[16]. In this thesis, we describe some new techniques and architectures to expand the bandwidth and lower the power consumption for wideband DT ΔΣ ADCs.

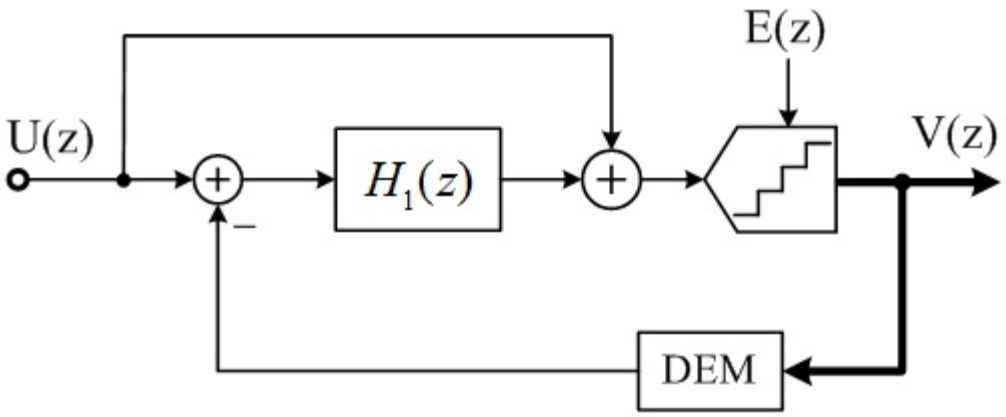

Figure 1.1: Feed-forward low-distortion ΔΣ ADC.

1.2. Contributions of This Research

In conventional DT ΔΣ modulators, high quantizer resolution and high loop filter order helps to provides high resolution and linearity. However, finite OTA gain and nonlinear slew-rate of integrators cause harmonic components in the digital output. One effective solution to attenuate the harmonics is higher oversampling ratio (OSR). But the OSR cannot be too high, since then high-speed OTAs will be much power-hungry in wideband applications. Another effective method to greatly attenuate the harmonics is adding a direct feed-forward path from the input signal to the quantizer, making STF = 1. This structure is called the low-distortion modulator, shown in Figure 1.1. The linearity requirements of this architecture are relaxed by cancelling the signal components in the loop filter $H_1(z)$ [17]. This situation gets even better when using multi-bit quantizer, because the quantization error is reducing further. And the DEM technique is required to improve the linearity of the feedback DAC in a multi-bit modulator. However, the processing time is restricted for the quantizer and DEM operation in the low-distortion modulator.

In this thesis, shifting loop delays technique is described to release the critical timing issue for the quantizer and DEM operation. Furthermore, the active adder is also eliminated by this technique. The major contributions of this research are summarized as follows:

1. A novel power-efficient ΔΣ modulator with shifted loop delays is proposed. In this new architecture, the speed of quantizer and DEM logic can be greatly reduced. To verify the effectiveness, a conventional DT low-distortion ΔΣ modulator are also designed and fabricated in a 0.18 um CMOS process to make the comparison.
2. Noise shaping enhancement techniques are demonstrated in the novel ΔΣ modulators. Two discrete-time ΔΣ modulator topologies combined with shifted loop delays (SLD) are proposed. One is self-noise coupling based on low-distortion ΔΣ modulator; the other one is noise-coupled time-interleaved structure. Both architectures are analyzed and simulated in a 0.18um CMOS technology to verify the effectiveness.
3. Shifting loop delays can also used in double-sampled wideband ΔΣ ADCs. Combining double sampling with shifted loop delays, the proposed modulators can relax the critical timing constraints in the modulator feedback path. In a 0.18um CMOS technology, a second-order and a third-order noise shaping ΔΣ ADCs were analyzed and simulated.

1.3. Organization of the Dissertation

This thesis presents the design of wideband discrete-time ΔΣ modulators in an advanced deep sub-micron CMOS technique. By shifting loop delays, several low-power high-performance ΔΣ ADCs are designed and analyzed. Both system level and transistor level design are covered in each modulator; and simulation results and measurement results are illustrated to verify the effectiveness of the proposed architectures. The thesis is organized as follows:

Chapter 2 introduces a novel low-distortion feed-forward ΔΣ modulator with shifted loop delays. This architecture relaxes the critical feedback timing issue by shifting one loop delay from the loop filter to the feedback path. The speed of quantizer and DEM logic can be greatly reduced, hence to save power consumptions of each integrator, quantizer and DEM logic. One extra feedback path is fed back into the last integrator to improve the loop stability and make the STF equal to be unity.

The transistor level circuits are also introduced; the simulation results and measurement results are illustrated.

Chapter 3 describes two techniques to enhance the noise shaping function in the proposed low-distortion ΔΣ modulator with shifted loop delays. One is self-noise coupling based on low-distortion ΔΣ structure; the other is noise-coupled time-interleaved ΔΣ modulator. Both architectures use shifted loop delays to relax the critical timing constraints in the modulator feedback path, then to save power consumption of each block in the modulators. Two ΔΣ ADCs were analyzed and simulated in a 0.18um CMOS technology. The simulation results highly verify the effectiveness of the proposed structure.

Chapter 4 presents several discrete-time double-sampled ΔΣ ADCs with shifted loop delays. The proposed architectures use the shifted loop delays to compensate the inherent quantization delay. The added loop delay in the feedback branch helps to relax the critical timing for DEM logic. Delay shifting can be combined with such useful techniques as low-distortion circuitry and noise coupling for wideband double-sampled ΔΣ modulators. The presented techniques reduce the speed requirements for the critical circuit blocks, and achieve power efficiency by replacing the power-hungry blocks normally used in the modulators. Analysis of all architectures allows the choice of the most power-efficient topology for a wideband ΔΣ modulator. The proposed second-order and third-order ΔΣ modulators were designed and simulated to verify the effectiveness of the shifted loop delays techniques.

The appendix analyzes the settling operation of cascaded integrators. By comparing delayed integrators and delay-free integrators, the penalty for removing the delay from two cascaded integrators is estimated. For a 0.1% resolution, two-stage cascaded delay-free integrators consume 21% more power consumption and three-stage ones take 40% more.

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CHAPTER 2 . LOW-POWER WIDEBAND DISCRETE-TIME DELTA-SIGMA ADCs WITH SHIFTED LOOP DELAYS

Low-distortion architecture is widely used in wideband discrete-time switched-capacitor delta-sigma ADC design [1]. However, it suffers from the power-hungry active adder and critical timing for quantization and dynamic element matching (DEM). In this chapter, shifted loop delays (SLD) technique is described to solve these problem. It can relax the speed requirements of the quantizer and the DEM block, and eliminate the last stage adder. To verify the effectiveness, the proposed architecture was implemented in 0.18 um CMOS. The conventional low-distortion ADC was also implemented on the same chip for comparison. The new circuit has superior performance, and dissipates 25% less power than the conventional one.

2.1. Introduction

With increasing market for battery-powered portable electronics in wireless communications and high-definition media applications, high-performance low-power analog-to-digital converters (ADCs) need to meet stringent specifications. Delta-sigma ($\Delta\Sigma$) modulators, because of their inherent oversampling and noise shaping, are well suited for medium-to-high resolution and MHz-bandwidth applications [2-4]. For discrete-time realization, the low-distortion $\Delta\Sigma$ ADC with feed-forward structure in Figure 2.1 is widely used in wideband application. The input signal *U* passes through the feed-forward branch, the quantizer and the DEM. When *U* arrives at the first integrator, it cancels the input signal, leaving only the shaped quantization noise. Hence the modulator can achieve high linearity by eliminating input signal component in its loop filter [1]. The linearity requirements for all integrators are even more relaxed when using multi-bit quantizer. However, the drawback is the need for a power hungry active adder and an additional time slot required for the quantization and the DEM circuitry. These issues become even more challenging with increasing signal bandwidth.

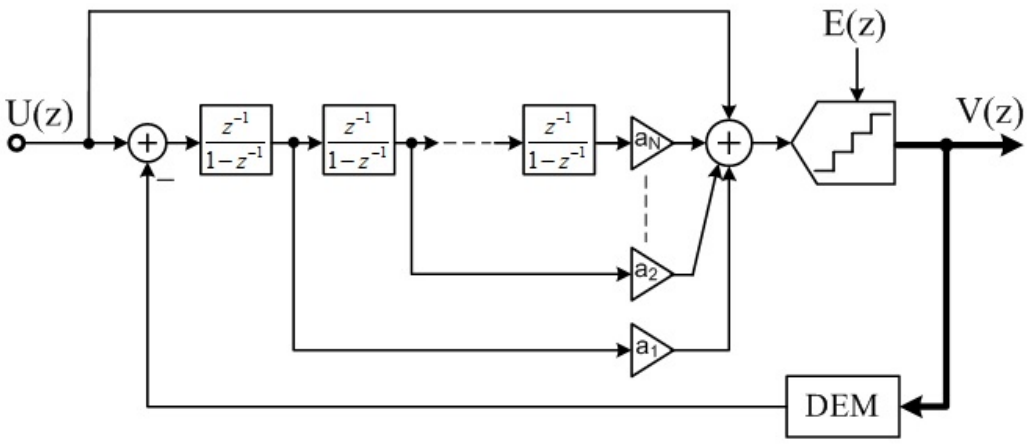


Figure 2.1: Conventional ΔΣ low-distortion modulator [1].

In this chapter, a shifted-loop-delay (SLD) architecture is proposed to solve these problems. It allows more time for quantization and DEM without degrading its loop stability, and reduces power consumption by eliminating the active adder [5]. A low-distortion ΔΣ ADC with SLD and its conventional counterpart, implemented in 0.18 μm CMOS technology are reported. The measured results verify that the ADC with SLD can achieve improved performance and dissipates less power than not only the conventional one, but also the state-of-the-art published ADCs. Section 2.2 introduces the shifted loop delays in ΔΣ ADCs, providing a general design procedure for loop filters with maximally flat noise transfer function (NTF). Design details and circuit implementation for two prototypes follow in Section 2.3. The measured results that verify the effectiveness of the proposed architecture are described in section 2.4. Finally, section 2.5 draws the summary of the implementation.

2.2. Architecture Considerations

A modulator with shifted loop delay was first introduced in [6], as a *"cascade of integrators with distributed feedback topology with capacitive input feed-forward (CIFB-CIF)."* Figure 2.2 shows a second-order CIFB-CIF ΔΣ modulator using two OTAs. In this topology, one cycle delay of the last integrator is shifted to the first stage and also to the feedback path. The delay shifted to the first stage helps to avoid making the second integrator two-pole system, and makes it still delayed integrator.

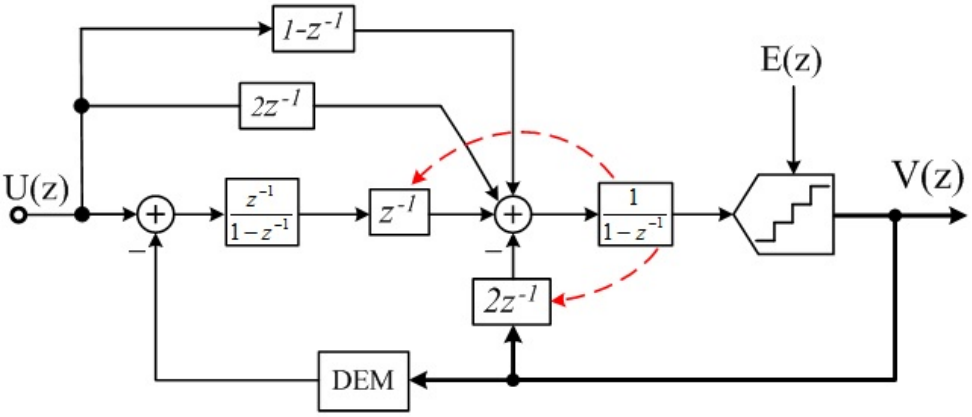


Figure 2.2: Shifted loop delays in the CIFB-CIF topology [6].

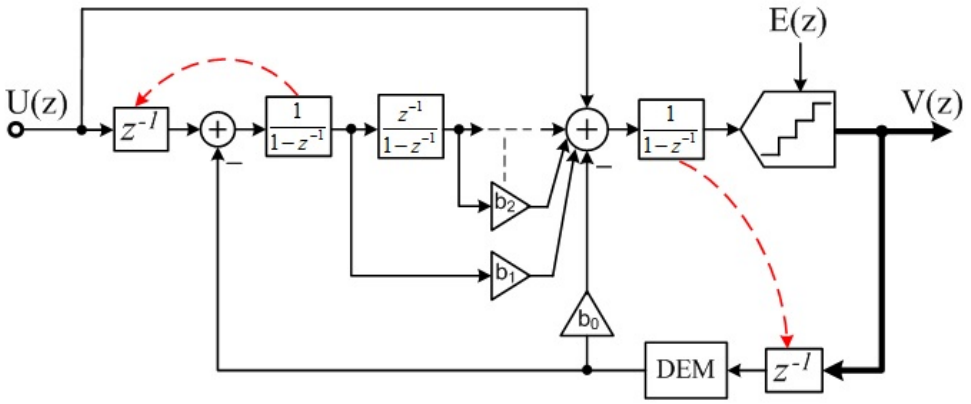


Figure 2.3: Low-distortion ΔΣ ADC with Shifted loop delays [7].

However, it still suffers from restricted timing; and it also needs complex feed-forward paths to retain the low-distortion property. This requires a larger capacitor area and more involved timing logic, and also consumes more power consumption due to the small feedback factor (β = 1/7) of the last integrator.

Next, we proposed shifted loop delay topologies to relax timing and power [7]. The basic idea is moving the delay of the last integrator to the feedback path, so that DEM can be performed in this delay. Also the modulator shifts the delay from the first integrator to the input signal path to keep the low-distortion property. To restore the stability affected by the shifted loop delays, an extra feedback path is also introduced to the last integrator. Figure 2.3 shows the resulting block diagram. Here, b_0 is the gain of the added feedback branch; b_1 and b_2 are the coefficients of the feed-forward paths.

The general design procedure to obtain the coefficients in Figure 2.3 is as follows. For a low-distortion DT ΔΣ ADC with N^{th}-order noise shaping (Figure 2.1), the loop gain *H(z)* is

$$H(z) = \sum_{i=1}^{N} \frac{a_i}{(z-1)^i} \tag{2.1}$$

Here, a_N is usually set to 1. The noise transfer function is

$$NTF(z) = \frac{1}{1+H(z)} \tag{2.2}$$

Matching the loop gains *H(z)* of the two systems shown in Figures 2.1 and 2.3 gives

$$\sum_{i=1}^{N} a_i I^i(z) = \frac{1}{1-z^{-1}} \left[b_0 z^{-1} + \sum_{i=1}^{N-1} b_i I^i(z) \right] \tag{2.3}$$

Here

$$I(z) = \frac{z^{-1}}{1-z^{-1}} \tag{2.4}$$

Equation (2.3) can be re-arranged as

$$\sum_{i=1}^{N} a_i I^i(z) = I(z) b_0 + \sum_{i=1}^{N-1} \left[b_i (I^i(z) + I^{i+1}(z)) \right] \tag{2.5}$$

For z = 0, $I(0) = -1$, so (2.5) gives

$$b_0 = \sum_{i=1}^{N} a_i (-1)^{i+1} \tag{2.6}$$

From (2.1) and (2.2),

$$b_0 = -H(0) = 1 - \frac{1}{NTF(0)} = 1 \tag{2.7}$$

Thus, b_0 is always equal to 1, regardless of the order of the modulator.

In matrix notation

$$\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ \mathsf{M} \\ a_{N-1} \\ a_N \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ \mathsf{M} \\ I^{N-1}(z) \\ I^N(z) \end{bmatrix} = \begin{bmatrix} b_0 + b_1 \\ b_1 + b_2 \\ b_2 + b_3 \\ \mathsf{M} \\ b_{N-2} + b_{N-1} \\ b_{N-1} \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ \mathsf{M} \\ I^{N-1}(z) \\ I^N(z) \end{bmatrix} \tag{2.8}$$

Matching the coefficients of $I^i(z)$ in (2.5)gives

$$\begin{bmatrix} a_1 \\ a_2 \\ \mathsf{M} \\ a_{N-1} \\ a_N \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & \mathsf{L} & 0 \\ 0 & 1 & 1 & \mathsf{L} & 0 \\ \mathsf{M} & \mathsf{M} & \mathsf{M} & \mathsf{O} & \mathsf{M} \\ 0 & 0 & \mathsf{L} & 1 & 1 \\ 0 & 0 & \mathsf{L} & 0 & 1 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ \mathsf{M} \\ b_{N-2} \\ b_{N-1} \end{bmatrix} \tag{2.9}$$

By inspection,

$$b_i = a_i - b_{i-1} \qquad (i = 1,2,\mathsf{L}\ ,N-2) \tag{2.10}$$

$$b_{N-1} = a_N \tag{2.11}$$

All b_i can be found directly from (7) and (9).

The linear model of a low-distortion ΔΣ modulator with SLD is shown in Figure 2.3. The delay of the last integrator is moved to the feedback path, so that the quantization and DEM can be performed in this period. Also, the modulator shifts the delay from the loop filter to the input signal path and introduces an extra feedback path to the summing node of the last integrator, so that the stability of the loop is preserved. The proposed scheme still uses a direct feed-forward path from the input to the last integrator to keep the low-distortion property. However, it utilizes the last integrator to achieve both integration and active summation, hence eliminating the active adder. As shown in equation 2.10 and 2.11, the order of the loop filter transfer function can be one less than that in Figure 2.1.

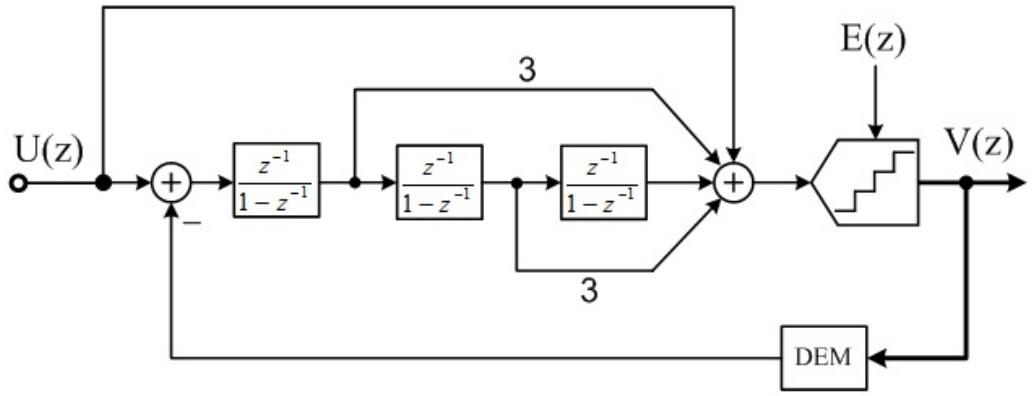


Figure 2.4: Conventional third-order low-distortion ΔΣ modulator.

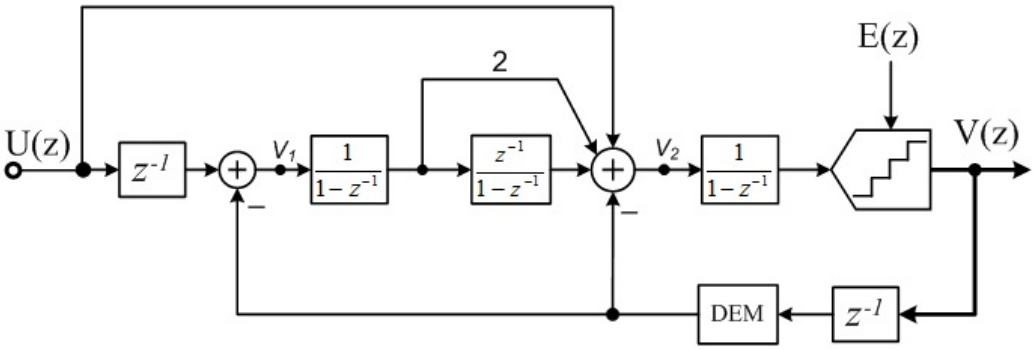


Figure 2.5: Proposed third-order low-distortion ΔΣ modulator with SLD.

To further verify the effectiveness of the proposed SLD architecture, two third-order ΔΣ modulator are analyzed. Figure 2.4 illustrates a conventional third-order low-distortion ΔΣ modulator. The quantization and DEM must be performed in the non-overlapping time slot. The extra time needed by the quantization and the DEM shortens the settling time, hence requires higher speed for all blocks, including the integrators, the quantizer and the DEM logic. To alleviate this problem, in the proposed third-order modulator (Figure 2.5), one delay is moved from the last integrator to the feedback path, so that the quantizer and the DEM logic can operate in one clock period, and the non-overlapping time slot can be compressed to minimum.

In the proposed ADC, the input signal *U* passes through the feed-forward branch, the last integrator, the quantizer and the DEM. When *U* arrives at the first

integrator, it cancels the signal travelling through the other delayed path. Thus the input signal of the loop filter does not contain the input signal, and the reduced signal swing and the low-distortion property of the conventional feed-forward ADC are preserved. The multi-bit (15-level) quantizer DAC further reduces the input/output swings of the integrators in the loop filter, and improves the modulator stability.

To keep the modulator stable, an extra feedback path is connected to the input of the last integrator (Figure 2.5). A first-order noise shaping function $(1-z^{-1})$ is applied to the input signal $U(z)$, when combining this feedback path and the feed-forward path. After passing through the delay-free integrator, $(1-z^{-1})U(z)$ will be again equal to $U(z)$, which makes the signal transfer function unity. The stability of the proposed modulator, its dynamic range and harmonic suppression are all improved because of the reduced signal swings at the internal nodes of the loop filter. An additional advantage is that the injected quantization noise works as a dither signal. Thus the proposed topology provides increased stability, as well as reduced idle tones and harmonic spurs [8].

Linear analysis of the modulator in Figure 2.5, given below, verifies the previous conclusions. It shows that there is only shaped quantization noise at the input of the loop filter, and that the signal swing at the input of the last integrator is also shaped:

$$V(z) = U(z) + (1 - z^{-1})^3 E(z) \tag{2.12}$$

$$V_1(z) = -z^{-1}(1 - z^{-1})^3 E(z) \tag{2.13}$$

$$V_2(z) = (1 - z^{-1})U(z) + (1 - z^{-1})^4 E(z) - (1 - z^{-1})E(z) \tag{2.14}$$

The MATLAB SIMULINK simulation results shown in Figure 2.6 also verify the analysis. They assume OSR = 15, a 15-level quantizer and 120 MHz clock for a 4 MHz bandwidth. The results in Figure 2.6 show that there is no signal component in V_1, leaving only the shaped quantization error. Thus the low-distortion characteristic has been preserved. V_2 at the input of the last integrator gives the shaped input signal at -75 dBFS, which is highly suppressed compared to the input swing in the last opamp of Figure 2.4, whose is almost full-scale swing.

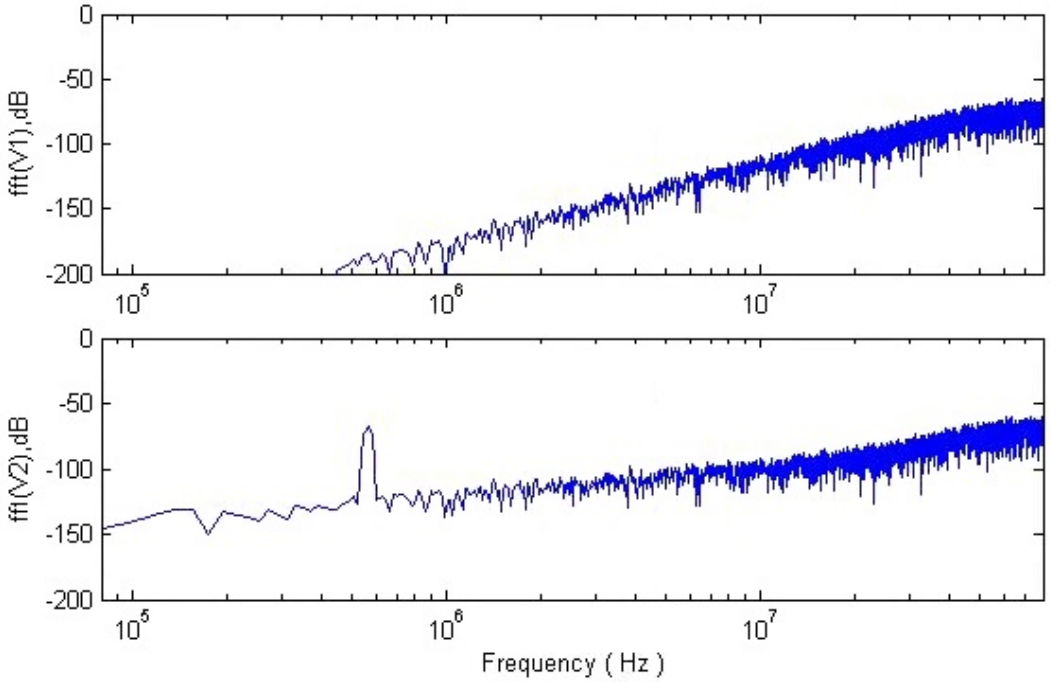


Figure 2.6: Simulated spectra of the node voltages V_1 and V_2 in Figure 2.5.

Table 2.1: Comparison Between ΔΣ ADCs in Figures 2.4 and 2.5

	Specification	Conv.	SLD
Architecture	*No. of opamp*	*4*	*3*
System timing	*Settling time*	*2.9 ns*	*3.7 ns*
	Advanced cutoff	*360 ps*	*180 ps*
	Non-overlapping	*790 ps*	*170 ps*
Specification for the last opamp	*Feedback factor*	*1/9*	*1/6*
	Input swing	*-0.05 dBFS*	*-7.21 dBFS*
	Output swing	*-0.05 dBFS*	*-0.06 dBFS*

Compared with the conventional ΔΣ modulator of Figure 2.4, the proposed modulator structure can use 27% more time to settle all opamps, which allows relaxation of the opamps' settling speed. The last opamp has 7.16 dB smaller input swing, which relieves also the slew rate requirement. The comparison results are shown in Table 2.1. A drawback of using shifted loop delays is that the cascaded delay-free integrators need a 20% longer settling time [7]. However, overall the required unity gain bandwidth of the last opamp in Figure 2.5 is 39% lower than for that in the circuit of Figure 2.4.

2.3. Circuit Implementation

It is straightforward to implement the Figure 2.5 using switched-capacitor (SC) circuits. The most sensitive performance happens at the input of the first integrator. The shifted loop delay in the first integrator can be implemented by two-phase sampling technique [5], double sampling [2] or triple sampling [3]. However, two-phase sampling suffers from large swings due to two-phase settling; double sampling and triple sampling results in linearity degradation due to path mismatch and interferers around $F_S/2$. In this design, the first integrator is implemented by conventional single sampling. Figure 2.7 illustrates the single-ended switched-capacitor circuit diagram of the proposed modulator. However, here the first integrator shifts only half a clock period in the input path. The missing $z^{-1/2}$ is not critical if the OSR is relatively large [4]. It causes a gain error of only 0.7% for OSR = 15. The input sampling and DAC capacitors of the first integrator are separated to avoid signal-dependent reference loading. The input sampling capacitors and DAC capacitors are reduced by half to preserve the same feedback factor with the shared capacitors [9], and the signal swings for input and DAC reference are doubled by cross-coupled sampling between positive and negative paths.

Bootstrapped clock signals are applied at the critical input switches to ensure signal-independent sampling. The 14 comparators use input offset sampling to minimize the offset effect. Data weighted averaging (DWA) is used to shape the mismatch errors of the 15-level DAC capacitors.

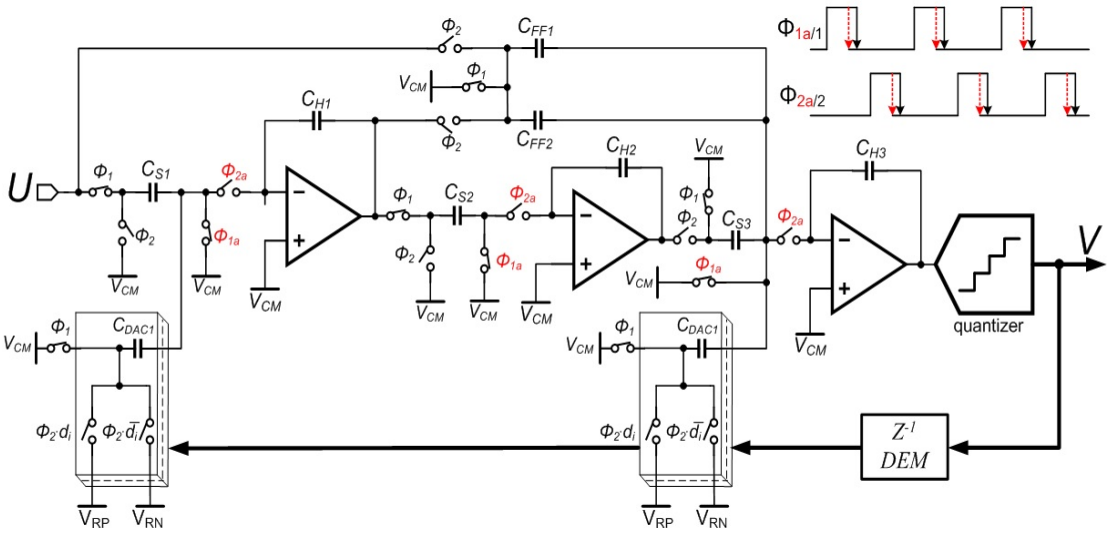


Figure 2.7: Single-ended SC circuit implementation of the proposed modulator with SLD of Figure 2.4.

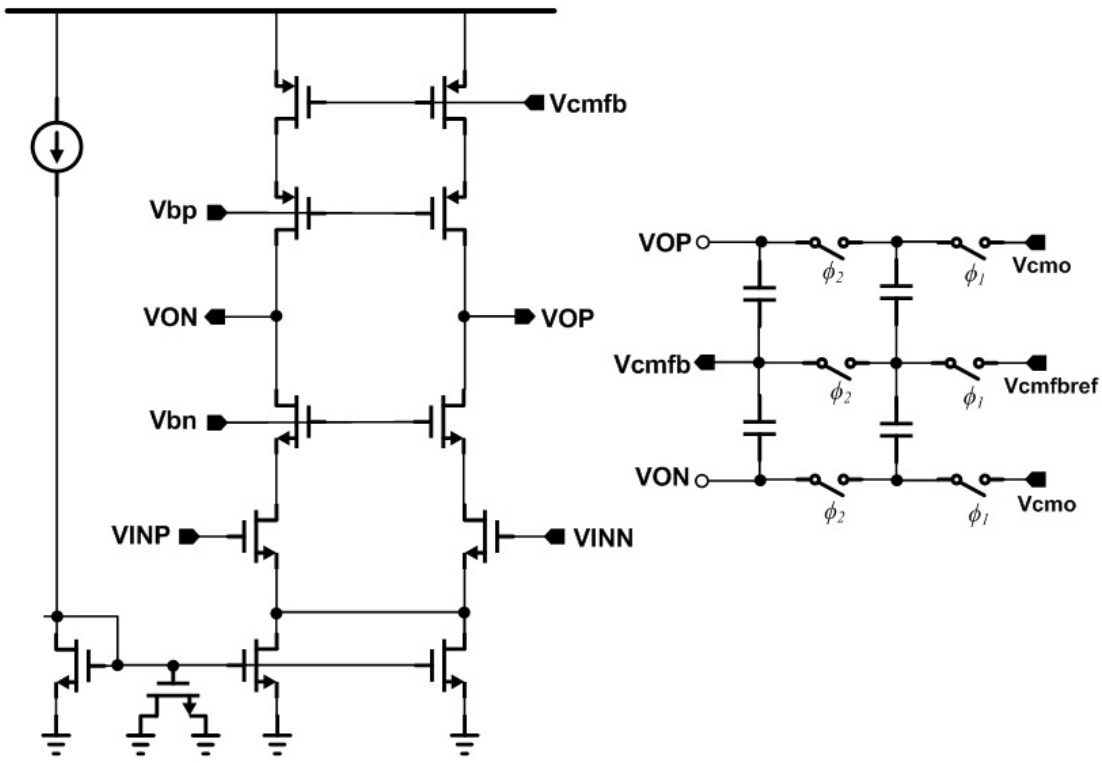


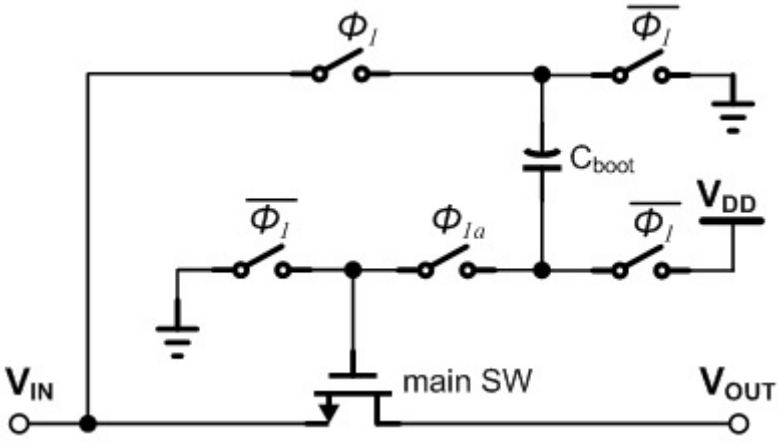
Figure 2.8: Telescopic cascode opamp with SC common-mode feedback.

Table 2.2: Simulated performance for the first integrator opamp

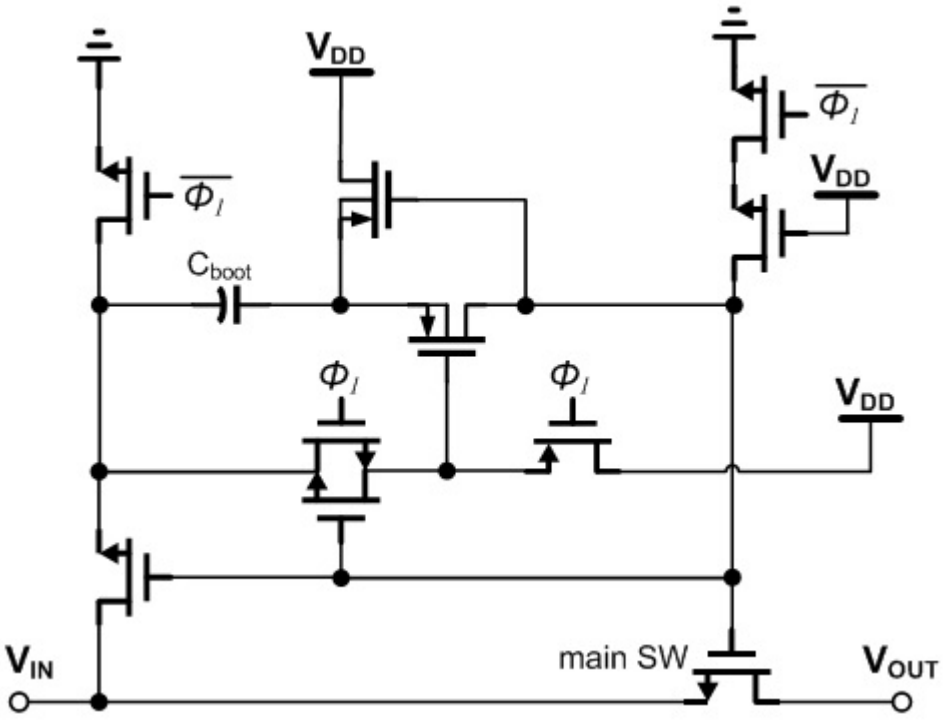
DC Gain	PM	UGBW	I_{TOT}	VDD	Process
55 dB	*65^o*	*1.25 GHz*	*2.0 mA*	*1.6 V*	*0.18 um*

The signal swings of the integrators in the loop filter are greatly reduced because of the low-distortion modulator architecture. The input swing of the last integrator is also highly reduced by the first-order noise shaping function to the input signal *U(z)*. Thus, a telescopic cascode opamp can be used to achieve a power-efficient low-noise integrator with a 1.6 V supply. The fully-differential output signal swing of the opamp is 1.48 Vpp. Power-efficient SC circuit is used to provide common-mode feedback voltage to the two top PMOS transistors. To minimize the noise contribution from two top PMOS transistors, their transconductances are designed much smaller than those of the input differential pair. The equivalent resistor R_{ds} of two top PMOS transistors are made larger to further suppress the noise comes from two cascode PMOS transistors. Figure 2.8 illustrates the telescopic cascode opamps in all integrators; Table 2.2 shows the simulated performance of the opamp in the first integrator. It achieves a DC gain of 55 dB to make the modulator gain error due to opamp finite gain lower than the thermal noise floor. To achieve the designed linearity, the unity gain bandwidth (UGBW) of the opamp is designed to 1.25 GHz to allow sufficient settling. It consumes 2.0 mA bais current with 1.6 V power supply. The opamps used in the second and third integrator are designed in the same structure but with scaled transistor size and current.

The sampling switches connected to the input signal are critical, because they limit the linearity of the modulator. To suppress the nonlinearity from charge injection and clock feedthrough, bootstrapped clock is used to ensure signal-independent sampling. Figure 2.9 shows the simplified diagram and the detailed circuit realization of the bootstrapped clock generator [10].



(a)



(b)

Figure 2.9: Bootstrapped clock generator (a) simplified diagram; (b) detailed circuit.

The 3.9 bits quantizer is realized by 14 comparators, based on thermometer coding. The comparator is composed of a preamplifier, a track-and-latch stage and a set-and-reset (SR) latch [11-12]. The block diagram is shown in Figure 2.10.

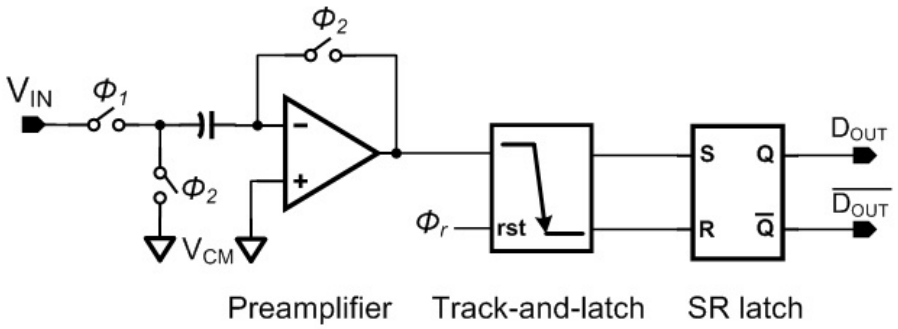


Figure 2.10: Comparator block diagram.

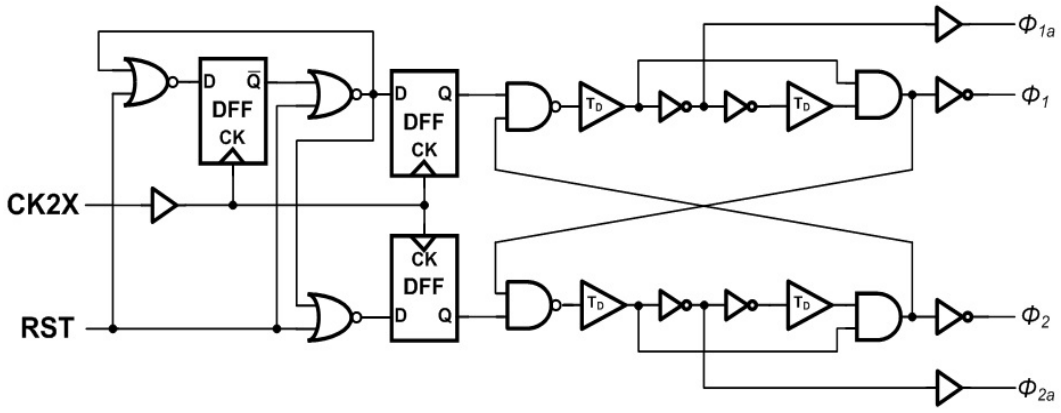


Figure 2.11: Clock generator diagram.

The gain of the preamplifier should not be too large; otherwise the time constants of the comparator are too large, which limits the speed, especially in track mode [13]. The preamplifier has an open loop gain of 12, and autozeroing technique is used to minimize the input-referred offset during Φ_2, which is reduced also by 12 [14]. During the phase Φ_1, the comparator works in the track mode and senses the output of the preamplifier. Before the end of phase Φ_1, the reset signal Φ_r locks the output of the track-and-latch stage and triggers the regeneration and SR latch. The speed of the quantizer is highly relaxed by the shifted loop delay, and hence the transistor sizes are easily to be optimized. The DWA logic is also working in the same time slot Φ_1, which means its speed requirement is also relaxed. Thus the transistor sizes of switches and digital blocks in DWA are also easily to satisfy the speed. Figure 2.11 illustrates the clock generator with on-chip dived-by-two circuit. It realizes 50% duty cycle and the advanced-cutoff clock.

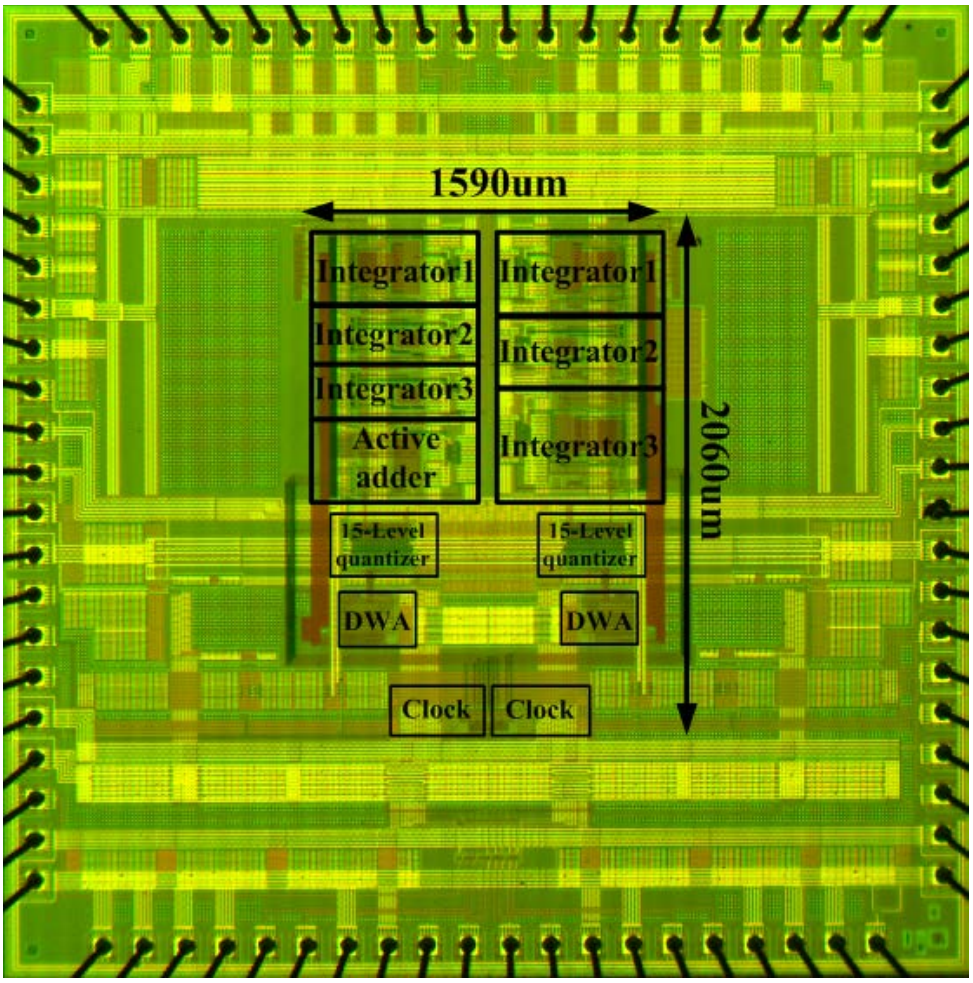


Figure 2.12: Chip micrograph for both modulators.

To verify the advantages of SLD structure, two ΔΣ ADCs were designed and fabricated in a 0.18 μm 2P4M CMOS process. The chip microphotograph is shown in Figure 2.12. The first modulator has a conventional low-distortion architecture, while the second one employs shifted loop delays. Both ADCs use a 1.6 V power supply for the analog circuitry, and a 1.55 V voltage for the digital circuit. The critical pins for input signals and analog bias voltages are at the top side; the power pins are at the corners at the top side; while the digital signal pins are at the bottom side. The die size is determined by the regulated pads. The core modulator area is only one fifth of the die area, while the empty area is filled with dummy metals and decoupling capacitors.

2.4. Measurement Results

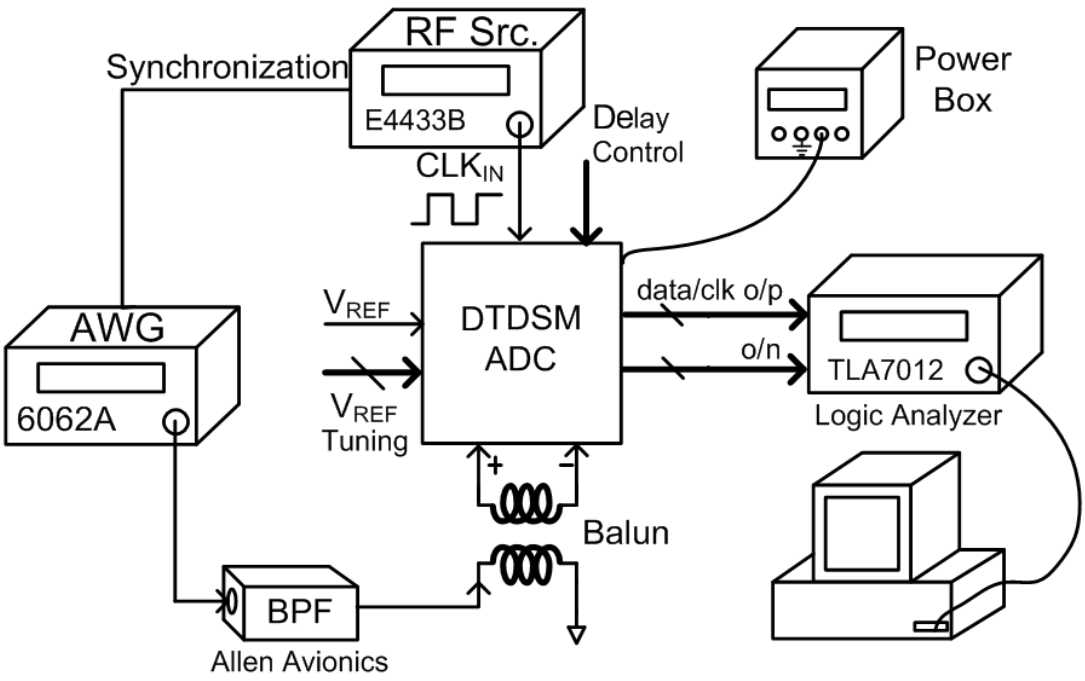


Figure 2.13: Test bench for chip measurement.

The test bench for chip measurement is shown in Figure 2.13. A single-tone sinewave input signal with frequencies from 10 kHz to 2 MHz is generated by AWG6062A. The single-ended signal is firstly filtered by a passive band pass filter, and then transformed to fully-differential signal by a passive balun. The sampling clock is generated by RF Src. E4433B. The bias current, input and output common voltages of all integrators are tunable on board, in order to get the best result by tweaking the opamps. The digital outputs and sampling clock of the chip are collected by Logic Analyzer TLA7012, then streamed to personal computer. The output data is analyzed by Matlab program. The power consumption is also be able to be measured on board. The test board setup is shown in Figure 2.14. In order to facilitate the setup of measurement, a corner detecting circuit is also implemented on chip. The test result in Figure 2.15 shows that all the chips in this tape-out shuttle are distributed between Slow-Fast and Slow-Slow corner.

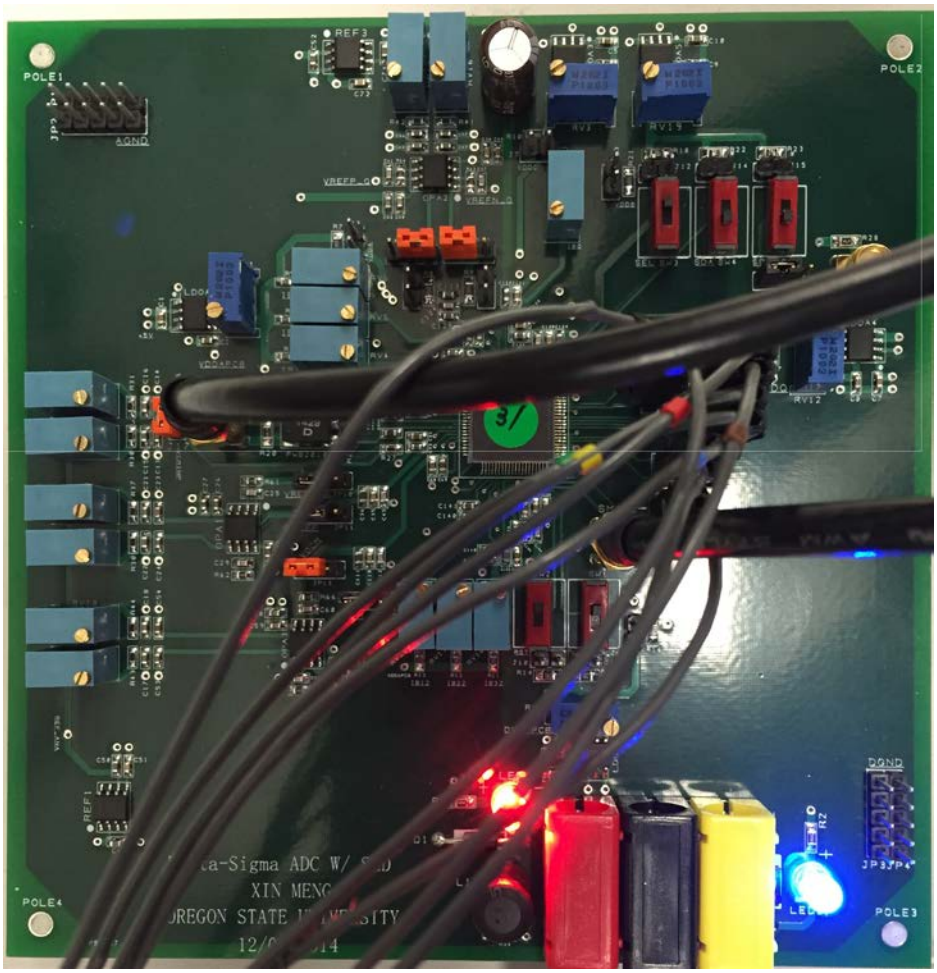


Figure 2.14: Test board for ADC measurement.

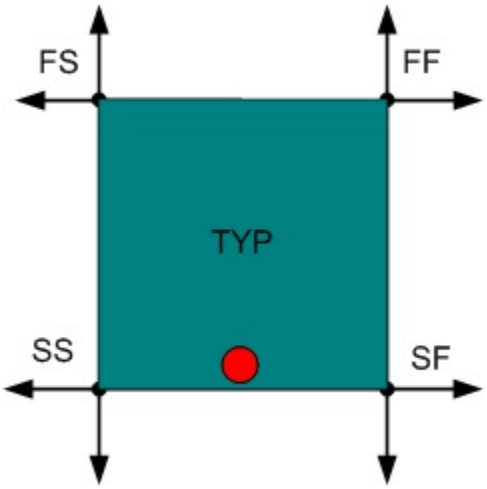


Figure 2.15: Chip corner.

When the conventional low-distortion ΔΣ modulator and the proposed ΔΣ modulator with SLD run as continuously-running modulators, the spectra of the output are as shown in Figure 2.16 and 2.17. Figure 2.16 shows the power spectral density of the conventional low-distortion ΔΣ modulator. The input signal is a 298.462 kHz sine wave with a -3.0 dBFS peak amplitude, and the clock frequency is 120 MHz. N=65536 points are sampled to get the power spectral density. The quantization noise with 60 dB/dec slope shows that a third-order noise shaping is achieved. After tweaking the bias currents and voltages, the peak SNDR can achieve 79.5 dB in a 4 MHz bandwidth, the THD is -87.2 dB, and the SFDR is 87.6 dB. The second harmonic (-90.6 dBFS) gives the largest distortion. The DC-offset is filtered by digital filter in Matlab code. The effective number of bits (ENOB) is 12.9 bits, calculated at ENOB = (SNDR – 1.76)/6.02. Figure 2.17 shows the measured results of the proposed ΔΣ modulator with SLD. The input signal is also a 298.462 kHz sine wave but with a -2.8 dBFS peak amplitude, and the clock frequency is 120 MHz. The quantization noise shaping function is obviously also a third-order with 60 dB/dec slope. After debugging, the peak SNDR can achieve 81.6 dB, the SFDR is 99.2 dB, and the THD is -95.6 dB. The DC-offset is filtered by digital filter in Matlab code. The effective number of bits (ENOB) is 13.3bits. The second harmonic (-102 dBFS) is also the largest distortion, which is much improved than the conventional low-distortion ΔΣ modulator. The harmonics come from the signal swings and the mismatch between the differential paths in the loop filter. Thanks to the extra feedback branch, signal swings and dynamic range (DR) of the proposed modulator are improved. Hence the second harmonic achieves 11.4 dB suppression than the conventional one. Figure 2.18 illustrates the SNR and SNDR variation with input signal power for both modulators. The conventional modulator achieves 80.8 dB DR over a 4 MHz signal bandwidth; while the proposed modulator with SLD achieves 81.8 dB DR. A single-ended input signal from 10 kHz to 2 MHz is obtained from a signal generator AWG6062A and bandpass filters. The single-ended input signal is converted into a fully-differential signal pair via an on-board balan. Figure 2.19 shows the SNDR with input signal frequencies variations.

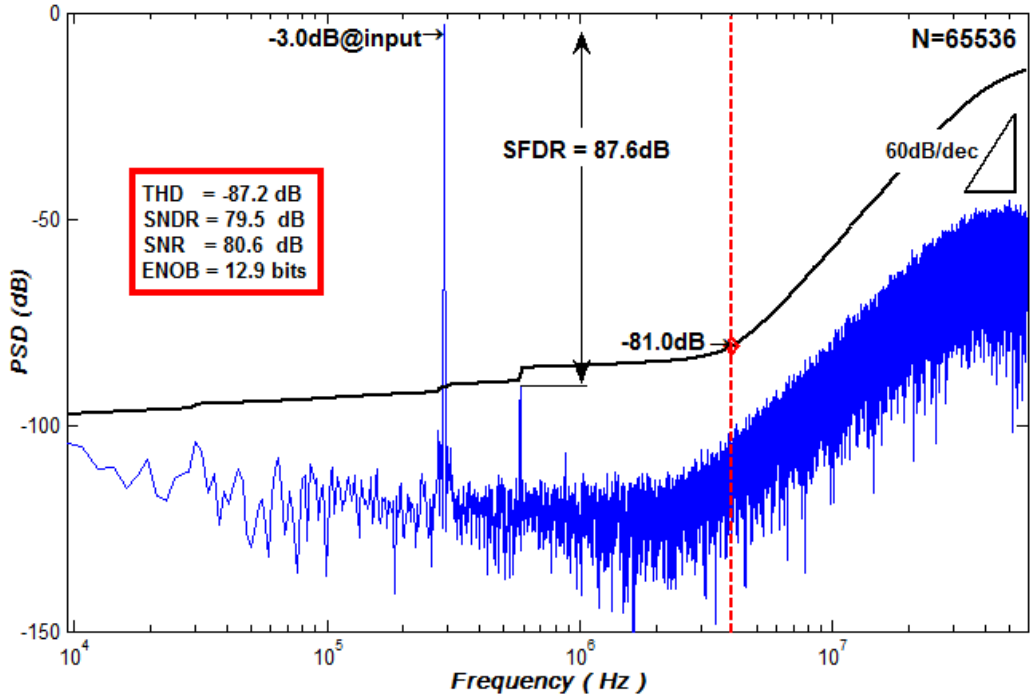


Figure 2.16: Measured spectrum at peak SNDR for the conventional ΔΣ modulator. The integrated noise PSD is shown in black.

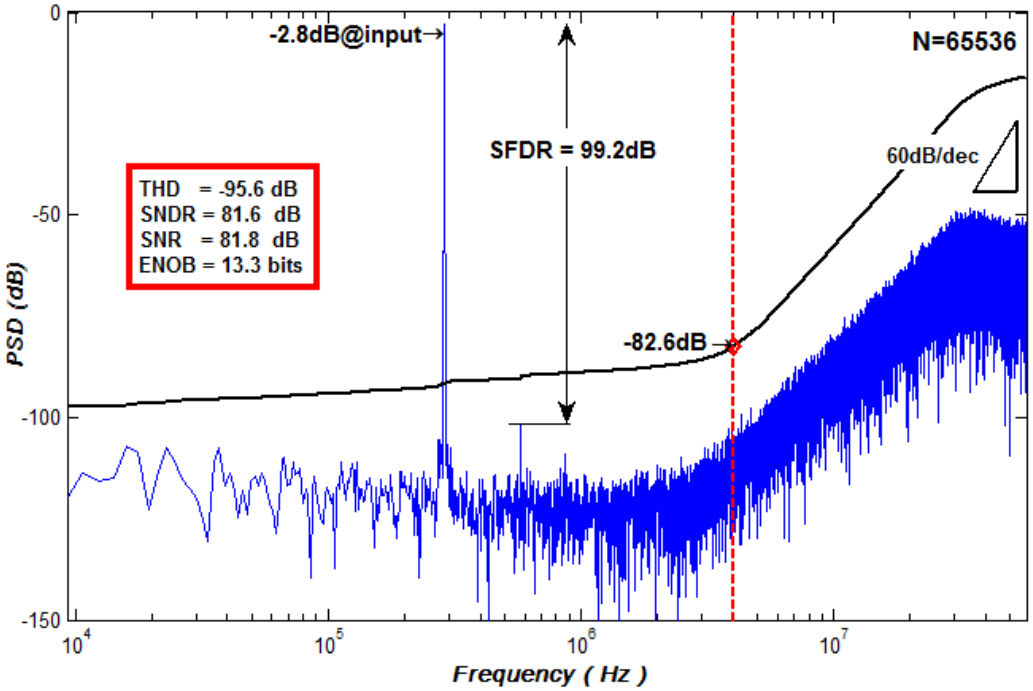


Figure 2.17: Measured spectrum at peak SNDR for ΔΣ modulator with SLD. The integrated noise PSD is shown in black.

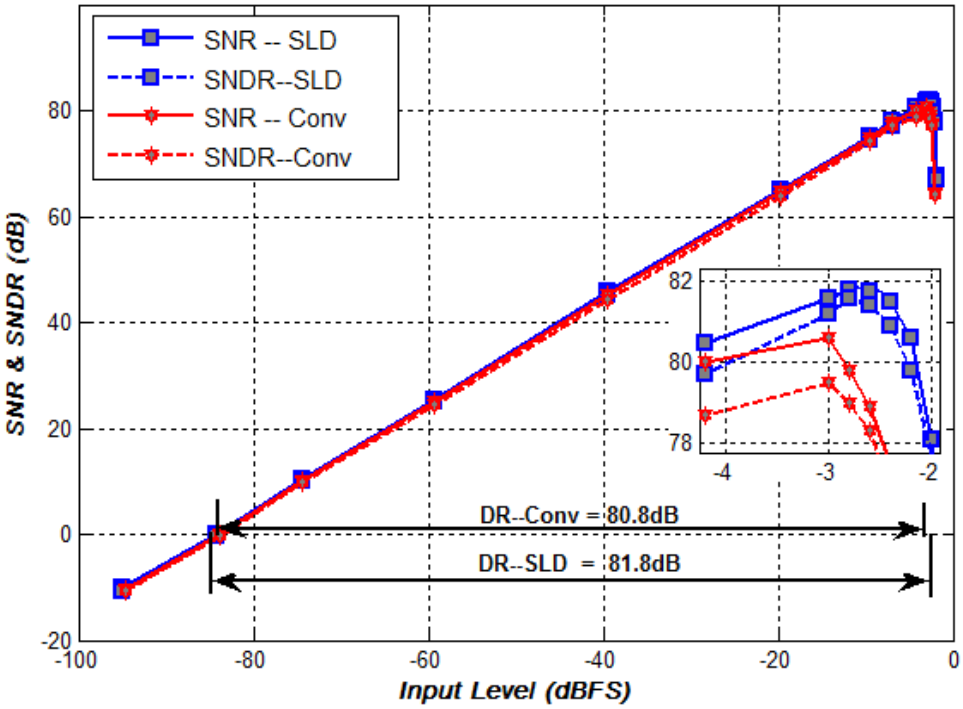


Figure 2.18: SNR and SNDR variations with input signal power.

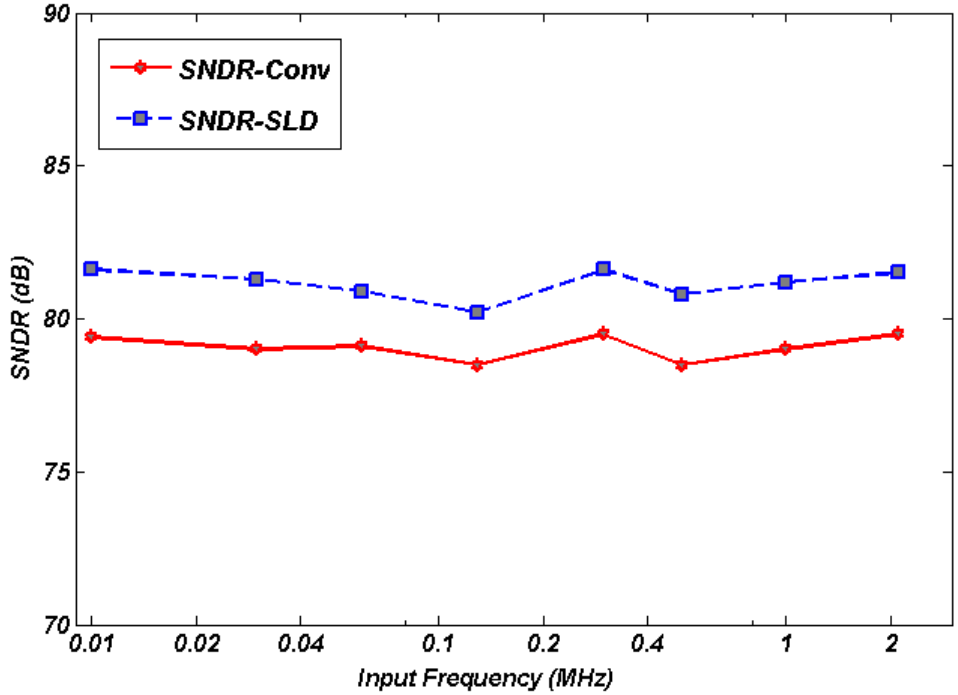


Figure 2.19: Measured SNDR variations with input signal frequency.

Table 2.3: Performance Summary of the SLD Versus Conventional ADCs

ADC	Conventional	SLD
Technology	*0.18 um 2P4M CMOS*	
Supply Voltage	*1.6 V (A), 1.55 V (D)*	
Clock Frequency	*120 MHz*	
Oversampling Ratio	*15*	
Signal Bandwidth	*4 MHz*	
Input Range (diff.)	*0.72 V*	
Dynamic Range	*80.8 dB*	*81.8 dB*
Peak SNDR	*79.5 dB*	*81.6 dB*
Peak SNR	*80.6 dB*	*81.8 dB*
SFDR	*87.6 dB*	*99.2 dB*
THD	*- 87.2 dB*	*- 95.6 dB*
Power Consumption	*24.9 mW*	*19.2 mW*
FOM	*0.41 pJ/conv-step*	*0.24 pJ/conv-step*

In the conventional modulator, the analog power is 13.2 mW and digital power is 11.7 mW, hence the figure-of-merit (FOM) is 0.41 pJ/conversion-step, while the proposed modulator with SLD consumes 8.78 mW analog power and 10.48 mW digital power, and its FOM is 0.24 pJ/conversion-step. The FOM is calculated from

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}} \tag{2.15}$$

The summary of the measured performances for both prototypes is shown in Table 2.3. In spite of the large output power of output buffers, the proposed ADC with SLD achieves 0.24 pJ/convention-step for 4 MHz signal bandwidth, which is almost 40% lower than the conventional ADC FOM. More detailed power breakdown is shown in Figure 2.20 (SLD only) and Table 2.4 (both modulators).

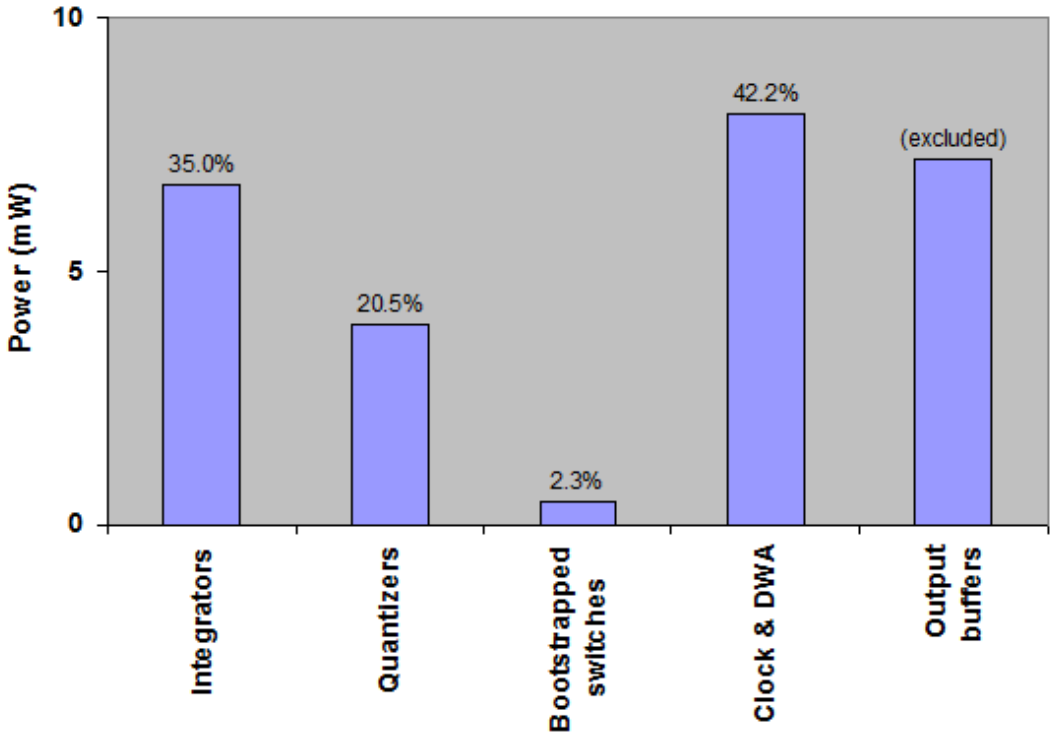


Figure 2.20: Power consumption breakdown for the proposed ADC with SLD.

Table 2.4: Performance Summary of the Conventional Versus SLD ADCs

ADC Power	Conventional (mW)	SLD (mW)
Integrator 1	*4.36*	*3.20*
Integrator 2	*0.64*	*0.51*
Integrator 3	*0.94*	*3.01*
Active adder	*5.26*	---
Quantizer	*3.94*	*3.94*
Bootstrapped switches	*0.43*	*0.43*
Clock & DWA	*9.33*	*8.11*
Output buffers	*7.19*	*7.19*

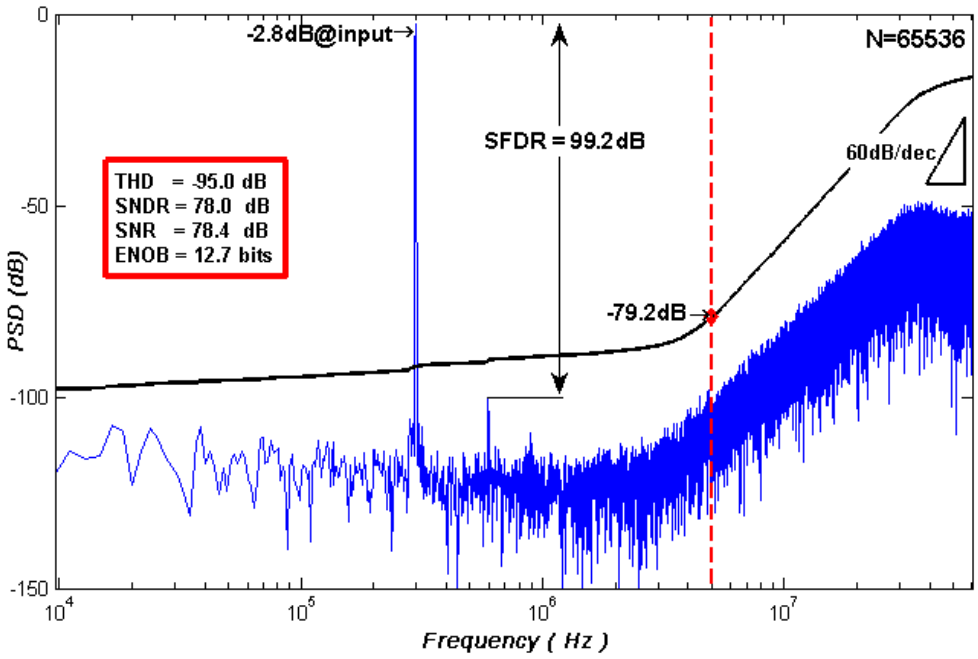


Figure 2.21: Measured spectrum at peak SNDR for ΔΣ modulator with SLD in 5 MHz bandwidth. The integrated noise PSD is shown in black.

Table 2.5: Performance Comparison With Other DT ΔΣ ADCs

Ref.	BW (MHz)	Power (mW)	SNDR (dB)	Process (um)	FOM (pJ/conv.)
[2]	*4*	*33.4*	*70.1*	*0.18*	*1.64*
[3]	*4*	*27.5*	*77.3*	*0.18*	*0.58*
[4]	*4*	*8.0*	*59.1*	*0.09*	*1.38*
[8]	*4.2*	*28*	*79*	*0.18*	*0.48*
[15]	*5*	*13.6*	*70.9*	*0.13*	*0.47*
[16]	*5*	*16*	*75.7*	*0.13*	*0.32*
This Work	*4*	*19.2*	*81.6*	*0.18*	*0.24*
	5	*19.2*	*78.0*	*0.18*	*0.30*

Figure 2.21 shows the measured spectrum for the proposed ADC with SLD in 5 MHz bandwidth. Table 2.5 compares the performance of the proposed ADC with state-of-the-art DT ΔΣ ADCs having bandwidths of 4-5 MHz. The proposed ADC with SLD is among the best reported for either 4 or 5 MHz discrete-time ADCs.

2.5. Summary

Two low-distortion third-order ΔΣ modulators were implemented. Compared to a conventional ΔΣ ADC, the proposed ADC with shifted loop delays can use a shifted delay to compensate the loop filter delay, hence relax the speed requirements of not only the quantizer and the block, but also the integrators in the loop filter. It eliminates the last stage adder and uses one extra feedback branch to make the STF be equal to unity. Finally, the proposed ADC with shifted loop delays could preserve the low-distortion property and optimize the stability, dynamic range and power consumption.

Compared to a conventional ΔΣ ADC, the proposed ADC with shifted loop delays achieved much better performance while saving 38% of the analog power. The measurement results of the prototype demonstrated excellent performance, and verified the power efficiency of the shifted loop delay architecture.

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CHAPTER 3 . NOISE SHAPING ENHANCED DELTA-SIGMA ADCs WITH SHIFTED LOOP DELAYS

Noise coupling and time interleaving are effective methods for expanding the signal bandwidth in the low-power wideband delta-sigma (ΔΣ) ADCs. In this chapter, two discrete-time ΔΣ modulator topologies combined with shifted loop delays (SLD), are proposed. One is based on a self-noise-coupled low-distortion structure; the other one is a noise-coupled time-interleaved ΔΣ modulator. Both architectures use shifted loop delays to relax the critical timing constraints in the modulator loop filter. To verify the effectiveness, both ΔΣ modulators were analyzed and simulated in a 0.18um CMOS technology.

3.1. Introduction

With increasing speed in wireless communication and portable electronics, high-resolution, low-power delta-sigma (ΔΣ) ADCs are required to achieve wider bandwidth. The feed-forward structure with low-distortion technique [1] is highly effective in wideband realization. Also, it achieves high accuracy by suppressing the input signal component and distortion in the loop filter. The dynamic requirements for all integrators are even more relaxed when the quantizer is multi-bit. The operational transconductance amplifiers (OTAs) have reduced design requirements of slewing and settling, and thus consume less power dissipation.

A drawback of the low-distortion architecture is that the adder needs to combine the signals of all feed-forward paths (Figure 3.1), either in a passive or active circuit. Although the passive summation does not need an extra OTA, the signal swing and the quantizer input steps are attenuated due to the parasitics. Also, mismatch effects and kick-back noise from the quantizer impair the performance of the modulator [2]. An active adder can achieve more accurate summation; however, it requires a fast power-hungry OTA. Thus, *Nth* order noise shaping modulator need *N+1* OTAs.

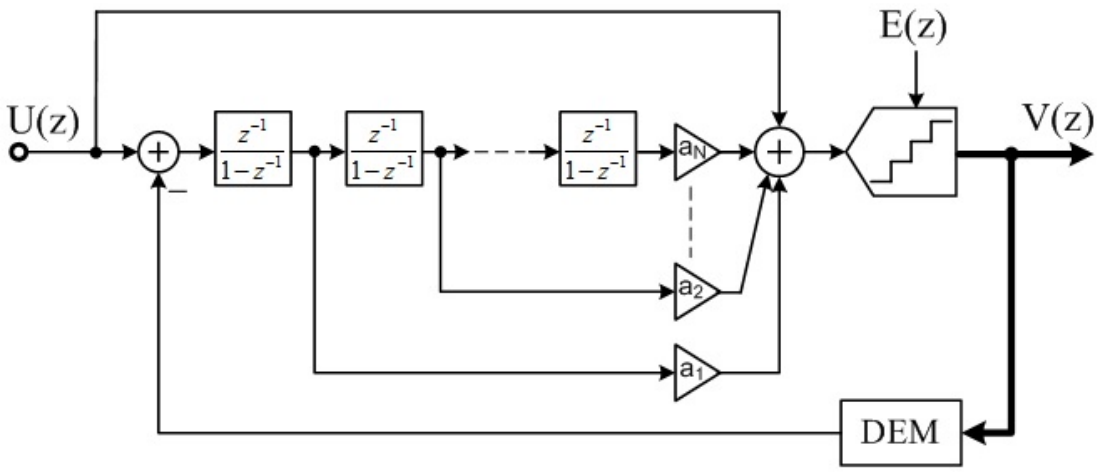


Figure 3.1: Feed-forward low-distortion ΔΣ ADC.

Noise shaping enhancement techniques such as noise coupling [2], VCO-based quantizer [3] and dual-slope quantizer [4] were used to compensate the extra OTA by increasing the order of the noise transfer function (NTF) in system level design. To further save power, charge-pump based integrators [5] and charge compensation [6] were suggested to relax the slew rate and settling requirements of the OTAs. However, the drawback of all these techniques is the critical timing required for the quantization and the dynamic element matching (DEM) circuitry [7]-[8]. The stability of the loop requires that the quantizer and the DEM operate in the non-overlapping clock intervals. This increases the power consumption in both OTAs and digital blocks. These issues become even more challenging with increased signal bandwidth.

To relax the timing restrictions, extra loop delay can be introduced in the feedback path [9]-[10]. However, this additional delay has to be compensated by extra feedback and feed-forward branches (Figure 3.2) to prevent instability [11]-[12]. Also, to keep the low-distortion property, additional delay should be injected in the signal path, which makes the timing in the input of the modulator more complex. Furthermore, this architecture cannot utilize noise shaping enhancement techniques, which means thus $N + 1$ OTAs are still required to achieve N^{th}-order noise shaping function, the same as the conventional low-distortion architecture.

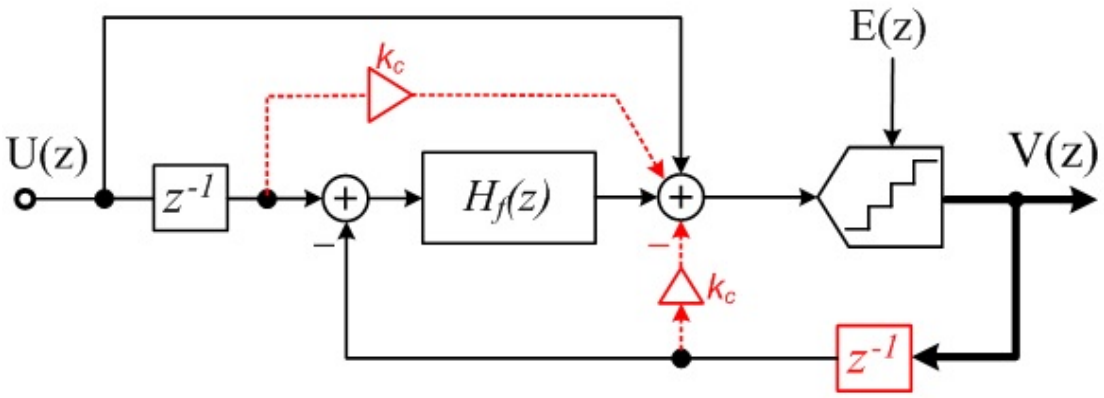


Figure 3.2: Low-distortion ΔΣ ADC with extra loop delays [12].

In this chapter, noise shaping enhancement techniques combined with shifted loop delays (SLD) are described. These structure shifts the loop delay from the last integrator to the feedback path, in order to relax the critical timing needed for the DEM logic. The active summation is achieved also by the last integrator, saving one OTA in the loop filter, which means that only *N* OTAs only required to achieve N^{th}-order noise shaping function. This chapter is organized as follows. Section 3.2 describes the proposed self-noise-coupled ΔΣ ADC with shifted loop delays. The proposed noise-coupled time-interleaved modulator architecture with shifted loop delays is described in section 3.3. Finally, Section 3.4 draws the summary.

3.2. Self-Noise-Coupled ΔΣ ADC with SLD

3.2.1 Architecture Considerations

Noise coupling is a power-efficient approach in wideband ΔΣ ADCs design. It boosts the noise shaping performance without requiring an extra integrator. As Figure 3.3 shows, noise coupling is achieved by delaying the quantization noise by one clock period delay, and injecting it into the summing node before the quantizer [2]. It effectively increases the modulator order of noise transfer function from N to N+1 without changing the signal transfer function. However, the extra OTA is indispensable because of the active addition and virtual ground. Additionally, the quantization noise works as a dither signal, thus it helps to reduce idle tone and harmonic spurs, and improves the modulator linearity [2].

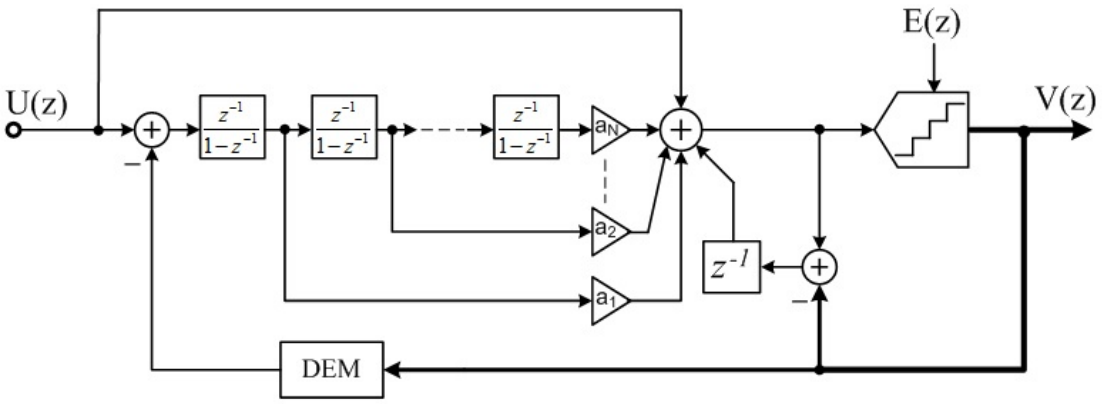


Figure 3.3: Block diagram of the low-distortion self noise-coupled ΔΣ ADC.

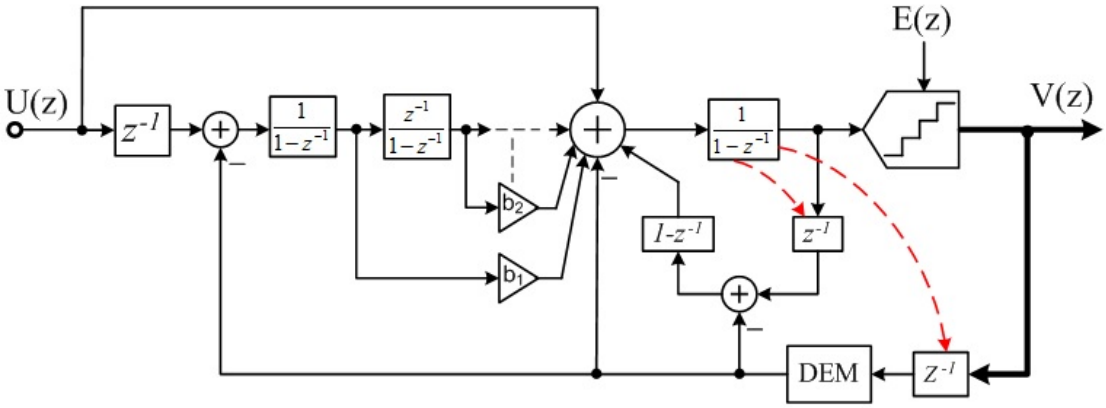


Figure 3.4: Low-distortion self noise-coupled ΔΣ ADC with shifted loop delays.

The shifted loop delays technique, which is introduced in chapter 2, can also be utilized in ΔΣ modulators combined with the self noise coupling technique. The stabilized ΔΣ ADC with shifted loop delays is illustrated in Figure 3.4. The proposed architecture shifts the loop delay from the last integrator to two feedback paths. One is the noise coupling branch to generate the extra noise shaping; the other one is the feedback branch to relax the timing restricts for DEM logic. Since the feed-forward and feedback signals are added at the input of the last delay-free integrator, the delayed coupling signal should be multiplied by $(1 - z^{-1})$. The drawback of this architecture is also the cascaded delay-free integrators, which burn more power to achieve the same linearity.

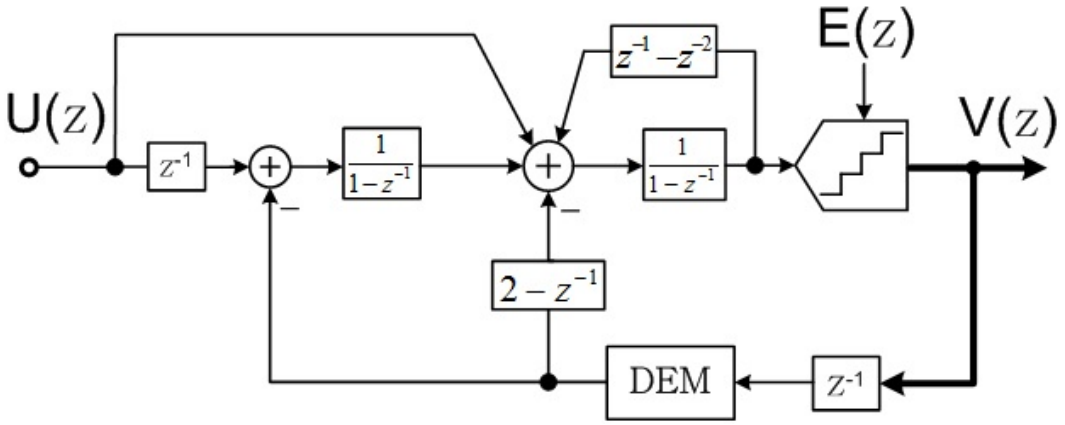


Figure 3.5: Low-distortion noise-coupled ΔΣ ADC with shifted loop delays [13].

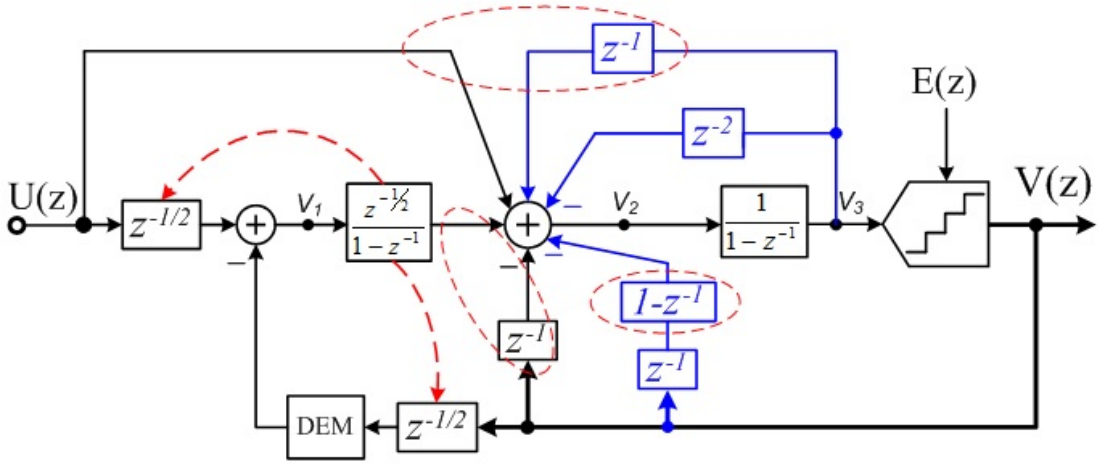


Figure 3.6: Improved noise-coupled ΔΣ ADC with shifted loop delays.

As discussed, noise coupling can be used to enhance the order of the noise shaping function. A third-order noise-coupled realization is shown in Figure 3.5 [13]. To save power and area, shared capacitors (in dashed circles) are used in an improved low-distortion noise-coupled ΔΣ ADC topology with shifted loop delays (Figure 3.6) [14]. This structure shifts the half clock period delay of the first integrator into the feedback and input signal paths. The half clock delay in the feedback path allows DEM logic operation. While the half clock delay in the input signal path helps to synchronize the signal components between direct input and feedback paths, and hence preserves the low-distortion property. Also, this modulator shifts one clock delay from the last integrator into the extra feedback branch to stabilize the loop. The proposed modulator also uses the last integrator to realize active summation. Three

capacitors can be shared in the last integrator. Hence, the feedback factor and the power consumption of the second OTA is further improved.

Linear analysis of the modulator in Figure 3.6 gives

$$STF = 1 \tag{3.1}$$

$$NTF = (1 - z^{-1})^3 \tag{3.2}$$

$$V_1(z) = -z^{-1/2}(1 - z^{-1})^3 E(z) \tag{3.3}$$

$$V_2(z) = (1 - z^{-1})U(z) - z^{-1}(1 - z^{-1})(2 - z^{-1})E(z) \tag{3.4}$$

Here, *E(z)* is the quantization error of the internal quantizer. Equation (3.3) shows that the loop filter only needs to process the shaped quantization error, and the proposed modulator topology thus remains the low-distortion architecture.

3.2.2 SC Circuit Implementation

Figure 3.6 is easily implemented by using switched-capacitor circuits. As discussed in chapter 2, the most sensitive operation in discrete-time modulators happens at the input of the first integrator. The SC circuit implementation of the first integrator is shown in Figure 3.7. It operates in three steps: step 1, the input signal *U(n-1)* is sampled at the end of clock phase Φ_1, transferred to the hold capacitor C_H in phase Φ_2 as *Vo(n-1/2);* step 2, during the clock phase Φ_2, the feedback DAC capacitors are refreshed to common-mode voltage V_{CM}, and the quantization and DEM can be operated; step 3, in the next Φ_1, the new DAC voltage is transferred to the integrator output to generate $V_1(n)$. Thus the feedback DAC signal is one clock delay than the input signal.

Clock phases Φ_1 and Φ_2 are non-overlapping. In the first integrator, the signal path works in delayed mode, while the DAC branches work in delay-free operation. Compared to double sampling realization in [15], this integrator eliminates the path mismatch and avoids the interferers around $F_S/2$. In the SC circuits implementation, the input sampling capacitor and the feedback DAC capacitors are separated to avoid the quantization noise coupling back to the signal path and to mitigate the signal dependent DAC reference noise.

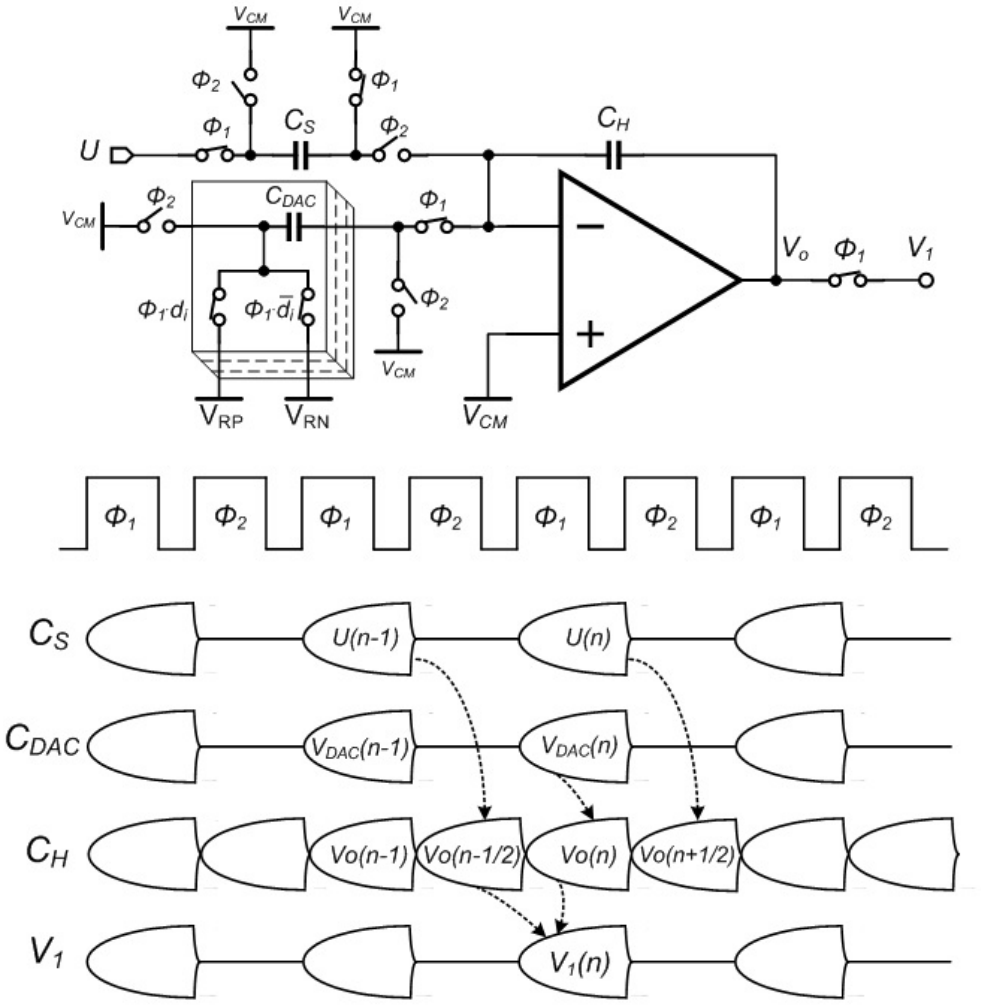


Figure 3.7: SC implementation of the first integrator in the proposed modulator.

Figure 3.8 illustrates the single-ended circuit diagram of the proposed ΔΣ ADC in Figure 3.6 and the clock signals. Shared capacitors are used in the last integrator to alleviate the reduction of the feedback factor. The negative coefficient is easily implemented by crossing the paths in the fully-differential circuits. The design of the z^{-2} delay is implemented in the dashed box. It operates for three steps: step 1, at the falling edge of Φ_{2e}, the adder's output is sampled to C_{F3} in the top path; step 2, this charge is holded for Φ_{1o} and Φ_{2o}; step 3, in phase Φ_{1e}, the charge will be transferred to the adder input. The bottom path is also works the same operation, but is sampled at Φ_{2o} and transferred at Φ_{1o}.

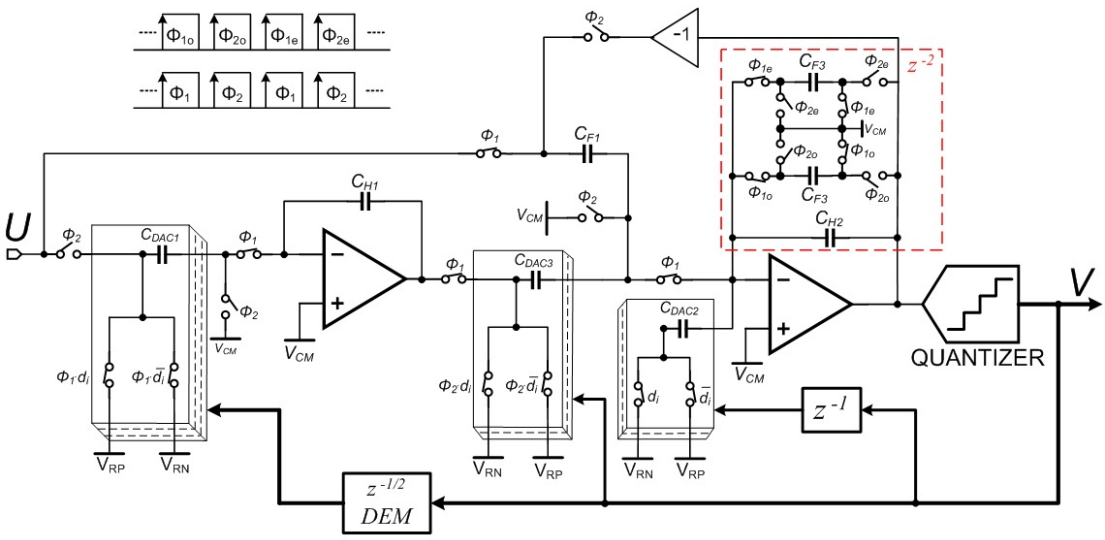


Figure 3.8: Single-ended circuit diagram of proposed self-noise-coupled low-distortion ΔΣ ADC with shifted loop delays.

3.2.3 Simulation Results

A comparison with a conventional noise-coupled ΔΣ ADC was made using MATLAB SIMULINK simulation. A conventional third-order noise-couple ΔΣ ADC can be easily generated as in Figure 3.3. It has to allocate a non-overlapping time slot to DEM; while the proposed SLD modulator can use the shifted loop delays to operate DEM. To verify the effectiveness of shifted loop delays, two ΔΣ ADCs with OSR = 16, 15-level quantizer and 160 MHz sampling frequency were designed. The conventional modulator requires 3 OTAs, while the proposed modulator with shifted loop delay utilizes only 2 OTAs.

The comparison results are shown in Table 3.1. The proposed modulator with shifted loop delays can have 33% more time to settle OTAs, and has 7.05 dB less input swing in the last OTA. This allows dynamic relaxation of the OTA. However, the drawback of shifted loop delay is that in cascaded delay-free integrators there is 21% slower settling for the second integrator (discussed in the Appendix). Overall, the necessary unity gain bandwidth of the last OTA in the proposed modulator with shifted loop delay is 38% less than the conventional noise-coupled modulator.

Table 3.1 Comparison Between Noise-Coupled ΔΣ ADCs W/ and W/O SLD

	Specification	Fig.5	Fig.10
System timing	*Settling time*	*2nS*	*2.95nS*
	Quantization	*0.25nS*	*0.25nS*
	DEM	*0.7nS*	*2.7nS*
Last OTA	*Feedback Factor*	*1/7*	*1/5*
	Input Swing	*-0.05dBFS*	*-7.10dBFS*
	Output Swing	*-0.05dBFS*	*-0.07dBFS*

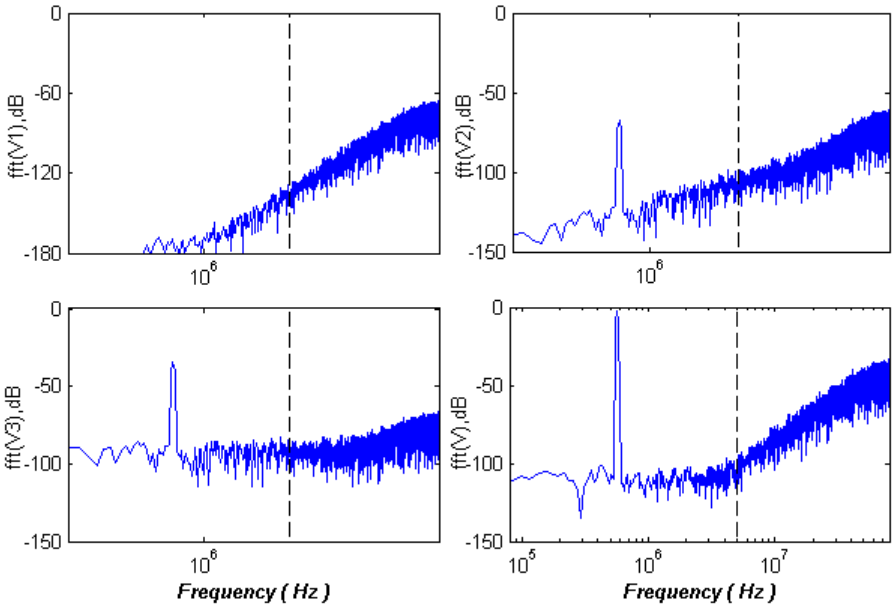


Figure 3.9: Simulated spectra of the node voltages of the circuit of Figure 3.6.

MATLAB SIMULINK simulation was used to verify the low-distortion property. Figure 3.9 shows the power spectral densities (PSDs) of V1, V2, V3 and V of the circuit of Figure 3.6. The results show that there is no signal component in V1, so that the modulator obviously retains the low-distortion property. The signal component in V2 is noise shaped, which relaxes the slew rate and settling requirement of the last OTA. Finally, the digital output V shows the modulator can also achieve a third-order noise shaping.

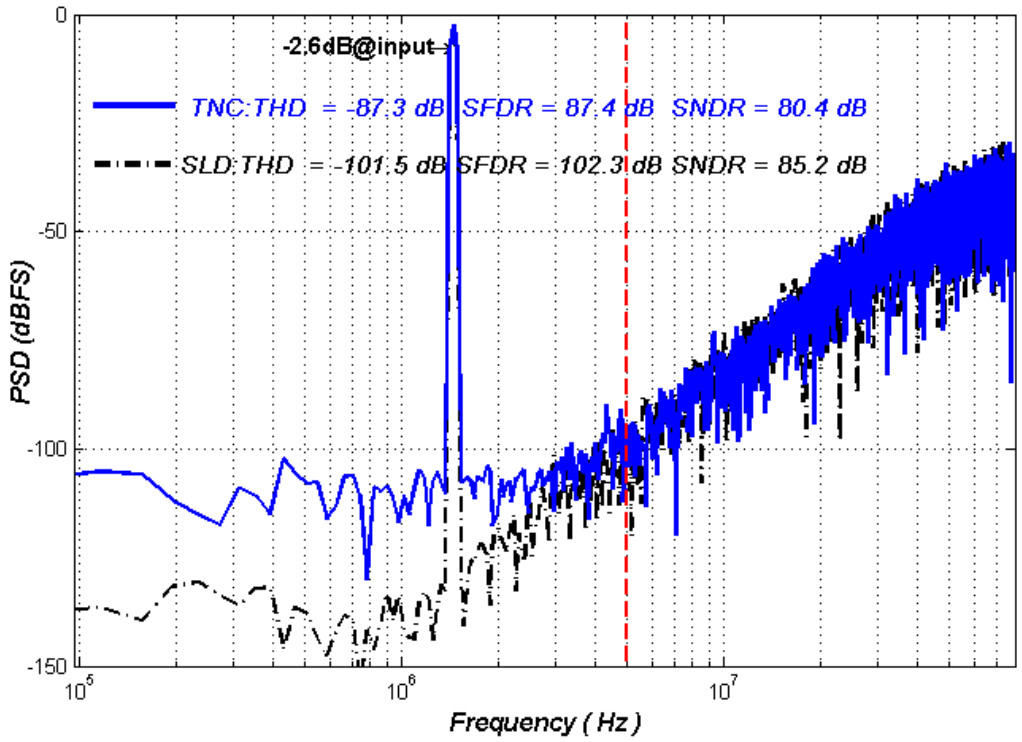


Figure 3.10: PSD of the output signal of the two ΔΣ ADCs W/ and W/O SLD.

The switched-capacitor implementation of Figure 3.6 was simulated in Cadence SPECTRE. The OTAs were modeled on the transistor level; the other blocks were simulated with operation models. A conventional noise-coupled modulator with the same OTAs' settling was also simulated to make the comparison, which has one more OTA to realize the same order of noise shaping.

In the transient simulation, the input signal is 0.72 Vpp, thus no slewing is required for the telescopic OTAs when a 1.8V supply voltage is used. Simulation results (Figure 3.10) show that with the same settling capacity in the OTAs, the proposed modulator could achieve 85.2 dB SNDR, 4.8 dB more than the conventional modulator. The THD was equal to -101.50 dB, 14.2 dB better. The SFDR was 102.3 dB, 14.9 dB more than for the conventional modulator. The noise floor was 20 dB improvement because of the better settling in all integrators.

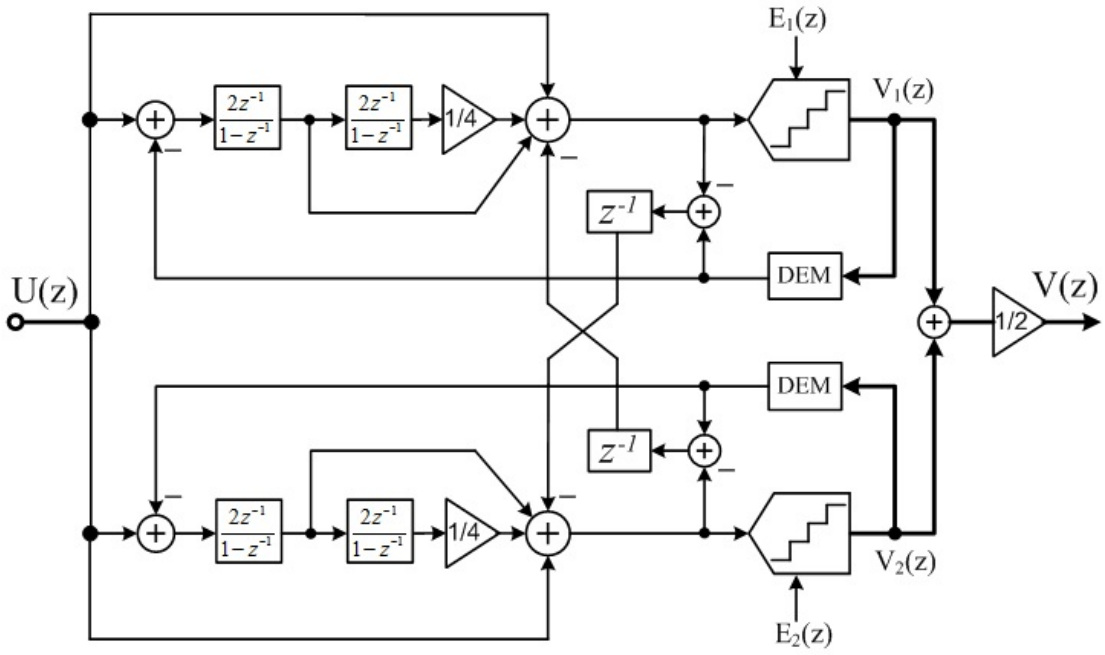
3.3. Noise-Coupled Time-Interleaved ΔΣ ADC with SLD

This section describes an effective wideband high-linearity ΔΣ ADC. It uses noise coupling, and time interleaving combined with shifting loop delays technique. A two-channel noise-coupled time-interleaved ΔΣ ADC with shifted loop delays was simulated in a 0.18um CMOS technology. Noise coupling between the channels increases the effective order of the noise-shaping function. Time interleaving enhances the effects of noise coupling by 6 dB. Shifted loop delays technique relaxes the time restricts on DEM.

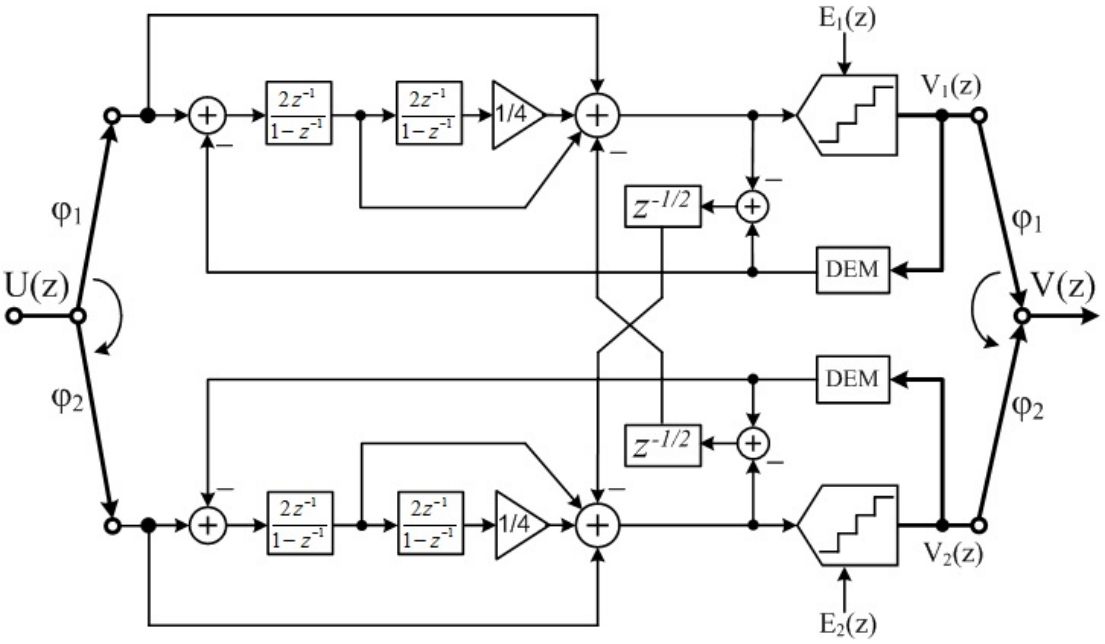
3.3.1 Architecture Considerations

The derivation of the noise-coupled time-interleaved architecture is presented in [16]. In noise-coupled split modulator architecture, as shown in Figure 3.11(a), noise coupling between two ΔΣ modulators enhances the original NTF by an additional factor $(1 - z^{-1})$ without extra overhead [17-18]. In each modulator, all capacitances and transconductances are cut in half. Both the thermal and quantization noise are doubled; however, the signal-to-noise ratio (SNR) keeps the same because the output signal power also doubles. Time-interleaving [19-20] adds further performance improvement. Figure 3.11(b) illustrates the resulting noise-coupled time-interleaved (NCTI) modulator [20]. Time interleaving changes the enhanced noise shaping factor from $(1 - z^{-1})$ to $(1 - z^{-1/2})$, Because $1-z^{-1/2} \approx (1-z^{-1})/2$ at very low frequency and dc, time interleaving gives an additional 6 dB improvement in the signal-to-quantization noise ratio (SQNR) when over-sampling the signal. The channel mismatch errors will be suppressed around the Nyquist frequency due to the noise shaping function.

However, these topologies require critical timing. Extra time in the non-overlapping slot required for the quantizer and DEM operation shortens the available processing time for the OTA slewing and settling, which increases power consumption of the whole loop filter. Another unfavourable issue is the power hungry active adder, which needs to perform the accurate active summation at the input of the quantizer.



(a)



(b)

Figure 3.11: (a) noise-coupled split modulator; (b) noise-coupled time-interleaved (NCTI) modulator.

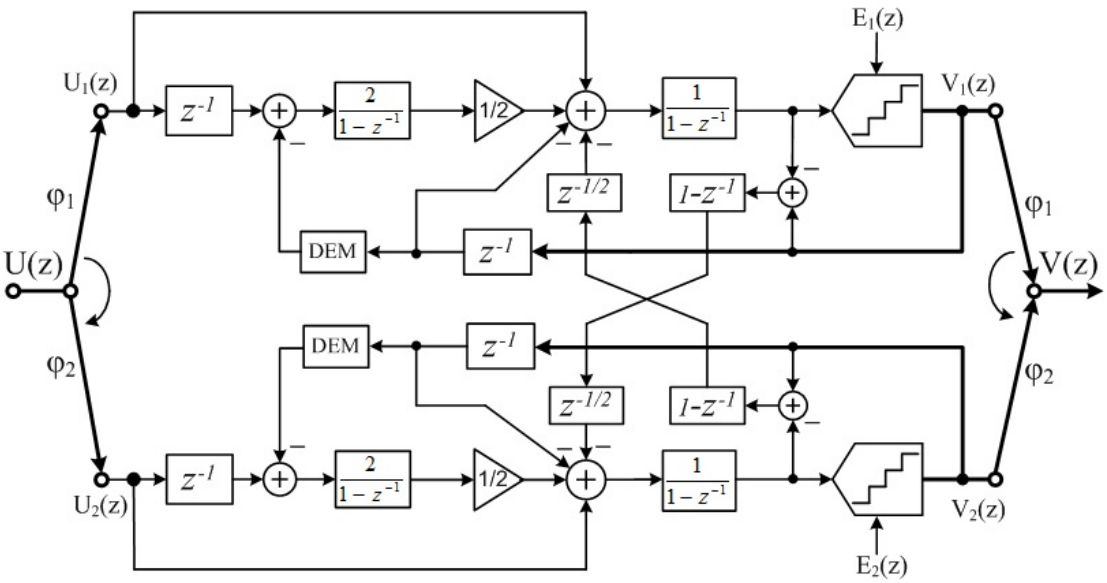


Figure 3.12: The proposed low-distortion noise-coupled time-interleaved (NCTI) ΔΣ ADC with shifted loop delays.

To solve these problems, shifted loop delays can be used to improve the noise-coupled time-interleaved low-distortion ΔΣ modulator, as shown in Figure 3.12 [21]. The proposed structure cross-couples the quantization error between the two loops to give the enhanced noise shaping function of $1 - z^{-1/2}$. However, compared to Figure 3.11(b), the cross-coupled paths have to utilize one more $1 - z^{-1}$ branch to compensate the third integrator. Fortunately, such a branch is easily realized by unswitched capacitor. Shifting the loop delay from the last integrator to the feedback path relaxes the critical timing needed for the DEM logic. One extra branch is used as feedback to the last integrator, which makes the STF be equal to unity when combined with the feed-forward branch. By relocating one clock period delay in both signal and feedback paths, the input and the feedback signal can be synchronized and cancelled, which allows the loop filter to process only the quantization error. Therefore, the low-distortion property is preserved. The active summation is achieved by the last integrator. This saves one OTA compared to Figure 3.11(b).

The input signal U(z) switches between two loops. $U_2(z)$ has a half clock delay with respect to $U_1(z)$, and $V_2(z)$ has half clock delay with regard to $V_1(z)$. Linear analysis of the proposed modulator in Figure 3.12 gives the equations.

$$V_1(z) = U_1(z) + NTF_1 \cdot [E_1(z) - z^{-1}E_2(z)] \tag{3.5}$$

$$V_2(z) = U_2(z) + NTF_2 \cdot [E_2(z) - E_1(z)] \tag{3.6}$$

The noise transfer functions are the same:

$$NTF_1 = NTF_2 = (1 - z^{-1})^2 \tag{3.7}$$

On the top level, the equations are

$$U(z) = U_1(z) + z^{-1/2}U_2(z) \tag{3.8}$$

$$V(z) = V_1(z) + z^{-1/2}V_2(z) \tag{3.9}$$

$$E(z) = E_1(z) + z^{-1/2}E_2(z) \tag{3.10}$$

Combining all these equations, we get

$$V(z) = U(z) + (1 - z^{-1})^2(1 - z^{-1/2})E(z) \tag{3.11}$$

Since U_1 and U_2 are strongly correlated, when OSR = 12 (the value used in this section), equation (3.8) gives

$$U(z) = U_1(z) + z^{-1/2}U_2(z) \approx 2U_1(z) \tag{3.12}$$

For the same signal power as in the modulators in Figure 3.11(b), the signals in equation (3.11) will be scaled by a factor of 1/2:

$$\frac{V(z)}{2} \approx \frac{U(z)}{2} + \frac{(1 - z^{-1})^2(1 - z^{-1/2})[E_1(z) + z^{-1/2}E_2(z)]}{2} \tag{3.13}$$

Since $E_1(z)$ and $E_2(z)$ are uncorrelated, $[\, E_1(z) + z^{-1/2} E_2(z) \,]/2$ gives almost the same power as $[\, E_1(z) + E_2(z) \,]/2$. Thus the enhancement factor of $(1 - z^{-1/2})$ does not depend on the correlation or equality of $E_1(z)$ and $E_2(z)$.

Unlike in Figure 3.11(b), the cross-coupled paths in the proposed structure are not filtered by DEM. The mismatch between the DACs in the cross-coupled paths is filtered only by the loop filter. In fact, the noise shaping factor of $(1 - z^{-1})(1 - z^{-1/2})$ filters out noise better than the DEM.

The drawback of this architecture is the same as that of Figure 3.6. Two delay-free integrators are cascaded, which results in slower settling for the second integrator. Analysis and simulation in Appendix show that for a 0.1% permissible settling error the second integrator needs about 21% more power than it would in a cascade of two delayed integrators.

3.3.2 SC Circuit Implementation

The system of Figure 3.12 can be easily realized using switched-capacitor circuits. The single-ended circuit diagram is shown in Figure 3.13. The most sensitive operation also takes place at the input of the first integrator. Shifting one clock delay from the first integrator to the input signal path is easily realized by holding one clock phase [13] or double sampling [15] on the transistor level. The delay in the input signal path helps to preserve the low-distortion property, as discussed in section 3.3.1. The cross-coupled paths require a function of $1 - z^{-1}$, which can be realized by unswitched capacitors. The half clock delay in the cross-coupled paths is initially achieved by the delay between the two loops. Shared capacitors are used in the feed-forward and feedback paths of the last integrator to increase the feedback factor. The negative coefficient is easily implemented by switching the reference voltages.

3.3.3 Simulation Results

A noise-coupled time-interleaved ΔΣ ADC of Figure 3.11(b) has to allocate a non-overlapping time slot to DEM, while the proposed NCTI modulator can use the shifted loop delay to operate DEM. To verify the effectiveness of relaxing timing, the third-order ΔΣ ADCs in Figures 3.11(b) and 3.12 are compared in Table 3.2.

Two ΔΣ ADCs with OSR = 12, 15-level quantizer and 120 MHz sampling frequency were simulated in MATLAB SIMULINK. Figure 3.11(b) requires six OTAs, while the proposed modulator with shifted loop delays needs only four. The OTAs in the proposed NCTI modulator with shifted loop delays can use 24% more time to settle, and has a 6.55 dB smaller input swing for the last OTA. Also, the feedback factor of the last integrator increases. These relax the slew rate and settling speed requirements of the OTAs.

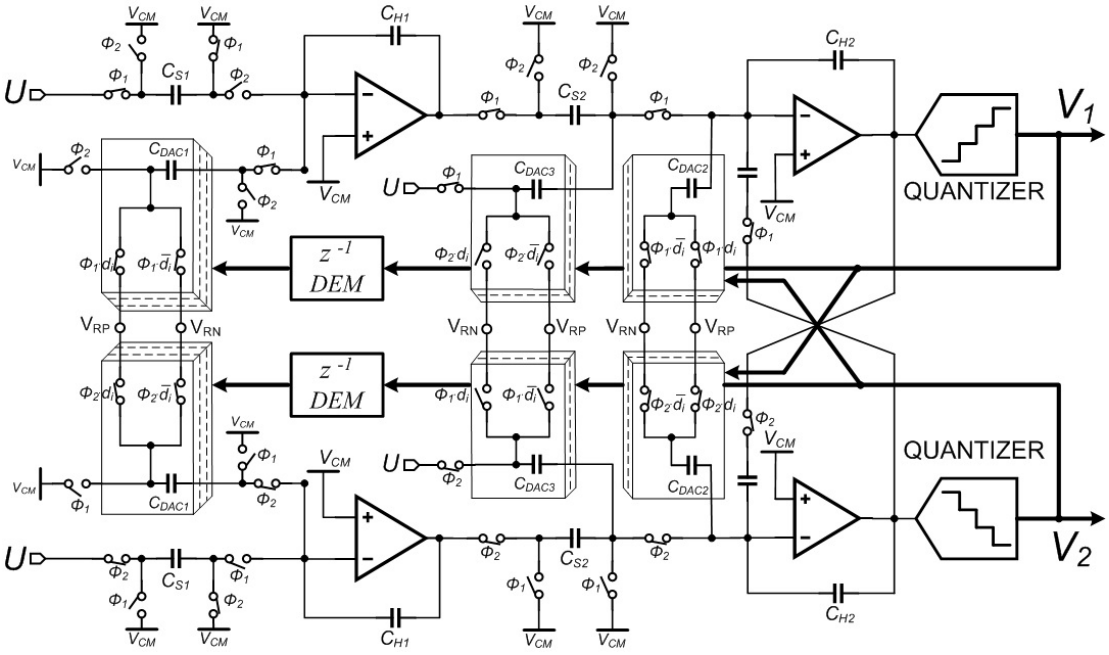


Figure 3.13: The single-ended circuit diagram of the proposed NCTI ΔΣ ADC with shifted loop delays.

Table 3.2 Comparison Between Noise-Coupled Time-Interleaved ΔΣ ADCs

	Specification	Figure 3.11(b)	Figure 3.12
System timing	*Settling*	*2.9nS*	*3.8nS*
	Quantization	*0.25nS*	*0.25nS*
	DEM	*0.9nS*	*3.8nS*
Last OTA	*Feedback Factor*	*1/5.25*	*1/4.5*
	Input Swing	*-0.06dBFS*	*-6.61dBFS*
	Output Swing	*-0.06dBFS*	*-0.05dBFS*

However, the drawback of the shifted loop delay architecture is that in cascaded delay-free integrators, it takes 20% slower settling for the second integrator to give 80 dB SNR. Overall, the necessary unity gain bandwidth of the last OTA in the proposed modulator with shifted loop delay is still 35% smaller than in the published NCTI modulator for the same resolution. Another benefit of the proposed architecture is the

simplified clock generator. The circuit of Figure 3.12 only needs two non-overlapping clock phases Φ_1 and Φ_2; while the modulator in Figure 3.11(b) needs not only Φ_1 and Φ_2, but also even and odd clock phases [16].

To verify the effectiveness of shifting loop delays and $1 - z^{-1/2}$, four third-order noise-coupled ΔΣ ADCs were simulated using the Cadence SPECTRE. The first one (Mod1) was self noise-coupled ΔΣ ADC [2]; Mod2 shifted loop delays in self noise-coupled ΔΣ ADC [13]; Mod3 was NCTI ΔΣ ADC without shifted loop delays [20]; and Mod4 used NCTI ΔΣ ADC combined with shifted loop delays [21]. Oversampling ratio OSR = 12, 15-level quantizer and 120 MHz sampling frequency were still assumed for 5 MHz bandwidth ADCs. In the modulators, all blocks were simulated with operational models except OTAs, which were modeled by macro models with the specified loop gain bandwidth for settling. To verify the effectiveness of the shifted loop delays, Mod1 and Mod2 used the same OTAs to make the comparison; while Mod3 and Mod4 were compared with the same OTAs. As Table 3.3 demonstrates, the ADCs with shifted loop delays (Mod2 or Mod4) could achieve better SNR than Mod1 or Mod3. In other words, to obtain the same SQNR, the ADCs with shifted loop delays consume less power. The comparison between Mod1 and Mod2 is simulated in section 3.2. While the comparison results of the simulation between Mod3 and Mod4 are illustrated in Figure 3.14. For the same sampling frequency, Mod4 allows more time to settle integrators. The simulation results also prove this. The proposed NCTI ΔΣ ADC with shifted loop delays (Mod4) could achieve 83.3 dB SQNR, 3.6 dB more than the NCTI modulator without Shifted loop delays (Mod3). The THD was equal to -99.7 dB, 4.1 dB better than before; the SFDR was 100.7 dB, 3.7 dB better than the NCTI modulator without shifted loop delays

The simulation results in Figure 3.15 verify the SQNR improvement due to $(1 - z^{-1/2})$. Mod2 has the NTF of $(1 - z^{-1})^3$; Mod4 is $(1 - z^{-1})^2(1 - z^{-1/2})$. Assuming all blocks including OTAs, switches, quantizers and DEMs were described by ideal macro models. The proposed Mod4 achieves 6.2 dB improvement in SQNR over Mod2, which matches the theoretical analysis in section 3.3.1.

Table 3.3: Comparison of Simulation Results with -2.6 dBFS Input Signal

	Settling Time	Nonoverlap Time	Noise Shaping Function	SNDR
Mod1	*2.9 nS*	*1.15 nS*	$(1 - z^{-1})^3$	*75.4dB*
Mod2	*3.8 nS*	*0.25 nS*	$(1 - z^{-1})^3$	*78.1dB*
Mod3	*2.9 nS*	*1.15 nS*	$(1 - z^{-1})^2 (1 - z^{-1/2})$	*79.7dB*
Mod4	*3.8 nS*	*0.25 nS*	$(1 - z^{-1})^2 (1 - z^{-1/2})$	*83.3dB*

Mod1: NC modulator without SLDs

Mod2: NC modulator with SLDs

Mod3: NCTI modulator without SLDs

Mod4: Proposed NCTI modulator with SLDs

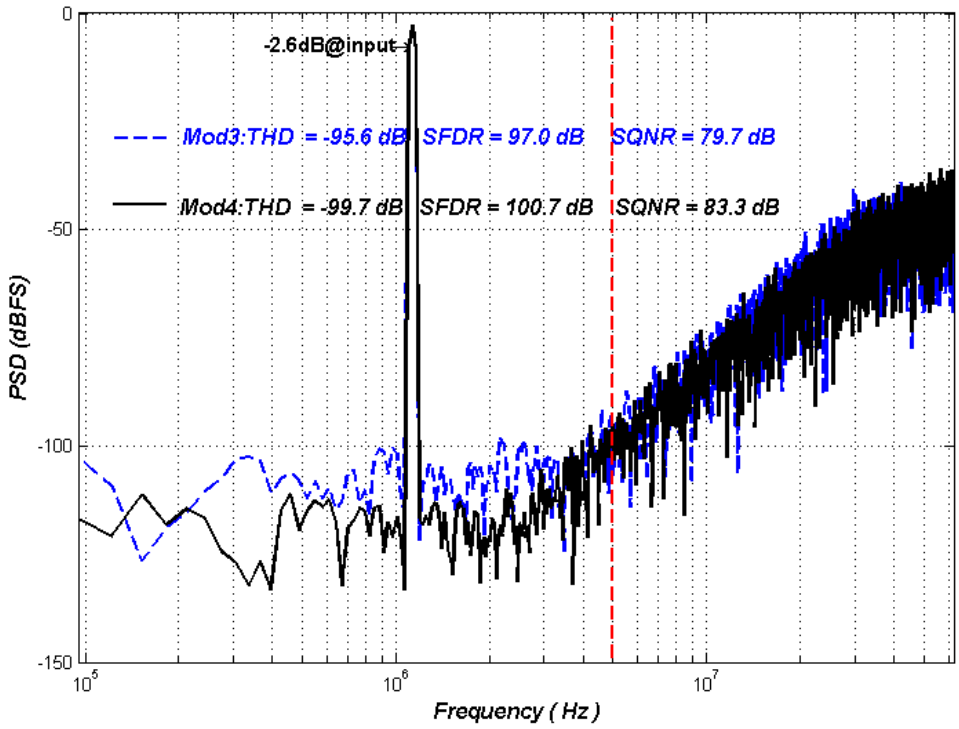


Figure 3.14: Simulated PSDs for comparison between Mod3 and Mod4.

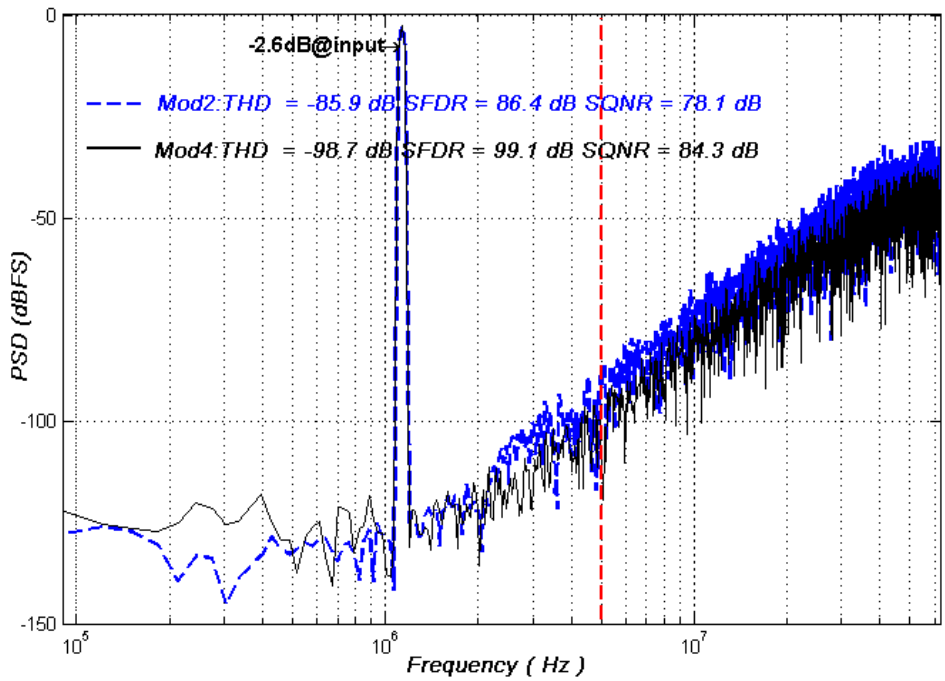


Figure 3.15: Simulated PSDs for comparison between Mod2 and Mod4.

3.4. Summary

Two noise shaping enhancement techniques with shifted loop delays are proposed in this chapter. One combines shifted loop delays and self-noise coupling for a low-distortion wideband delta-sigma modulator. With shifted loop delays, the proposed modulator eliminates the active adder, relaxes the timing for quantization and DEM, and preserves the low-distortion property. With the self noise coupling technique, a low-power third-order delta-sigma modulator was designed requiring only 2 OTAs.

The other low-power low-distortion wideband ΔΣ ADC uses noise-coupled time-interleaved architecture along with shifted loop delays. In this architecture, the necessary speed of the quantization and DEM can be greatly relaxed by shifting loop delays. Also, the proposed modulator uses a single integrator to perform both integration and active summation, thus saving a significant amount of power. When noise coupling and time interleaving are used, a low-distortion third-order enhanced

noise shaping ΔΣ ADC requiring only four OTAs can be implemented. Simulations verified the improved performance.

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CHAPTER 4 . DOUBLE-SAMPLED WIDEBAND DELTA-SIGMA ADCS WITH SHIFTED LOOP DELAYS

This chapter describes the design technique for double-sampled wideband ΔΣ ADCs with shifted loop delays (SLD). It uses double sampling combined with shifted loop delays to expand the bandwidth and lower the power consumption. Second-order and third-order noise shaping ΔΣ ADCs were analyzed and simulated in a 0.18um CMOS technology.

4.1. Introduction

The rapidly expanding market for wireless communication systems, high-definition consumer electronics and medical imaging increases the demand for high performance, low-power wideband ΔΣ ADCs. Compared with discrete-time (DT) switched-capacitor (SC) counterpart, continuous-time (CT) ΔΣ modulators, because of their inherent anti-aliasing filtering performance and higher permissible frequency, are widely used to realize ADCs with 10 MHz or greater bandwidths [1~3]. Using double sampling [4] and/or extra loop delay [5], recently published DT ΔΣ ADCs could achieve 10 to 20 MHz bandwidths [6]-[7]. Double sampling is an effective technique to realize a wideband ΔΣ modulator, because it allows a sampling frequency twice high as in a single-sampled modulator. The feed-forward structure [8] has also been used in modulators with double sampling, because in those the loop filter processes only the quantization noise within the whole signal band. Consequently, the linearity requirements for all integrators are relaxed. Further relaxation is obtained when using a multi-bit quantizer. However, one drawback of the low-distortion architecture is that it requires an active adder, which consumes a large amount of power. To solve this issue, Figure 4.1 shows a low-distortion double-sampled architecture [4] that can eliminate the active adder. It used an embedded-adder quantizer to achieve both the summation and the quantization.

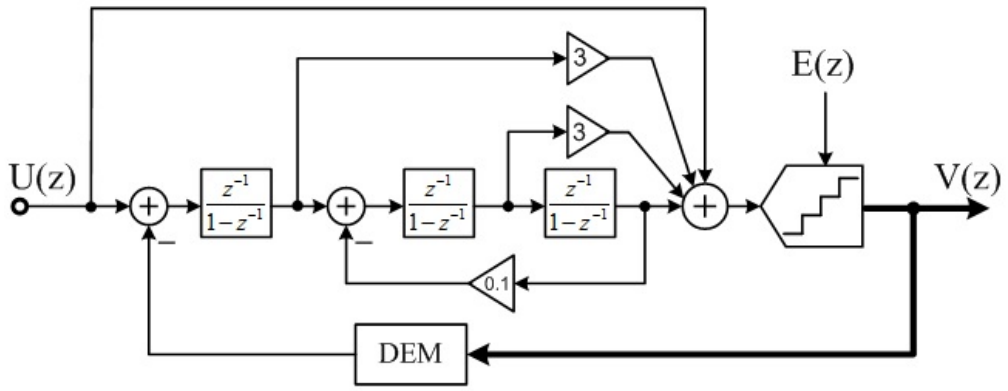

Figure 4.1: Low-distortion ΔΣ ADC with embedded-adder quantizer [4].

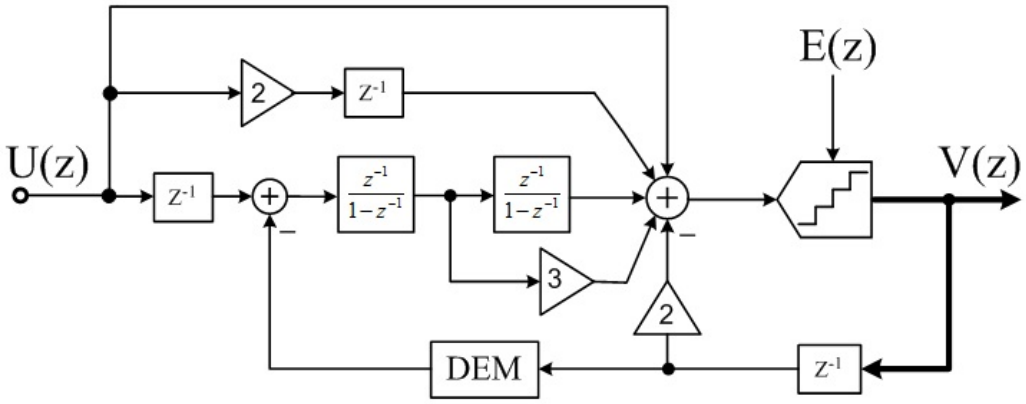

Figure 4.2: Second-order ΔΣ modulator with relaxed DEM timing [10].

Although this architecture used an embedded-adder preamplifier to avoid the attenuation from the parasitic capacitors, the overall linearity of the modulator is still affected by mismatch effects and kick-back noise.

Another problem in double-sampled low-distortion modulators is the critical timing for the quantization and dynamic element matching (DEM) logic. Since all circuits are operating in each clock phase in double-sampled ΔΣ ADCs, the quantization and DEM must be performed during the non-overlapping intervals. The timing becomes even more restricted when considering the inherent quantization delay in the double-sampling scheme [9]. Therefore, the required speed for the quantizer and DEM must be much higher than for other blocks in the modulator. Also, the time slot in the non-overlapping intervals also shorten the working clock phase, which calls for higher speed of all integrators.

Figure 4.2 illustrates a solution to this problem using an extra loop delay in the feedback loop for DEM [10]. However, this topology is not power-efficient, because it consumes three operational transconductance amplifiers (OTAs) to achieve a second-order noise shaping function, including one OTA for the active adder. Furthermore, the complex feed-forward architecture needs larger capacitor area and more complex timing logic, and also increases the power needed by the active adder due to the small feedback factor (β = 1/10).

In this chapter, several double-sampled ΔΣ modulator topologies with shifted loop delay were proposed. By shifting loop delays, the structures relax the critical timing constraints in the modulator feedback path, and achieve more power-efficient operation by eliminating the active adder. Also, the topologies simplify the feed-forward paths, hence to reduce the power consumption.

The chapter is organized as follows. General architecture considerations using shifted loop delays in double-sampled modulators are introduced in Section 4.2. Section 4.3 describes a design example for a second-order double-sampled ΔΣ modulator. Section 4.4 presents a design for a third-order double-sampled ΔΣ ADC. Finally, a summary of the results is given in Section 4.5.

4.2. Architecture Considerations

Double sampling technique is an effective technique to realize a wideband ΔΣ modulator, because it allows an effective sampling frequency twice the actual clock frequency. Both clock phases are indistinguishable since the modulator operates the same way in each phase. Figure 4.3 shows the conventional double-sampled ΔΣ ADC based on the low-distortion feed-forward structure [8]. In the end of each phase, the quantizer samples the voltage from the active adder and latches the digital code before the rising edge of the next phase. Subsequently in the next phase, the digital code signal must be integrated at the first integrator. Systematically, the first integrator works as a delay-free integrator for the digital code, and the quantization operation is performed during the non-overlapping time slot because of the inherent quantization delay. When using a multi-bit quantizer, the critical timing issue gets

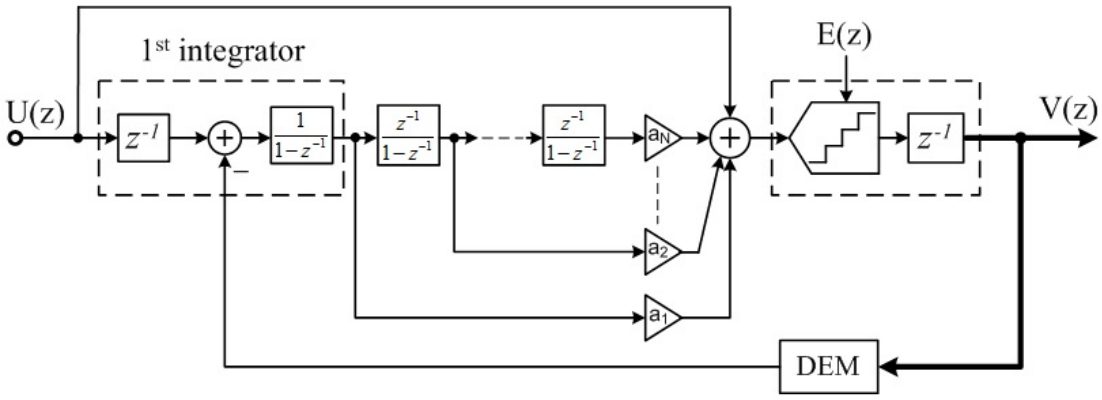

Figure 4.3: Conventional low-distortion double-sampled ΔΣ ADC.

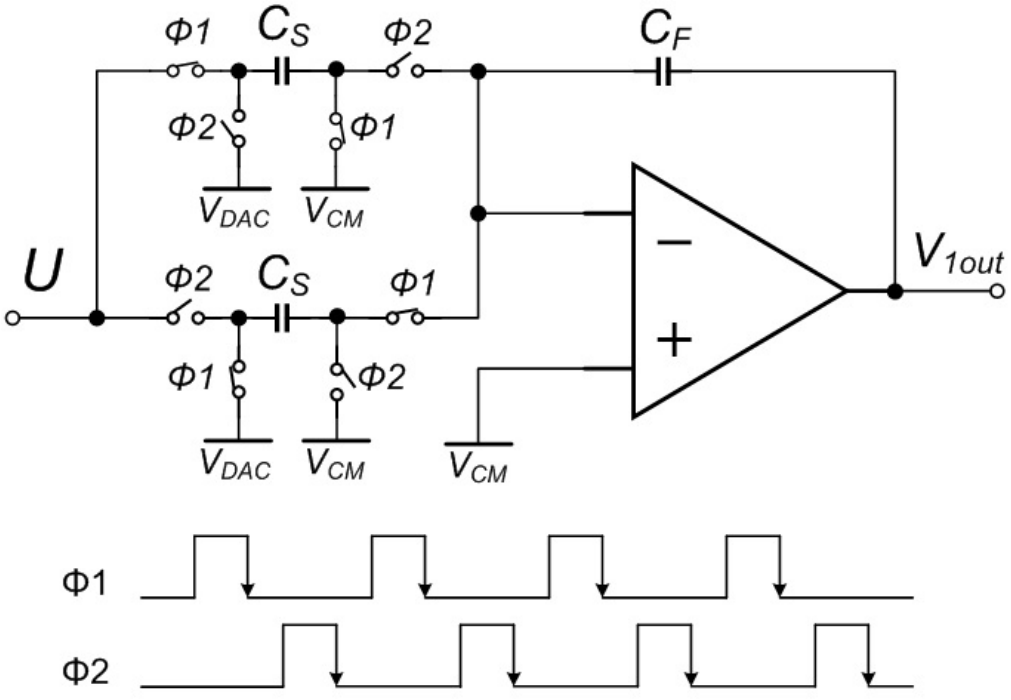

Figure 4.4: Single-ended version of a double-sampled SC integrator.

worse because DEM uses non-overlapping time slot also. Additionally, in order to keep low-distortion property, the first integrator has to shift the loop delay.

Figure 4.4 illustrates the single-ended version of a double-sampled SC integrator as the first integrator used in Figure 4.3. Phase Φ_1 and phase Φ_2 are non-overlapping clock phases. The output of the integrator is updated during each phase. The first integrator operates in two steps: during phase Φ_1, Cs in the top path samples

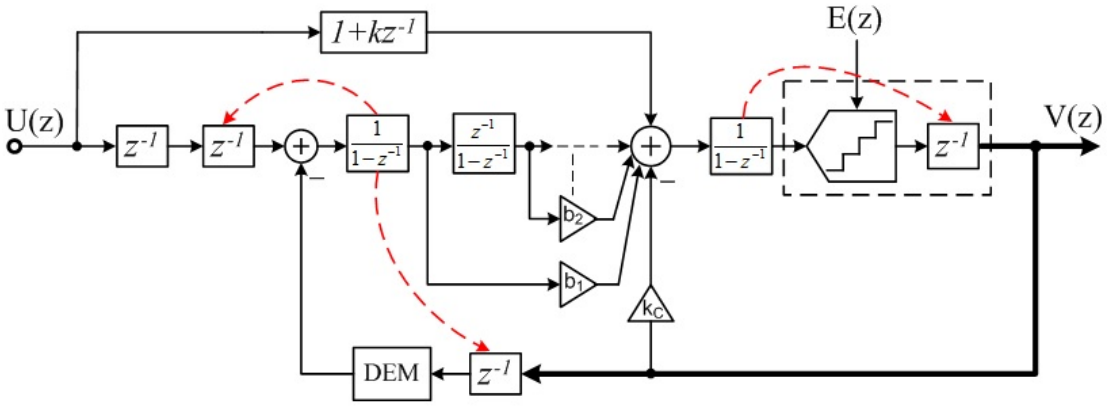

Figure 4.5: Proposed low-distortion double-sampled ΔΣ ADC with shifted loop delays.

the input signal U and Cs in the bottom path transfers the charge of $Cs*V_{DAC}[n]$ minus the previously sampled charge of Cs*U[n-1] to the feedback capacitor C_F. During phase *Φ2*, Cs in the top path transfers charge, and Cs in the bottom path samples the updated input signal U. As a result, the first integrator works as a delay-free integrator with a shifted loop delay in the signal path.

However, the disadvantages of double sampling technique restrict the performance of the modulator. One is the nonlinearity caused by the capacitor mismatch between the two feedback DAC paths. Fortunately, a fully-floating differential SC integrator [11] or the modified efficient fully-floating double-sampling integrator [12] can be utilized to highly suppress the nonlinearity. Another disadvantage of conventional double sampling technique is the critical timing constraints. As previously discussed, the conventional double-sampled ΔΣ ADC based on the low-distortion feed-forward structure has to operate the quantization and DEM in the non-overlapping time slot. In order to achieve the desired linearity, the required speed for quantizer and DEM must be much higher than the sampling frequency. Another issue is that the non-overlapping time slot must be wide enough, which means suppress the operating time slot of phase *Φ1* and *Φ2*.

To solve the timing issue, a double-sampled ΔΣ ADC with shifted loop delays is proposed to relax the DEM. As Figure 4.5 illustrates, the inherent quantization

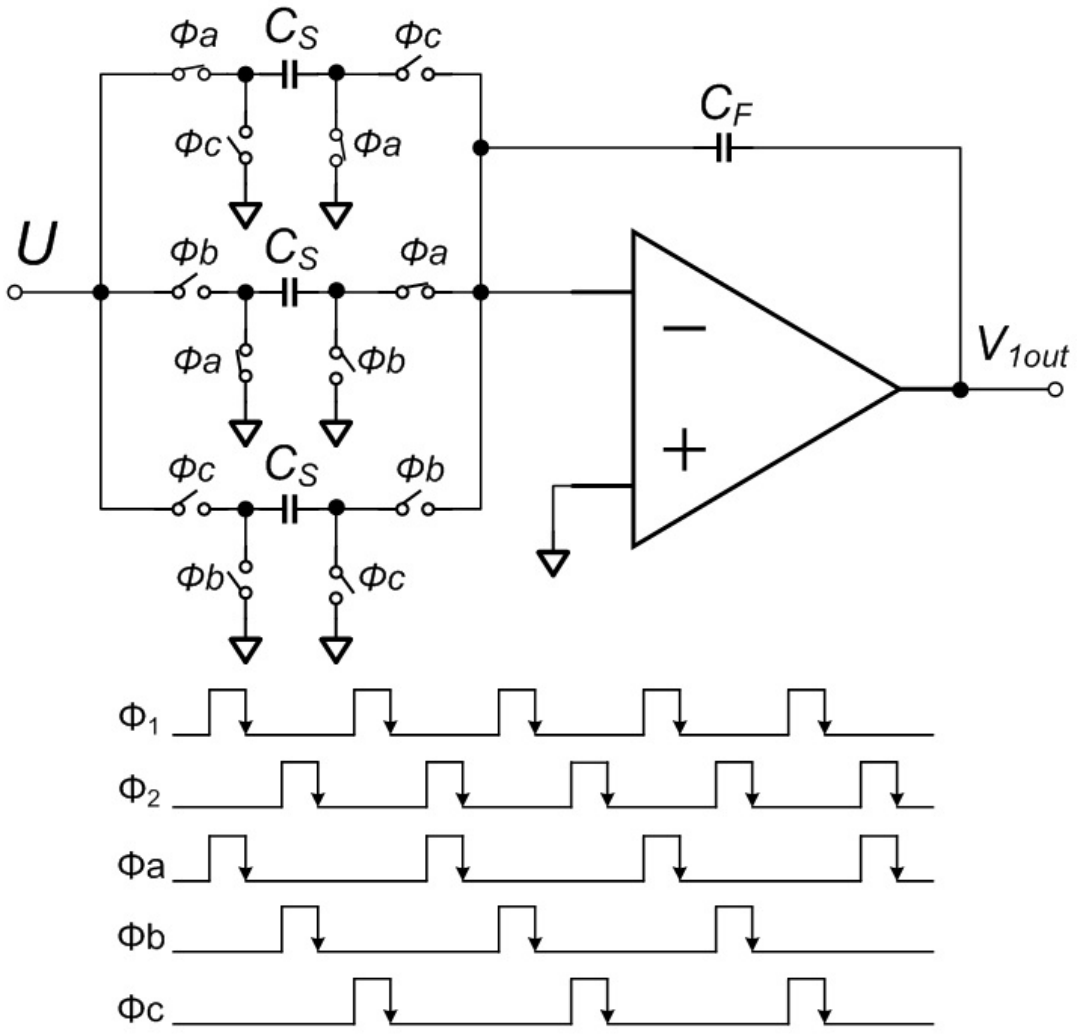

Figure 4.6: SC implementation for the first integrator in the proposed ΔΣ modulator.

delay of double sampling is shifted from the last integrator. Also, the loop delay from the first integrator is shifted to both input signal path and the feedback path. The loop delay in the feedback path helps to relax the DEM logic. The quantization has to work still in the clock intervals. One more delay is injected in the input signal path to keep low-distortion property. The feed-forward path of $1+kz^{-1}$ helps to keep the STF = z^{-1}. To make the modulator stable, one more path is feed back to the last integrator with the coefficient Kc. Another benefit of Figure 4.5 is by using shifted loop delays, the proposed structure operates active summation in the last integrator, hence eliminates the active adder.

It is straightforward to implement the first integrator in Figure 4.5 by using SC circuitry. Its implementation may be the same as that in [10], shown in Figure 4.6. The proposed integrator operates in three steps: In the top path, the input signal *U* is sampled at the end of clock phase *Φa*, then held during *Φb*, and finally processed at *Φc*. The operation is *Φb* --> *Φc* --> *Φa* and *Φc* --> *Φa* --> *Φb* in the other two branches. During the holding phase, the feedback path can use one clock cycle to operate the DEM logic. The quantization is performed during the non-overlapping intervals. *Φa*, *Φb* and *Φc* are easily generated from non-overlapping clock phases Φ_1 and Φ_2. The sampling of the input signal realizes the required clock delays shown in Figure 4.5.

4.3. Second-order ΔΣ ADC with SLD

In order to further analyze the details of the low-distortion double-sampled ΔΣ ADC with shifted loop delays, a second-order double-sampled ΔΣ modulator example is presented in this section.

4.3.1. Proposed Architecture

Figure 4.7 shows the proposed low-distortion double-sampled ΔΣ modulator with shifted loop delays. This structure shifts the loop delay of the first integrator into the input and the feedback path, and adds an extra delay into the input signal path. The delay in the feedback path helps to relax the speed requirement for DEM logic operation; the delay in the input signal path allows retaining the low-distortion property. Also, the proposed modulator shifts a loop delay from the last integrator into the quantizer, to allow for the inherent quantization delay. The proposed modulator uses the last integrator to realize both the integration and the active summation, and hence eliminates the active adder. Thus, a second-order noise shaping function can be achieved by using only two OTAs. Because an extra delay is injected in the signal path, the input and DAC signals are synchronized, and hence the loop filter only processes the shaped quantization error. In order to stabilize the loop, two branches are added, which are circled by dashed lines in Figure 4.7 for a second-order modulator.

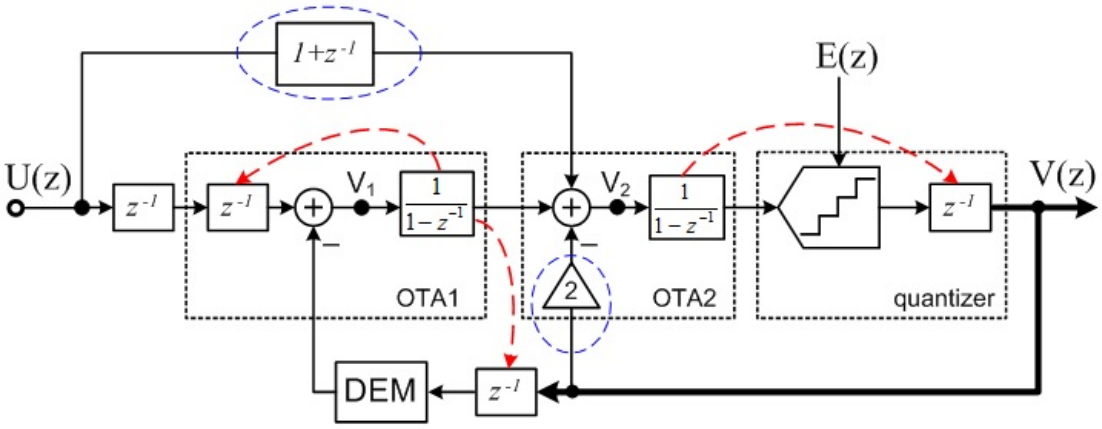

Figure 4.7: Proposed double-sampled ΔΣ modulator with shifted loop delays.

A drawback of all double-sampled modulators is that the cascaded delay-free integrators result in slower settling for the second integrator. Analysis and simulation in Appendix show that for a 0.1% settling error the second integrator needs about 21% more power than for delaying integrators.

In the proposed ΔΣ ADC of Figure 4.7, the modulator still performs the quantization during the non-overlapping intervals because of double sampling, unless a second quantizer is included. DEM can be operated in one extra clock phase. Hence, due to the loop delay included in the feedback path, both quantizer and DEM have relaxed speed requirements and robust operation. The quantization can monopolize the non-overlapping time slot, and DEM can be operated during one whole clock phase. Furthermore, compared to Figure 4.1 and 4.2, the feed-forward paths of the proposed architecture is simpler, and the coefficients of each path is smaller, which makes the feedback factor of the second amplifier larger ($\beta = 1/5$). Hence, the power consumption is significantly decreased. Also, the input signal of the second OTA is 7 dB lower than that of the active adder in the circuit of Figure 4.2, which allows relaxed slew rate and settling requirements for this OTA.

4.3.2 Transfer Functions

Linear analysis of the proposed modulator in Figure 4.7 gives

$$STF = \frac{V(z)}{U(z)} = z^{-1} \tag{4.1}$$

$$NTF = \frac{V(z)}{E(z)} = z^{-1}(1-z^{-1})^2 \tag{4.2}$$

$$V_1(z) = -z^{-2}(1-z^{-1})^2 E(z) \tag{4.3}$$

$$V_2(z) = (1-z^{-1})U(z) - z^{-1}(1-z^{-1})(2-z^{-1})E(z) \tag{4.4}$$

Here, E(z) is the quantization noise of the internal quantizer. Compared to the conventional low-distortion ΔΣ modulator, both STF and NTF in the proposed modulator contain an extra delay factor z^{-1}. Hence, the loop filter only needs to process the shaped quantization noise, the same as in the structure of Figures 4.1 and 4.2. So the proposed modulator topology retains the low-distortion property. Equation 4.4 shows that the node voltage V_2 contains the shaped signal component and shaped quantization noise, which lowers the input swing of the last integrator.

4.3.3 Circuit Implementation

The single-ended switched-capacitor realization of Figure 4.7 with the proposed integrator of Figure 4.6 is shown in Figure 4.8. Φ_D is the double sampling phase; Φ_R is the phase of the non-overlapping interval, which is used to reset the circuits. Φ_R is decided by the time constant, which is generated by the turn-on resistance of the MOS switches multiplied by the capacitor. Generally speaking, *Φ_R is 1/20 of clock phase Φ_D*. *$\Phi 1$* and *$\Phi 2$* are non-overlapping clock phases. The first integrator processes the DAC signal without delay. The input sampling capacitors and the feedback DAC capacitors are separated to avoid the quantization noise folding back into the signal band, and to reduce signal-dependent DAC reference noise. The feed-forward path $1+z^{-1}$ is easily realized as in [13]. The negative coefficient is implemented by crossing of leads in the fully-differential circuit.

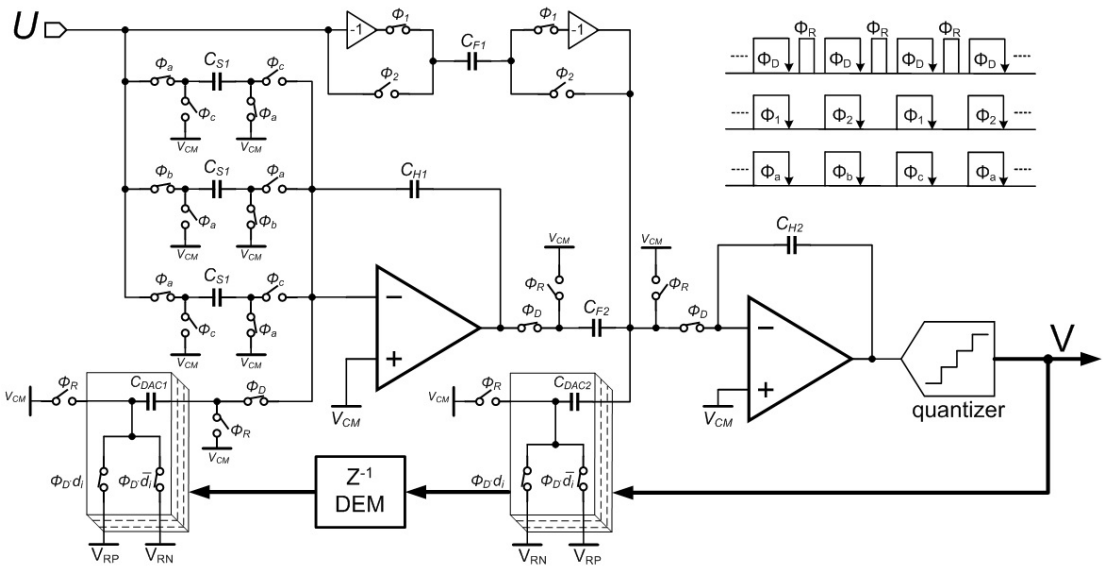

Figure 4.8: single-ended circuit diagram of proposed double-sampled low-distortion ΔΣ ADC.

4.3.4 Simulation Results

To verify the effectiveness of the proposed modulator, the transient behavior of second-order ΔΣ ADCs was simulated by using MATLAB SIMULINK and Cadence SPECTRE. 15 internal quantization levels and 160 MHz clock frequency were used for a 10 MHz bandwidth ADC, which may be needed in WLAN or LTE wireless applications. A -2.6 dBFS sine-wave input was assumed for the simulation, with full swing of 1.44 V.

The SIMULINK simulation results in Figure 4.9 show the PSD of V1, V2 and V (Figure 4.7), hence to verify the low-distortion property of the proposed modulator. They show that there is no signal component in V1, which consists with the equation 4.1. The signal component in V2 is very small, which relaxes the slew rate and settling requirement of the OTAs. Finally, the digital output V achieves a second-order noise shaping.

The fully-differential circuit of Figure 4.8 was simulated in Cadence SPECTRE assuming a 0.18um 2P4M CMOS technology.

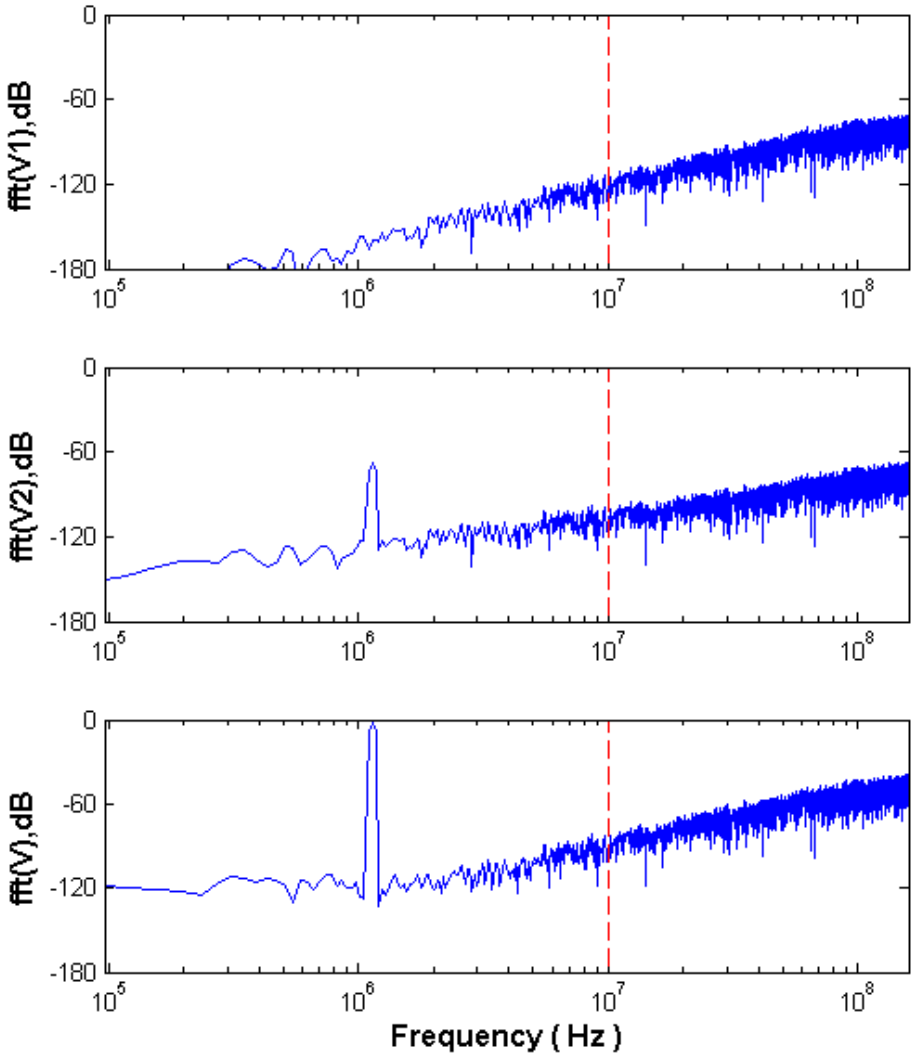

Figure 4.9: Simulated results of spectrums for the node voltages.

The OTAs were described by macro models with finite gain (50dB). The other blocks were simulated on the transistor level, but without noise and other non-ideal effects. The output digital bits were processed in MATLAB to give the power spectral density (PSD). A comparison between single sampling and double sampling ΔΣ ADC is illustrated. For a single-sampled second-order ΔΣ modulator with OSR = 8, the simulated SQNR by Cadence SPECTRE was 55 dB (Figure 4.10). For a double-sampled ΔΣ modulator, OSR = 16, and the simulated SQNR was 70.2 dB (Figure 4.11), about 15 dB more than that for the single-sampled modulator.

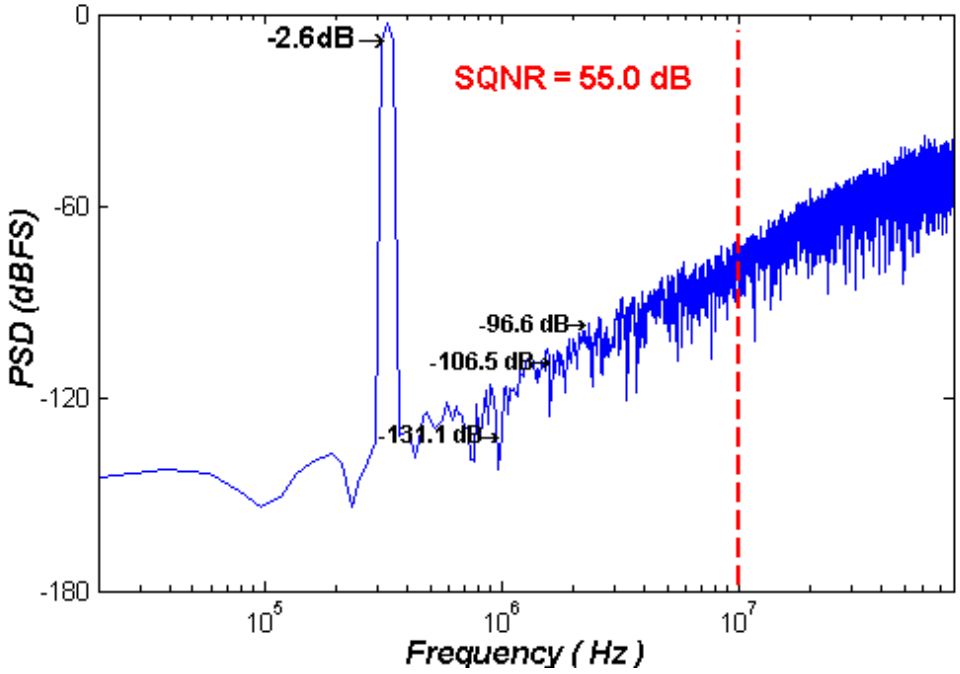

Figure 4.10: Simulated PSD of the single-sampled ΔΣ modulator.

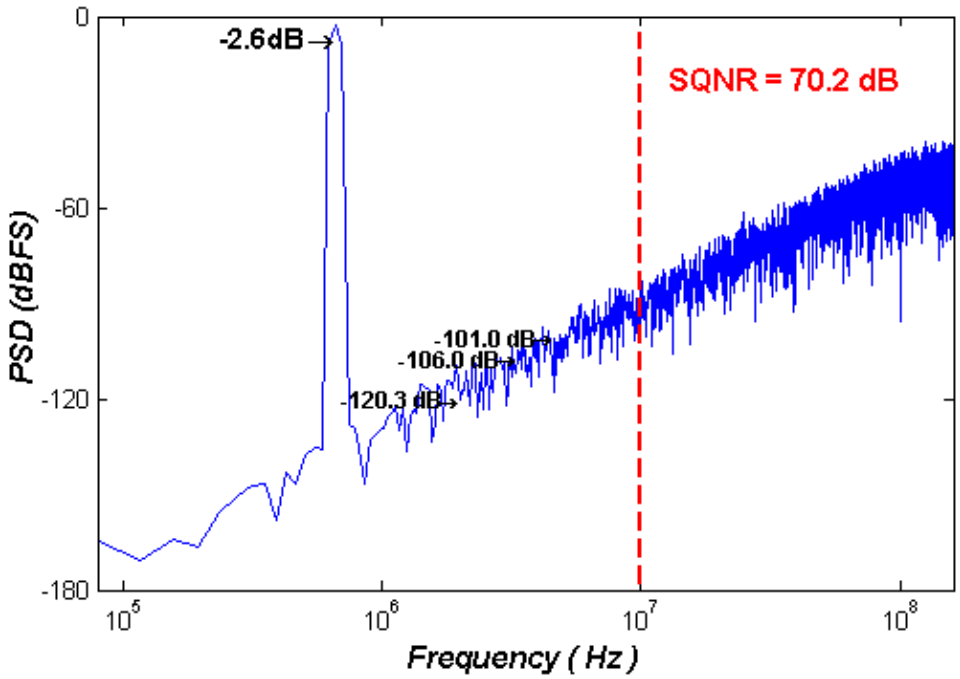

Figure 4.11: Simulated PSD of the double-sampled ΔΣ modulator.

4.4. Third-order ΔΣ ADC with SLD

Noise coupling technique can be used to boost the order of the noise shaping function. Figure 4.12 shows the noise-coupled double-sampled ΔΣ ADCs with Shifted loop delays. However, since the double sampling circuit is active in both click phases, the noise-coupled paths of z^{-1} and z^{-2} (circled in red) highly increase the load capacitance of the last integrator, which means that its power consumption will also be much increased. Hence, noise coupling is not discussed for double sampling modulators in this thesis. In this section, several third-order double-sampled ΔΣ ADCs without noise coupling are illustrated. Analysis of all architectures allows the choice of the most power-efficient topology for a wideband ΔΣ modulator.

4.4.1 Proposed architectures

Following to the generalized design procedure in section 4.2, a third-order double-sampled ΔΣ modulator with shifted loop delays can be easily obtained in Figure 4.13. However, the feed-forward paths and feedback paths decrease the feedback factor of the third integrator, which makes this architecture power-hungry.

Figure 4.14 presents an improved architecture for the double-sampled third-order ΔΣ modulator. By adding the feed-forward and feedback branches to the second integrator (enclosed by dashed lines), the third integrator has an increased feedback factor (β =1/4). Using shared capacitors, the second integrator has the same feedback factor (β =1/4). The critical timing of DEM is relaxed by the loop delay shifted from the first integrator. The delay in the internal quantizer is implemented by the shifted loop delay from the last integrator.

The drawback of this architecture is that the cascaded delay-free integrators consume more power than delayed ones. Analysis in Appendix shows that for a given 0.1% settling error, the second integrator needs about 21% more power, and the third integrator about 40% more power, than in a cascade of delaying integrators. Although the feedback factors of the second and the third integrators are highly increased, the proposed architecture in Figure 4.14 is still power-hungry.

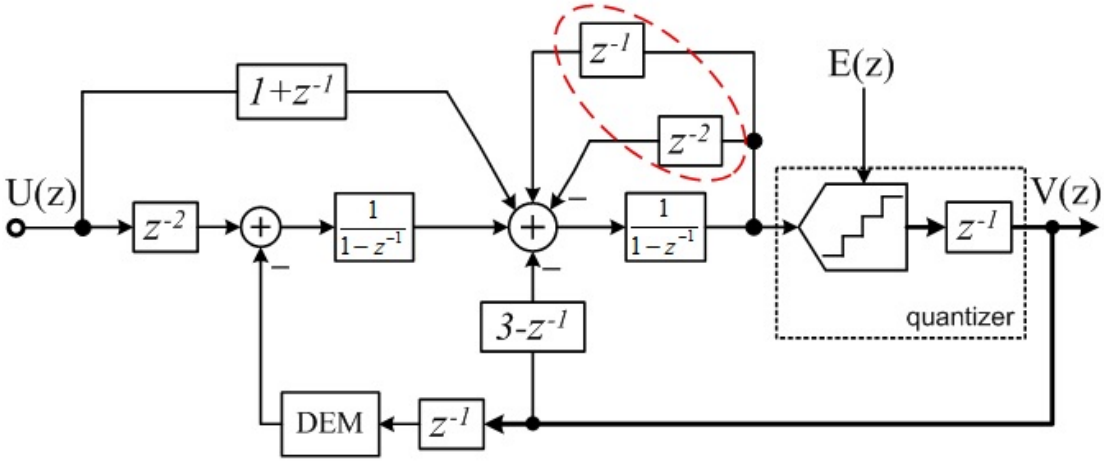

Figure 4.12: Noise-coupled double-sampled ΔΣ ADC with shifted loop delays.

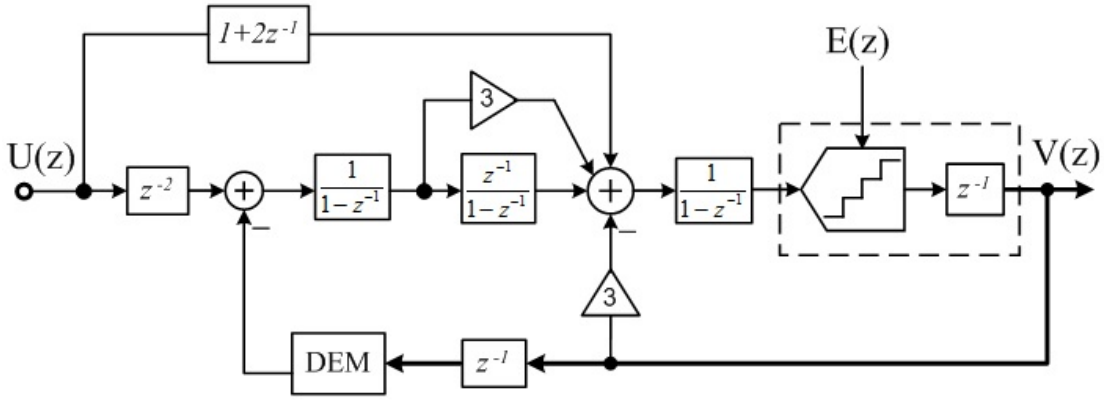

Figure 4.13: Double-sampled third-order ΔΣ ADC with shifted loop delays.

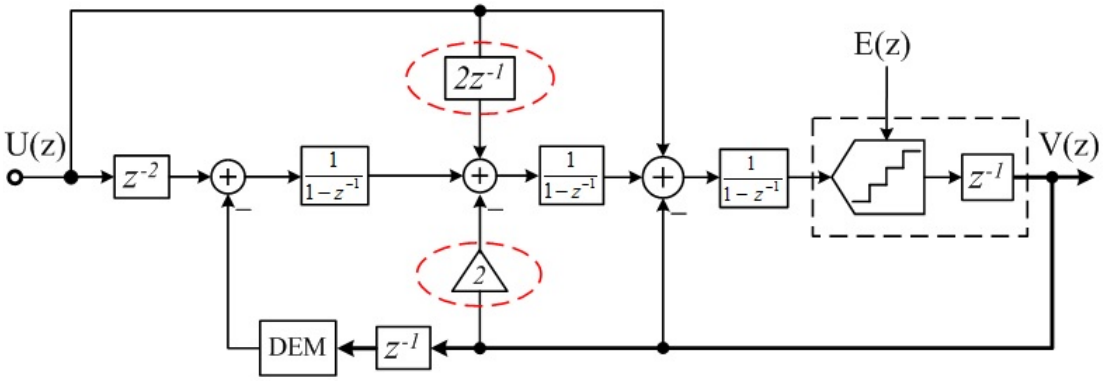

Figure 4.14: Double-sampled third-order ΔΣ ADC with improved feedback factor.

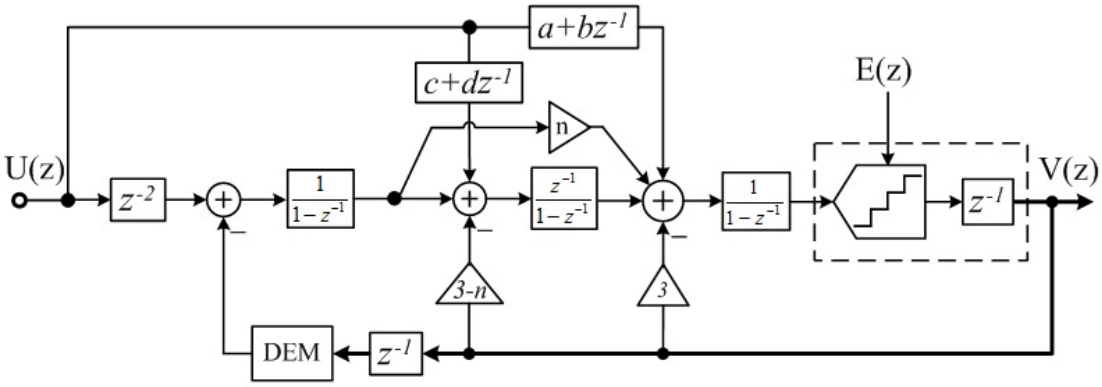

Figure 4.15: Double-sampled third-order ΔΣ ADC with delayed integrator.

To avoid the added power due to the cascaded delay-free integrators, the system of Figure 4.15 uses a delayed integrator in the second stage. This helps to eliminates the extra power consumption of the second integrator, and reduces the extra power consumption of the third integrator from 40% to 21% for a 0.1% settling error. The coefficients in Figure 4.15 can be found using linear analysis [13]. The additional feed-forward branch has a gain n (n = 0, 1, or 2). The feed-forward branches realizing $a+bZ^{-1}$ and $c+dZ^{-1}$ are used to achieve $STF = z^{-1}$. Linear analysis gives 12 possible solutions for the coefficients a, b, c and d. The best choice can be based on increasing the OTAs' feedback factors second and third integrators. Choosing $n = a = b = c = d = 1$ gives $\beta_2 = 1/5$ and $\beta_3 = 1/7$.

Shifted loop delays can also be used in the second integrator to further optimize the feedback factors. In Figure 4.16, the loop delay of the second integrator is shifted to the first stage of the loop filter. This delay reduces the power required by the third integrator by the same amount as in the system of Figure 4.15. It allows the gain of the feedback path to the third integrator to have any arbitrary value n. The delay z^{-1} can be realized by two SC sampling branches in a push-pull mode, which can share the capacitor. Linear system analysis gives $a+c = 1$. The other coefficient and feedback factor values are shown in Table 4.1.

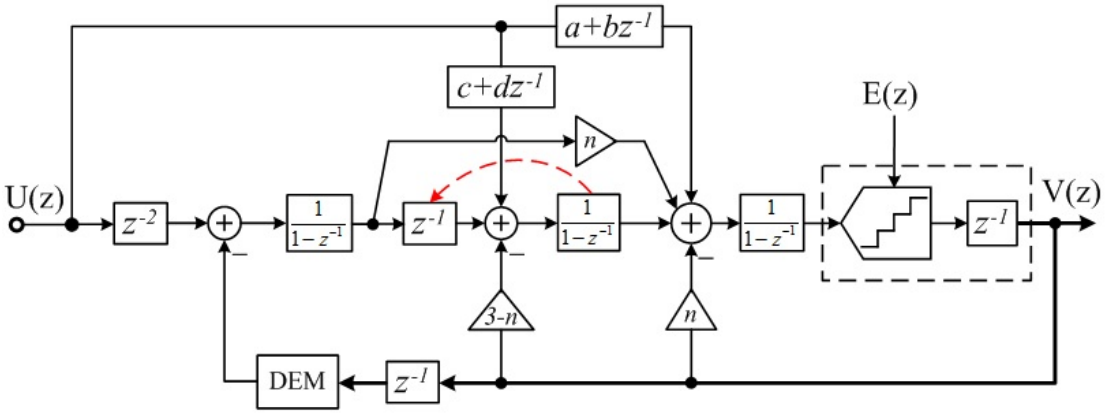

Figure 4.16: Double-sampled third-order ΔΣ ADC with shifted loop delays in the second and the third integrators.

Table 4.1 Coefficients and feedback factors in Figure 4.16

$a+c = 1$	Other coefficients			Feedback factors	
	n	b	d	β_2	β_3
$a = 0$ $c = 1$	0	-1	2	1/5	1/2
	1	0	1	1/4	1/4
	2	1	0	1/3	1/6
$a = 1$ $c = 0$	0	-1	3	1/5	1/3
	1	0	2	1/4	1/5
	2	1	1	1/3	1/7

Calculation and simulation shows the most power-efficient modulator is based on $n = 0$ and $b = -1$. Subsequently, the coefficients of a and c need to be meticulously chosen. Although $a = 0$ and $c = 1$ give the largest feedback factors, the maximum stable amplitude is degraded to -7.2 dBFs. Simulation shows that the best choice is $a = 1$, $c = 0$, hence $d = 3$. The proposed power-efficient double-sampled third-order ΔΣ modulator is shown in Figure 4.17 [14]. In the second integrator, the paths circled by dashed lines can share capacitors. The feedback factors are then $\beta_2 = 1/5$ and $\beta_3 = 1/3$.

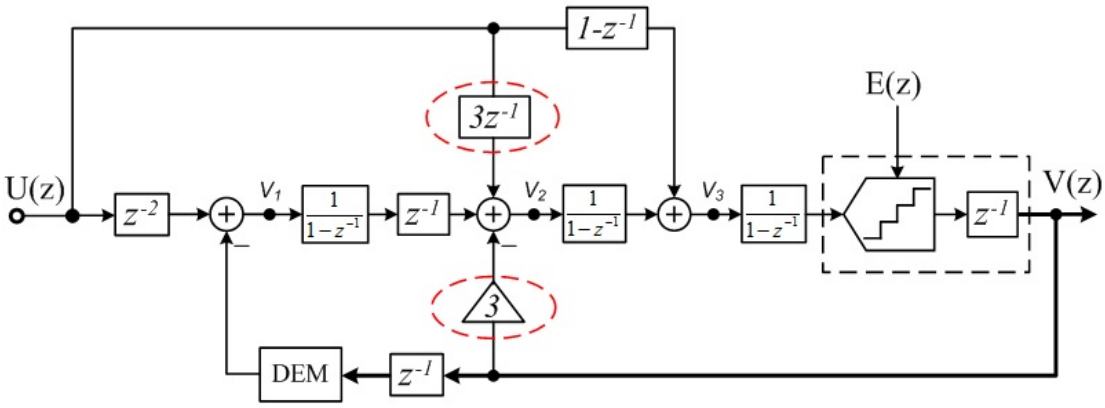

Figure 4.17: Most power-efficient double-sampled third-order ΔΣ ADC with shifted loop delays.

4.4.2 Transfer functions

Linear analysis of the modulator in Figure 4.17 gives

$$STF(z) = \frac{V(z)}{U(z)} = z^{-1} \tag{4.5}$$

$$NTF(z) = \frac{V(z)}{E(z)} = z^{-1}(1-z^{-1})^3 \tag{4.6}$$

$$V_1(z) = -z^{-2}(1-z^{-1})^3 E(z) \tag{4.7}$$

$$V_2(z) = \left[(1-z^{-1})^5 - (1-z^{-1})^2\right] E(z) \tag{4.8}$$

$$V_3(z) = (1-z^{-1})U(z) + \left[(1-z^{-1})^4 - (1-z^{-1})\right] E(z) \tag{4.9}$$

NTF in the proposed modulator achieves a third-order noise shaping function. Equation 4.6 and 4.7 shows that the loop filter only needs to process the shaped quantization noise; hence the proposed modulator topology retains the low-distortion property. Equation 4.9 demonstrates that the input signal of the last integrator contains the shaped signal component and shaped quantization noise, which means that its swing is lowered.

4.4.3 Circuit Implementation

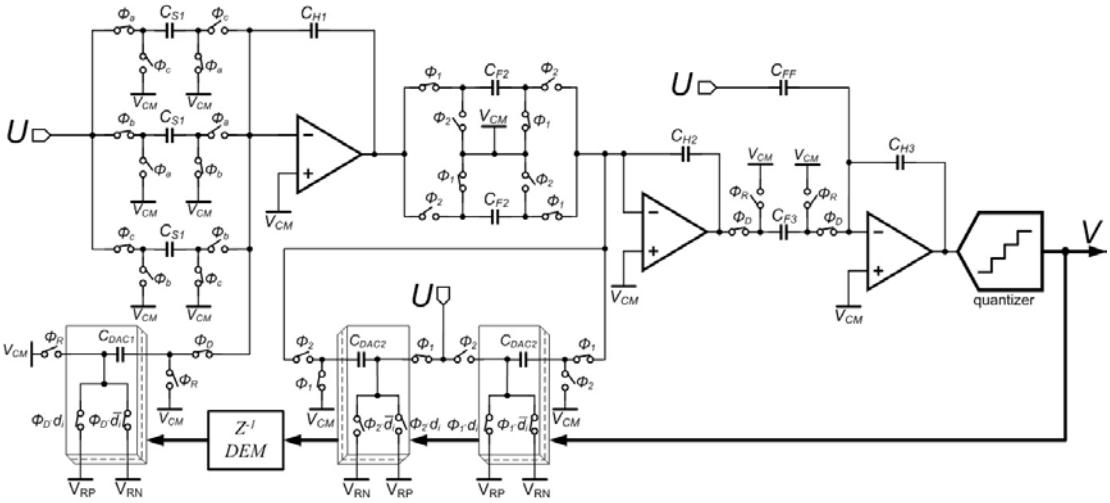

Figure 4.18: Single-ended circuit diagram of proposed double-sampled low-distortion third-order ΔΣ ADC with shifted loop delays.

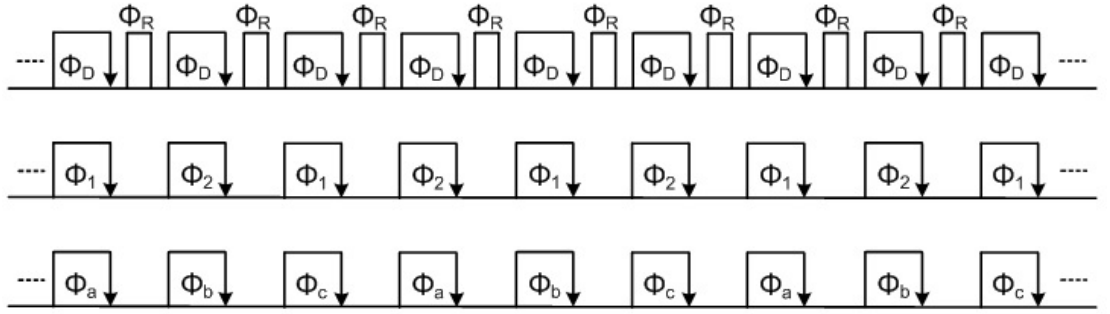

Figure 4.19: Clock phases for the circuit of Figure 4.18.

The single-ended switched-capacitor realization of the proposed ΔΣ ADC topology of Figure 4.17 is illustrated in Figure 4.18. The first integrator is the same as Figure 4.6. The clock timing for Figure 4.18 is shown in Figure 4.19. Φ_D is the double sampling phase; Φ_R is the phase of the non-overlapping interval, which is used to reset the circuits. $\Phi 1$ and $\Phi 2$ are non-overlapping clock phases, easily generated from Φ_D. Φa, Φb and Φc are the special clock phases for the first integrator, also obtained from Φ_D.

4.4.4 Simulation Results

15 internal quantization levels and a 160 MHz clock frequency were used for a 10 MHz bandwidth application. Due to double sampling, OSR = 16. The simulation

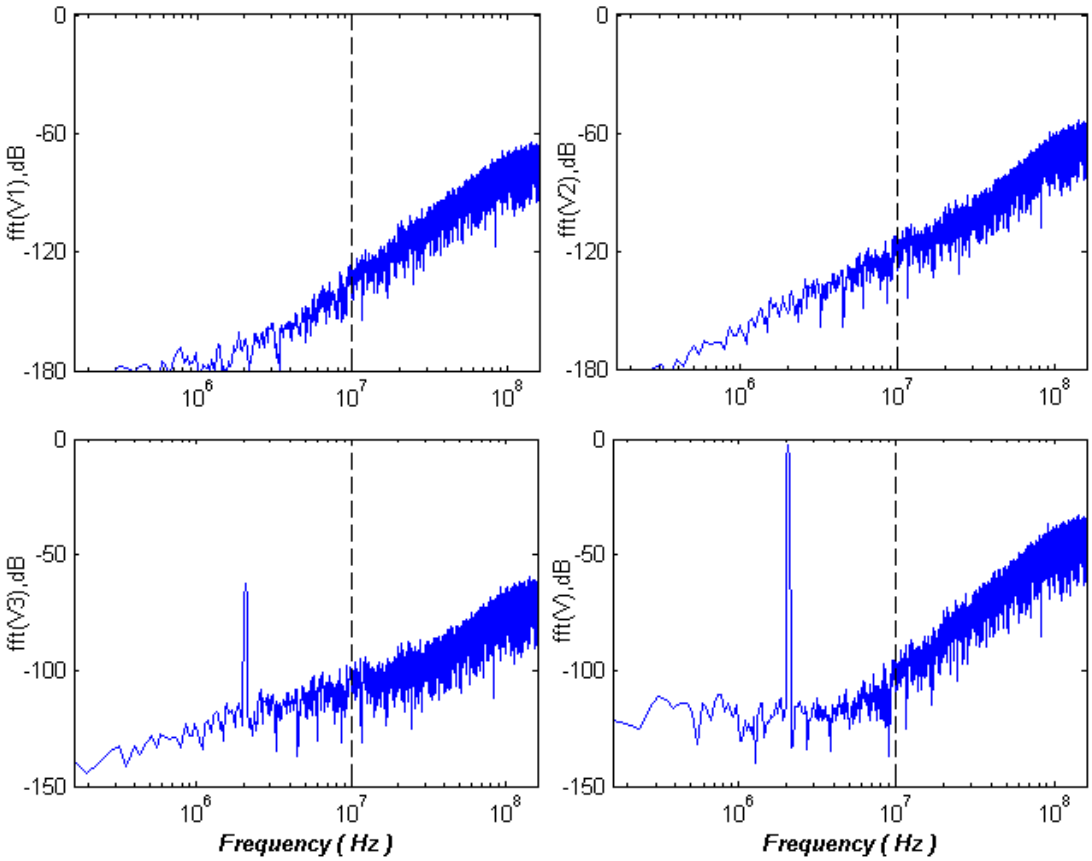

Figure 4.20: Simulated PSD of the node voltages in the proposed double-sampled ΔΣ ADC.

results (Figure 4.20) are obtained by using MATLAB SIMULINK. The PSDs of V1, V2, V3 and V verify the low-distortion property in the proposed modulator. The results show that there is no signal component in V1 and V2, and the digital output V achieves a third-order noise shaping function.

The fully-differential version of Figure 4.18 was simulated using Cadence SPECTRE, assuming a 0.18um 2P4M CMOS technology. The OTAs were represented by macro-models with finite gains (50 dB); the switches were also macro-models. All other blocks were described on transistor-level, but without noise and other non-ideal effects. For a -2.6 dBFS input sine wave at 1.1328 MHz, simulation results in Figure 4.21 show that 83.9 dB SNDR and 106.9 dB SFDR could be achieved. The THD was -103.58 dB.

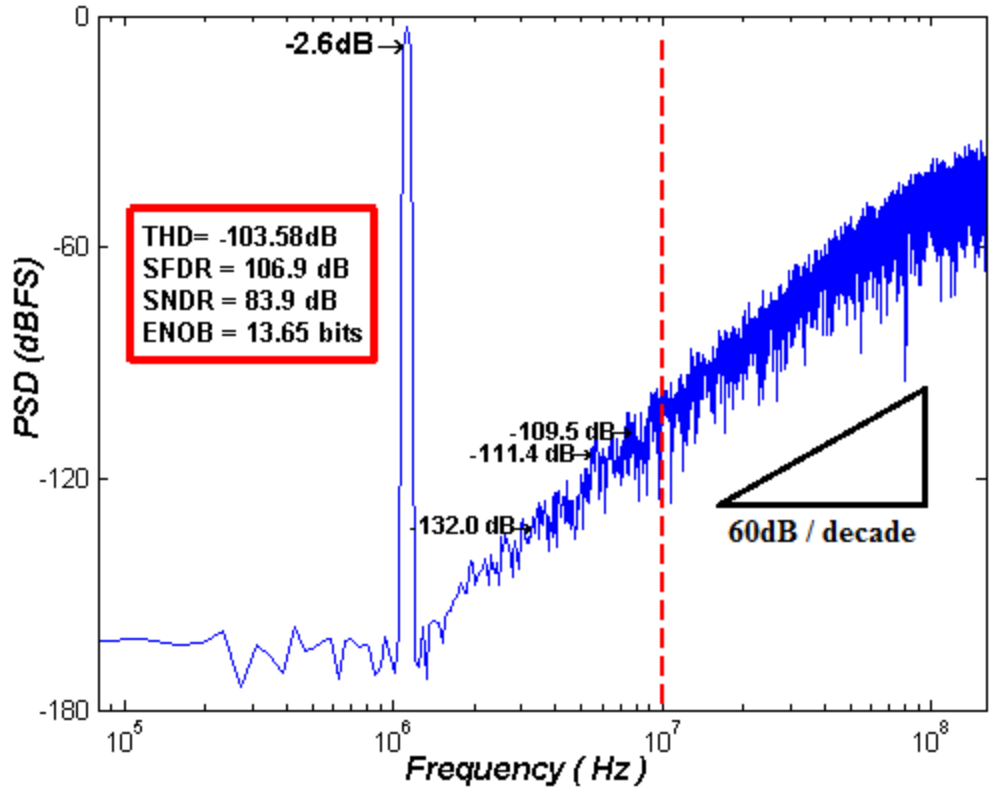

Figure 4.21: Simulated PSD of the proposed double-sampled ΔΣ ADC output signal.

4.5. Summary

This chapter described the discrete-time double-sampled ΔΣ ADCs with shifted loop delays. The added loop delay in the feedback branch relaxes the critical timing for DEM logic. Delay shifting can be combined with such useful techniques as low-distortion circuitry and noise coupling for wideband ΔΣ modulators. The presented techniques relax the timing for inherent quantization delay, reduce the speed requirements for the critical circuit blocks, and achieve power efficiency by replacing the power-hungry blocks normally used in the modulators. Analysis of all architectures allows the choice of the most power-efficient topology for a wideband ΔΣ modulator. The proposed second-order and third-order ΔΣ modulators were designed and simulated to verify the effectiveness of the shifted loop delays techniques.

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APPENDIX

SETTLING ANALYSIS OF CASCADED INTEGRATORS

To estimate the penalty for removing the delay from two cascaded integrators, consider two cascaded stages with an input signal which is a step function *u(t)*, changing from 0 to 1 volt. The stages are separated by a delay block and a switch which closes at $t = T$ (Figure A.1).

The transfer functions V_{out}/V_{in} of both stages are:

$$H_1(s) = H_2(s) = \frac{A_0}{1+s\tau} \tag{A.1}$$

At time t_1, $v_1=A_0[1-e^{-t1/\tau}]$; the settling error is $\varepsilon_1 = A_0 e^{-t1/\tau}$. If $t_1=T$, and the delay satisfies $T >> \tau$, then the input to the second stage is to a good approximation $v_2=A_0[1- e^{-T/\tau}]u(t-T)$. Thus, the settled output of the cascaded stages at time $t=2T$ is:

$$v_o = A_0^{\,2}[1-e^{-T/\tau}]^2 \tag{A.2}$$

The settling error is $\varepsilon_o = -2A_0e^{-T/\tau} + A_0^{\,2}e^{-2T/\tau}$. Usually $e^{-T/\tau} << 1$, so the settling error is $\varepsilon_{o1} \sim 2A_0e^{-T/\tau}$, twice that of a single stage.

If the two stages are directly cascaded, without the delay and switch (Figure A.2), the output voltage at $t = T$ is given by

$$v_o(t) = A_0^{\,2}[1-(1+T/\tau)e^{-T/\tau}] \tag{A.3}$$

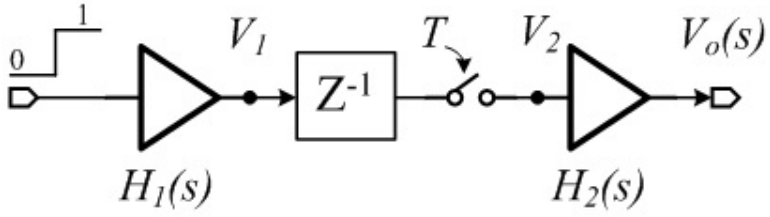

Figure A.1: Cascaded stages separated by a delay and a switch.

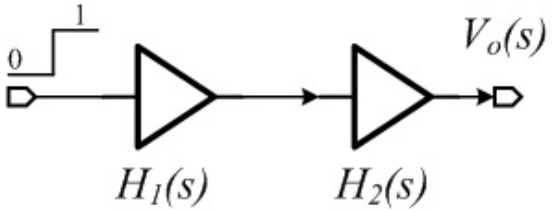

Figure A.2: Delay-free cascaded integrators.

The settling error is $\varepsilon_{o2} = A_0^2(1+T/\tau)e^{-T/\tau}$.

If the same OTAs are used in the stages of Figures A.1 and A.2, the settling error of the delay-free circuit shown in Figure A.2 is much larger than that of Figure A.1:

$$\frac{\varepsilon_{02}}{\varepsilon_{01}} = \frac{(1+T/\tau)}{2} \tag{A.4}$$

If the same settling error is required, the time constants τ of the delay-free cascade circuit of Fig. A2 must be shorter than those of the delaying cascade. The ratio τ1/ τ2 can be found from $\varepsilon_1 = \varepsilon_2$ as shown below:

$$For\ \varepsilon_{o1} = \varepsilon_{02} = 10^{-2} \Rightarrow \tau_1 = \frac{T}{5.3}, \tau_2 = \frac{T}{6.6} \Rightarrow \frac{\tau_1}{\tau_2} \approx 1.25$$

$$For\ \varepsilon_{o1} = \varepsilon_{02} = 10^{-3} \Rightarrow \tau_1 = \frac{T}{7.6}, \tau_2 = \frac{T}{9.2} \Rightarrow \frac{\tau_1}{\tau_2} \approx 1.21$$

$$For\ \varepsilon_{o1} = \varepsilon_{02} = 10^{-4} \Rightarrow \tau_1 = \frac{T}{9.9}, \tau_2 = \frac{T}{11.8} \Rightarrow \frac{\tau_1}{\tau_2} \approx 1.19$$

Note that this ratio (the penalty for delay-free operation) is not very large, around 20% for typical applications.

In a single-pole OTA circuit (Figure A.3), the time constant τ can be tuned by changing the tail current I_T of the OTA.

For the circuit of Figure A.3, the time constant is given by equation A.5:

$$\tau = \frac{C_L + (1-\beta)C_F}{2\beta I_T / V_{ov}} \tag{A.5}$$

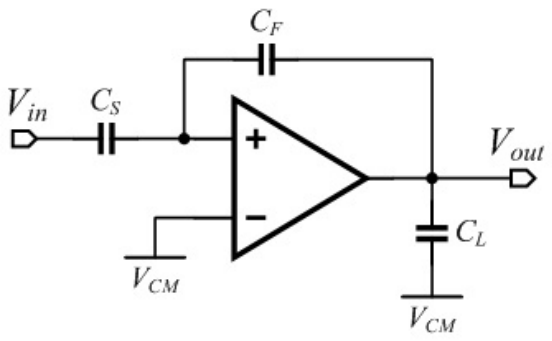

Figure A.3: Single-end circuit of the single-pole system.

Here, I_T is the tail current, V_{ov} is the overdrive voltage of the input transistors, and β is the feedback factor. Hence, the bias current ratio between delaying and delay-free circuits is the same as the ratio of the time constants. The penalty in power dissipation for removing the delay is thus around 21%.

For a three-stage cascade of delayed integrators (Figure A.4), the output voltage V_o is given as:

$$v_o = A_0^{\,3}[1-e^{-T/\tau}]^3 \tag{A.6}$$

The settling error is approximately $\varepsilon_{o3} \sim 3A_0^{\,3}e^{-T/\tau}$.

For three cascaded delay-free integrators (Figure A.5), the output voltage V_o is

$$vo(t) = A_0^{\,3}[1-(1+\frac{T}{\tau}+\frac{T^2}{2\tau^2})e^{-T/\tau}] \tag{A.7}$$

The settling error: $\varepsilon_{o4} = A_0^{\,3}[1+T/\tau+(T^2/2\tau^2)]e^{-T/\tau}$.

If the same OTAs are used in the Figures A.4 and A.5, the settling error in Figure A.5 is much larger than that in Figure A.4.

$$\frac{\varepsilon_{04}}{\varepsilon_{03}} = \frac{1}{3}(1+\frac{T}{\tau}+\frac{T^2}{2\tau^2}) \tag{A.8}$$

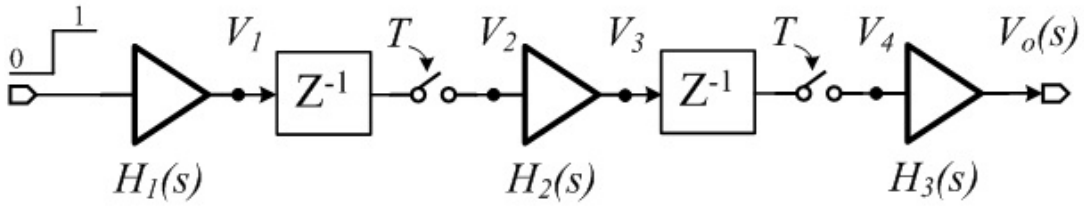

Figure A.4: Cascaded delayed integrators with three stages.

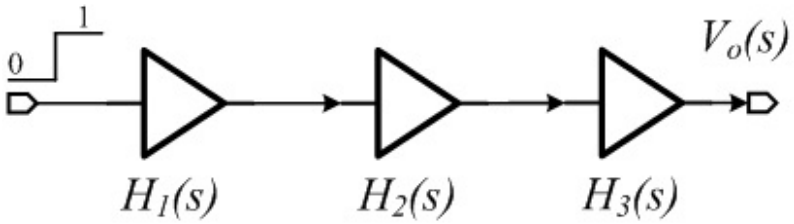

Figure A.5: Cascaded delay-free integrators with three stages.

To make the settling error the same in both circuits for a given delay time *T*, the OTAs in Figure A.5 must consume more power. As the equations below shows, the penalty is around 40%.

$$For\ \varepsilon_{o3} = \varepsilon_{04} = 10^{-2}, t_3 = t_4 \Rightarrow \frac{I_{D4}}{I_{D3}} \approx 1.47$$

$$For\ \varepsilon_{o3} = \varepsilon_{04} = 10^{-3}, t_3 = t_4 \Rightarrow \frac{I_{D4}}{I_{D3}} \approx 1.40$$

$$For\ \varepsilon_{o3} = \varepsilon_{04} = 10^{-4}, t_3 = t_4 \Rightarrow \frac{I_{D4}}{I_{D3}} \approx 1.35$$