AN ABSTRACT OF THE DISSERTATION OF

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Title: High Efficiency Delta-Sigma Modulation Data Converters.

Abstract approved:_____

Gabor C. Temes

Enabled by continued device scaling in CMOS technology, more and more functions that were previously realized in separate chips are getting integrated on a single chip nowadays. Integration on silicon has opened the door to new portable wireless applications, and initiated a widespread use of these devices in our common everyday life. Wide signal bandwidth, high linearity and dynamic range, and low power dissipation are required of embedded data converters that are the performance-limiting key building blocks of those systems. Thus, power-efficient and highly-linear data conversion over wide range of signal bands is essential to get the full benefits from device scaling. This continued trend keeps innovation in the design of data converter continuing.

Traditionally, delta-sigma modulation data converters proved to be very effective in applications where high resolution was necessary in a relatively narrow signal band. There have been active research efforts across academia and industry on the extension of achievable signal bandwidth without compromising the performance of these data converters. In this dissertation, architectural innovations, combined with effective design techniques for delta-sigma modulation data converters, are presented

to overcome the associated limitations. The effectiveness of the proposed approaches is demonstrated by test results for the following state-of-the-art prototype designs: (1) a 0.8 V, 2.6 mW, 88 dB dual-channel audio delta-sigma modulation D/A converter with headphone driver; (2) an 88 dB ring-coupled delta-sigma ADC with 1.9 MHz bandwidth and -102.4 dB THD; (3) a multi-cell noise-coupled delta-sigma ADC with 1.9 MHz bandwidth, 88 dB DR, and -98 dB THD; (4) an 8.1 mW, 82 dB self-coupled delta-sigma ADC with 1.9 MHz bandwidth and -97 dB THD; (5) a noise-coupled time-interleaved delta-sigma ADC with 4.2 MHz bandwidth, -98 dB THD, and 79 dB SNDR; (6) a noise-coupled time-interleaved delta-sigma ADC with 2.5 MHz bandwidth, -104 dB THD, and 81 dB SNDR. As an extension of this research, two novel architectures for efficient double-sampling delta-sigma ADCs and improved low-distortion delta-sigma ADC are proposed, and validated by extensive simulations.

High Efficiency Delta-Sigma Modulation Data Converters

by

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Kyehyung Lee, Author

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DEDICATION

Praise The Lord for his gracious guidance and being with me!

I would like to express my deepest gratitude to my family for their sacrifice and unconditional love. I would like to dedicate this dissertation to my parents, Narkhun Lee and Boonhark Goo, my parents-in-law, Donghyun Kim and Duksim Kim. My admired father, who passed away during my study, taught me the importance of learning and education and did his best during his life to provide good educational environment to his family. My beloved mother always showed me an endless love, sacrifice, and support. My adored parents-in-law gave me a deep faith and encouragement. This work was made possible with the love and patience of my beloved and treasured wife, Jungyeon Kim. I thank my dear two sons, Seyeon and Elliot Sebin, for their growing with good health and brightness.

To my parents Narkhun Lee and Boonhark Goo,

my parents-in-law Donghyun Kim and Duksim Kim,

my wife Jungyeon Kim,

my sons Seyeon and Elliot Sebin

HIGH EFFICIENCY DELTA-SIGMA MODULATION DATA CONVERTERS

CHAPTER 1. INTRODUCTION

1.1. MOTIVATION

The application of delta-sigma modulation data converter is getting extended rapidly to new emerging applications such as wired and wireless communications in addition to commodity consumer electronics beyond its earlier traditional narrow-band applications. This popularity comes from its inherent high resolution and low power characteristics. It is also triggered by the dramatic increase of signal bandwidth from several tens kHz to several tens MHz the delta-sigma modulation data converter can deal with. It is enabled by device scaling, architectural innovations, and efficient circuit design. One of the great advantages of delta-sigma modulation data converter is that the accuracy requirements for its analog circuitry are greatly relaxed thanks to oversampling and noise shaping. This relaxation can be further expanded by introducing more effective modulator architecture such as low-distortion topology. We need to maximize this leverage of architectural modifications to cope with design challenges and to meet more demanding design specifications.

In this dissertation, novel design techniques based on both architecture and circuit level are proposed to improve the efficiency of delta-sigma modulation data converter. The efficiency of a data converter can be quantitatively specified by the figure-of-merit (FOM) defined as dissipated power divided by bandwidth and total

effective conversion steps that is calculated with 2 to the power of effective number of bits. The effectiveness of the proposed techniques is validated by experimentation with cutting-edge prototype designs.

1.2. CONTRIBUTIONS OF THIS RESEARCH

The major contributions of this research can be summarized as follows.

- Low-voltage and low-power time-interleaved interpolation filter and delta-sigma modulator design and its verification with CMOS for dual-channel audio DAC.
- Multi-cell architecture and first-order quantization noise coupling across modulator loops and within each loop of delta-sigma ADC.
- Generalization of quantization noise coupling to higher-order enhancement.
- Clarification of time evolution of cross-correlation and auto-correlation of quantization noises of multi-cell and noise-coupled delta-sigma ADC.
- Extension of noise coupling to time-interleaved delta-sigma ADC.
- SC circuit realization and verification with CMOS for various types of noise-coupled delta-sigma ADCs.
- Realization of state-of-the-art high-efficiency and high-linearity wideband delta-sigma ADC.
- Analysis of extra feedback factor introduced with conventional Senderowicz's double-sampling integrator onto the stability of modulator loop and the introduction of efficient double-sampling integrator.
- Development of improved low-distortion topology for delta-sigma ADC which does not require signal summation at the input of quantizer and allows

relaxed timing for dynamic element matching (DEM) to linearize multi-bit DAC in single-sampled operation.

- Development of improved low-distortion topology suitable for double-sampling delta-sigma ADC.

1.3. ORGANIZATION OF DISSERTATION

Design techniques for improving the efficiency of data converter are shown in the first three chapters for a low-voltage audio delta-sigma DAC and wideband high-linearity delta-sigma ADCs. In the following two chapters, key issues with each conventional double-sampling modulator and low-distortion modulator are addressed and effective solutions are proposed, respectively.

In Chapter 2, the first sub-1V dual-channel audio DAC with on-chip headphone driver is presented. Various design techniques to enhance the hardware efficiency of interpolation filter, delta-sigma modulator, and DEM circuitry are described.

In Chapter 3, novel architectures for delta-sigma ADCs are proposed based on multi-cell structure and quantization noise coupling. Cellular approach allows robustness and flexibility. Noise coupling enhances the noise shaping of modulator loops without degrading its stability and improves the linearity of the modulator. Measured results prove the proposed concepts.

In Chapter 4, a wideband high-linearity delta-sigma ADC is introduced. The noise coupling is applied to time-interleaving modulator, which results in 19 dB SQNR improvement with little extra circuitry. Two versions of a two-channel time-interleaved noise-coupled delta-sigma ADC are described. Both prototypes show leading-edge performance.

In Chapter 5, the limitations of conventional double-sampling technique are analyzed and novel double-sampling architecture is proposed. The same modulator coefficients and design methodology available for a single-sampled modulator are applicable to a double-sampled modulator with the proposed architecture.

In Chapter 6, an improved low-distortion delta-sigma modulator topology is proposed to overcome the associated drawback of prior art. The efficiency of delta-sigma ADC can be significantly improved by applying both techniques introduced in Chapter 5 and 6.

CHAPTER 2. A 0.8 V, 2.6 MW, 88 DB DUAL-CHANNEL AUDIO DELTA-SIGMA MODULATION D/A CONVERTER WITH HEADPHONE DRIVER

Abstract

A 0.8 V third-order ΔΣ DAC with headphone driver is described. The circuit requires only one opamp per channel, which is shared by the internal DAC, the FIR and a second-order Rauch low-pass filter, as well as by the headphone driver. Two prototype ICs (separate digital and analog chips), implemented in a 0.35μm CMOS process, achieved 88 dB dynamic range, while consuming 2.6 mW from a 0.8 V supply.

2.1. INTRODUCTION

Battery-powered portable audio devices require low-voltage, low-power, and medium-accuracy digital-to-analog converters (DACs). With the continuing demand for portable consumer electronics, such as digital audio/video (AV), cellular phones, and handheld global positioning systems, the downscaling of device dimensions to enable the integration of increasing numbers of transistors on a single chip is important. This trend also results in lowered power supply voltages, to reduce the power consumption and to improve the reliability of gate dielectrics. As predicted by International Technology Roadmap for Semiconductors (ITRS), for low operating power, the power supply voltage and gate length of digital CMOS devices will continue to scale down towards 0.5 V in the next decade. While the reduction of power supply voltages benefits the essential digital blocks performing data storage

and digital signal processing, it makes it hard to realize indispensable analog building blocks, such as analog-to-digital converters (ADCs), DACs, and drivers.

Delta-sigma (ΔΣ) data converters employ oversampling and noise shaping to achieve a wide dynamic range (DR) in the band of interest. They trade speed and digital complexity for the desired insensitivity to analog nonidealities, which results in high DR with low-cost and low-power digital circuitry.

In this chapter, an audio-band ΔΣ DAC will be discussed. It contains a digital interpolation filter, followed by a digital ΔΣ modulator, a low-resolution DAC, and an analog low-pass filter. The basic criteria for selecting the order of the ΔΣ modulator and the quantizer resolution are 1) to make the pass-band quantization noise sufficiently low, so that the analog noises (thermal noise and 1/f noise) dominate the noise budget; 2) to reduce the out-of-band noise sufficiently so a low-order analog postfilter may be used; 3) to reduce clock jitter sensitivity sufficiently at the discrete-to-continuous-time interface [2].

Since thermal noise, sampled noise (kT/C), and transistor flicker noise do not scale down with the finer line-width process, smaller resistors, bigger capacitors and transistors have to be used to reduce noise, which necessitates larger drivers with more power consumption; furthermore, due to the reduced signal voltage swing, to achieve the required signal-to-noise plus distortion ratio (SNDR), extra power has to be dissipated. Switched-capacitor direct-charge-transfer DACs [2],[3] have superior noise-versus-power efficiency, but they require floating switches, which are difficult to implement with a low supply voltage. Bootstrapping [4] and switched-RC [5] circuits were proposed to realize the floating switches. In the first approach, the voltage difference between the gate and the source is kept constant at a level high enough to turn on the switch. However, this is not a truly low-voltage solution, especially for a nanometer process, since the gate voltage can then become higher

than the supply voltage, which results in potential reliability issues. In switched-RC circuits, the floating switches are replaced by resistors, and signal leakage occurs through them. This causes nonlinearity, which needs careful circuit design and optimization.

This chapter proposes a new DAC structure [6] that contains no floating switches, and requires only one opamp per channel, shared by the internal DAC, an FIR sampled-data filter, and a second-order Rauch low-pass filter [7],[8], as well as by the headphone driver. It achieves an 88 dB DR over a 20 Hz to 24 kHz passband, and consumes 2.6 mW from a 0.8 V power supply. (To our knowledge, this is the first sub-1V audio ΔΣ DAC with headphone driver integrated.) Section 2.2 describes the architecture of the DAC. Section 2.3 describes the digital stages including the interpolation filter, the ΔΣ modulator and the dynamic element matching (DEM) circuitry. Section 2.4 presents the low-voltage and low-power analog DAC structure. The experimental results are shown in Section 2.5. Finally, a summary is provided in Section 2.6.

2.2. ARCHITECTURE

The block diagram of the DAC is shown in Fig. 2.1. The digital part contains a four-stage finite impulse response (FIR) interpolation filter, a ΔΣ modulator (DSM) and a data-weighted averaging (DWA) logic. The analog part contains the two switched-resistor DACs (R-DAC) and the RC low-pass filters (RC-LPF) that also act as the drivers for the headphones. The digital filter increases the sampling rate from f_s = 48 kHz to 64·f_s = 3.072 MHz, and suppresses the spectral replicas to improve the DR of the DSM, and to simplify the analog filtering performed by the RC-LPF. The DSM reduces the word length of the signal from 17 bits to 3 bits, with

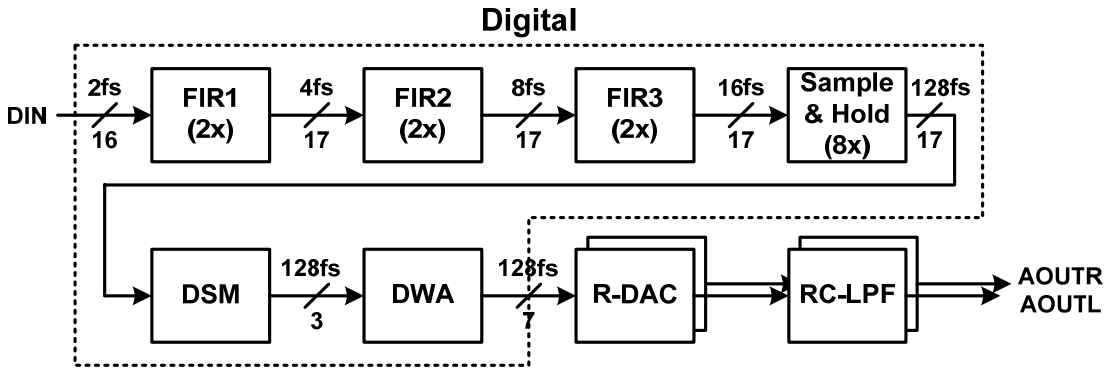

Figure 2.1: DAC architecture.

negligible added passband truncation noise. The DWA scrambles the bits of the thermometer-coded output of the DSM, so as to reduce the in-band power spectral density of the error due to element mismatches in the R-DAC. Finally, the RC-LPF both filters and buffers the DAC output, and is capable of driving a low-impedance (16 Ω || 300 pF) headphone.

2.3. DIGITAL STAGES

The digital section of the DAC includes a serial-to-parallel converter, an interpolation filter, a ΔΣ modulator, and the DWA logic for the DAC.

2.3.1. Serial to parallel converter

The 1b serial input data is converted into 16b parallel output data for the signal processing performed in interpolation filter.

2.3.2. Interpolation filter

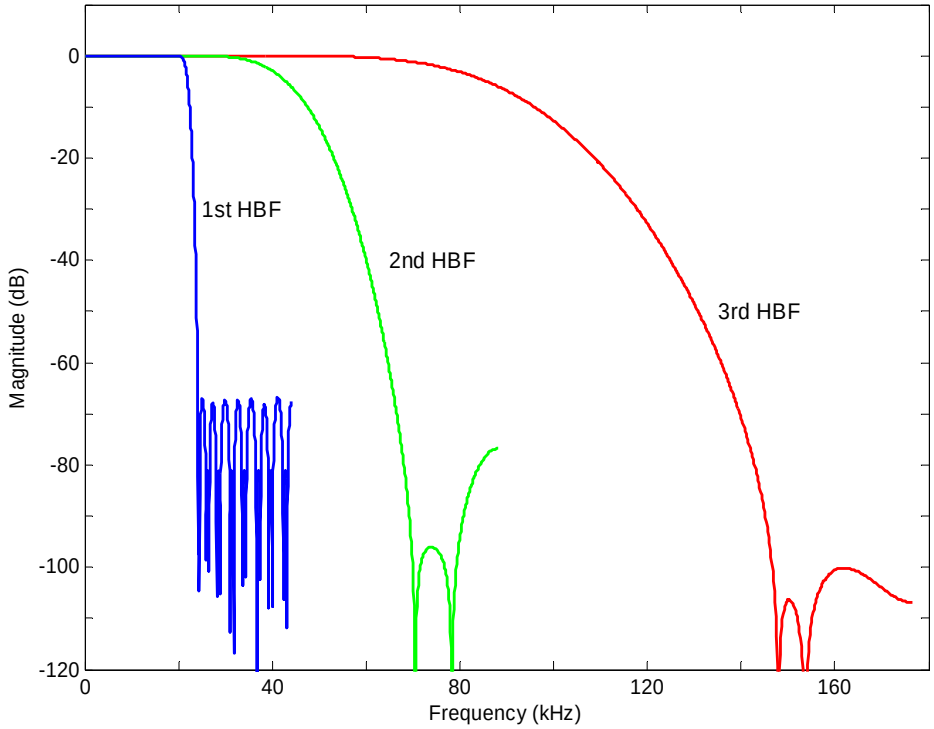

Figure 2.2: Frequency responses of the HBFs in the interpolation filter.

An efficient dual-channel interpolation filter was required. The strict requirements on the linear phase characteristics in audio applications mandate the use of a FIR filter, rather than an infinite impulse response (IIR) filter. An FIR interpolation filter is hardware-intensive compared to the other design blocks. So an efficient realization of the interpolation filter was important to minimize its silicon area and power consumption. To this end, it was realized with as a cascade of several stages, rather than a single stage [9]. Also, the total number of multiplication with the filter coefficient was minimized by using half-band filter (HBF) sections. The filter coefficients in a linear-phase FIR filter are symmetric with respect to the center tap, which allows the reduction by half of the required multiplication with the filter coefficients. In addition to this advantage, HBF has a zero filter coefficient at every other tap (except for the center tap). Also, each filter coefficient was quantized to

the sum of a few integer powers of two, and represented by a canonic signed digit (CSD). The CSD allows encoding a binary number such that it contains the minimum possible number of non-zero bits [10]. The computation-intensive multiplication with filter coefficient is thus replaced with a few shift-and-add operations without multiplier. More aggressive quantization was applied to filter coefficients that were distant from the center tap. This results from the observation that the required accuracy for each filter coefficient is relaxed proportionately with its distance from the center tap. This reduces the total number of computation with negligible performance degradation. The computation path that takes more than half of the total active chip area was shared by both channels by introducing a time-interleaved operation between channels, at the cost of the doubled operating frequency. This enables a significant saving of silicon area without increasing the power consumption. Finally, all required filtering operations in all stages are performed using the lowest possible clock frequency to reduce the power dissipation.

The interpolation filter is composed of three cascaded FIR HBFs, followed by a sample-and-hold register. It interpolates by the oversampling ratio (OSR = 64), and achieves more than 57dB attenuation in the stopband and less than ±0.02dB ripple in the passband. The first 3 HBFs increase the OSR to 8, and the last sample-and-hold stage further increases the OSR by 8 times, to provide the overall OSR of 64. The first HBF is the most demanding, since it provides the sharpest cutoff. Later stages are simplified due to their much wider transition bandwidth specifications, as illustrated in Fig. 2.2. The orders of the three FIR filter stages are 66, 14, and 2. Thus, the numbers of realized distinct nonzero filter coefficients for these filters are 17, 4, and 1 thanks to their HBF properties. The filter coefficients are obtained using the method described in [11]. Table 2.1 shows the quantized filter coefficients in CSD for the first HBF. A direct-form structure, shown in Fig. 2.3, was selected for each

TABLE 2.1: FILTER COEFFICIENT IN CSD FOR THE FIRST HBF.

Coefficient		Value	CSD	Relative Error (%)
C(1)	C(67)	0.00112899823880	$2^{-10}+2^{-13}$	-2.6895902
C(3)	C(65)	-0.00119220557225	$-2^{-10}-2^{-12}$	2.3903221
C(5)	C(63)	0.00178804184892	$2^{-9}-2^{-13}$	2.4055834
C(7)	C(61)	-0.00257976433083	$-2^{-9}-2^{-11}-2^{-13}$	-0.6313665
C(9)	C(59)	0.00357827122113	$2^{-8}-2^{-12}-2^{-14}$	0.6372630
C(11)	C(57)	-0.00485062139929	$-2^{-8}-2^{-10}$	0.6636490
C(13)	C(55)	0.00642693964630	$2^{-7}-2^{-10}-2^{-11}+2^{-14}$	-0.2839336
C(15)	C(53)	-0.00840515050728	$-2^{-7}-2^{-11}-2^{-13}$	0.2105977
C(17)	C(51)	0.01085841433138	$2^{-7}+2^{-8}-2^{-10}+2^{-13}$	0.0538152
C(19)	C(49)	-0.01396316591895	$-2^{-6}+2^{-9}-2^{-12}-2^{-14}$	0.0994392
C(21)	C(47)	0.01793207410656	$2^{-6}+2^{-9}+2^{-12}+2^{-13}$	0.0683793
C(23)	C(45)	-0.02320312292368	$-2^{-6}-2^{-7}+2^{-12}$	-0.0420786
C(25)	C(43)	0.03053302596726	$2^{-5}-2^{-11}-2^{-12}$	-0.0505939
C(27)	C(41)	-0.04162991022557	$-2^{-5}-2^{-7}-2^{-9}-2^{-11}-2^{-13}$	-0.0094491
C(29)	C(39)	0.06086374667043	$2^{-4}-2^{-9}+2^{-12}+2^{-14}$	-0.0192165
C(31)	C(37)	-0.10440943788907	$-2^{-3}+2^{-6}+2^{-8}+2^{-10}$	0.0792549
C(33)	C(35)	0.31773802216750	$2^{-2}+2^{-4}+2^{-8}+2^{-10}+2^{-12}$	-0.0349562

FIR filter, instead of a transposed direct-form one, where extra registers are required to generate the center tap data. The relatively long critical-path delay with this structure is not an issue in this design, even without any retiming, since it takes a small fraction of the whole operation period. As mentioned earlier, each filter coefficient is quantized as a sum of a few integer powers of 2, and is realized as a series of shift-and-add operations. Since fixed filter coefficients are used in this design, the shift operation is realized in a hard-wired circuit without extra registers. A ripple-carry adder (RCA) is employed throughout the design. Four types of adder cells are used, each with the same transistor count. One of them is shown in Fig. 2.4. The two adder cells in category I are for addition, and the other two in category II for subtraction. One adder takes carry-in and outputs inverted carry-out, and the other

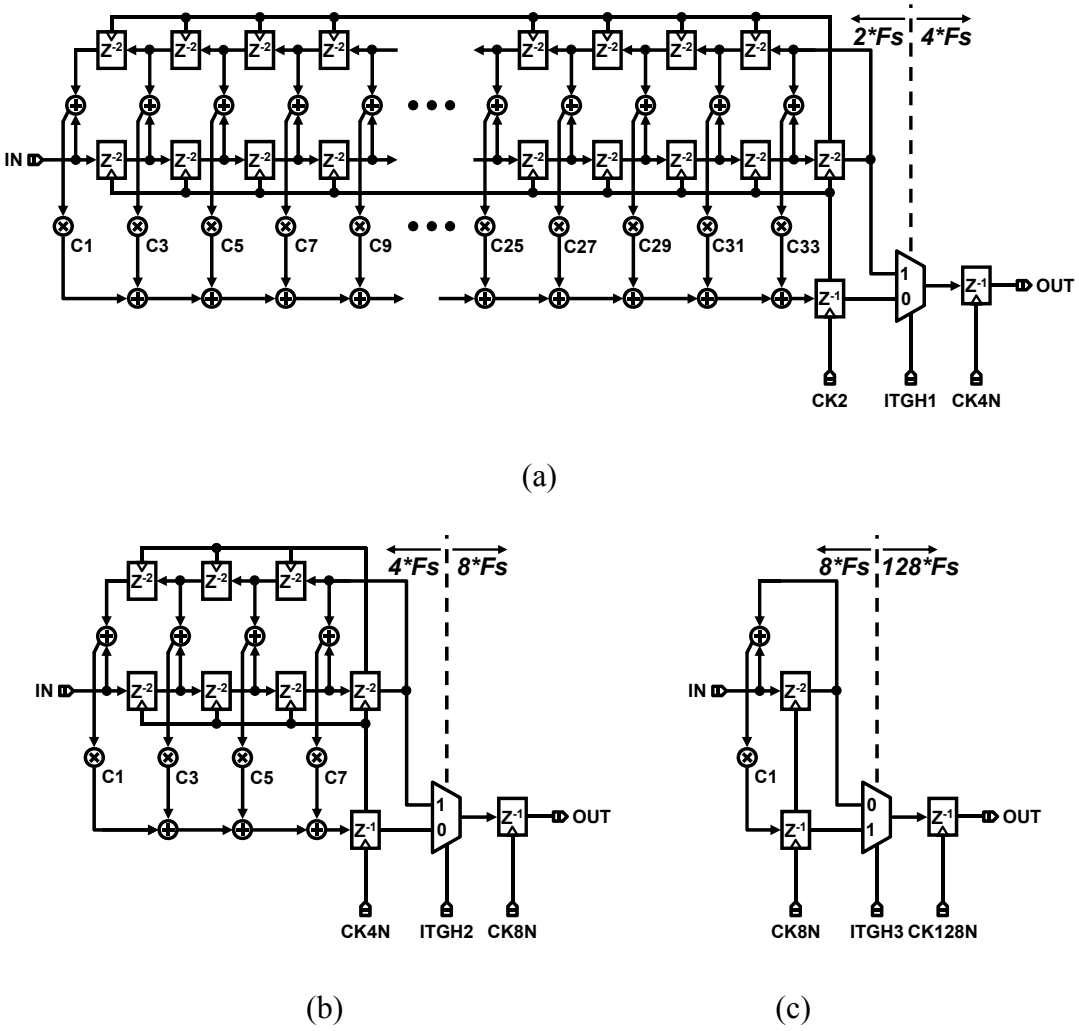

Figure 2.3: Direct form realization of the HBFs and a sample-and-hold register.

takes inverted carry-in and outputs carry-out in each category. The word length for each internal node of the interpolation filter is chosen carefully to avoid an overflow with a full-scale input signal. The truncation error in CSD multiplication is minimized by applying Horner's rule to all the partial product accumulations, where the scaling operation common to the partial products are delayed to improve its accuracy [10]. As illustrated in Fig. 2.3, the cascaded registers represented in z^{-2} and doubled operating frequency enable the time-interleaved operation of the two channels. Therefore, all channel data are processed in every other cycle. Care was

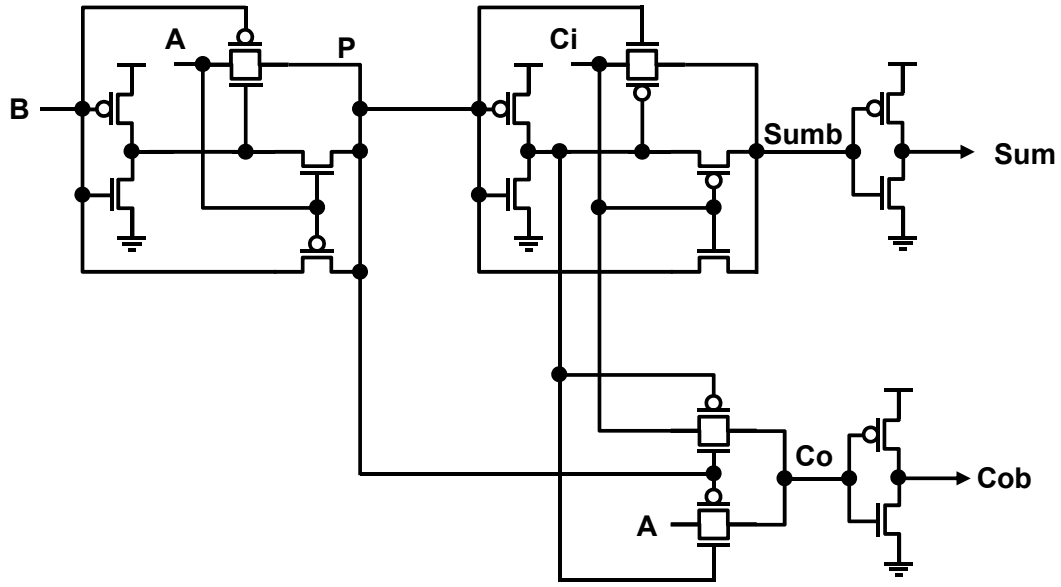

Figure 2.4: One of the four basic adder cells.

taken in reordering the interleaved output data stream from each stage of the interpolation filter for the proper time- interleaved dual-channel operation in the following stage. This was achieved with an additional register in the filtering path and a proper control signal to the multiplexer, as shown in Fig. 2.3.

The simulated SNR of the interpolation filter with a 16b resolution full-scale sine-wave input was 96.2 dB, while the SNRs of the intermediate HBF stages were 96.9 dB, 96.2 dB, and 96.1 dB.

2.3.3. Delta-sigma modulator

The main design considerations for the ΔΣ modulator were: 1) negligible in-band quantization noise compared with the analog noise; 2) reduced complexity of the reconstruction filter; 3) reduced sensitivity to clock jitter for the following analog circuitry; 4) reduced idle tones; 5) minimized word length for the adders and

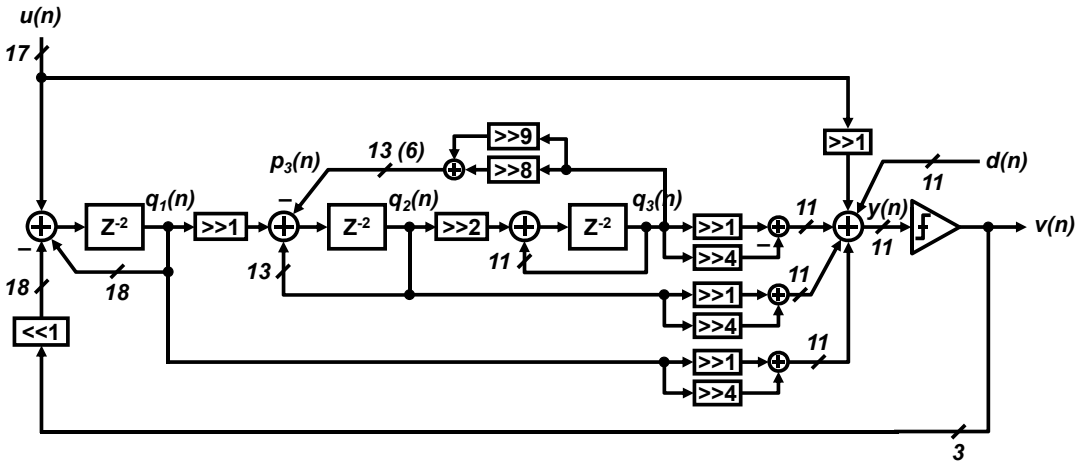

Figure 2.5: Dual-channel third-order ΔΣ modulator with resonator.

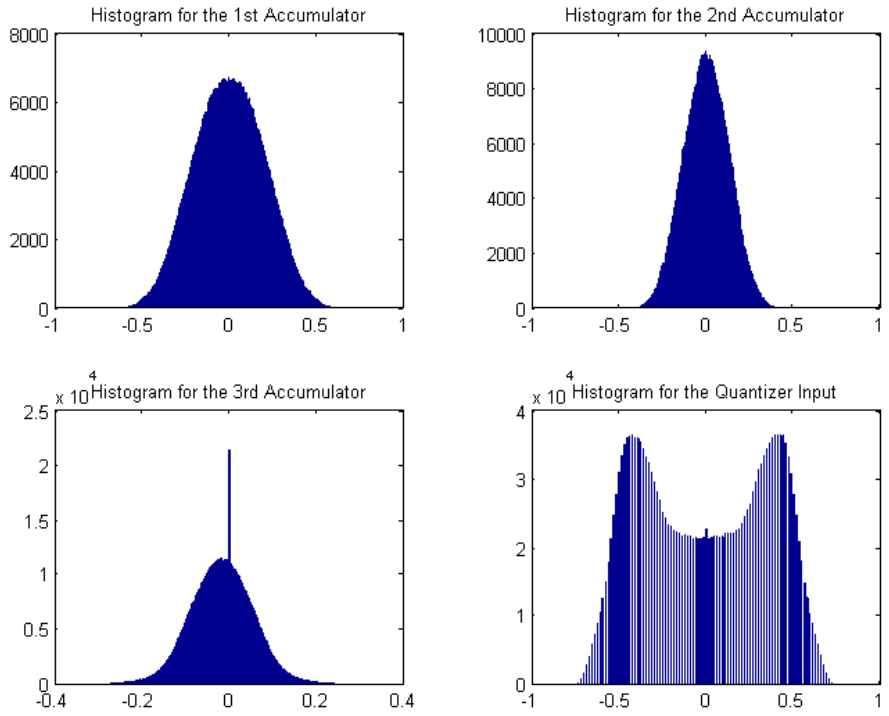

Figure 2.6: Histogram of the internal nodes in the ΔΣ modulator.

registers. Based on these criteria, a third-order modulator with a 7-level truncator, shown in Fig. 2.5, was realized. Since its in-band quantization noise is less than -95 dB, the total noise budget is dominated by the analog noise of the following stages,

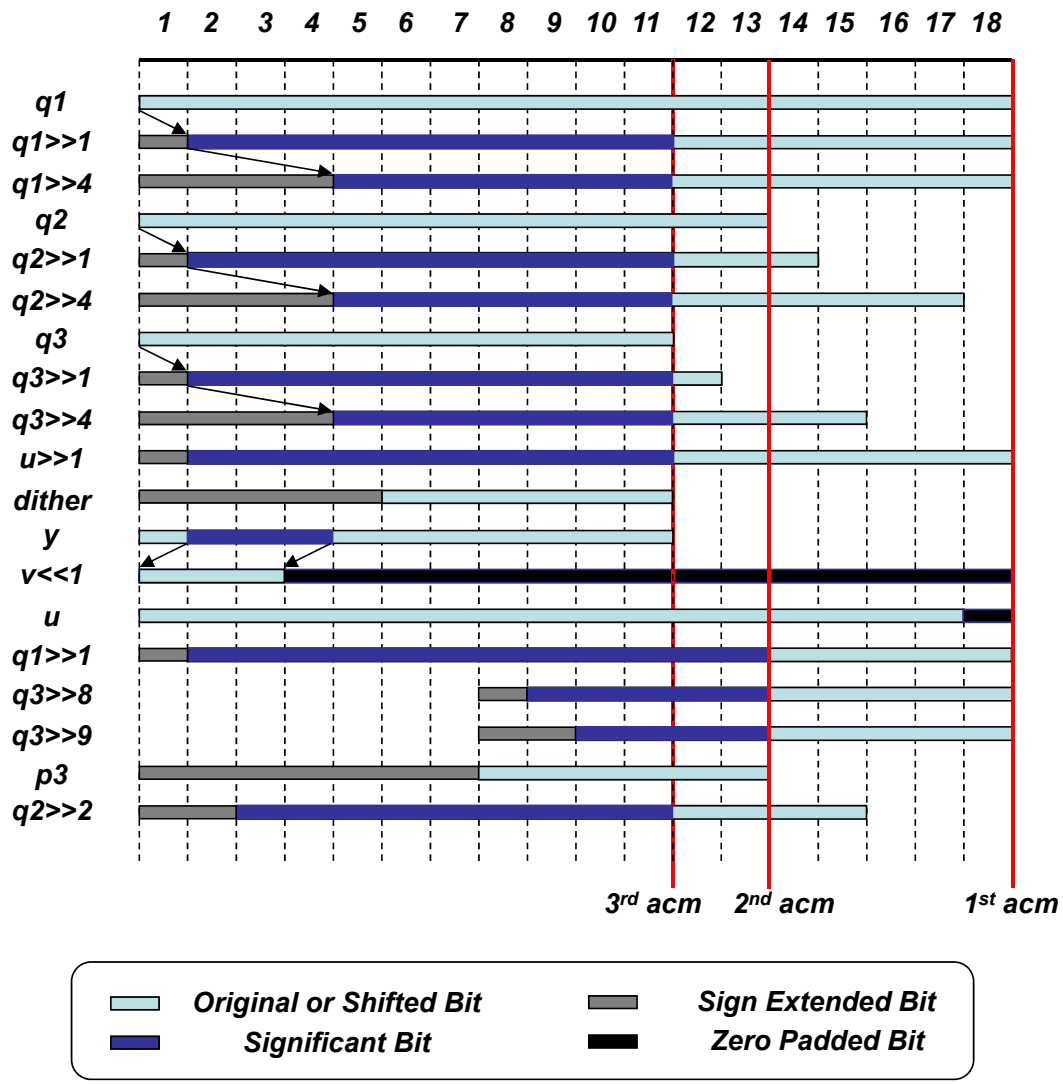

Figure 2.7: Bit alignment of the ΔΣ modulator.

such as 1/f and thermal noise, clock jitter noise, and mismatch noise.

The word length and power dissipation in each accumulator is reduced by using a direct feedforward path from the input to the quantizer. The word length in each accumulator was determined by requiring that its input-referred truncation noise power be -120 dB below the full-scale signal power [12]. After appending a guard bit to prevent the overload condition, the final word length was confirmed using fixed-point simulation. The histogram plots for the outputs of each accumulator and the

TABLE 2.2: THRESHOLDS OF THE 7-LEVEL QUANTIZER.

Quantizer Input (Y)	Input Range	Decision Range	Quantizer Output	Decimal Value
0 . 1 1 1 X	7 / 8 ≤ Y < 1	5 / 8 ≤ Y < 1	0 . 1 1	3 / 4
0 . 1 1 0 X	6 / 8 ≤ Y < 7 / 8			
0 . 1 0 1 X	5 / 8 ≤ Y < 6 / 8			
0 . 1 0 0 X	4 / 8 ≤ Y < 5 / 8	3 / 8 ≤ Y < 5 / 8	0 . 1 0	2 / 4
0 . 0 1 1 X	3 / 8 ≤ Y < 4 / 8			
0 . 0 1 0 X	2 / 8 ≤ Y < 3 / 8	1 / 8 ≤ Y < 3 / 8	0 . 0 1	1 / 4
0 . 0 0 1 X	1 / 8 ≤ Y < 2 / 8			
0 . 0 0 0 X	0 ≤ Y < 1 / 8	−1 / 8 ≤ Y < 1 / 8	0 . 0 0	0
1 . 1 1 1 X	−1 / 8 ≤ Y < 0			
1 . 1 1 0 X	−2 / 8 ≤ Y < −1 / 8	−3 / 8 ≤ Y < −1 / 8	1 . 1 1	−1 / 4
1 . 1 0 1 X	−3 / 8 ≤ Y < −2 / 8			
1 . 1 0 0 X	−4 / 8 ≤ Y < −3 / 8	−5 / 8 ≤ Y < −3 / 8	1 . 1 0	−2 / 4
1 . 0 1 1 X	−5 / 8 ≤ Y < −4 / 8			
1 . 0 1 0 X	−6 / 8 ≤ Y < −5 / 8	−1 ≤ Y < −5 / 8	1 . 0 1	− 3 / 4
1 . 0 0 1 X	−7 / 8 ≤ Y < −6 / 8			
1 . 0 0 0 X	−1 < Y < −7 / 8			

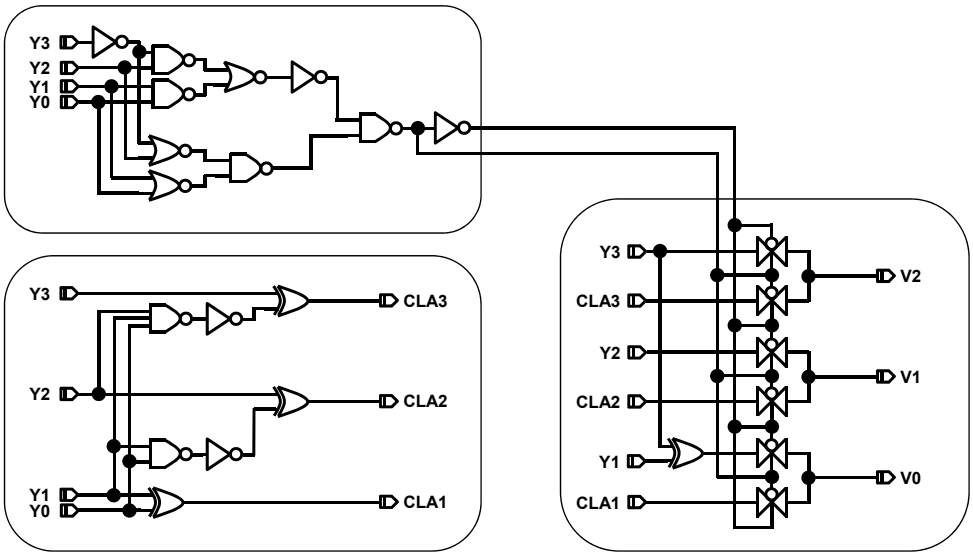

Figure 2.8: Schematic for 7-level quantizer.

input of the quantizer are shown in Fig. 2.6. They confirm the stable operation of the modulator, and a reasonable signal swing with a full-scale input signal. The resonator formed by the local feedback path ($-p_3$) minimizes the in-band quantization

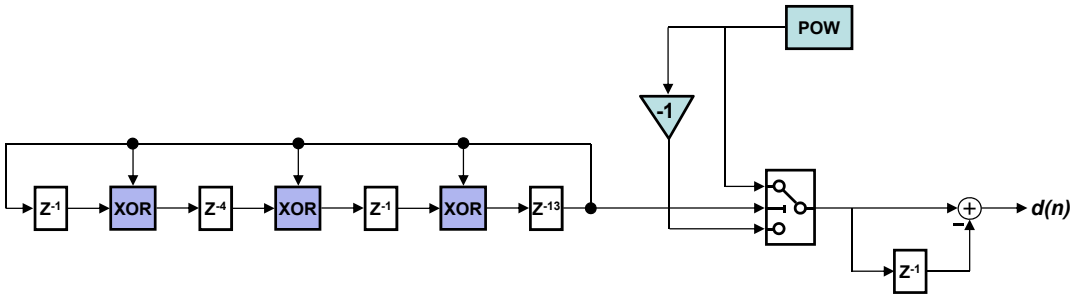

Figure 2.9: Dither from the LFSR in Galois configuration [13].

noise in the modulator loop by placing two complex-conjugate zeros close to the edge of the signal band. The optimized zeros of the noise transfer function NTF (one at DC and the other two at 20.4 kHz) in the third-order loop improves the signal-to-quantization noise ratio (SQNR) by 8 dB. The word length for the local feedback path p_3 is only 6, due to its small value. The bit alignment for each node in the modulator is shown in Fig. 2.7. A carry-save adder (CSA) is used at the summing node of the modulator to reduce the carry-propagation delay. The thresholds of the 7-level quantizer and its detailed schematic are shown in Table 2.2 and Fig. 2.8. Idle tones are suppressed by injecting a dither signal that is generated using a linear feedback shift register (LFSR) in Galois configuration. The generator polynomial of the LFSR is $x^{19}+x^6+x^5+x+1$. The pseudo-random binary sequence from the LFSR is scaled and differentiated before it is injected [13], as shown in Fig. 2.9. The scale factor is programmable down from 1/16 up to half the step size of the quantizer threshold. A single modulator is time-shared between the two channels, using the cascaded registers at doubled frequency, as in the interpolation filter.

The simulated and measured SNRs of the ΔΣ modulator with a 16b full-scale single-tone input were 95.9 dB and 95.6 dB, respectively. The measured spectrum at V_{DD} = 0.62V is shown in Fig. 2.10. The out-of-band tone at 44 kHz results from the limited (57 dB) stopband attenuation in the first HBF. This tone is reduced further by

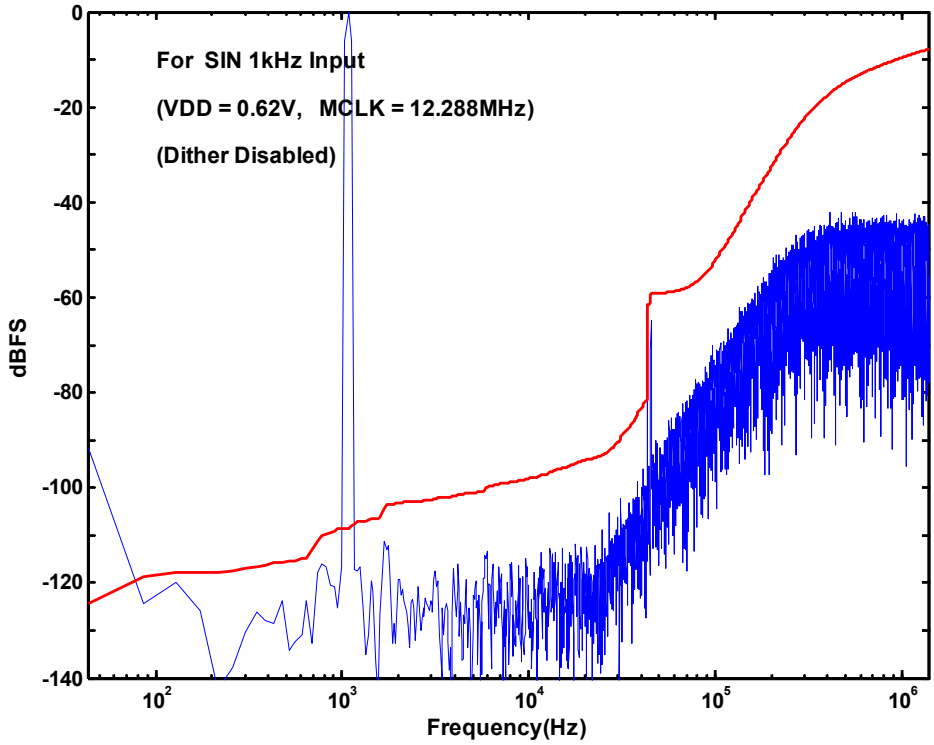

Figure 2.10: Measured spectrum for the ΔΣ modulator at V_{DD} = 0.62 V.

TABLE 2.3: MEASURED POWER DISSIPATION OF THE DIGITAL CHIP.

Supply	Power Consumption
0.7 V	0.098 mW
0.8 V	0.128 mW
0.9 V	0.162 mW
1.0 V	0.200 mW
1.1 V	0.242 mW
1.2 V	0.288 mW
1.5 V	0.495 mW
1.8 V	0.954 mW

the following analog filter. Measurements showed that this performance can be obtained with supply voltages in the range of 0.62 V ~ 1.8 V. The power consumption increases from 98 μW to 954 μW as shown in Table 2.3.

DSM Output (7 level)	2's Complement [B3 B2 B1]	Accumulator Input [~B3 B2 B1]	Pointer P(i+1)
-3/4	101	001 (1)	P(i)+1
-2/4	110	010 (2)	P(i)+2
-1/4	111	011 (3)	P(i)+3
0	000	100 (4)	P(i)+4
1/4	001	101 (5)	P(i)+5
2/4	010	110 (6)	P(i)+6
3/4	011	111 (7)	P(i)+7

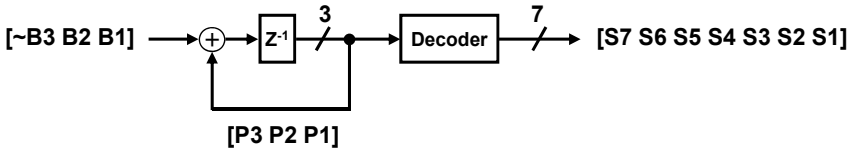

Figure 2.11: Pointer genertion for DWA. A 3b RCA with modulo 7 is used for the accumulator.

2.3.4. DWA

The DWA stage effectively filters the mismatch noise from the following multibit R-DAC. It is common to use 6 element DAC following a ΔΣ modulator with a 7-level quantizer. In this design, a seven-element DAC is created by adding one extra element to the usual six-element DAC, to shift the DAC mismatch noise and DWA-induced tones away from the signal band. An incremental DWA was applied to the $N + K$ element DAC, where N is the original DAC element number and K is the number of added extra elements. The tones are shifted to

$$f_{tone} = \frac{r}{2(N+K)} \cdot f_s \cdot m, \qquad m = 1,2,3\ldots \tag{2.1}$$

where r is the greatest common divisor (GCD) of N and $N + K$ [14],[15]. Specifically, the tones are shifted to the multiples of $f_s/14$, which is well outside of the signal band in this design. As shown in Fig. 2.11, a 2's complement number from the

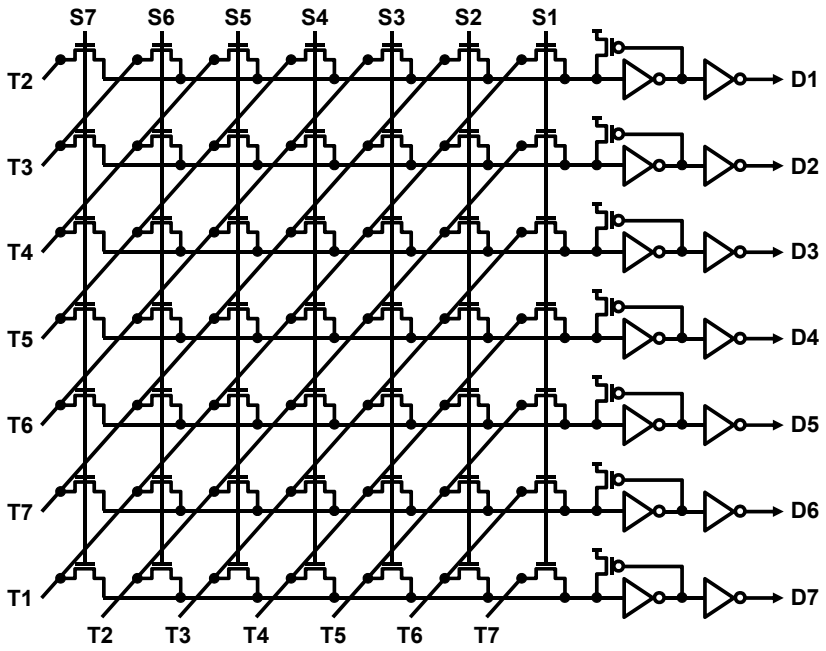

Figure 2.12: Rotating barrel shifter for DWA.

quantizer is converted to the unipolar integer number, by inverting its most significant bit (MSB) for the calculation of the pointer in DWA, where a 3b RCA with modulo 7 is used. The pointer output is decoded to control the rotating barrel shifter, as illustrated in Fig. 2.12. The DWA logic is also time-shared between both channels.

2.4. ANALOG STAGES

The analog stages were designed by Quingdong Meng.

2.4.1. Switched R-DAC

In the analog part of the system, the switched R-DAC is combined with a first-order FIR filter, a second-order Rauch filter, and the headphone driver, as shown in

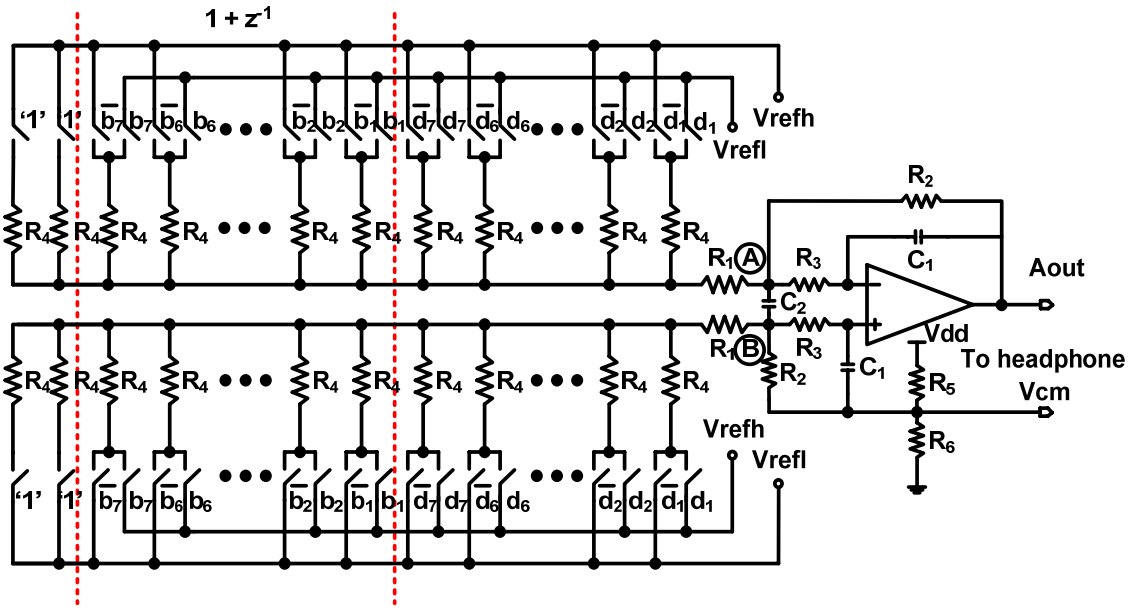

Figure 2.13: R-DAC with first-order FIR filter, second-order Rauch filter, and headphone driver (d_i = *delayed* b_i).

Fig. 2.13. It needs only one opamp per channel to implement the D/A conversion, the first-order FIR and second-order IIR filtering, as well as the power amplification for the headphone. The opamp provides a low-frequency virtual short circuit at nodes A and B for the DAC output currents. An analog first-order FIR filter is also integrated into this stage, by duplicating the original DAC elements with a control signal delayed by one clock cycle. This introduces a zero at one-half the sampling frequency, and reduces the clock jitter sensitivity. The embedded second-order Rauch low-pass filter has a -3 dB cutoff frequency at 150 kHz, and its pole Q is 0.707. The values of all resistors and capacitors were optimized to achieve the minimum capacitor area for the given pole Q, cutoff frequency, and the targeted SNR.

In the switched R-DAC shown in Fig.2.13, all switches are connected either to the high reference (V_{DD}) or to the low reference voltage (GND). This avoids the problem arising with floating switches. The value of R_1 was chosen carefully to reduce the

size of the R_4, without sacrificing its matching accuracy. DWA technique is used to provide first-order noise shaping for the mismatch error among the DAC elements. Four extra resistors are added to make the output common-mode voltage equal to $V_{DD}/2$ for maximum voltage swing.

The operation of the DAC is affected by the residual mismatch error after DWA, and by the clock jitter. Both theoretical analysis and simulations predict that these effects will be negligible in this device, due to the relatively high OSR (64), the conservative design of the DSM, and the noise shaping effect of the FIR filter. The measured results confirmed this prediction.

2.4.2. Analog low pass filter and headphone driver

As mentioned earlier, a second-order Rauch filter (Fig. 2.14) is used to suppress out-of-band noise. The transfer function of the filter (for the differential input and single-ended output) is

$$H(s) = \frac{-R_2 / R_1}{2R_2R_3C_1C_2s^2 + (R_2 + R_3 + R_2R_3 / R_1)s + 1} \tag{2.2}$$

The external bypass capacitor (10 μF) at V_{cm} node provides a solid ac ground, even at very low frequencies. The DC gain of the filter is chosen as -6 dB, since the negative and positive inputs of this filter are both full-scale signals coming from the DAC output. Assuming $R_3 = mR_2 = mR$, $C_2 = nC_1 = nC$, the -3 dB cutoff frequency and pole Q are

$$\omega_{-3dB} = \frac{1}{\sqrt{2mnRC}} \tag{2.3}$$

$$Q = \frac{\sqrt{2mn}}{1 + 1.5m} \tag{2.4}$$

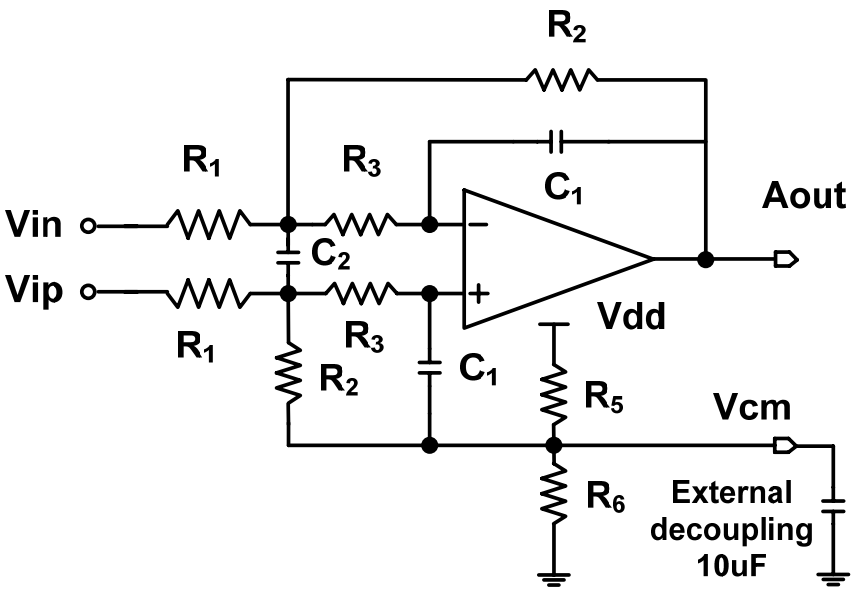

Figure 2.14: Second-order Rauch low-pass filter.

TABLE 2.4: COMPONENTS VALUES FOR THE SECOND-ORDER RAUCH FILTER.

R_1	30 kΩ
R_2	15 kΩ
R_3	10 kΩ
R_5, R_6	45 kΩ
C_1	50 pF
C_2	75 pF

Since the resistor value R_1 is defined by the specifed fixed gain of the filter (0.5 in this design), it does not enter into the formulation (2.3) and (2.4) of the filter optimization. The filter -3 dB cutoff frequency is chosen to be 150 kHz, and Q is 0.707. The high cutoff frequency prevents the poorly defined -3 dB cutoff frequency from causing any gain drooping in audio band, and still provides sufficient suppression for the shaped high- frequency quantization noise. Note that the pole Q is well defined, since it only depends on the ratios R_2 / R_1 and C_2 / C_1 as indicated by (2.4). The input/output common-mode level is set by the resistor divider containing

R5 and *R6*. Minimizing the total capacitor area is critical in reducing the whole DAC area due to the low -3 dB cutoff frequency at 150 kHz. For the circuit shown in Fig. 2.15, the total capacitor area is

$$C_{total} = (1+2n)C \tag{2.5}$$

Using (2.4),

$$C_{total} = (1+2n)C = (1+\frac{Q^2(1+1.5m)^2}{m})C \tag{2.6}$$

Taking the derivative with respect to *m*, the minimum capacitor area is achieved with $m = 2/3$. Since $Q = 0.707$, $n = 1.5$ results. From the noise budget for the output-referred resistor noise, the resistor values can be calculated. Substituting them into (3) gives the capacitor values. Table 2.4 summarizes the nominal values for the components of the Rauch filter.

The amplifier in the filter provides the power amplification for driving the headphone as well. It must achieve a high DC gain, and also have the capability to drive a load of a 16 Ω resistor in parallel with a 300 pF capacitor, with sufficiently low thermal and flicker noises, all from a 0.8 V power supply voltage. Fig. 2.15 shows the schematic diagram of the amplifier. Since the filter has a differential input and single-ended output, it does not need a CMFB amplifier to stabilize the output common-mode level. The amplifier has two stages: a folded cascode input stage to provide a voltage gain, and a class-AB output stage to provide the headphone driving capability. For sub-1V operation, it is necessary to keep the output common-mode voltage at $V_{DD}/2$, to maximize the output signal swing. For the amplifier shown in Fig. 2.15, since the input and output common mode levels are the same, the minimum power supply voltage is

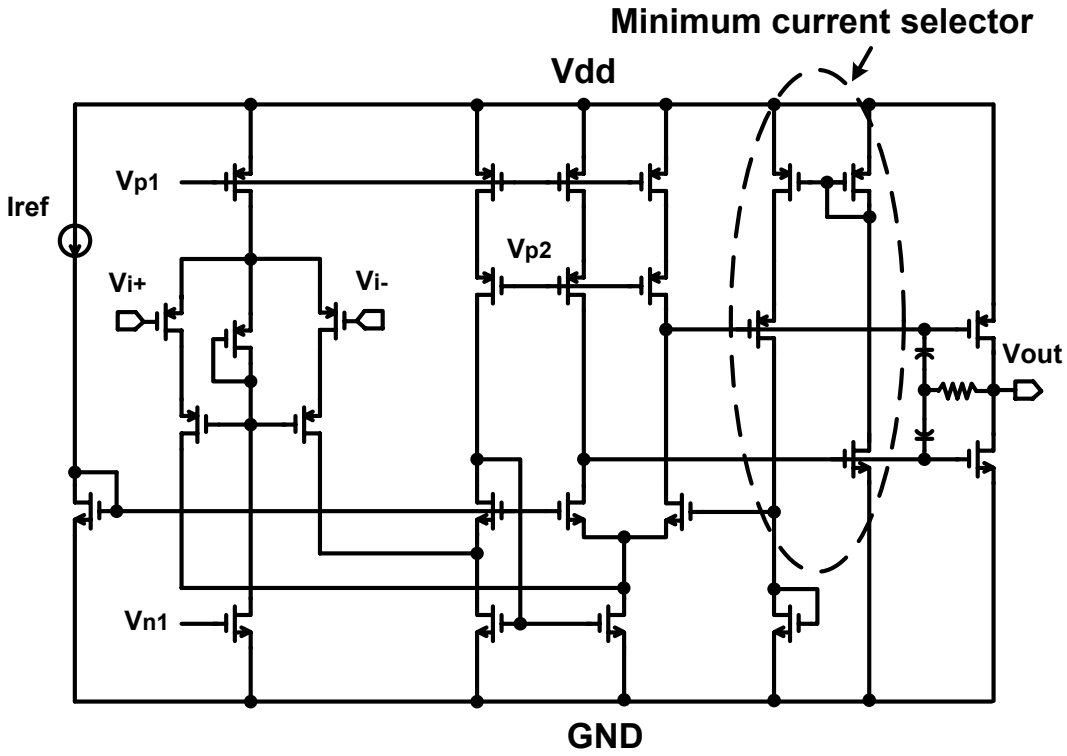

Figure 2.15: Opamp with class-AB output stage.

$$V_{DD\_MIN} = 2V_{th} + 4(V_{gs} - V_{th}) \tag{2.7}$$

For the given process, the threshold voltage is around 300 mV, which means that the gate overdrive voltage can be as low as 50 mV. This makes a folded-cascode first stage possible, and avoids a cascaded multi-stage configuration with complicated nested Gm-C or Miller compensation needed to guarantee stability [16]. The output stage of the opamp [17] incorporates a minimum current selector in a feedback loop, which contains the split output transistors of the first stage. Since the output of the minimum current selector is equal to the bias current *Iref*, the bias current of the output transistors is determined by the current mirror ratio in the minimum current selector. The simulated voltage gain for this amplifier with a 16 Ω resistive and 300 pF capacitive load is 65 dB, and the UGBW is 7 MHz.

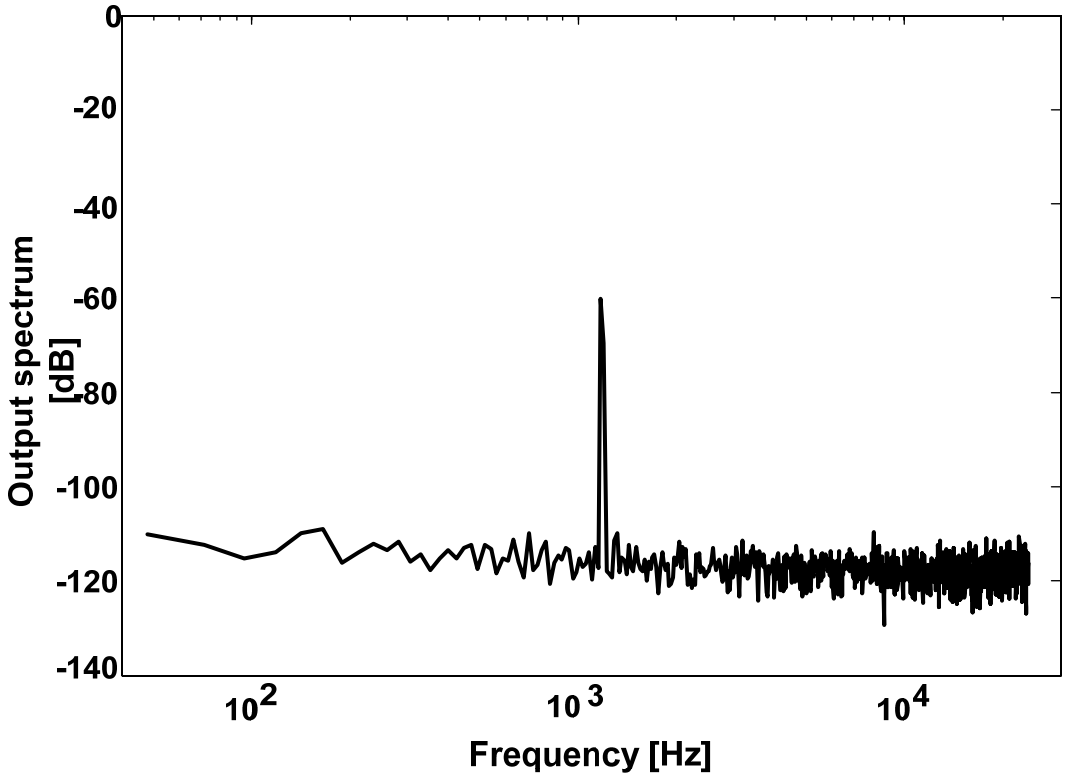

Figure 2.16: Measured output spectrum with a 1.17 kHz -60 dB sine-wave input at V_{DD} = 0.8 V.

2.5. EXPERIMENTAL RESULTS

The DAC was fabricated in the Asahi Kasei Microsystem 2P3M 0.35μm CMOS technology, and occupies 1.6 mm × 0.9 mm and 1.6 mm × 1.3 mm active die area for the digital and the analog chips, respectively. Both digital and analog chips are mounted on the same printed circuit board and the 7 DWA output signals from the digital chip are connected to the corresponding input ports of the analog chip. A Tektronix AWG520 (arbitrary waveform generator) was used to generate the 1b serial digital input and clock, and an Audio Precision audio analyzer was used for the measurements. Fig. 2.16 shows the measured output spectrum for a 1.17 kHz, -60 dB sine-wave input using a 0.8 V power supply. There are no idle tones present in the

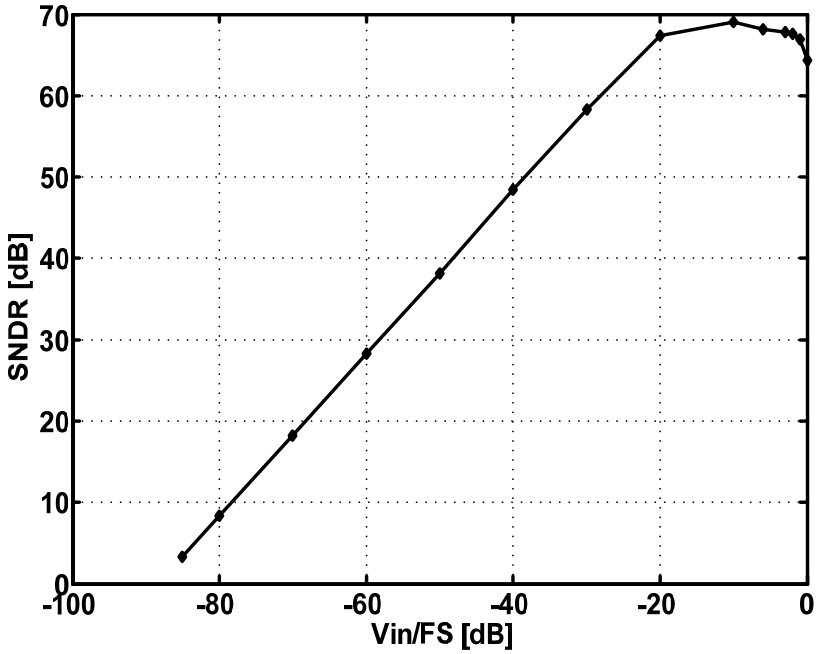

Figure 2.17: Measured SNDR versus input signal power with a 1.17 kHz sine-wave input at V_{DD} = 0.8 V.

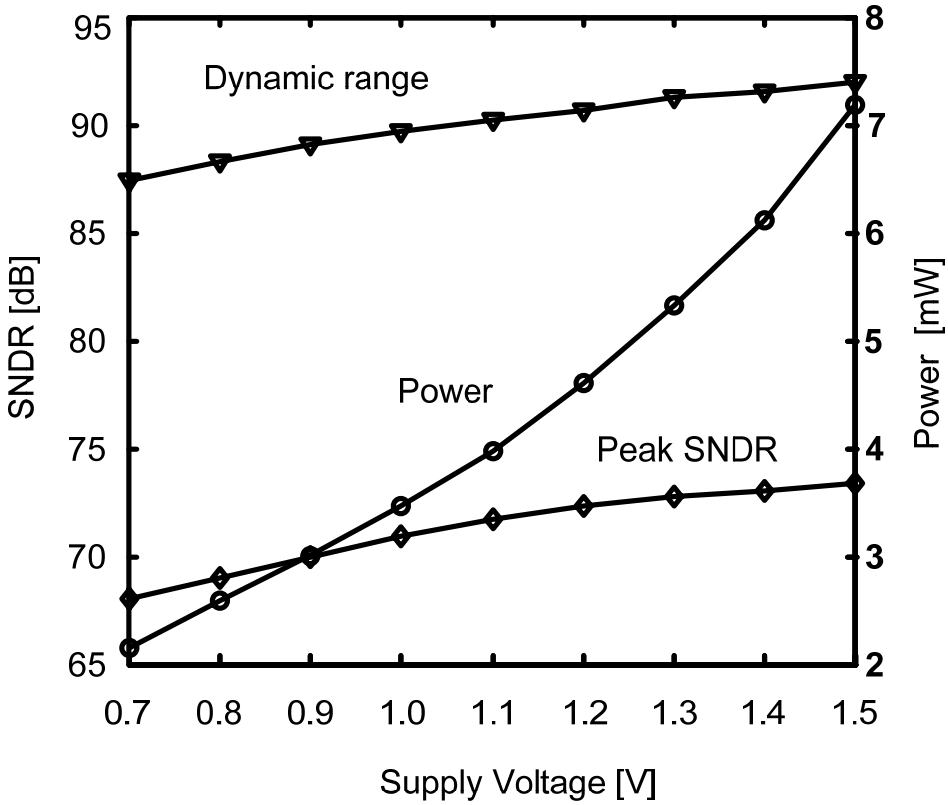

Figure 2.18: Measured performance with supply voltage.

TABLE 2.5: PERFORMANCE SUMMARY.

Power supply voltage	**0.8 V**
Signal bandwidth	**24 kHz**
Clock frequency	**3.072 MHz**
Oversampling ratio	**64**
Load	**Headphone (16 Ω ll 300 pF)**
Total power consumption	**2.6 mW**
Output range	**0.45 V_{PP} (single-ended)**
Peak SNDR	**69 dB @ Vdd = 0.8 V** **68 dB @ Vdd = 0.7 V**
Dynamic range	**88 dB @ Vdd = 0.8 V** **87 dB @ Vdd = 0.7 V**
Active die area	**Digital chip: 1.6 X 0.9 mm^2** **Analog chip: 1.6 X 1.3 mm^2**
Technology	**0.35μm CMOS**

quantization noise. The spurs caused by DWA rotation are also negligible (below -109 dB). The SNDR performance versus input signal power from -85 dB to 0 dB (relative to 56% of the 0.8 V supply voltage) is shown in Fig. 2.17. The SNDR was measured over a 20 Hz to 24 kHz audio band. Without A-weighting, the prototype achieved a 69 dB peak SNDR and an 88 dB DR with a 0.8 V supply voltage. Using a 0.7 V supply, the peak SNDR and the DR were reduced to 68 dB and 87 dB, respectively. The peak SNDR is limited by the second harmonic distortion of the single-ended opamp for large input signal swings. The peak SNDR and DR both gradually improve for supply voltages increasing from 0.7 V to 1.5 V, as shown in Fig. 2.18. The chips consume 2.6 mW (0.1 mW for the digital chip, 2.5 mW for the analog chip,) with a 0.8 V supply. Table 2.5 summarizes the performance of the chip for 0.8 V supply. The die photographs are shown in Fig. 2.19. The performance of

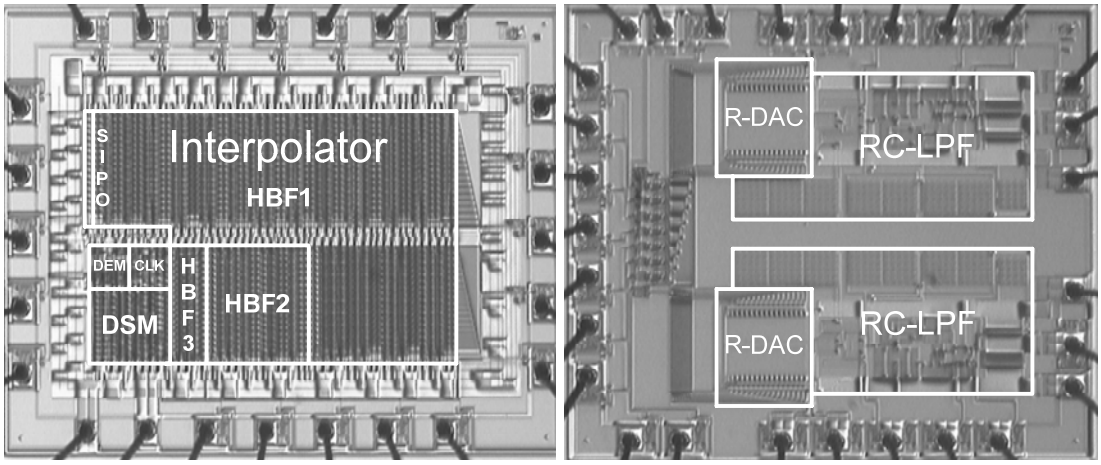

Figure 2.19: Die micrographs.

TABLE 2.6: PERFORMANCE COMPARISON.

Refs	DR/SNDR [dB]	Supply [V]	Load	Power [mW]	Process [μm CMOS]	Headphone Driver
[Adams98] [18]	113/100	5.0	1 kΩ	250	0.6	No
[Fujimori00] [2]	120/102	5.0	0.6 kΩ	310	0.5	No
[Fujimori98] [3]	87/81	1.5	10 kΩ	4.1	0.6	No
[Annovazzi02] [13]	98/86	3.3	15 kΩ	56	0.35	No
[Colonna05] [19]	97/88	3.3	40 kΩ	14.5	0.35	No
This work	88/69	0.8	16 Ω	2.6	0.35	Yes

this device is compared with the other audio ΔΣ DACs published earlier in Table 2.6.

2.6. SUMMARY

A 0.8 V third-order ΔΣ DAC with headphone driver was presented. It incorporates a novel digital ΔΣ modulator and interpolation filter. The analog circuitry requires only one opamp per channel, shared by the internal DAC, the FIR and the second-order Rauch low-pass filter, as well as by the headphone driver for 16 Ω resistor and 300 pF capacitor. The prototype ICs, implemented in a 0.35μm

CMOS process, achieved 88 dB DR, while consuming 2.6 mW from a 0.8 V supply for the dual channels.

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CHAPTER 3. NOISE-COUPLED MULTI-CELL DELTA-SIGMA ADCS

Abstract

Two novel architectures are proposed for delta-sigma ADCs. The first one is the multi-cell structure, with common input and summed outputs. It allows flexible trade-off between resolution and power dissipation, and also improves the SQNR due to the uncorrelated nature of the quantization errors of the cells. The second structure couples quantization noise into the modulator loop, to enhance the noise shaping. The coupling may occur between the cells of a multi-cell structure (cross-coupling), or within a single loop (self-coupling). Noise coupling will raise the effective order of the noise transfer function, without introducing stability issues. While this feature is similar to the operation of the cascade (MASH) structure, the noise-coupled modulator does not rely on noise cancellation, and hence is less sensitive to analog circuit imperfections than MASH. Both extensive simulations and experimental results verify that the proposed schemes have significant advantages over existing ones under practical fabrication constraints.

3.1. INTRODUCTION

Delta-sigma (ΔΣ) analog-to-digital converters rely on oversampling and noise shaping to achieve very high accuracy even using inaccurate analog components [1]. The accuracy improves with higher oversampling ratio (OSR), but the OSR is limited by the bandwidth of the amplifiers used and by the permissible power dissipation. The performance can also be enhanced by using higher-order loop filters,

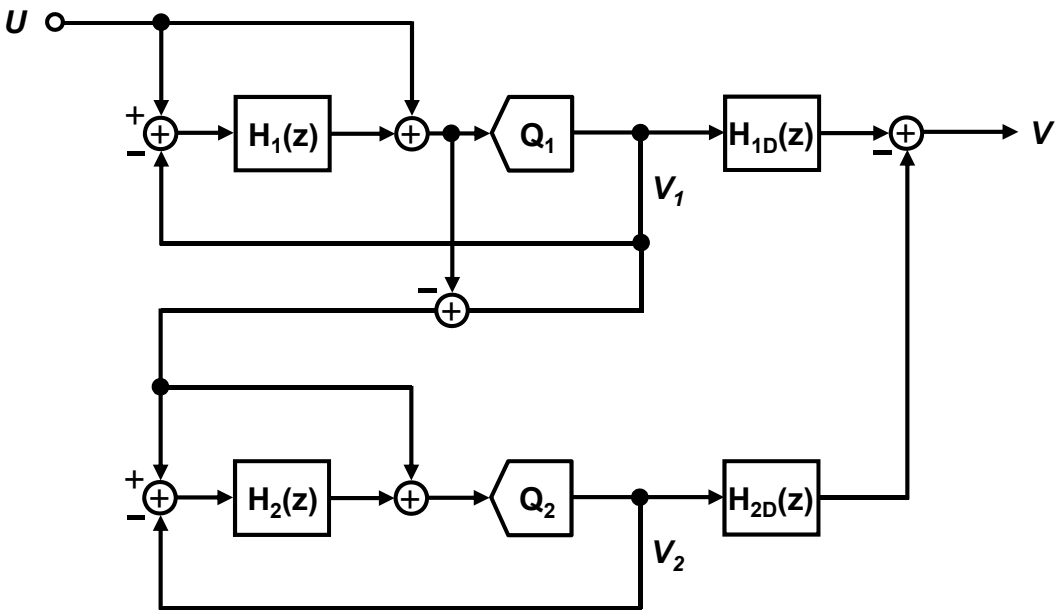


Figure 3.1: Two-stage cascaded (MASH) delta-sigma ADC.

but this may lead to instability. Finally, higher resolution may also be attained by embedding a multibit internal quantizer in the loop. However, the complexity of the quantizer and the required dynamic matching logic increases exponentially with the number of bits used in the quantizer, so this approach is also limited in effectiveness. A different structure, which combines noise shaping with noise cancellation, is used in the cascade or MASH modulator as illustrated in Fig. 3.1. Under ideal conditions, a MASH structure provides a noise transfer function (NTF) equal to the product of the NTFs of several modulator loops coupled together. Thus, for example, fourth-order noise shaping may be achieved by coupling two second-order loops. Since second-order loops are inherently stable, while fourth-order ones are not, MASH allows high-order noise filtering without stability problems.

A shortcoming of the MASH ADC is that it relies on the accurate matching of one or more analog NTFs to digital ones to achieve the cancellation of unfiltered or poorly filtered noise from the input stage(s). For high-accuracy and high-OSR ADCs

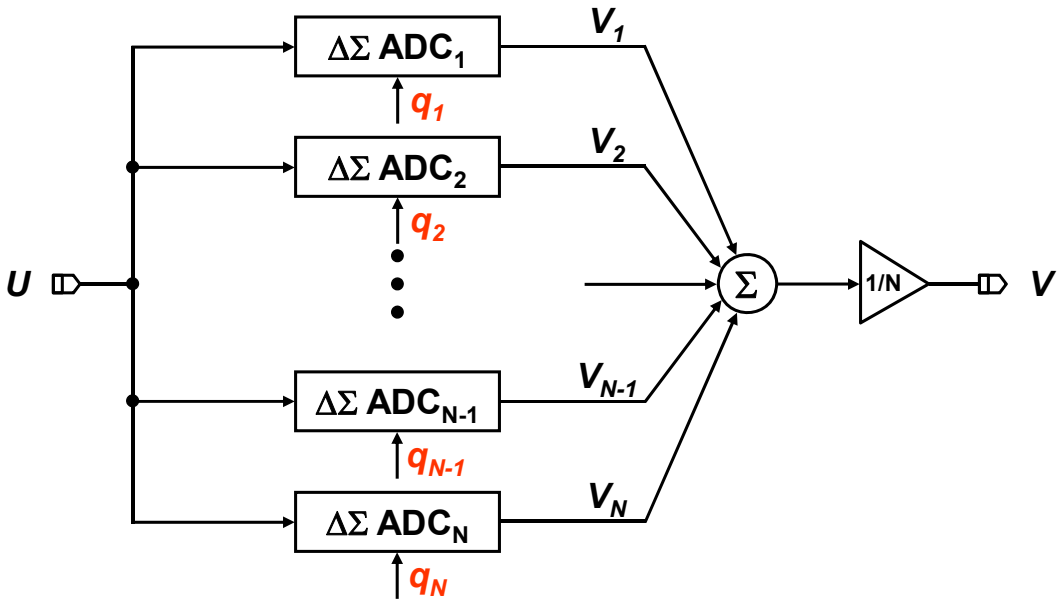


Figure 3.2: Multi-cell delta-sigma ADC.

this puts difficult constraints on the analog circuitry in these stages. While it is possible to overcome this problem using adaptive tuning of the digital filters [2], this requires additional digital logic.

In this chapter, two alternative configurations are proposed for ΔΣ ADCs. The first one (Fig. 3.2) contains a multiplicity of ΔΣ loops, with a common input *u(n)*. The individual output signals $v_i(n)$ are averaged to produce the ADC output *v(n)*. As shown in Section 3.2, to a first approximation this segmentation of a single ΔΣ loop into the multi-cell structure does not require added power or chip area [3][4]. It does, however, enhance the signal-to-quantization-noise ratio (SQNR), and increases the potential for trade-offs between SQNR and power dissipation.

The second proposed structural innovation is noise coupling, discussed in Section 3.2. The basic idea is illustrated in Fig. 3.8. for a multi-cell ADC configuration, and in Fig. 3.11 for a single-cell ADC. In the structure of Fig. 3.8, the quantization noise of stage *i* is coupled into the quantizer of stage *j* via coupling branch G_{ji}, and vice versa. Assuming symmetry, the noise transfer functions of both branches have been

transformed from *NTF* into *(1 - G)·NTF*. Thus, the order of noise filtering can be increased. If the coupling branch is passive, the resulting enhanced noise shaping does not require additional amplifiers and bias power. The same considerations hold for the self-enhanced structure of Fig. 3.11. Sections 3.3-3.5 discuss 3 prototype designs based on the proposed new structures, and measured results verify the theoretical results derived in the preceding Sections.

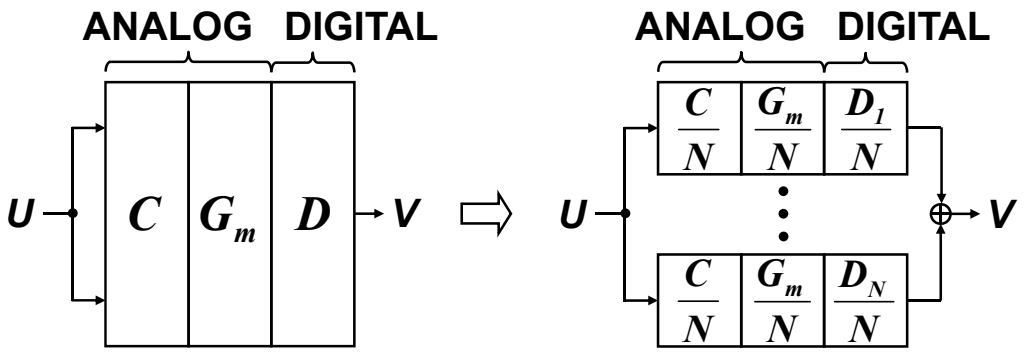
3.2. PROPOSED ARCHITECTURES

3.2.1. Multi-cell delta-sigma ADC

The multi-cell delta-sigma ADC architecture is an extension of split delta-sigma ADC configuration. The z-transform of the output signal of the basic multi-cell structure of Fig. 3.2 can be written in the form

$$V(z) = STF \cdot U(z) + \frac{1}{N}\sum_{i=1}^{N} STF \cdot N_i(z) + \frac{1}{N}\sum_{i=1}^{N} NTF \cdot Q_i(z) \qquad (3.1)$$

Here, *STF* and *NTF* are the signal and noise transfer functions, respectively, of all cells, assumed at this point to be perfectly matched. $Q_i(z)$ is the quantization noise of cell *i*, and $N_i(z)$ represents all other noises (thermal noise, 1/f noise, etc.) of stage *i*, referred to its input terminals. It will next be shown that (to a first approximation) the bias power and chip area of this segmented realization need not be larger than what a single-cell realization for the same specifications would require. Assuming that N_i is dominated by thermal and 1/f noises of the input stage (which is usually a valid assumption), the input capacitor of the first stage in the single-cell realization is determined by the permissible thermal noise power $\sigma^2 = kT/C$. The minimum transconductance G_m of the input stage is then given by the specified unity-gain band



Speed	$f_T = l \cdot \frac{G_m}{C}$	$f_{T_s} = l \cdot \frac{G_m / N}{C / N} = l \cdot \frac{G_m}{C}$
Power	$P = m \cdot G_m$	$P_s = N \cdot m \cdot \frac{G_m}{N} = m \cdot G_m$
Noise	$\sigma^2 = n \cdot \frac{kT}{C}$	$\sigma_s^2 = \frac{1}{N^2} \cdot N \cdot n \cdot \frac{kT}{C / N} = n \cdot \frac{kT}{C}$
	$\sigma_q^2 = n_q \cdot E_{rms}^2$	$\sigma_{q,s}^2 = \frac{1}{N^2} \cdot N \cdot n_q \cdot e_{rms}^2 = n_q \cdot \left(\frac{e_{rms}}{\sqrt{N}} \right)^2$

Figure 3.3: Splitting is free for multi-cell delta-sigma ADC.

width $\omega_u = G_m/C$. Finally, the required bias power P of the input stage (for fixed aspect ratios) is $P = m \cdot G_m$, where m is a circuit constant.

Consider next the N-cell realization. The input signal U will remain unchanged. Assuming equal input capacitors, each of value c, the thermal noise power at the output will be $(1/N^2) \cdot N \cdot kT/c$, where the first factor is due to the multiplication by $1/N$ after the output adder, and the factor N due to the addition of N uncorrelated noises. For the same output noise as in the single-cell ADC, $c = C/N$ results. Hence, the total input capacitance in the N-cell realization remains C. To retain the same unity-gain bandwidth in the multi-cell structure, the transconductance g_m of each cell needs to satisfy $g_m/c = g_m/(C/N) = G_m/C$. This gives $g_m = G_m/N$. The power required by the

first stage is then $p = m \cdot g_m = m \cdot G_m/N = P/N$. Thus, the total power required by the input stages remains unchanged. Assuming the same channel lengths in all input amplifiers, the areas of input devices will be scaled down by N in the multi-cell implementation, and the 1/f noise powers will be scaled up by the same factor. Hence, the overall SNR associated with the input noise N_i will be the same. The total area occupied by the input capacitors and amplifiers will also be approximately the same, as will be the bias power. The area occupied by the quantizers, however, will be increased.

The multi-cell realization clearly offers increased flexibility for the ADC. For a fabricated converter, by putting some of the cells in a sleep mode, the bias power can be reduced at the cost of reduced SNR. If necessary, this can be done on a dynamic basis, depending on the changing requirements and the properties of the input signal. In addition, it turns out that for practical circuits, the quantization noises q_i of the cells become nearly completely uncorrelated after only about 50~100 clock periods. This advantageous fact is due to several factors, including thermal and 1/f noises, dc offsets, and the combination of mismatch errors and nonlinearities of the analog components. As an illustration, Fig. 3.4 and Fig. 3.5 show the time dependence of the crosscorrelation factor

$$corr\,(1,2)\big|_{t=nT} = \frac{1}{n}\sum_{k=1}^{n} q_1(k)\cdot q_2(k) \tag{3.2}$$

for the quantization noises $q_1(k)$ and $q_2(k)$ of two nominally identical delta-sigma ADCs under ideal and nonideal conditions, respectively. The assumed nonidealities are coefficient errors in modulator due to capacitor mismatch, nonlinearities of opamp in integrator, nonlinearities of DAC, and thermal noises. Simulations indicated that for realistic models the noise correlation decreases drastically after only 50~100 clock periods. Due to the low correlation in the output signal, after

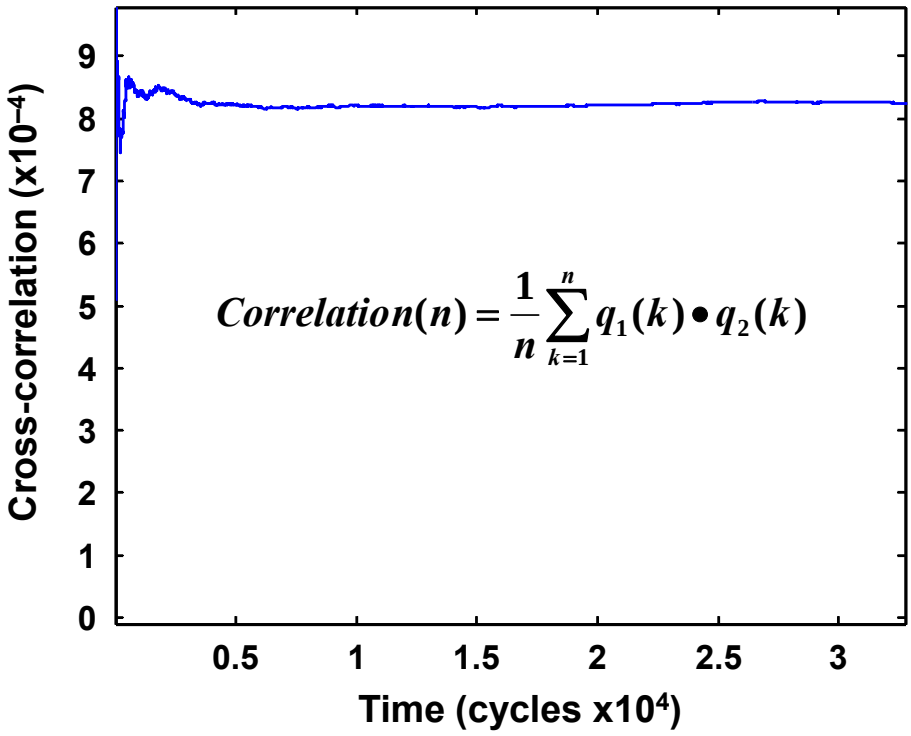


Figure 3.4: Crosscorrelation of quantization noise for two ideal ΔΣ ADCs.

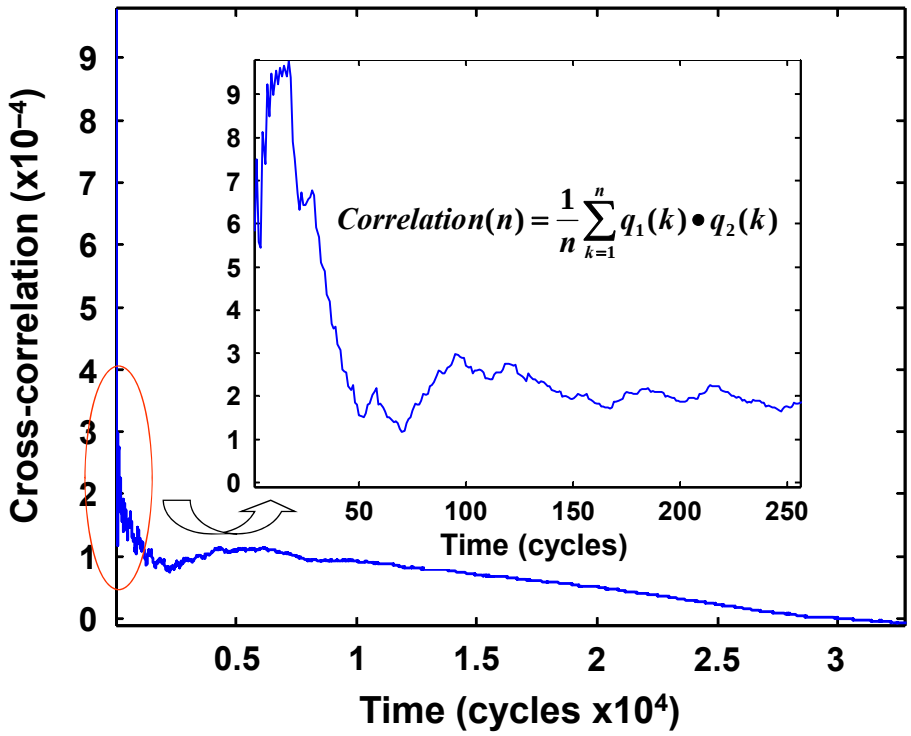


Figure 3.5: Crosscorrelation of quantization noise for two nonideal ΔΣ ADCs.

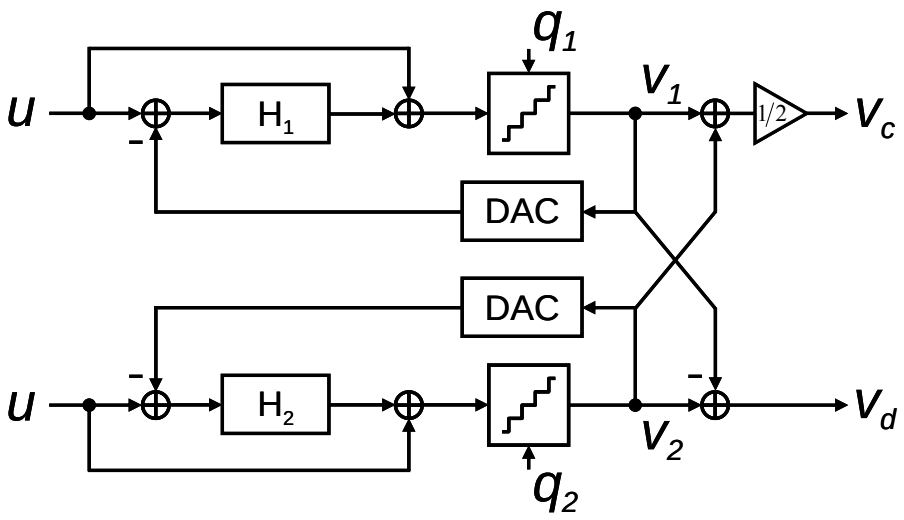


Figure 3.6: Conventional split delta-sigma ADC.

some 100 clock periods, only the quantization noise powers will be added, resulting in a reduction of the noise power by a factor *1/N*, corresponding to an increase of the SQNR by *10·log N*. As shown in the next Section, additional improvements in the SQNR can be obtained by using noise coupling.

3.2.2. Noise-coupled delta-sigma ADC [5][6]

The basic idea of noise coupling is illustrated for split delta-sigma ADC shown in Fig. 3.6 to simplify the associated argument and generalized to a multi-cell delta-sigma ADC in the following Section. Since split delta-sigma ADC is a special case of multi-cell delta-sigma ADC configuration, the argument in this section can be extended easily to any number of delta-sigma ADC cells without loss of generailty. Noise coupling increases the effective order of noise shaping for overall loops. Thus, using second-order cells and first-order coupling branches, third-order noise shaping can be obtained as shown below. Fig. 3.7 shows the block diagram of the proposed structure. Each half of the delta-sigma ADC has an extra delayed quantization signal

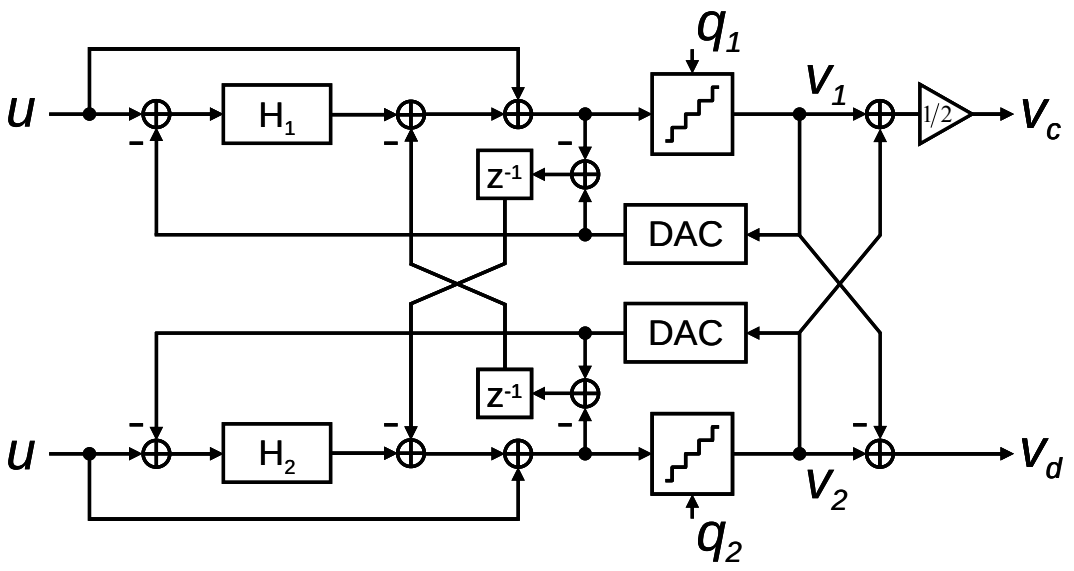


Figure 3.7: Proposed enhanced split delta-sigma ADC.

injected from the other half. *Vc* is the signal output, obtained as the average of the output codes, and *Vd* is the calibration output given by the difference between them. Inherent modulator mismatches between the loops and the uncorrelated thermal noises justify the assumption of statistical independence between the quantization noises.

Applying a linear model to both quantizers, the z-domain outputs from the loops can be obtained

$$V_1 = U + NTF_1 \cdot (Q_1 - z^{-1}Q_2) \tag{3.3}$$

$$V_2 = U + NTF_2 \cdot (Q_2 - z^{-1}Q_1) \tag{3.4}$$

Here, NTF_1 and NTF_2 denote the noise transfer functions, while Q_1 and Q_2 are the quantization noises in the two loops. Hence, the signal output *Vc* of the split modulator is given by

$$V_c = U + (1 - z^{-1}) \cdot NTF \cdot (Q_1 + Q_2)/2 \tag{3.5}$$

where $NTF_1 = NTF_2 = NTF$ is assumed. (Good matching between NTF_1 and NTF_2 is relatively easy to achieve in a split ADC, since they are realized by nominally identical circuits.) Equation 3.5 clearly demonstrates the noise shaping enhancement. For example, if each modulator contains a second-order loop, then the overall modulator will deliver third-order noise shaping. Despite its enhanced noise shaping, the second-order stability condition is preserved, since the injected quantization noise from the other loop is uncorrelated with the signals in the receiving loop. In fact, in addition to noise cancellation, the injected noise also acts as a dither signal, reducing tones and harmonic spurs. The lack of correlation is due to several factors, including thermal and 1/f noise and offset, as well as mismatch errors combined with nonlinearities of the opamps and switches. Unlike in MASH, this architecture does not require stringent matching of the noise transfer functions in the analog and digital domains. This allows the use of relatively low-gain opamps for the integrators, an advantage for wideband and low power applications.

3.2.3. Higher-order noise coupling [7][8]

The noise coupling scheme described in the previous section can be extended to higher-order enhancement. Fig. 3.8 illustrates a portion of a generalized split-architecture delta-sigma ADC with mutual noise coupling. The quantization error q_j of stage j is coupled into stage i in such a way that its z-transform Q_j appears in the output signal V_i of stage i in the form $-NTF_i \cdot G_{ij} \cdot Q_j$. Here, G_{ij} is the transfer function applied to the quantization error Q_j of stage j before injecting it into the summing node of stage i. Combined with the term $NTF_j \cdot Q_j$ appearing in the output V_j of stage j, Q_j is multiplied by $NTF' = NTF \cdot (1-G_{ij})$ in the overall ADC output V. (Here, $NTF_i = NTF_j = NTF$ is assumed.) G_{ij} can be chosen so as to provide the desired enhancement

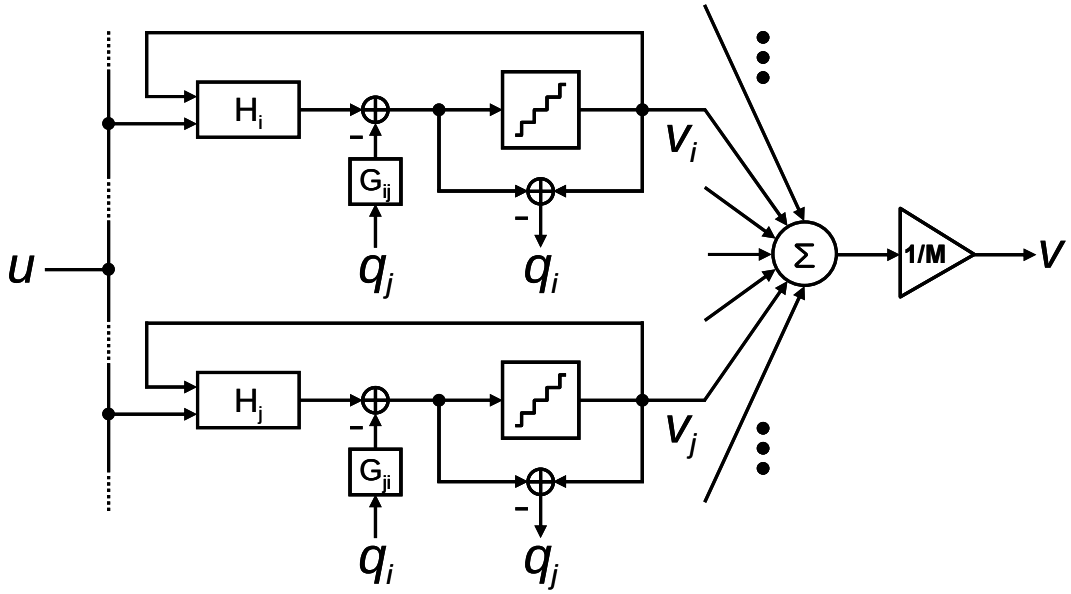


Figure 3.8: Multi-cell delta-sigma ADC with noise coupling.

of the noise shaping. If, e.g., $NTF' = NTF \cdot (1-z^{-1})^2$ is required, then $G_{ij} = 2z^{-1}-z^{-2}$ may be used. Similarly, the *NTF* of stage *i* can be enhanced by coupling q_i into stage *j*, or any other stage in the ADC. In general, for $NTF' = NTF \cdot (1-z^{-1})^N$, G_{ij} can be expressed as

$$G_{ij} = z^{-1} \sum_{k=0}^{N-1} (1 - z^{-1})^k \tag{3.6}$$

Thus, using second-order cells and also second-order coupling branches, fourth-order noise shaping can be obtained As discussed in previous section, the coupled noise q_j is nearly completely uncorrelated with the native noise q_i, and so it acts as a dither, not as a feedback signal, in the loop. Thus, the stability of the individual loops is comparable to that of a dithered second-order stage, i.e., quite robust. Furthermore, the dithering effect spreads the power of the spurs caused by harmonics and idle tones over the whole spectrum, thus improving the spurious-free dynamic range (SFDR) significantly.

This effect is illustrated in Fig. 3.9 and Fig. 3.10, which compare the simulated

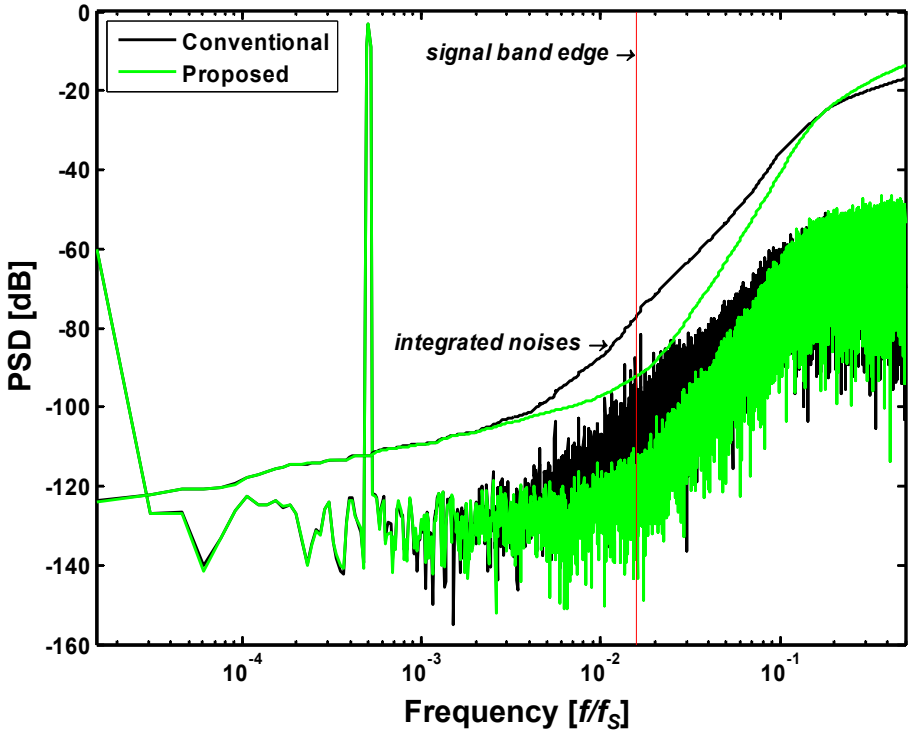


Figure 3.9: PSDs for split ΔΣ ADC without and with 1st-order noise coupling.

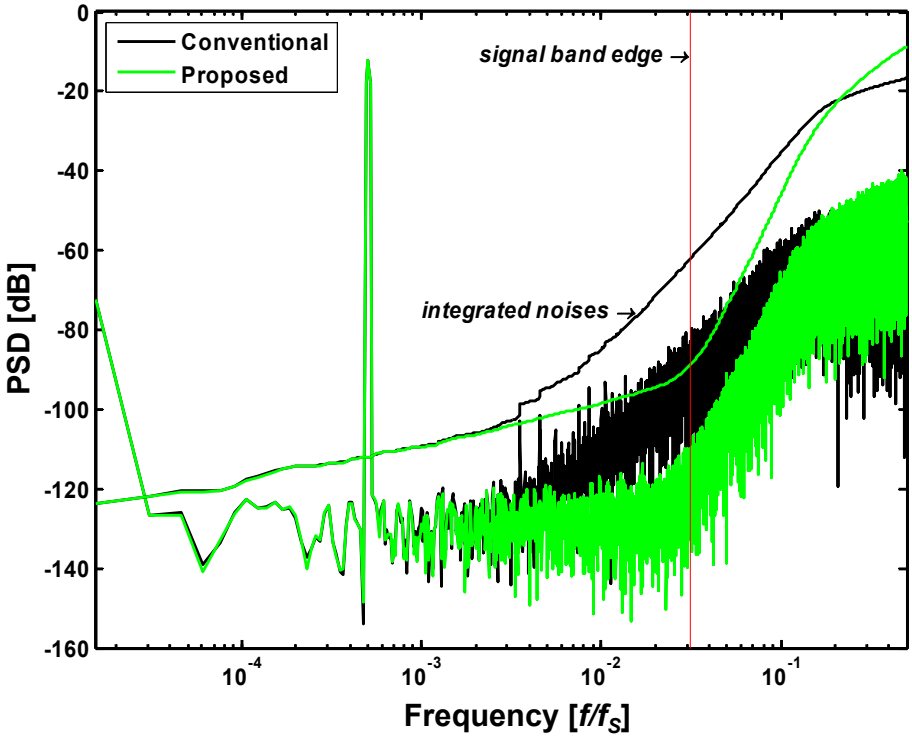


Figure 3.10: PSDs for split ΔΣ ADC without and with 2nd-order noise coupling.

output spectra of a two-cell ADC without and with 1st-order and 2nd-order noise coupling, respectively. Thermal noises and various realistic circuit errors are assumed for each split 2nd-order modulator with 9-level quantizer and DAC. The SNDR improved by 15.2 dB for 1st-order noise-coupled modulator with OSR 32, and by 26.8 dB for 2nd-order noise-coupled modulator with OSR 16.

3.2.4. Self noise coupling [7][8]

Somewhat surprisingly, noise coupling can also be used in a single stage, as illustrated in Fig. 3.11. This is because the coupling branch includes at least one clock period delay, and under busy signal conditions the correlation between the quantization noise *q(k)* and its delayed replica *q(k-1)* becomes low after a brief (typically about 100 period) warm-up interval. This is illustrated in Fig. 3.12 which shows the decline of the autocorrelation function given by

$$corr\,(1,1)\big|_{t=nT} = \frac{1}{n}\sum_{k=1}^{n} q_1(k)\cdot q_1(k-1) \tag{3.3}$$

in the presence of thermal noises and practical circuit errors. Fig. 3.13 compares the output spectra for second-order ΔΣ ADC without and with the self-coupling branches under the same simulation conditions as in Fig. 3.9. The SNDR was improved by 15.3 dB due to the noise coupling.

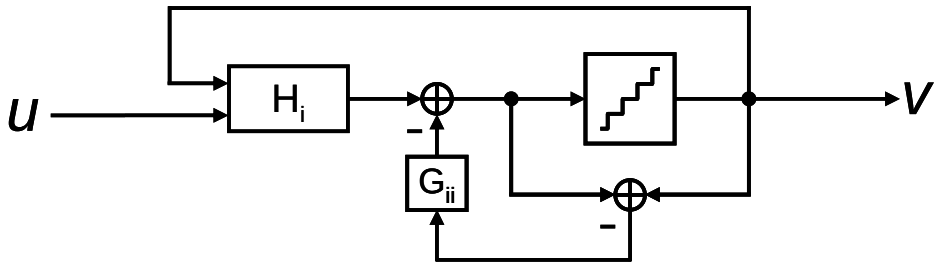


Figure 3.11: Noise coupling in a single delta-sigma ADC.

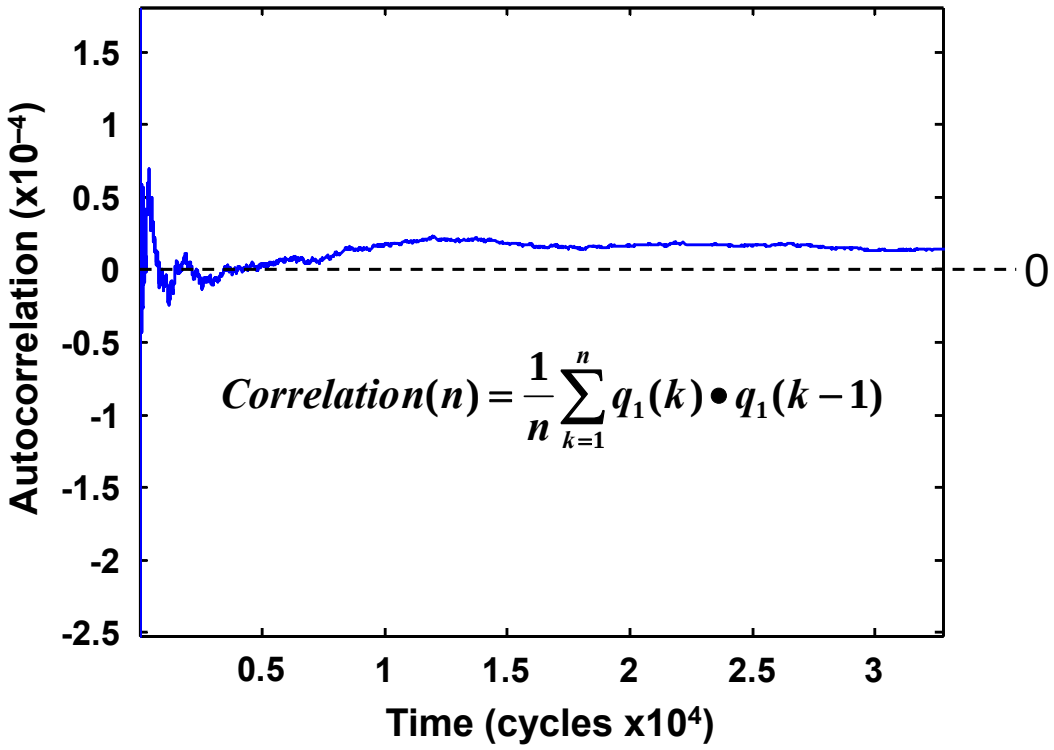


Figure 3.12: Autocorrelation of quantization noises for a single delta-sigma ADC.

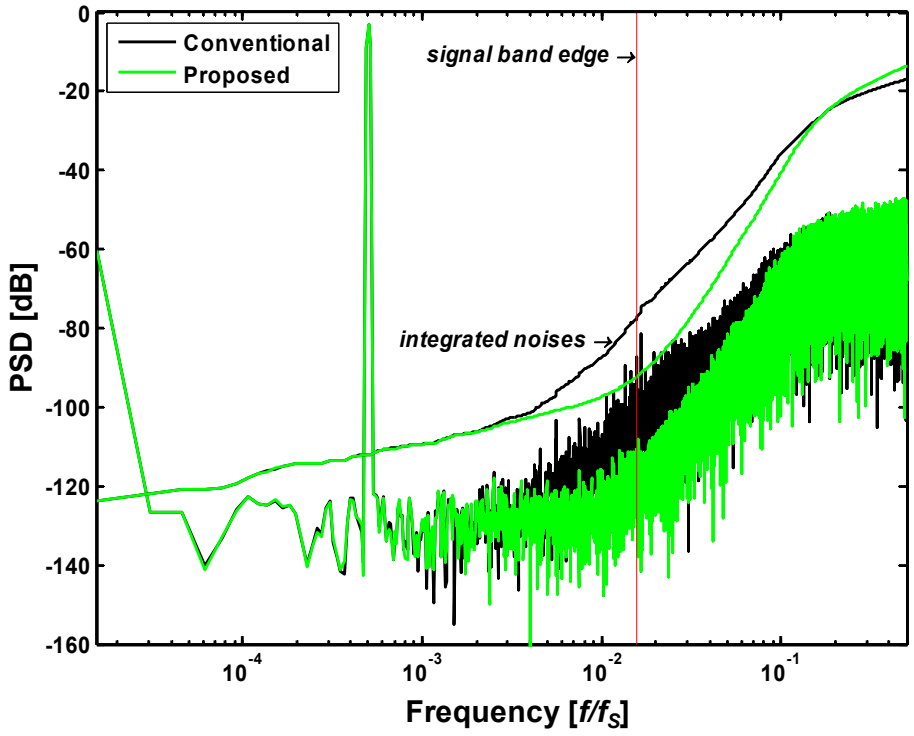


Figure 3.13: PSDs for a single ΔΣ ADC without and with self noise coupling.

3.3. **RING-COUPLED 4-CELL ΔΣ ADC** (abbreviated by RC4)

3.3.1. Architecture

The linearity of the modulator can be decoupled from that of the loop filter by selecting a low-distortion topology, where a direct feedforward path from the input to the quantizer allows the loop filter to process only shaped quantization noise. This significantly reduces the signal swing and nonlinear signal distortion [9]. However, the linearity of the modulator may still be limited by harmonic spurs and idle tones generated in the loop. Hence, an external dither is often injected into the loop to prevent periodic tones. This, however, requires additional hardware for dither generation, and also reduces the DR of the modulator. In this section, a novel technique is introduced, whereby the quantization noise of another modulator is used as a dither. The injected noise also enhances the noise shaping of the overall converter.

The proposed modulator architecture is shown in Fig. 3.14 [5][6]. A single modulator is divided into multiple cells, with minimal additional power and area requirement [3][4]. Every splitting into two halves results in a 6 dB increase in the signal and thermal noise powers at the output. The quantization noise power, however, increases by only 3 dB if the output word length is kept unchanged, and by 9 dB if it is reduced by one bit for each sub-modulator. A 6 dB increase for the quantization noise power can be obtained then by reducing the LSB level by $1/\sqrt{2}$. Thus, the SNR, power dissipation, and chip area can all be maintained at the same value for the multi-cell ADC. The ring-coupling of quantization noises in the split modulator will then break up idle tones as well as harmonic spurs, and increase the SNR by raising the order of the noise shaping. The SNR improvement obtained by

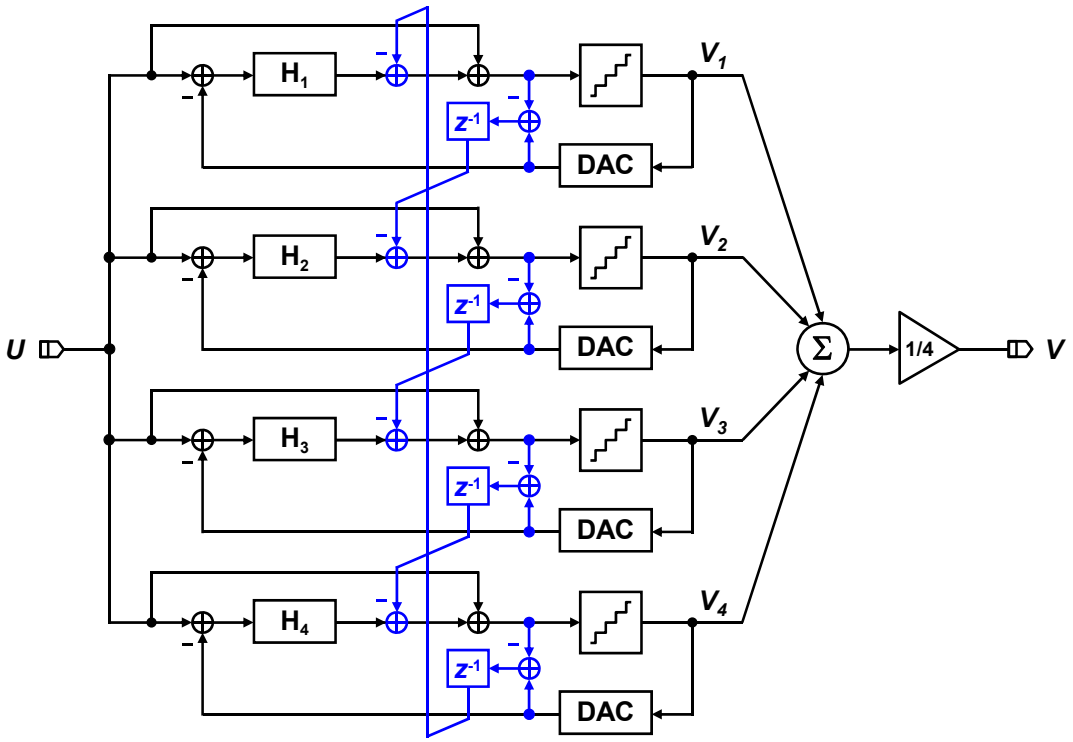


Figure 3.14: Block diagram of ring-coupled 4-cell ΔΣ ADC (RC4).

the noise coupling depends on the order, oversampling ratio (OSR), and resolution of the modulator.

3.3.2. Circuit design

The proposed ring-coupled modulator was implemented with switched-capacitor (SC) circuitry, as shown in Fig. 3.15. Separate input and DAC capacitors were used to eliminate any signal dependence of the reference driver. The feedback factor and total capacitance of the 1st integrator opamp is retained by halving each capacitor and by increasing the signal swing through cross-coupled switches between both rails. A cascode single-stage opamp with an SC common-mode feedback is used in both integrators and also in the active summer. The slew rate requirement for the opamp is

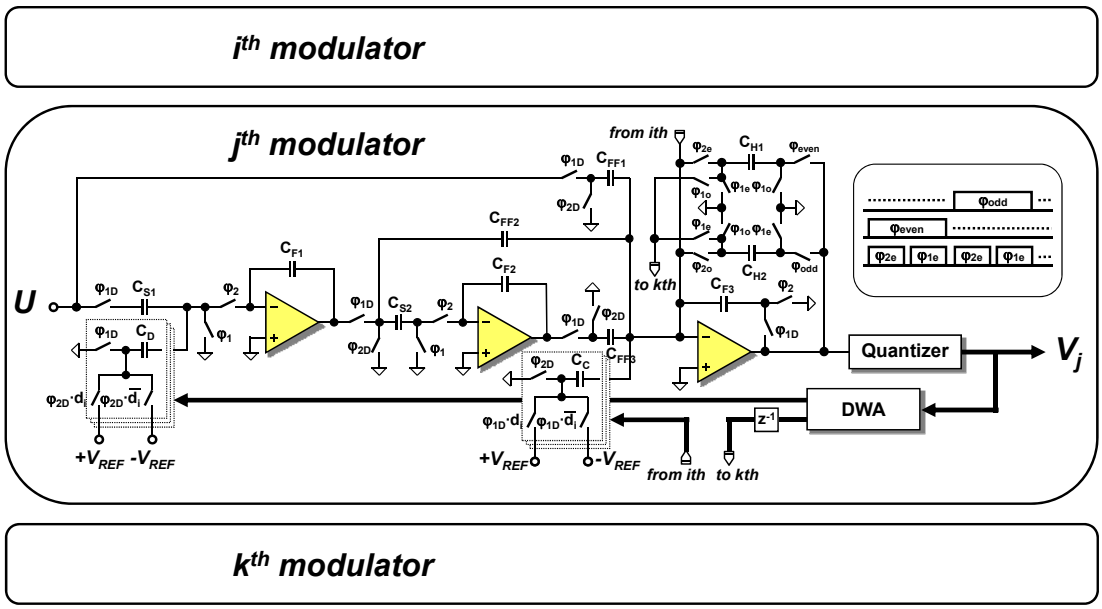


Figure 3.15: SC circuit implementation of the prototype ADC (RC4).

greatly relaxed due to the low-distortion topology and to 15-level quantization. Highly linear sampling is obtained by using bootstrapped input switches. These were designed to stay within the allowed maximum gate stress voltage [10]. The active summation and noise coupling are realized using an offset-compensated opamp. A two-stage preamplifier with an input offset sampling followed by a track-and-latch and an SR latch form the quantizer. The reference voltages are supplied by a resistor string. The mismatch errors of the 15-level DAC are shaped with data weighted averaging (DWA). The timing of the quantizer and the 4-stage logarithmic shifter for DWA do not limit the modulator performance, thanks to the optimized sizing the transistors in the critical path. The effect of switching noise, coupled from the digital blocks, was reduced by using the triple wells available in the process used.

3.3.3. Experimental result

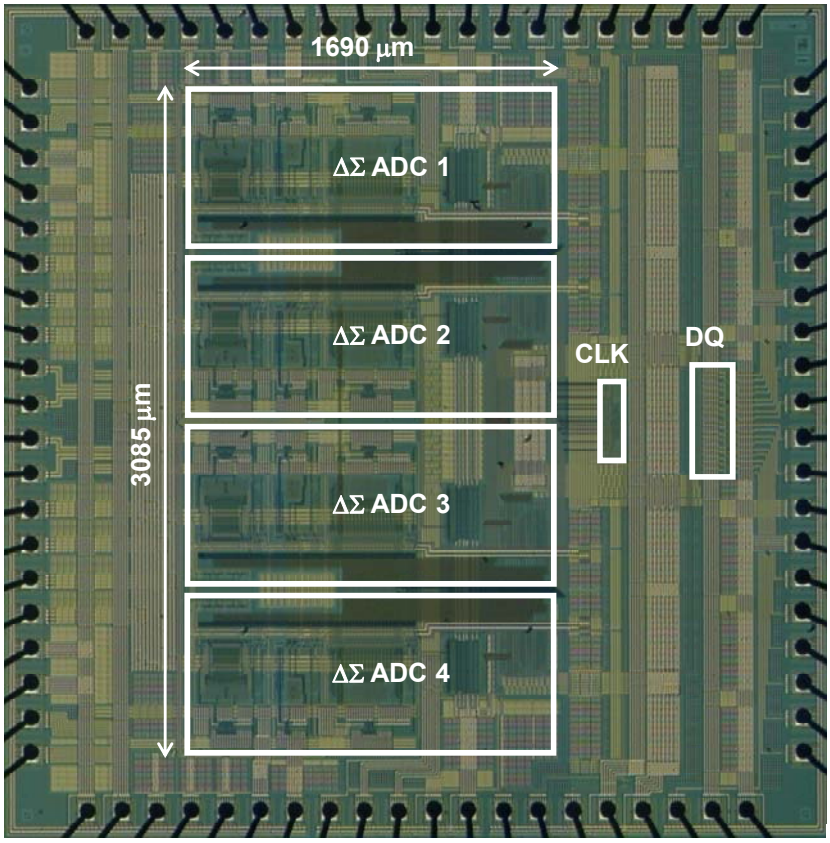


Figure 3.16: Chip micrograph for the prototype ADC (RC4).

A proof-of-concept prototype was fabricated in a 0.18μm 2P4M CMOS process. The die micrograph is illustrated in Fig. 3.16. With a single-tone input swept from 10 kHz to 1 MHz, and sampled at a 60 MHz rate, it provides 86 dB peak SNR and SNDR, 88 dB DR, and -102.4 dB THD. The excellent linearity is verified in Fig. 3.17, and 3.18 for a -0.92 dBFS, 21.06 kHz input. Fig. 3.17 shows the measured spectrum for a single path with dithering (SNDR = 65 dB), and Fig. 3.18 for the 4-path ADC (SNDR = 86 dB). A two-tone test gave a -94.4 dB IMD (Fig. 3.19). The SNR and SNDR variations with signal power are shown in Fig. 3.20. The SNR, SNDR, and DR performances with input signal frequencies are illustrated in Fig. 3.21. The measured power dissipation is P = 33.7 mW (analog: 18.8 mW, digital: 14.9 mW), and the figure-of-merit defined as $P/(2 \cdot BW \cdot 2^{ENOB})$ is 0.546 pJ/conversion

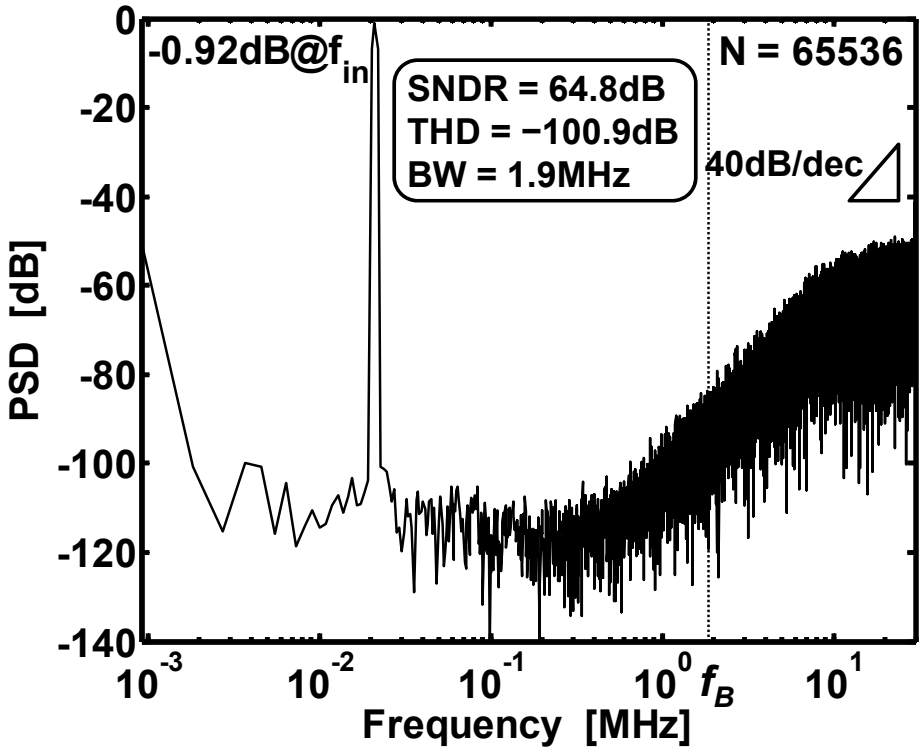


Figure 3.17: Measured spectrum for the prototype ADC (a single cell only in RC4).

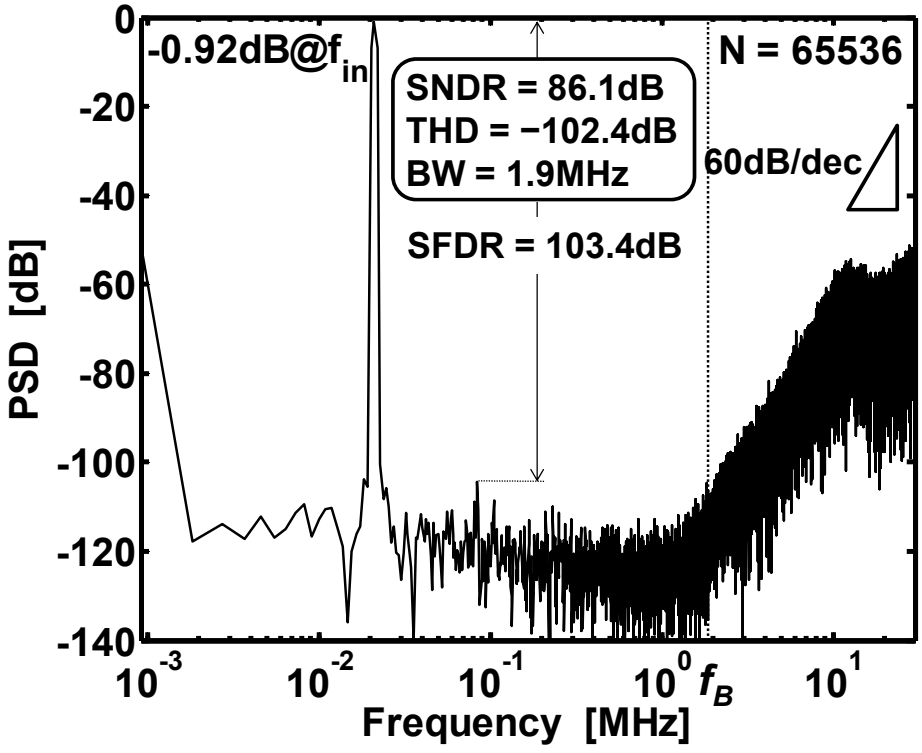


Figure 3.18: Measured spectrum for the prototype ADC (RC4).

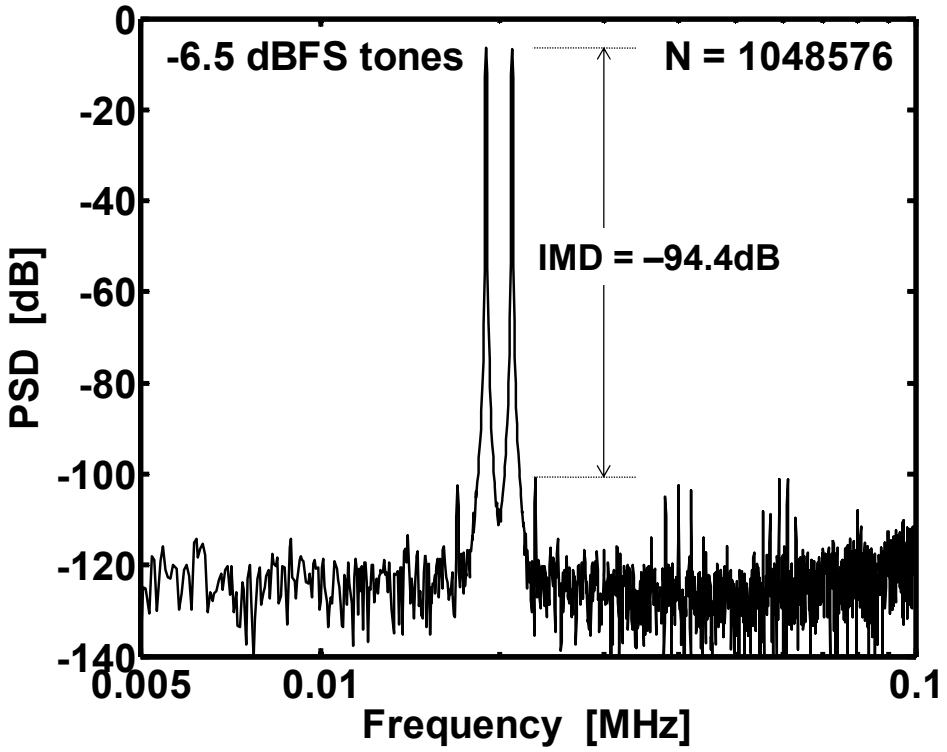


Figure 3.19: Measured two-tone spectrum for the prototype ADC (RC4).

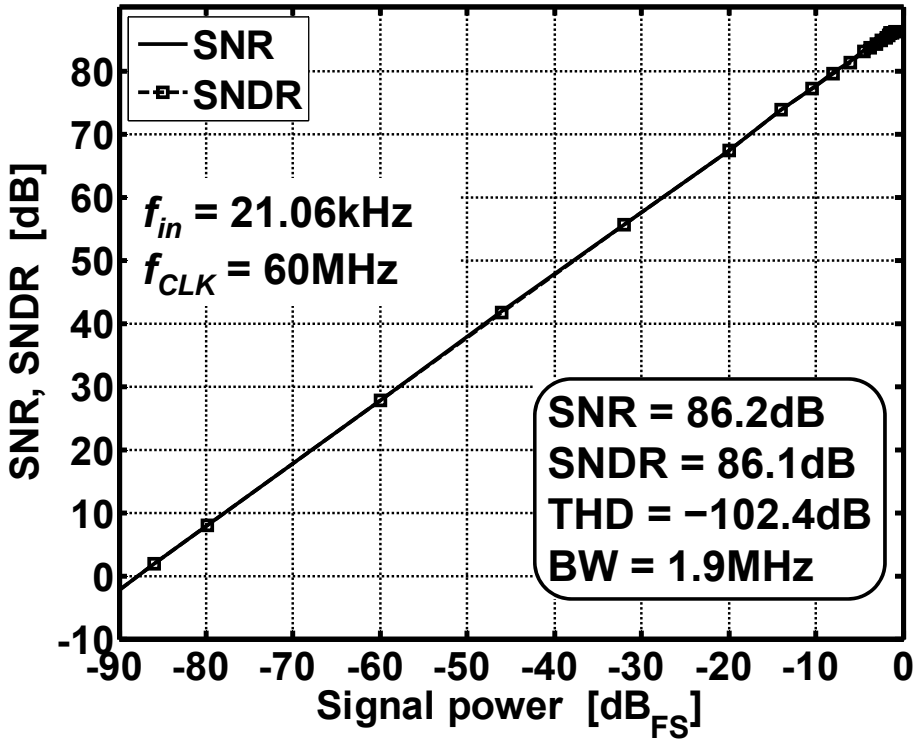


Figure 3.20: Measured SNR and SNDR with input signal power for the RC4.

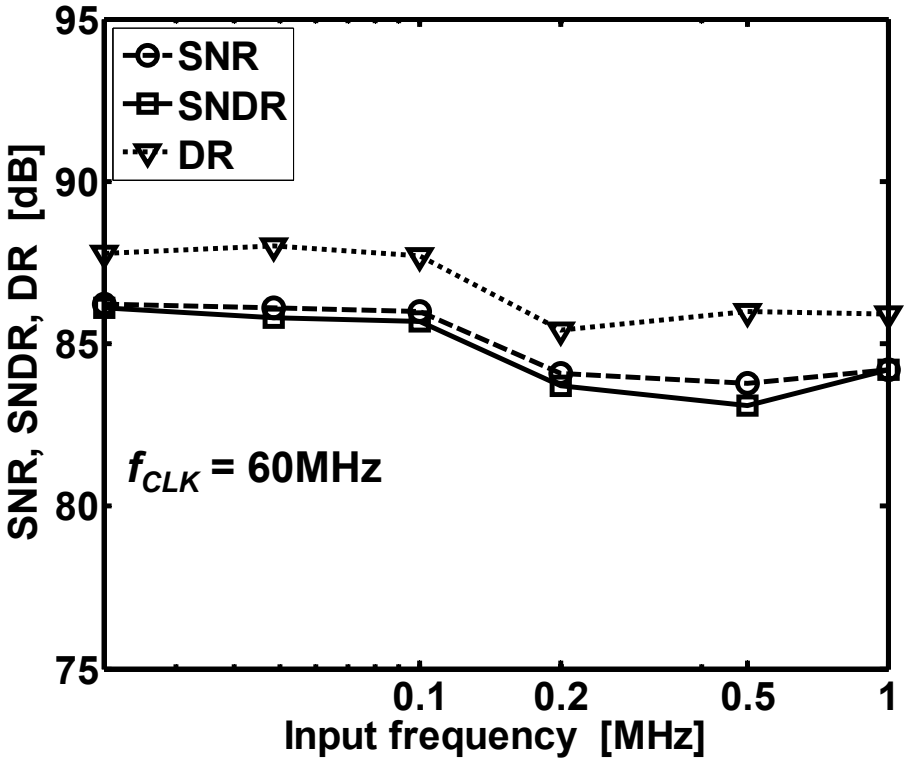


Figure 3.21: Measured SNR, SNDR, and DR with input frequencies for the RC4.

TABLE 3.1: PERFORMANCE SUMMARY FOR THE RC4.

Clock frequency	**60 MHz**
Signal bandwidth	**1.9 MHz**
OSR	**16**
Input range (diff.)	**1.44 V_{pp}**
C_{IN} and C_{DAC}	**separate**
Dynamic range	**88.0 dB**
SNR	**86.2 dB**
SNDR	**86.1 dB**
THD	**−102.4 dB**
FOM	**0.546 pJ/conv.**
Power consumption	**18.8 mW (A), 14.9 mW (D)**
Power supply	**1.5 V (A), 1.4 V (D)**
Process	**0.18μm 2P4M CMOS**
Core area	**5.24 mm^2**

-step. The measured performance is summarized in Table 3.1.

3.3.4. Summary

A highly linear ring-coupled ΔΣ ADC (RC4) was described. A single 2^{nd}-order modulator is split into four identical sub-modulators, and their quantization noises are coupled in a ring topology. The coupled noises raise the effective order of the overall modulator from two to three, and also remove harmonic spurs and idle tones. The prototype achieved a 86 dB signal-to-noise-and distortion ratio (SNDR), 88 dB dynamic range (DR) and -102.4 dB THD in a 1.9 MHz signal band, using a 1.5 V power supply.

3.4. SELF-COUPLED 4-CELL ΔΣ ADC (abbreviated by SC4)

3.4.1. Architecture

Some applications demand robust and flexible data conversion. There are versatile applications where robustness and programmability are vital characteristics, and total failure of the device is not allowed. Space and satellite electronics exposed to intense cosmic rays, military devices open to severe environments and bioelectronics related with human life such as defibrillators are just a few examples. A multi-cell realization provides an efficient solution to this with minimal overhead [3][4]. A single bulky ADC is splintered into a lot of small ADCs. The acceptable maximum number of split cells depends on the specification of an original ADC and the limitation on the components matching. The splitting process does not entail any drawback until reaching this limit.

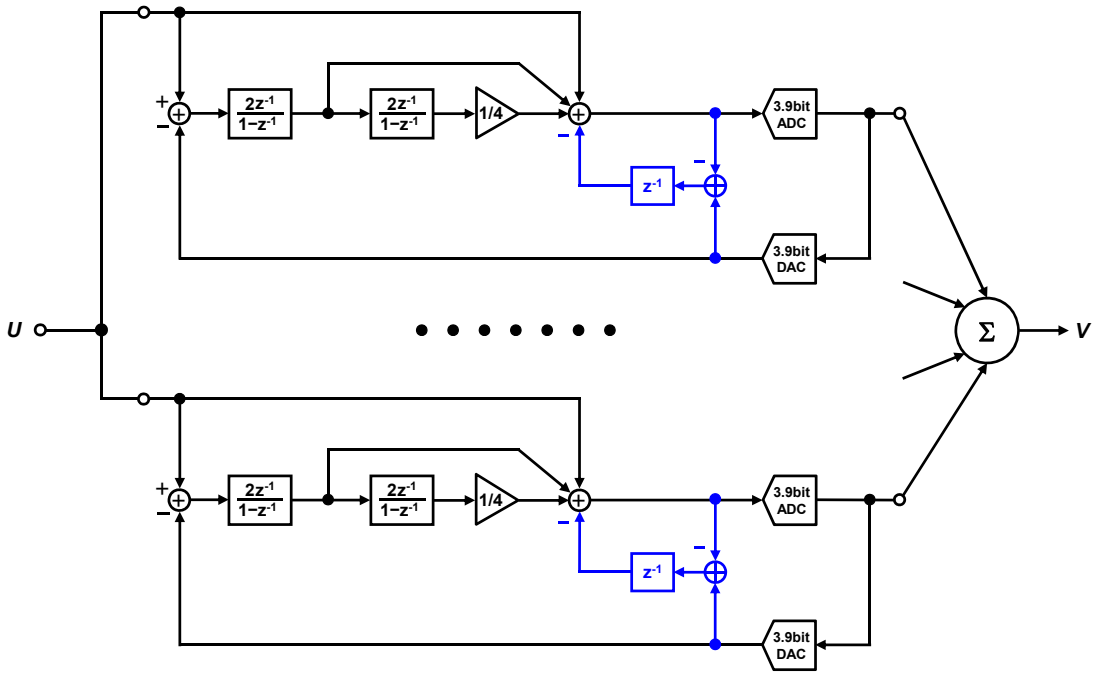


Figure 3.22: Block diagram of self-coupled 4-cell ΔΣ ADC (SC4).

The cellular approach is applied to a low-distortion 2nd-order ΔΣ ADC to obtain robustness and flexibility of data conversion. From the robustness perspective, device failure in a multi-cell ADC does not cause an abrupt system malfunction but leads to a graceful gradual performance degradation. From the flexibility viewpoint, it enhances the adaptability and reconfigurability of the ADC to various applications, where the number of activated cells is controlled, and unused cells are powered down to save power. A proof-of-concept chip includes 4 modulator cells, as shown in Fig. 3.22. The basic principle of operation of multi-cell ADCs relies on the statistical independence of thermal and quantization noises among ADC cells. Under ideal conditions, excluding any circuit errors and thermal noise, the complete decorrelation of noises is not met and the multi-cell approach is no longer valid. However, once realized on silicon, the inevitable circuit errors and thermal noise are introduced, and contribute to the decorrelation of overall noises across cells. These

circuit errors should be large enough to decorrelate the quantization noise among cells, but small enough not to raise the noise level too much. From simulations, it is found that typical circuit errors introduced during the fabrication satisfy this condition without injecting intentional systematic offsets during the design. As in stochastic resonance (SR), the performance of multi-cell ADC attains peak value for a certain level of circuit errors. SR is prevalent and observed in a large variety of disciplines such as physics, chemistry, biology, and physiology.

The splitting of a single modulator can be analyzed by considering the signal and noise powers associated with it. Every dividing-by-two results in a 6 dB increase of the signal and thermal noise powers at the output. The quantization noise power increases by 3, 6, or 9 dB depending on the number N of quantization levels for each cell. A 6 dB increase in the overall quantization noise power occurs when reducing N by $1/\sqrt{2}$ for each segmented modulator. Hence, the SNR, power dissipation, and silicon area can be substantially maintained unchanged with this multi-cell approach. Furthermore, quantization noise coupling within each split modulator significantly extends the range of the whole ADC when the order, oversampling ratio (OSR), and resolution of the modulator are changed [7][8].

3.4.2. Circuit design

The proposed multi-cell noise-coupled delta-sigma ADC was implemented with SC circuitry as shown in Fig. 3.23. It employs separate input and DAC capacitors to avoid any signal-dependent loading on the reference driver. The closed-loop BW and total capacitance area for the 1st integrator opamp is nevertheless kept the same, by maximizing the related signal swing via cross-coupled switches between dual rails. The reduced signal swing with a low-distortion architecture [9] allows a telescopic

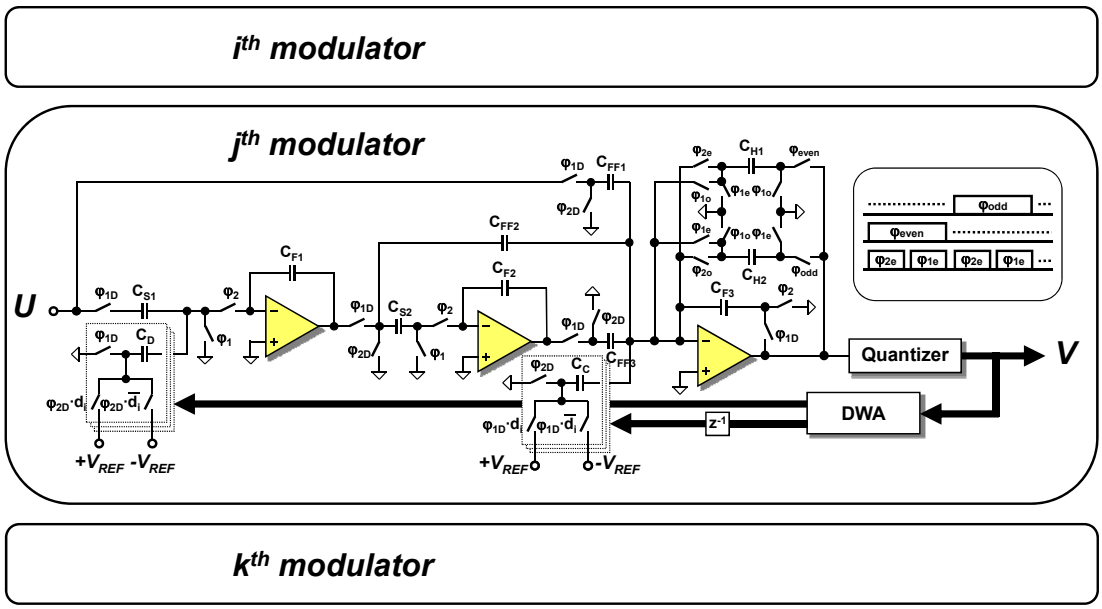


Figure 3.23: SC circuit implementation of the prototype ADC (SC4).

cascode opamp at a 1.5 V power supply for each integration and active summation along with noise coupling. The relatively large signal swing at summing node dominated with a feedforward input signal does not limit the linearity of the modulator since its associated nonlinearity is effectively attenuated by the preceding loop filter. The critical input switches are realized with bootstrapped switches to achieve highly linear sampling. A 15-level quantizer is composed of a two-stage preamplifier with an input offset sampling, a track-and-latch, and an SR latch. Data weighted averaging (DWA) linearizes the 15-level DAC. A critical timing in the quantizer and in the 4-stage logarithmic shifter for DWA is satisfied with optimized design.

3.4.3. Experimental result

Fabricated in a 0.18μm 2P4M CMOS process, the prototype, illustrated in Fig.

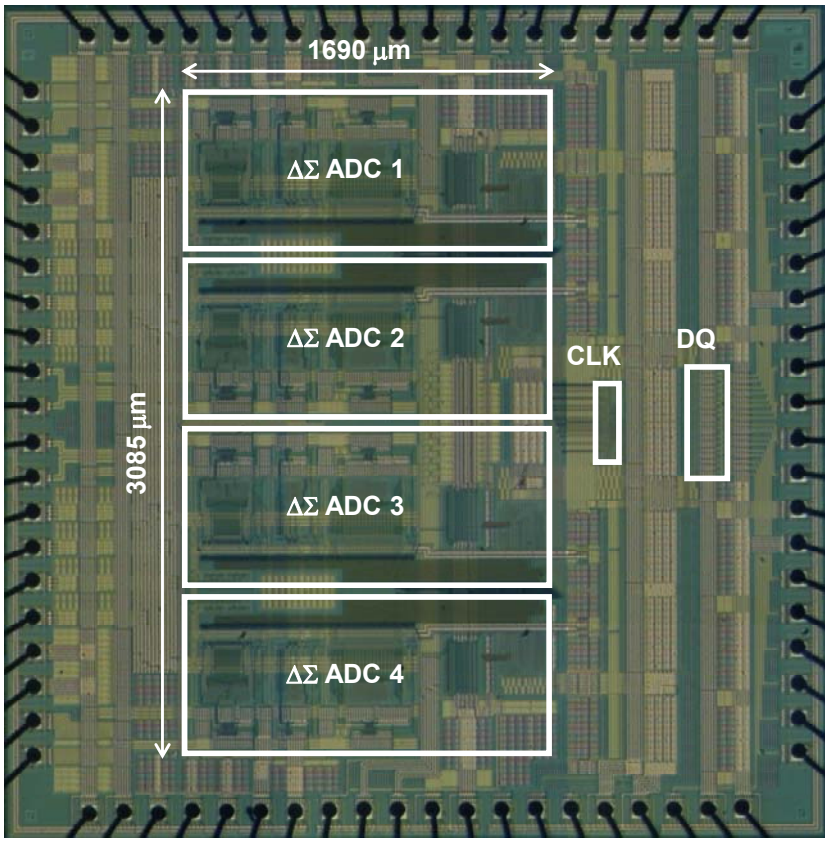


Figure 3.24: Chip micrograph for the prototype ADC (SC4).

3.24 shows over 86 dB peak SNR and SNDR, 88 dB DR, and -98 dB THD in the 1.9 MHz signal band with a 10 kHz to 1 MHz input signal sampled at a 60 MHz clock. The measured spectrum with a -1.13 dBFS 100 kHz input is shown in Fig. 3.25. The SNR and SNDR versus signal power and performance with input signal frequency is shown in Fig. 3.26 and Fig. 3.27, respectively. With 4 modulators activated, the measured power dissipation is 32.3 mW (analog: 17.6 mW, digital: 14.7 mW) and the figure-of-merit (FOM) defined by Power/($2 \cdot BW \cdot 2^{ENOB}$) is 0.52 pJ/conversion-step. The measured performance is summarized in Table 3.2.

3.4.4. Summary

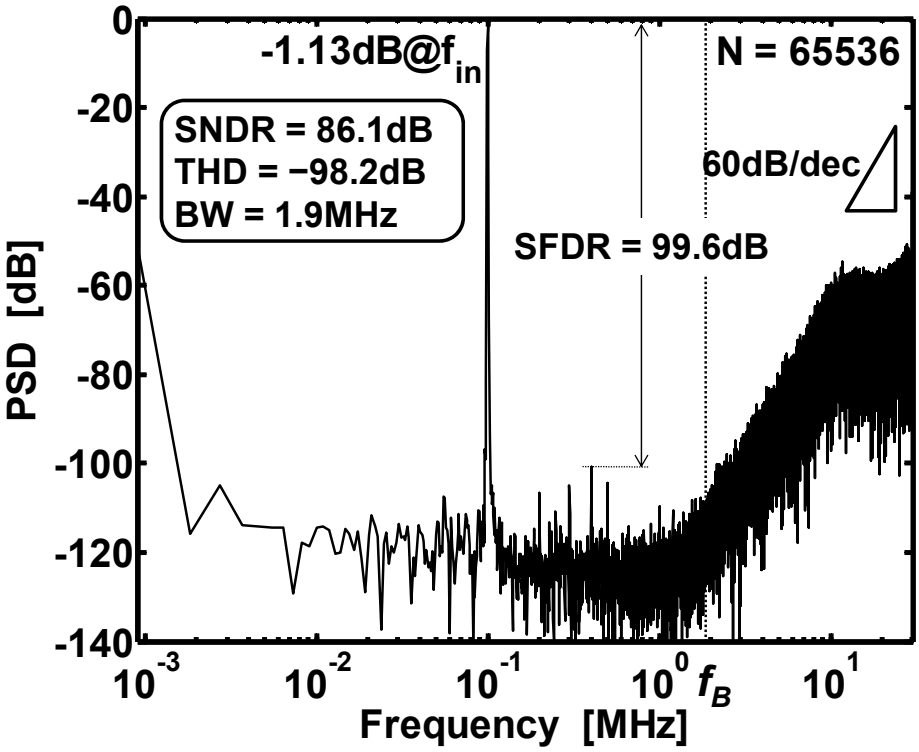


Figure 3.25: Measured spectrum for the prototype ADC (SC4).

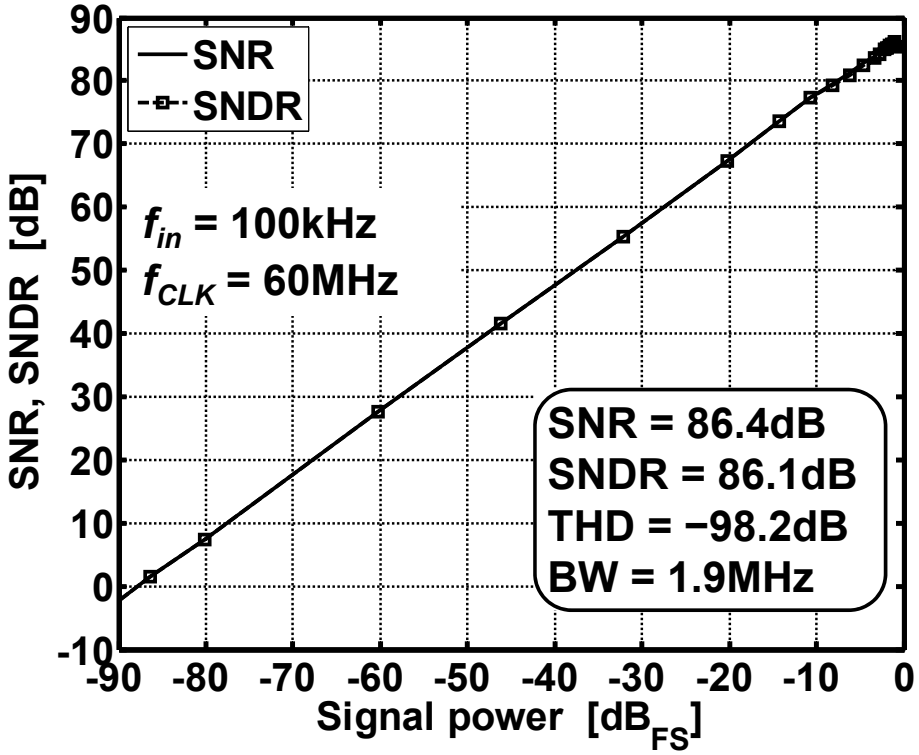


Figure 3.26: Measured SNR and SNDR with input signal power for the SC4.

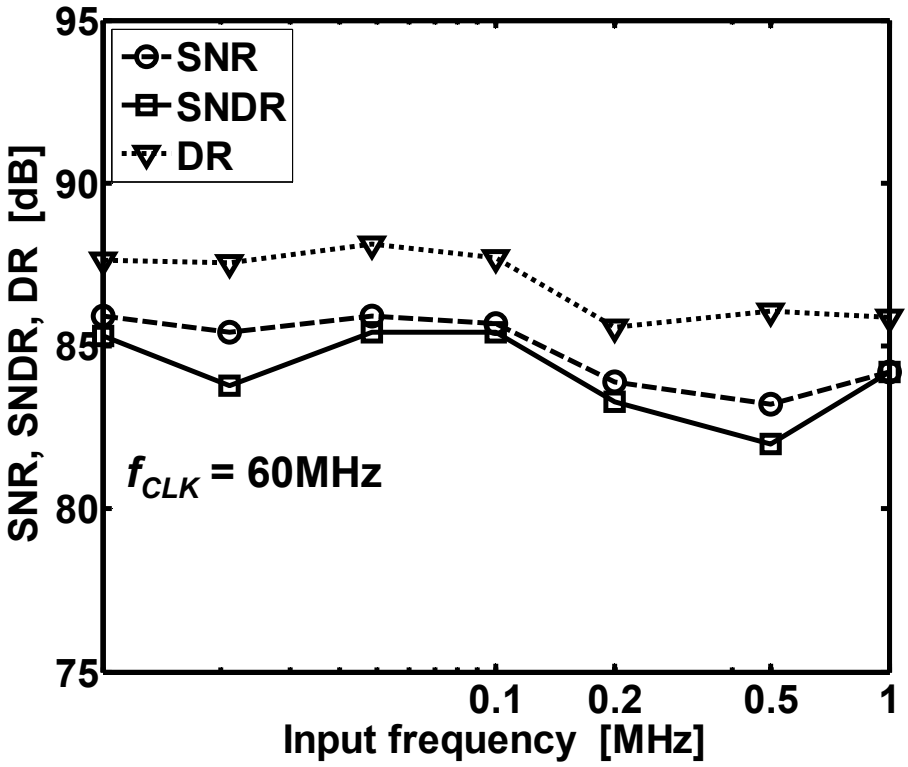


Figure 3.27: Measured SNR, SNDR, and DR with input frequencies for the SC4.

TABLE 3.2: PERFORMANCE SUMMARY FOR THE SC4.

Clock frequency	**60 MHz**
Signal bandwidth	**1.9 MHz**
OSR	**16**
Input range (diff.)	**1.44 V_{pp}**
C_{IN} and C_{DAC}	**separate**
Dynamic range	**87.8 dB**
SNR	**86.4 dB**
SNDR	**86.1 dB**
THD	**−98.2 dB**
FOM	**0.52 pJ/conv**
Power consumption	**17.6 mW (A), 14.7 mW (D)**
Power supply	**1.5 V (A), 1.45 V (D)**
Process	**0.18μm 2P4M CMOS**
Core area	**5.24 mm^2**

A robust and reconfigurable multi-cell noise-coupled ΔΣ ADC was presented. Instead of a single full-size 2^{nd}-order modulator, an array of 4 tiny modulators are realized to enable efficient trade-off between resolution and power dissipation according to a specific application and to increase robustness in a harsh operating condition. The trade-off and flexibility are further enhanced using quantization-noise coupling in each modulator cell. The prototype achieved 86 dB SNDR, 88 dB DR, and -98 dB THD in the 1.9 MHz signal band using a 1.5 V power supply.

3.5. SELF-COUPLED SINGLE-CELL ΔΣ ADC (abbreviated by SC1)

3.5.1. Architecture

With increasing demand for wide-band low-power data converters in many wired and wireless applications, both the proper selection of ADC topology and the efficient circuit realization to meet stringent specifications are becoming important. Discrete-time delta-sigma ADCs can provide more than 80 dB SNDR for MHz-range signals with low power consumption. For given bandwidths, dynamic range and resolution, the power dissipation should be minimized through the choice of power-efficient modulator architecture and circuit implementation. A low-distortion delta-sigma ADC topology greatly relaxes the linearity requirements for its loop filter by reducing the internal signal swing considerably [9]. This is achieved by providing a direct feedforward path from the input to the quantizer. This makes the signal transfer function (STF) equal to 1, so that the loop filter processes the quantization noise only. The summation of signals at the quantizer input may be performed by either a passive adder or an active one. Passive summing can be done with a capacitive adder, which does not require an extra opamp. However, the attenuation

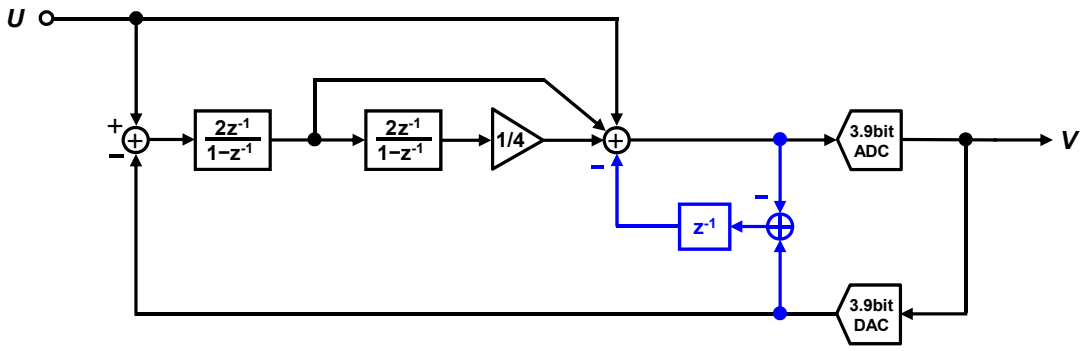


Figure 3.28: Block diagram of self-coupled single-cell ΔΣ ADC (SC1).

of the signal due to parasitics results in increased power dissipation and mismatch effects at the quantizer. On the other hand, active summation requires an extra opamp. Neither of the two approaches is thus power-efficient.

In this Section, a low-distortion ADC is described, which uses noise coupling [7][8] to boost the noise shaping performance from second to third order without requiring an extra amplifier. It demonstrates a power-efficient design approach to wide-band ADC design.

The proposed modulator architecture is shown in Fig. 3.28. Noise coupling is achieved by delaying the quantization noise by one clock cycle, and injecting it into the summing node before the quantizer. The injected quantization noise effectively raises the modulator order from two to three, without changing its signal transfer function [7][8]. Thus, the low-distortion property is preserved, and the modulator performance and power efficiency are improved. The sampling frequency and OSR can be reduced for the same bandwidth (BW) and SNDR performance, or either the BW or the SNDR performance can be increased for the same sampling frequency, by applying this technique. The use of an extra opamp is now justified, since it provides the virtual ground for both active addition and noise coupling. Compared with conventional third-order low-distortion delta-sigma ADCs, the proposed topology

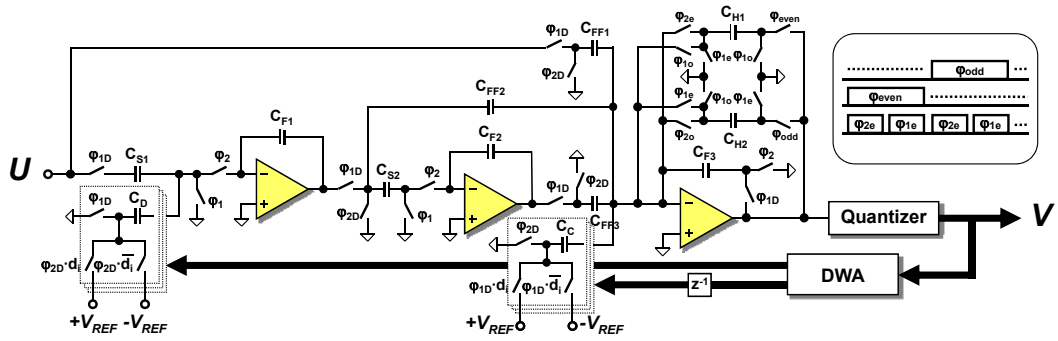


Figure 3.29: SC circuit implementation of the prototype ADC (SC1).

provides similar noise shaping, but with increased stability as well as reduced tone generation and THD, while using a reduced number of amplifiers. (A different way of removing the extra adder at the quantizer input for a low-distortion modulator was introduced in [11].) The use of a multi-bit quantizer and DAC reduces the signal swings at the internal nodes of the loop filter further, and improves the modulator stability. The quantization noise of the modulator also becomes more random due to multi-bit quantization and noise coupling. The additional advantage for this modulator architecture is that the injected quantization noise works as a dither signal, and thus idle tones and harmonic spurs are reduced, and the modulator linearity is improved.

3.5.2. Circuit design

Fig. 3.29 illustrates the simplified SC circuit diagram of the modulator. The input sampling and DAC capacitors are separated to avoid any reference errors due to signal-dependent loading. Even with the separate input sampling and DAC capacitor scheme, the feedback factor and capacitive load of the first opamp are preserved by halving the input capacitances, and by doubling the signal swing through the use of cross-coupled switches between positive and negative rails. A power-efficient

telescopic cascode opamp with a SC common-mode feedback circuit is used in the integrators and the active adder. The slew rate requirement for the opamp is greatly relaxed by using the low-distortion modulator topology and multi-bit quantization. Bootstrapped switches are applied for linear sampling at the critical input switches. An offset-compensated opamp is used for the active adder. Each comparator contains a two-stage preamplifier followed by a track-and-latch and an SR latch. The threshold voltages of the quantizer are generated by a resistor string. Data weighted averaging (DWA) is applied to shape the mismatch errors from the 15-level DAC. The transistors in the quantizer and in the 4-stage logarithmic shifter of the DWA circuit are sized appropriately to meet the critical timing specifications. The essential timing parameters, such as clock nonoverlap time, are digitally programmable via a 3-wire serial interface to get optimum performance reliably under variations of process, voltage, and temperature.

3.5.3. Experimental result

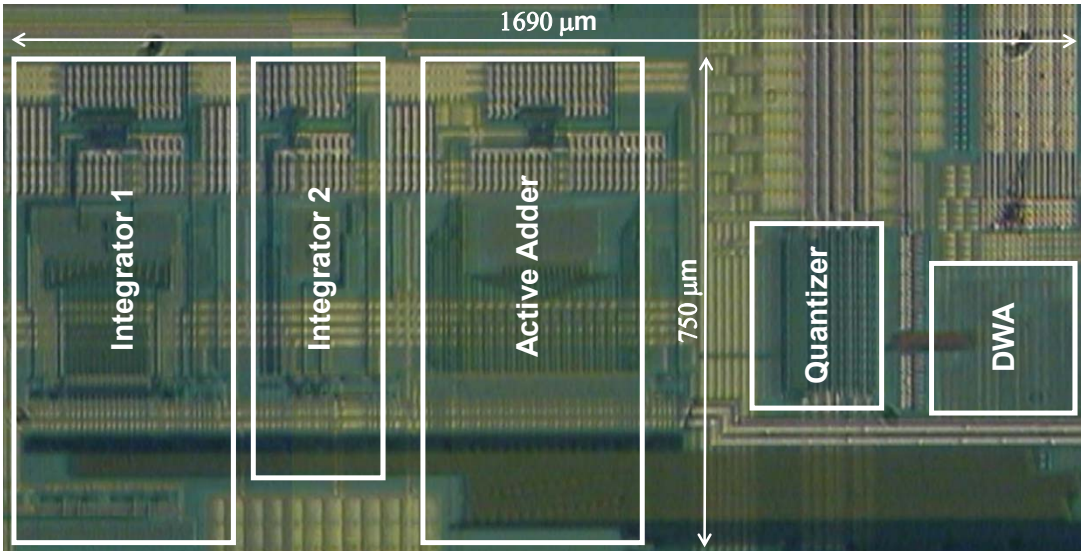


Figure 3.30: Chip micrograph for the prototype ADC (SC1).

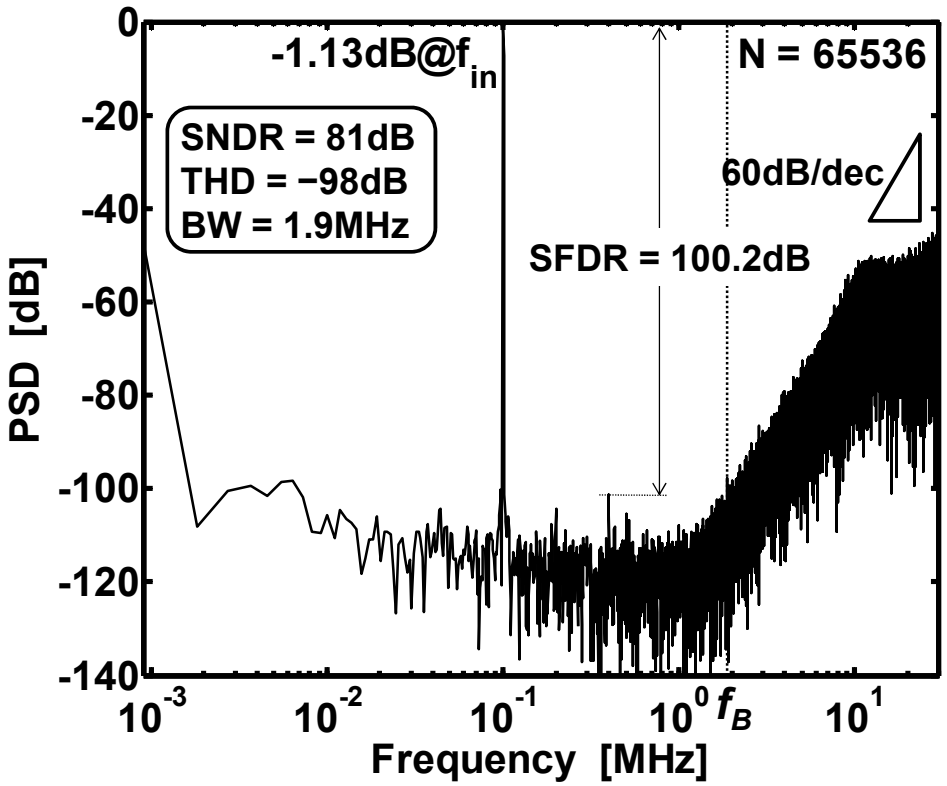


Figure 3.31: Measured spectrum for the prototype ADC (SC1).

A prototype device was fabricated in a 0.18μm 2P4M CMOS process. The die micrograph is shown in Fig. 3.30. It uses a 1.5 V power supply for the analog circuitry and a 1.45 V one for the digital stages. The modulator was tested with a single-tone input from 10 kHz to 1 MHz. It shows uniform performance in this range with a 60 MHz sampling clock. The measured spectrum at peak SNDR is illustrated in Fig. 3.31 for a -1.13 dBFS 100 kHz input signal. It shows a SFDR around 100.2 dB. The SNR and SNDR variations with input signal level are shown in Fig. 3.32. They illustrate linearly increasing SNDR for signal powers from -85 dBFS up to -1 dBFS, indicating highly linear modulator operation. The prototype achieves 81 dB peak SNR and SNDR, 82 dB DR, and -98 dB THD. The measured power dissipation is P = 8.1 mW (analog: 4.4 mW, digital: 3.7 mW) and the figure-of-merit, defined by $P/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$, is 0.25 pJ/conversion-step, which is among the lowest one

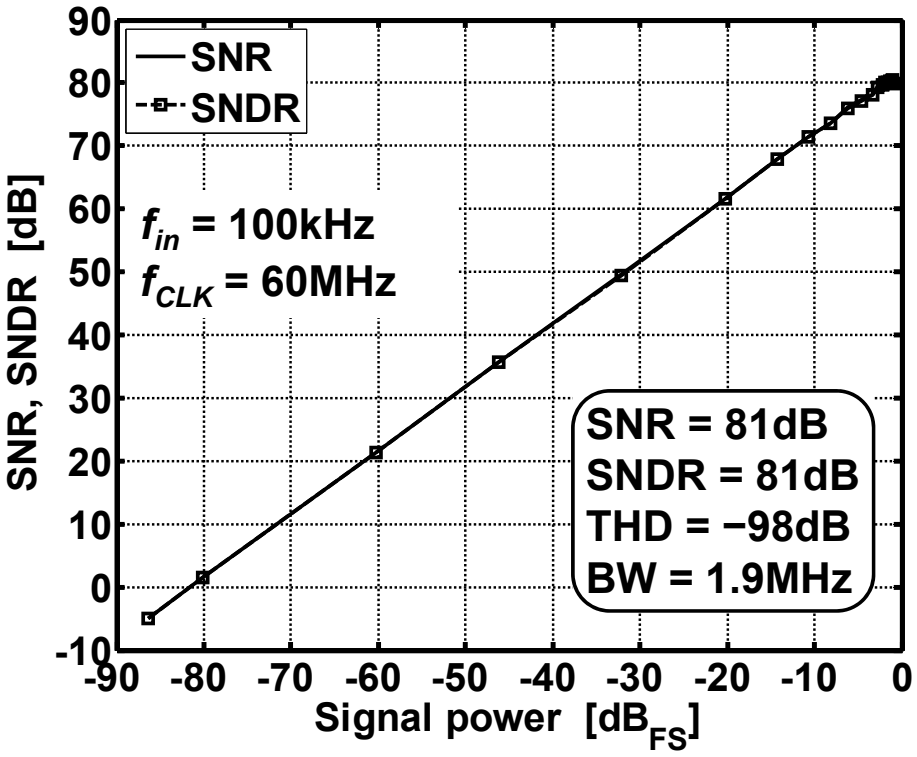


Figure 3.32: Measured SNR and SNDR with input signal power for the SC1.

TABLE 3.3: PERFORMANCE SUMMARY FOR THE SC1.

Clock frequency	**60 MHz**
Signal bandwidth	**1.9 MHz**
OSR	**16**
Input range (diff.)	**1.44 V_{pp}**
C_{IN} and C_{DAC}	**separate**
Dynamic range	**82 dB**
SNR	**81 dB**
SNDR	**81 dB**
THD	**−98 dB**
FOM	**0.25 pJ/conv**
Power consumption	**4.4 mW (A), 3.7 mW (D)**
Power supply	**1.5 V (A), 1.45 V (D)**
Process	**0.18μm 2P4M CMOS**
Core area	**1.27 mm^2**

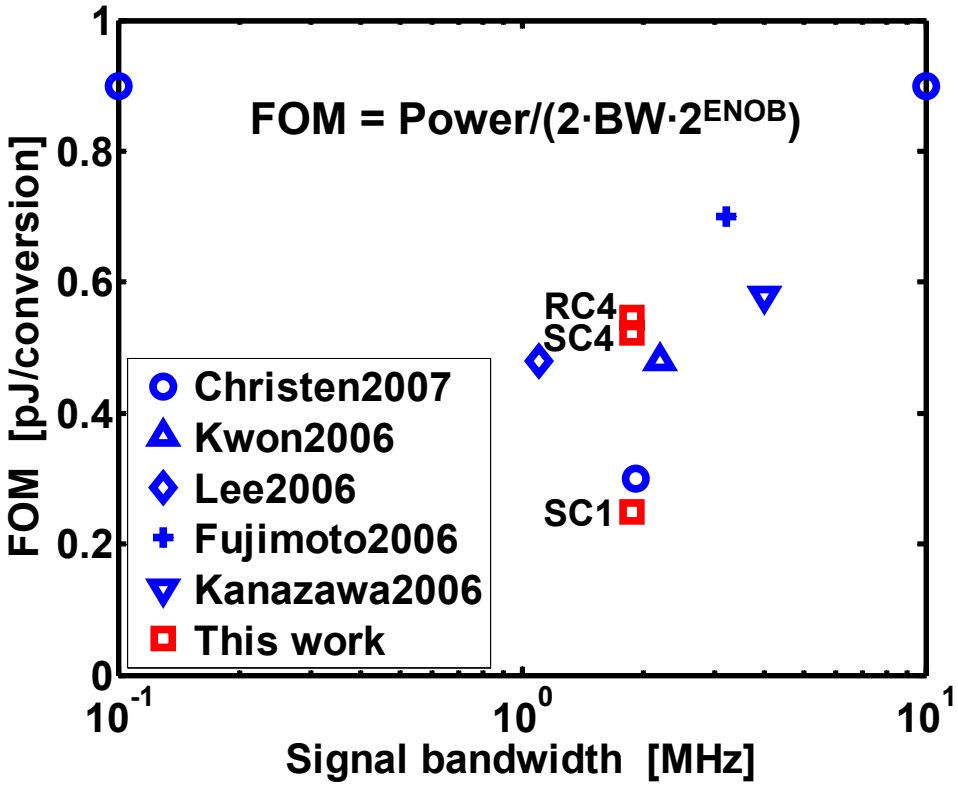


Figure 3.33: Comparison with other DT modulators published recently.

published for a wideband discrete-time delta-sigma ADC. The measured performance is summarized in Table 3.3.

3.5.4. Summary and performance comparison

A switched-capacitor low-distortion 15-level delta-sigma modulator was described. It achieves a third-order noise shaping performance with only two integrators by using quantization noise coupling. It provides 81 dB SNDR, 82 dB DR, and -98 dB THD in a signal bandwidth of 1.9 MHz. It dissipates 8.1 mW with a 1.5 V power supply (analog power 4.4 mW, digital power 3.7 mW).

The measured performances for 3 prototype delta-sigma ADCs described in this chapter are compared with those of other state-of-the-art discrete-time delta-sigma

ADCs published recently on major journals and conferences, as illustrated in Fig. 3.33.

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CHAPTER 4. A NOISE-COUPLED TIME-INTERLEAVED DELTA-SIGMA ADC WITH 4.2 MHZ BANDWIDTH, -98 DB THD, AND 79 DB SNDR

Abstract

This chapter describes a wideband high-linearity ΔΣ ADC. It uses noise coupling combined with time interleaving. Two versions of a two-channel time-interleaved noise-coupled ΔΣ ADC were realized in a 0.18μm CMOS technology. Noise coupling between the channels increased the effective order of the noise-shaping loops, provided dithering, and prevented tone generation in all loops. Time interleaving enhanced the effects of noise coupling. Using a 1.5 V supply, the device achieved excellent linearity (SFDR > 100 dB, THD = -98 dB) and an SNDR of 79 dB in a 4.2 MHz signal band.

4.1. INTRODUCTION

As wireless applications and digital broadcasting proliferate, there is increasing demand for wideband data converters. Their bandwidth requirements range up to several megahertz, and keep increasing. The signal bandwidth requirement gets more stringent in direct conversion receivers. Along with the wide signal bandwidth, high dynamic range (DR) and linearity are also required in these applications. This performance should be achieved in a power-efficient way, since power dissipation determines the battery life for mobile devices. Delta-sigma ADCs can deliver high performance with low power consumption over signal bandwidths in the MHz range, and it is hence the ADC architecture of choice in many wired and wireless receivers.

There are two possible realizations of a delta-sigma modulator. Discrete-time (DT) realization, based on switched capacitor (SC) circuitry, is the traditional one, and continuous-time (CT) realization is getting popular for wideband modulators. Compared with CT modulators, a DT modulator offers robust operation under process variation, and is less sensitive to clock jitter. Its accuracy relies on precise capacitor matching, which is relatively easy to achieve. Also, it is easy to design and test. The disadvantages of DT modulator are higher power dissipation, and a need for an antialiasing filter. On the other hand, CT modulators usually do not require any antialiasing filtering, since it this inherent in the continuous-time loop filter.

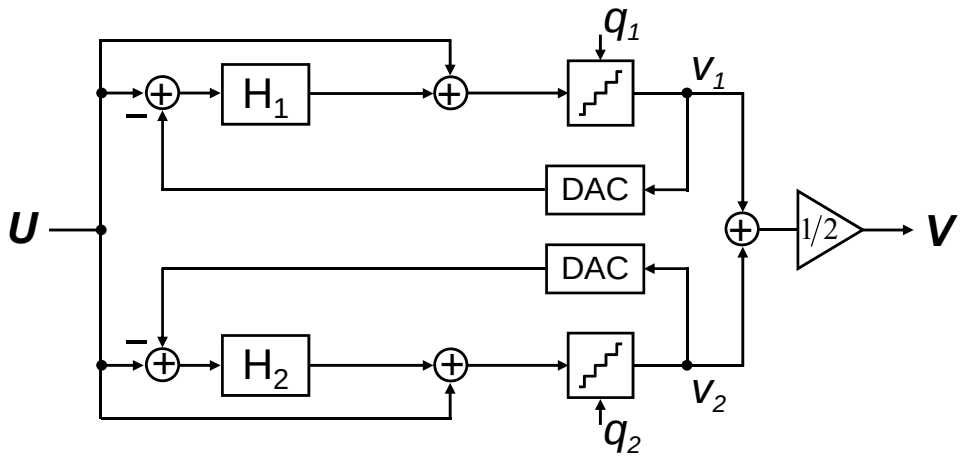
There has been widespread effort recently to design power-efficient wideband delta-sigma modulators. Several DT ΔΣ ADCs have been reported with signal bandwidths in the MHz range, and figures-of-merit (FOMs) below 0.5 pJ/conversion step [1][2][3]. In the design of the device discussed in this chapter, DT realization was chosen for improved performance. The power dissipation of the modulator has been significantly reduced using architectural methods. Basically, a delta-sigma ADC provides high resolution and linearity while using only a low-resolution quantizer by taking advantage of oversampling and noise shaping. There are three key design parameters: (1) quantizer resolution; (2) loop filter order; (3) oversampling ratio (OSR). Increasing any of these improves the resolution under ideal conditions. However, there are limitations associated with each design parameter. In a wideband modulator, the OSR cannot be too high, since then the amplifiers require too much power dissipation. To meet demanding design targets with low OSR, high quantizer resolution and loop filter order are required. These in turn demand increased power dissipation. Hence, in the design of the modulator discussed in this chapter, we relied on architectural innovations to achieve good performance combined with low power dissipation.

This chapter is organized as follows. A split delta-sigma modulator architecture using noise coupling and time interleaving is proposed in Section 4.2. Design details for two prototypes follow in Section 4.3. Section 4.4 describes the measured results that verify the effectiveness of the proposed architecture. Finally, a summary of the results is given in Section 4.5.

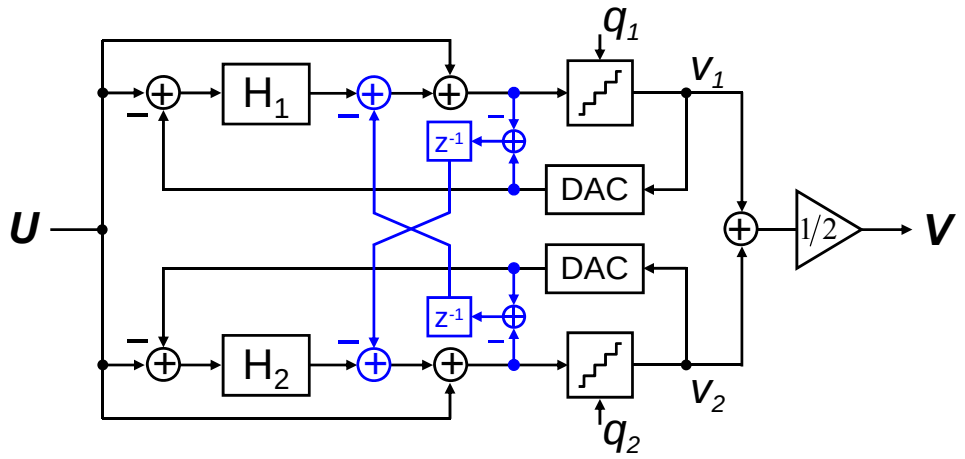
4.2. ARCHITECTURAL CONSIDERATIONS

Effective modulator architecture is a key factor enabling high-resolution and low-power wideband modulator design. The derivation of the configuration used in the device described in this chapter is illustrated in Fig. 4.1. Fig. 4.1(a) shows a split modulator using low-distortion configuration in each path. The advantage of this topology comes from the cancellation of the input signal at the input of loop filter [4][5]. This results in reduced signal swing, and reduces distortion and slew rate effects. The split ADC architecture was proposed earlier in pipeline and successive approximation ADCs, to facilitate digital background calibration [6][7]. It is, however, used in a different context in this design. In splitting the modulator, all capacitances and transconductances (g_m) are cut in half. For constant power dissipation, it can be shown that the split modulator provides the same signal-to-noise-ratio (SNR) and signal bandwidth as the single-path one. This is because both the thermal and quantization noise are enhanced by 6 dB, and so is the output signal.

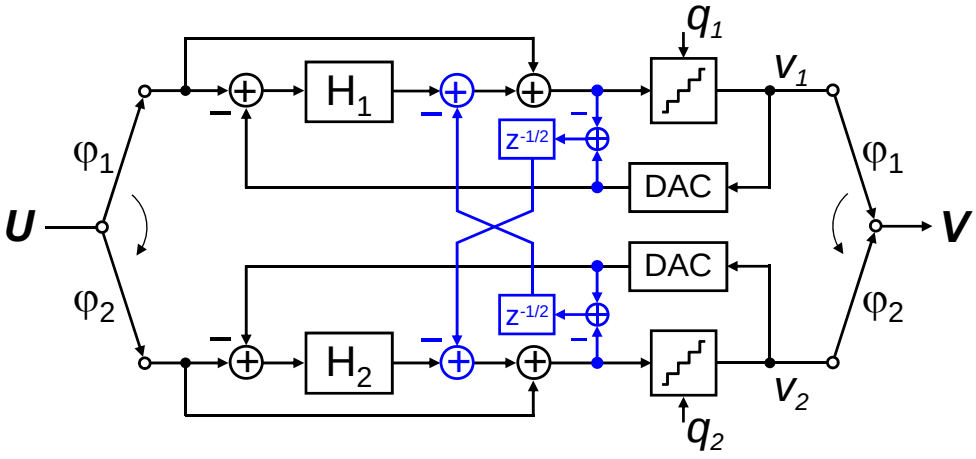
The next step is to introduce quantization noise coupling between the two ΔΣ modulators, as shown in Fig. 4.1(b). The quantization noise of each modulator is delayed by one cycle, and injected into the summing node at the input of the quantizer in other modulator. This results in a new noise transfer function (NTF) for the overall modulator, which is the original NTF multiplied by an additional factor



(a)



(b)



(c)

Figure 4.1: Derivation of the proposed modulator architecture (a) Split modulator; (b) noise-coupled split (NCS) modulator (c) noise-coupled time-interleaved (NCTI) modulator.

$(1-z^{-1})$ [8][9]. Thus, the noise coupling increases the order of the noise shaping by one. This improvement does not require an extra opamp in a low-distortion modulator. Thus, it allows significant performance improvement with little extra overhead. Using a filter instead of a simple delay in the coupling branch, the modulator order can be increased by two or more [9][10]. Since a noise-coupled split (NCS) modulator contains the coupling branches following the gain stages, circuit errors in these branches will be shaped by the preceding loop filter, and hence the performance improvement is insensitive to circuit errors. By enhancing the order of the NTF, noise coupling is equivalent to adding one more integrator to the loop filter. In fact, however, it is better than this, since it does not affect the stability of the loop as much, and enhances the linearity of the A/D conversion. This is true since the noise injected into each loop from the other is uncorrelated to any signal already in the loop.

In a split modulator without noise coupling, the quantization noises of the two loops are decorrelated quickly (typically within a few hundred cycles after power-up) in the presence of thermal noises and circuit errors such as opamp offsets, settling errors and nonlinearities. Fig. 4.2 illustrates the process of the decorrelation of the quantization noises of a split modulator. Here, the correlation of quantization noises from the two loops at time step n after power-up is defined by

$$Correlation(n) = \frac{1}{n}\sum_{k=1}^{n} q_1(k) \cdot q_2(k) \tag{4.1}$$

Therefore, the injected quantization noise is acting as a random dither, and it improves the linearity of the modulator. The stability of the noise-coupled modulator is comparable to that of the original modulator with dither.

Further performance improvement can be achieved by adding time interleaving to the system. The resulting noise-coupled time-interleaved (NCTI) modulator is

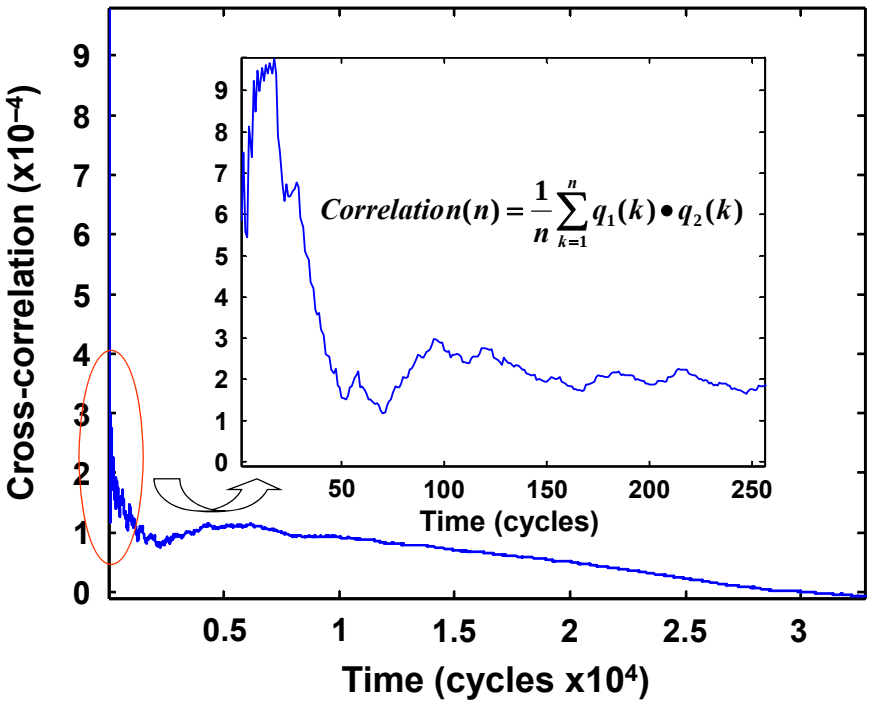
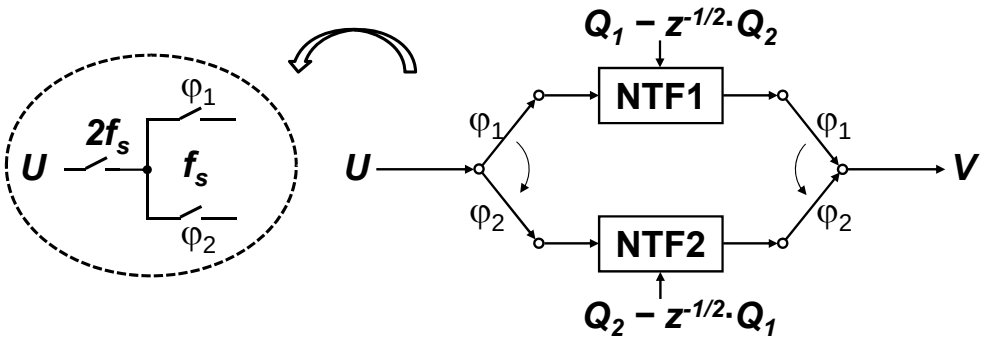


Figure 4.2: The dcorrelation of quantization noises for a split delta-sigma ADC.

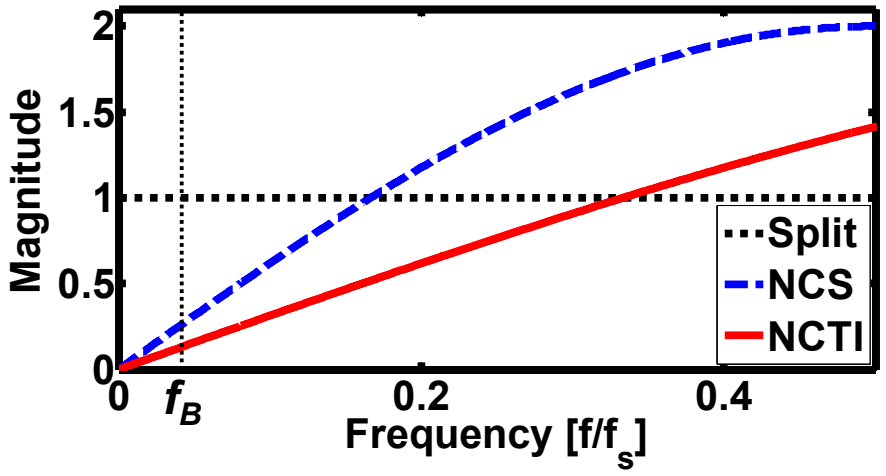
illustrated in Fig. 4.1(c) [11]. As shown in the simplified conceptual block diagram of Fig. 3(a), time interleaving changes the extra factor in the noise transfer function from $(1\text{-}z^{-1})$ to $(1\text{-}z^{-1/2})$. This new factor gives an additional 6 dB signal-to-quantization noise-ratio (SQNR) improvement in the signal band. This occurs since $(1\text{-}z^{-1/2}) \sim (1\text{-}z^{-1})/2$ at low frequencies where $z \sim 1$. The frequency responses of the enhancement factors of the three modulators shown in Fig. 4.1 are compared in Fig. 4.3(b).

Time interleaving also allows a simpler realization of the noise coupling branches, and provides balanced clock loading between both clock phases. Finally, it reduces sensitivity to channel mismatch errors, as a result of the quantization noise suppression around the Nyquist frequency due to the out-of-band zeros of the modulator.

Note that there is also a reduction of signal power due to sampling phase offset



(a)



(b)

Figure 4.3: (a) Block diagram of a NCTI modulator. (b) Comparison of the NTF enhancement factors for various split modulators.

between two channels in NCTI modulator. But this is negligible in time-interleaved oversampled ADC, unlike in time-interleaved Nyquist ADC, since the corresponding factor $(1+z^{-1/2})/2$ is very close to 1 in the signal band.

Generally, the performance of a time-interleaved Nyquist ADC is severely limited by channel mismatch errors, such as timing skew for sampling, channel gain mismatch, channel offset mismatch, and channel bandwidth mismatch [14][15][16]. Foreground or background calibration is often used, either in the analog or digital domain to address these issues [17][18]. This increases the hardware complexity and

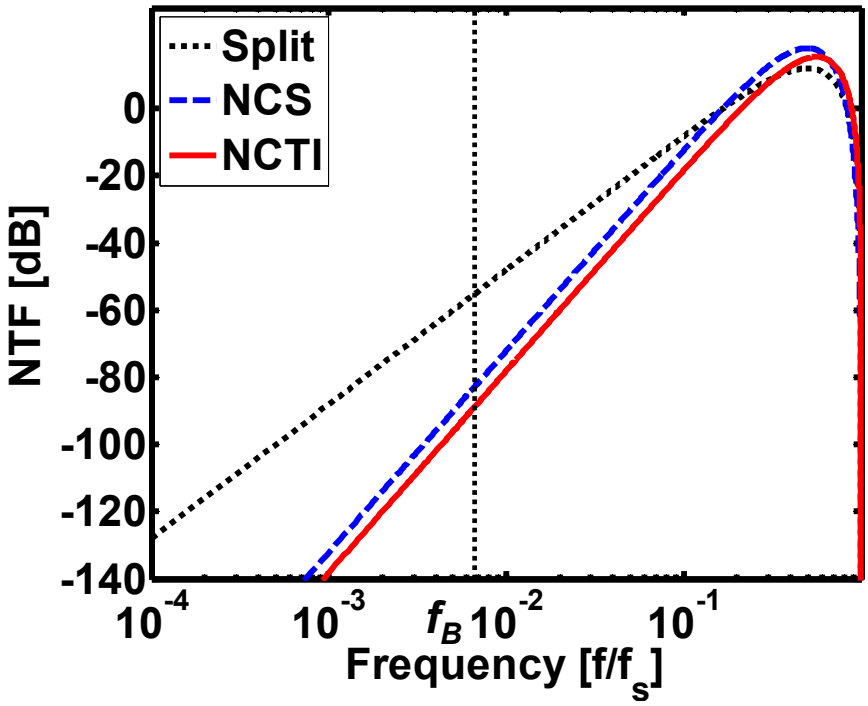


Figure 4.4: Comparison of the NTFs of the three modulators shown in Fig. 4.1, with a second-order loop filter H(z).

power consumption of these ADCs. By contrast, channel mismatch errors do not limit the performance of the proposed modulator. The performance of these modulators is quite robust to channel mismatches, due to the double zeros of the NTF at the Nyquist frequency f_s, as illustrated in Fig. 4.4. These double zeros are introduced by operating the two second-order delta-sigma modulators with time-interleaved sampling. Since there is thus no significant quantization noise power at the Nyquist frequency f_s, the modulator can tolerate noise folding due to channel mismatches up to 5%. However, the added double zeros at Nyquist frequency also raise the in-band noise floor, exhibiting a trade-off between SQNR performance and robustness to channel mismatch errors.

The proposed modulator topology was realized with second-order low-distortion loops. Figure 4.4 shows the NTF magnitude responses of the three delta-sigma

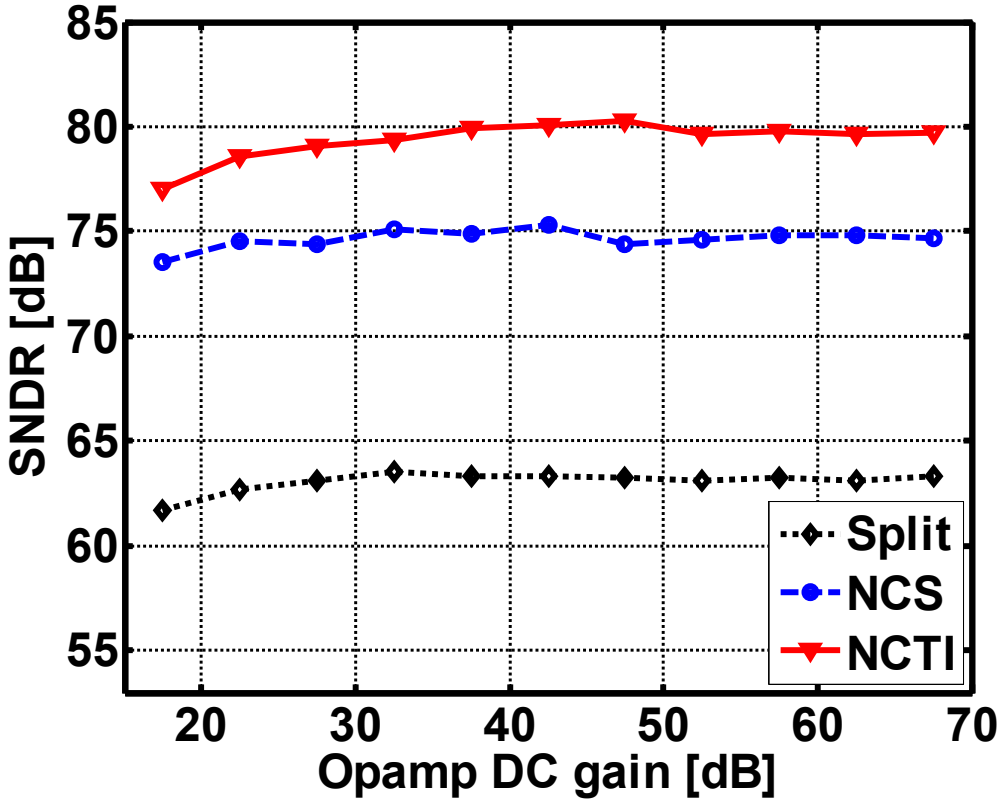


Figure 4.5: SNDR variation with opamp DC gain whose mismatch is 5% between the two channels.

ADCs introduced in Fig. 4.1. The dotted line for the uncoupled second-order modulator shows the expected 40 dB/decade slope. The NCS second-order modulator (dashed line) shows a 60 dB/decade slope. Finally, the time-interleaved noise-coupled modulator has the same slope as the NCS one, but the curve is 6 dB lower. With an OSR of 12, the SQNR improvement with NCTI modulator is 19 dB compared to a conventional second-order modulator and it requires only minimal extra hardware cost. To verify the concept, a realistic delta-sigma modulator model was simulated with Matlab and Simulink. The modeled delta-sigma modulator included various circuit errors mentioned earlier. The graph in Fig. 4.5 shows the signal-to-noise-and-distortion-ratio (SNDR) as a function of the integrator opamp DC gain and channel mismatch. The proposed modulator shows more than 17 dB

SNDR improvement over the conventional modulator, and its performance is robust in the presence of various circuit and channel mismatch errors. This simulation result confirms that the proposed topology is effective and applicable to practical modulator design.

4.3. SC CIRCUIT IMPLEMENTATION

The implementation of proposed NCTI modulator in a 0.18μm CMOS process is described in this section. Figure 4.6 shows the block diagram of implemented prototype ADC. It is a time-interleaved second-order low-distortion modulator with noise coupling. It provides third-order noise shaping due to noise coupling and an additional 6 dB SQNR thanks to time interleaving.

The detailed switched-capacitor (SC) circuit realization is shown in Fig. 4.7. The details of the input circuitry are omitted here for simplicity. Each loop contains two integrators, followed by an active adder. The low-distortion modulator requires

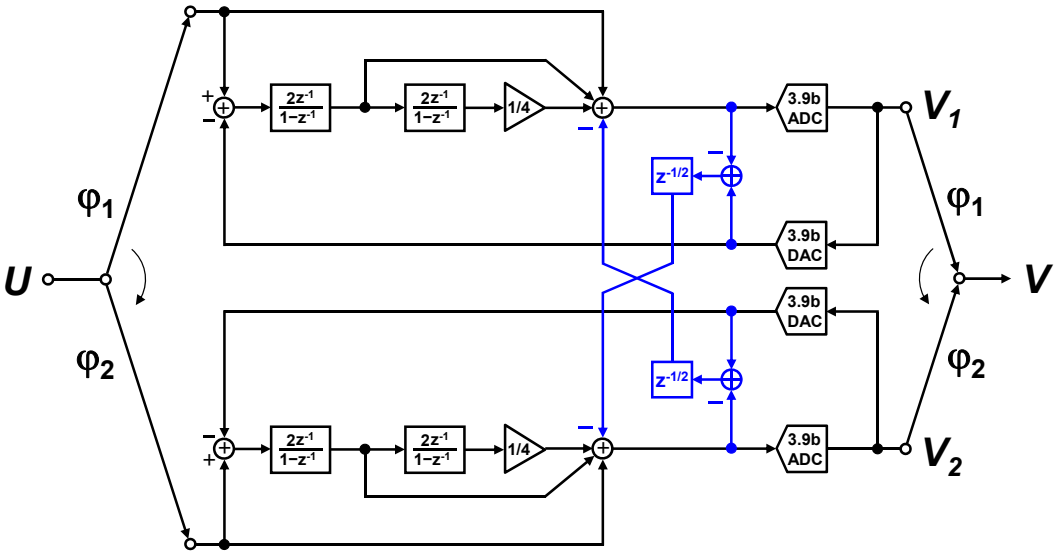


Figure 4.6: Block diagram of the prototype ADC.

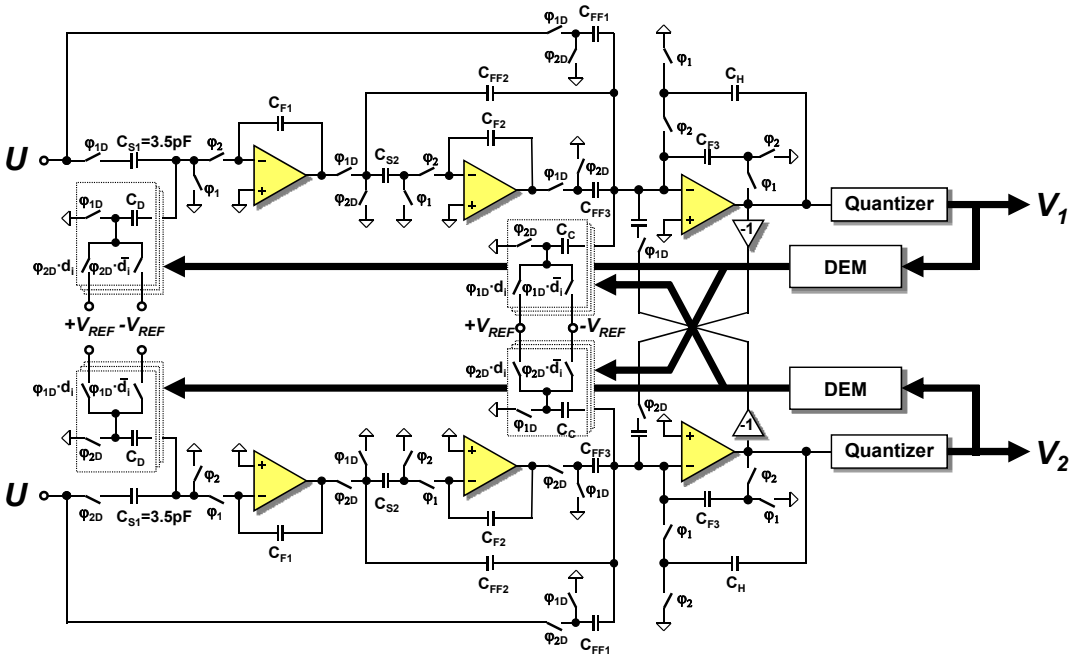
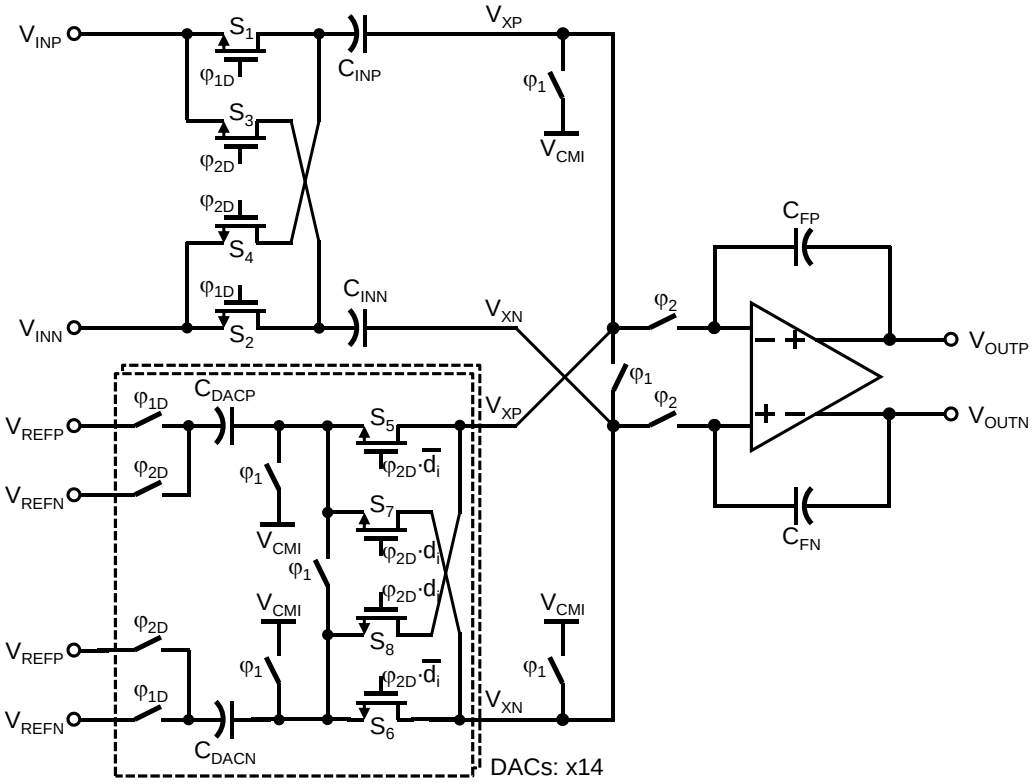


Figure 4.7: SC circuit implementation of the prototype ADC.

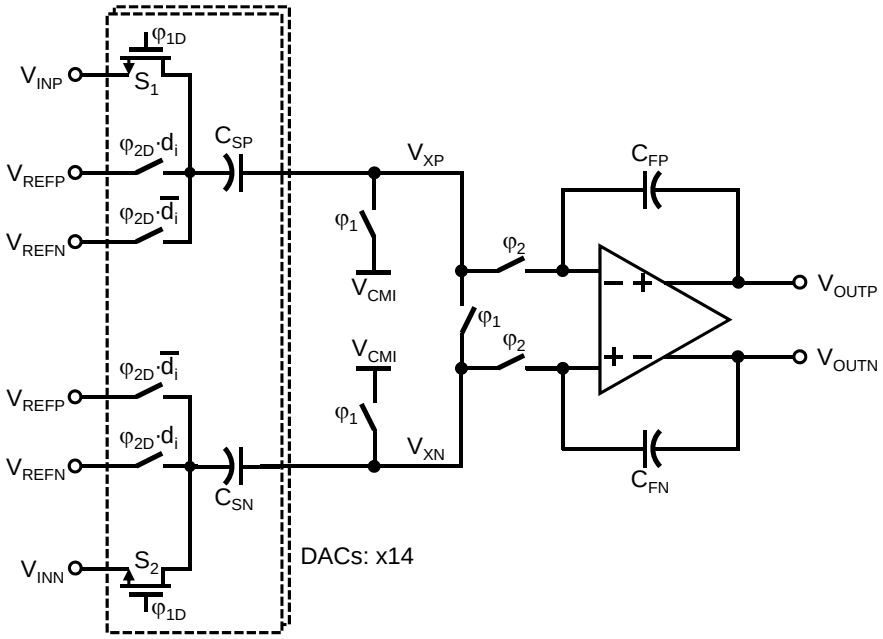
signal summation at the input of quantizer. Passive SC adder, which does not require extra opamp, could also be used, but the signal swing is then reduced due to parasitic capacitances, especially when the loop contains a multibit quantizer. The SC adder is also susceptible to kick-back noise from quantizer. For these reasons, in this design active, rather than passive, summing with an offset-compensated amplifier was used. The noise coupling also utilized the active adder opamp.

To compensate for the low OSR of 12, 15-level quantizers were used, along with 15-level unit-capacitor DACs. Data-weighted averaging (DWA), using a 4-stage logarithmic shifter, was applied to filter the mismatch errors of the 15 level DACs.

Two slightly different prototypes were implemented, Prototypes A and B. They differed only in their input branches, as shown in Fig. 4.8. One of the key problems with wideband modulators is signal dependent DAC reference noise. This is particularly serious when shared input sampling and DAC capacitors are used. To avoid this problem, separate input sampling and DAC capacitors were used for

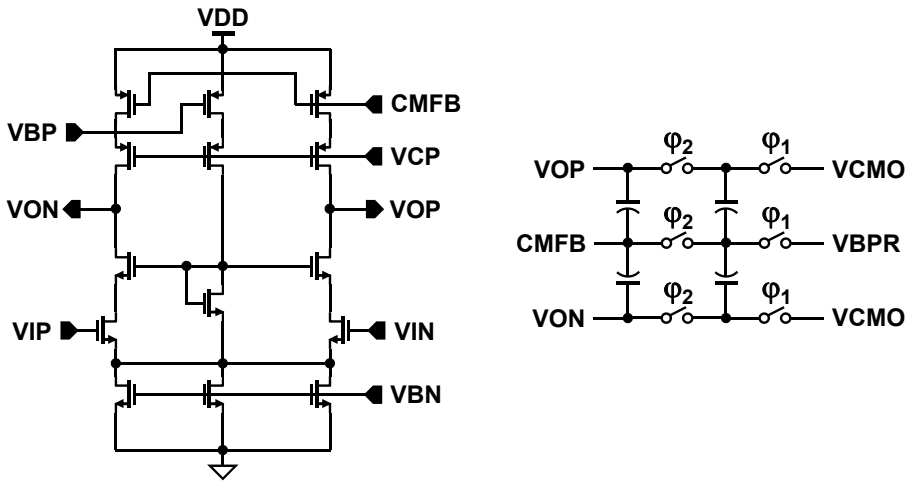


(a)



(b)

Figure 4.8: SC circuit implementation of the 1st integrator (a) for prototype A; (b) for prototype B.



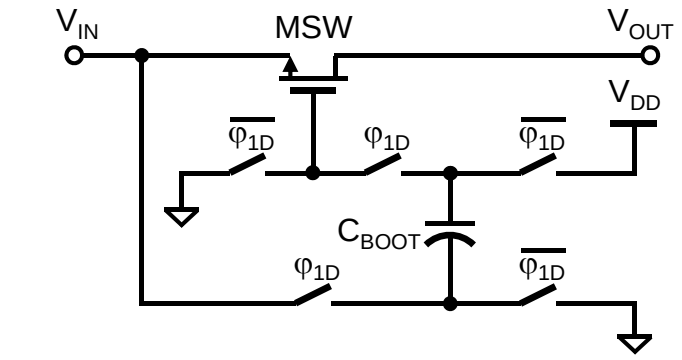
For first integrator opamp

DC Gain	PM	UGBW	I_{TOT}	VDD	Process
50dB	> 70°	1.2GHz	2.6mA	1.5V	0.18μm

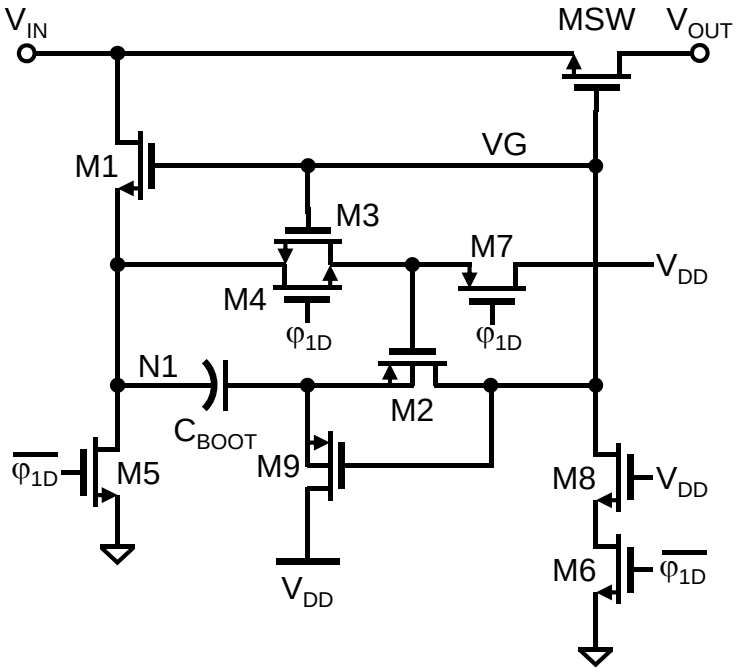
Figure 4.9: Telescopic cascode opamp with SC common-mode feedback.

Prototype A, while shared capacitors in Prototype B. However, the same feedback factor as in Prototype B was preserved in Prototype A, by reducing the size of each input sampling and DAC capacitor by half, and doubling the input and DAC signal swings using cross-coupled switches between positive and negative rails, as illustrated in Fig. 4.8.

The signal swing of the loop filter of the low-distortion modulator is greatly reduced. This allowed the use of the power-efficient and low-noise telescopic cascode opamp with a 1.5 V supply (Fig. 4.9). To minimize the noise contribution from two top PMOS transistors controlled by the common-mode feedback voltage, the transconductances of these devices were made much smaller than those of the input differential pair, by assigning bigger overdrive voltage for the given output swing requirement. The differential output signal swing of the opamp is ±0.72 V. Power-efficient SC common-mode feedback is used. Figure 4.9 shows the opamp structure, along with its simulated performance in the first integrator. It achieves a



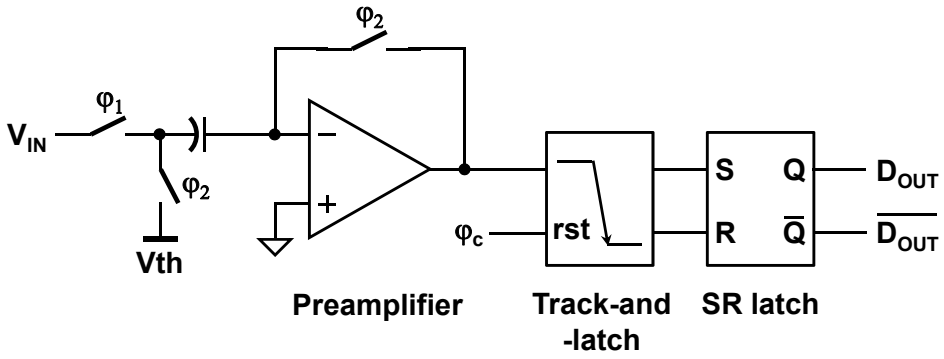
(a)



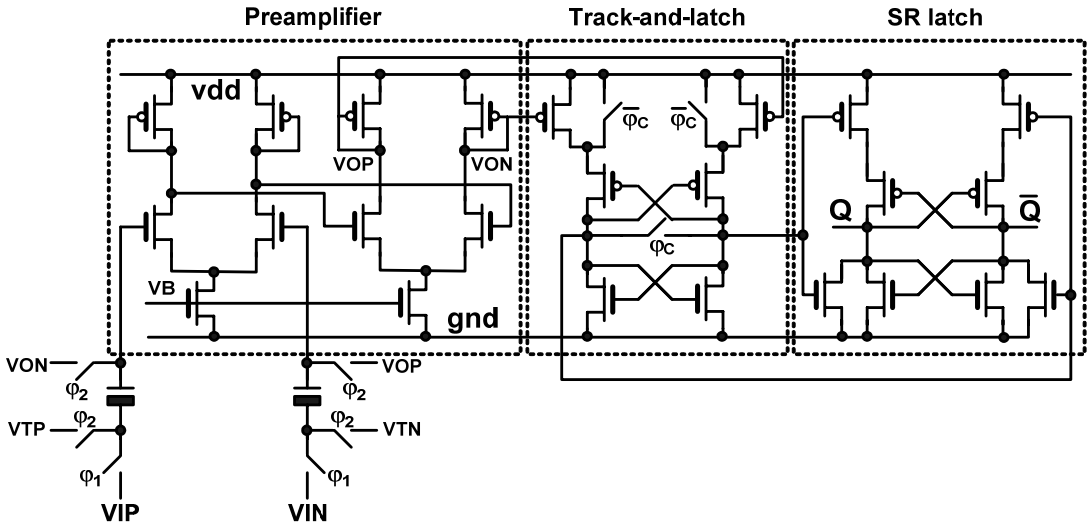
(b)

Figure 4.10: The bootstrapped clock signal generator (a) simplified diagram; (b) detailed circuit realization [19].

UGBW of 1.2 GHz and a DC gain of 50 dB, while drawing 2.6 mA bias current. Similar but scaled opamps are used in the second integrator and the active adder. The critical input sampling switches use bootstrapped clock signals to insure linear sampling. Figure 4.10 shows the generator circuit for the bootstrapped clock signal [19].



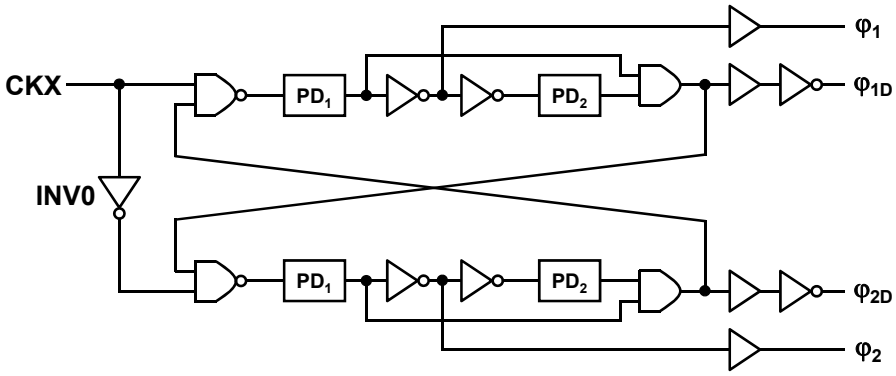
(a)



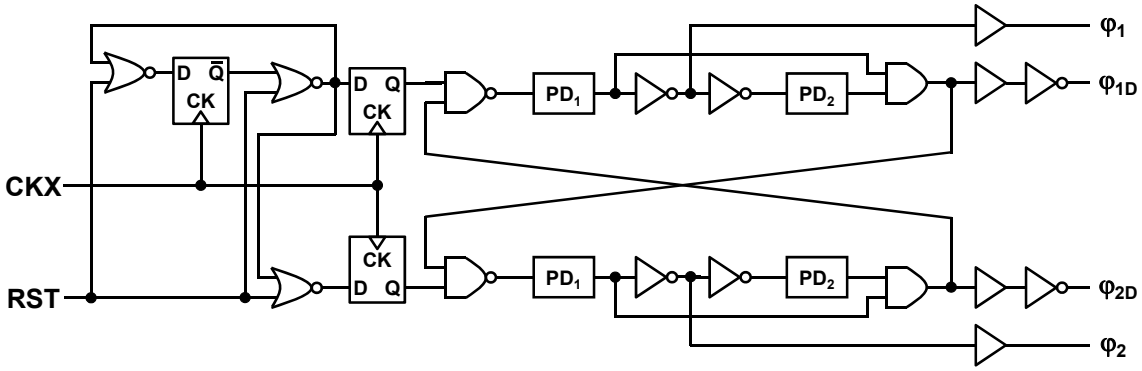
(b)

Figure 4.11: Quantizer branch: (a) block diagram (b) circuit implementation.

The 4b quantizer is composed of a two-stage preamplifier, a track-and-latch stage and a set-and-reset (SR) latch, as shown in Fig. 4.11 [20][21]. Input offset sampling is used to minimize the effects of offset errors. Since the preamplifier has an open-loop gain of around 10, the input-referred offset is reduced by about this factor. During the comparison phase φ_1, the track-and-latch is in the track mode and senses the output of the preamplifier. Before the end of φ_1 phase, the φ_c (reset) signal of the track-and-latch stage goes from high to low, and triggers the regeneration and latch. The transistor sizes in the quantizer and the DWA logic were optimized to satisfy the



(a)



(b)

Figure 4.12: Clock generator: (a) conventional (b) proposed.

critical timing requirements.

By using both edges of the clock for sampling in the dual-channel time-interleaved modulator, the clock frequency did not have to be doubled. However, equal lengths of the clock pulses for both phases of clock were critical to avoid any performance deterioration due to mismatch-induced quantization noise folding in the dual-channel NCTI modulator. Conventional nonoverlapping clock generator is not appropriate, as illustrated in Fig. 4.12 (a). This is because the inverter 0 introduces the difference of pulse width between both clock phases corresponding to twice its delay. The proposed clock generator that is suitable for time-interleaved or double-sampled modulator is shown in Fig. 4.12 (b). To ensure 50% duty cycle and the

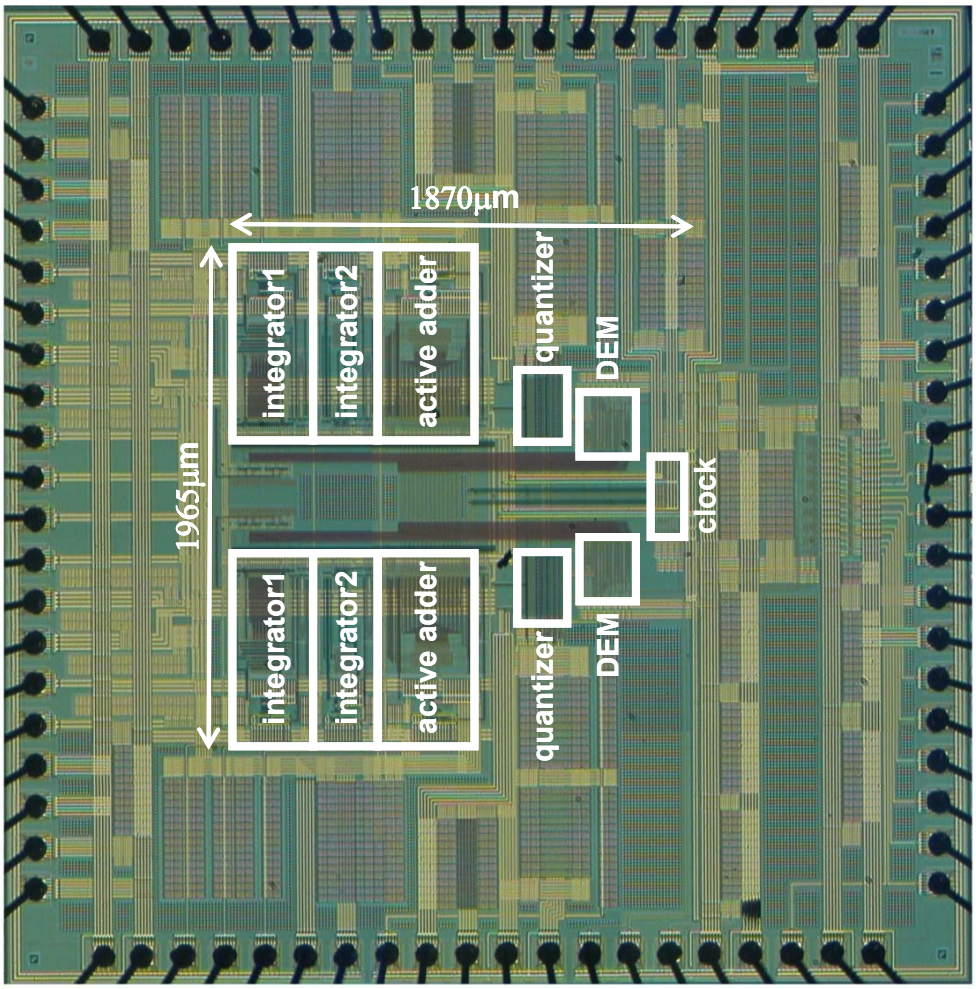


Figure 4.13: Chip micrograph for prototype A.

generation of two equal clock-phase pulse, a $2{\cdot}f_S$ clock and an on-chip divide-by-two circuit is used as illustrated in Fig. 4.12.

Both proposed modulator architectures were designed and fabricated in a 2P4M 0.18μm CMOS process. The die micrograph for prototype A is shown in Fig. 4.13. The two modulators have a mirror symmetry, and the clock generator is located at the right center. The critical pins for analog signals and power pins are at the left, top, and bottom sides, while the digital signal pins are at the right side. The die size was determined not by the core modulator area, but by the required number of pads. Most of the empty area was filled with dummy metals and decoupling capacitors.

4.4. EXPERIMENTAL RESULTS

Figure 4.14 shows the measured output spectrum of prototype A operated at peak SNDR. The input signal was a 47.3 kHz sine wave with -1.45 dBFS amplitude, and the clock frequency was 100 MHz. The 60 dB/dec slope of the quantization noise shows that third-order noise shaping was achieved with noise coupling. The SNDR is 79 dB in a 4.2 MHz signal band. The linearity is also improved due to noise coupling, and the SFDR is 101 dB. Figure 4.15 shows the spectrum at peak SNDR for prototype B, using shared input sampling and DAC capacitors. The input signal was a 200 kHz sine wave with -1.37 dBFS amplitude, and the clock frequency was 60 MHz. The SNDR is 81 dB in a 2.5 MHz signal band, and the SFDR is 105 dB. The maximum clock frequency for this prototype is restricted up to 60 MHz by the signal-dependent DAC reference noise caused by the shared input and DAC capacitors. Figure 4.16 shows the SNR and SNDR variation with input signal amplitude for prototype A. It demonstrates nearly identical SNR and SNDR performances, indicating the high linearity and low distortion of the proposed modulator. The peak SNDR was 79 dB, the DR was 81 dB, and the peak total harmonic distortion (THD) was -98 dB. The analog power was 13 mW and the digital power was 15 mW. In spite of the large digital power (due to rushed design), the FOM was only 0.48 pJ/conversion-step. Figure 4.17 shows the SNR, SNDR, and DR variations with input signal frequencies from 10 kHz to 4 MHz, for prototype A. A fully-differential input signal up to 200 kHz was obtained from an Audio Precision signal generator, and a single-ended input signal from 200 kHz to 4 MHz was obtained from an RF signal source and bandpass filters. The single-ended input signal was converted into a differential signal via an on-board differential buffer. Figure 4.18 shows the SNR and SNDR variations with input signal power for

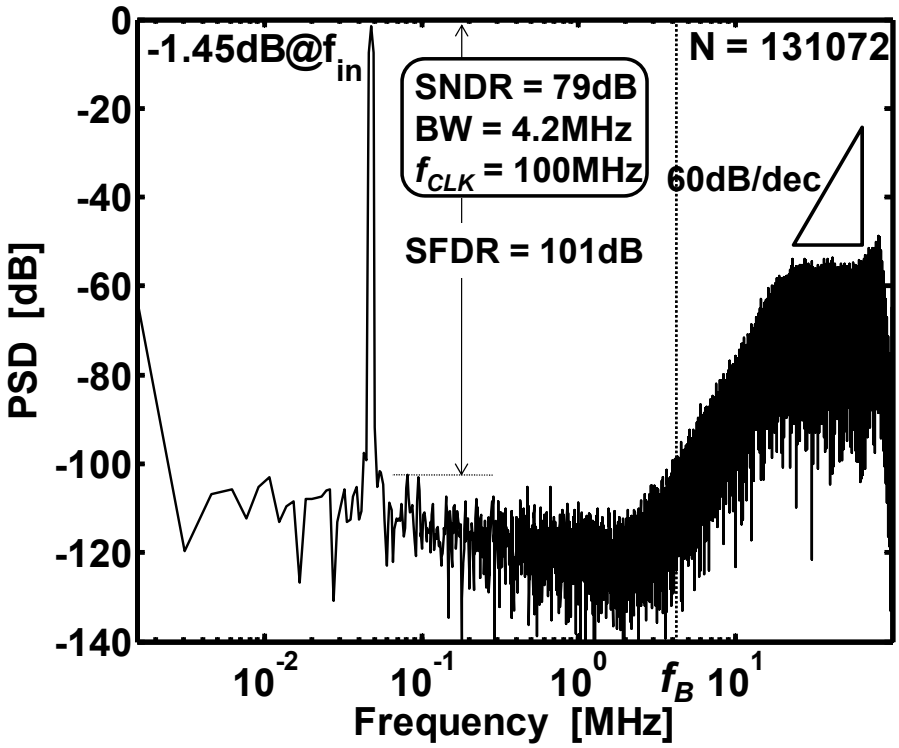


Figure 4.14: Measured spectrum for prototype A.

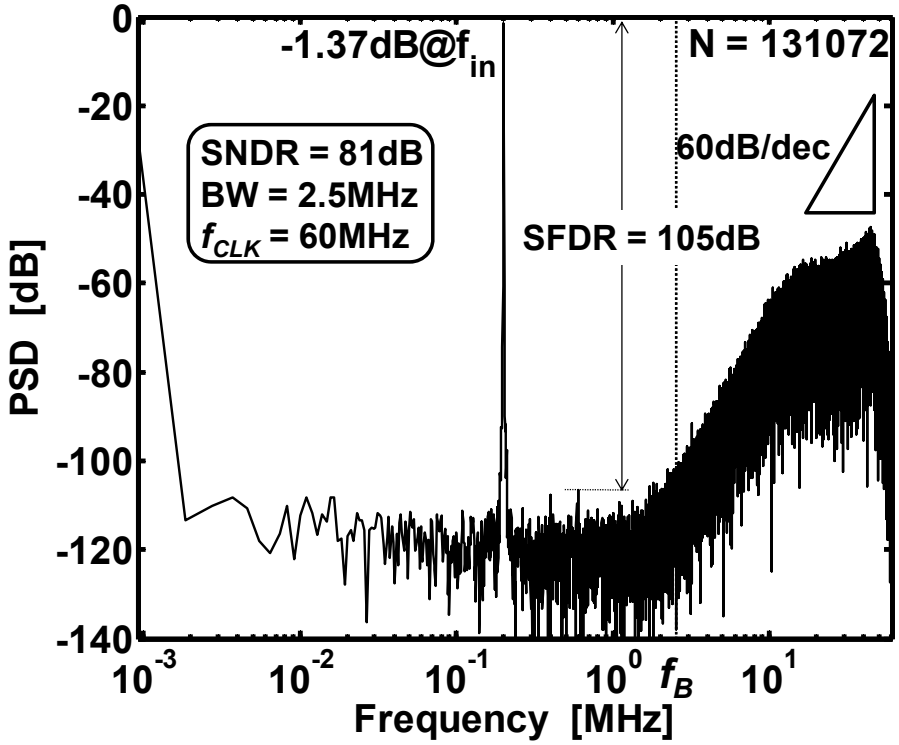


Figure 4.15: Measured spectrum for prototype B.

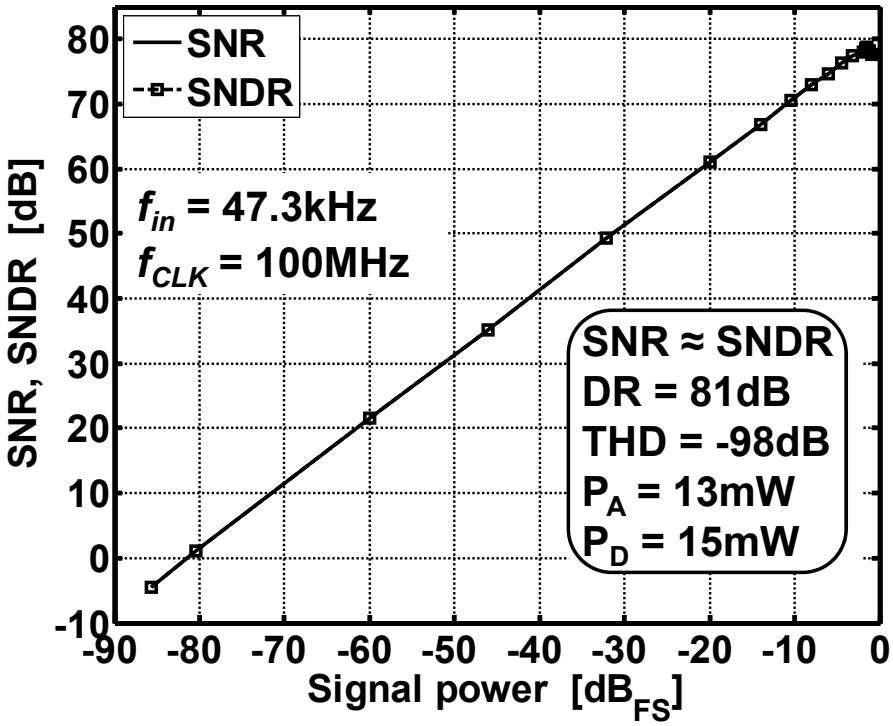


Figure 4.16: Measured SNR and SNDR variation with input signal power for prototype A.

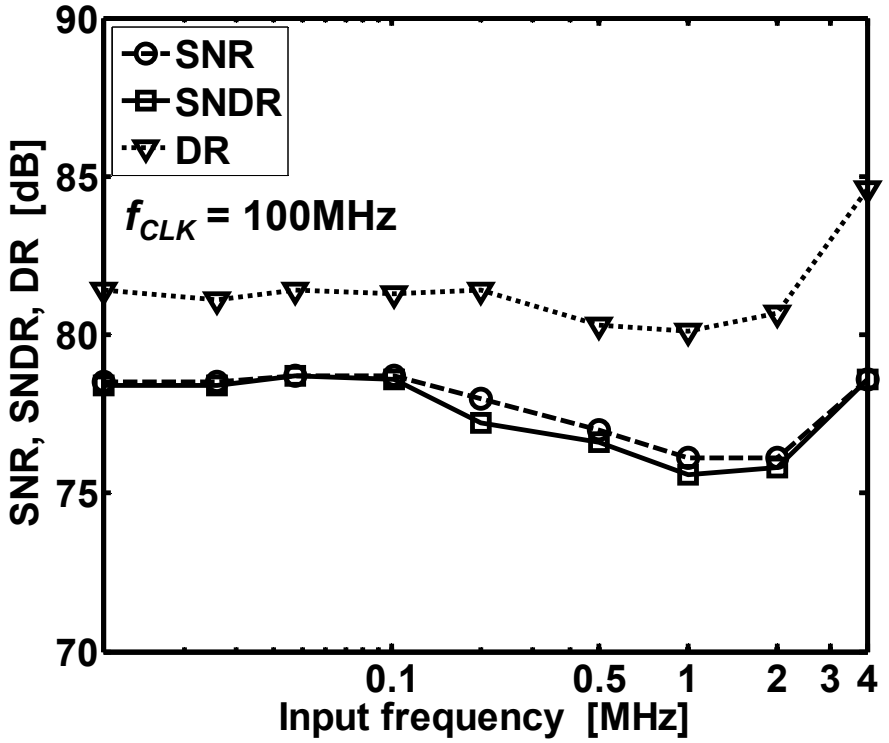


Figure 4.17: Measured SNR, SNDR, and DR variation with input signal frequencies for prototype A.

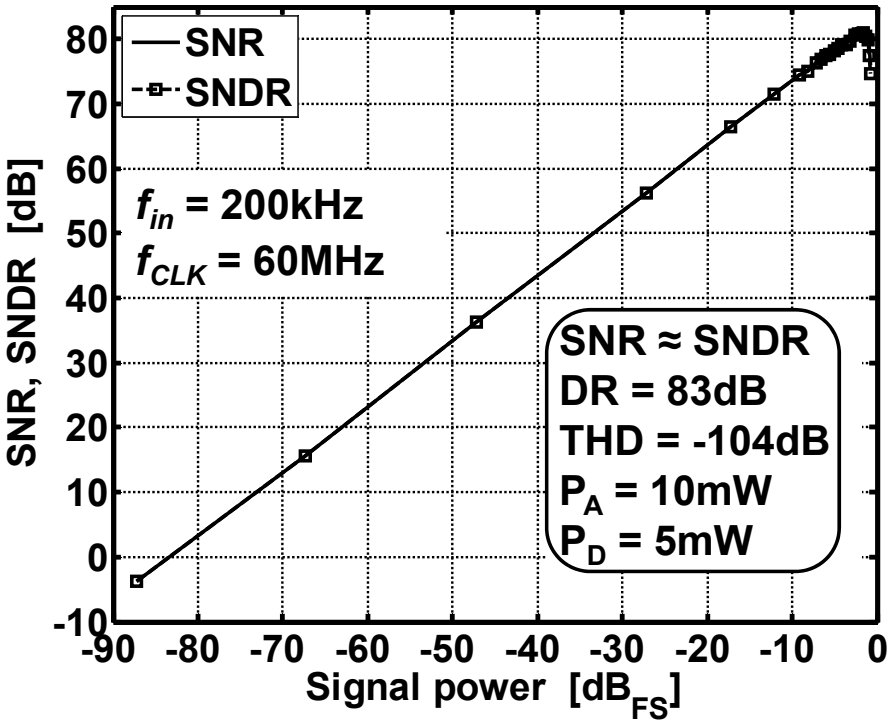


Figure 4.18: Measured SNR and SNDR variation with input signal power for prototype B.

prototype B. The peak SNR and SNDR were both over 81 dB, and the DR was 83 dB in a 2.5 MHz signal band. The analog power was 10 mW and digital power was 5 mW. The FOM was 0.33 pJ/conversion-step. Table 4.1 shows the summary of the measured performances for both prototypes. For prototype A, 81 dB DR, 79 dB SNDR, and -98 dB THD are achieved in a 4.2 MHz signal band with a 100 MHz clock and an OSR of 12. The total power dissipation is 28 mW, drawn mostly from the digital circuitry, and the FOM is 0.48 pJ/conversion step. For prototype B, 83 dB DR, 81 dB SNDR and -104 dB THD are obtained in a 2.5 MHz signal band with a 60 MHz clock. The total power dissipation is 15 mW and the FOM is 0.33 pJ/conversion-step. Figure 4.19 compares the described devices with other DT modulators publicized recently. Both prototypes show good FOMs in a MHz range signal band, and their FOMs could readily be improved further with optimized digital design. This illustrates the potential usefulness of the proposed modulator

TABLE 4.1: PERFORMANCE SUMMARY.

Prototype	A	B
Sampling frequency	200MHz	120MHz
ΔΣ clock frequency	100MHz	60MHz
Signal bandwidth	4.2MHz	2.5MHz
OSR	12	
Input range (diff.)	$1.44V_{pp}$	
C_{IN} and C_{DAC}	separate	shared
Dynamic range	81dB	83dB
SNDR	79dB	81dB
THD	−98dB	−104dB
FOM	0.48pJ/conversion	0.33pJ/conversion
Power consumption	13mW (A), 15mW (D)	10mW (A), 5mW (D)
Power supply	1.5V (A), 1.6V (D)	
Process	0.18μm 2P4M CMOS	
Core area	$3.67mm^2$	

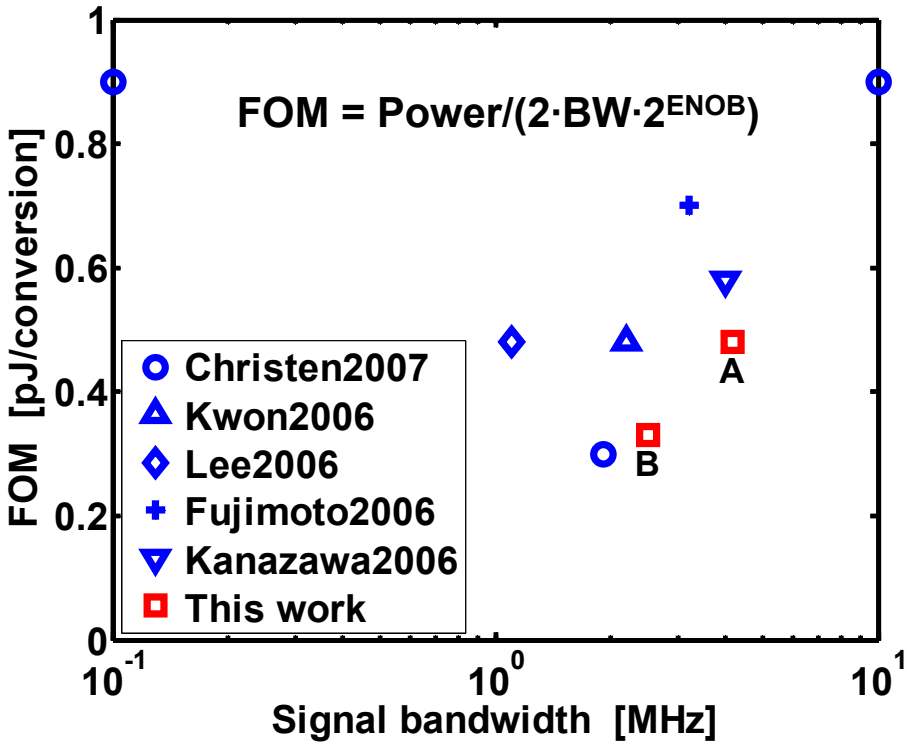


Figure 4.19: Comparison with other DT modulators published recently.

architecture.

4.5. SUMMARY

A noise-coupled time-interleaved ΔΣ ADC architecture was proposed. It offers enhanced noise shaping, improved linearity, and robust performance. This allows significant performance improvement with little overhead, and is particularly suitable for the design of wideband low-power modulators. The disadvantages are more complicated layout and clock routing. Two prototype designs based on the proposed architecture have been realized, and their measured performances confirmed the effectiveness of this design appraoch. Prototype A showed a 79 dB SNDR and -98 dB THD in a 4.2 MHz signal band. This compares well with the theoretical prediction of the SQNR for a conventional third-order modulator with a 4b quantizer, which is 80 dB with an OSR of 12.

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CHAPTER 5. EFFICIENT DOUBLE-SAMPLING DELTA-SIGMA ADC

Abstract

A novel double-sampling integrator is proposed, which is insensitive to path mismatch, and does not introduce a detrimental extra factor into the loop gain. It allows the use of efficient design methods for ΔΣ ADCs.

5.1. INTRODUCTION

Double sampling allows the speeding up of the operation of switched-capacitor (*SC*) integrators without increasing the required opamp bandwidth [1]. It allows the doubling of the oversampling ratio (*OSR*) in a ΔΣ ADC. However, in its simplest implementation with two sampling capacitors in a push-pull mode, any mismatch in the values of the two paths introduces the modulation of the input signal with an *fs/2* carrier, where *fs* is the doubled sampling rate. This in turn results in the folding of the spectrum around *fs/2* to the baseband as shown in Fig. 5.1. Usually, the input signal to ΔΣ ADC is band-limited by a front-end antialiasing filter, so that the residual spectral power around *fs/2* is significantly reduced. Thus, the noise folding due to the input signal path is negligible. However, as explained in [2], it is unacceptable in a ΔΣ ADC when the integrator processes the wideband feedback DAC signal, which has most of its spectral power around *fs/2*.

5.2. CONVENTIONAL DOUBLE-SAMPLING INTEGRATOR

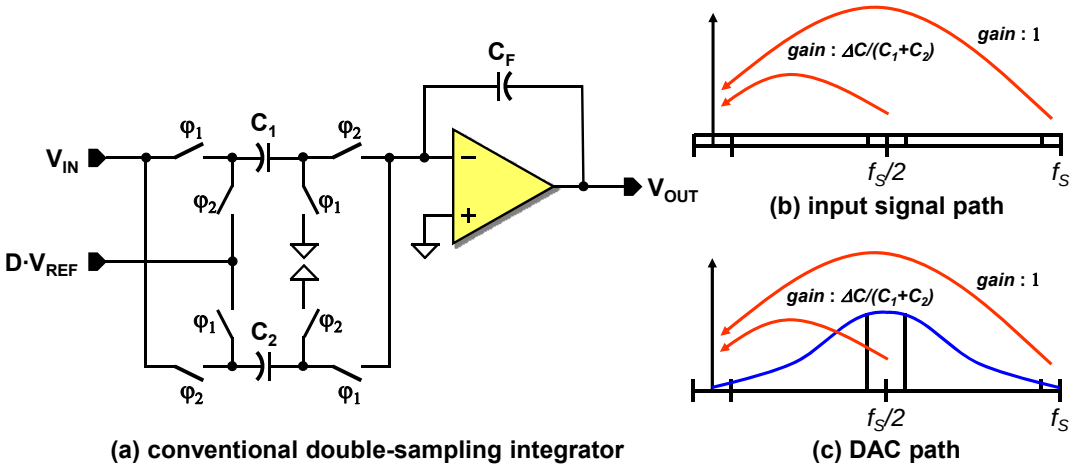

Figure 5.1: Conventional double-sampling integrator and quantization noise folding by the amplitude modulation due to capacitor mismatch between C_1 and C_2 [2].

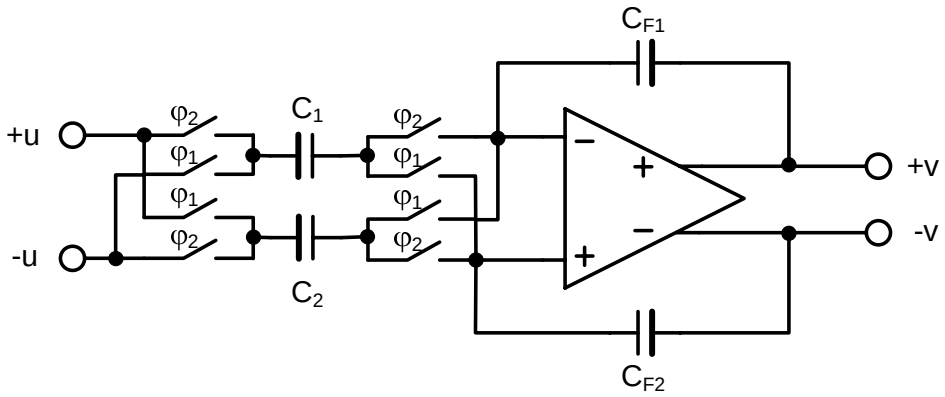

Figure 5.2: Fully floating differential SC integrator [2].

5.2.1. Senderowicz's fully-floating integrator

The floating integrator proposed by Senderowicz et al. [2] (Fig. 5.2) remedies this problem. Nominally, $C_1=C_2=C$; As shown in [2], a mismatch of C_1 and C_2 does not cause modulation of the differential signal. Modulation occurs only in the common-mode (*CM*) input signal component, which is rejected by the differential structure. A shortcoming of this integrator is that it introduces an extra factor $(1+z^{-1})/2$ into the loop gain. As shown below, the resulting added pole affects the stability, and hence

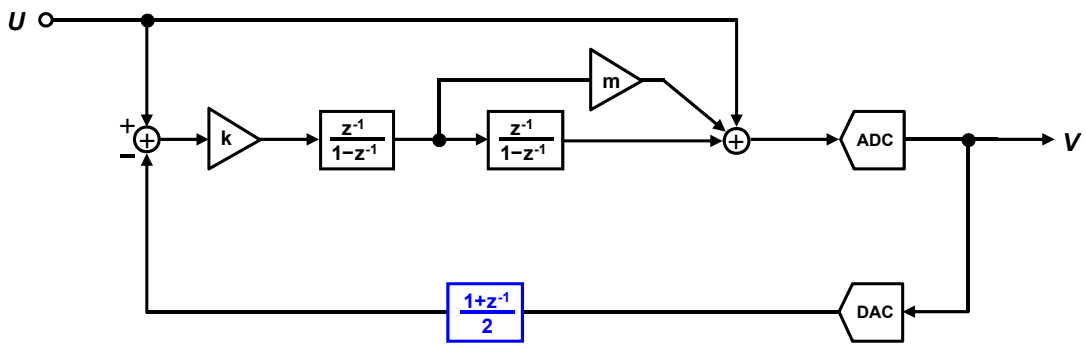

Figure 5.3: Second-order low distortion modulator [4] with extra feedback factor.

requires a modification of the design parameters of the circuit, resulting in larger integrator capacitors, and a loss in the signal-to-quantization noise ratio (*SQNR*) of the ADC. The latter can be reduced by using more complex architectures and/or sophisticated design procedures (see, e.g., [3]).

5.2.2. Extra feedback factor and modulator loop stability

To evaluate the effect of extra factor $(1+z^{-1})/2$ on the modulator loop dynamics, the stability of a second-order low distortion ΔΣ ADC [4] with added feedback factor (Fig. 5.3) was analyzed. The extra pole introduced makes the stability of this loop to be that of third-order one. The three poles cannot be chosen independently, due to the limited degrees of freedom afforded by parameters k and m [3]. The signal transfer function (*STF*) and noise transfer function (*NTF*) are given by

$$STF = \frac{1+(km-2)z^{-1}+(k-km+1)z^{-2}}{1+(\frac{km}{2}-2)z^{-1}+(\frac{k}{2}+1)z^{-2}+\frac{k}{2}(1-m)z^{-3}} \tag{5.1}$$

$$NTF = \frac{(1-z^{-1})^2}{1+(\frac{km}{2}-2)z^{-1}+(\frac{k}{2}+1)z^{-2}+\frac{k}{2}(1-m)z^{-3}} \tag{5.2}$$

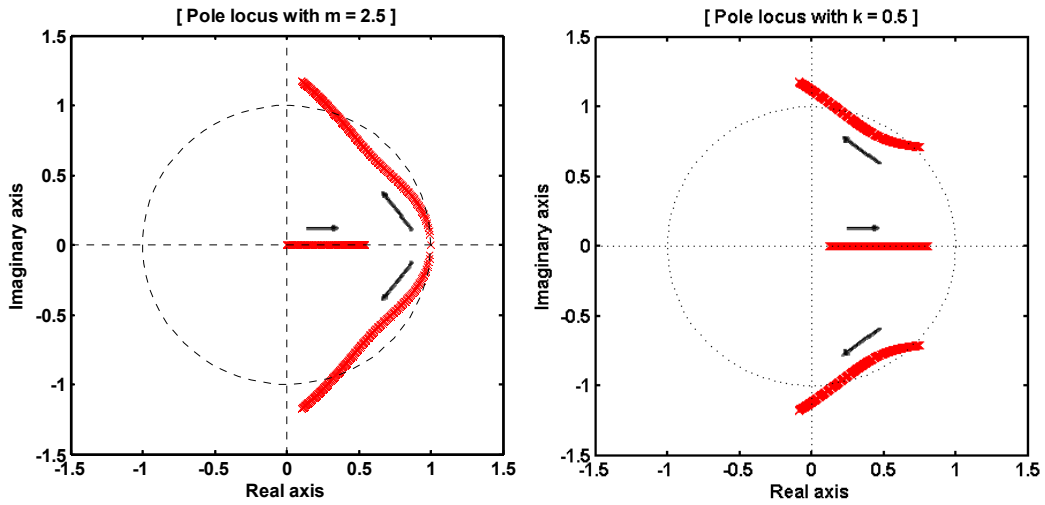

Figure 5.4: (a) Pole locus with k at m = 2.5. (b) Pole locus with m at k = 0.5 for modulator in Fig. 5.3 (arrows for increasing k and m).

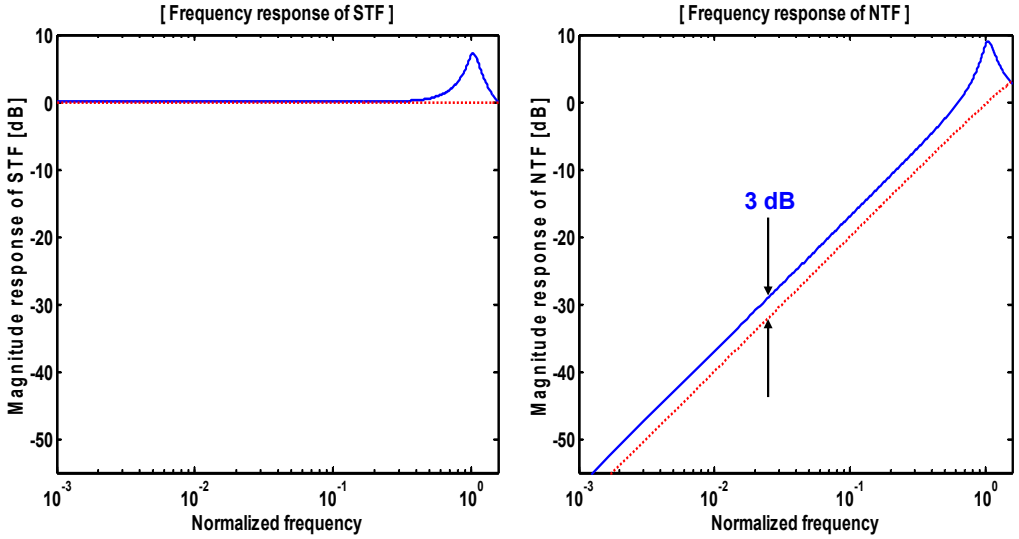

Figure 5.5: Frequency response of *STF* and *NTF* with k = 0.5 and m = 2.5 for modulator in Fig. 5.3. Dotted lines are for the same modulator without extra feedback factor.

The poles of *STF* and *NTF* should be inside the unit circle in the complex z-plane for the modulator loop to be stable. For the original parameter values (k = 1, m = 2) two of the poles will be larger than 1 in magnitude. To find coefficient pairs which make the loop stable, the pole locus was drawn by sweeping one of the coefficients while

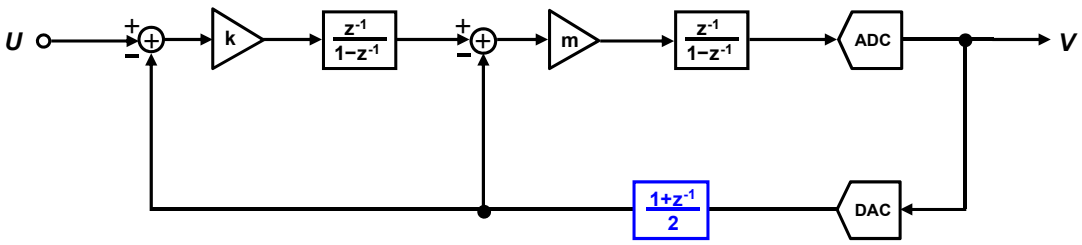

Figure 5.6: Second-order Boser-Wooley modulator [5] with extra feedback factor.

keeping the other one constant at each run. It was found that with $m = 2$, k should be less than 0.33172 to meet its stability requirement. In Fig. 5.4, the pole locus was drawn with different k values at $m = 2.5$ and with m values at $k = 0.5$. For $m = 2.5$, k should be 0 to 0.66 for the stable operation. Likewise, m should be between 1.725 and 3.77 for $k = 0.5$. The frequency response of *STF* and *NTF* was illustrated in Fig. 5.5 with $k = 0.5$ and $m = 2.5$. The quantization noise is 3 dB higher than the original one without the extra feedback factor. It can be observed that at least 3 dB performance degradation is unavoidable. There is out-of-band peaking observed in both *STF* and *NTF* frequency responses. The performance gap gets bigger with reduced peaking in *STF* and *NTF*.

A similar analysis was done for a classical second-order feedback modulator (Fig. 5.6) [5]. The *STF* and *NTF* are given by

$$STF = \frac{kmz^{-2}}{1 + (\frac{m}{2} - 2)z^{-1} + (\frac{km}{2} + 1)z^{-2} + \frac{m}{2}(k-1)z^{-3}} \tag{5.3}$$

$$NTF = \frac{(1 - z^{-1})^2}{1 + (\frac{m}{2} - 2)z^{-1} + (\frac{km}{2} + 1)z^{-2} + \frac{m}{2}(k-1)z^{-3}} \tag{5.4}$$

The pole locus was drawn by sweeping k at $m = 0.5$, and by sweeping m at $k = 0.5$ in Fig. 5.7. It was found that k should be $0 \sim 0.62$ at $m = 0.5$ and m should be $0 \sim 1.33$ at $k = 0.5$ for stable modulator operation. The frequency responses of *STF* and *NTF*

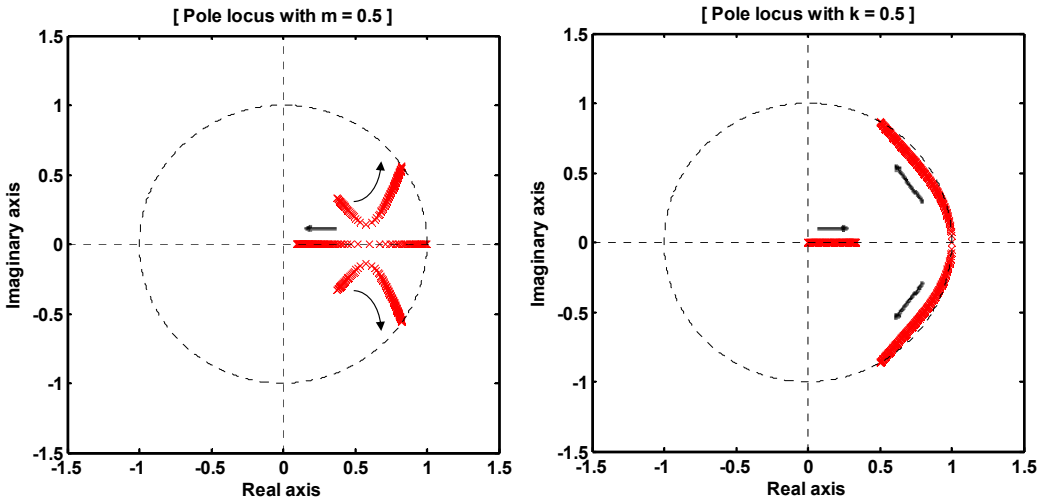

Figure 5.7: (a) Pole locus with k at m = 0.5. (b) Pole locus with m at k = 0.5 for modulator of Fig. 5.6 (arrows for increasing k and m).

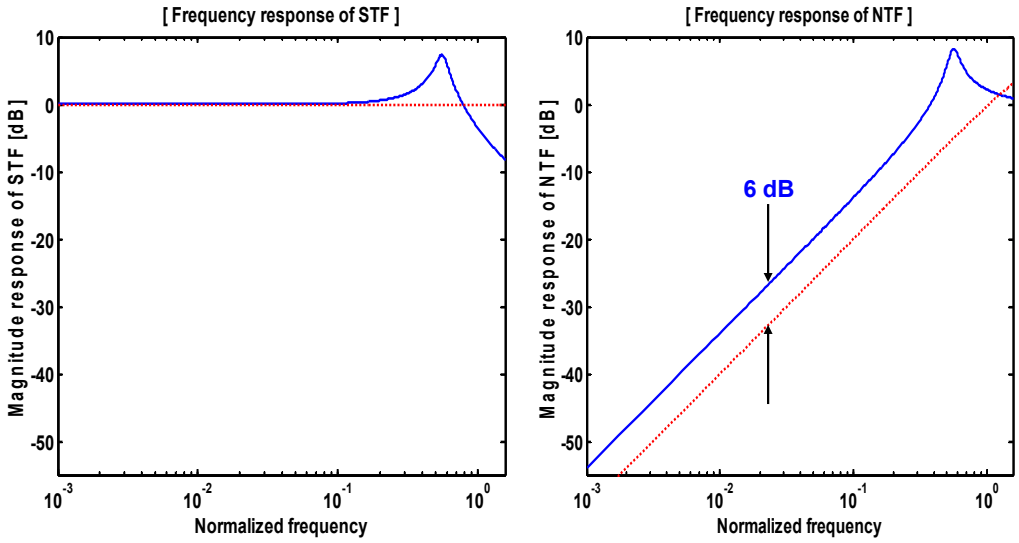

Figure 5.8: Frequency response of *STF* and *NTF* with k = 0.5 and m = 0.5 for the modulator of Fig. 5.6. Dotted lines are for the same modulator without extra feedback factor.

for this modulator are shown in Fig. 5.8 with k = 0.5 and m = 0.5. There is a 6 dB performance degradation due to the increased *NTF,* along with out-of-band peaking in both *STF* and *NTF* frequency responses, as was the case for the low-distortion modulator.

5.3. PROPOSED DOUBLE-SAMPLING INTEGRATOR

Here, we propose a circuit-level solution to the above-mentioned problem, through a modification of the Senderowicz integrator. The proposed circuit retains the robustness to mismatch errors, and yet avoids the detrimental extra feedback factor $(1+z^{-1})/2$, thus allowing the design of more stable and efficient ADCs using optimized architectures and circuitry. The standard design procedures developed for single-sampled modulators are therefore directly applicable to the proposed double-sampled modulator, without incurring any instability and/or performance degradation.

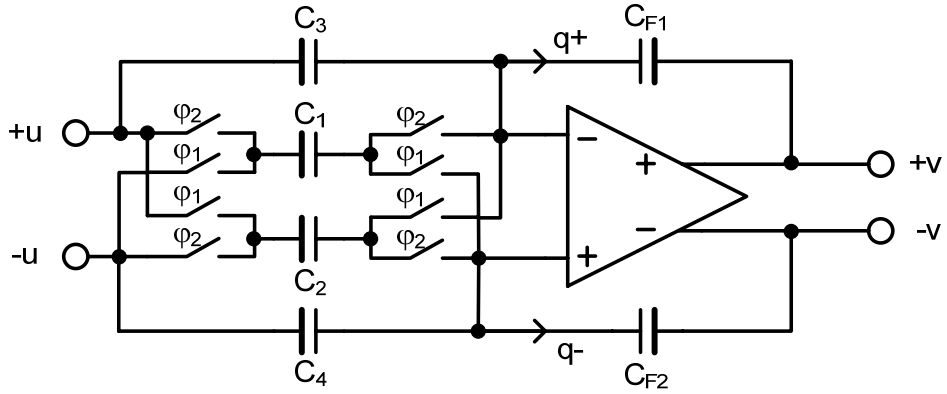

Figure 5.9: Proposed floating differential SC integrator.

5.3.1. The proposed fully-floating integrator

Fig. 5.9 shows the proposed floating integrator. Two unswitched capacitors C_3 and C_4 have been added to the integrator of Fig. 5.2, with the nominal values all equal to C. Analysis of the operation of the circuit when phase φ_2 rises shows that the charges q_i contributed to the feedback capacitors by the input capacitors C_i in the nth clock period are

$$q_1(n) = C_1[u(n) + u(n-1)] \tag{5.5}$$

$$q_2(n) = -C_2[u(n) + u(n-1)] \tag{5.6}$$

$$q_3(n) = C_3[u(n) - u(n-1)] \tag{5.7}$$

$$q_4(n) = -C_4[u(n) - u(n-1)] \tag{5.8}$$

The differential charge is hence

$$dq = q^+ - q^- = (q_1 + q_3) - (q_2 + q_4) \tag{5.9}$$

$$\therefore dq = (C_1 + C_2 + C_3 + C_4) \cdot u(n) + (C_1 + C_2 - C_3 - C_4) \cdot u(n-1) \tag{5.10}$$

Since dq remains the same during φ_1 and φ_2, there is no modulation of the differential signal. Ideally, the factor multiplying *u(n-1)* is zero. The only effect of capacitance mismatches is the introduction of an extra factor $(1+\delta \cdot z^{-1})$ into the transfer function, where δ is the relative capacitance error

$$\delta = \frac{C_1 + C_2 - C_3 - C_4}{C_1 + C_2 + C_3 + C_4} \tag{5.11}$$

Since $\delta << 1$ (typically around 0.001 or less for state-of-art CMOS processes), this extra factor has very little effect on the *SQNR*, unlike the $(1+z^{-1})/2$ factor introduced by the circuit of Fig. 5.2.

Analysis of the *CM* component $(q^+ + q^-)/2$ of the input charges reveals that it does contain a small alternating term proportional to the capacitance error $(C_1 - C_2)$. This causes folding of its spectral components around *fs/2* to the baseband. However, as before, the *CM* charge is rejected by the differential structure, and hence the *SQNR* remains unaffected.

An important aspect of the performance is that an opamp input offset V_{os} introduces only a constant offset $2CV_{os}$ into *dq*. Since this is independent of *u(n)*, it does not cause folding or harmonic distortion.

Comparison of the proposed stage with the Senderowicz integrator reveals that the total capacitance of the input branch is doubled in the new circuit. However, the integrator coefficient can be increased, and hence the value of the feedback capacitor reduced significantly. Also, by eliminating the extra pole in the signal and noise transfer functions, the design process as well as the circuitry of the complete modulator is vastly simplified.

5.3.2. The effect of the residual factor $(1+\delta z^{-1})$ on the loop stability

The shift of pole location due to capacitor mismatch in the double-sampled low-distortion modulator using the proposed fully-floating integrator in Fig. 5.10 can be visualized by sweeping δ from -0.1 to 0.1. As demonstrated in Fig. 5.11, the poles are located well within the unit circle, even with 10% capacitor mismatch. With typical capacitor mismatches of the order of 0.1%, all three poles remain very close to the origin, and the effects of the pole shifts are completely negligible. The *SQNR* improves by around 0.46 dB when $\delta = -0.1$ and degrades by 0.42 dB when $\delta = 0.1$. The same result was obtained for the second-order Boser-Wooley modulator in Fig. 5.12.

5.4. SIMULATION RESULTS

Extensive time-domain simulations of double-sampled modulators shown in Fig. 5.3 and Fig. 5.6 with conventional Senderowicz integrator and with proposed fully-floating integrator were performed using Matlab and Simulink. The modulator coefficients were $k = 0.5$, $m = 2.5$ for the circuit of Fig. 5.3, and $k = 0.5$, $m = 0.5$ for that of Fig. 5.6. The voltage- to-charge transfer function in the feedback path equaled

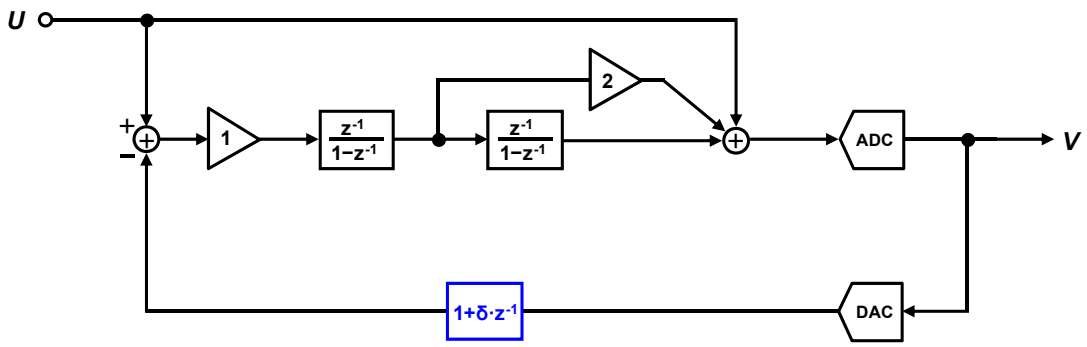

Figure 5.10: Second-order low distortion modulator [4] with the proposed fully-floating integrator.

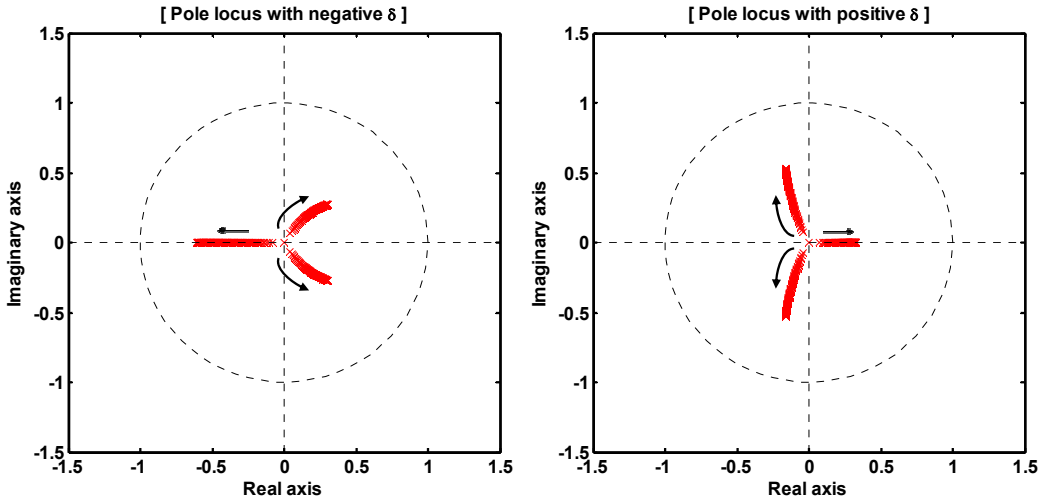

Figure 5.11: (a) Pole locus with δ = -0.1~0. (b) Pole locus with δ = 0~0.1 for the modulator shown in Fig. 5.10 (arrows indicate increasing $|\delta|$).

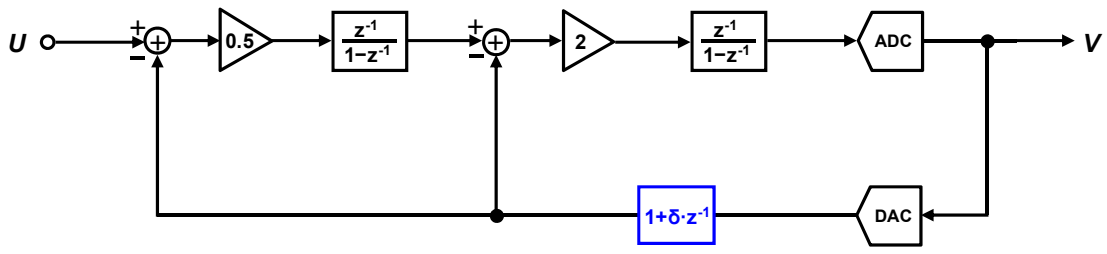

Figure 5.12: Second-order Boser-Wooley modulator [5] with the proposed fully-floating integrator.

$(1+z^{-1})/2$ for the Senderowicz floating integrator, and $(1+\delta \cdot z^{-1})$ for the proposed one. The effective *OSR* was 16, and 5-bit quantizer was assumed. Apart from DAC mismatch, ideal noiseless blocks were assumed. Fig. 5.13 shows the output spectra with a 0.1% mismatch between the DACs for the [2] circuit and the proposed one, with a -2 dB input. The latter shows a 6.3 dB *SNDR* improvement over the former, which is bigger than the 3 dB shown in Fig. 5.5. The spectrum of the circuit using the integrator of [2] also shows a peaking around 0.15*fs*, indicating marginal stability. Fig. 5.14 shows the output spectrum obtained under the same conditions for the modulator of Fig. 5.6. The *SNDR* performance difference was 6.9 dB.

It was found from extensive simulations with Matlab, Simulink, and Spectre that the proposed fully-floating double-sampling integrator can be used in a variety of ΔΣ ADC configurations without significant performance degradation in the presence of DAC mismatch.

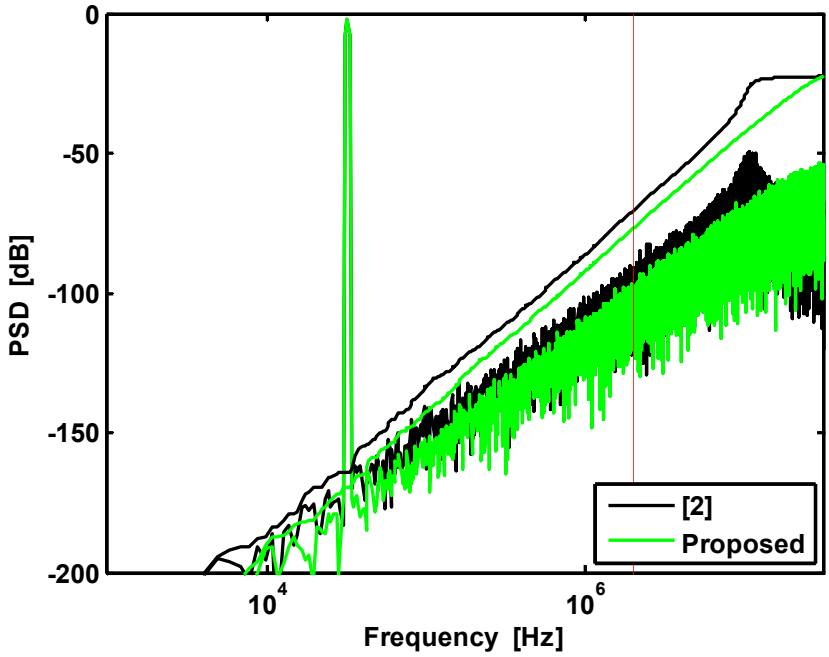

Figure 5.13: Simulated PSDs for double-sampled low distortion modulator in Fig. 5.3 with the conventional Senderowicz integrator (*SNDR* = 70.7 dB) and with the proposed fully-floating integrator (*SNDR* = 77.0 dB).

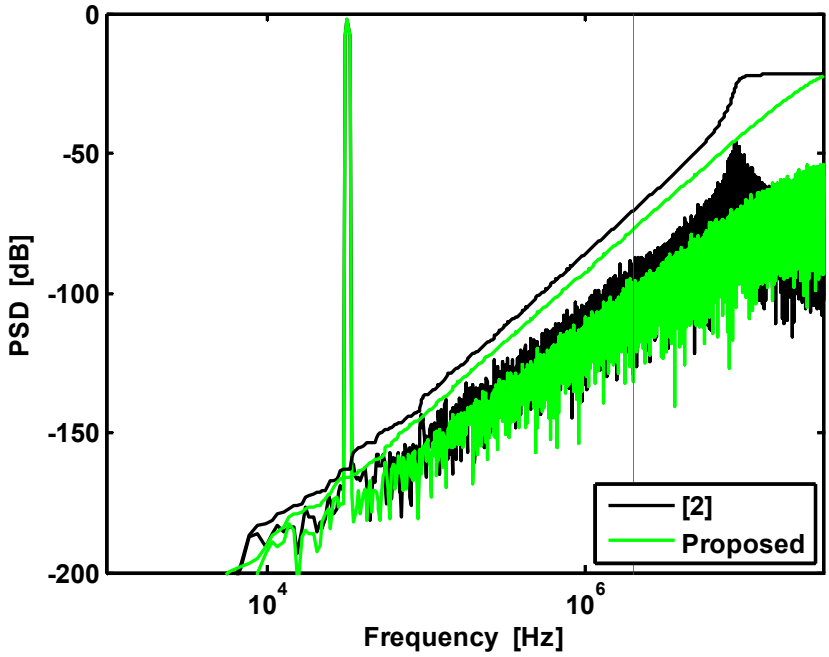

Figure 5.14: Simulated PSDs for double-sampled Boser-Wooley modulator in Fig. 5.6 with the conventional Senderowicz integrator (*SNDR* = 70.6 dB) and with the proposed fully-floating integrator (*SNDR* = 77.5 dB).

5.5. SUMMARY

A novel double-sampling integrator is proposed, which allows robust operation under path mismatch conditions, without introducing extra poles and zeros into the transfer functions. It allows the design of efficient double-sampling ΔΣ ADCs with optimum design methodology. The effectiveness of the proposed double-sampling integrator was verified with extensive simulations.

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CHAPTER 6. IMPROVED LOW-DISTORTION DELTA-SIGMA ADC

Abstract

Architectural considerations for ΔΣ modulator are critical to achieve wideband and low-power data conversion. The low-distortion single-loop ΔΣ modulator provides improved performance, and allows robust performance insensitive to circuit errors. However, it requires multiple signal summation at the input of the quantizer, and reduced processing time available for DAC linearization. It is also difficult to incorporate double-sampling in the low-distortion modulator. This chapter suggests an improved low-distortion modulator topology, derived by signal flow graph manipulations, to overcome these limitations.

6.1. INTRODUCTION

The ΔΣ ADC has been used widely for a variety of applications where high resolution at medium conversion speed is required. With increasing demand for high-resolution data conversion in a wider signal band and with lower power dissipation, there is a renewed interest in extending the bandwidth and reducing the power dissipation of ΔΣ ADCs while keeping their high resolution. The operation of ΔΣ ADCs relies on oversampling and noise shaping. The maximum sampling frequency is limited by the device f_T dictated by the given process technology, and by the permissible power dissipation. For a given sampling frequency, the oversampling ratio (OSR) is determined from the required signal bandwidth. Various wired and wireless applications in communication and consumer electronics today

require signal bandwidths ranging from below 20 kHz to over 20 MHz. The OSR for wideband ADCs is typically 8 to 24, much lower than that in traditional narrow-band applications. To achieve high resolution under low OSR condition, more aggressive noise shaping and multi-bit quantization should be applied [1]. However, the order of noise shaping in a single-loop modulator is limited by the signal swing inside the loop filter and the stability of modulator. Cascaded or multi-stage noise shaping (MASH) architecture can provide high-order noise shaping without sacrificing the modulator stability, and it also allows further improvement of the signal-to-quantization noise ratio (SQNR) setting the interstage gain to a value larger than one. But the performance of cascaded modulators is significantly degraded by quantization-noise leakage caused by the mismatch of noise transfer functions (NTF) of the analog and digital paths. This performance degradation can be reduced by making the analog NTF close to its ideal value, which is not power-efficient, or by including an adaptive digital filter to cancel the difference of analog and digital NTFs [2][3], which requires additional digital circuitry.

Multi-bit quantization increases the SQNR of a modulator by at least 6 dB for every additional bit, irrespective of modulator order and OSR. It also improves the stability of modulator and relaxes the required slew rate (SR) of loop filter. Typically, the maximum number of level for quantizer and feedback DAC is constrained by the exponential growth in the associated hardware and its power dissipation. This limits the quantizer resolution to about 4 to 5 bits in practical applications. This limitation can be relaxed by employing a two-step flash and redistributing the loop filter delay over the modulator loop [4][5]. Further SQNR improvement can be obtained by spreading the NTF zeros within the frequency band of interest, which is achieved by introducing resonators in the modulator loop. The SQNR improvement with optimized NTF zeros is significant when the order of

modulator is larger than two [1].

The low-distortion modulator topology [6][7] can provide several advantages over other architectures. By introducing a direct feedforward path from the input to the internal quantizer, unity signal transfer function (STF) is achieved, which enables the cancellation of an input signal at the input of loop filter. Since the loop filter processes the quantization noise only and not the signal, the signal swing at each internal node of the loop filter can be significantly reduced. Thus, the analog circuit requirements for the loop filter, such as opamp DC gain, UGBW, SR, and linearity, are greatly relaxed, and the harmonic distortion due to imperfections of the analog circuitry is considerably reduced. This results in large savings in power dissipation, and in robust performance insensitive to various circuit nonidealities. However, the low-distortion modulator topology introduces several critical issues: (1) additional signal summation is needed at the input of quantizer; (2) the signal processing time available for DAC linearization is reduced; (3) double sampling the input signal of the modulator becomes difficult, due to the stringent timing constraints. These issues should be addressed in wideband low-power applications. Reference [8] discussed some of these problems, and proposed architectural modifications to resolve issues (1) and (2). However, it is still not clear how to combine their solutions in a general high-order low-distortion modulator. It gives no solution for the introduction of double sampling.

In this chapter, an improved low-distortion single-loop ΔΣ modulator topology is proposed which solves the problems listed above. It will be shown how to derive this by transformations of the signal flow graph representing the system. In Section 6.2, prior solutions to mitigate the issues related with the realization of low-distortion modulator topologies are discussed and compared. An improved modulator architecture is proposed in Section 6.3, along with its detailed derivation. A summary

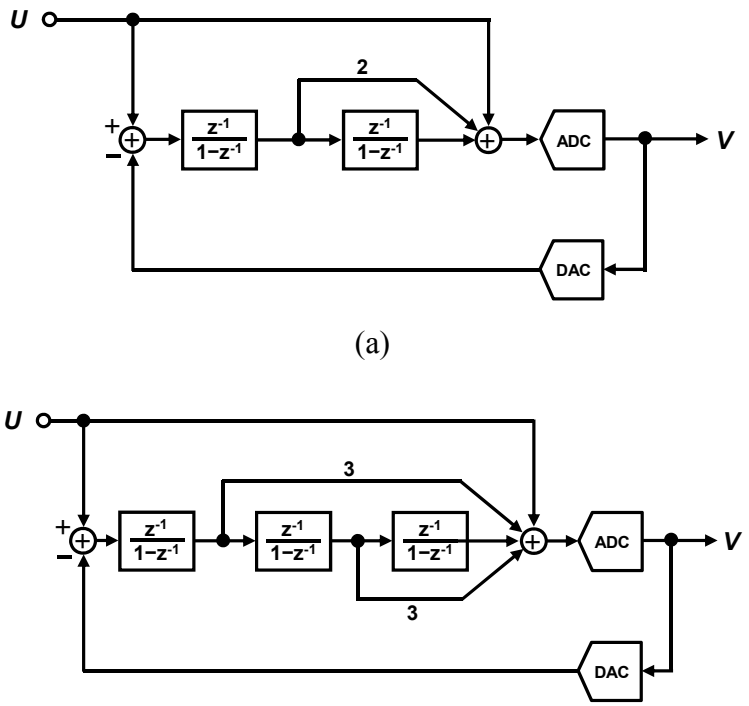


Figure 6.1: Traditional single loop low-distortion modulator topologies: (a) 2nd-order modulator; (b) 3rd-order modulator.

is given in Section 6.4.

6.2. PRIOR ART

The conventional low-distortion modulator requires additional signal summation at the input of quantizer, as illustrated in Fig. 6.1 for 2nd and 3rd order modulators. This can be performed with an active or passive adder. The active adder needs an extra opamp, which increases power consumption. Passive summation may be achieved using a capacitive adder, and it does not need additional active components. But this leads to reduced step size of the quantizer thresholds due to the signal attenuation caused by parasitics, and required increased power for the quantizer.

Furthermore, the extra signal summation requires an additional phase in a single-sampled modulator, so that the signal processing time for the linearization of multi-bit DAC must be reduced. Usually, DAC linearization is achieved by shaping the mismatch errors of the multi-bit DAC using dynamic element matching (DEM). Data weighted averaging (DWA) and its variants often require a barrel or logarithmic shifter, and their critical path delay should be smaller than the clock signal's non-overlapping time to avoid performance degradation.

Several techniques were proposed to resolve the issues associated with the implementation of low-distortion modulators. The first three techniques are mainly for the removal of the analog adder at the input of the quantizer; the last one is for the relaxation of DEM timing.

6.2.1. Capacitive input feedforward (CIF) path

The excess signal summation at the input of quantizer can be eliminated by taking the following two steps. The first step is to move all the signal paths except for the input feedforward path to the input of last integrator of loop filter H(z) [7]. Then, the input feedforward path to the input of quantizer can also be shifted to the same node through an unswitched capacitor. The resulting capacitive input feedforward (CIF) structure is shown in Fig. 6.2 [8]. All the signal summation is thus done at the input of last integrator instead of the quantizer input. The increased signal swing of last integrator will minimally affect the modulator performance, since the associated nonlinearity will be attenuated with the overall gain of the previous stage of loop filter. However, CIF does not relax the DEM timing, as illustrated in Fig. 6.3. Extension to double-sampled modulator with this topology is not available, due to the last delay-free integrator.

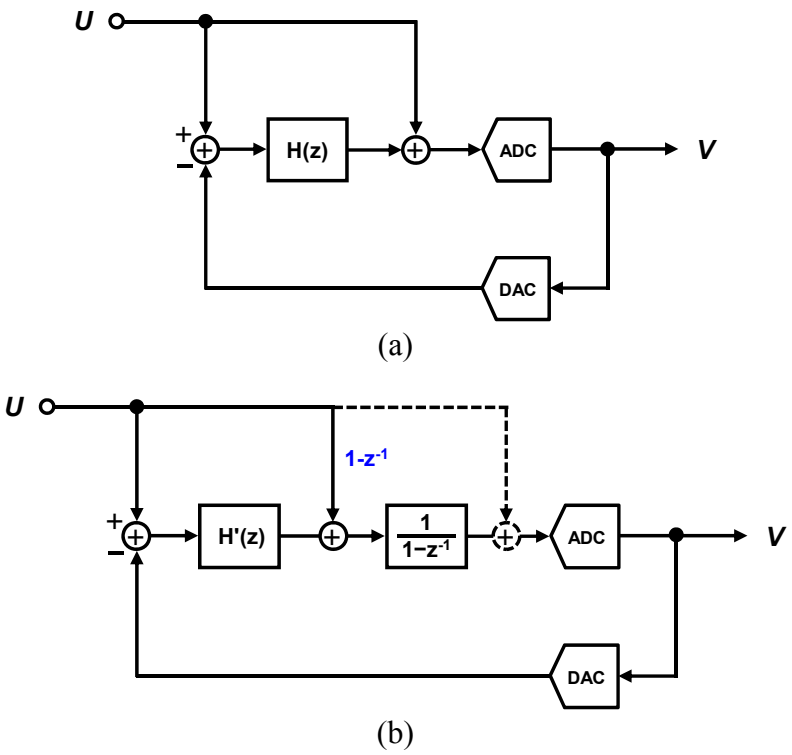


Figure 6.2: (a) Low-distortion modulator topology; (b) capacitive input feedforward (CIF) structure [8] using an unswitched capacitor branch to eliminate additional signal summation at the quantizer input.

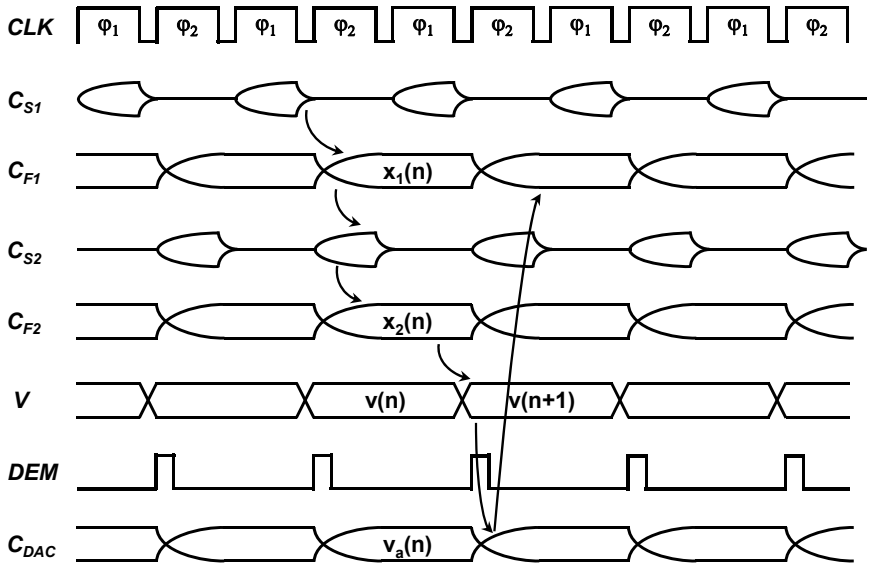
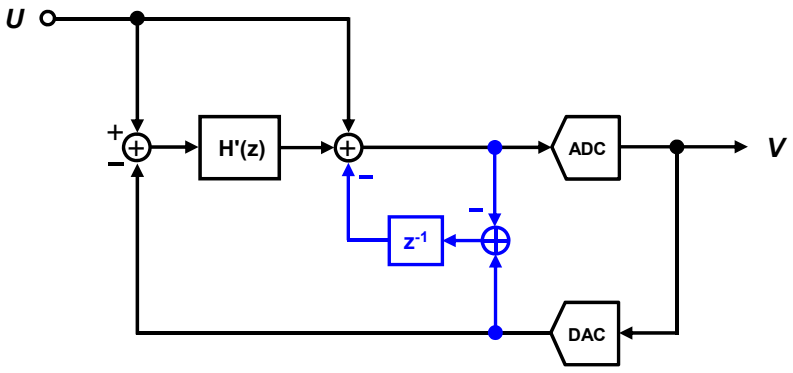
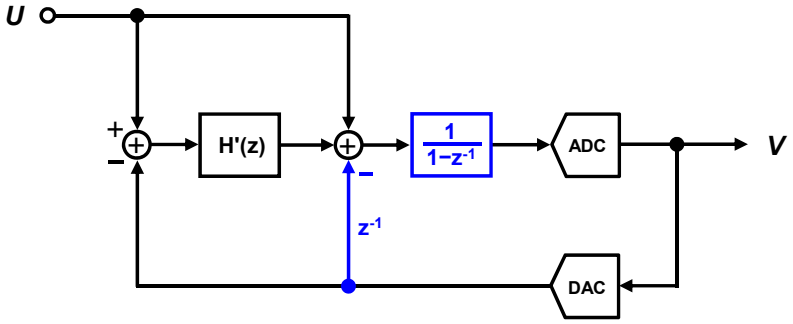


Figure 6.3: Timing diagram for a 2nd-order low-distortion modulator with CIF. For proper shaping of DAC mismatch errors, the DEM switching should be done within the nonoverlapping time interval of the clock phases.



(a)



(b)

Figure 6.4: (a) Quantization noise self-coupling (QNSC) [9] in a low-distortion modulator and (b) its equivalent topology.

6.2.2. Quantization noise self-coupling (QNSC) structure

The addition of signals at the quantizer input can also be avoided by applying a feedback of the quantization noise, as illustrated in Fig. 6.4 [9]. This is a general technique that is applicable to any modulator architecture. But QNSC is especially useful when it is applied to a traditional low-distortion modulator, since it does not need an additional opamp. QNSC increases the effective order of modulator, while keeping the advantage of low-distortion operation. However, like CIF, QNSC does not relax the DEM timing.

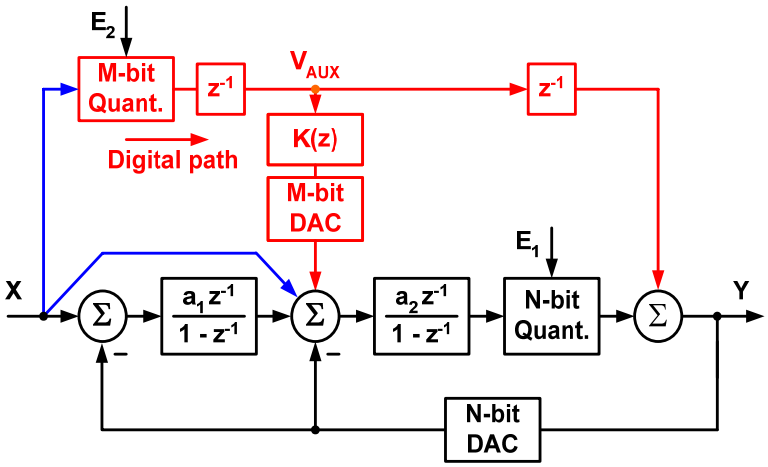


Figure 6.5: Digital feedforward (DFF) in a low-distortion modulator [10].

6.2.3. Digital feedforward (DFF) structure

The digital feedforward (DFF) architecture was proposed to remove the analog summer at the quantizer input [10][11]. The signal summation for input feedforward path is moved into the digital domain, by introducing an auxiliary quantizer, as shown in Fig. 6.5. The additional quantization noise injected into the auxiliary quantizer is cancelled by incorporating a simple digital filter and an extra DAC. However, the STF of this architecture is modified, and it peaks by several dBs outside of the signal band. This may boost out-of-band noise significantly.

6.2.4. Delay redistribution (DRC) structure

The DEM timing can be relaxed by applying DRD, as illustrated in Fig. 6.6 [8][12][13]. This slightly changes the STF from unity to z^{-1} while keeping the same NTF. The perfect cancellation of an input signal at the input of loop filter that makes the low-distortion architecture attractive is nevertheless preserved. This is achieved by including an extra delay in the input path to the loop filter, and by redistributing

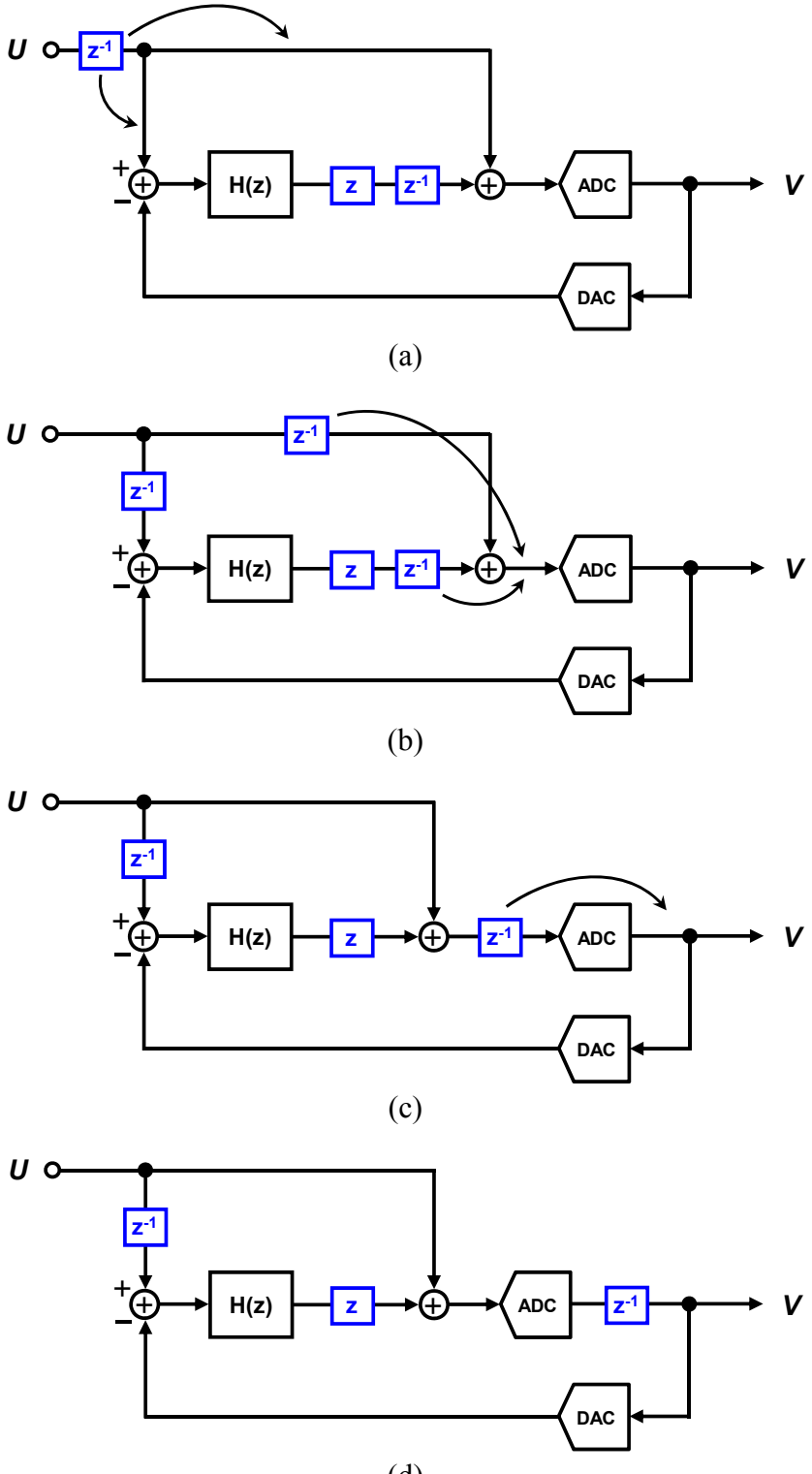


Figure 6.6: Delay redistribution (DRD) to relax DEM timing in a low-distortion modulator [8][12][13].

the delay of loop filter over the loop. But the redistribution of loop delay to accommodate DRD technique is not always feasible, and it usually results in the degradation of integrator settling and increased power dissipation. This technique does not affect the location of adder, which is still at the input of quantizer.

6.3. PROPOSED LOW-DISTORTION MODULATOR TOPOLOGY

The advantages of the improved low-distortion single-loop ΔΣ modulator topology proposed in this chapter are as follows:

(1) it retains the unity STF;

(2) it does not require an (active or passive) adder at the input of the quantizer;

(3) it allows relaxed DEM timing;

(4) it uses delaying integrators for fast settling and low power dissipation;

(5) it allows double-sampling without any architectural modification.

None of the techniques reviewed in the previous section satisfy all of these.

The proposed structures are obtained using flow-graph manipulations, which involves some previous techniques, as well as some new ones. One of key techniques applied to perform the flow-graph transformation is shown in Fig. 6.7, where the two modulator topologies are equivalent, if the value of coefficient k_2' is selected as shown in the Figure.

6.3.1. Second-order modulator

A 2^{nd}-order low-distortion cascade-of-integrators modulator with weighted feedforward summation (CIFF-LDM) topology is illustrated in Fig. 6.8 (a). It requires only one DAC. Several equivalent cascade-of-integrators modulators with

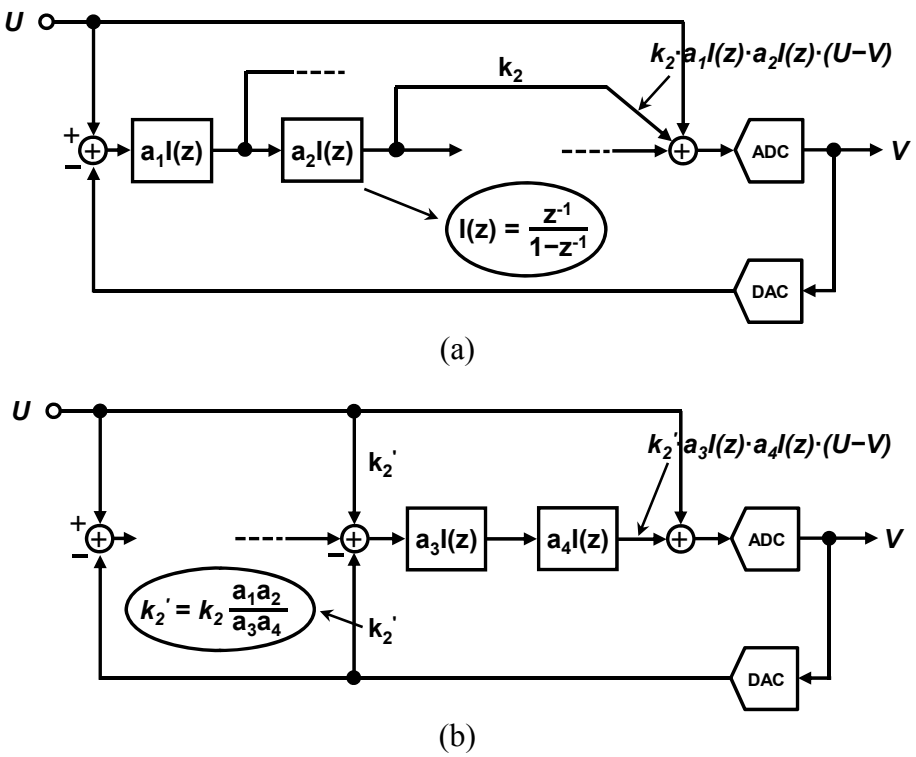
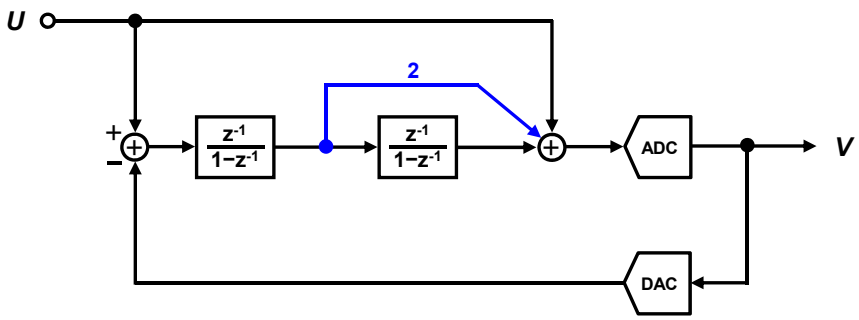
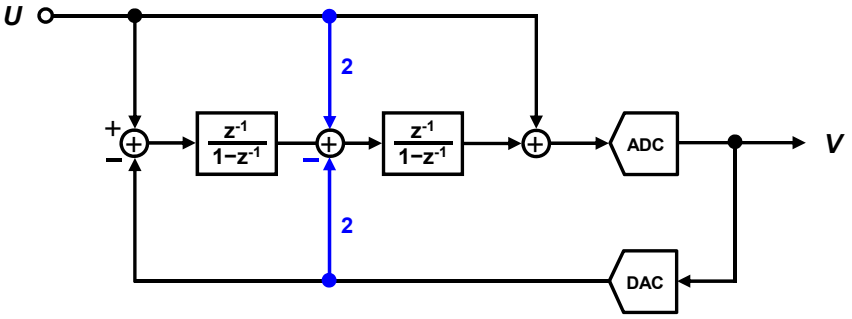


Figure 6.7: One of key architectural modification techniques to achieve improved low-distortion modulator topology.

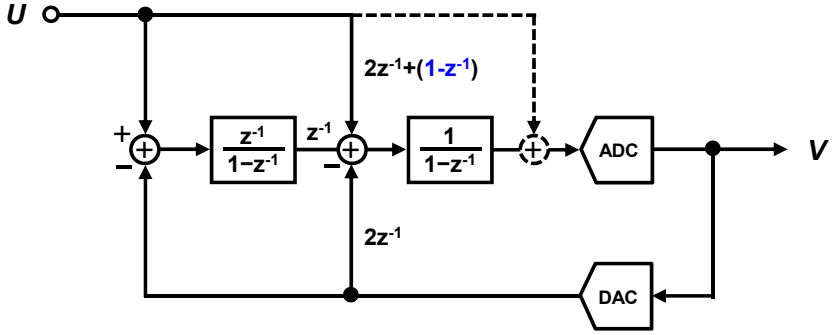
distributed feedback and low distortion (CIFB-LDM) that have two DACs can be derived successively from CIFF-LDM by using the transformation of its signal flow graph. The circuit of Fig. 6.8 (b) is obtained by applying the technique introduced in Fig. 6.7. It is observed that the paths with signal gains of 2 are equivalent since they contribute the delayed and first-order-shaped quantization noise to the input of quantizer. Fig. 6.8 (c) is derived from Fig. 6.8 (b) by applying the capacitive input forward (CIF) path to eliminate signal summation at the input of quantizer. To relax DEM timing, delay redistribution (DRD) is applied to Fig. 6.8 (c), which results in Fig. 6.8 (d). The single-sampled modulator with the topology of Fig. 6.8 (d) retains all the unity STF, but the signal summation is done at the input of 2nd integrator, which does not require additional active or passive adder. It also has relaxed DEM



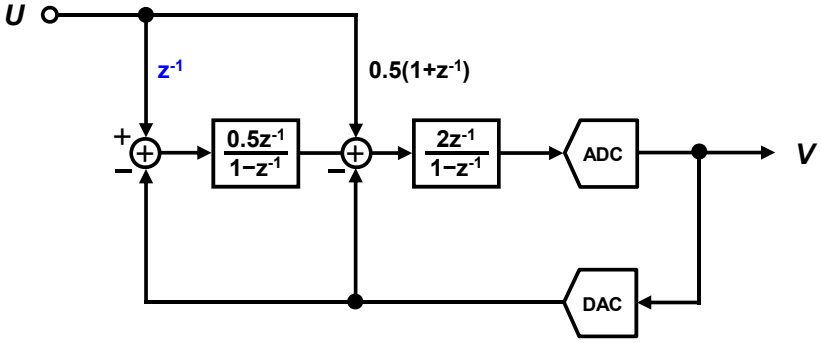
(a)



(b)



(c)



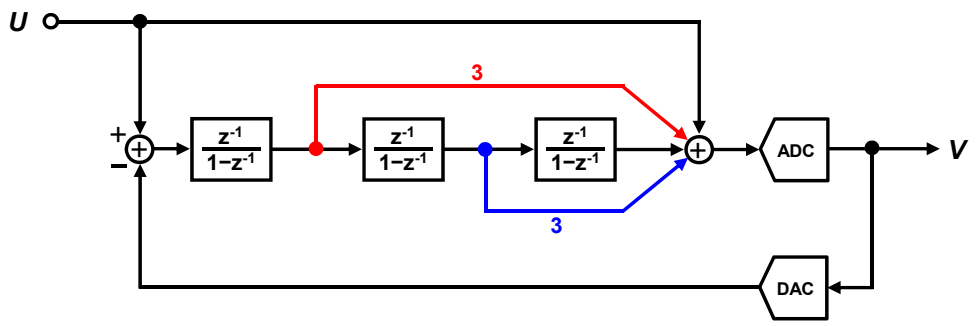
(d)

Figure 6.8: Steps to get the improved second-order low-distortion modulator based on equivalent transformation of its signal flow graph.

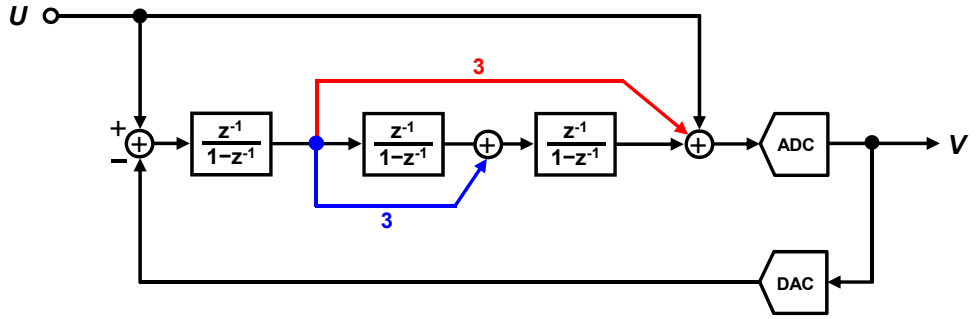
timing, due to the delayed integrators. This structure is especially useful when it is used as a double-sampled modulator. It allows a direct implementation of a double-sampled modulator without any further architectural changes. In this case, the delay z^{-1} at the input can be realized by using two SC sampling branches in a push-pull mode, as is common in a double-sampled input path. The $0.5(1+z^{-1})$ term is also easily implemented by applying Senderowicz's fully-floating integrator [14]. The feedback DAC path for a double-sampled modulator can be effectively realized with the structure proposed in [15][16]. This does not introduce extra poles into the loop gain of modulator, and allows the same design parameters and design procedure as applied to a single-sampled modulator. Thus, it greatly simplifies the design of a double-sampled modulator. Note that the structure of Fig. 6.8 (c) is not suitable for a double-sampling modulator due to stringent timing requirement for the second integrator and the quantizer. The DEM timing becomes tight again in Fig. 6.8 (d) when it implements a double-sampled modulator. This may make it necessary to use foreground or background DAC error calibration techniques [17][18] instead of DEM technique. For the capacitive DACs common in SC circuit realization, a simple foreground calibration during power-up may be adequate, since the time drift of DAC errors is usually negligible.

6.3.2. Third-order modulator

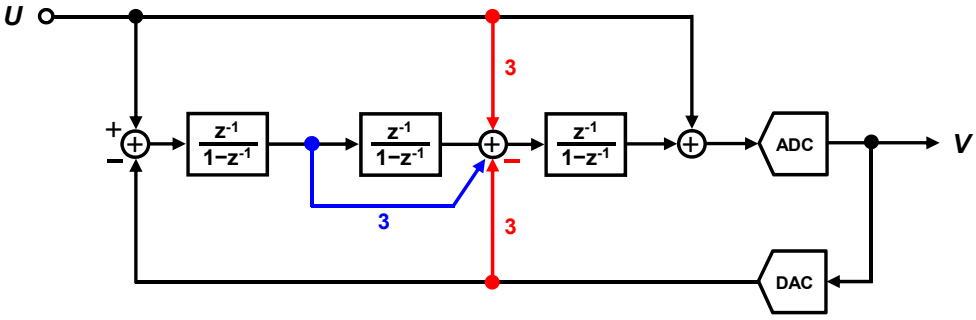
The proposed efficient 3rd-order low-distortion modulator topology can be derived by transforming the CIFF-LDM structure using the design techniques described earlier. The 3rd-order CIFF-LDM topology is illustrated in Fig. 6.9 (a). The structure of Fig. 6.9 (b) is obtained by replacing the upper feedforward path inside the loop filter. Then, Fig. 6.9 (c) results from the transformation used earlier in Fig. 6.8 (b).



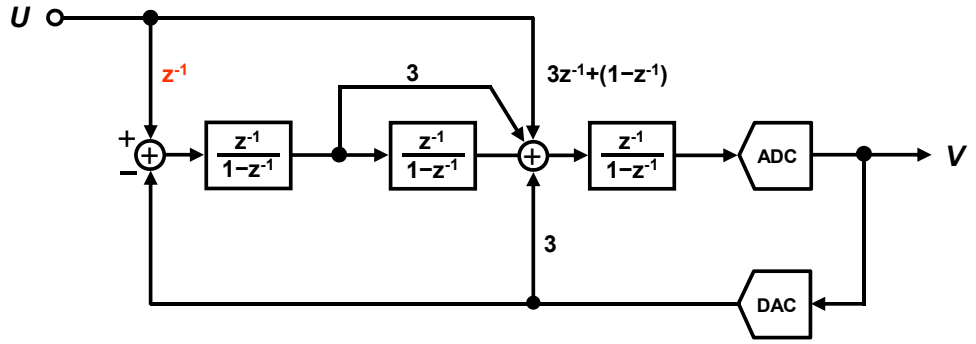
(a)



(b)



(c)



(d)

Figure 6.9: Steps to get the improved third-order low-distortion modulator structure using equivalent transformations of its signal flow graph.

Finally, Fig. 6.9 (d) is achieved by applying CIF and DRD. Compared with Fig. 6.9 (a) [8], it has relaxed DEM timing for a single-sampled modulator and is immediately extendable to double-sampled modulator.

6.3.3. Higher-order modulators

By performing the same transformations as described for 2^{nd}-order and 3^{rd}-order modulators, improved low-distortion structures can be achieved for higher-order loops. Examples for 4^{th}-order and 5^{th}-order modulators are shown in Fig. 6.10 and 6.11, respectively.

The signal swing in a single-loop modulator is an important design consideration for its stable operation. The signal swing inside the loop filter for a low-distortion modulator is reduced significantly by bypassing an input signal outside the loop filter so that the loop filter processes quantization noise only. But the summing node includes both quantization noise and an input signal and its swing should be controlled not to cause excessive quantizer overload to avoid performance degradation. The summing node has been moved into the input of the last integrator for the proposed modulator and its increased swing can lead to reduced modulator linearity and reduced maximum input signal amplitude. This problem can be prevented by taking quantizer resolution to be greater than or equal to modulator order plus one. So, the quantizer resolution of the single-loop modulator should be increased by at least one bit whenever its order increases by one. This makes sense readily by considering the worst-case signal swing of the summing node in a traditional CIFF low-distortion modulator. For an Nth-order conventional low-distortion modulator with an M-bit quantizer, the worst-case maximum signal swing of the modulator that the summing node experiences can be expressed as follows

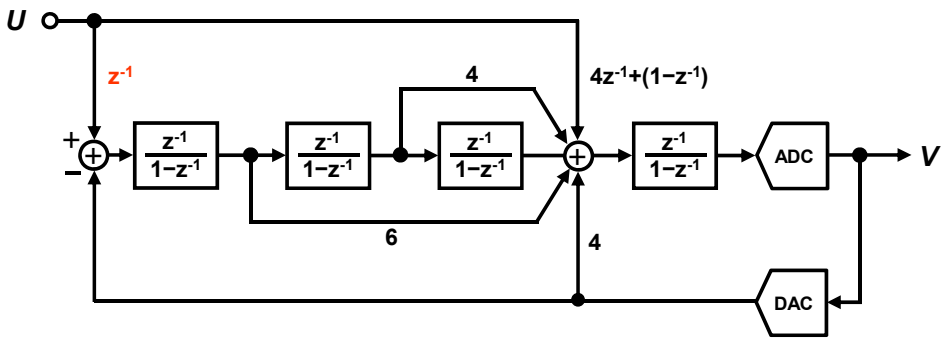


Figure 6.10: Proposed improved fourth-order low-distortion modulator.

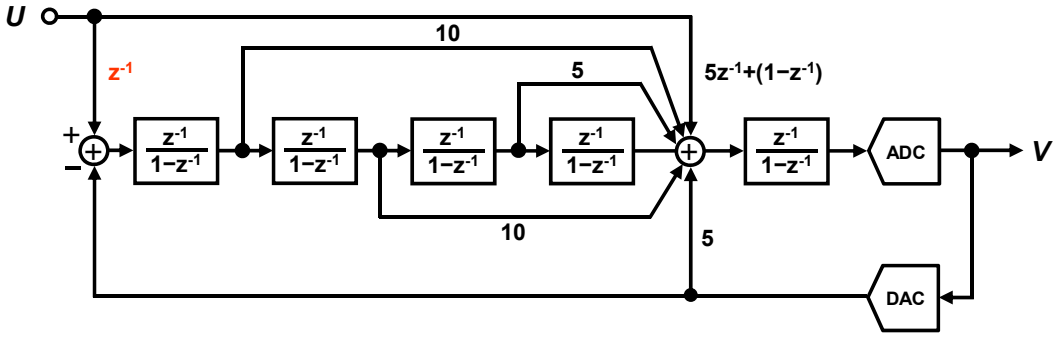


Figure 6.11: Proposed improved fifth-order low-distortion modulator.

$$S_{\max} = (2^N - 1) \cdot \Delta_q \tag{6.1}$$

excluding an input signal. Here, Δ_q is a quantizer step size that can be expressed as the following equation,

$$\Delta_q = \left| V_{thq}^{+} - V_{thq}^{-} \right| / 2^M \tag{6.2}$$

where V_{thq}^{+} and V_{thq}^{-} are positive and negative reference voltage for resistor string to generate the quantizer thresholds, respectively. Complete decorrelation is assumed among shaped or delayed quantization noises in the derivation, which is over-estimation. Therefore,

$$S_{\max} = (2^N - 1) / 2^M \cdot \left| V_{thq}^{+} - V_{thq}^{-} \right| \tag{6.3}$$

results and it clearly shows that the signal swing and stability of the low-distortion single-loop modulator can be preserved by selecting its quantizer resolution appropriately according to its modulator order when the same input signal condition is kept.

The performance improvement with zero optimization begins to be significant when the modulator order is greater than or equal to three. The introduced resonator for this does not shift the original pole location of the single-loop modulator significantly. So, the zero optimization can be accomplished almost independently while keeping the original modulator coefficients and it requires only extra small capacitors and switches. Resonator can be formed with a backend integrator pair so that the associated thermal noise with the small capacitors does not dominate the overall noise budget.

6.4. SUMMARY

An improved low-distortion single-loop ΔΣ modulator topology was proposed. It retains all the advantages of traditional CIFF-LDM, but it does not require signal summation at the quantizer input, so that no additional adder is needed. When it is used as a single-sampled modulator, it allows relaxed DEM timing. Since it uses only delayed integrators, it can be extended easily to double-sampled modulator. Combined with the techniques introduced in [15][16], it can provide improved performance with a low OSR, and relaxes the circuit requirements for the modulator loop filter. The speed limitations due to DEM timing in a double-sampled modulator can be overcome by using efficient circuit design and advanced technology, which may enable DEM signal processing between clock phases. Alternatively, DAC calibration techniques may replace DEM, thus eliminating the related timing issues.

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CHAPTER 7. CONCLUSIONS

There is increasing demand for high efficiency delta-sigma modulation data converters in a variety of applications, such as wired and wireless communication, instrumentation, medical and automotive electronics as well as consumer electronics. Large SNR over the signal band, along with excellent linearity and wide dynamic range, should be provided in a power-efficient manner for these data converters. It is also important to extend the signal bandwidth for these data converters substantially without performance degradation to accommodate fast-growing recent wideband applications. Architectural innovations, together with efficient circuit design, are required to accomplish the design goals and to meet various stringent design specifications. In this dissertation, several enabling design techniques to improve the efficiency of delta-sigma modulation data converters were introduced, and the effectiveness of the proposed techniques was verified by experiments with state-of-the-art prototype designs.

In Chapter 2, a low-voltage dual-channel audio delta-sigma modulation DAC was presented. It is the first sub-1V audio DAC with on-chip headphone driver. It incorporates a novel digital interpolation filter and delta-sigma modulator. By employing a cascaded half-band interpolation filter and a feedforward delta-sigma modulator, and by introducing time-interleaving operation between both channels for all digital paths, considerable amount of hardware was saved. The prototype ICs, implemented in a 0.35μm CMOS process, achieved 88 dB dynamic range, while consuming 2.6 mW from a 0.8 V supply for the dual channels.

In Chapter 3, two novel architectures were proposed for delta-sigma ADCs. The multi-cell structure allows flexible trade-off between resolution and power

dissipation by controlling the number of activated modulator cells according to the application. It is also the architecture of choice in applications where robustness and programmability are critical. The cellular approach does not increase area and power dissipation compared with the conventional approach. In the other proposed architecture, the performance of delta-sigma ADC was significantly improved by coupling the quantization noises among different modulator loops or within each loop. Noise coupling raises the effective order of the noise transfer function without introducing stability issues, and improves the linearity of the modulator. It is robust to analog circuit errors, unlike the cascaded modulator. Measured results with three prototype ADCs based on proposed architecture showed outstanding linearity and good figure-of-merit.

In Chapter 4, a wideband high-linearity delta-sigma ADC was described. The noise coupling introduced in Chapter 3 was combined with time interleaving. This provides a further improvement of SQNR by 6 dB, in addition to the 13 dB improvement obtained with noise coupling. Two versions of a two-channel time-interleaved noise-coupled delta-sigma ADC were realized in a 0.18μm CMOS technology. Noise coupling between the channels increased the effective order of the noise-shaping loops, provided dithering, and prevented tone generation in all loops. Time interleaving enhanced the effects of noise coupling. Using a 1.5 V supply, the device achieved excellent linearity (SFDR > 100 dB, THD = -98 dB) and an SNDR of 79 dB in a 4.2 MHz signal band.

In Chapter 5, a novel double-sampling technique was proposed. It allows robust operation under path mismatch conditions, without introducing extra poles and zeros into the transfer functions. It permits the design of efficient double-sampling delta-sigma ADCs with optimum design methodology. The effectiveness of the proposed double-sampling technique was verified with extensive simulations.

In Chapter 6, an improved low-distortion single-loop delta-sigma modulator topology was proposed. It retains all the advantages of traditional low-distortion topology, but it does not require signal summation at the quantizer input, so that no additional adder is needed. When it is used as a single-sampled modulator, it allows relaxed timing for dynamic element matching to linearize multi-bit DAC. Since it uses only delayed integrators, it can be extended easily to double-sampled modulators. Combined with the techniques introduced in Chapter 5, it can provide improved performance with a low OSR, and relaxes the circuit requirements for the modulator loop filter.