# AN ABSTRACT OF THE DISSERTATION OF

Jason Russell Muhlestein for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on June 14, 2017.

Title: Next Generation Analog-to-Digital Conversion Using Time-based Encoding and Digital Synthesis Techniques

Abstract approved: _____

Un-Ku Moon

The internet-of-things is a growing market segment which is based on an array of portable communication devices with high power efficiency. Advanced semiconductor technology can easily improve their digital performance, but the same cannot be said for the analog blocks which are vital to their operation. High performance analog circuits continue to use conventional design techniques and architectures at the expense of power efficiency. Deeply scaled CMOS exaggerates this trade-off, opening the door for novel system techniques that take advantage of the digital nature of sub-micron transistors. This research focuses on two highly digital ADCs which can mitigate the short channel effects of limited output swing and low intrinsic gain while also benefiting from process scaling.

First, a multi-domain ADC is used to perform quantization on both voltage and time domain signals, relaxing the power-performance trade-off. This hybrid

approach can lead to a high resolution, high efficiency data converter in scaled process. A prototype ADC was fabricated in 180nm CMOS, showing an SNDR of 73 dB, operating at 20 MHz sampling frequency, with a power consumption of 1.28 mW.

Next, an automated synthesis process is used to automatically generate a high speed VCO-based quantizer from verilog code. Stochastic spatial averaging is combined with a high speed open-loop noise-shaping quantizer to provide enhanced resolution in the presence of device mismatch. Simulation results of a prototype ADC in 180nm CMOS shows an SNDR of 49 dB, operating at 800 MHz sampling frequency and 50 MHz signal bandwidth.

# Next Generation Analog-to-Digital Conversion Using Time-based Encoding and Digital Synthesis Techniques

by

Jason Russell Muhlestein

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APPROVED:

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Major Professor, representing Electrical and Computer Engineering

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Jason Russell Muhlestein, Author

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*For my brothers,*

*Rusten and Ryan*

# Chapter 1: Introduction

> "The objective of doing the research, is not to solve some specific problem ... Its to learn how to go on an intellectual adventure. The whole idea is to have fun."
>
> — *Al Oppenheim*

Most people have no idea of the power they hold in their hands on a daily basis. That new smart phone is so much more than the screen and battery and speakers you may be familiar with. Over the past decade, we have seen cell phones emerge from being a portable telephone extension into sophisticated miniature computers with continuous network connectivity. In terms speed and complexity, any modern smart-phone can out-pace the Apollo Guidance Computer used by NASA to put a man on the moon [1]. In order to appreciate the computational power in your pocket, it is necessary to first look back over the history of modern electronics.

## 1.1 History of the Integrated Circuit

The device that started the modern age of electronics was the transistor, first constructed in 1947 at AT&Ts Bell Labs by John Bardeen, Walter Brattain and William Shockley [2].

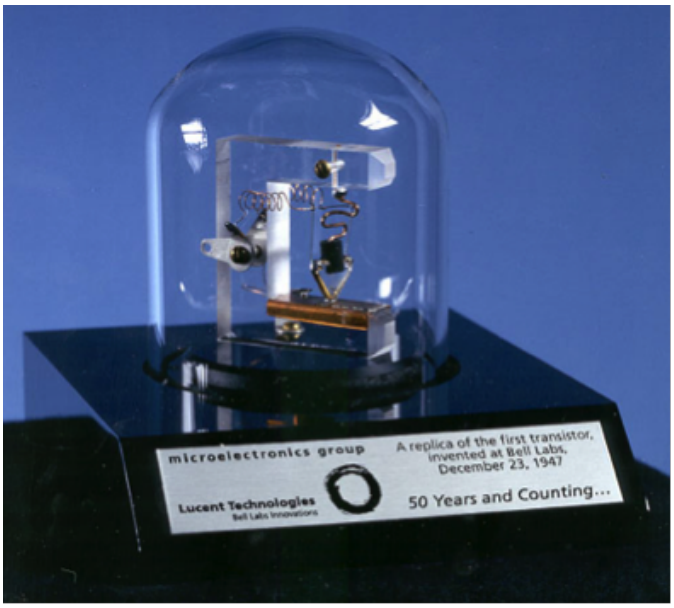


Figure 1.1: A replica of the first transistor ever created by William Shockley.

The phenomenon they observed was that when two gold contacts were placed close together on a germanium substrate, an input signal could be amplified, creating the first point-contact transistor. This breakthrough allowed advances in communications applications because now a signal could be sent across larger distances without using the larger, more expensive vacuum tubes. This achievement was large enough to warrant earning its creators a Nobel Prize in Physics in 1956 [3].

A replica of the original transistor is shown in Figure 1.1. Although huge by todays standards, the first 0.5 inch high transistor was able to consume less power, and switch much faster than the existing vacuum tubes due to its smaller size. At this point, semiconductor manufacturers began to push the limits of small in terms of electronics. Up until now, every circuit was built with discrete components that

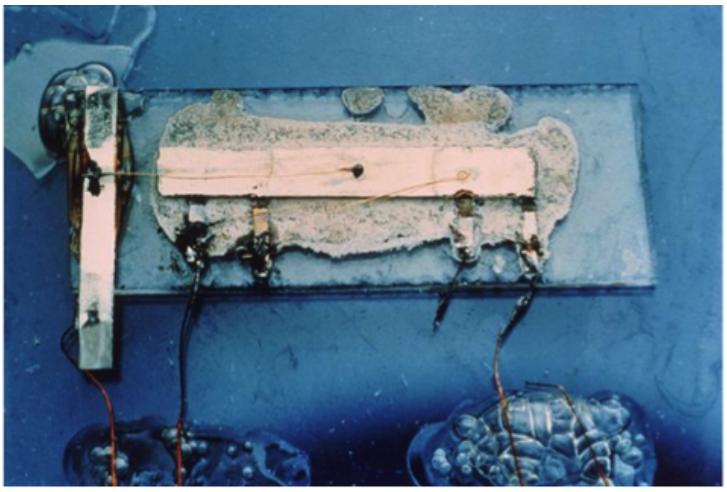

Figure 1.2: The first solid-state integrated circuit.

would be soldered together by hand. This approach resulted in bulky and hot electronics that were unreliable and expensive.

Circuit fabrication changed when Jack Kilby invented the integrated circuit (IC) at Texas Instruments in 1958. Figure 1.2 shows a photo of this invention. This revolutionary new technique allowed multiple circuit devices to be synthesized on a single monolithic substrate made of germanium. Several months later, Robert Noyce developed a silicon based IC which utilized p-n junction isolation to allow each device to work independently. This miniaturization of electronics led to rapid improvements in computational ability, greatly accelerating electronic circuit capabilities.

The relentless shrinking of circuit component dimensions is known today as Moores Law, named for Intel Engineer and co-founder Gordon Moore. In 1965, Moore noted that in order to remain competitive, a semiconductor company would

need to double the number of transistors on an IC every two years [4]. Although this prediction was made after less than 5 years of data, the trend has persisted to this day, spanning over 50 years. While this could be a self-fulfilling prophecy, the competitive benchmark Moore laid out has driven the evolution of nearly every electronic device you have ever used.

By the year 1971, the first-generation Intel 4004 processor contained 2,300 10 $\mu$m transistors, running at a speed of 740,000 Hz (740 kHz). Fast forward to a modern technology, and the evidence of Moores law is staggering. Figure 1.3 shows the 10-core Intel i7 Broadwell-E, which now contains 3.2 billion 14 nm transistors running at over 3,600,000,000 Hz (3.6 GHz). To give a general idea of the scale of these transistors, 14nm is roughly 30 silicon atoms wide. The end of Moores law device scaling is predicted to end every several years, only to be thwarted by ingenious new fabrication and development techniques. Some predictions indicate that the number of transistors on a single chip could approach 100 Billion, the number of neurons in an average human brain, by the year 2026 [5].

While it can be difficult to know exactly where the technology will take us, several assumptions will be made for the remainder of this dissertation. First, that while transistor geometry may not continue to scale, the intrinsic speed and power efficiency of these devices will continue to improve. This assumption is primarily based on the economic incentive of IC companies to produce high efficiency designs. The second assumption is that despite the prevalence of digital signal processing, analog signals are inevitable in the real world. Processing these signals through conventional analog blocks or data converters is therefore a necessary requirement

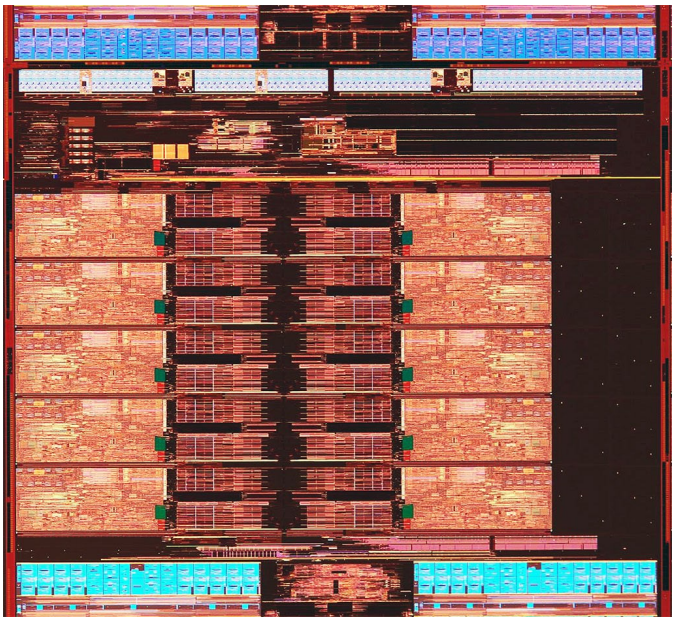

Figure 1.3: Die photo of the 10-core Intel i7 Broadwell-E.

for next generation systems.

## 1.2 Modern Electronic Systems

Some modern smart electronic devices that may be familiar to the reader are shown in Figure 1.4. In most cases, the identifier smart indicates the ability of a device to connect to the internet. These include items like a wrist watch, laptop computer, cellphone, tablet, and even the car you drive. These devices must incorporate a large array of communications systems and protocols. Some of the systems integrated into these products include a processor, baseband modem, RF transceiver, power management ICs, microphones, flash memory, cameras, touch screen controller, NFC Controller, Wi-Fi, GPS, Audio ICs and miscellaneous ICs

Figure 1.4: Modern portable electronics surround us on a daily basis.

for other sensors and a battery.

Monitoring these various systems is a vital task to optimize the operation and battery life of these devices. One primary component used for this purpose is known as the Analog-to-Digital converter (ADC). The operation and background of the ADC is described in the next section.

## 1.3 Analog-to-Digital Converters

Electrical engineering and computer science is the study of electronic hardware and the coded instructions given to those electronic circuits. This symbiotic relationship works mainly because of the digital abstraction used by every computer ever created. In this binary language, everything is represented with either a 0 or a 1. A storage slot holds one of these values, and is known as a bit. While it is very simple to make one computer communicate with another, it is much more challenging for a human to spout off a command in raw binary. It is desirable for a computer to interpret the world around us so it can monitor physical quantities

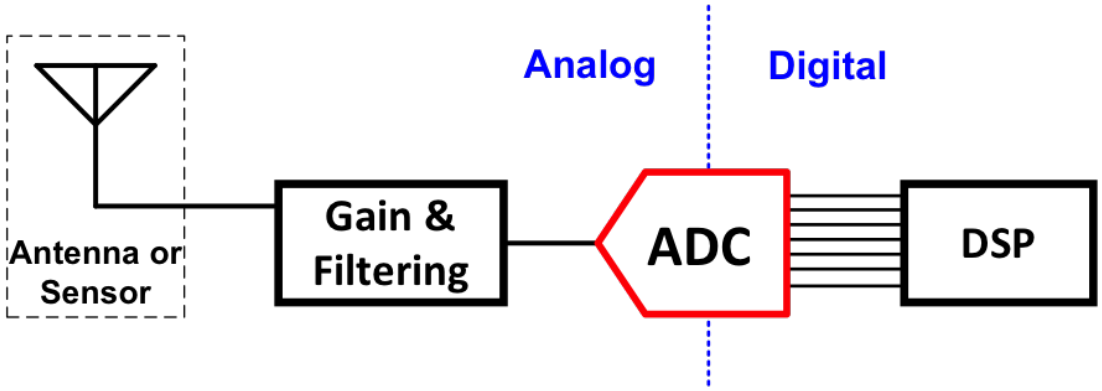


Figure 1.5: Signal path for a standard receiver architecture showing the ADC as the interface between analog and digital domains.

like speed, direction, sound level, and temperature through electrical parameters like voltage, current or charge.

In order for the complex interplay between hardware and software to be possible, a vital connection must be made which can translate something we understand into that which an algorithmic machine can process. The device that performs this translation is the ADC. Figure 1.5 shows a conventional receiver interface and how the ADC is incorporated. The input signal is first picked up by an antenna or sensor of interest. Next the signal is conditioned through the use of low-noise amplifiers, filters, and mixing to a baseband frequency to allow the ADC to convert the continuous input to a discrete output.

Data converters are ubiquitous blocks in a modern system-on-chip (SOC). A rapidly growing trend is the prevalence of digital systems replacing analog blocks. In order to process inputs from radio and sensor interfaces, there is a need for an ADC to generate the binary code word to the Digital Signal Processing (DSP)

engine with a high signal bandwidth and low latency.

## 1.4 Analog Scaling

As digital systems dominate the silicon area and design resources, it is obvious that the CMOS technology will be further modified to reduce their cost and increase their power efficiency. While this is advantageous from a system and financial perspective, it also creates an interesting challenge for analog and mixed-signal design engineers. As the process scales, the transistors intrinsic gain is reduced along with the maximum supply voltage.

Figure 1.6 shows a schematic simulation of the effect of short channel transistors on intrinsic gain. With longer channel lengths, the output impedance is higher, resulting in large intrinsic gain. With the longer length comes increased parasitic capacitance, resulting in lower operating speeds. Alternatively, the shorter channel lengths can operate at higher speed, but at the same time experiencing degraded intrinsic gain due to the lower output impedance.

Another trend noted from scaling CMOS process is the limited signal headroom, which is shown graphically in Figure 1.7. As devices are made smaller and thinner, the maximum applied voltage must also reduced to guarantee their reliability and prevent premature aging effects. This can benefit digital circuits because they now have a smaller voltage swing to change state. Analog circuits conventionally require some finite threshold voltage range below the supply voltage and above the ground voltage which is required to bias an NMOS or PMOS transistor in

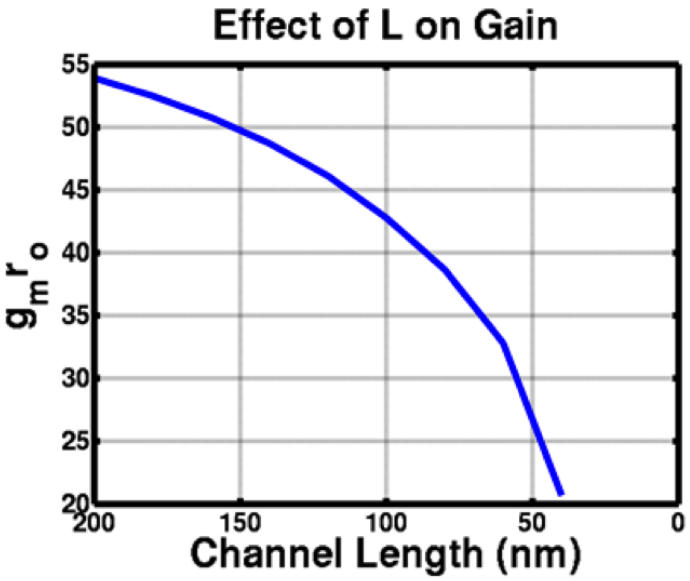


Figure 1.6: Effect of reducing channel length for transistor intrinsic gain.

its active region of operation. As process scales and the supply is reduced, the threshold voltage is not reducing at the same rate as the supply itself, resulting in less linear swing for signals.

The quest of an analog circuit designer is to manage various trade offs between noise, matching, linearity, and speed. To address the challenges presented by a digitally-focused CMOS process technology, a designer can implement architectural changes that are more friendly to process scaling. Intuitively, if CMOS technology is designed to favor digital applications, future-ready analog designs can transition to more digital system techniques and tools. The remainder of this dissertation will explore different circuit techniques which attempt to provide analog solutions that take advantage of the digital nature of future CMOS transistor technology.

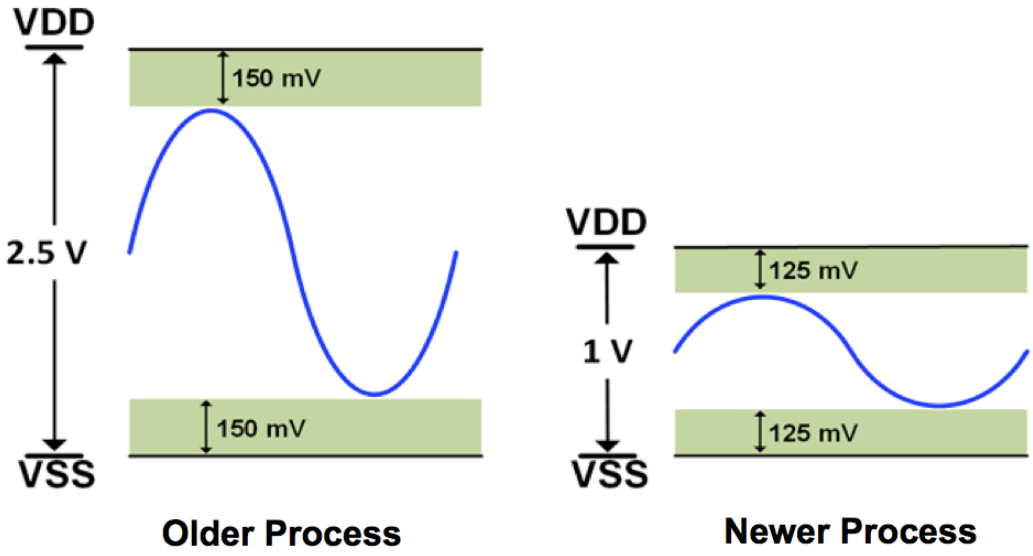


Figure 1.7: Effect of reducing supply voltage from one process to the next.

A comprehensive literature review is provided in Chapter 2, where highly digital time-based techniques attempt to solve the scaling dilemma. Chapter 3 discusses the theory, implementation, and measurement of a hybrid voltage and time domain ADC used for low power, high resolution applications. Power efficiency is achieved by splitting the quantization effort into a SAR-TDC configuration and using a highly linear voltage-to-time residue amplifier. Next, Chapter 4 presents a way to automate the creation of a moderate resolution, wide bandwidth ADC. The implementation and simulated performance of the spatially averaged stochastic ADC using voltage-controlled-oscillator based quantizers is discussed. This second project shows the feasibility of using a highly digital time-based ADC within existing digital design tools to provide rapid development of an ADC. Chapter 5 offers suggestions for future work in highly digital and time based data converters.

Chapter 6 will summarize the dissertation.

# Chapter 2: Digital Design Techniques using Time

> "If I have seen further, it is by standing on the shoulders of giants."
>
> — *Isaac Newton*

Incorporating mixed signal systems on a single die requires significant effort to maintain analog performance at smaller process nodes. This performance comes at the cost of larger area, increased power consumption, and high design complexity [6, 7].

Instead of processing quantities of voltage or charge, interest has been generated surrounding signal processing techniques which contain analog signals in the delay between two clock edges [8, 9]. By using clock edges to represent the input, data converters can harness digital CMOS characteristics of noise immunity, speed, and power to efficiently process analog signals, rather than be limited by them. Time information can also be used to supplement conventional ADC techniques to provide benefits in terms of area [10], power [11, 12], and offset correction [13].

The rest of this chapter is organized as follows: Section 2.1 introduces time domain signal processing. Section 2.2 reviews Time-to-Digital converters (TDC) and describes techniques to improve their resolution and input range. Section 2.3 explores ADC techniques which utilize time information to enhance their perfor-

mance. Section 2.4 provides a chapter summary and conclusion.

## 2.1 Time Utilization Concepts

A voltage domain ADC quantizes an input signal which is often represented by a voltage potential. The minimum detectable change in the input is:

$$V_{LSB} = \frac{V_{MAX}}{2^N} \tag{2.1}$$

where N is the bit resolution. As CMOS scales down, thinner gate oxides require a reduction in the supply voltage to ensure circuit reliability. Low supply voltages reduce ADC input range while the thermal noise power remains constant. This reduction in Signal-to-Noise Ratio (SNR) can be improved with larger capacitors, but results in poor energy efficiency and can quickly eliminate the area savings of using more advanced process technology. The left side of Figure 2.1 shows how thermal noise added to a signal directly impacts the minimum voltage resolution, a problem which becomes more evident at lower supply voltages. For a given resolution, a reduction of the maximum voltage to $V_{MAX2}$ will reduce the quantization voltage $V_{LSB2}$.

Time signals are represented by the delay between two signal events. Any small change in a time input only adjusts the relative delay between the two signaling events. The magnitude of the voltage transitions used to represent the signal remain constant, swinging from rail-to-rail. The right side of Figure 2.1 shows two time inputs with different supply voltages. Transitioning to a lower supply voltage

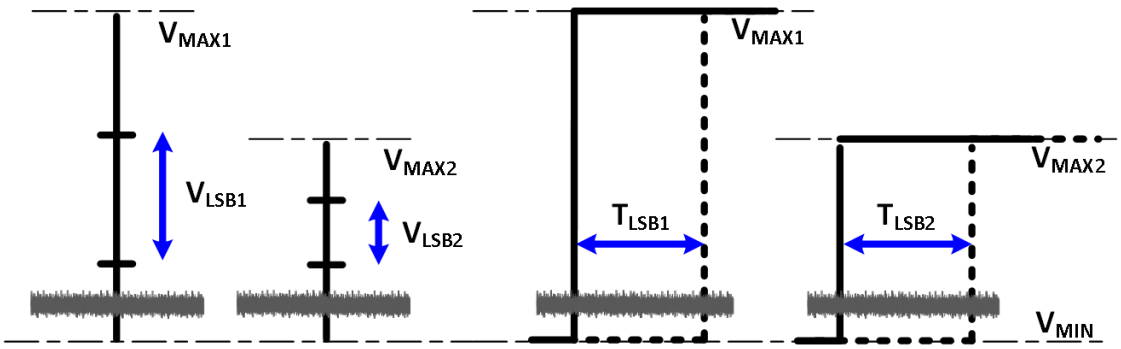


Figure 2.1: Minimum signal representation in the Voltage domain (left) and the Time domain (right).

does not directly reduce the time domain quantization step, as it does in the voltage domain. Additionally the input range of a time signal is not limited by the supply voltage. By containing analog signal information in the delay between two digital signals, time domain circuits are less sensitive to a lowered supply voltage while also benefiting from reduced gate delays in advanced sub-micron CMOS.

Time information utilization in data converters can be coarsely classified by the input signal domain and further by how the time information is used. With a time input, the desired digital code can be generated directly with a digital TDC. Alternatively, time inputs can be integrated onto a capacitor and quantized by traditional voltage techniques with a Time-to-Analog-to-Digital converter (TADC) [14], but ultimately experience the same supply voltage drawbacks mentioned previously, and are primarily used when a pure TDC architecture cannot deliver the necessary resolution of the given application.

Voltage signals can be processed using time domain techniques with a hybrid Analog-to-Time-to-Digital converter (ATDC). This category can be further clas-

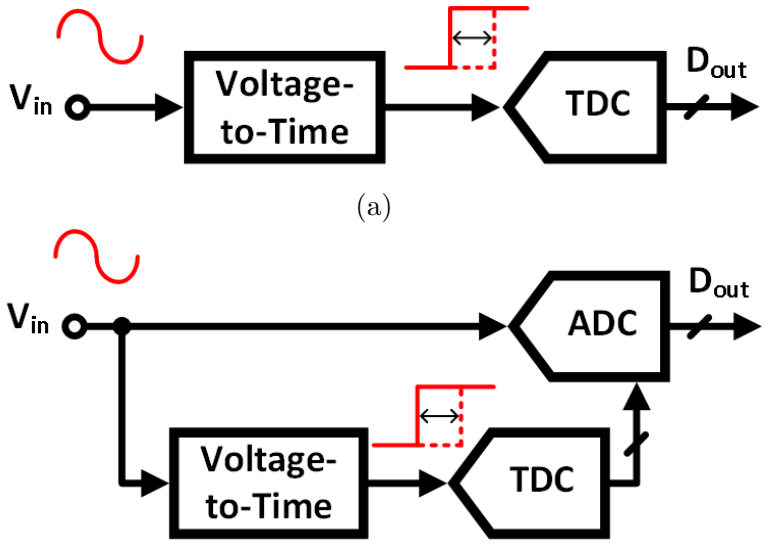


Figure 2.2: Block diagram of S-ATDC (a) and P-ATDC (b).

sified based on the order the time information is used, denoted serial-ATDC (S-ATDC) and parallel-ATDC (P-ATDC). The block diagram for a S-ATDC is shown in Figure 2.2a and works by translating the entire input voltage, or the quantization error from a coarse ADC, into a pair of clock events. A P-ATDC block diagram is shown in Figure 2.2b. P-ATDCs process signal information without exclusively relying on a TDC, using voltage and time information simultaneously to deliver output codes.

## 2.2 Time-to-Digital Converters

TDCs quantize the time interval between two events. The input can be represented by the time difference between two clock signals denoted START and STOP. The

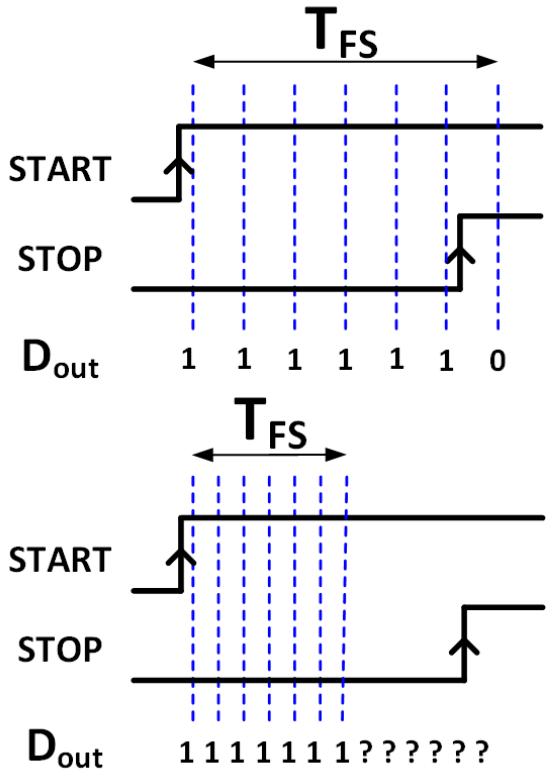


Figure 2.3: Time domain trade off between resolution and signal range.

output digital code is proportional to the duration of the pulse $T_{IN}$ defined as:

$$T_{IN} = START - STOP \tag{2.2}$$

An important characteristic of a TDC is the minimum time interval which can be measured ($T_Q$), also called the resolution. The maximum time interval that can be resolved ($T_{FS}$) is the input range. Input range is calculated as:

$$T_{FS} = K \cdot T_Q \tag{2.3}$$

where $K$ is the number of quantization steps. The fundamental tradeoff in TDC design is resolution vs. input range. Figure 2.3 shows how reducing $T_Q$ (improving the resolution) for a set number of quantization steps also reduces input range. If comparable range is required by the application, more quantization steps must be generated at the cost of additional hardware. TDC techniques focus on breaking this tradeoff while keeping power and latency low.

TDC designs can be broken down into three generations of development starting with delay line implementations, followed by multi-step and pipeline TDCs, and eventually progressing into oversampling $\Delta\Sigma$ modulators. The following sections introduce various TDC architectures.

### 2.2.1 First Generation TDCs

#### 2.2.1.1 Flash TDC

A Flash TDC is shown in Figure 2.4. It uses a chain of $K$ delay cells to generate $K$ reference clock signals [15]. The clock signals are separated by a constant period $t_d$. The STOP signal clocks the time domain comparators to sample the propagation of the START signal in terms of unit delays ($t_d$). A Flash TDC has the advantages of low latency and a highly digital implementation. Flash TDC resolution is limited to the minimum inverter delay of a given process. Conversion latency doubles for each extra bit of quantization, as does the integral non-linearity (INL), which is proportional to the length of the delay chain.

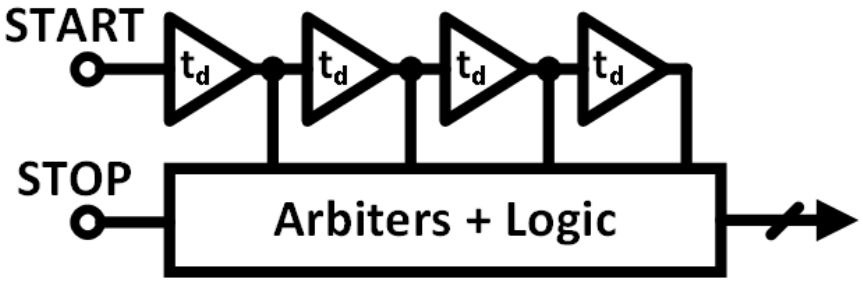


Figure 2.4: First generation TDC implemented with flash architecture [15].

#### 2.2.1.2 Vernier TDC

To address the issue of limited resolution found in Flash TDCs, a Vernier TDC (see Figure 2.5) makes use of two delay chains with different delay cells, a fast and a slow line [16]. Delaying the STOP signal by a shorter period than the START signal allows the STOP signal to propagate faster and eventually 'catch up' to the START signal, ending the conversion. The resolution of a Vernier TDC is determined by the delay difference between the fast and slow delay cells. This gives the design freedom to resolve sub-gate delay resolutions. The Vernier TDC requires precise matching between two delay lines. A delay locked loop (DLL) can be used to compensate for variations across process, voltage, and temperature (PVT). A DLL can only correct the delay of the entire chain, but is unable to correct mismatch between individual cells. Vernier TDCs ultimately improve upon Flash TDC resolution at the cost of increasing the power, area, and conversion latency.

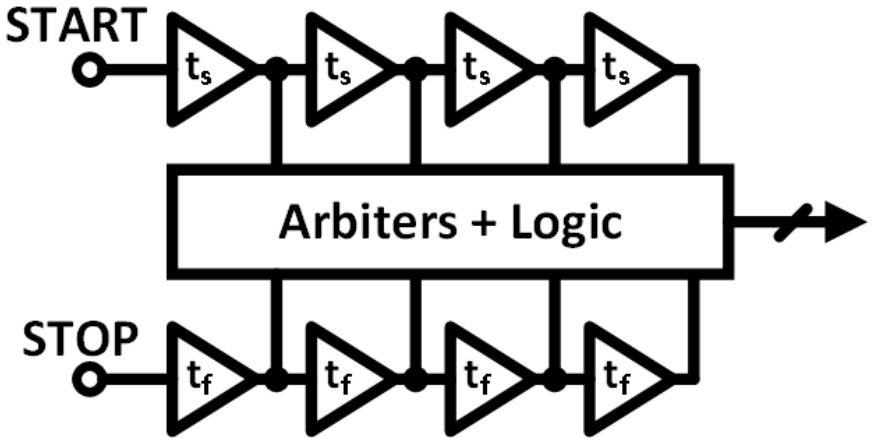


Figure 2.5: First generation TDCs implemented with vernier architecture [16].

### 2.2.2 Second Generation TDCs

#### 2.2.2.1 Coarse-Fine Interpolator

A coarse-fine interpolating TDC uses a low resolution TDC with large input range to quantize the most significant bits. A second TDC with high resolution and small input range resolves the quantization error from the coarse step, similar to a sub-ranging ADC. Breaking up the time quantization in this manner can reduce the number of delay elements, but also requires precise coordination between the two TDCs.

The fine TDC in [17] achieves high resolution and large input range with only 20 delay elements by using a two-level interpolating scheme. The coarse counting TDC extends the range by counting periods of a 5 MHz reference clock. Fine TDC precision is guaranteed across PVT by an analog intensive DLL, evident in the 40 mW power consumption. Digital correction is used to correct mismatch between

individual delay cells.

The technique in [18] adds a self clocking mechanism to the coarse-fine concept, allowing the coarse counter to extend indefinitely. This robust clocking scheme allows a time resolution of 8.125 ps over a 200 ns input range, delivering 14.6 effective number of bits (ENOB).

#### 2.2.2.2 Vernier Ring TDC

Another method to extend the range of a TDC without increasing the number of unit delay cells is to connect the last cell to the first and create a ring oscillator. Two such oscillators are combined in [19] to create a Vernier ring TDC. A ring structure allows indefinite range extension of the fine TDC, which reduces the need for a high frequency reference clock fed to the coarse counter. The Vernier ring quantizes the input phase within the ring when the STOP arrives. The reduced number of elements in a ring structure reduces the area overhead, but the power consumption and matching requirements of a delay line remain. The resolution is still ultimately dictated by the delay difference between two delay cells.

#### 2.2.2.3 Successive Approximation TDC

A successive approximation TDC was implemented in [20]. Successive approximation is performed by adjusting the relative delay between START and STOP signals by binary weighted delay periods to achieve high resolution. A pair of

digital-to-time converters (DTC) create time pulses that delay both the START and STOP until the delay difference is less than $T_Q$. Binary weighted delay cells reduce the total number required, but the long loop delay limits the maximum conversion rate.

[21] addresses this issue by only adjusting the delay added to the STOP signal. The START signal is always delayed by a time period that is relative to the current delay stage. This operation is similar to a Vernier TDC where the STOP signal 'catches up' to the START signal. Successive approximation attains resolution comparable to Vernier, but reduces conversion time to allow higher sampling rates.

#### 2.2.2.4 Pipelined TDCs

Much like pipelined ADCs, time amplifiers can be coupled with residue generation blocks to process the quantization error from a coarse TDC. A four stage pipelined TDC and MDAC stage are shown in Figure 2.6. This hierarchical approach can improve the time resolution without limiting the sampling speed and permits the use of simple sub-TDCs such as flash [22, 23, 24, 25]. The drawback of pipelined TDCs is that negative feedback techniques are difficult to implement on time domain signals. Additionally, it is impossible to store pure time information. To perform amplification, the time signal must be converted to an intermediate quantity of voltage or charge to implement a true synchronous pipeline. The nonlinear amplifier characteristic currently limits pipelined TDC performance to resolutions of about 1 ps.

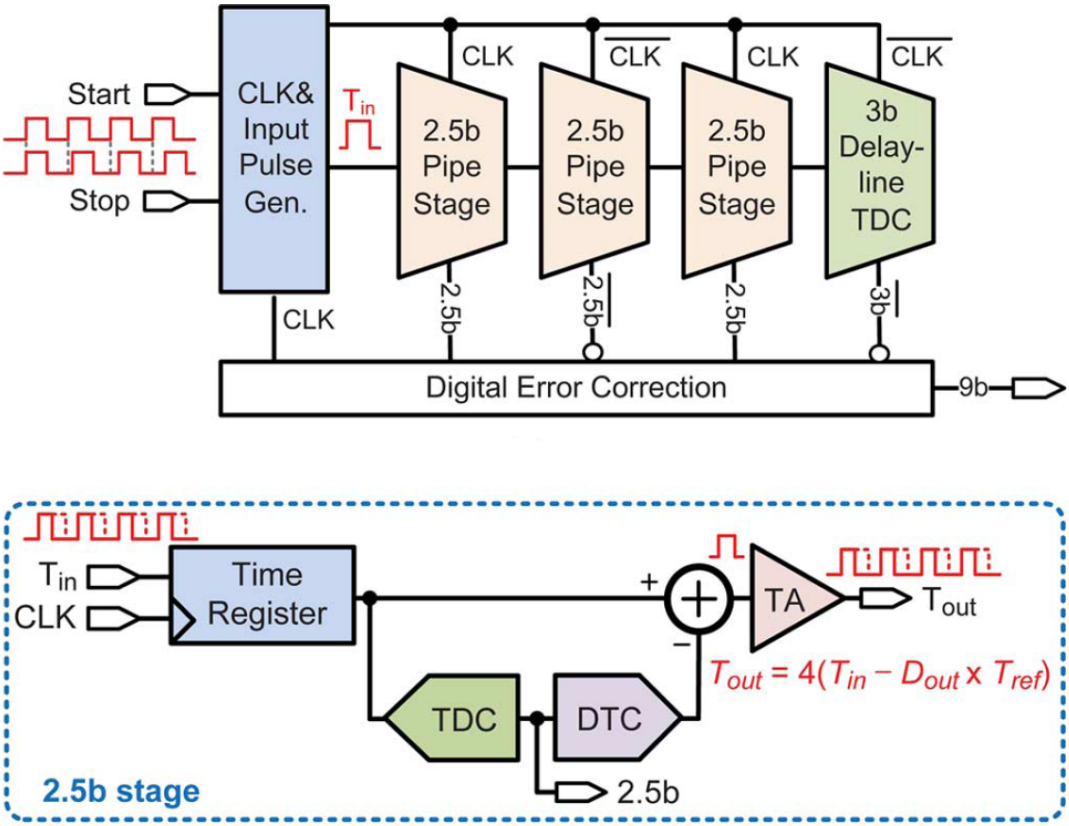


Figure 2.6: Pipelined TDC (top) and pipeline stage (bottom) [24].

### 2.2.3 Third Generation TDCs

$\Delta\Sigma$ TDCs are capable of high resolution due to their noise shaping properties. The challenge lies in the interface between the voltage and time domains in the feedback network to achieve high order noise shaping. The work in [26] achieves third order noise shaping with a (MASH) architecture with low sensitivity to PVT variations. Here the quantization error is stored in the phase of a relaxation oscillator, providing an extra order of noise shaping from the quantizer. [26] achieves 5.6 pS resolution over a 20 nS range with 1.7 mW of power consumption, demonstrating a high efficiency for time domain conversion.

## 2.3 Time-Assisted ADCs

A growing area of interest lies in ADCs which do not rely exclusively on voltage or time domain techniques, but instead combine the two into hybrid architectures. These techniques achieve high resolution or low power consumption at low supply voltages. These converters benefit from highly digital blocks that process time signals that are proportional to the input voltage.

### 2.3.1 Serial-ATDC

Serial-ATDCs are a subset of ADCs which use a TDC to resolve the least significant bits (LSB). A Voltage-to-Time converter (VTC) is used to transform a voltage into a set of clock edges.

#### 2.3.1.1 Pulse Position Modulation ADC

The pulse position modulation (PPM) ADC in [27] replaces voltage measurement with time measurement to significantly reduce power and silicon area. PPM compares a voltage input $V_{in}$ to a steady ramp voltage $V_{ramp}$. A coarse-fine TDC quantizes the time period between START and STOP. The ramp START signal is the rising edge of the sampling clock and the STOP signal is generated by the level-crossing event as seen in Figure 2.7. The sampling instants occur at non-uniform intervals depending on the input magnitude. These non-uniform samples require additional digital filtering, but the overhead is negligible in advanced process. The front end comparator input common mode range can limit the usable input swing, and can have signal dependent delay with a wide range input, producing harmonic distortion.

#### 2.3.1.2 Time-Based Pipelined ADC

A low power, high resolution ADC based on a time domain pipeline TDC is presented in [28]. A 4 bit voltage domain flash quantizer is used to reduce the input swing to a VTC. High linearity V-T conversion and residue amplification is achieved with a simple 24 dB amplifier. After sampling and amplification, the third phase of the VTC is discharging. Fig 2.8 shows the three phases of operation. In the third phase, a discharging current source is connected to the virtual ground of the amplifier to begin discharging the sampling capacitor. An amplified version of the virtual ground is sensed by a level crossing comparator. The length

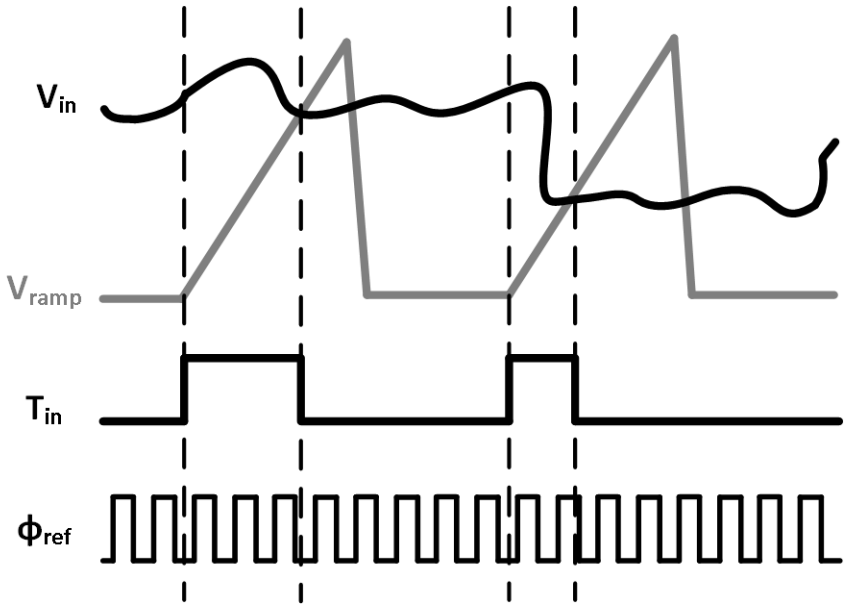


Figure 2.7: Signal diagram displaying non-uniform sampling of PPM [27].

of the discharging period is then quantized by a pipeline TDC.

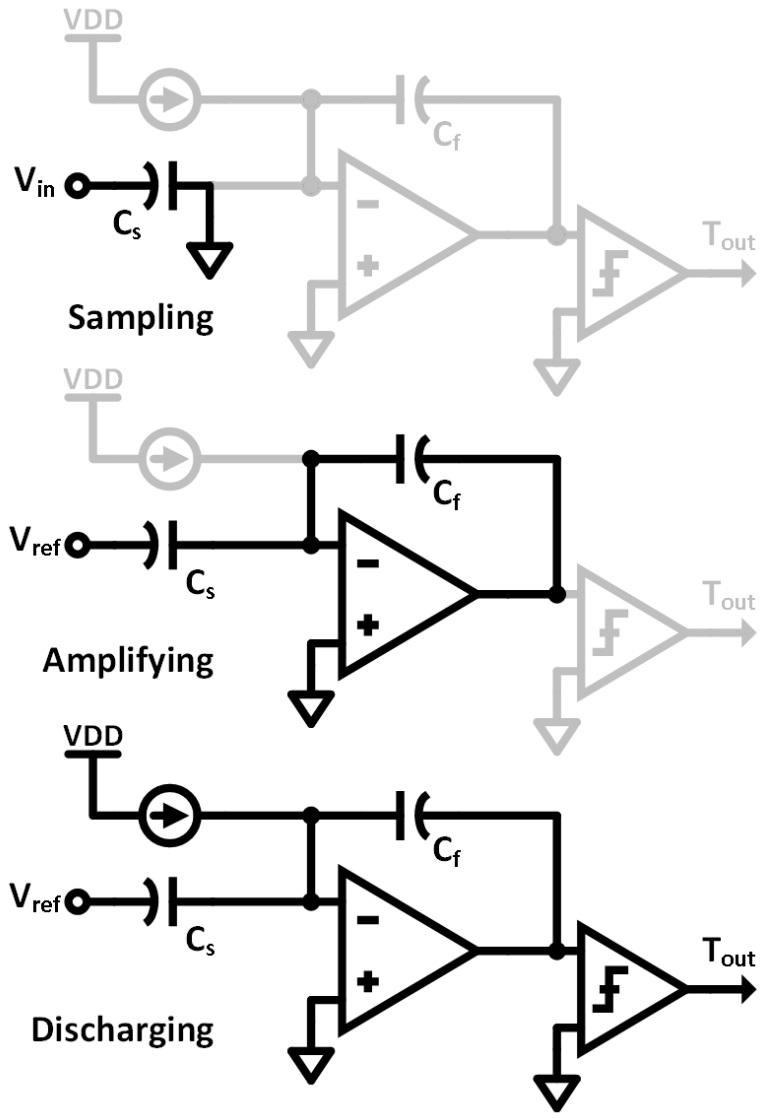


Figure 2.8: Three-phase Voltage-to-Time converter during each phase of operation [28].

A single pipeline stage is shown in Figure 2.9. It is comprised of a 2.5 bit flash TDC, asymmetric charge pump for time amplification, a capacitive DAC for

residue generation, and a level crossing comparator. MDAC linearity depends on the current source linearity and capacitor matching. Pipelined operation results in increased sampling rate, high resolution, and low power. Time domain pipeline stages avoid traditional power hungry analog blocks and instead use highly digital TDCs. The overall performance is limited by the speed of the three phase VTC, the lack of sufficient delay correction range, and matching between delay cells [28].

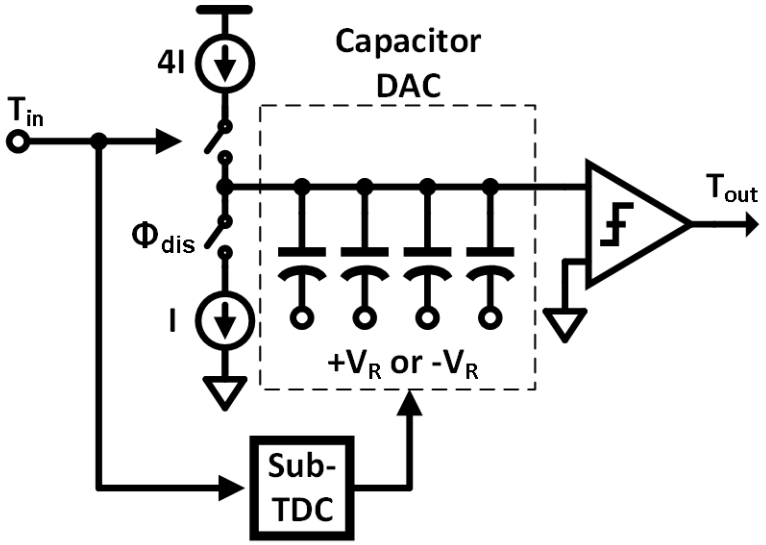


Figure 2.9: A single stage of the time-based pipeline ADC [28].

#### 2.3.1.3 Successive Approximation Register with Time-Domain Quantizer

Ultra low-voltage performance is demonstrated by the hybrid successive approximation register (SAR) ADC in [10]. A front end SAR ADC coarsely quantizes

the input voltage. Residual charge left on the DAC can then be used to generate a proportional time pulse which is sent to a TDC. The block diagram for this architecture is shown in Figure 2.10. The non-linearity of VTC is mitigated by operating on a small range input signal. A voltage controlled delay line (VCDL) uses the SAR residue as its tuning voltage to provide a time domain output. A Vernier TDC with redundancy quantizes the time pulse to complete the conversion. There are two main benefits of performing fine quantization in the time domain. First, the SAR comparator area can be reduced due to the relaxed noise and offset specification of a lower resolution ADC. Second, the total number of unit capacitors can be reduced by a factor of two for each additional bit of time domain quantization.

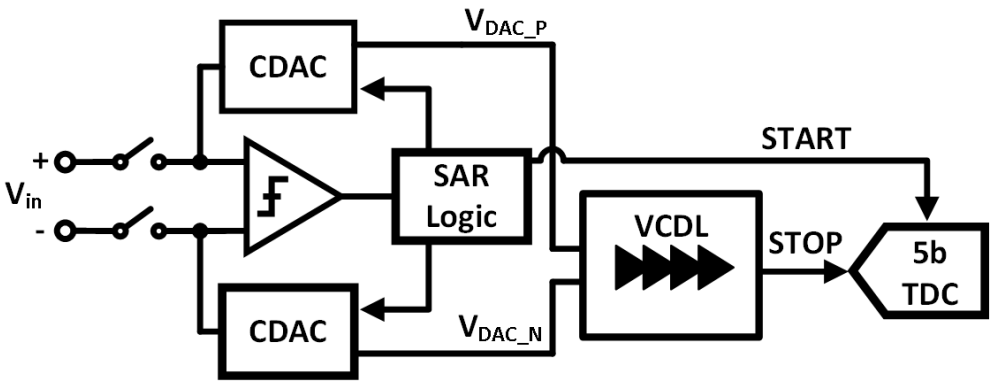


Figure 2.10: Hybrid SAR-TDC architecture that uses a time domain back end quantizer [10].

### 2.3.2 Parallel-ATDCs

Parallel-ATDC techniques utilize both voltage and time information simultaneously, without transferring the signal information exclusively to a single domain.

Parallel techniques main application is in improving the energy efficiency of an ADC.

#### 2.3.2.1 SAR with Time Domain MSB Control

The SAR ADC in [29] shown in Figure 2.11 uses a rail-to-rail V-T converter and a 3.5 bit TDC to perform multi-bit quantization at the start of conversion cycle to increase the speed over a traditional SAR ADC. Capacitor switching energy is reduced by switching the large capacitors in parallel, and the multi-bit TDC results in smaller area and kickback noise when compared to a conventional flash quantizer. In this configuration the V-T converter requires an increased supply with thick oxide devices to increase the linear conversion range, raising reliability concerns for advanced CMOS implementations.

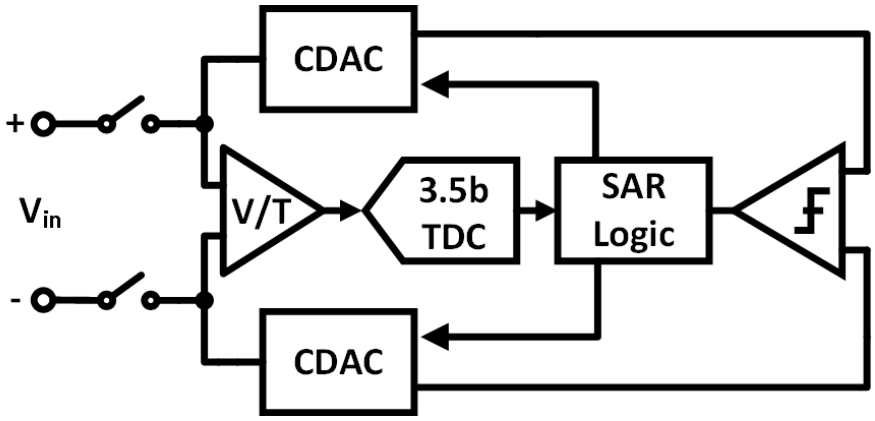


Figure 2.11: Hybrid TDC-SAR architecture that uses a VTC and TDC to control the 3 MSB capacitors

#### 2.3.2.2 Data Driven Noise Reduction

Data driven noise reduction (DDNR) is proposed as an effective way to reduce the effects of thermal noise in high efficiency SAR converters with asynchronous clocking [12]. DDNR takes advantage of the fact that there is generally one noise-critical comparator decision per sample, which can result in excessively long latched comparator regeneration time [30]. This 'hard' decision is detected by sending the comparator clock through a VCDL and comparing this delayed clock with the comparator's internally generated ready signal. A simplified schematic is shown in Figure 2.12. A small differential input voltage represents a slower comparator decision, prompting the necessity for noise reduction. Effective noise is reduced by repeating the comparator decision five times and applying a majority voting process. The time reference is generated with a feedback loop that manages the number of fast and slow detection events as set by the operator. This technique trades off conversion speed for noise reduction and ultimately power efficiency, using a 1 bit time domain comparator to manage the tradeoff.

#### 2.3.2.3 Ternary SAR

Time based quantizers have been proposed to replace voltage comparators in SAR ADCs [31, 32], but lose the accuracy and global offset provided by a single voltage comparator. The VTC implemented by a VCDL in [31, 32] must accommodate a wide input range with high linearity while also adding delay to the critical path of the signal. Ternary-SAR (TSAR) takes advantage of a time domain quantizer,

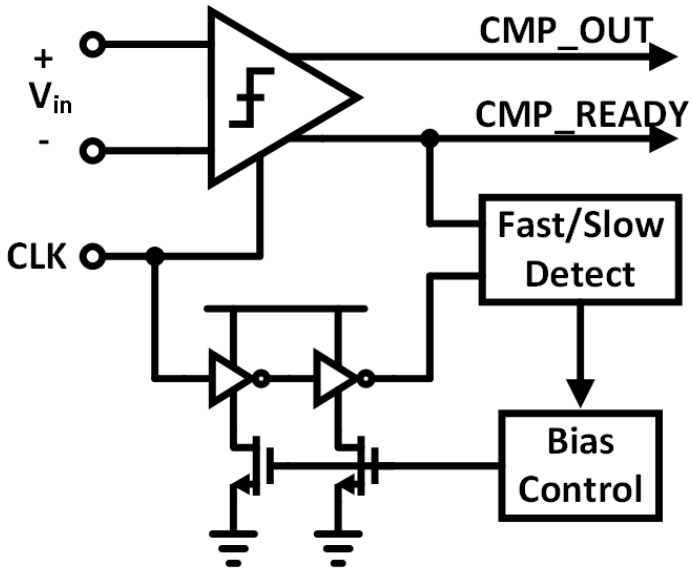


Figure 2.12: Data driven noise reduction operation [12].

but maintains the benefits of a voltage comparator.

Similar to DDNR [12], TSAR enlists a 1 bit TDC to enhance power efficiency in a SAR ADC as seen in Figure 2.13a, but adds speed benefits through stage skipping [11]. The unique aspect of TSAR lies in how it uses the TDC output code along with the comparator code, shown in Figure 2.13b. Where DDNR applied a majority vote to noise-critical decisions (relying on binary codes), TSAR skips them and instead depends on the subsequent SAR bit cycles to determine the final output code (ternary codes). TSAR gains redundancy benefits similar to a dual-comparator SAR without the added voltage domain DAC and comparator.

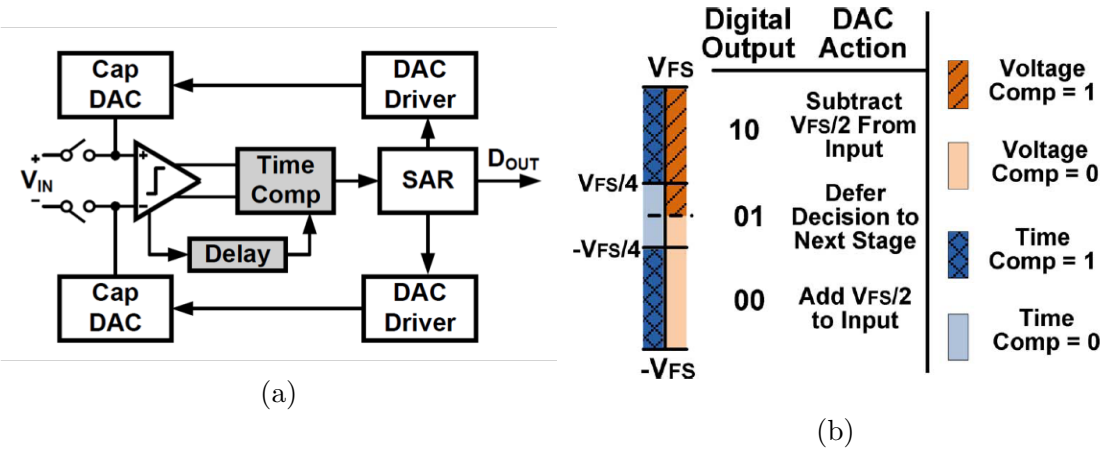


Figure 2.13: Block diagram 2.13a and truth table 2.13b showing dual domain operation principle of TSAR.

#### 2.3.2.4 Voltage Controlled Oscillator based ADC

Nyquist ADCs rely on precise matching of analog components to perform with high accuracy. As technologies scale and geometric matching degrades, the ratio of clock jitter to the minimum gate delay increases. Much like voltage domain designs, time domain solutions can trade off bandwidth for higher resolution with an oversampled $\Delta\Sigma$ ADC.

A voltage controlled oscillator (VCO) can use its output oscillation frequency as the time reference required by a TDC. Previous techniques use an input voltage to modify a pulse width which is then compared to a static reference clock. Instead, the input voltage is used to modify the reference clock period (VCO output frequency) as shown in Figure 2.14. Counting the number of VCO edges that occur within a sampling period gives a digital estimate of the input voltage.

Figure 2.15 shows a high speed implementation used in [33]. The phase differ-

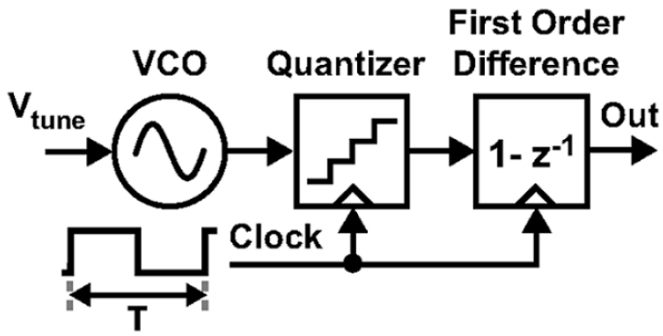


Figure 2.14: Linear model for VCO based Quantizer [33].

ence between the VCO output and the reference clock represents the quantization error. During the successive conversion, the oscillator resumes where it left off, providing first order noise shaping. The issue that arises is the linear tuning range of the voltage-to-frequency conversion. The work in [33] suppresses the VCO non-linearity by pairing it with a loop filter and using it as the quantizer in a $\Delta\Sigma$ ADC.

The inherent barrel shifting of the oscillator reduces the need for explicit dynamic element matching. This work uses a highly digital multi-bit VCO quantizer and time domain principles to reduce the quantization noise in a high performance $\Delta\Sigma$ ADC. The noise shaping property of the quantizer saves significant analog power consumption by reducing the order of the loop filter by one.

## 2.4 Conclusion

Time domain signal representation has been reviewed both as an alternative, and as a support mechanism for Analog-to-Digital converters. As transistor sizes scale

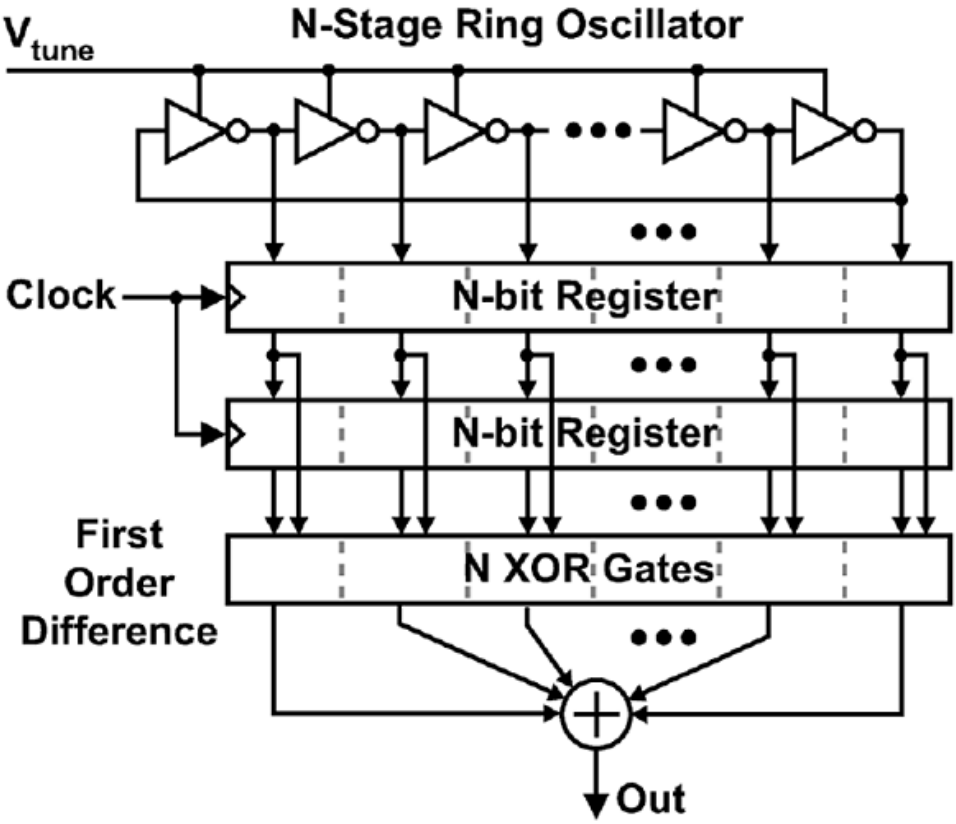


Figure 2.15: High speed VCO based quantizer implementation [33].

down and supply voltages decrease, traditional analog design techniques face challenges in terms of area and power efficiency. Time domain techniques result in highly digital architectures whose performance will scale much more easily than their analog counterparts. The performance of the various TDCs discussed in this paper are shown in Table 2.1. Performing signal conversion entirely in the time domain is limited by the input range vs. resolution tradeoff. Difficulties in amplification and storage of time signals prove to be an valuable area of further study.

Table 2.1: Performance Comparison of TDC Techniques

| **Architecture** | **Technology (nm)** | **Resolution (pS)** | **Range (nS)** | **Power (mW)** |
|---|---|---|---|---|
| **Vernier [16]** | 700 | 30 | 3.84 | - |
| **SATDC [20]** | 350 | 1.22 | 327000 | 33 |
| **Vernier Ring [19]** | 130 | 8.00 | 32.8 | 7.5 |
| **SATDC [21]** | 65 | 9.77 | 10 | 9.6 |
| **Coarse-Fine [17]** | 350 | 12.2 | 204000 | 40 |
| **Pipeline [24]** | 65 | 1.12 | 0.573 | 15.4 |
| **111 MASH [26]** | 130 | 5.60 | 20 | 1.7 |

ATDC techniques allow time domain circuits to process a wide array of input signals, but also require a power efficient and linear VTC. The performance of several time supported architectures are compared in Table 2.2. Direct comparisons of TDC to ATDC performance are challenging due to the difficulty of generating a pure sinusoidal time domain input signal. Clearly highly digital and time based circuit implementations are increasing in scope and performance.

Table 2.2: Performance Comparison of Time supported ADC Techniques

| **Architecture** | **Technology (nm)** | **Bandwidth (MHz)** | **Power** | **SNDR (dB)** | **FOM* (fJ/C-S)** |
|---|---|---|---|---|---|
| **PPM [27]** | 90 | 0.3 | 14 uW | 49.3 | 97.9 |
| **Pipeline [28]** | 130 | 50 | 6.38 mW | 62.6 | 57.9 |
| **SAR+TDC** | 90 | 0.125 | 200 nW | 53.7 | 2.02 |
| **DDNR SAR [12]** | 65 | 0.0189 | 97 nW | 62.5 | 2.35 |
| **TSAR [11]** | 130 | 4 | 83.8 uW | 57.56 | 16.9 |
| **VCO DSM [33]** | 130 | 10 | 40 mW | 72 | 615 |

* FOM = $\frac{Power}{2^{(ENOB^{**})} * 2 * Bandwidth}$ ** ENOB = $\frac{SNDR - 1.76}{6.02}$

# Chapter 3: A Hybrid SAR-TDC Nyquist ADC

> "If you're not making mistakes, then you're not doing anything. I'm positive that a doer makes mistakes."
>
> — *John Wooden*

Design of a high resolution analog-to-digital converter (ADC) is becoming more challenging in sub-micron CMOS due to reduced intrinsic gain and limited voltage headroom. The goal of this chapter is to design a high resolution, low power ADC. Time domain techniques will be explored to assist in signal quantization and provide a scalable ADC solution.

## 3.1 The SAR ADC

The basic SAR ADC is a highly efficient architecture owing to its simple structure using mostly digital parts, allowing its performance to scale with CMOS technology. A basic block diagram and transient waveform are shown in Figure 3.1. After the input is sampled, the sampling capacitor bottom plates can be pulled to a high or low voltage, implementing a feedback DAC. The voltage at the input of the comparator is defined by Equations 3.1 and 3.2, where $i$ represents the current bit cycle, and $D_i$ is the comparator result for each cycle. With each decision, the

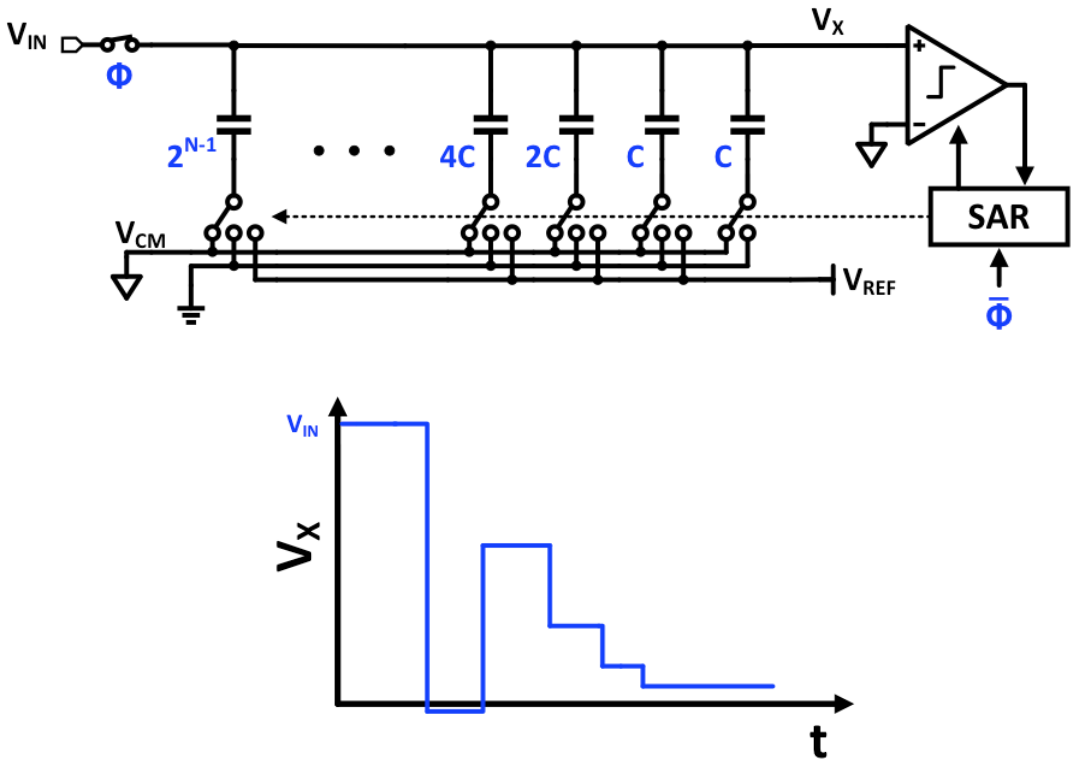


Figure 3.1: A basic SAR ADC using top plate input sampling and the merged capacitor switching algorithm [34].

difference between the input and DAC voltage is reduced. After the final decision, we are left with the N-bit residue voltage.

$$V_X = V_{IN} - V_{DAC} \tag{3.1}$$

$$V_{DAC} = \sum_{i=1}^{N-1} D_i \cdot \frac{V_{REF}}{2^i} \tag{3.2}$$

Attaining high resolution with a single SAR quantizer is difficult due to two

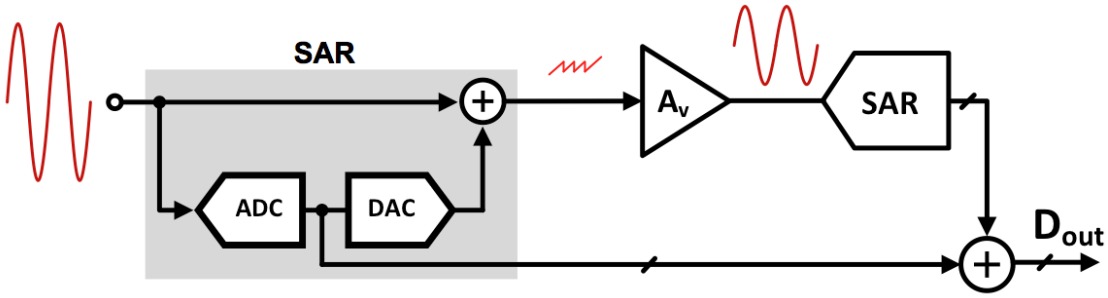


Figure 3.2: Simplified block diagram of the two-step SAR-assisted pipeline architecture.

primary reasons. The first is that with each additional bit of resolution, the DAC used for feedback switching must generate additional references for successive comparisons. This is achieved by doubling the number of unit capacitors with each bit. If the unit capacitor value cannot be reduced, the switching power consumption inevitably goes up. The second reason is that the comparator used must reduce its input referred noise power for each additional bit required. In this high resolution case, the comparator is designed for the worst case comparison. The overhead from reducing noise power results in wasted energy in all but one of the SAR decision cycles.

## 3.2 The SAR-Assisted Pipeline

The SAR-assisted pipeline ADC was proposed in [35]. A block diagram is shown in Figure 3.2. A SAR-assisted pipeline works by splitting the conversion between two SAR quantizers, using a residue amplifier to amplify the first SAR residue.

The SAR-assisted architecture can be used to replace the flash sub-ADC as

the speed of SAR increases with advanced CMOS, but the residue amplifier ($A_V$) continues to be a critical design bottleneck. Novel architectures such as ring amplifiers [36] and dynamic amplifiers [37] have been proposed to overcome challenges that arise due to process scaling, but still face headroom challenges as they operate using large signal swings in the voltage domain. The design of a conventional residue amplifier in the context of a SAR-assisted pipeline will be explored in the next section.

### 3.2.1 Residue Amplification

A switched capacitor residue amplifier works on the well known principles of high gain and bandwidth in negative feedback, ans using two non-overlapping clocks as shown in Figure 3.3. The operating principle is that the input signal is stored as a charge in the large capacitor $C_S$. Then, the charge is transferred to the smaller capacitor $C_F$. If there is no charge loss during this transfer, the resulting output voltage is perfectly amplified by a set amount. The right side of Figure 3.3 shows step response voltages at both the output $V_O$ and virtual ground nodes $V_X$. The transfer function of this approach is defined by Equation 3.3 [38].

$$\frac{V_O(s)}{V_I(s)} = -\frac{C_S}{C_F} \cdot \frac{\beta A_0}{1+\beta A_0} \cdot \frac{1}{1+\frac{s}{\omega_p}} \tag{3.3}$$

The feedback factor $\beta$ can be approximated as follows for a high resolution first stage ADC:

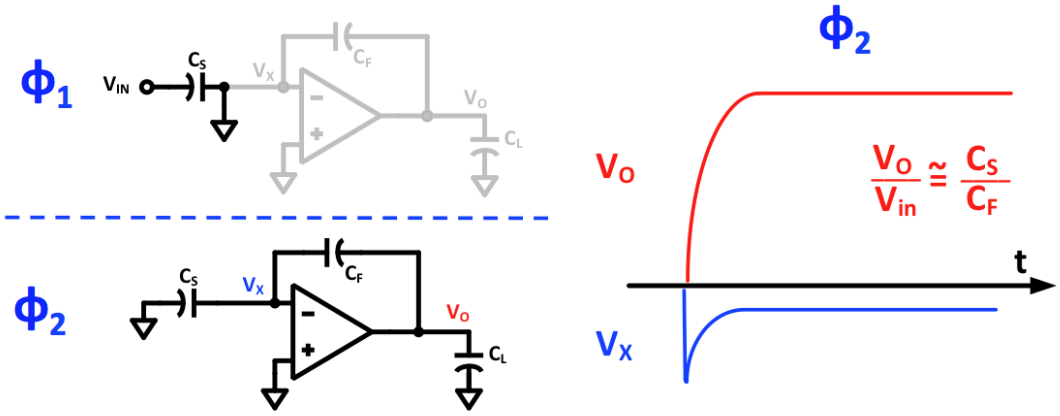


Figure 3.3: Simplified view of a switched capacitor residue amplifier with approximate transfer function.

$$\beta = \frac{C_F}{C_S + C_F + C_X} \approx \frac{C_F}{C_S} \tag{3.4}$$

where we can often use the following approximation if the low frequency gain $A_O >> 1$.

$$\frac{V_O}{V_I} \approx \frac{1}{\beta} = \frac{C_S}{C_F} \tag{3.5}$$

This result shows a well defined gain based on capacitor ratios that is highly desirable. However, if the gain does not follow the approximation $A_O >> 1$, as is often the case in scaled CMOS with limited intrinsic gain, the transfer function becomes non-linear with regards to the input voltage.

There is an additional frequency dependent term in Equation 3.3, where $\omega_p$ is defined by:

$$\omega_p = \frac{\beta G_m}{C_L + (1-\beta)C_F} \tag{3.6}$$

This single pole model can only be used for a single stage amplifier, severely limiting our choice of architecture. Multiple stages can be used to increase $A_0$, but also results in multi-pole system dynamics. This limits the bandwidth for a given power consumption.

Also take into account the size of $C_L$ which must be designed to meet the SNR requirement of the second stage SAR, and must usually swing to at least half of the reference voltage range (in the case of a 1 bit redundancy between stages). If the process has a minimum capacitor size $C_{min}$, the total load capacitor required to implement a second stage SAR DAC is found to be:

$$C_L = 2^m \cdot C_{min} \tag{3.7}$$

The minimum capacitor for the available process was approximately 30 fF. For a 30 fF unit capacitor, this total load capacitance can dominate the settling performance, and far exceeds the minimum required capacitance as defined by thermal sampling noise contribution. Therefore, the larger load capacitance also necessitates an increase in amplifier transconductance $G_m$ for a given $\omega_p$. Amplifier techniques based in the time domain have the potential to reduce this load capacitance, minimize output swing requirements, and relax the gain requirement.

## 3.3 Hybrid Domain ADC Techniques

Hybrid voltage-to-time (V-T) techniques have been proposed as an alternative to conventional amplifier based pipelines. For time domain quantizers, signal-to-noise ratio (SNR) is ultimately dictated by the relationship of the sampling period to the inverter delay, and not by the supply voltage. This design paradigm offers potential advantages in environments with a low supply voltage and fast inverter propagation delays, as described in Chapter 2.

Reference [39] cascades a SAR with a digital slope ADC [40] for low power operation, but has limited resolution and speed due to its sub-ranging nature. Reference [41] implements a multi-bit per step SAR which uses a voltage-controlled-oscillator (VCO) based quantizer, demonstrating high resolution and speed under a low supply voltage, but also requires non-linearity calibration of multiple VCO tuning characteristics. The time-based pipeline in [42] combines a flash sub-ADC and V-T residue amplifier with a cascade of time-based pipeline stages, achieving high resolution and speed, but consumes extra power due to a pipelined time-to-digital converter (TDC) back-end. The hybrid SAR-VCO technique in [43] demonstrates another method to take advantage of the fast switching of sub-micron CMOS by using a VCO-based second step, but has limited bandwidth due to its oversampling requirement.

The architecture proposed in this chapter combines the high efficiency and digital nature of a SAR ADC as a coarse quantizer, a power efficient V-T residue amplifier, and a simplistic flash time-to-digital converter (TDC)[44]. The goal

of this ADC is to deliver high resolution and wide bandwidth by using a simple amplifier with low gain and swing specifications. In addition, a time domain back-end can use a low supply voltage because the signal is simply the delay between two digital edges, rather than a voltage or current signal. The time based back-end can directly benefit from process scaling. As switching speeds increase, so does the resolution of a TDC. The digital nature of this technique provides a level of scaling immunity that has previously been limited to low and mid resolution ADCs.

## 3.4 Proposed Hybrid Voltage and Time Domain ADC

The hybrid architecture proposed here is very similar to the SAR-Assisted Pipeline described in the previous section. The key difference is that the residue amplifier generates a time pulse, instead of a voltage output. A simplified block diagram is shown in Figure 3.4. The left side of Figure 3.4 shows a standard SAR feedback loop in which the DAC voltage is continually driven towards the input, making their difference approach zero. This residue voltage is then driven into the VTC denoted $K_{VT}$. The resulting output pulse can be further quantized by the back end TDC. As is the case with a conventional pipeline, the actual implementation of the VTC is the key to a power efficient architecture.

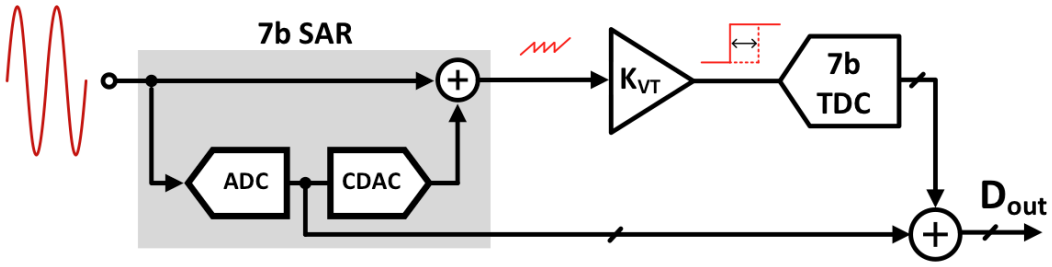


Figure 3.4: Simplified block diagram of the proposed two-step architecture.

### 3.4.1 A High Speed VTC

One implementation of a high speed VTC is shown in Figure 3.5. A conventional residue amplifier can be modified by adding a discharging current source $I_D$ and a continuous-time comparator acting as a zero-crossing detector (ZCD) as shown. After the amplification phase ($\phi_2$), the amplified signal is stored on capacitor $C_F$. During the following phase $\phi_1$, the current source is enabled, causing a voltage ramp to appear at the output. This ramp continues until the output reaches zero, causing the ZCD to change state, disabling the current source. The duration of the discharge period is proportional to the input voltage.

To find the output voltage, we must combine the terms from the feedback amplifier charge transfer, and the current source charge. The current source charge can be found by equating charge equations as follows.

$$Q_1 = C \cdot V \tag{3.8}$$

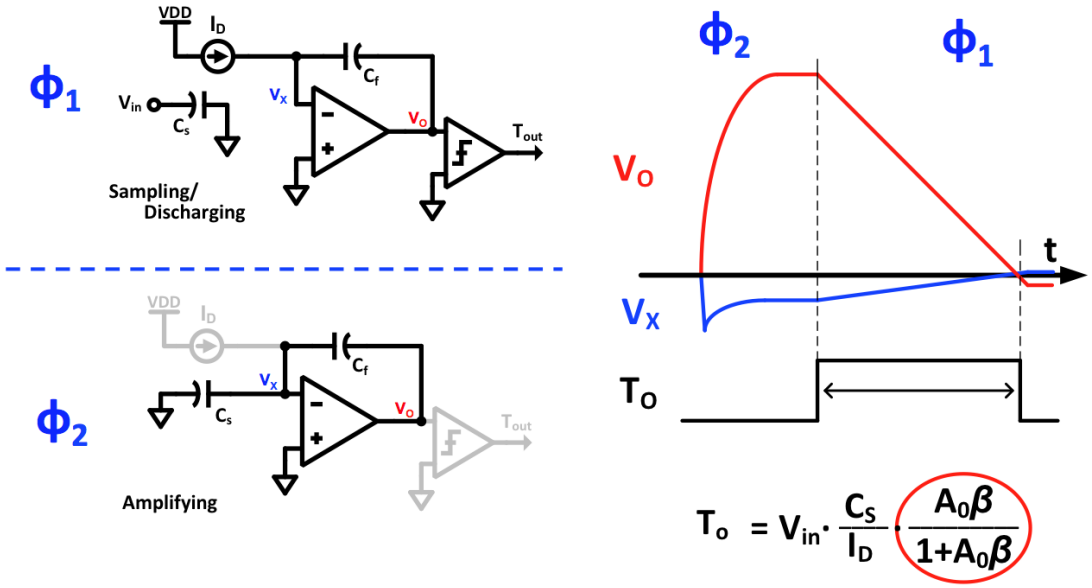


Figure 3.5: High speed voltage-to-time converter.

$$Q_2 = I \cdot T \tag{3.9}$$

Setting charges equal and solving for voltage gives the current source contribution to output voltage. This is then subtracted from the amplifier voltage as defined in Equation 3.10. At the zero-crossing event, the output voltage is zero. Solving this equation for the time domain signal $T_O$, we arrive Equation 3.11.

$$V_O = -V_{IN} \cdot \frac{C_S}{C_F} \cdot \frac{\beta A_0}{1+\beta A_0} - \frac{I_D T_O}{C_F} \tag{3.10}$$

$$T_O = V_{IN} \cdot \frac{C_S}{I_D} \cdot \frac{\beta A_0}{1+\beta A_0} \tag{3.11}$$

Based on Equation 3.11, we can see that the time domain output is still highly dependent on the amplifier performance. This can also make intuitive sense because the initial amplified signal was subject to the closed loop transfer function including $C_S$, whereas the current source was only discharging the feedback capacitor $C_F$. Therefore, any charge loss during $\phi_2$ would result in similar non-linearity as a conventional residue amplifier.

### 3.4.2 A Low Power VTC

A modified version of the VTC presented in the last section was proposed in [42]. In this work, three clock phases were used as opposed to two. The first two phases ($\phi_1$ and $\phi_2$) are identical to a voltage domain residue amplifier. When the current source is enabled however, the sampling capacitor connection is maintained. Now that the current source sees the same circuit configuration as the initial residue amplification from $\phi_2$, the output voltage can be described by Equation 3.12. This assumes the amplifier bandwidth is much greater than the discharge period. Solving for the time domain output at zero-crossing again now results in Equation 3.13. In this configuration, the output time domain signal $T_O$ is independent of the amplifier gain $A_0$.

$$V_O = -V_{IN} \cdot \frac{C_S}{C_F} \cdot \frac{\beta A_0}{1+\beta A_0} - \frac{I_D T_O}{C_F} \frac{\beta A_0}{1+\beta A_0} \tag{3.12}$$

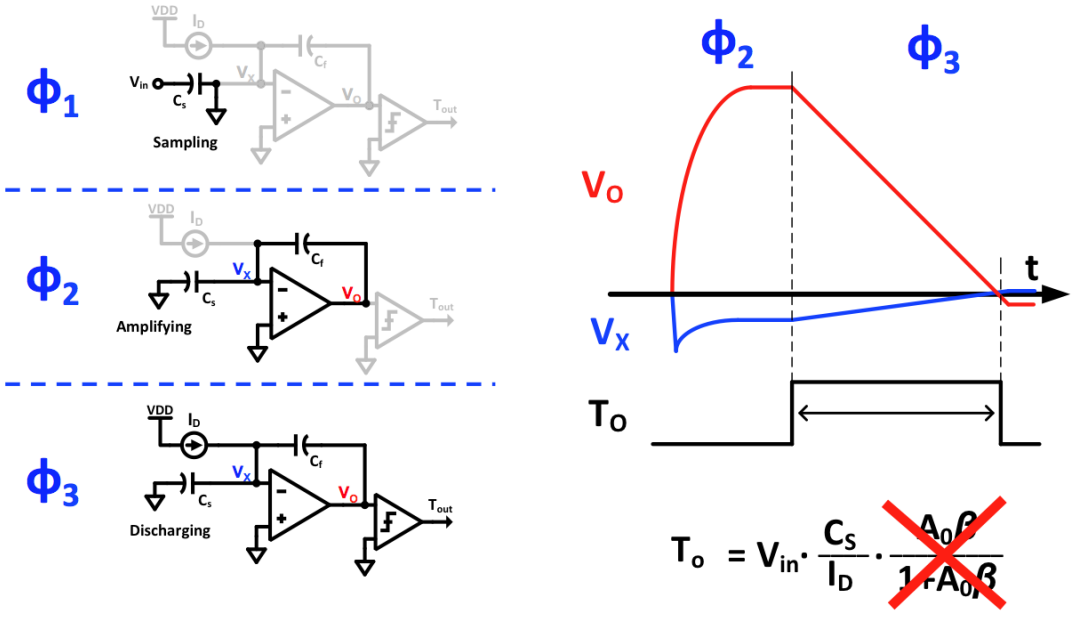


Figure 3.6: Low power three phase voltage-to-time converter proposed in [42].

$$T_O = V_{IN} \cdot \frac{C_S}{I_D} \tag{3.13}$$

A VTC modeled after this implementation can relax both the required gain and output swing specifications of the residue amplifier. The primary cost of this technique is a reduction in speed, as we now require the sampling capacitor to stay connected during the discharge period. High linearity despite a small linear output range is possible because the time domain sampling instant always occurs with the same zero differential output swing. This allows the use of a single-stage amplifier with high bandwidth, avoiding the wasted power of a 2-stage compensated amplifier.

Assuming the amplifier has sufficient bandwidth, the V-T residue gain depends

on the sampling capacitor and discharge current magnitude as shown in equation 3.14, which is independent of the amplifier finite gain. In this configuration, $K_{VT}$ primarily depends on the current source, whose linearity should exceed that of the 7-bit TDC.

$$K_{VT} = \frac{T_O}{V_{IN}} = \frac{C_S}{I_D} \tag{3.14}$$

The discharge current source also contributes additional noise compared to a conventional pipeline ADC. This results in an increase in sampling capacitance for the same SNR performance. Even considering this, there are two main advantages gained: substantial power savings from the low amplifier gain requirement, and the reduced signal headroom constraint, which can be a limiting factor in low voltage designs. A single stage residue amplifier with low gain is sufficient because the architecture does not require high gain to accurately transfer charge from a large capacitor to a smaller one. Instead of gain, this technique trades off speed for design simplicity, which has favorable outcomes in scaled process. The reduced swing specification obviates the need for a dedicated output stage with wide swing, resulting in large power savings, and a small analog footprint.

### 3.4.3 Circuit Implementation

Shown in Figure 3.7 is a simplified diagram of the proposed hybrid SAR ADC with time-based quantizer. It consists of a 7-bit asynchronous SAR ADC, a V-T residue amplifier stage in gray, and a 7-bit TDC back-end. In this configuration,

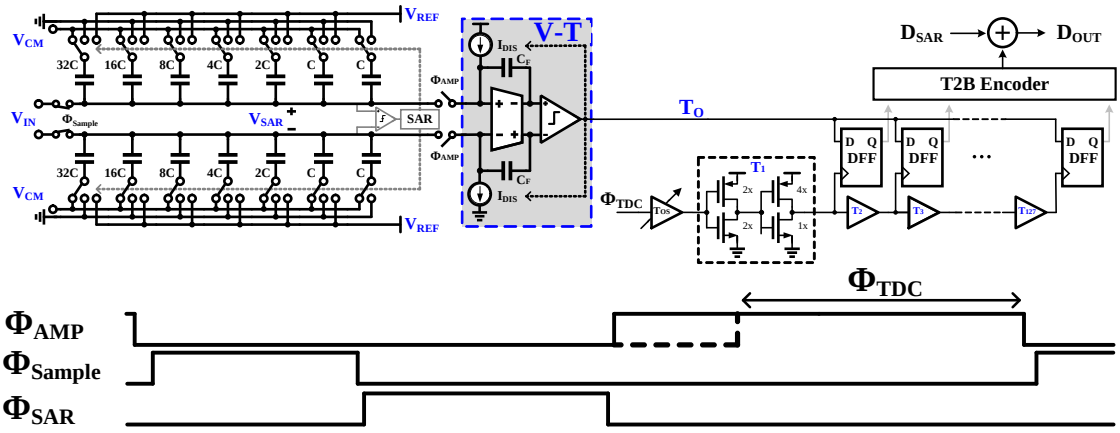


Figure 3.7: Simplified implementation schematic of the proposed architecture. The voltage-to-time conversion block is highlighted in gray.

the SAR feedback can efficiently minimize the signal swing, relaxing the linearity requirements of the residue amplifier and TDC back-end.

A 1-bit redundancy between stages allows for correction of SAR conversion errors. The operation of the ADC is as follows. Bootstrapped switches sample the input onto the 1.92 pF SAR digital-to-analog converter (DAC). Merged capacitor switching (MCS) technique is used in the SAR DAC to minimize switching energy and to maintain the signal common-mode voltage [34].

Following the SAR bit-cycling, the residual 7-bit voltage is available on the DAC output ($V_{SAR}$). This residue is differential, and therefore can have either positive or negative polarity. If unmodified, this residue would require four current sources (plus and minus on each DAC top plate) to properly discharge the residue towards zero. This adds an additional matching requirement and increases design complexity. Instead,a DC level shift guarantees the signal is always positive for unidirectional discharging. After a short pre-amplification period, current sources

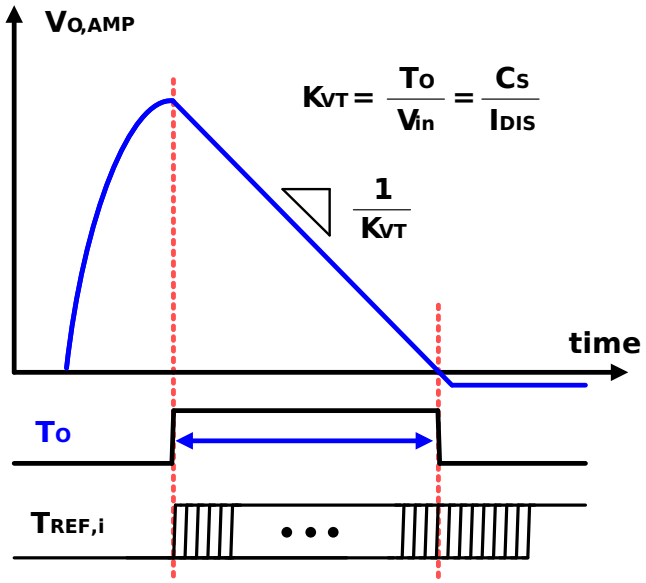


Figure 3.8: Example waveform showing the residue amplifier output ($V_{O,AMP}$), time domain signal ($T_O$), and TDC time references ($T_{REF,i}$).

discharge both the SAR and feedback capacitors, driving them towards common-mode. The output of the amplifier is sensed by a zero-crossing detector that generates a time pulse output signal. A single-ended waveform of the amplifier output is shown in Figure 3.8. This time interval represents the amplified residue which is quantized by the flash TDC. Thermometer-encoded outputs are converted to binary through a multiplexer based architecture for a short critical path and a more regular layout [45]. The digital output is produced by aligning digital bits from the SAR and TDC conversion steps.

By using the residue amplifier and a back-end quantizer after the SAR, the DAC capacitor spread can be reduced by a factor of 64. Additionally, the comparator noise and offset requirements are set by the coarse SAR resolution of 7 bits, instead

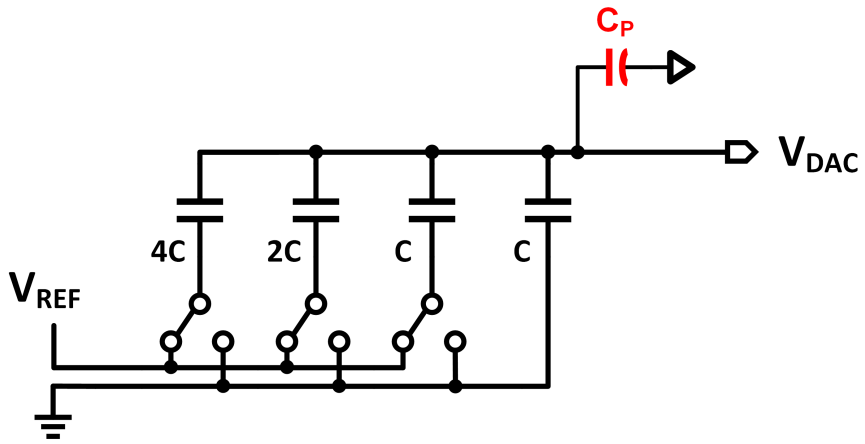


Figure 3.9: Additional top-plate parasitic capacitor $C_P$ will attenuate SAR DAC switching magnitude.

of the total ADC resolution, resulting in dramatic power savings.

## 3.5 Design Considerations

### 3.5.1 SAR DAC

The SAR capacitors are used for sampling as well as generating successive reference voltages. Top plate sampling is used to increase the conversion speed by eliminating the MSB DAC switching event. The inputs are sampled versus $V_{CM}$. After opening the sampling switches, the comparator can be clocked immediately to determine the polarity of the input. This speed enhancement comes with the drawback of increased sensitivity to parasitic capacitance. This is due to the additional unswitched capacitance on the SAR DAC outputs as shown in Figure 3.9. This extra capacitor $C_P$ will result in a gain error in the DAC transfer function.

Normally, SAR DAC switching magnitude for bit cycle $i$ with radix $r$ and resolution $N$ is defined by Equation 3.15. Adding an unswitched capacitor will change the switching magnitude to that defined in Equation 3.16. Careful layout can help minimize this parasitic effect, but the finite capacitor value will force the input swing to be reduced by the same factor $\epsilon$ to result in a sufficiently small signal to the back end quantizer.

$$V_{DAC,i} = \frac{V_{REF}}{r^i} \quad (i = 1 : N) \tag{3.15}$$

$$V_{DAC,i,\epsilon} = \frac{V_{REF}}{(r+\epsilon)^i} \quad (i = 1 : N) \tag{3.16}$$

### 3.5.2 Residue Amplifier

This work employs a residue amplifier based on the VTC described in Section 3.4.2. For this type of amplifier, bandwidth is of primary importance, whereas gain and output swing requirements are minimized by the nature of the system topology. Based on these requirements, a simple single stage Class-AB architecture is used as seen in Figure 3.10. This allows the $G_m$ to be the summation of both the NMOS and PMOS input pairs. The simulated low-frequency gain of 24 dB is sufficient to deliver the 7 bit reside. Switched capacitor common-mode feedback was chosen based on its compact implementation and low static power consumption. For added power efficiency, the amplifier and zero-crossing detector are disabled after the zero-crossing instant to minimize static power consumption.

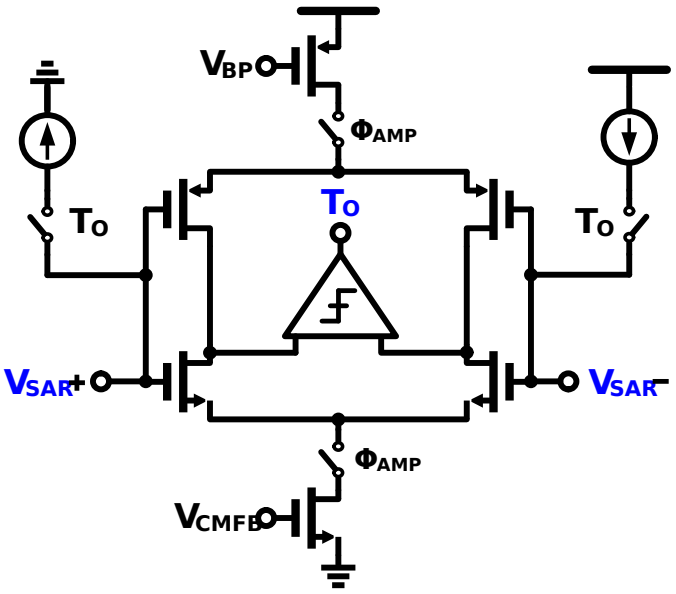


Figure 3.10: Voltage-to-time residue amplifier schematic.

### 3.5.3 Discharging Current Source

The ramp generating current source is the main determining factor for back end linearity of the proposed two-step architecture. A single-ended schematic of the V-T residue amplifier highlighting the current source is shown in Figure 3.11. Here the sampling capacitor is the entire SAR DAC array, whereas the feedback capacitor is a fixed value.

The two techniques used to ensure high linearity are the high resolution of the preceding SAR quantizer along with the virtual ground provided by the residue amplifier. The high quantization first stage can reduce the input swing to a small value defined by Equation 3.17. This amplitude of this swing is below 15 mV for this implementation. In addition to this small swing, the residue amplifier

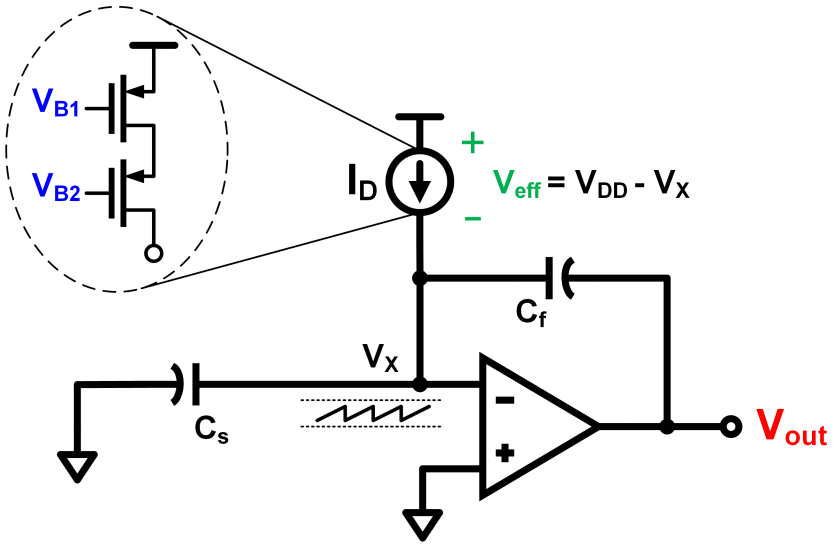


Figure 3.11: Discharging current source implementation.

negative feedback pushes the amplifier inputs toward virtual ground before the current source is switched on, further improving the linearity.

$$V_{Residue} = \frac{V_{REF}}{2^N} \tag{3.17}$$

### 3.5.4 Voltage-to-Time Gain Sensitivity

For a conventional residue amplifier, the closed loop gain is set by a capacitor ratio, resulting in a well-defined and predictable voltage gain. However, the V-T gain is set by the ratio defined in Equation 3.14. Variation of the current source magnitude can result in degraded performance if not calibrated. This work uses a one time start-up calibration to correct for static offset in the voltage and time domain paths. Figure 3.12 shows the effect of variations in the current magnitude.

The x-axis plots the ratio of the digital gain used in reconstruction $K_D$ to the actual analog gain value $K_V$. Results show that a variation of $\pm 3\%$ is acceptable to achieve 70 dB SNDR. Sensitivity to this variation can be reduced with the use of additional feedback loops to adjust the current value over PVT variations based on the total delay of the TDC full-scale reference $T_{FS}$.

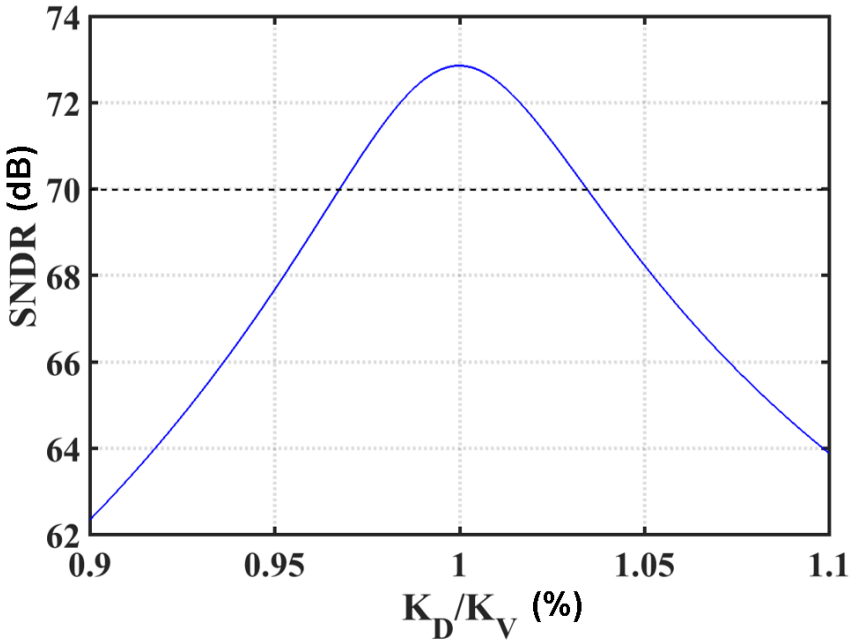


Figure 3.12: Voltage-to-Time residue amplifier gain sensitivity. $K_D$ is the digital reconstruction gain while $K_V$ is the actual gain from implementation.

### 3.5.5 Asynchronous Timing Control

While the entire ADC is synchronous, both the SAR feedback loop and the V-T conversion operate with asynchronous controls. Separate state machines exist

for the SAR and the V-T conversion blocks. The SAR control logic is shown in Figure 3.13. This creates a self-oscillating clock for reset and latching of the strong arm comparator. Asynchronous SAR eliminates the need for a high frequency clock generator and automatically adjusts the period for each bit trial by taking advantage of the signal dependent delay of the comparator in the feedback loop [46]. Additionally, the settling period for the DAC is adjustable through a variable delay on the comparator reset signal.

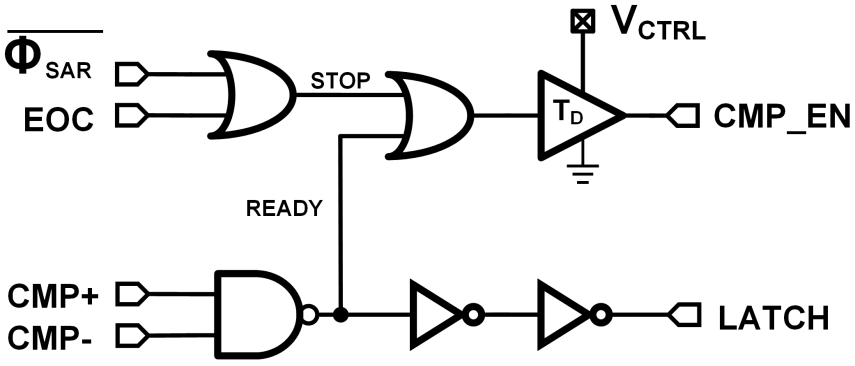


Figure 3.13: Asynchronous SAR Control Logic

The V-T conversion is also controlled by asynchronous digital logic. After the 7-bit SAR switching is complete ($\Phi_{SAR}$), the amplifier enable signal is asserted to begin charge transfer to the feedback capacitors. Following an adjustable delay, the zero-crossing detector enable signal is asserted, indicating the start of the discharge period. The delay between enable signals gives added time for residue pre-amplification. Along with a reduction of false positive zero-crossing events, this period also reduces the necessary bandwidth specification of the amplifier by providing more time for dynamic settling. Following the zero-crossing event,

both the amplifier and zero-crossing detector are power gated to avoid wasting power from additional static bias currents. The result of asynchronous controls is that ADC power consumption is primarily dynamic, making it suitable for a wide range of signal bandwidths. Figure 3.14 shows the measured ADC power consumption across sampling frequency. The linear trend shows that the power is mostly dynamic, with only a small absolute minimum power due to the unswitched bias network.

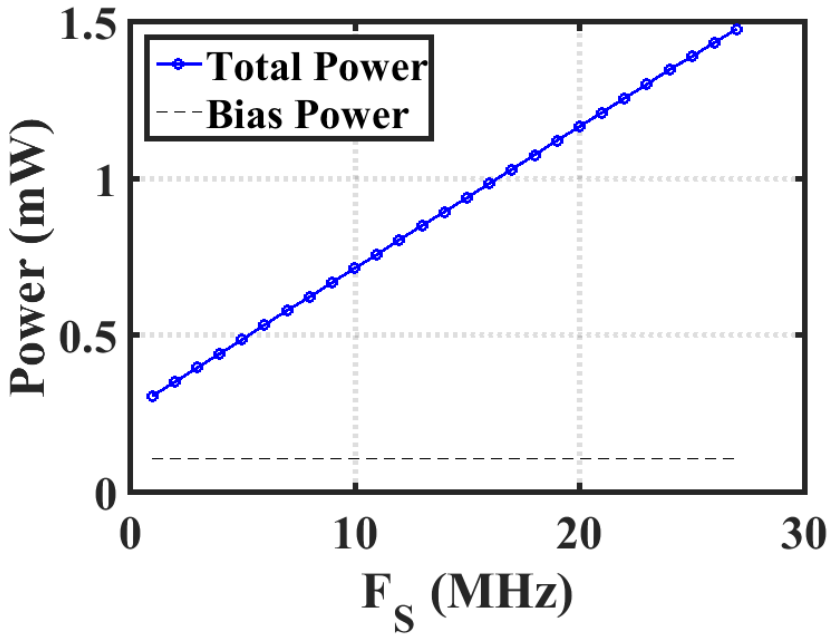


Figure 3.14: Measured ADC power consumption across sampling frequency.

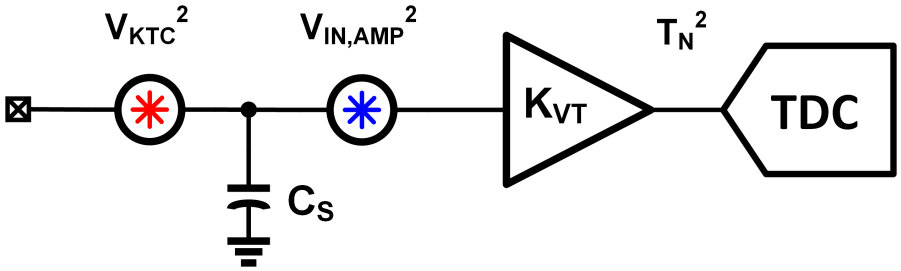


Figure 3.15: System level dominant noise sources.

### 3.5.6 Voltage-to-Time Noise

The major noise sources of the ADC are from sampling, amplification, and the quantization error. The dominant noise source of the V-T amplifier is from the current source. This is because the current source is directly connected to the sampling node, or the top plate of $C_S$. This current source noise is also integrated onto the feedback capacitor during amplification phase, adding sampling jitter to the time domain sampling instant. This time domain noise $T_N^2$ can be referred to the amplifier input by the V-T gain $K_{VT}$. A system level view of the dominant noise sources is shown in Figure 3.15, which includes this integrated amplifier noise when input-referred, and the standard thermal noise due to sampling. The amplifier noise can be approximated by a random walk process, where the variance increases as function of the integration time [47]. To increase the effective resolution of the back-end TDC there are two options, either reduce the unit time reference $T_{LSB}$, or increase the maximum time input $T_{FS}$. Reducing $T_{LSB}$ adds circuit complexity and power, and is limited by process technology. Increasing $T_{FS}$ directly trades off with the ADC bandwidth, and increases noise at the TDC input.

This V-T noise effect on SNR is shown in Figure 3.16 as a function of effective inter-stage gain $G_{EFF} = \frac{T_{FS}}{T_{LSB}}$. Also shown is the Signal-to-Quantization-noise Ratio (SQNR) of an ideal hybrid-domain ADC. This shows the fundamental tradeoff between voltage and time resolution. In this model, $T_{LSB}$ is constant and $T_{FS}$ is increased, allowing more time for TDC quantization. When $T_{FS}$ is short, the noise power from the V-T amplifier is low, but the total ADC SNR is limited by the quantization noise of the TDC. As $T_{FS}$ is extended, TDC quantization noise is suppressed while the integrated noise accumulates. The intersection point represents the gain for which quantization noise power is equal to thermal noise power. Considering this V-T noise and the 20 MHz sampling clock which limits the TDC operation to one half cycle, this work uses an effective inter-stage gain ($G_{EFF}$) of 64. This effective gain simplifies digital reconstruction, and suppresses quantization noise, making the ADC limited by thermal noise.

### 3.5.7 Time-to-Digital Converter

The flash TDC is designed using near minimum sized inverters and standard cell flip-flops as time comparators. A simplified circuit implementation is shown in Figure 3.17. As the V-T amplifier is operating, a DC level shift is applied to the final SAR residue voltage to guarantee a single ended residue. This allows a uni-directional current in the V-T stage, but also adds a DC component to the output pulse width ($T_O$). As this DC component increases, the input range of the TDC is reduced, limiting its effective resolution. This is corrected by adding

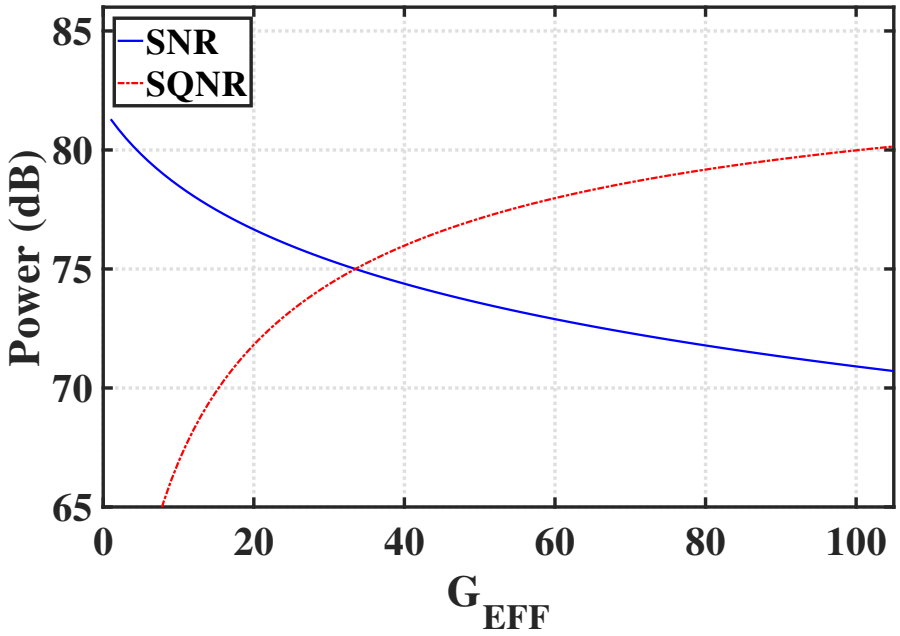


Figure 3.16: Noise tradeoff of the two-step voltage-time hybrid ADC. Increasing $T_{FS}$ allows more quantization levels by using more time. Alternatively increasing the integration window results in more noise at the TDC input.

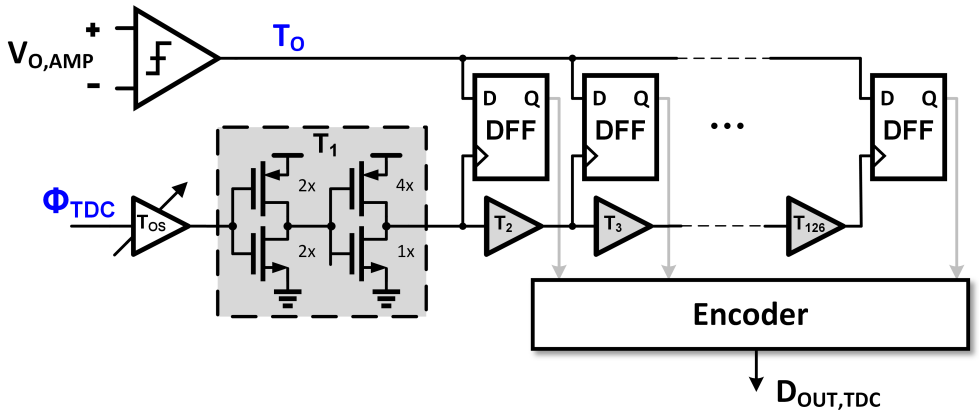


Figure 3.17: Delay line Time-to-Digital Converter circuit implementation.

a delay to the input of the delay line ($\Phi_{TDC}$), shifting all of the time references which clock the flip-flops. This simple modification allows control over the mean TDC output code through a one time foreground calibration, thus maximizing the effective TDC resolution.

## 3.6 Measurement Results

A proof-of-concept prototype was implemented in 180nm CMOS along with a testing PCB. The testing setup used for measurements is shown in Figure 3.18. The PCB setup utilized a motherboard for generating all bias currents, reference voltages, and supply voltages. This was connected to the daughter board which contained the ADC prototype chip, SMA inputs for clock and input signal, and output pins for the digital logic analyzer. All equipment used for generating signals and monitoring power consumption is also indicated in Figure 3.18.

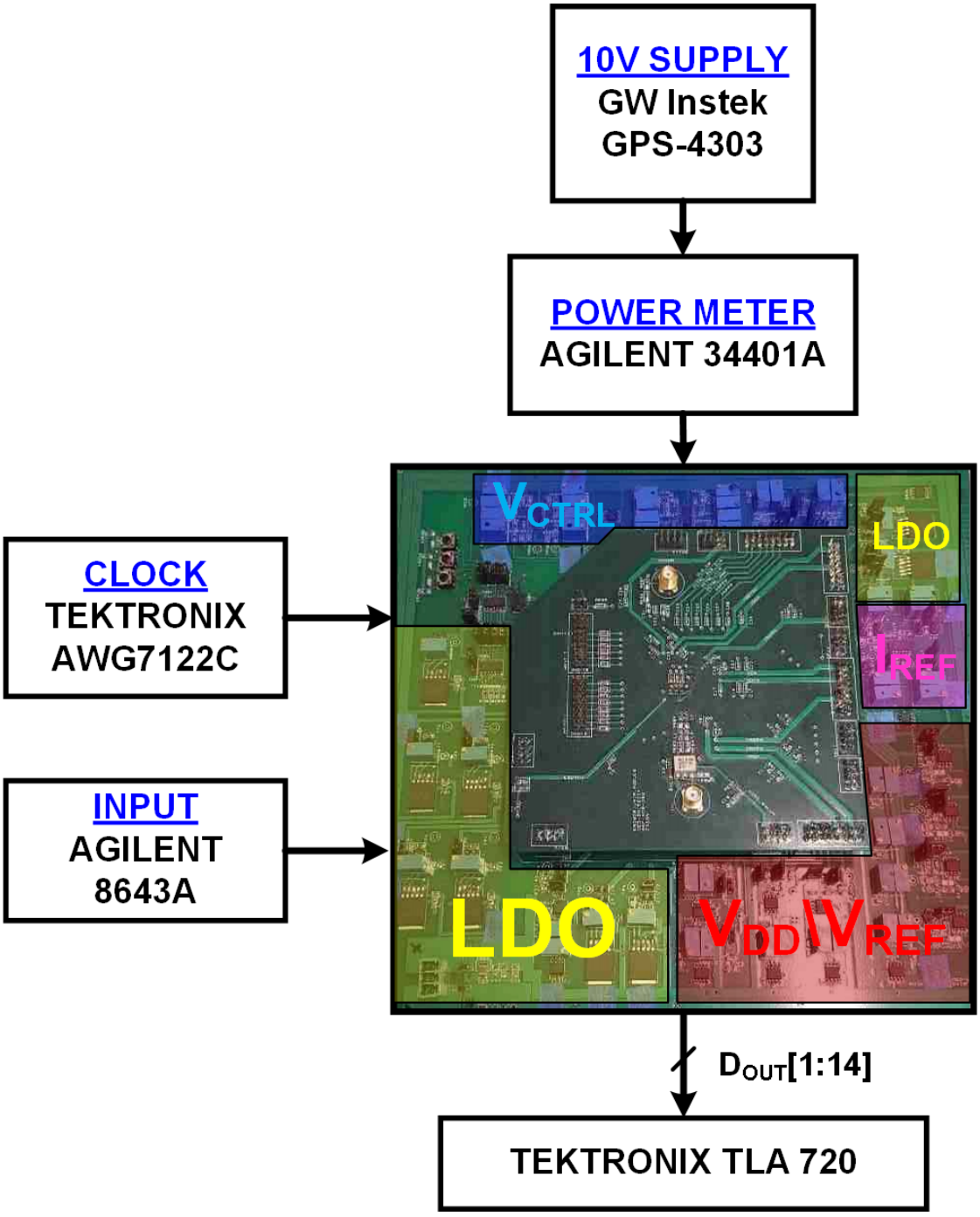


Figure 3.18: Testing Setup indicating hardware used for power, clocking, and input sources.

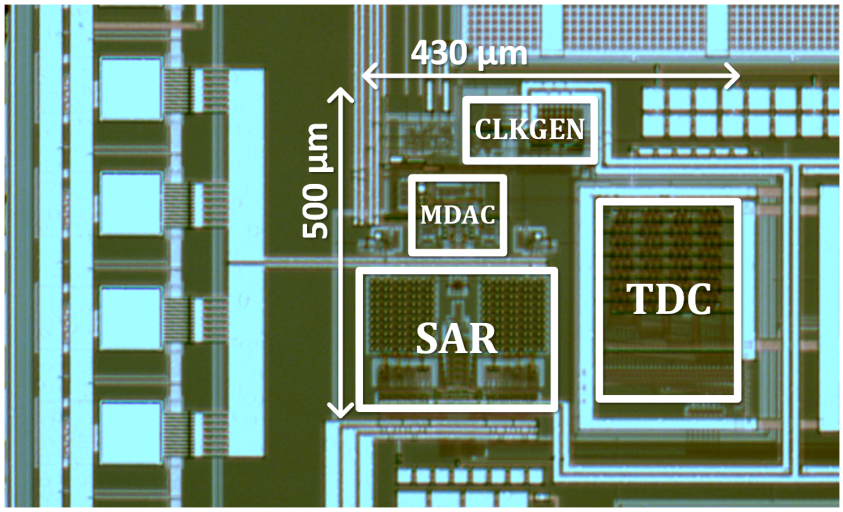


Figure 3.19: Die photograph showing the core ADC blocks.

Figure 3.19 shows a die photograph and lists the performance summary. The core ADC occupies 0.5 mm × 0.43 mm. Despite the low loop gain of the residue amplifier, a linear digital radix calibration applied off chip is sufficient to achieve over 11.8 effective number of bits (ENOB).

Figure 3.20 shows the measured histogram for a 0 V input signal. The variance of this code change can be used to calculate the input-referred noise as indicated in Equation 3.18. Using $N = 13$ and $\sigma_n^2 = 0.39LSB$, we arrive at the input referred noise of 73.3 dB, giving us the maximum possible resolution of the ADC.

$$SNR_{Input} = 10 * Log\frac{\frac{2^{2(N-1)}}{2}}{\sigma_n^2} \tag{3.18}$$

A detailed power breakdown by block is shown in Table 3.1. The analog and digital power consumption were 555 $\mu$W and 732 $\mu$W, respectively. This means that the majority of the power consumption is from digital blocks, whose efficiency

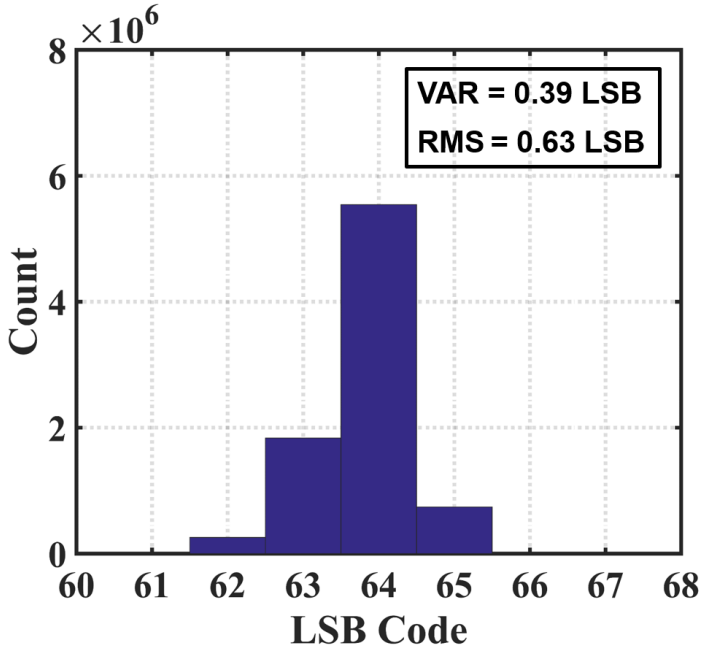


Figure 3.20: Measured histogram of digital outputs with 0 V (grounded) input.

is limited in 180nm, and is predicted to be reduced at the same rate as digital circuits if the same architecture were implemented in a smaller process node.

Figure 3.21 shows the measured dynamic performance for a 1 MHz input with 3 $V_{PP}$ input swing. The peak measured SNDR and SFDR were 73dB and 91.9dB, respectively. The 13-bit static linearity is shown in Figure 3.23. The maximum DNL and INL were +0.92/-0.79 LSB and +1.47/-1.47 LSB, respectively. To check performance drift over time, an additional test was conducted where the ADC was left running for several days without re-calibration. The results show consistent performance as seen in Figure 3.24.

Table 3.1: SAR-TDC Power Breakdown

| Supply | Voltage (V) | Power (uW) |
|---|---|---|
| Analog | 1.5 | 287 |
| Digital | 1.4 | 398 |
| TDC | 1.0 | 335 |
| Switch | 1.8 | 128 |
| Reference | 1.6 | 140 |

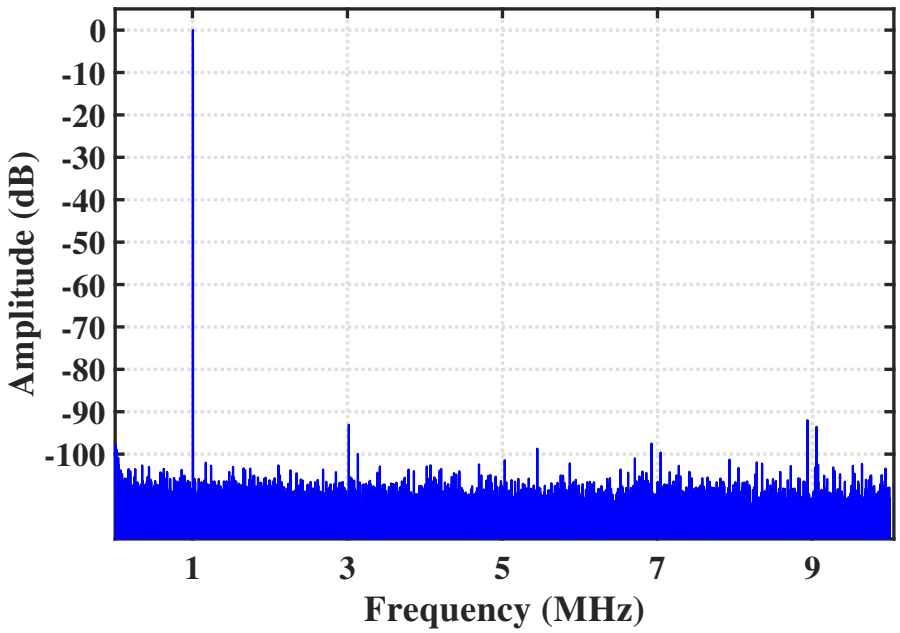


Figure 3.21: Measured dynamic performance with $f_{in} = 1$ MHz.

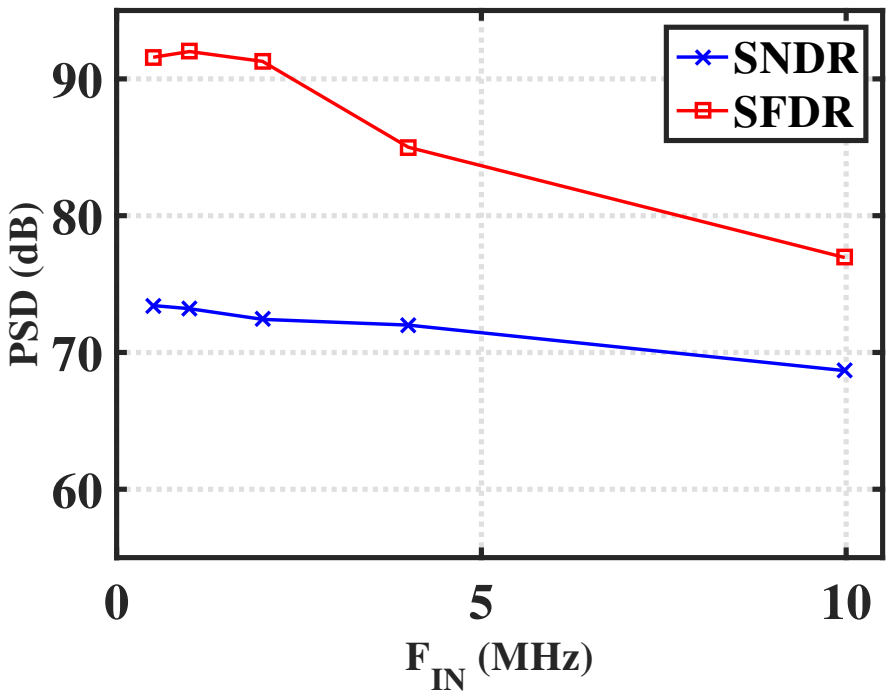


Figure 3.22: Measured dynamic performance across $f_{in}$ to the Nyquist input rate.

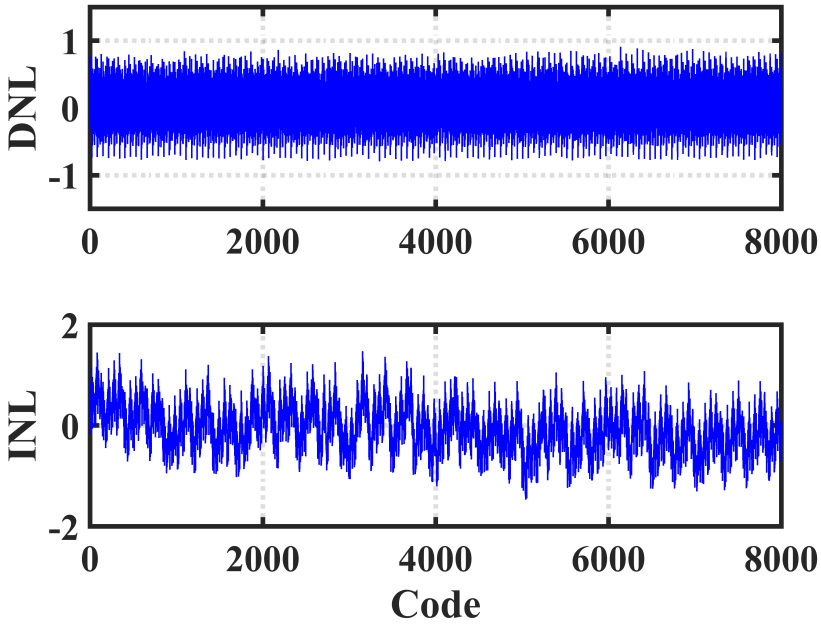


Figure 3.23: Measured static linearity.

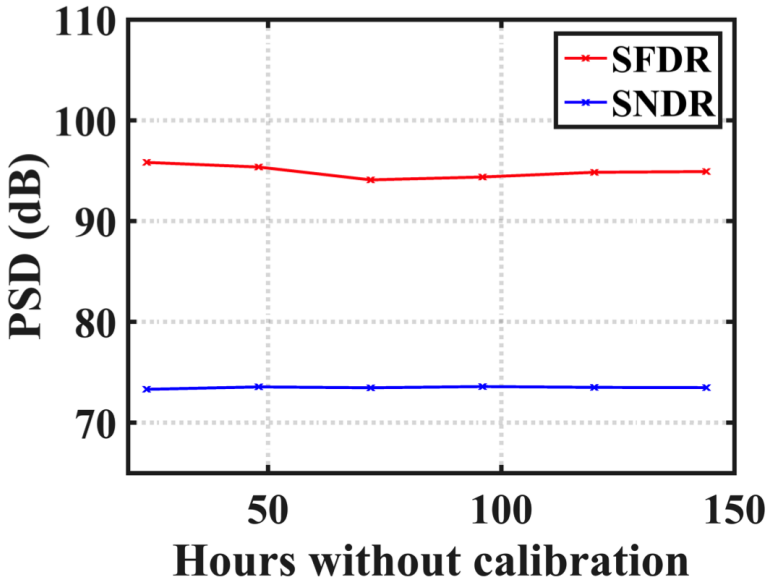


Figure 3.24: Free Running test without calibration.

## 3.7 Conclusion

This chapter presents a two-step ADC technique and proof-of-concept prototype. The primary goal is to design a mostly digital ADC which can effectively scale into sub-micron CMOS. Measurement results show a high efficiency design which uses simple voltage quantization for coarse bits, and time quantization for fine bits. A V-T residue amplifier relaxes gain and linearity specifications compared to a conventional amplifier approach.

Table 3.2 shows a comparison among recent high efficiency publications. Although there are several works which achieve high bandwidth with superior power efficiency [36, 37, 41], they are also based in deep sub micron CMOS, and therefore exhibit speed and area advantages. This table highlights designs with a process technology of 90nm and larger for a straightforward comparison. The proposed ADC has state-of-the-art performance for resolutions above 70 dB SNDR and greater than several MHz bandwidth.

Figure 3.25 shows a comparison with recently published state of the art works from [48]. An modified version of the survey is shown in Figure 3.26 which only shows other published results in 180nm technology. This work contributes a highly digital and future scalable technique that can be applied in high resolution applications using deep sub micron technologies.

Table 3.2: SAR-TDC comparison with prior art

| Specification | **This Work** | [42] | [43] | [49] | [50] |
|---|---|---|---|---|---|
| Architecture | **2 Step SAR-TDC** | V-T Pipeline | 2 Step SAR-VCO | SAR | 2 Step SAR-SAR |
| Technology [nm] | **180** | 130 | 180 | 90 | 130 |
| Area [$mm^2$] | **0.22** | 0.5 | 0.4 | 0.01 | 0.24 |
| $F_S$ [MHz] | **20** | 70 | 35 | 50 | 30 |
| Power [mW] | **1.28** | 6.38 | 3.5 | 4.2 | 2.54 |
| SNDR [dB] | **73.1** | 69.3 | 70 | 71 | 70.4 |
| SFDR [dB] | **91.9** | 80.6 | - | 85 | 79.6 |
| $FOM_W$ [fj/c-s] | **17.4** | 38.2 | 272 | 28.7 | 31.3 |

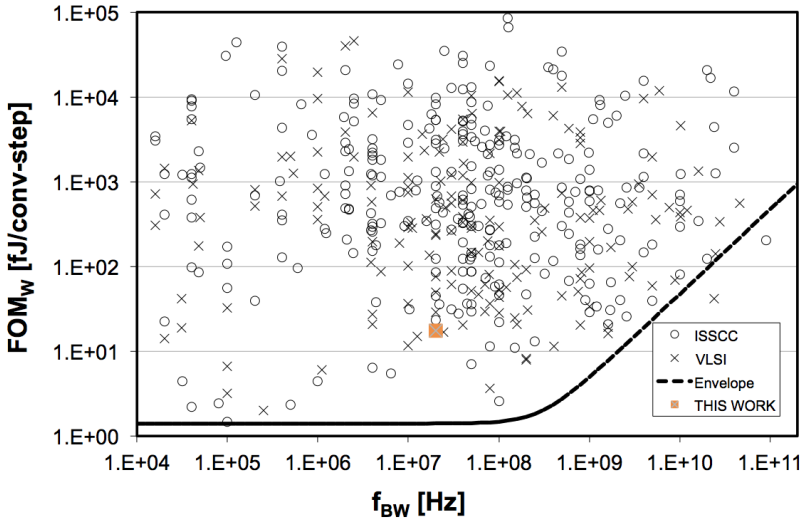


Figure 3.25: Walden figure of merit plot comparing proposed work with state of the art [48].

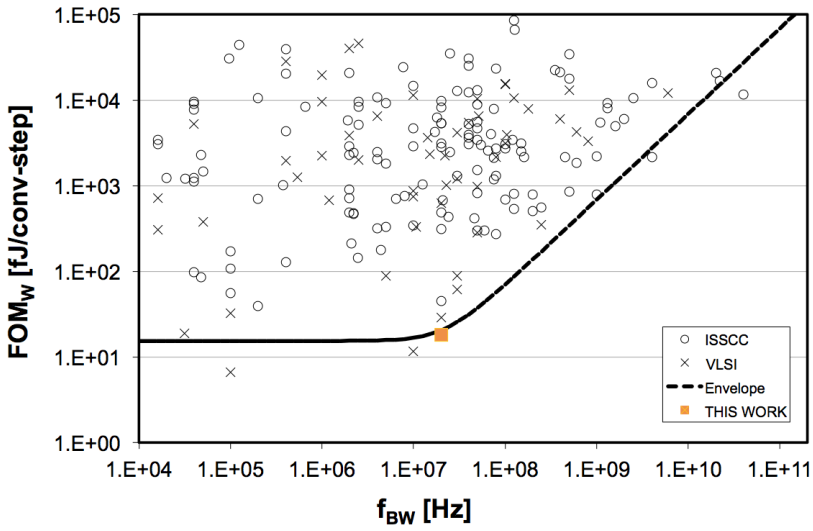


Figure 3.26: Walden Figure of Merit plot comparing proposed work with state of the art in 180nm technology [48].

# Chapter 4: A Synthesized Stochastic ADC

> "It is the struggle itself that is most important. We must strive to be more than we are. It does not matter that we will not reach our ultimate goal. The effort itself yields its own reward."
>
> — *Gene Roddenberry*

A major difference between analog and digital circuit design is evident when existing systems must be ported to a new technology node. Because digital systems have a low sensitivity to physical layout, design automation tools allow for rapid prototype development from simplified behavioral instructions.

Analog-to-Digital Converters are one mixed signal block which contains a combination of analog and digital sub-systems. While the digital pieces can be automatically re-synthesized, the analog sections must be manually designed and carefully laid out. This is a time consuming step to achieve the desired resolution and speed. To take full advantage of next generation CMOS, it is vital to develop techniques that speed up the development cycle for the analog portions of a mixed signal ADC design.

The goal of this chapter is to discuss the possibility of automating the design and layout of a moderate resolution ADC using circuit synthesis tools that operate

with verilog source code. A stochastic approach is combined with rudimentary analog and digital standard cells to achieve high resolution and bandwidth for an automatically synthesized design. This technique allows analog designers to take advantage of the large collection of digital design tools to reduce total design effort.

## 4.1 Prior Synthesized ADCs

The most important factor for automating the design of an ADC is selecting an architecture which lends itself well to the synthesis process. These architectures can best be described as pushing more computation into the digital domain. To automate analog circuit design, there are two basic avenues:

1. Emphasize highly digital data converter architectures.

2. Use digital design tools to implement analog systems.

A combination of these approaches can be used to create new design paradigms which leverage computational processing and intelligent design decisions to automate analog circuits with less overhead.

### 4.1.1 Synthesis Friendly Approach

One popular approach is to create highly-digital ADCs like those discussed in Chapter 2. The use of time-to-digital converters is appealing because a quantizer can be implemented with simple inverters and D-type Flip Flops. One limitation

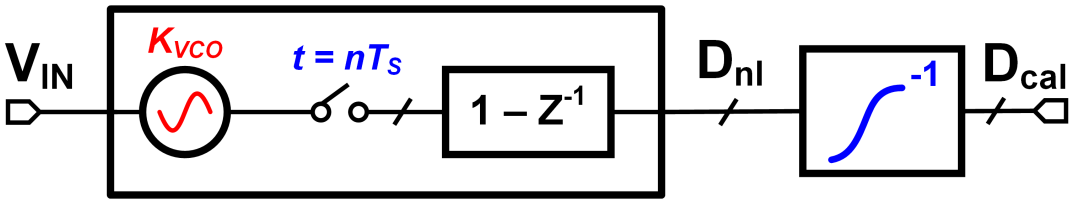


Figure 4.1: Open loop VCO quantizer with digital non-linearity calibration used in [52].

to this approach is that a time domain signal is required. A VTC is usually implemented with an analog-intensive solution such as a feedback amplifier or integrator.

Use of a VCO has been proposed to form a highly digital quantizer[33] [51]. The cyclical nature implements an implicit barrel shift to shape the quantization noise. Full rail-to-rail switching can also offer advantages in noisy, low-supply applications.

The work in [52] creates a digitally-intensive, continuous time $\Delta\Sigma$ ADC based on a VCO quantizer. The block diagram shown in Figure 4.1 shows how a VCO is followed by a inverse function which attempts to undo the VCO non-linearity. In this case, calibration for VCO non-linearity delivers an SNDR of 78 dB without the use of conventional analog integrators, comparators, voltage references or a feedback DAC. Analog circuit minimization is a critical aspect of a successful synthesized ADC. By using an open loop VCO and primarily digital blocks, this technique results in low power consumption and small area. This approach is expected to improve with future process scaling, but was ultimately implemented with a manual layout to achieve this level of performance.

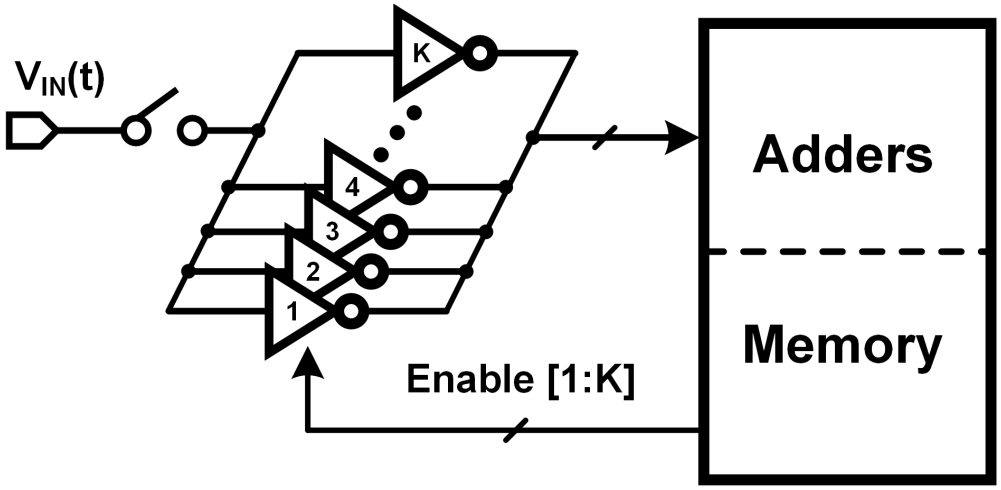


Figure 4.2: Low-voltage redundant flash ADC used in [53].

Another highly digital ADC was proposed in [53] in which random variations can be tolerated. For this concept, an array of inverters are connected in parallel and used as analog comparators as shown in Figure 4.2. The area and power consumption are reduced by using small size inverters and by operating at a supply voltage near the transistors threshold voltage $V_{TH}$, respectively. These techniques inevitably increase mismatch, degrading overall linearity performance. Additional digital signal processing is leveraged to improve linearity by only enabling a subset of the large array of redundant comparators rather than forcing a precise transfer function through conventional sizing and offset cancellation. Low power and design automation are possible with this strategy, but an area overhead is required to create the redundant thresholds which are eventually unused and only serve to increase parasitic capacitance and area.

### 4.1.2 Digital Standard Cells

Stochastic ADCs are a prime candidate for data converter synthesis. The automatic place-and-route techniques used will inevitably result in large mismatch due to the asymmetric loading and variable edge effects. Conventional ADCs using explicit reference signals experience large errors from these effects, whereas stochastic ADCs actually require circuit mismatch to create implicit references. Eliminating the analog reference is another key enabler for automating ADC design.

#### 4.1.2.1 Stochastic Background

As opposed to simply tolerating mismatch by disabling undesirable contributors, a stochastic ADC uses random variations to create various analog references used in quantization [54]. The basic idea behind stochastic a ADC is that a set of simple, redundant quantizers can be used to improve SQNR if the dominant noise source is uncorrelated. The SNR is defined in Equation 4.1, where the noise power is composed of various sources defined in Equation 4.2.

$$SNR = 10 \cdot \log(\frac{P_{Signal}}{P_{Noise}}) \tag{4.1}$$

$$P_{Noise} = P_{thermal} + P_{offset} + P_{qe} \tag{4.2}$$

For a moderate resolution ADC, the quantization noise power can be much larger than the rest, so the total noise power can be approximated by this dominant

noise source. The resulting in the SNR defined in Equation 4.3.

$$SNR \approx SQNR = 10 \cdot \log(\frac{P_{Signal}}{P_{qe}}) \tag{4.3}$$

Building a conventional quantizer by arranging K ADC channels in parallel and summing the digital outputs can increase the signal power in the digital outputs, but the dominant noise contributor (quantization errors) are also fully correlated for well matched quantizers. This results in no improvement in the SNR, and comes at the cost of K times the area and power consumption.

Stochastic ADCs instead exaggerate one of the noise sources, usually through device sizing, such that the dominant noise sources are uncorrelated. Recall that for correlated signals, the power ($P_{corr}$) can be calculated by squaring the sum of voltages as shown in Equation 4.4.

$$P_{corr} = (V_1 + V_2 + ... + V_K)^2 \tag{4.4}$$

For uncorrelated signals, the total power ($P_{uncorr}$) is defined by Equation 4.5

$$P_{uncorr} = V_1^2 + V_2^2 + ... + V_K^2 \tag{4.5}$$

Therefore, by adding correlated input signals which contain uncorrelated noise sources, we arrive at the following SQNR for a stochastic ADC using K redundant quantizer channels.

$$SQNR_{stochastic} = 10 \cdot \log(\frac{K^2 \cdot P_{Signal}}{K \cdot P_{Dominant}}) = 10 \cdot \log(\frac{K \cdot P_{Signal}}{P_{Dominant}}) \quad (4.6)$$

#### 4.1.2.2 Prior Stochastic Implementations

The work in [55] uses a comparator cell that is built intentionally small to increase the decision point distribution between parallel comparators. This technique makes the comparator offsets uncorrelated and the $P_{offset}$ from Equation 4.2 becomes the dominant noise source. The number of comparators $n$ required to achieve $N$ bit resolution was described in [55] as shown in Equation 4.7. This is in stark contrast to the same equation for a standard flash shown in Equation 4.8. The conventional flash requires far fewer comparators for the same resolution, but also requires well matched (and therefore larger area with high power consumption) comparators.

$$n_{stochastic} \approx 2 \cdot 4^N \quad (4.7)$$

$$n_{flash} = 2^N - 1 \quad (4.8)$$

The resulting ADC was capable of SNDR of 33.6 dB, but was limited to a relatively small input range of 280 mVpp due to the highly non-linear Gaussian distribution of the comparators used. Linearization must be implemented to acquire a desirable transfer characteristic when the random variable cumulative distribution function (CDF) follows a Gaussian distribution, which can be described by Equa-

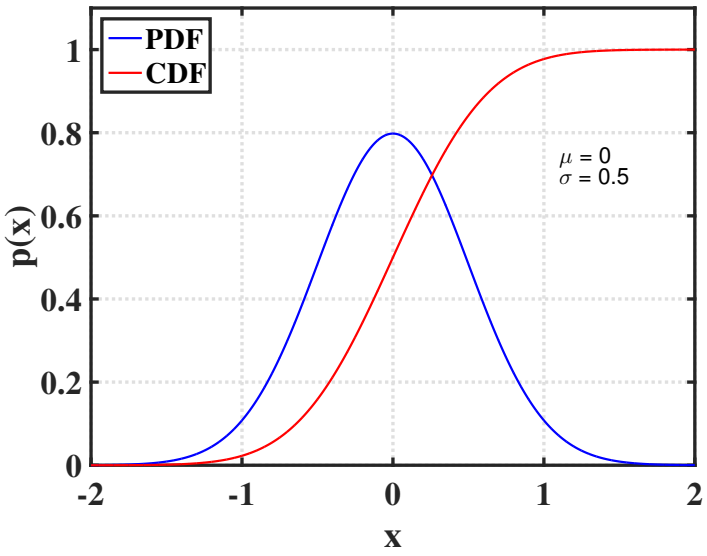


Figure 4.3: PDF and CDF for a Gaussian (normal) distributed random variable.

tions 4.9 and 4.10 and is shown in Figure 4.3. Larger input swings are possible, but would require either a digital linearization block or more comparator groups with different global mean offsets through additional analog reference voltages.

$$CDF_{Gaussian}(x) = \frac{1}{2}\left(1 + \text{erf}\left(\frac{x-\mu}{\sigma\sqrt{2}}\right)\right) \tag{4.9}$$

$$\text{erf}(x) = \int_{-\infty}^{x} \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(u-\mu)^2}{2\sigma^2}} du. \tag{4.10}$$

[56] uses a stochastic approach to create a highly digital flash ADC with a bank of parallel comparators similar to [55]. This ADC was fully described with verilog code by using cross-coupled NAND gates for the analog comparator function. Here again, the Gaussian distribution of comparator trip points was used to create

implicit references. This work used an inverse-Gaussian look up table to roughly match the slope of the Gaussian CDF in different code regions. A higher order look up table could improve linearity, but would also require more power and area in the digital back end implementation to more closely approximate the curve.

[57] presents a reconfigurable stochastic, which attempts to use digital reference generation to create a linear transfer function. Comparator offsets are controlled by digitally re-configuring composite NAND cells to change the standard deviation of their offset. This avoids the requirement of analog references to spread the random distributions, but again has limited resolution in actual implementation.

Using verilog input, these stochastic methods allow a design to be re-implemented relatively quickly when migrating to a new process technology. Despite this portability aspect, the application space is limited to low resolution or low speed targets due to the difficulty in creating an ideal estimator for a Gaussian noise source [58].

### 4.1.3 Analog Standard Cells

One way to attain higher resolution from a synthesized design is to expand the scope of a verilog based design by adding a set of basic analog cells to perform linear circuit functions. The work in [59] proposes the use of rudimentary analog cells alongside the digital standard cell library to improve the architectural limitations of previous stochastic ADCs used in all-digital synthesis. A typical digital design flow is modified by adding several analog cells as shown in Figure 4.4.

This technique showed much higher resolution and greatly expanded the scope

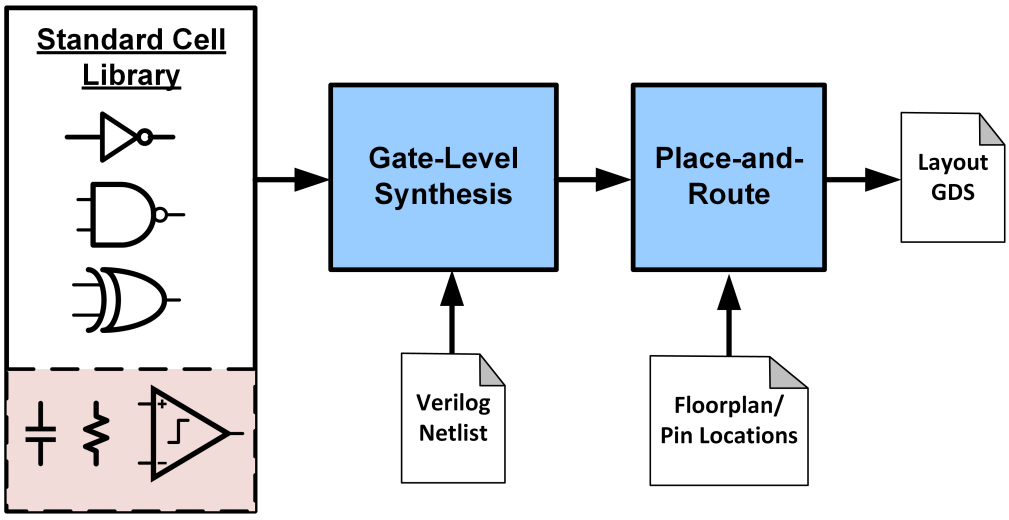


Figure 4.4: Digital design flow with additional analog standard cells shown in pink [59].

of synthesized ADCs. Here the authors created an oversampled 1-1-1 MASH ADC with simplified analog integrator cells, which was fully defined in verilog code. This code was then used to generate the same ADC in 2 process nodes (130nm and 65nm CMOS), showing a high resolution of 56dB SNDR, but was also limited to a bandwidth of 2 MHz.

The spectrum of the synthesized ADC showed a larger than expected second-order distortion. It was found through simulation that the ADC contained a small parasitic capacitor that asymmetrically loaded the virtual ground of an integrator [60]. This illustrates a key drawback to using digital tools to create analog systems, the concept of circuit symmetry. This work elected to sacrifice design control for rapid portability, allowing non-symmetric loading of critical analog nodes to reduce design time.

## 4.2 Proposed Synthesized ADC

For a synthesized ADC, sensitive analog circuits like amplifiers or integrators should be avoided to minimize the impact of asymmetric parasitics from automatic place-and-route. This obviously limits the maximum resolution possible. Building off the previous works discussed in Section 4.1, stochastic techniques are well suited for the synthesis process because they do not require an external reference, and offer a way to increase resolution without requiring amplification. They are limited however by the nonlinear CDF of the dominant noise source. This noise source useded in prior works has primarily consisted of thermal noise [61, 62], or device offset [56, 57] distributions.

### 4.2.1 Spatial Averaging

The work in [63] proposed the use uniformly distributed quantization errors to provide stochastic operation. This is possible when using mismatched VCO quantizers (VCOQ). First, recall that the VCO output phase is defined as shown in Equation 4.11. This means that the VCO accumulates phase based on the voltage input, free-running frequency $f_{osc}$, and the voltage-to-frequency gain $K_{VCO}$.

$$\Phi(t) = \Phi(0) + 2\pi \int_0^{\infty} f_{osc} + V_{in}(t) K_{VCO} \; dt \tag{4.11}$$

Consider configuring two VCOQ in parallel as shown in Figure 4.5. After they are reset, their initial output phase is identical and zero. During the first sev-

eral conversion cycles, the phase quantization errors $\Phi_{qe_i1,2}[n]$ are fully correlated. Given that the two VCOQ contain mismatch, their center frequency $f_{osc,i}$ will be different, and therefore they will accumulate phase at different rates. After a sufficient number of cycles, the quantization errors become fully uncorrelated. This is the condition required for a stochastic noise source. Greater levels of mismatch only serve to meet the uncorrelated condition in fewer number of cycles.

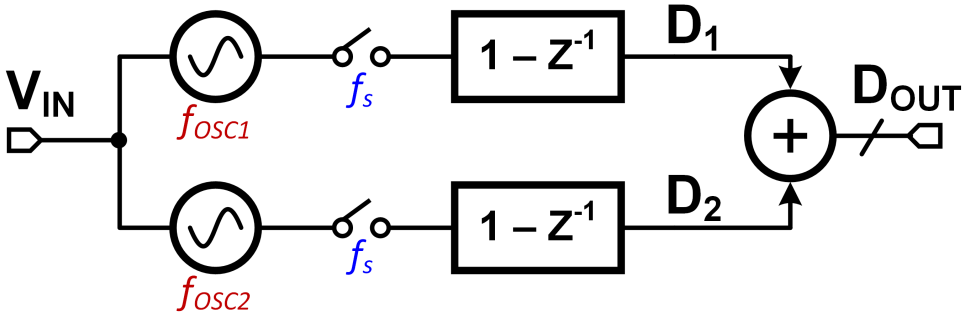


Figure 4.5: Two Channel VCO Quantizer with spatial Averaging Factor K = 2.

A simulation of this idea was carried out in MATLAB/SIMULINK. Here the multi-channel VCO was simulated with center frequency mismatch of 20% and the digital output stream from the single, and multi-channel summed output are analyzed with a FFT. Figure 4.6 shows that the SQNR can be improved by using redundant VCOQ with center frequency mismatch. The SQNR improvement is equal to $10 \cdot log(K)$.

By using the quantization error as the dominant noise source, the hardware implementation of an ideal estimator is greatly simplified due to the uniform quantization error. The simplicity of estimating a uniformly distributed random noise

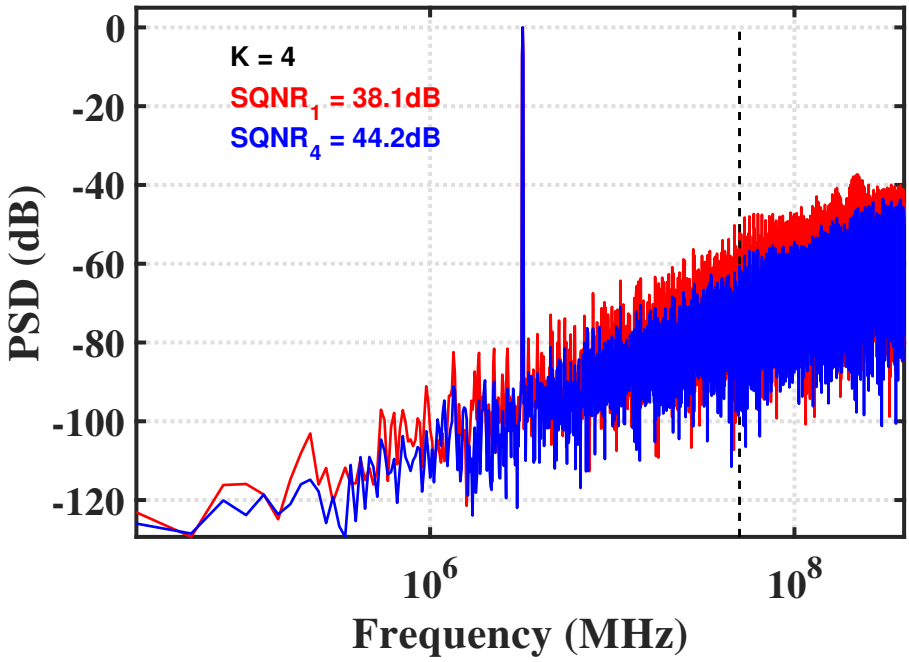


Figure 4.6: Simulink simulation of spatial averaging concept.

is apparent when examining the PDF and CDF, shown in Figure 4.7.

A fully custom prototype was designed and implemented in 180nm CMOS in [64]. In this stochastic ADC, a simple digital adder can be used to form the ideal estimation engine. Reference [64] was the first implementation of this spatial averaging using open-loop VCO quantizers, showing a high bandwidth of 50 MHz with a low OSR of 8 and SNDR of 54 dB. The bandwidth of this technique could be improved, but was limited by the speed of digital adders in the estimation engine.

This tactic produces an ADC which contains no explicit reference signals, feedback DACs, analog amplifiers or integrators. Additionally, the open-loop VCO is capable of high speed, while also providing first-order noise shaping. Based on

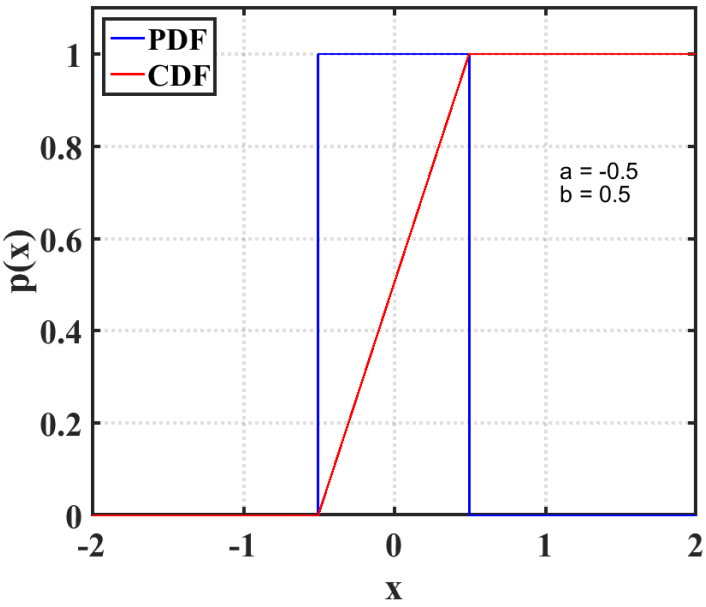


Figure 4.7: PDF and CDF for a uniform distributed random variable.

these advantages, the quantization error based stochastic ADC is a prime candidate to synthesize a wide bandwidth, moderate resolution ADC from verilog code.

## 4.3 Synthesis Specific Considerations

### 4.3.1 Cell Creation

Augmenting the digital standard cell library with custom cells can be performed by creating a minimalist set of analog blocks. The process described in [60] was used for the custom cells required in this design. The only analog section of this design is the ring oscillator, which is designed with a differential delay cell.

To fully integrate the analog cells into the digital design flow, careful consideration must be placed into the size and location of the analog I/O pins. To ensure high levels of analog and digital integration and to minimize routing conflicts, the existing digital routing pitch rules should be used. As with digital cells, the analog I/O should fall onto the existing grid locations, as shown with red **X**'s in Figure 4.8.

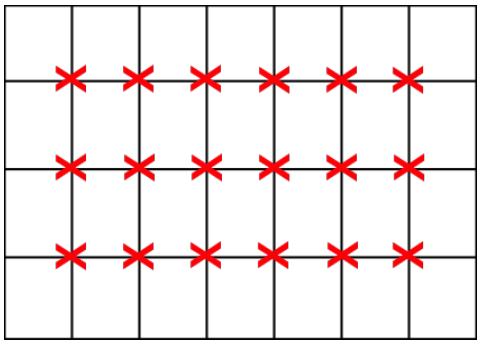

Figure 4.8: Routing pitch for digital cells that must be matched for the analog counterparts.

There is an additional limitation to using analog cells within a digital synthesis flow. As described in [60], asymmetric coupling can cause excessive distortion. Two techniques can be used to address this. The first is to simply create a stricter set of routing obstructions in your LEF library file. A second technique is to simply create larger analog cells, which include an unused region to minimize coupling. An example cell is shown in Figure 4.9 in which $W_A$ is added to reduce parasitic coupling, but also to meet DRC rules when mixing different threshold devices. Both of these techniques inevitably increase the overall silicon area used, which can cause a reduction in speed. This analog overhead is acceptable, giving the

modest specifications of the target ADC desired and the general trend of geometry scaling for advanced CMOS.

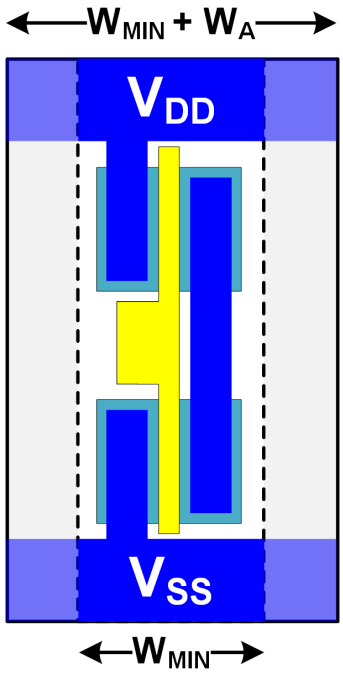


Figure 4.9: A simple cell with both the minimum width $W_{MIN}$ and the additional width due to analog overhead $W_A$.

### 4.3.2 Netlisting

The use of verilog implementation allows highly flexible netlisting abilities. The following example code snippet in Figure 4.10 shows how a **FOR** loop can describe a ring oscillator which is defined by the input parameter N to control the number of phases. Similar loops can be used to implement the quantizer array, and first-order difference block.

ringOSC.v

```
 1 module ringOSC(input vctrl,
 2                input init,
 3                parameter N=15,
 4                output [1:N] phip,
 5                output [1:N] phin
 6                );
 7
 8   delay_cell U1( .CTRL(vctrl),
 9                  .VIN(phin[N]),
10                  .VIP(phip[N]),
11                  .VON(phip[1]),
12                  .VOP(phin[1]) );
13
14   generate
15     genvar i
16     for (i=1; i<N; i=i+1) begin :  ROSC
17       delay_cell U2( .CTRL(vctrl),
18                      .VIN(phin[i]),
19                      .VIP(phip[i]),
20                      .VON(phip[i+1]),
21                      .VOP(phin[i+1]));
22     end
23   endgenerate
24
25 endmodule
```

Figure 4.10: Code snippet showing a FOR loop method for creating a ring oscillator.

### 4.3.3 System Planning

A floor plan can be used to define approximate locations of sub-systems of a design. The number of hierarchical levels used is a design tradeoff where deeper levels of floor planning could improve speed or reduce power thanks to more direct routing, but will also sacrifice portability. The floor plan used in this design is made intentionally simple to allow the synthesizer to freely place cells without input from the designer. This design freedom comes in large part from the highly digital and stochastic properties of the chosen architecture.

Driving the clock signals for the digital logic is a difficult task, but is made much simpler by the synthesis tools. As opposed to setting the location of each local non-overlapping clock generator with a floor plan, this design elects to use a clock mesh approach to operate the digital circuits. The clock mesh results in larger load capacitance, but also limits clock skew between digital logic leaf cells.

Pin locations of sub-modules is also important for synthesized ADC optimization. The synthesizer places output cells as close as possible to their respective pin locations. Use of pin spacing based on unit-cell dimensions can greatly limit routing effort and congestion for high speed nets. These pin locations are explicitly set with variables inside the *placeandroute.tcl* configuration file.

### 4.3.4 Symmetry

Moderate to high resolution ADCs typically employ differential circuits to improve the power supply rejection and reduce even order distortion terms. Prior analog

synthesis techniques used symmetry at the *cell* level to mimic a custom layout. In this work, we instead employ symmetry at the *system* level to guarantee sufficient matching.

This ADC uses a pseudo differential VCOQ in each spatial averaging channel. While mismatch between adjacent stochastic quantizers is acceptable, mismatch between differential half-circuits is not desirable. The entire differential quantizer can be described in verilog and synthesized. With this method, there is no guarantee that the cell placement will even remotely match the appropriate cell in the complementary half-circuit, resulting in poor supply rejection and even order distortion.

The alternative approach used in this design is to only define a half-circuit in the input verilog file. Next, we can simply re-use the synthesized VCO half-circuit for each half. This macro cell re-use can minimize differential mismatch and therefore limit even order distortion terms.

### 4.3.5 Background Harmonic Calibration

Because the proposed ADC uses an open-loop VCO, voltage-to-frequency non-linearity can limit the input swing. A non-linear system with $n^{th}$ order distortion coefficients can be modeled as shown in Equation 4.12, where $D_O$ is the non-linear digital output, and $D$ is the desired linear output.

$$D_O = D + \alpha_2 D^2 + \alpha_3 D^3 + ... + \alpha_n D^n \tag{4.12}$$

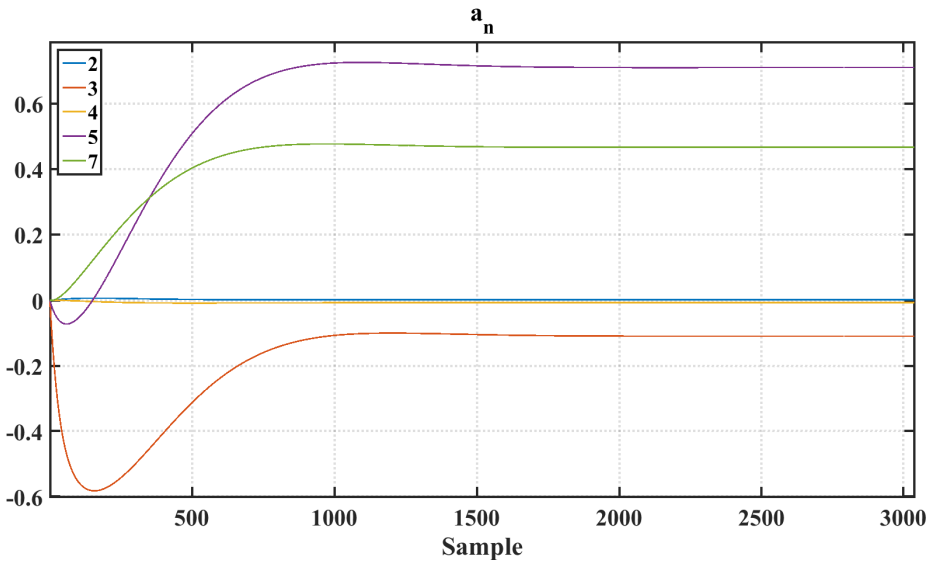


Figure 4.11: Blind background calibration coefficient convergence.

These distortion terms limit the SFDR and SNDR performance of analog systems. The spatial averaging technique only acts to reduce noise, but does not change the distortion performance. A highly digital blind background calibration was proposed in [65] for cancellation of VCOQ non-linearity. This technique is based on concepts of down-sampling and orthogonality to form a least-mean-squares error minimization loop to estimate the nonlinear coefficients. Figure 4.11 shows the algorithm being applied to a Monte Carlo simulated VCOQ with device mismatch, to calibrate the non-linearity from harmonics at 2,3,4,5, and 7 times the input frequency. With a $\mu = 0.5$, the coefficients can converge within 3000 cycles from reset.

Once these coefficients are estimated, a calibrated output can be computed by evaluating the linearization function in Equation 4.13.

$$D_{CAL} = D_O - \alpha_2 D^2 - \alpha_3 D^3 - ... - \alpha_n D^n \tag{4.13}$$

This design elected to use this calibration method to handle VCO non-linearity due to its highly digital approach and ability to cancel distortion of multiple terms simultaneously.

## 4.4 Circuit Implementation

The proposed system block diagram is shown in Figure 4.12. The ADC uses eight pseudo-differential VCOQ channels and a digital estimation engine to calculate the raw digital output, which is then sent off-chip for the non-linearity calibration. Each VCO output is sampled at the full clock speed of $f_S = 800MHz$. The design for the unit VCOQ is based on the analysis and equations shown in [66]. The VCO used is comprised of 15 delay stages which use a simple structure with weak positive feedback, shown in Figure 4.13. This provides sharp signal transitions, but also allows a large range of control inputs without largely impacting the delay cell output amplitude.

The cell used to quantize VCO phase is a conventional sense-amplifier flip-flop shown in Figure 4.14. This primary latch shown is sent to a slave latch before being sent to the digital estimation engine.

The digital back end is comprised of the first-order difference, thermometer-to-binary conversion, and the spatial averaging estimator. The speed of these systems is limited in 180nm, and high $F_S$ was desired to maximize OSR. Therefore, a 4x

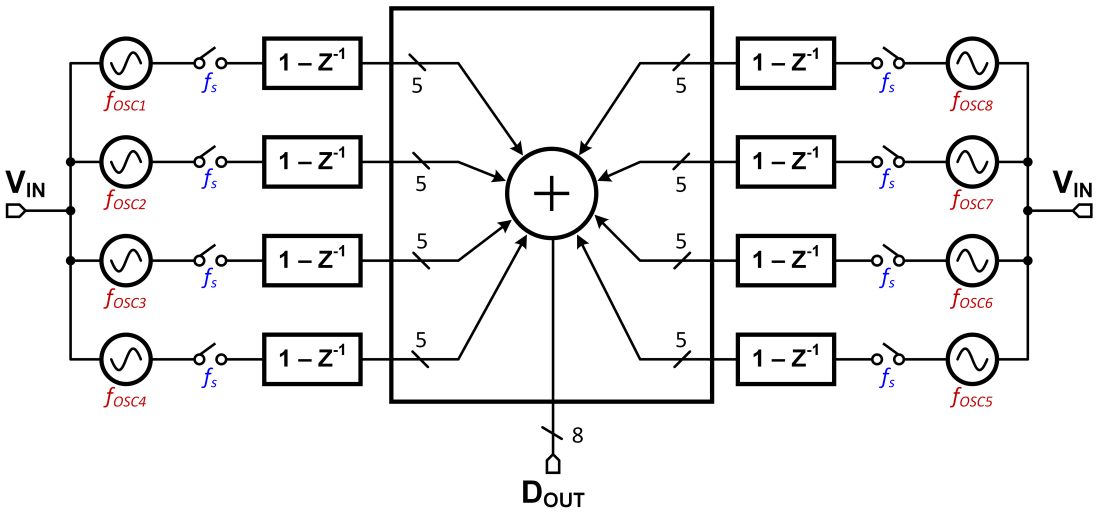


Figure 4.12: Stochastic Spatial Averaging VCO block diagram.

time interleaved digital back end was selected to reduce the speed of the digital to $\frac{F_S}{4} = 200MHz$.

## 4.5 Results

The described ADC was designed and synthesized in 180nm CMOS. The core ADC comprised of the VCOQ (x8) and the digital estimation engine was synthesized from verilog code. The complete ADC core is shown in Figure 4.19. The overall dimensions are 720 $\mu$m by 1050 $\mu$m. The large area is due to the use of 4x time interleaving in the estimation engine as well as a relatively low 60% core utilization setting in synthesis configuration. This core was then inserted into an ADC pad ring with readout circuitry. The parasitic extracted results are reported here.

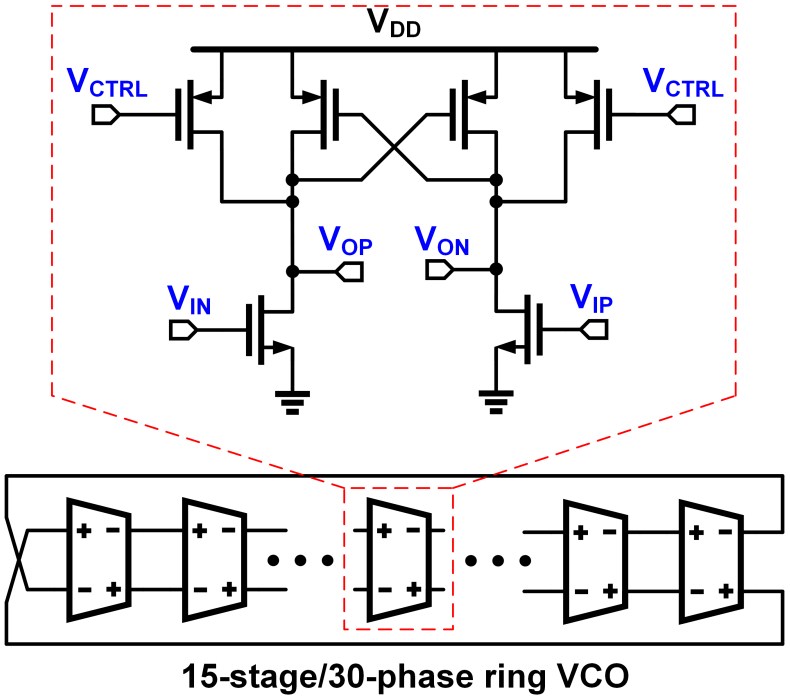


Figure 4.13: Differential Ring VCO and its unit delay element.

Sweeping the DC input voltage and measuring the output frequency shows the single-ended VCO transfer function shown in Figure 4.15. The actual implementation contains pins to extract the output phase from the VCO in Channel 8. This is used to demonstrate the spatial averaging effect versus a single quantizer.

Using a sine wave input test and checking the digital outputs, a 1024-point FFT was used to check ADC performance. Figure 4.16 shows the raw digital output. Severe harmonic distortion is clearly evident, limiting the overall performance. Here the ADC has an SNDR of just over 23 dB, limited by third order distortion. Using the calibration technique described in Section 4.3.5, the performance is dramatically improved as seen in Figure 4.17. Here the performance jumps to

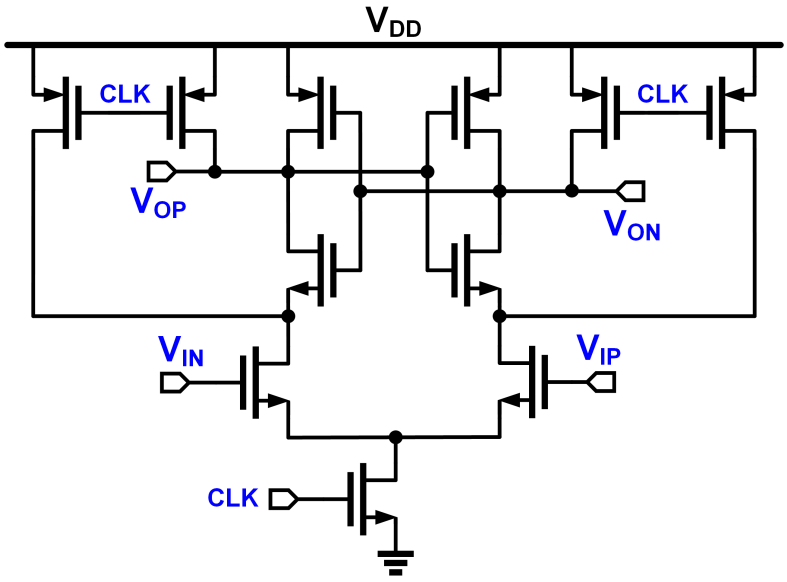


Figure 4.14: Sense amplifier used as a phase sampler. An additional slave latch is used to further buffer the digital output.

Table 4.1: Synthesized VCO Power Consumption Breakdown

| Supply | Voltage (V) | Current (mA) | Power (mW) |
|---|---|---|---|
| Analog | 1.5 | 37.3 | 55.95 |
| Digital | 1.5 | 62.3 | 93.45 |
| Total | - | 99.6 | 149.4 |

49 dB SNDR, a difference of 26 dB. If the OSR is doubled to 16, the noise power is reduced, resulting in the spectrum shown in Figure 4.18 with an SNDR of almost 54 dB over 25 MHz bandwidth.

The simulated power consumption of the proposed ADC is shown in Table 4.1.

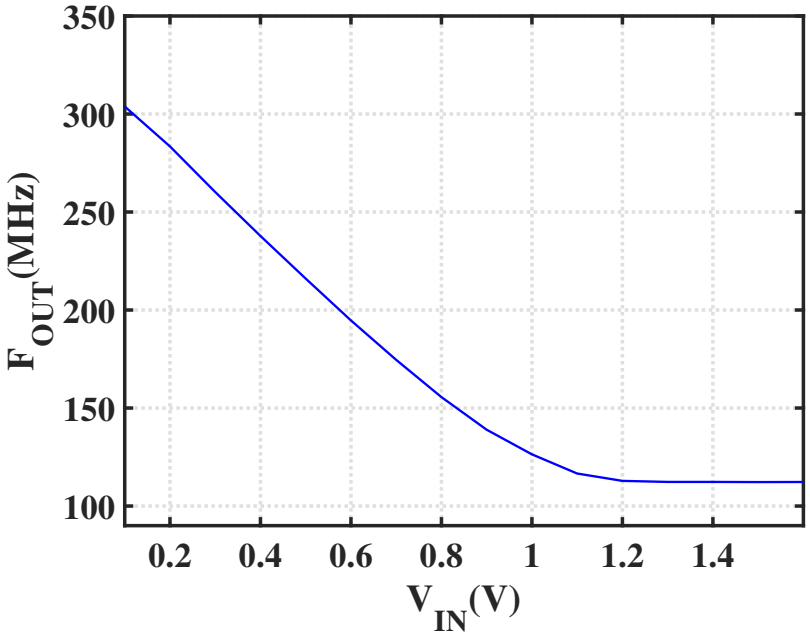


Figure 4.15: Simulated VCO transfer function with parasitic extrated annotation.

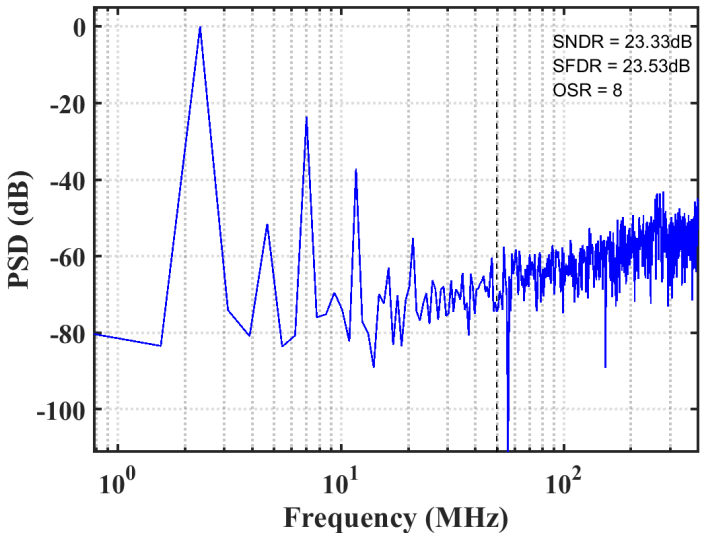


Figure 4.16: Monte Carlo simulation of parasitic extracted ADC without calibration.

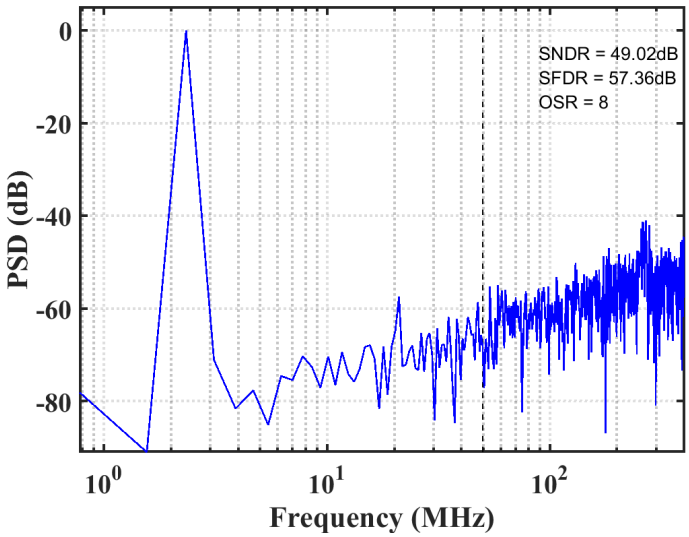


Figure 4.17: Monte Carlo simulation of parasitic extracted ADC with calibration.

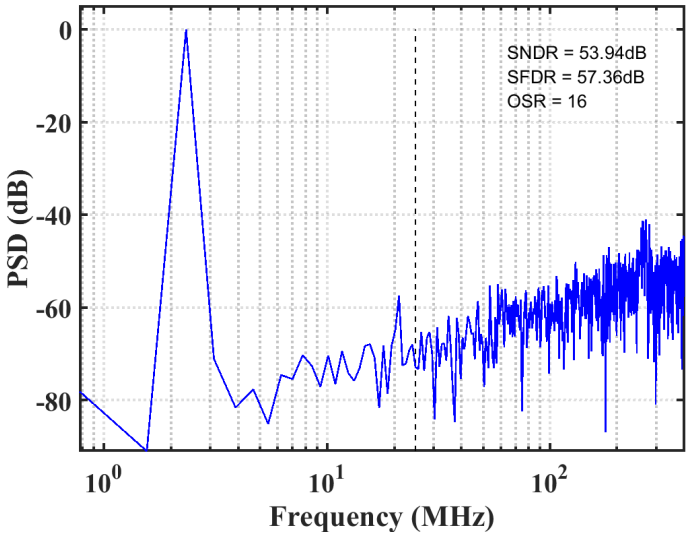


Figure 4.18: Monte Carlo simulation of parasitic extracted ADC with calibration.

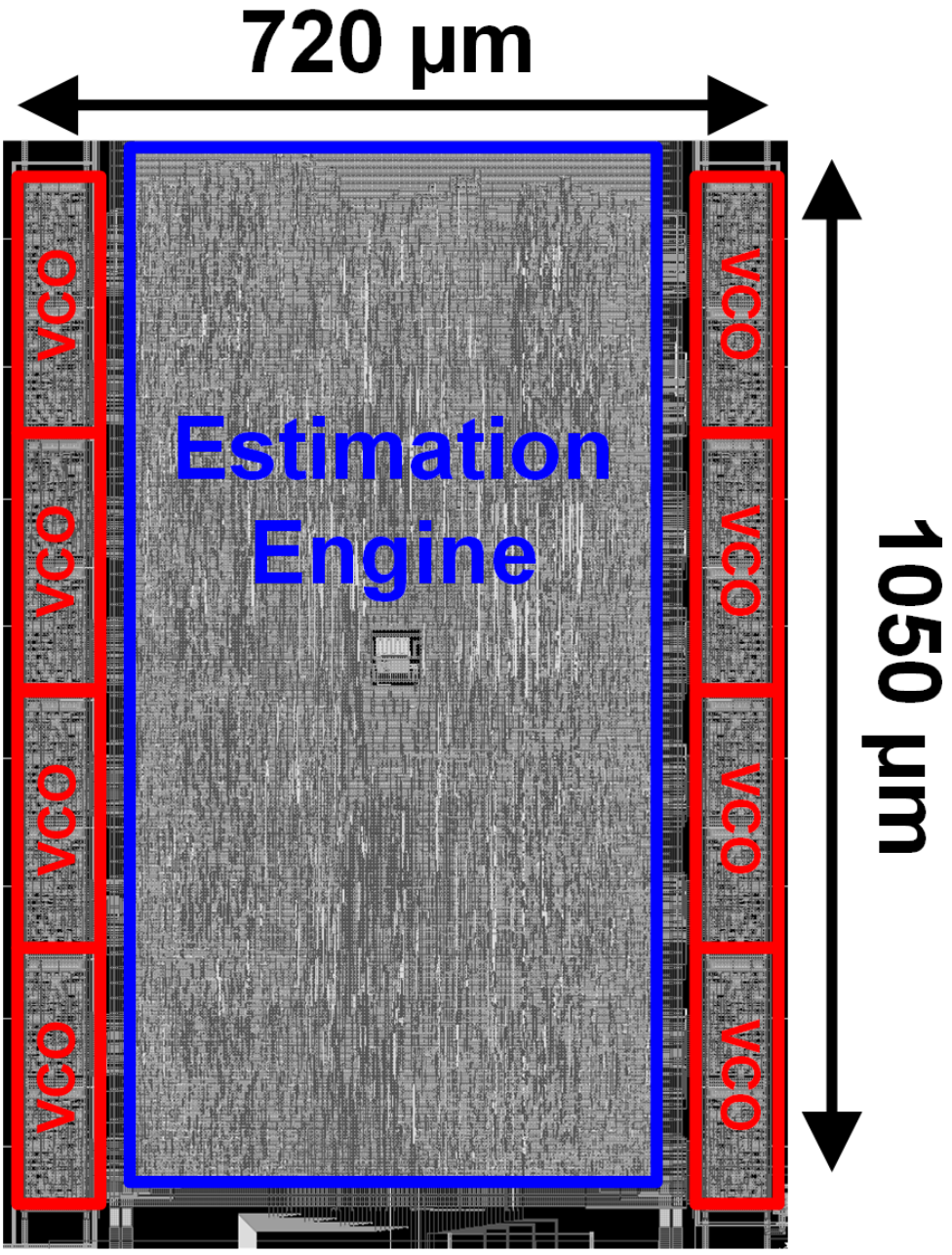


Figure 4.19: Proposed Stochastic VCO layout screenshot with minimal floor plan.

## 4.6 Conclusion

The work presented in this chapter describes a process where architecture selection and minimal custom dell design are combined with stochastic ADC principles to create a future ready, highly-digital design technique that offers opportunities for data converter designers.

Generating a fully synthesized ADC is a challenging new method to realize an analog design. It does offer the potential to speed up design flow, further integrating analog and digital design teams for increased productivity. While it may never replace traditional analog designers, it does deliver a fast, effective way to realize an ADC when low to moderate resolution specifications are required.

# Chapter 5: Future Work

> "All you need in this life is ignorance and confidence, and then Success is sure."
>
> — *Mark Twain*

This chapter will discuss possibilities for further investigation. Both of the major techniques presented in this dissertation can offer a wide range of research topics for further study and development.

## 5.1 Hybrid Domain Architecture Improvements

Regarding the work in Chapter 3, there are two major design points that can be developed to improve the performance. The first being a method to calibrate the static mismatch present in the capacitive DAC used in the SAR feedback loop. The second is the PVT related variations in the inter-stage gain $K_{VT}$.

### 5.1.1 DAC Calibration

Static mismatch of the capacitors in the first stage SAR are a limiting factor to higher resolution quantization. Some binary weighted combination of unit capac-

itors can be compared to the total DAC capacitance $C_{TOT}$. This ratio represents the actual bit weight of each decision. The ideal set of weights for a radix-2 DAC is simply:

$$Weight_{DAC} = [2^{N-1}\ 2^{N-2}\ ...\ 2^{N-N+1}\ 2^{N-N}]\ =\ [64\ 32\ 16\ 8\ 4\ 2\ 1] \tag{5.1}$$

In a real implementation where the capacitors have a random distribution, the actual values can take on a set of values such as:

$$Weight_{DAC,Actual} = [63.89\ 32.01\ 16\ 7.99\ 4.02\ 2.02\ 0.99] \tag{5.2}$$

This difference between ideal and real values will primarily result in degraded DNL for a binary weighted DAC. The standard 'brute-force' method to improve this matching is by increasing the total area used by increasing $C_U$ and therefore reducing the ratio $\frac{\Delta C_U}{C_U}$. It may be possible to use a foreground calibration method in which the digital output code of the TDC can be leveraged to correct for capacitor mismatch. This works because the code distribution of the second quantizer should be uniform, but in the presence of first stage capacitor mismatch, there is portions of codes that fall below or above the mean value in terms of the second stage output histogram.

Front-end DAC calibration schemes are a fundamental data converter problem, and the use of a time-domain background calibration loop would serve to be an interesting research topic for further study.

### 5.1.2 V-T Gain Calibration

The V-T gain is one parameter that requires monitoring to deliver a robust ADC. The effective gain between stages can be defined as:

$$\frac{V_{LSB,SAR}}{T_{LSB,TDC}} \cdot \frac{C_S}{I_D} \tag{5.3}$$

A background calibration loop would require a DLL to set the total delay line time, effectively setting $T_{LSB,TDC}$ to be some integer division of the total delay. Additionally $I_D$ would need to be adjusted to maximize inter-stage gain without over range.

### 5.1.3 Increasing Speed

The overall speed of the proposed two-step ADC was limited for several reasons. The main factor for this was the V-T technique used to save power consumption in the residue amplifier. This was because of the three phase scheme which required the SAR DAC to be connected to the amplifier until the zero-crossing event. This time period is proportional to the resolution of the back-end TDC. While this is reduced by using advanced CMOS, speed can be improved through architectural changes.

The first possibility is to time-interleave two front end SAR quantizers. This would allow a ping-pong operation in which one SAR is sampling and bit-cycling while the other is being discharged with prior sampled information. This would

result in increased area, but not necessarily by a factor of two. SAR components like the comparator and sampling switch could be shared between the front end channels.

A second possibility is by changing the TDC implementation. A flash design was used for its simplicity, but a vernier architecture may be more well suited for high speed as described in Section 2.2.1.2. This is because the vernier attains finer resolution by comparing two well matched delay cells. This does increase latency, but could be designed such that the zero-crossing event happens quickly after discharge start. Then while the $START$ and $STOP$ signals are propagating their respective delay lines, the SAR DAC can transition back to input sampling to increase speed. In this setup, the added latency must only be less than a full clock half-cycle before it would limit the overall speed.

## 5.2 Synthesized Architecture Improvements

The work presented in Chapter 4 for ADC synthesis was a preliminary step in the evolution of this concept. Although many steps were automated, several key steps were manually performed. These include the verilog netlist generation (a one-time process per design), and the selection of the appropriate analog cell based on layout parasitics encountered. Future research could further develop the software tools used to perform circuit synthesis to enhance its capabilities in the analog domain.

In this work, the ADC non-linearity was mitigated by using post-processing of the digital outputs. Another method to address this is to use the stochastic ADC

as the back end quantizer is a two-step implementation. This verilog-assisted ADC would not be fully synthesized, but would be capable of higher resolution performance without the need for digital non-linearity correction.

## 5.3 Software-Defined ADC

One extra area of study is the potential for architecture reconfiguration, also known as a software-defined ADC. Based on the highly digital architecture shown in Chapter 4, modifications based on software control are viable. Essentially, all eight VCO channels can be used in parallel to form a stochastic ADC as was reported here. As an alternative, the VCO channels could be time interleaved by changing the sampling clock sent to each channel and then bypassing the estimation engine. This would lose the resolution enhancement from spatial averaging, but can increase the signal bandwidth. A third mode of operation is also possible by simply disabling a portion of the VCO channels to reduce power consumption. Combining some of these software-defined configurations can deliver an ADC with a wide range of operating points to meet the requirements of an array of independent ADC channels currently required in SOC designs.

# Chapter 6: Conclusion

> "The spread of civilisation may be likened to a fire; first, a feeble spark, next a flickering flame, then a mighty blaze, ever increasing in speed and power."
>
> — *Nikola Tesla*

The study of data converters is a well established field with a wide range of applications. Their position at the critical junction between analog and digital domains continues to be a bottleneck in portable electronic systems. With the advent of newer and smaller CMOS process technology, new design paradigms that leverage highly digital time based processing are growing in popularity. This thesis has presented two works which offer potential methods to take advantage of the intrinsic properties of future scaled transistors.

Chapter 1 provided a brief history of modern electronic circuits, starting with the invention of the transistor and IC, eventually leading to the complex SOC used today. A background on ADCs and the difficulties in their design was discussed.

Chapter 2 reviewed a growing approach to creating data converters which uses time domain information to either replace, or supplement existing voltage domain techniques. These works show a wide range of applications and performance targets can be met by taking advantage of the digital characteristics of CMOS.

Chapter 3 showed a hybrid domain approach that uses conventional voltage quantization in the first stage followed by a time based quantizer that can deliver high resolution with low power consumption. The implementation is realized with a residue amplifier that mitigates the high gain and swing requirements of a conventional two-step ADC, making it ideal for future process technology in which both of these parameters are inherently limited.

Chapter 4 describes a method to automate the creation of an ADC, using existing digital design tools. This approach can greatly reduce the overall design time for moderate resolution targets with wide bandwidth. As the size and switching speed of transistors continues to decrease, automated design and layout techniques with digital calibration offer an efficient way to quantize input signals into the digital domain.

In Chapter 5, several areas for future study were presented. These techniques include enhancements to the circuit topologies to improve speed and reliability, calibration algorithms, as well as further developing the software and tools used to automate ADC creation.

It is truly fantastic what our modern electronics are capable of. Each new process technology presents opportunities and challenges for mixed-signal circuit designers. This dissertation shows a collection of techniques to address the challenges faced due to process scaling. The hybrid use of voltage and time information can be optimized for high resolution and low power, whereas the digital nature of a stochastic ADC lends itself well to circuit synthesis and the rapid system development it offers. Although these are not magic solutions that suddenly solve timeless

design trade offs, they are a relatively promising class of circuits that show great potential to embrace the future of CMOS, whatever it may be.

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