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Abstract approved: _____

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There is a large and growing market for portable consumer audio products with very small size. As the size of these products is reduced, the area occupied by batteries becomes significant and hence limits the number of batteries to one. In order to build such small products, high levels of integration are required to minimize both the number of integrated circuits and off-chip discrete components. With supply voltages limited to that supplied by one battery, special *low-voltage* and *low-power* circuit design techniques are required. For digital circuits integrated on a chip, the reduction in supply voltage directly translates to reduced power dissipation. However, for analog circuits on the same chip, the reduction in supply voltage can cause a significant increase in both required power dissipation and die area primarily due to the reduction in available signal swing and the limited selection of suitable low-voltage circuit architectures.

The objective of this research was to provide analysis and optimization techniques to meet signal-to-noise ratio specifications with minimum power dissipation and die area. A $0.9V$ microphone preamplifier and programmable gain amplifier system was designed using these techniques and fabricated with a $0.35\mu m$ CMOS process.

Noise Optimization for Low-Voltage CMOS Audio Preamplifier Systems

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Dean of the Graduate School

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Matthew Eugene Brown, Author

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DEDICATION

This thesis is dedicated to the memory of my sister,

Dana Quinn Rothacker, Ph.D.

March 17, 1952 - July 4, 2004

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1. INTRODUCTION

1.1. Motivation

There is a large and growing market for portable consumer audio products with very small size. As the size of these products is reduced, the area occupied by batteries becomes significant and hence limits the number of batteries to one. In order to build such small products, high levels of integration are required to minimize both the number of integrated circuits and off-chip discrete components. With supply voltages limited to that supplied by one battery, special *low-voltage* and *low-power* circuit design techniques are required. For digital circuits integrated on a chip, the reduction in supply voltage directly translates to reduced power dissipation. However, for analog circuits on the same chip, the reduction in supply voltage can cause a significant increase in both required power dissipation and die area primarily due to the reduction in available signal swing and the limited selection of suitable low-voltage circuit architectures.

The objective of this research was to provide analysis and optimization techniques to meet signal-to-noise ratio specifications with minimum power dissipation and die area. A $0.9V$ microphone preamplifier and programmable gain amplifier system was designed using these techniques and fabricated with a $0.35\mu m$ CMOS process.

1.2. Organization

This document is organized into the following chapters with the intent of presenting the material in the approximate sequence that would be used to complete a similar design:

Chapter 2: Audio Preamplifier Systems Provides background on the functional and performance requirements of a microphone preamplifier and PGA sysptem for portable products.

Chapter 3: Low-Voltage Circuit Design Provides background on the limitations imposed by using a low supply voltage and the means of dealing with those limitations.

Chapter 4: Noise Analysis Presents fundamental noise analysis techniques.

Chapter 5: Low-Noise Amplifier Design Presents low-voltage low-noise amplifier analysis and design techniques.

Chapter 6: Noise Optimization Presents optimization techniques that can be used to meet noise specifications and other limitations while minimizing cost.

Chapter 7: Preamplifier and PGA System Design Presents the design of a 0.9V microphone preamplifier and Programmable Gain Amplifier (PGA) system that was designed using the presented optimization techniques and fabricated with a $0.35\mu m$ CMOS process.

Chapter 8: Test Results Presents the measured performance of a fabricated preamplifier integrated circuit.

Chapter 9: Conclusions Summarizes the main conclusions from this research as well as proposes future work for further research to advance this field of study.

2. AUDIO PREAMPLIFIER SYSTEMS

2.1. Introduction

This section describes audio preamplifier systems from general considerations to the target specifications of this work. A preamplifier, commonly called a *preamp*, is an amplifier that is used to amplify a low level external input signal to a higher signal level that is less susceptible to noise and interference. The amplified signal is then processed, recorded, and/or further amplified depending on the particular application.

For this project, the intended input signals are analog audio signals from an external microphone and the output of the preamplifier system is connected to the input of an Analog-to-Digital Converter (ADC) fabricated on the same integrated circuit die. The preamplifier amplifies the low-level output signal of a microphone, and drives the amplified signal into the inputs of an ADC at a level which provides the desired balance of ADC dynamic range and distortion.

The desired preamplifier output level can be maintained for different and varying input signals by adjusting the gain of the preamplifier. Although preamplifiers generally amplify signals, some preamplifier systems can also attenuate signals as needed to provide the desired output levels. Gain settings are typically controlled by user selection or dynamically as part of an integral limiter and/or compressor system.

2.2. Microphones

Microphones provide very low level output signals, thus the need for a preamplifier. The intended microphone for this project is an *electret* microphone

which is a type of *condenser* microphone that has one fixed capacitor plate with built in charge and another capacitor plate which is a flexible membrane that moves with changes in sound pressure [11]. The single ended output of the electret microphone is generally buffered by a single BJT device built into the microphone. The noise and distortion performance of a preamplifier system is often is expected to exceed that of the microphone it will be connected to.

2.3. Programmable Gain Amplifiers

Both amplifier stages used for the preamplifier system designed for this project are Programmable Gain Amplifiers (PGA). Gain is variable and gain settings are digitally controlled. The first stage is designed to be set to the appropriate gain for the system, while the second stage is designed to be dynamically adjusted and could be used to perform digitally controlled analog compression or limiting functions. Gain settings are in discrete steps. For the dynamically operated PGA, these steps are on a logarithmic scale and are kept very small so that the distinction between the different gain steps is not noticeable to the consumer.

2.4. Portable Consumer Audio Product Requirements

Portable consumer audio product requirements include: Few batteries, low power consumption (i.e. long battery life), small package sizes, few off-chip components, high level of integration, and performance comparable to non-portable products.

2.5. Target Specifications

The detailed target specifications presented in Table 2.1 provided for this project were strictly observed when possible. This is unlike many research projects where the goal is to demonstrate a new performance level or topology. Here the basic topology and performance were specified in advance, leading the research towards optimization. Noise is expressed in terms of 'dBV', which is dB referenced to $1V_{RMS}$, and in 'dBA' which is shorthand for units of dBV when *A-weighting* is applied. A-weighting is an ANSI band-pass filtering standard intended to represent human hearing response. A-weighting reduces the measured noise.

Fig. 2.1 shows the required block diagram for both (a) the final product, and (b) the test chip. The circuit block labeled "SE2D" performs a Single Ended to Differential conversion. Fig. 2.2 shows the required implementation in further detail with allowable off-chip components and pins. The specified topology and limitations on off-chip components dictate that that a single ended architecture is used for the gain stages which limits performance. Fig. 2.3 illustrates the implementation of the digital potentiometers as included in Fig. 2.2.

TABLE 2.1. Target Specifications

Input Referred Noise	$\leq -122dBV$ $10Hz - 20kHz$
Input Referred Noise	$\leq -124dBA$ $10Hz - 20kHz$
Output Referred Noise	$\leq -98dBV$ $10Hz - 20kHz$ for gain $\leq 24dB$
Preamp Gain Settings	$10dB$ and $20dB$
PGA Gain Settings	$0dB$ to $49dB$ in $0.5dB$ increments
Output Signal	$0.8Vpp$ differential
Distortion Level	$-80dB$ at $V_{dd} = 1.2V$
Power Supply Range	$0.9V$ to $1.8V$

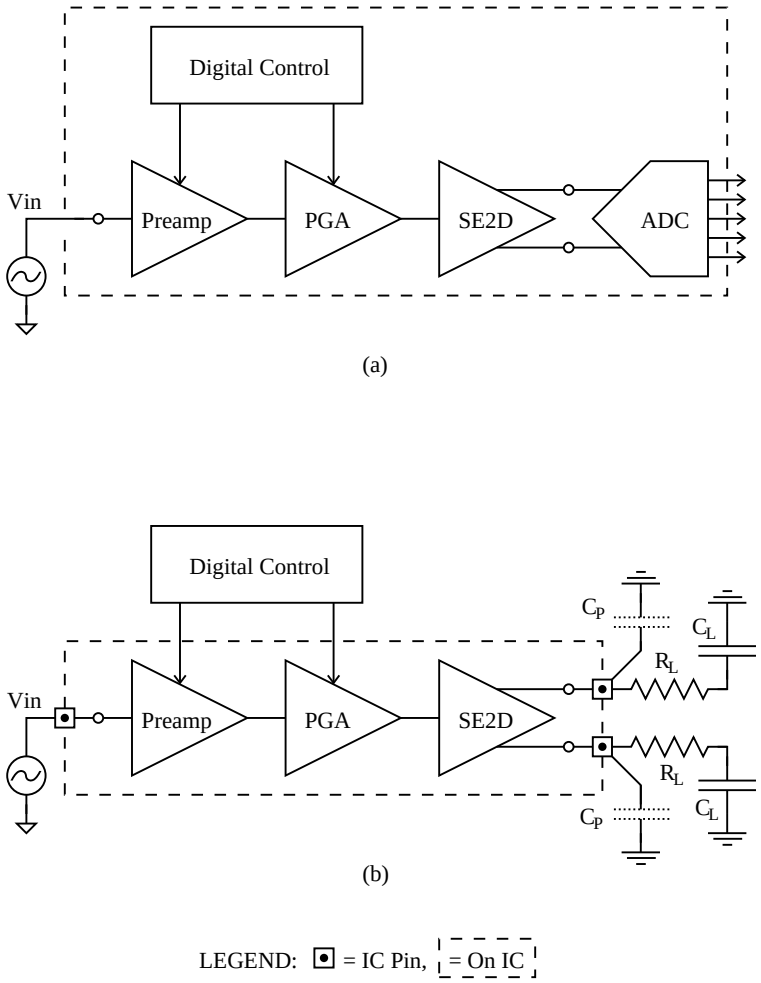

FIGURE 2.1. Preamplifier system block diagram for both (a) the final product, and (b) the test chip.

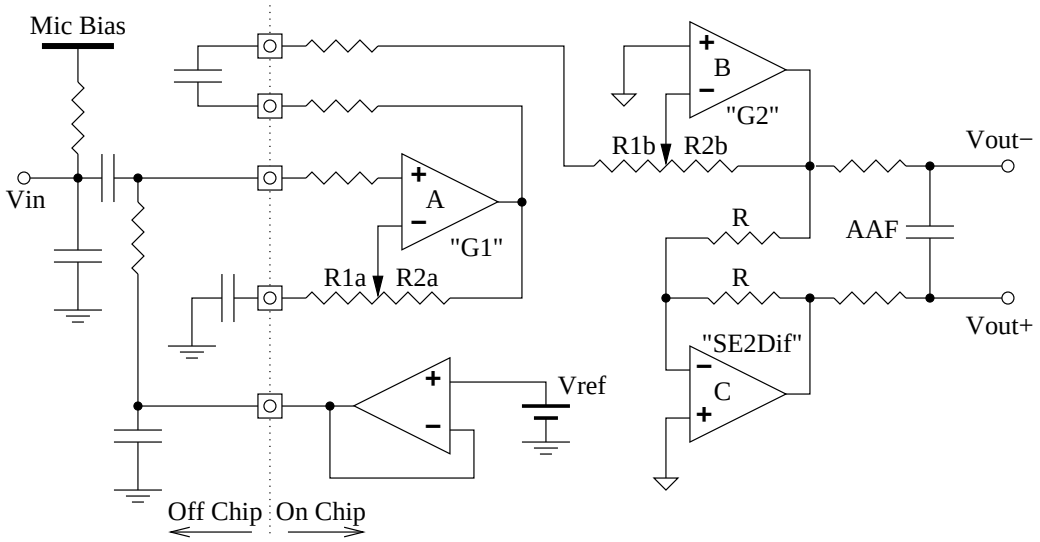

FIGURE 2.2. Microphone preamplifier system

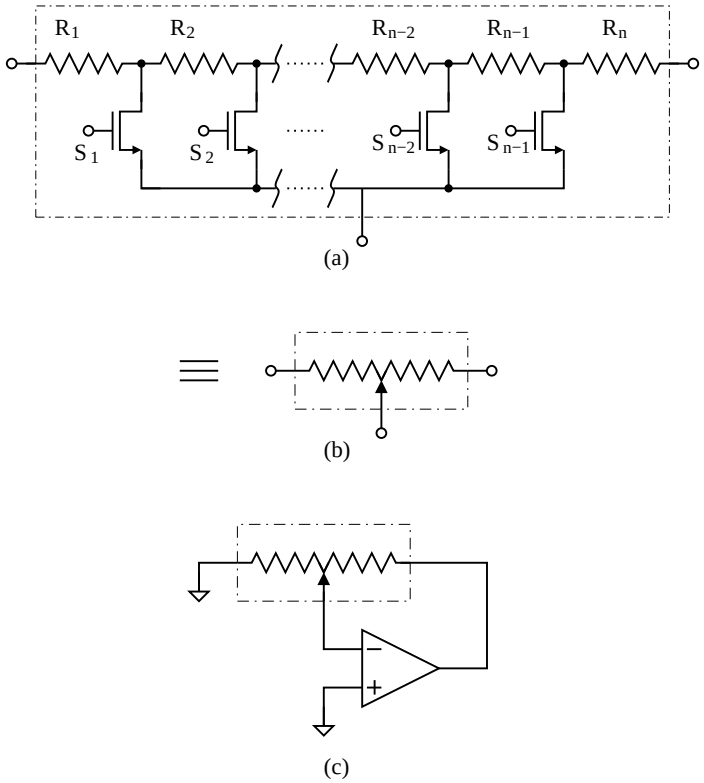

FIGURE 2.3. Digital potentiometer implementation where (a) shows the transistor level implementation, (b) shows the equivalent potentiometer symbol, and (c) shows the digital potentiometer as part as an amplifier stage.

3. LOW-VOLTAGE CIRCUIT DESIGN

3.1. Introduction

Low-voltage circuits are circuits that operate with a supply voltage notably lower than commonly available (which, at present, is typically about 3.3V). Lower supply voltages are being mandated by the reduction of gate breakdown voltages due to the thinner gate oxides used in finer line-width CMOS processes. Lower supply voltages can also be used in order to reduce power consumption for digital circuits and, for portable products, to operate with fewer batteries. The target power supply voltage for this project is limited to that which can be supplied with one common battery, nominally around 1.2V, and well below that which the process can sustain. This section describes some of the fundamental requirements and design considerations for low-voltage analog audio designs.

3.2. Low-Voltage Digital Power Dissipation

Although leakage currents are increasingly contributing to low-voltage digital power dissipation, digital power consumption is primarily dynamic. The dynamic power dissipation of a digital circuit can be expressed as

$$P = C_{eff} V_{dd}^2 f \tag{3.1}$$

where C_{eff} is the total effective capacitance that is being driven by the circuit, V_{dd} is the supply voltage, and f is the switching frequency. Interconnect capacitance contributes to the total capacitance C_{eff}, however this is typically dominated by gate capacitance for most digital circuit blocks. Thus, digital power consumption can be reduced by reducing one or both of C_{eff} and V_{dd}. For example, for a given

process, reducing V_{dd} from $3.3V$ to $1.2V$ can theoretically reduce digital power consumption by a factor of 7.5, a significant improvement.

Unfortunately, as is demonstrated by this work, a reduced supply voltage can cause a considerable increase in the power dissipation of analog circuits. It must not be assumed that a reduced power supply will reduce the overall power dissipation of an integrated system containing both analog and digital circuits.

3.3. Battery Powered Devices

Commonly available batteries suitable for portable audio products (AA and AAA cells) supply a maximum voltage of about $1.5V$ which quickly reduces to about $1.2V$ and, near complete discharge, to about $0.8V$. The voltages and discharge rates are dependent on the electrochemistry of a particular battery.

Battery voltage is commonly increased by connecting batteries in series, and also by using switched capacitor voltage boosting techniques. However, the trend is now to create products that require only one battery in order to achieve a very compact form factor and, for reasons of power consumption and reliability, boosted voltages are best avoided where possible. A goal of this work is to use the directly available battery voltage as much as possible as voltage changes throughout the battery discharge cycle. This requires that the circuits function (although at reduced performance) with supply voltages down to $0.9V$.

3.4. Switches

Analog switches, critical for PGAs and other analog blocks, are difficult to implement with low supply voltages [8]. In order for a switch to be turned on, the magnitude of the gate to source voltage must be at least the threshold voltage

of the switching device i.e. $|V_{gs}| - |V_T| > 0$. This can, for many continuous-time analog circuits, only be overcome by using a boosted gate voltage for the switches, although this implies reduced reliability [7]. For discrete-time circuits, this limitation can be overcome by techniques such as presented in [6]. however for continuous-time analog circuits, switch gate voltage boosting can be unavoidable.

3.5. Signal Swing and Offset

Signal swing and offset are of particular importance for low-voltage, low-noise, and low-distortion designs. From a noise perspective, signal swing needs to be as large as possible to maximize SNR. From a distortion perspective, signal swings need to be as small as possible for the most linear operation. Thus, there is a clear tradeoff between noise and distortion performance.

Distortion can be strongly influenced by the DC offset of the signal. The offset that is ideal for one amplifier stage is not necessarily ideal for another in the same circuit and a compromise must be made for best performance, which could necessitate DC blocking capacitors, such as used for this project.

3.6. Device Operating Regions

With a low supply voltage, for large-signal considerations it is often necessary to bias devices such that only very small drain-to-source voltages (V_{ds}) are required to keep the devices in saturation. Large transconductances are required for input devices to achieve good noise performance and also to achieve adequate gain when driving low resistance loads. Because of these demands, it may be necessary to drive some devices into moderate or perhaps even weak inversion.

Since, with weaker inversion, there is a departure from ideal square-law behavior, it is important to make the following distinctions. Let the bias current to transconductance ratio be defined as

$$\triangle \equiv \frac{2I_D}{gm} \tag{3.2}$$

such that

$$g_m \equiv \frac{2I_D}{\triangle}. \tag{3.3}$$

For simplicity, the overdrive voltage notation

$$V_{gst} \equiv |V_{gs}| - |Vt| \tag{3.4}$$

is introduced. In strong inversion

$$g_m \approx \frac{2I_D}{V_{gst}} \tag{3.5}$$

such that

$$\triangle \approx V_{gst}. \tag{3.6}$$

However, in moderate to weak inversion

$$g_m < \frac{2I_D}{V_{gst}} \tag{3.7}$$

such that

$$\triangle > V_{gst}. \tag{3.8}$$

For each $\triangle$ value, there is a corresponding V_{gst} value that must be determined through simulations. The $\triangle$ values will be used for calculations involving transconductance, while the corresponding V_{gst} values will be used for large signal calculations as the minimum V_{ds} value for saturation.

3.7. Maximum Transconductance to Current Ratios

For the process used for this project, in moderate to weak inversion, and for a given V_{gst} value, PMOS devices deviate more from ideal square-law behavior than NMOS devices. In order to make a more objective comparison of the two devices for optimization purposes, a method was devised for accounting for this deviation and determining the minimum V_{gst} values and thus minimum $\triangle$ values that can be worked with. Although this method is somewhat arbitrary, it is better than arbitrarily choosing a single minimum V_{gst} value to be used for both devices. This technique is analogous to determining the 3dB point when considering changes in frequency response and is shown in Fig. 3.1. The ratio g_m/I_d is plotted versus V_{gst} on a log-log scale and straight lines are drawn tangent to the strong and weak inversion regions. The minimum allowable V_{gst} values are defined as being at the intersection of these lines.

From this determination, the following minimum values are used. For NMOS devices, a minimum value of $V_{gst} = 0.11V$ corresponds to the maximum value of $g_m/I_D = 13.5$, which gives a minimum $\triangle = 0.15V$. For PMOS devices, a minimum value of $V_{gst} = 0.14V$ corresponds to the maximum value of $g_m/I_D = 11.6$, which gives a minimum $\triangle = 0.17V$.

Beyond these minimum V_{gst} values, devices may be biased such that the V_{gst} values are as large as large-signal considerations allow, which will be done to reduce the transconductance of certain devices to reduce noise.

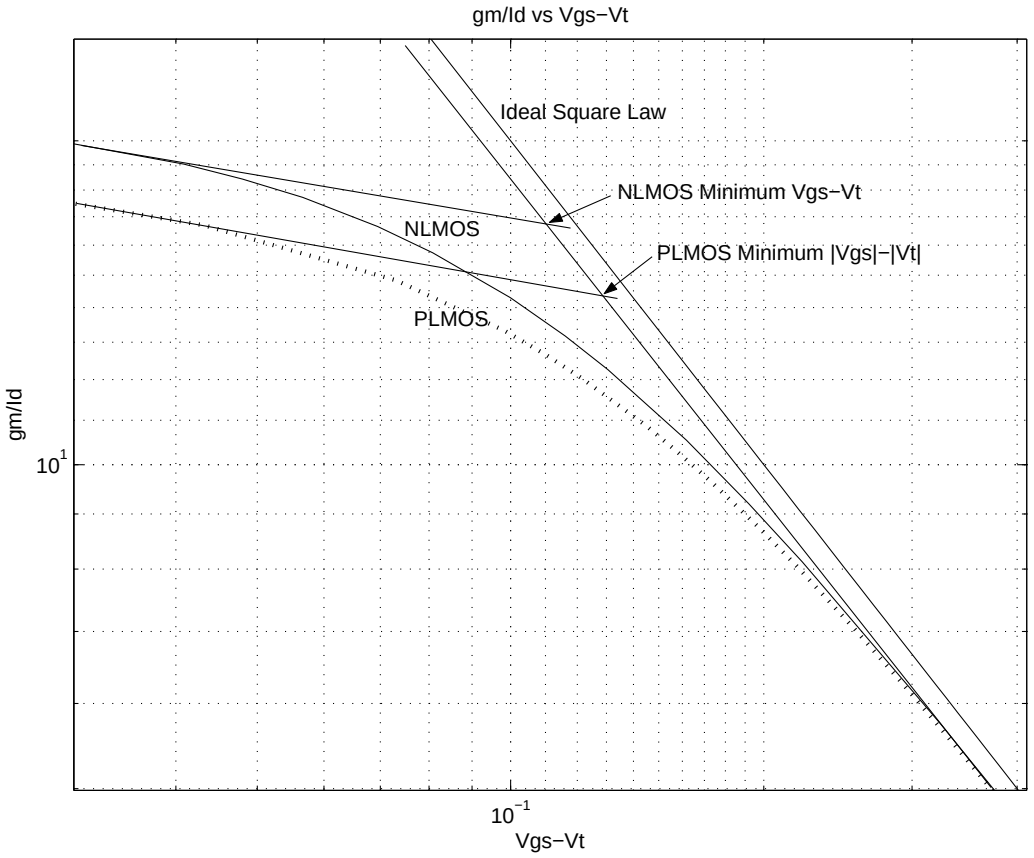

FIGURE 3.1. Graphical Determination of Minimum $|V_{gs}| - |V_t|$

4. NOISE ANALYSIS

4.1. Introduction

This chapter introduces noise sources that must be considered in the design of continuous-time CMOS audio circuits and techniques for analyzing them. The three dominant intrinsic noise sources are: resistor noise, MOSFET thermal noise, and flicker noise.

4.1.1. Noise versus Interference

As stated in [2], noise in the broadest sense is "any unwanted disturbance that obscures or interferes with the desired signal." In this document, the term 'noise' will only refer to intrinsic noise, which is generated by the circuit components themselves. That is the circuit is considered perfectly isolated from the rest of the world. Careful IC and PCB layout as well as the use of symmetrical differential structures where possible can be used to reduce interference, but this will not be covered in this document which will focus on the noise inherent in the circuit devices.

4.2. Zipper Noise

Zipper noise is an audible sound similar to the sound produced when operating a garment zipper, which is produced by a PGA when changing gain settings. It is not really noise such as inherent noise, but rather a result of interference and distortion. Because the gain changes in discrete steps, there is a abrupt change in the instantaneous signal level at the moment that the gain changes. This abrupt

gain change produces high frequency distortion which, when quickly changing through a series of gain settings, produces the zipper-like sound. Zipper noise can also have a small component caused by the charge transfer between switches and any interruption in the normal feedback of the amplifying stage.

Zipper noise can be reduced by designing a PGA with finer gain increments, and by changing gain settings only when the instantaneous signal is at a zero crossing. Any DC offsets that are amplified will significantly contribute to zipper noise, and so low offset design is important for zipper noise reduction. There are other possibilities for reducing zipper noise which are beyond the scope of this research project but would make for future work. Zipper noise is not a focus of this research, however small gain increments for the dynamically switched second stage PGA are used, and DC blocking capacitors are employed to avoid the amplification of offsets.

4.3. General Analysis Methodology

Every electrical component, even wires, contributes to the total circuit noise. Fortunately, most of the noise comes from a few of the noise sources, and so analysis can be greatly simplified by focusing on those few noise sources. For this project the dominant noises come from the amplifier feedback resistors and the transistors of the differential pairs of each opamp. Other noise sources need not be considered analytically, but some allowance should be made for them, and they will, by default, be included in transistor level simulations.

Some assumptions that can be made to simplify analysis are that all noise sources are uncorrelated and that the noise bandwidth $\triangle f$ is the same for the entire system. Bandwidth will be limited by the DC blocking capacitors, anti-

alias filtering, and, for test, by the filters of the Audio Precision tester on which noise is measured. Uncorrelated noise powers can analyzed with simple addition and multiplication.

Low-noise design is performed by starting with a noise power *budget*, subtracting the noise power due to noise sources that cannot be reduced, and then designing the remaining noise sources to meet what is left of the noise budget. Since low noise performance is costly in terms of die area and power consumption, it is not efficient to reduce the noise power any more than required.

Noise power is often *referred* to the input of the system or the output of the system. To refer noise to a node, all noise power source RMS magnitudes are multiplied or divided by the total gain from the source node to the node the noise is being referred to. Both the Input Referred Noise power (IRN) and the Output Referred Noise power (ORN) are of particular interest for the complete system and for individual amplifier blocks.

4.4. Resistor Noise

Resistor noise, for typical CMOS processes with unsalicided poly or n-well resistors, consists of only thermal noise. Although it should be noted that the absence of flicker noise in resistors should not be taken for granted. The thermal noise power P_{nR} of a resistor is given by

$$P_{nR} = v_n^2 = 4kTR\triangle f \tag{4.1}$$

The notation v_n refers to the RMS noise voltage. Because inherent noise sources are non-correlated, calculations will be in terms of v_n^2 for the convenience of being able to sum individual noise contributions. This is the voltage noise form of the

equation as will be used for all noise equations. That is, the noise is injected as a series voltage source.

4.5. MOSFET Noise

The noise equations used to calculate the inherent noise generated by the MOSFET devices are those as used in HSPICE for the provided Level 49 models, and thus are in agreement with simulation results, and are the best prediction available for test results. For more information on these models refer to [10]. The total RMS noise v_n^2 is the sum of the total RMS thermal noise v_{nT}^2 and total RMS flicker noise v_{nf}^2

$$v_n^2 = v_{nT}^2 + v_{nf}^2. \tag{4.2}$$

Thermal and flicker noise are treated separately for both analysis and optimization purposes.

4.5.1. Thermal Noise

The thermal noise power spectral density (PSD) equation given in [10] is

$$channel\,thermal\,noise = \left(\frac{8k_BTg_m}{3}\right)^{\frac{1}{2}} \tag{4.3}$$

which has units of $\frac{A}{\sqrt{Hz}}$. Dividing this expression by g_m and taking bandwidth into account assuming flat frequency response yields the expression for the mean square value of the equivalent gate noise voltage

$$v_{nT}^2 = \frac{8k_BT\left(f_h - f_l\right)}{3g_m}. \tag{4.4}$$

4.5.2. Specification Thermal Noise Constant

Combining specification-dependent constants into one constant,

$$K_T \equiv \frac{8k_B T\left(f_h - f_l\right)}{3} \tag{4.5}$$

such that

$$v_{nT}^2 = \frac{K_T}{g_m}. \tag{4.6}$$

With $k_B = 1.38 \times 10^{-23} J/K$, $T = 300K$, $f_l = 20Hz$, and $f_h = 22kHz$:

$$K_T = 243 \times 10^{-18}[VA] \tag{4.7}$$

such that

$$v_{nT}^2 = \frac{243 \times 10^{-18}}{g_m} \tag{4.8}$$

regardless of process parameters.

4.5.3. Thermal Noise in terms of Transconductance Ratio

With $g_m = 2I_D/\triangle$,

$$v_{nT}^2 = \frac{K_T}{g_m} = \frac{K_T \triangle}{2I_D}. \tag{4.9}$$

4.5.4. Flicker Noise

The PSD of the channel flicker noise current equation given in [10] is

$$flicker\, noise = \left(\frac{\mathrm{KFg_m^2}}{C_{OX} W_{eff} L_{eff} f^{AF}}\right)^{\frac{1}{2}}, \tag{4.10}$$

which must be integrated with respect to f to yield the RMS value. The parameters KF and AF are process dependent empirically determined constants. Dividing by g_m and integrating with respect to f yields

$$v_{nf}^2 = \frac{\mathrm{KF}}{C_{OX} W L \left(\int_{f_l}^{f_h} f^{AF}\, df \right)}. \tag{4.11}$$

Introducing the gate area notation

$$A \equiv WL, \tag{4.12}$$

$$v_{nf}^2 = \frac{\mathrm{KF}}{C_{OX} A \left(\int_{f_l}^{f_h} f^{AF}\, df \right)}. \tag{4.13}$$

Combining specification and device constants into one constant which will be unique to each device type,

$$K_f \equiv \frac{\mathrm{KF}}{C_{OX} \left(\int_{f_l}^{f_h} f^{AF}\, df \right)} \tag{4.14}$$

such that

$$v_{nf}^2 = \frac{K_f}{A}. \tag{4.15}$$

For a given frequency response, device flicker noise power is inversely proportional to device gate area.

4.5.5. The Underrated Significance of AF

The SPICE parameter AF is often neglected in texts. However, particularly for low frequency applications, this parameter can be significant and should not be neglected.

The term $\left(\int_{f_l}^{f_h} f^{AF}\, df\right)$ is a constant for a given bandwidth and frequency response. If it is assumed that the coefficient $AF = 1$, (also assuming a flat frequency response) then

$$\int_{f_l}^{f_h} f^{(1)}\, df = ln\left(\frac{f_h}{f_l}\right), \tag{4.16}$$

which is a commonly made simplification. However, this assumption should not be made if it can be avoided and particularly if it is known that $AF \neq 1$, as a small change in AF can cause a large variation in the value of v_{nf}^2. For $AF \neq 1$,

$$\int_{f_l}^{f_h} f^{AF}\, df = \frac{f_l^{1-AF} - f_h^{1-AF}}{AF - 1}. \tag{4.17}$$

For example, the audio band is typically defined such that $f_l = 20Hz$ and $f_h = 20kHz$. The values of KF typically can vary from 0.8 to 1.2. The resulting values of $\int_{20Hz}^{20kHz} f^{AF}\, df$ vary by a factor of about $\pm 6dB$ which is significant. This is plotted in Fig. 4.1.

4.5.6. Total Device Noise

The total input referred noise for any MOSFET can be expressed in terms of the previously derived constants as

$$v_n^2 = v_{nT}^2 + v_{nf}^2 = \frac{K_T}{g_m} + \frac{K_f}{A} = \frac{K_T \triangle}{2I_D} + \frac{K_f}{A}. \tag{4.18}$$

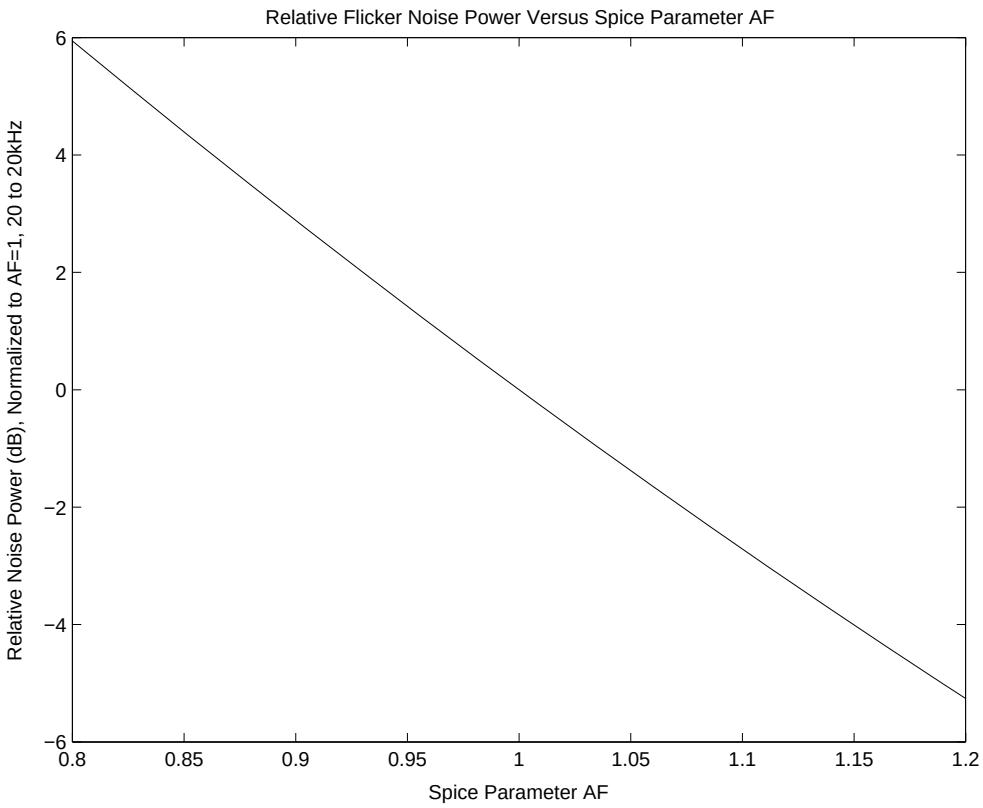

FIGURE 4.1. Flicker Noise Power versus Parameter AF

5. NOISE OPTIMIZATION

5.1. Introduction

With limited design architecture and transistor biasing options, meeting challenging noise specifications will come at a cost of significant die area and power dissipation. Both die area and power dissipation are costs that must be reduced as much as possible. A closed form optimization method is presented here that can be used to meet noise performance requirements for the minimum cost. This method can also be used for other simple circuit optimization problems such as capacitor scaling for kT/C noise which is presented as an example.

Even if computer systems are ultimately employed to solve optimization problems, it is useful for the circuit designer to determine what variables are most important such that the number of variables can be reduced. Only a few noise sources dominate the total circuit noise and those are the only ones that need be considered for optimization purposes. Assumptions about cost will also need to be made. Fortunately, through simulation, these assumptions can usually be verified. A simplified noise model and closed form optimization solution can provide the designer with valuable insights as well as the most efficient noise budgeting. This method may also be useful for providing a good starting point for some linear optimization programs where the problem is too complicated for this simple method to solve.

5.2. Cost Simplifications and Limiting Factors

Engineers always struggle to either provide specified performance for minimum cost or maximum performance for a set cost. Cost analysis can easily be

more complicated than circuit analysis and, since the focus here is on the latter, some assumptions and simplifications about cost need to be made. Many cost considerations are already inherent in the specifications and features including the number of pads and off-chip components and especially in the choice of a particular CMOS technology. Here, for noise optimization purposes, the only costs that are considered are die area and power consumption.

5.2.1. Cost of Die Area

Die area is a direct manufacturing cost. Although yield goes down with increased die size due to defect density, cost per die area is approximately linear in the range of die areas that would be acceptable for such a circuit. The assumption is made that die cost is directly proportional to die area.

5.2.2. Cost of Power Consumption

Power dissipation is a marketing cost. That is, the more power a component dissipates the smaller the market for that component. From a marketing standpoint, this is an extreme simplification, but for our purposes it is adequate. The assumption is made that there is a cost directly proportional to total power dissipation.

5.2.3. Limiting Factors

There will likely be specification limits imposed on either power consumption or area. It would not be possible to constrain power consumption, die area, and noise performance simultaneously.

Since the total noise power is a sum of the flicker noise power and the thermal noise power, regardless of how much power or area one is willing to expend, there will be a minimum power consumption and minimum area required to meet a given noise specification.

5.3. Noise and Cost Equations

5.3.1. Noise Specification Equation

The total system noise voltage squared P_s can be expressed as the sum of N noise sources P_i, each multiplied by the power gain G_i that each noise source is amplified (or attenuated) by to the node at which P_s is measured:

$$\boxed{\sum_{i=1}^{N} G_i P_i = P_s} \tag{5.1}$$

Because the P_i terms represent total RMS noise voltage squared, bandwidth is included in those quantities. Bandwidth can be considered separately, however, for this application bandwidth will be limited equally for all noise sources.

5.3.2. Noise Cost Equations

In many situations, for a given noise bandwidth, the cost of low noise performance is inversely proportional to the total noise. This cost can be in terms of any combination of area, power, or a more expensive technology more suitable for low noise design. For example, for a CMOS differential pair meeting all other design constraints, the total input referred noise power can be expressed as a function of area and power according to

$$P_n = v_n^2 \triangle f = \frac{K_t}{I_D} + \frac{K_f}{A} \tag{5.2}$$

where K_t and K_f are thermal and flicker noise coefficients respectively, I_D is the bias current (thus a cost in the form of power dissipation), and A is the total gate area. Often, the technology is given and either power consumption or die area will be the limiting factor.

Since cost is generally inversely proportional to the noise power, the variable D is introduced to represent relative cost such that

$$D_n = \frac{K_n}{P_n} \tag{5.3}$$

where K_n is a relative cost weighting constant. For example, if NMOS input devices were used for one opamp in a circuit and PMOS input devices were used on another, different values of K_n would be used to express the relative difference in the cost of attaining equivalent noise performance.

The total cost for a complete system can be expressed as the sum of the individual costs for each circuit element being considered

$$\boxed{D = \sum_{i=1}^{N} \frac{K_i}{P_i}} \tag{5.4}$$

The objective is to satisfy the noise specification as given in Eq. 5.1 for the lowest possible cost. In order to achieve this objective, the quantity D of Eq. 5.4 must be minimized while satisfying the performance specification of Eq. 5.1.

5.3.3. Region of Constants and Variables

Consideration of the physical nature of the problem provides the additional constraint that all of the constants and variables are positive real numbers

$$\boxed{\{P_s, P_i, G_i, K_i\} \in Real > 0} \tag{5.5}$$

5.4. Derivation Of Optimization Equation

5.4.1. First Partial Derivative

The first partial derivative of Eq. 5.4 with respect to any variable P_i is found. Then, a general solution for all P_i is determined such that the the first partial derivative is equal to zero for each P_i. From Eq. 5.1,

$$P_N = \frac{P_s - \sum_{i=1}^{N-1} G_i P_i}{G_N} \tag{5.6}$$

From Eq. 5.4,

$$D = \sum_{i=1}^{N-1} \frac{K_i}{P_i} + \frac{K_N}{P_N} \tag{5.7}$$

$$D = \sum_{i=1}^{N-1} \frac{K_i}{P_i} + \frac{G_N K_N}{P_s - \sum_{i=1}^{N-1} G_i P_i} \tag{5.8}$$

$$\frac{\partial D}{\partial P_i} = -\frac{K_i}{{P_i}^2} + \frac{G_N K_N G_i}{\left(P_s - \sum_{i=1}^{N-1} G_i P_i\right)^2} \tag{5.9}$$

Setting the derivative equal to zero,

$$\frac{\partial D}{\partial P_i} = 0 \tag{5.10}$$

$$\frac{P_i^2}{K_i} = \frac{\left(P_s - \sum_{i=1}^{N-1} G_i P_i\right)^2}{G_N K_N G_i} \cdot \frac{G_N}{G_N} \tag{5.11}$$

$$\frac{P_i^2}{K_i} = \frac{G_N}{K_N G_i} \cdot \left(\frac{P_s - \sum_{i=1}^{N-1} G_i P_i}{G_N}\right)^2 \tag{5.12}$$

$$\frac{P_i^2}{K_i} = \frac{G_N}{K_N G_i} \cdot (P_N)^2 \tag{5.13}$$

$$\frac{P_i^2 G_i}{K_i} = \frac{P_N^2 G_N}{K_N} \tag{5.14}$$

$$P_i = P_N \sqrt{\frac{G_N K_i}{G_i K_N}} \tag{5.15}$$

From Eq. 5.1 and Eq. 5.15,

$$\sum_{i=1}^{N} G_i \left(P_N \sqrt{\frac{G_N K_i}{G_i K_N}} \right) = P_s \tag{5.16}$$

$$P_N = \frac{P_s}{\sum_{i=1}^{N} G_i \sqrt{\frac{G_N K_i}{G_i K_N}}} \tag{5.17}$$

$$P_N = \frac{P_s \sqrt{K_N}}{\sqrt{G_N} \sum_{i=1}^{N} \sqrt{G_i K_i}} \tag{5.18}$$

From Eq. 5.15 and Eq. 5.18,

$$P_i = \left(\frac{P_s \sqrt{K_N}}{\sqrt{G_N} \sum_{i=1}^{N} \sqrt{G_i K_i}} \right) \sqrt{\frac{G_N K_i}{G_i K_N}} \tag{5.19}$$

The total cost D is minimized when each variable P_i is scaled according to

$$\boxed{P_i = \frac{P_s \sqrt{K_i}}{\sqrt{G_i} \sum_{i=1}^{N} \sqrt{G_i K_i}}} \tag{5.20}$$

5.4.2. Second Derivative and Boundary Tests

The second derivative is determined to confirm the concavity of the solution region. The second partial derivative is

$$\frac{\partial^2 D}{\partial {P_i}^2} = \frac{2K_i}{{P_i}^3} + \frac{2 G_N K_N G_i^2}{\left(P_s - \sum_{i=1}^{N-1} G_i P_i \right)^3} \tag{5.21}$$

Because of the constraints of Eq. 5.5, $P_s - \sum_{i=1}^{N-1} G_i P_i > 0$, and thus the second derivative is positive with respect to all variables.

$$\frac{\partial^2 D}{\partial {P_i}^2} > 0 \tag{5.22}$$

From Eq. 5.1 and Eq. 5.5 the theoretical maximum values of each P_i can be determined by setting all other P_i values to zero which yields the 'noise corners'

$$P_i < \frac{P_s}{G_i} \tag{5.23}$$

Taking the limit of Eq. 5.4 as any value of P_i approaches its 'noise corner' yields

$$\lim_{P_i \to \frac{P_s}{G_i}} D = \infty \tag{5.24}$$

The theoretical minimum values for each P_i are limited by the physical nature of the problem as given in Eq. 5.5 such that

$$P_i > 0 \tag{5.25}$$

Taking the limit of Eq. 5.4 as any value of P_i approaches zero yields

$$\lim_{P_i \to 0} D = \infty \tag{5.26}$$

The minimum value of the cost function D is not contained on the boundaries of the solution region; the second partial derivative with respect to any variable P_i in the solution region is always positive; and there exists a single solution as given in Eq. 5.20 for which the first partial derivative with respect to all variables P_i is zero. Therefore, it is reasonable to conclude that the solution provided in Eq. 5.20 is the global minimum.

5.5. Minimum Cost and Equivalent Total Noise

5.5.1. Minimum Optimized Cost

When individual noise sources are scaled accordingly to Eq. 5.20, the theoretical relative minimum cost of achieving the noise performance specification can be expressed as

$$D = \sum_{i=1}^{N} \frac{K_i}{P_i} = \sum_{i=1}^{N} \frac{K_i}{\left(\frac{P_s \sqrt{K_i}}{\sqrt{G_i} \sum_{i=1}^{N} \sqrt{G_i K_i}} \right)} \tag{5.27}$$

$$\boxed{D = \frac{\left(\sum_{i=1}^{N} \sqrt{K_i G_i} \right)^2}{P_s}} \tag{5.28}$$

5.5.2. Equivalent Total Noise

From the minimized cost of Eq. 5.28, the abstract quantity of an equivalent total noise can be considered. Since the units of D are the inverse of total rms noise voltage squared, an equivalent total noise can be useful in some situations as will be discussed in later sections.

From Eq. 5.28, it is easy to determine the relative consequences of different gain scaling arrangements. For example, for cascaded gain stages such as $G_1 = A_{v1}^2 A_{v2}^2 A_{v3}^2$, $G_2 = A_{v2}^2 A_{v3}^2$ and $G_3 = A_{v3}^2$, it is easy to prove the advantage of having most of the total gain at the first stage A_{v1} from a noise (or even distortion) perspective.

5.6. kT/C Capacitor Area Optimization

Another noise budgeting problem for which Eq. 5.4 is suited is for capacitor sizing for kT/C noise in discrete-time switched-capacitor circuits. Given a noise specification, capacitor sizes can be determined that meet that specification with the minimum total capacitance, therefore die area.

The total in-band kT/C noise for a certain ADC [12] is given by

$$P_s = 2kT\left[\frac{0.25}{Cs_{11}} + \frac{7.4\times10^{-3}}{Cs_{12}} + \frac{1.1\times10^{-3}}{Cs_{21}} + \frac{1.6\times10^{-5}}{Cs_{22}} + \frac{1.6\times10^{-6}}{Cs_{31}} + \frac{2.9\times10^{-7}}{Cs_{32}} + \frac{8.1\times10^{-7}}{Cf_{31}}\right]. \tag{5.29}$$

The total noise specification is given as $P_s = 80.7\times10^{-12}$ mean squared volts. Eq. 5.20, with all $K_i = 1$, provides the capacitor values for the minimum total capacitance. Cost is minimized by setting $Cs_{11} = 3.2\times10^{-11}F$, $Cs_{12} = 5.5\times10^{-12}F$, $Cs_{21} = 2.1\times10^{-12}F$, $Cs_{22} = 2.6\times10^{-13}F$, $Cs_{31} = 8.1\times10^{-14}F$, $Cs_{32} = 3.5\times10^{-14}F$, and $Cf_{31} = 5.8\times10^{-14}F$. This provides a total minimum capacitance of $C_{total} = 4.0\times10^{-11}F$. This optimization was performed instantly with only a few lines of code, but it could have just as easily have been done by hand. Capacitance values which fall below a minimum unit capacitance can be replaced with the minimum capacitance, subtracted from the noise specification.

It is important to note that the total capacitance could have been calculated without calculating the individual capacitances by use of Eq. 5.28 which can be expressed as

$$\boxed{C_{total} = \frac{2kT\left(\sum_{i=1}^{N}\sqrt{G_i}\right)^2}{P_s}} \tag{5.30}$$

This can provide a convenient means to evaluate the relative cost in capacitor area for different gain scaling schemes.

6. LOW-NOISE AMPLIFIER DESIGN

6.1. Introduction

This chapter introduces analysis and design techniques for low-noise, low-voltage, continuous-time, resistor divider feedback, audio preamplifier gain stages.

6.2. Resistor Divider Feedback Amplifier

The ubiquitous resistor divider feedback amplifier is used for the gain stages of the vast majority of audio preamplifer systems including PGAs [1]. Noise analysis is performed here for different configurations, gain settings, and as functions of other related design parameters.

6.2.1. Resistor Noise Sources

The variable gain amplification stages include feedback resistors and gain-changing switch on-resistances, all of which contribute to the overall circuit resistor noise. For this work, gain changing switch resistances, R_{sw}, are designed to be low enough such that that they do not contribute significantly to the overall resistor noise. This switch sizing is also done in order to reduce the distortion generated by nonlinear effects in the switch resistance. Other resistor noise sources, including pad resistance noise, are taken into account for simulations but do not significantly contribute to the overall noise. Thus, resistor noise is dominated by the feedback resistors of the three amplifying stages.

6.2.2. Feedback Resistor Noise

Gain settings are changed by turning on individual switches for each of the gain settings. Each switch is connected to a different node in a string of resistors on one end, and to the inverting input of an opamp on the other end. Gain settings are changed by changing the ratio of feedback resistors, R_f/R_i, where $R_i + R_f$ is constant for all gain settings. This arrangement is important for low distortion and monotonic gain changes with this low-voltage circuit. The feedback resistor noise power, referred to the input of the opamp (or IRN), is given by

$$P_{nRf} = 4kT(R_i \| R_f) \triangle f. \tag{6.1}$$

The way that $R_i \| R_f$ varies with gain is different for inverting and non-inverting stages and will be presented in following sections.

6.2.3. Low Frequency Response

For DC decoupled stages, such as the first two amplifier stages of this project, the off-chip capacitors C_{OC}, and the variable input resistance R_i for each gain setting form RC time constants which set the frequencies of the low-frequency poles. This results in each of these stages high-pass-filtering the signal with variable pole frequencies. Since the off-chip capacitors must be limited to fixed practical maximum values, and since the low-frequency side of the signal bandwidth much be kept sufficiently low, there exists a practical minimum value for R_i designated R_{imin}. Setting R_i to a higher value than R_{imin} has the distinct advantages of decreasing the required off-chip capacitor values and increasing the amplifier load resistance. However, as is demonstrated later, for the target specifications of this project, even with input resistances set to the minimum value R_{imin}, there is

little noise budget remaining for opamp noise and thus this value of R_{imin} is used for this design.

Since the off chip capacitor values, C_{OC} and the maximum low-frequency pole frequencies, f_{LFmax}, are fixed by practical limitations, the minimum input resistor values can be expressed as a function of these constants:

$$R_{imin} = \frac{1}{2\pi f_{LFmax} C_{OC}}. \tag{6.2}$$

For this project, because the first stage gain is not dynamically changing as is the case for the second stage, the first stage pole frequency, f_{LFmax1}, is chosen such that it is a decade higher than that of the second stage f_{LFmax2}:

$$f_{LFmax1} = 10 f_{LFmax2}. \tag{6.3}$$

This is done so that the effects of the constantly changing bandwidth caused by the PGA are not noticeable.

The minimum input resistance values are set to $R_{i1} = 500\Omega$ and $R_{i2} = 5k\Omega$. With the values of both off-chip capacitors set to $C_{OC} = 2\mu F$, $f_{LFmax1} = 160Hz$ and $f_{LFmax2} = 16Hz$. Note that although this puts the lower 3dB frequency above 20Hz, this is common for portable recording devices where proximity effects and other undesired low-frequency signal coupling effects are dealt with by setting the low-frequency cutoff frequency similarly above 20Hz. If needed, increasing the bandwidth for microphone recording can be achieved by increasing the off-chip capacitor values. If a line-in signal were inserted directly to input of the second stage, as previously discussed as a possible use, the low frequency cutoff would be limited only by the second stage frequency response and would provide full audio bandwidth down to below $20Hz$.

6.2.4. Non-Inverting Stage

For a non-inverting resistor-string-switching amplifying stage such as the first stage in this project, $(R_i \| R_f)_{ni}$ can be expressed as a function of R_{imin}, the particular signal power gain setting G_s, and the maximum signal power gain setting G_{max}:

$$(R_i \| R_f)_{ni} = \frac{(\sqrt{G_s} - 1) R_{imin} \sqrt{G_{max}}}{G_s}. \tag{6.4}$$

Substituting the expression for R_{imin} from Eq. 6.2 yields an expression for $(R_i \| R_f)_{ni}$ as a function of C_{OC}, f_{LFmax}, the particular signal power gain setting G_s, and the maximum signal power gain setting G_{max}:

$$(R_i \| R_f)_{ni} = \frac{(\sqrt{G_s} - 1) \sqrt{G_{max}}}{2\pi f_{LFmax} C_{OC} G_s}. \tag{6.5}$$

6.2.5. Inverting Stage

Similarly, for an inverting resistor-string-switching amplifying stage such as the second stage in this project, $(R_i \| R_f)_i$ can be expressed as a function of R_{imin}, the particular signal power gain setting G_s, and the maximum signal power gain setting G_{max}:

$$(R_i \| R_f)_i = \frac{\sqrt{G_s} R_{imin} (1 + \sqrt{G_{max}})}{(\sqrt{G_s} + 1)^2}. \tag{6.6}$$

The distinction between the signal power gain P_s and the noise power gain P_n is important here because they are different quantities for an inverting stage.

Substituting the expression for R_{imin} of Eq. 6.2 yields an expression for $(R_i \| R_f)_i$ as a function of C_{OC}, f_{LFmax}, the particular signal power gain setting G_s, and the maximum signal power gain setting G_{max}:

$$(R_i \| R_f)_i = \frac{\sqrt{G_s}(1+\sqrt{G_{max}})}{2\pi f_{LFmax} C_{OC}(\sqrt{G_s}+1)^2}. \tag{6.7}$$

6.3. Basic Two-Stage Opamp Noise

A basic two-stage opamp is shown in Fig. 6.1. The output referred noise current can be expressed as

$$i_{orn}^2 = A_{v1}^2 \left(g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m3}^2 v_{n3}^2 + g_{m4}^2 v_{n4}^2\right) + g_{m6}^2 v_{n6}^2 + g_{m7}^2 v_{n7}^2 \tag{6.8}$$

where A_{v1} is the voltage gain of the first stage. Referring the noise to the input,

$$v_{irn}^2 = \frac{g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m3}^2 v_{n3}^2 + g_{m4}^2 v_{n4}^2}{g_{m1}^2} + \frac{g_{m6}^2 v_{n6}^2 + g_{m7}^2 v_{n7}^2}{A_{v1}^2 g_{m1}^2}. \tag{6.9}$$

The magnitude of $A_{v1}^2 g_{m1}^2$ is assumed to be large enough such that the noise contribution of $g_{m6}^2 v_{n6}^2 + g_{m7}^2 v_{n7}^2$ can be ignored such that

$$v_{irn}^2 = \frac{g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m3}^2 v_{n3}^2 + g_{m4}^2 v_{n4}^2}{g_{m1}^2}. \tag{6.10}$$

Taking matching into account

$$v_{irn}^2 = 2\left[v_{n1}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 v_{n3}^2\right]. \tag{6.11}$$

Defining the large signal constraint dependent term

$$g_{mr3} \equiv \frac{g_{m3}}{g_{m1}}, \tag{6.12}$$

$$v_{irn}^2 = 2\left[v_{n1}^2 + g_{mr3}^2 v_{n3}^2\right]. \tag{6.13}$$

Since M1 and M3 share the same bias current, the term g_{mr3} can be expressed in terms of $\triangle_3$ and $\triangle_1$ as

$$g_{mr3} = \frac{g_{m3}}{g_{m1}} = \frac{\left(\frac{2I_D}{\triangle_3}\right)}{\left(\frac{2I_D}{\triangle_1}\right)} = \frac{\triangle_1}{\triangle_3}. \tag{6.14}$$

6.3.1. Thermal Noise

With $v_{nT}^2 = \frac{K_T}{g_m}$, the input referred thermal noise is

$$v_{irnT}^2 = 2\left[\frac{K_T}{g_{m1}} + g_{mr3}^2\frac{K_T}{g_{m3}}\right] = \frac{2K_T}{g_{m1}}\left(1 + g_{mr3}\right), \tag{6.15}$$

which in terms of transconductance ratios is

$$v_{irnT}^2 = \frac{K_T \triangle_1}{I_D}\left(1 + \frac{\triangle_1}{\triangle_3}\right). \tag{6.16}$$

6.3.2. Flicker Noise

Input referred flicker noise is

$$v_{irnF}^2 = 2\left[\frac{K_{f1}}{A_1} + g_{mr3}^2\frac{K_{f3}}{A_3}\right], \tag{6.17}$$

which in terms of transconductance ratios is

$$v_{irnF}^2 = 2\left[\frac{K_{f1}}{A_1} + \left(\frac{\triangle_1}{\triangle_3}\right)^2\frac{K_{f3}}{A_3}\right]. \tag{6.18}$$

If the areas are optimized according to the optimization equation, then the flicker noise as a function of the total gate area of the differential pair input and load transistors is given as

$$v_{irnF}^2 = \frac{2\left(\sqrt{2K_{f1}} + \sqrt{K_{f3}\left(\frac{\triangle_1}{\triangle_3}\right)^2}\right)^2}{A_{Total}} \tag{6.19}$$

where $A_{Total} = A_1 + A_2 + A_3 + A_4$.

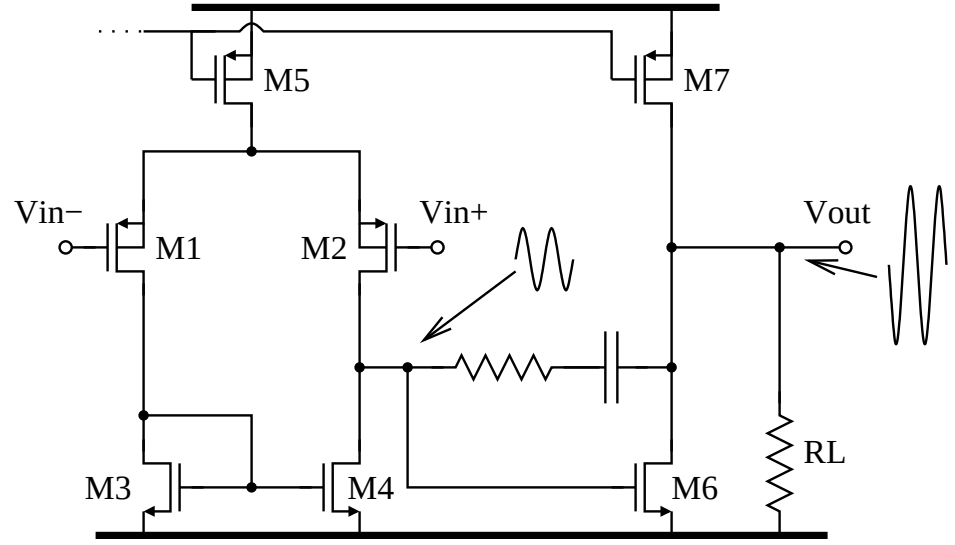

FIGURE 6.1. Basic Two-Stage Opamp

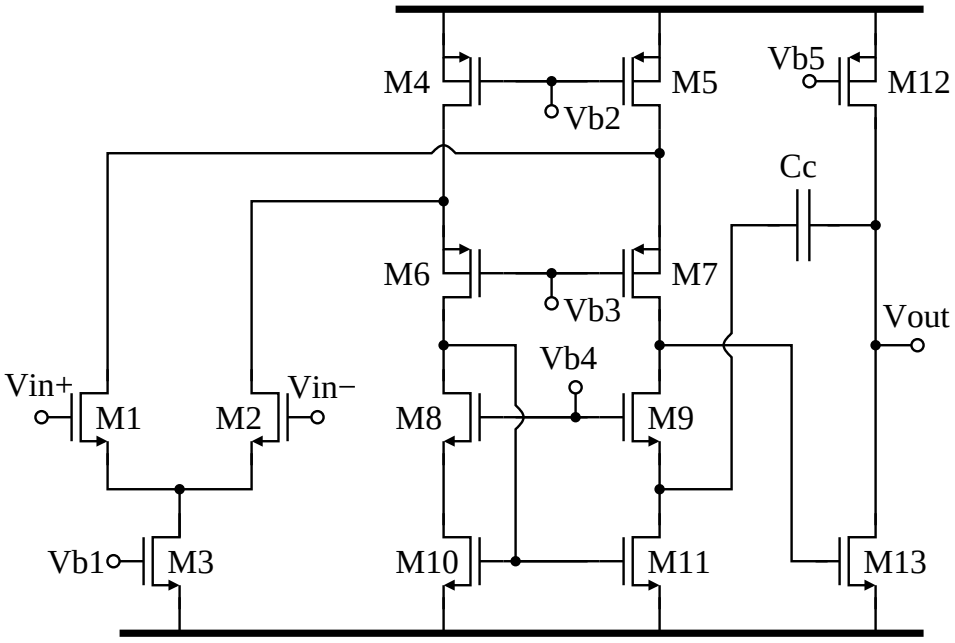

FIGURE 6.2. Two-Stage Folded Cascode

6.4. Folded Cascode Opamp Noise

A folded cascode opamp is shown in Fig. 6.2. Although the basic folded cascode is shown with an additional second stage, with sufficient gain the noise performance is approximately the same.

The output referred noise current is

$$i_{orn}^2 = g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m4}^2 v_{n4}^2 + g_{m5}^2 v_{n5}^2 + G_{m6}^2 v_{n6}^2 + G_{m7}^2 v_{n7}^2 + G_{m8}^2 v_{n8}^2 + G_{m9}^2 v_{n9}^2 + g_{m10}^2 v_{n10}^2 + g_{m11}^2 v_{n11}^2. \quad (6.20)$$

By symmetry and assuming good matching,

$$i_{orn}^2 = 2\left(g_{m1}^2 v_{n1}^2 + g_{m5}^2 v_{n5}^2 + G_{m7}^2 v_{n7}^2 + G_{m9}^2 v_{n9}^2 + g_{m11}^2 v_{n11}^2\right). \quad (6.21)$$

The effective transconductance of the cascoded devices can be expressed as

$$G_{m7} = \frac{g_{m7}}{1 + g_{m7}(r_{d1} \| r_{d5})} \quad (6.22)$$

and

$$G_{m9} = \frac{g_{m9}}{1 + g_{m9} r_{d11}}. \quad (6.23)$$

For higher frequencies, parasitic capacitances can cause noise from these devices to increase. However, for audio frequencies, this will not be a problem. Since $g_m r_d \gg 1$, $G_m \approx 1/r_d$, and $gm^2 \gg Gm^2$, the noise contribution from the cascode devices is negligible and need not be considered for noise optimization purposes. However, like all such assumptions, this assumption should be checked upon implementation to ensure that a sufficient allowance for these and other additional noise sources has been made. The output current noise expression can be simplified as

$$i_{orn}^2 = 2\left(g_{m1}^2 v_{n1}^2 + g_{m5}^2 v_{n5}^2 + g_{m11}^2 v_{n11}^2\right). \quad (6.24)$$

Dividing by the input device transconductance squared yields the input referred noise

$$v_{irn}^2 = \frac{i_{orn}^2}{g_{m1}^2} = 2\left[v_{n1}^2 + \left(\frac{g_{m5}}{g_{m1}}\right)^2 v_{n5}^2 + \left(\frac{g_{m11}}{g_{m1}}\right)^2 v_{n11}^2\right]. \quad (6.25)$$

Defining

$$gmr_5 \equiv \frac{g_{m5}}{g_{m1}} \tag{6.26}$$

and

$$gmr_{11} \equiv \frac{g_{m11}}{g_{m1}}, \tag{6.27}$$

the total input referred noise can be expressed in terms of transconductance ratios as

$$v_{irn}^2 = 2\left(v_{n1}^2 + gmr_5^2 v_{n5}^2 + gmr_{11}^2 v_{n11}^2\right). \tag{6.28}$$

Note the strong dependence on the transconductances ratios gmr_5 and gmr_{11}. These transconductance ratios are determined by the current distribution between M1 and M11, large signal constraints, and the device inversion limits.

6.4.1. Current Distribution

The current distribution between M1 and M11 is accounted for as

$$I_5 = I_1 + I_{11}. \tag{6.29}$$

Let

$$I_R \equiv \frac{I_1}{I_{11}} \tag{6.30}$$

such that

$$I_1 = I_R I_{11} \tag{6.31}$$

and

$$I_5 = I_{11}\left(1 + I_R\right). \tag{6.32}$$

Thus,

$$g_{m1} = \frac{2I_1}{\triangle_1} = \frac{2I_R I_{11}}{\triangle_1}, \tag{6.33}$$

$$g_{m5} = \frac{2I_5}{\triangle_5} = \frac{2I_{11}\left(1 + I_R\right)}{\triangle_5}, \tag{6.34}$$

$$g_{m11} = \frac{2I_{11}}{\triangle_{11}}, \tag{6.35}$$

$$g_{mr5} = \frac{\triangle_1}{\triangle_5}\left(1 + \frac{1}{I_R}\right), \tag{6.36}$$

and

$$g_{mr11} = \frac{\triangle_1}{\triangle_{11}}\left(\frac{1}{I_R}\right). \tag{6.37}$$

6.4.2. Thermal Noise

The total input referred thermal noise is

$$v_{irnT}^2 = 2\left(\frac{K_T}{g_{m1}} + gmr_5^2\frac{K_T}{g_{m5}} + gmr_{11}^2\frac{K_T}{g_{m11}}\right), \tag{6.38}$$

simplifying to

$$v_{irnT}^2 = \frac{2K_T}{g_{m1}}\left(1 + g_{mr5} + g_{mr11}\right). \tag{6.39}$$

This can be expressed in terms of $\triangle$s as

$$v_{irnT}^2 = \frac{K_T\triangle_1}{I_R I_{11}}\left[1 + \frac{\triangle_1}{\triangle_5}\left(1 + \frac{1}{I_R}\right) + \frac{\triangle_1}{\triangle_{11}}\left(\frac{1}{I_R}\right)\right]. \tag{6.40}$$

6.4.3. Flicker Noise

The total input referred flicker noise is

$$v_{irnf}^2 = 2\left(\frac{K_{f1}}{A_1} + gmr_5^2\frac{K_{f5}}{A_5} + gmr_{11}^2\frac{K_{f11}}{A_{11}}\right), \tag{6.41}$$

which can be expressed as

$$v_{irnf}^2 = 2\left[\frac{K_{f1}}{A_1} + \left(\frac{\triangle_1}{\triangle_5}\left(1+\frac{1}{I_R}\right)\right)^2\frac{K_{f5}}{A_5} + \left(\frac{\triangle_1}{\triangle_{11}}\left(\frac{1}{I_R}\right)\right)^2\frac{K_{f11}}{A_{11}}\right]. \tag{6.42}$$

6.5. Leveraged Current Mirror Opamp Noise

A leveraged current mirror opamp, similar to that as presented in [13], is shown in Fig. 6.3. The current ratios are such that

$$K_2K_3 = K_1. \tag{6.43}$$

Output referred noise can be expressed as

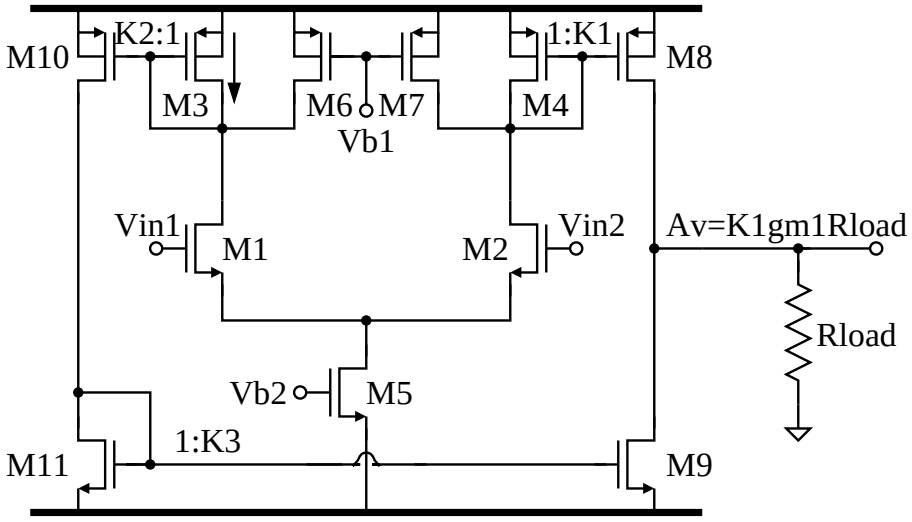

FIGURE 6.3. Leveraged Current Mirror Opamp

$$i_{orn}^2 = 2K_1^2\left(g_{m1}^2 v_{n1}^2 + g_{m3}^2 v_{n3}^2 + g_{m6}^2 v_{n6}^2\right) + K_3^2\left(g_{m10}^2 v_{n10}^2 + g_{m11}^2 v_{n11}^2\right) + g_{m8}^2 v_{n8}^2 + g_{m9}^2 v_{n9}^2. \tag{6.44}$$

Input referred noise can be expressed as

$$v_{irn}^2 = \frac{2K_1^2\left(g_{m1}^2 v_{n1}^2 + g_{m3}^2 v_{n3}^2 + g_{m6}^2 v_{n6}^2\right) + K_3^2\left(g_{m10}^2 v_{n10}^2 + g_{m11}^2 v_{n11}^2\right) + g_{m8}^2 v_{n8}^2 + g_{m9}^2 v_{n9}^2}{K_1^2 g_{m1}^2}. \tag{6.45}$$

6.5.1. Current Distribution

In order to provide good current mirroring and to avoid amplifying the noise from M10 and M11, the current distribution is set such that $K_2 = 1$ and $K_3 = K_1$ such that

$$v_{irn}^2 = 2\left(v_{n1}^2 + g_{mr3}^2 v_{n3}^2 + g_{mr6}^2 v_{n6}^2\right) + g_{mr10}^2 v_{n10}^2 + g_{mr11}^2 v_{n11}^2 + \frac{g_{mr8}^2 v_{n8}^2 + g_{mr9}^2 v_{n9}^2}{K_1^2}. \tag{6.46}$$

Unfortunately, the current mirror ratio needs to be relatively small such that all devices must be considered. This is not a preferable topology for low noise, however, it has its merits for driving a low-impedance load.

7. PREAMPLIFIER AND PGA SYSTEM DESIGN

7.1. Introduction

A noise optimized preamplifier system is systematically optimized to meet the noise performance specification most cost effectively. This preamplifier is fabricated in a $0.35\mu m$ CMOS process.

7.2. Methodology

The design is performed according to the following sequence with some iteration as needed:

1. Identify all known parameters to reduce the 'degrees of freedom'.
2. Determine total resistor noise as a function of gain.
3. Compare resistor noise to the specification noise at each gain setting to identify to the gain setting at which the noise specification is most difficult to meet.
4. Determine the opamp noise budget for the most difficult gain setting by subtracting the resistor noise from the specification noise at that setting.
5. Use the optimization equation Eq. 5.4 to scale the opamp noise.
6. Design each opamp using the optimization equation Eq. 5.4.
7. Reiterate opamp noise scaling as needed.

7.3. Opamp Requirements

Some assumptions need to be made as to other opamp performance parameters as discussed in this section.

7.3.1. Gain Bandwidth Product

The audio bandwidth upper limit is $\sim 20kHz$, so there must be sufficient gain at that frequency for acceptable distortion performance. The goal is to have $20dB$ of loop gain, i.e. gain beyond the signal gain, for each amplifier stage and at each gain setting. Distortion is difficult to predict, but with adequate loop gain and slew rate the distortion level is likely to be acceptable, or close enough not to invalidate the noise optimization work that follows. With this in mind, the goal is to get as close as possible to $GBP_1 \sim 2MHz$, $GBP_2 \sim 2.8MHz$, and $GBP_3 \sim 0.3MHz$. These gain bandwidth products are not trivial to achieve considering that these amplifiers are driving low-impedance loads without efficient output stages such as source-followers.

7.3.2. Slew Rate

Distortion generated by inadequate slew rates can be significant for audio designs. The minimum slew rate requirements can be expressed as a function of the peak-to-peak output signal level and the maximum frequency and will be the same for all three amplifiers:

$$V_{out} = \frac{V_{pp}}{2} \sin(2\pi f_{max} t). \tag{7.1}$$

$$\frac{\partial V_{out}}{\partial t} = \pi f_{max} V_{pp} \cos(2 f_{max} t) \tag{7.2}$$

is maximized when $t = 0$ which gives the minimum slew rate

$$SR = \frac{\partial V_{out}}{\partial t}|_{t=0} = \pi f_{max} V_{pp} \tag{7.3}$$

in order to avoid slew rate induced distortion for the entire audio band $f_{max} \geq 20kHz$. With $V_{pp} = 0.4V$,

$$SR \geq 0.0251 \frac{V}{\mu s}. \tag{7.4}$$

Although maintaining a minimum slew rate $0.0251 \frac{V}{\mu s}$ would theoretically eliminate slew limiting distortion for a single sinusoid, maintaining low intermodulation distortion requires a faster slew rate. A slew rate of $SR = 0.1 \frac{V}{\mu s}$, calculated for $f_{max} = 80kHz$, will provide better distortion performance [1], but this value is considered more of a goal than a requirement.

7.3.3. Operating in Moderate and Weak Inversion

Batteries spend a very small percentage of their lifetime in the vicinity of $0.9V$ and much of it at or above $1V$. Therefore, for large signal considerations it is better to design for the higher $1V$ supply and then check if performance at $0.9V$ has been compromised more than allowed by the relaxed specifications for that supply voltage.

The approach to choosing device operating regions is to bias the opamp input devices close to weak inversion to maximize the g_m/I_d ratio while biasing current mirroring devices in moderate to strong inversion as topology allows.

The closer a device is biased towards weak inversion, the worse it performs as a current mirror. By biasing devices too 'tightly' DC offsets can increase and use up the the extra signal swing to offsets caused by poor mirroring. The desire

is to keep all devices in saturation for the $1V$ case and not worry so much about the $0.9V$ case as long as devices are not cut off.

The techniques for sizing transistors for optimal g_m/I_d ratios, such as presented in [4], are useful for opamp optimization.

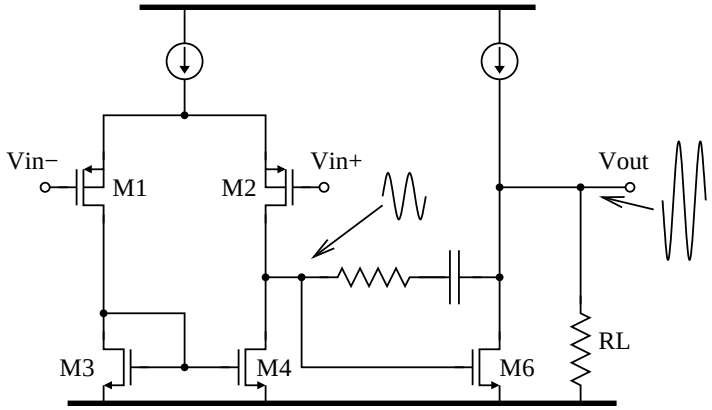

FIGURE 7.1. Two stage opamp illustrating the signal swing problem from insufficient M6 voltage gain

7.3.4. Driving Low Resistance Loads

With operation required down to a 0.9V supply, unity gain common source buffers are not an option. Two-stage opamps, as shown in Fig. 7.1, can have some major problems driving low reististance loads without a source follower. With a variable resistive load, the loop gain changes with the load resistance. With the Miller effect, this causes the pole frequency of the compensation capacitor to change with the load resistance. At any gain setting, the gain of the output stage is relatively low and so the Miller effect is not as advantageous, causing compensation capacitors to be larger than would be typically required. A low voltage gain for the output device M6 resulted in the gate of $M6$ swinging when

it had little room to do so with it being connected to the small common mode range differential pair.

Alternative opamps were considered such as the folded cascode, Fig. 6.2, and particularly the leveraged current mirror opamp, Fig. 6.3, which are superior for driving these low resistive loads with a low supply voltage. However, they are inferior from a noise perspective. They could be placed inside a gain nesting structure, Fig. 7.2, for low noise and sufficient gain overall. However, since the focus of this research was on noise optimization, and since there are compensation risks for nested gain stages, the basic two-stage opamp was chosen for this design.

Nested gain structures which allow for a low noise opamp optimized for that purpose alone and a low resistance driving opamp optimized for that purpose to work together in a combined structure would make for interesting future work.

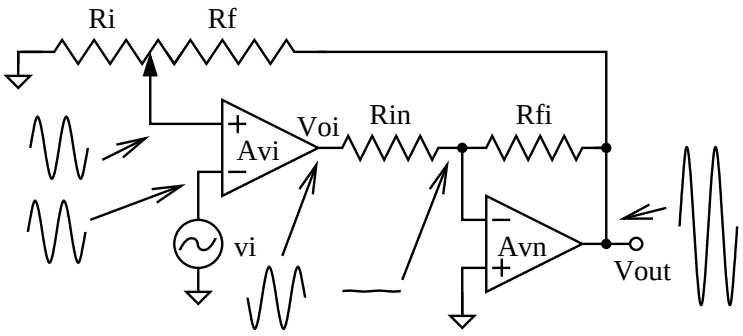

FIGURE 7.2. Nested inverting gain stage

7.4. Total Resistor Noise

Here the total resistor noise is determined as a function of gain and compared to the specification.

The total resistor output referred noise (ORN) as a function of the total system signal gain settings is shown in Fig. 7.3. This plot is a result of a MATLAB

simulation which uses the above derivations of resistor string noise and corresponds well to HSPICE simulations. Third stage feedback resistor values are set to $5k\Omega$, although the total noise is not strongly dependent on their values. Also included in the simulations are the small switch resistance values, as determined from HSPICE simulations, as well as predicted pad and other parasitic resistance. These small resistance values do not significantly contribute to the total resistor ORN.

Note that the dominant amplification stage resistor noise changes at the $36dB$ setting, and that the 3rd stage resistance only contributes significantly to the total noise at the lowest gain settings.

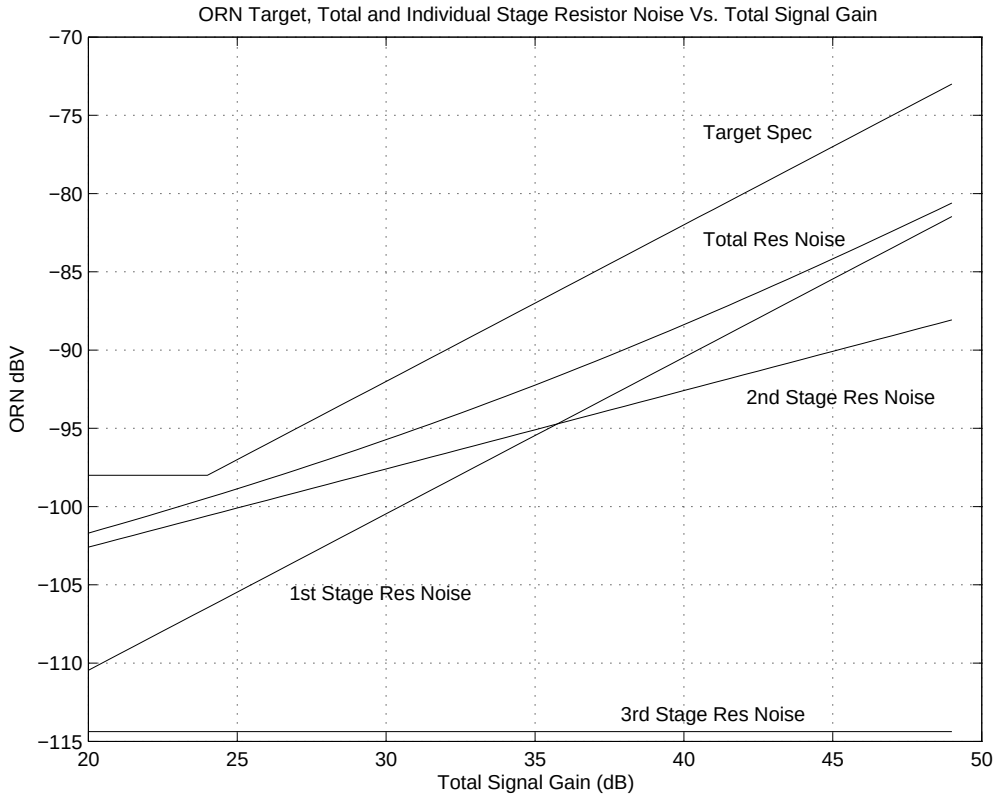

FIGURE 7.3. Total resistor ORN and individual contributions to the resistor ORN from the individual amplification stages for each total gain setting with the first stage fixed at 20dB

When compared to the ORN specification, it is clear that the close proximity of the total resistor noise to the specification curve in the region around the $24dB$ gain setting leaves a minimal noise budget for the total opamp noise.

7.5. Opamp Noise Budget

Here, the total combined opamp noise budget is determined.

The total opamp ORN noise budget can be found by subtracting the resistor noise power from the specification noise power as shown in Fig. 7.4. Note that the resulting opamp noise curve is not the ORN noise curve of the opamps, it is the maximum noise ORN noise level for different gain settings. In order to

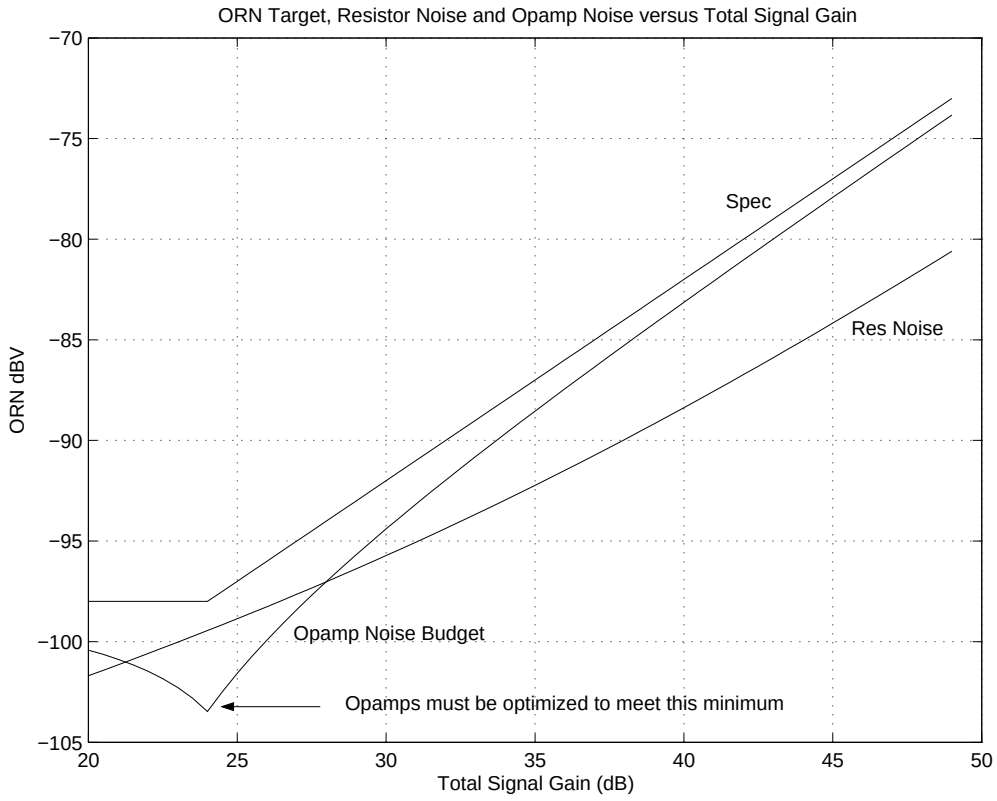

FIGURE 7.4. Opamp noise budget

find the optimum opamp noise scaling, i.e. individual opamp noise budgets, the optimization equation is employed in the next section.

7.6. Opamp Noise Scaling Optimization

Similar to the previous kT/C noise scaling example, opamp noise scaling is performed using Eq. 5.20. For optimization, it is assumed that there will be similar noise performance per unit cost such that all $K_i = 1$. This first optimization will provide an approximately optimized noise scaling and a good starting point for the design. Once opamp topologies are chosen for the individual stages based on the required noise performance and other factors, the noise scaling can be further refined by reoptimizing with appropriate K_i weighting factors if needed.

For each of the gain settings shown in Fig. 7.4 there exists an optimized opamp noise scaling which would satisfy the specification for minimum cost as shown in Fig. 7.5. However, individual opamp input referred noise (IRN) levels will be constant. At the 24dB gain setting, the specification is most difficult to achieve and so the opamp noise is optimized for that particular gain setting.

A comparison of the relative cost of meeting a particular gain setting is plotted in Fig. 7.6 and is normalized to the relative cost of meeting only the 49dB gain setting condition. This type of plot could be useful for considering the relative cost of a certain specification.

With the opamp noise scaled according to Eq. 5.20, the combined resistor and opamp noise is plotted in Fig. 7.7. Note that the total ORN performance greatly exceeds the specification except in the region of the 24dB setting where it is exactly met.

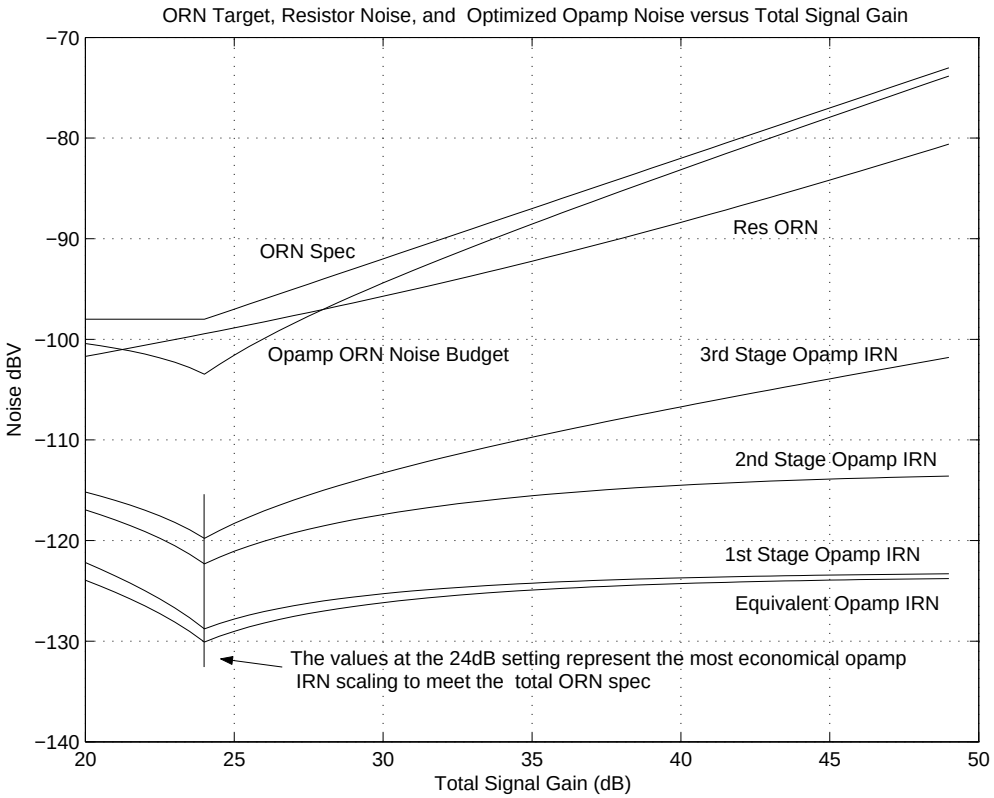

FIGURE 7.5. Opamp optimizations to meet particular points of the specification and equivalent opamp IRN versus total signal gain

The equivalent opamp noise curve, plotted in Fig. 7.7, is analogous to the total capacitance of the kT/C example. For example, if three similar (same topology, V_{dsat}, values etc..) differential pairs were sized to meet their optimized scaled noise specifications, then they would take the same area and bias current of a single differential pair which met the equivalent opamp specification. This is indeed an abstraction, but it has proven to be a useful optimization tool.

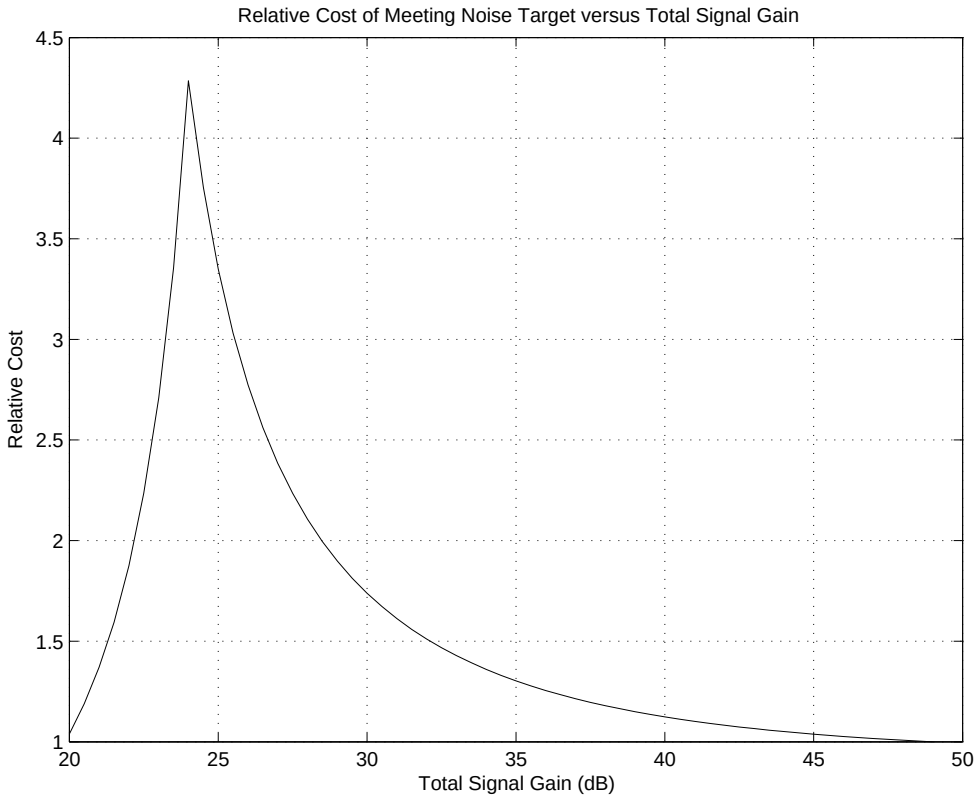

FIGURE 7.6. Relative cost of opamp noise in order to meet particular specification points normalized to the 49dB setting

7.7. Opamp Noise Specifications

For each of the gain settings shown in Fig. 7.4 there exists an optimized opamp noise scaling which would satisfy the specification for minimum cost as shown in Fig. 7.5. However, individual opamp IRN levels will be constant. At the $24dB$ gain setting, the specification is most difficult to achieve and so the total opamp noise is optimized for that gain setting.

The resulting optimized input referred noise targets are:

- First Stage: $-128.8dBV = 363nVrms = 132 \times 10^{-15}Vrms^2$
- Second Stage: $-122.4dBV = 759nVrms = 575 \times 10^{-15}Vrms^2$

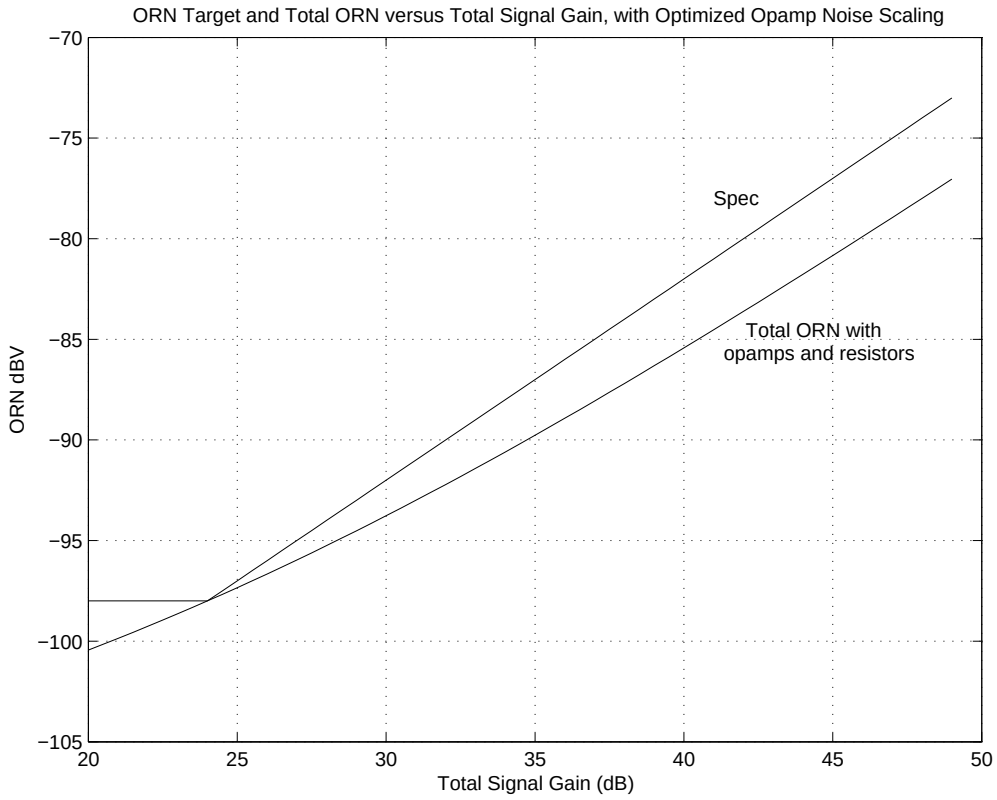

FIGURE 7.7. Total combined resistor and opamp ORN

- Third Stage: $-119.8dBV = 1023nVrms = 1047 \times 10^{-15}Vrms^2$
- Equivalent Opamp: $-130.1dBV = 312nVrms = 97.37 \times 10^{-15}Vrms^2$.

This particular noise scaling assumes identical structures and shall be changed if different structures are used according to the optimization equation.

7.8. Noise Optimized Standard Differential Pairs

With the noise IRN noise budget specifications for each opamp established, the opamps can be design to most efficiently meet those specifications

For a two stage opamp, the noise is dominated by the first stage differential pair which can be expressed as a simple function of area and power. As with this and similar designs, most cost and design focus is allocated to the reduction of noise. If other opamp performance parameters become more important, then this still provides a good reference point to start with. For minimum total gate area, the areas of the load transistors and the input transistors should be ratioed according to

$$\frac{A_3}{A_1} = \frac{KF_3' gm_R^2 + \sqrt{KF_1' KF_3' gm_R^2}}{KF_1' + \sqrt{KF_1' KF_3' gm_R^2}}, \tag{7.5}$$

where

$$KF_1' = \frac{2KF_1}{C_{ox1}} \int_{fl}^{fh} \frac{df}{f^{AF1}} \tag{7.6}$$

and

$$KF_3' = \frac{2KF_3}{C_{ox3}} \int_{fl}^{fh} \frac{df}{f^{AF3}} \tag{7.7}$$

are fixed device constants, and where $gm_R = \frac{gm_3}{gm_1}$ is available to the designer for optimization. This equation could be modified to take into account total device area as opposed to just gate area, however, this is approximately proportional to gate area for large, long length devices.

With optimized areas, the total noise of the optimized differential pair can be expressed as

$$P_n = \frac{1}{I_T}\left[\frac{2KT'(1+gm_R)}{\beta'}\right] + \frac{1}{A_T}\left[2KF_3' gm_R^2 + 4gm_R\sqrt{KF_1' KF_3'} + 2KF_1'\right] \tag{7.8}$$

where $\beta' = \frac{gm_1}{I_D}$ is also available to the designer for optimization.

The noise performance predicted by Eq. 7.8 was verified with HPICE simulations. It is important to maximize gm_1, and minimize gm_3 as much as possible

for the most economical noise performance without driving gm_1 too deeply into weak inversion for any simulation case. For non-low-voltage low-noise designs, it is common to see $M3$ sized with a very small W/L ratio in order to reduce gm_3 as much as possible for optimal performance. Unfortunately, for this low-voltage design, sizing $M3$ with a very small W/L ratio would increase the saturation voltage more than the supply common mode voltages can allow. This is why there is an exponential increase in cost for low-noise, low-voltage design as compared to higher voltage designs. Other topologies such as the folded cascode and leveraged current mirror opamps [13] start to rival the noise performance of this differential pair due to increased biasing headroom, but not enough for this design.

A practical strategy for this design is to set the total gate area to a maximum 'reasonable' size and then design for the minimum power consumption. Power consumption can be plotted as a function of total area for given noise specifications and design parameters. If it turns out that the thermal noise power overly dominates the flicker noise power, such that area is being needlessly consumed or if power consumption turns out to be sufficiently low, then the area can be reduced and the design performed again iteratively etc... Calculations can be performed quickly with MATLAB.

Total system optimization for minimum cost would require establishing a numerical relationship between the relative costs of power consumption (a marketability cost) and die area (a manufacturing cost). When there is no idea as to what is 'reasonable' for area or power consumption, it may be a useful starting point to equate the contributions of flicker and thermal noise power to the total noise power and see what values result. If either flicker noise or thermal noise power is an order of magnitude larger than the other, than either area or power is being wasted.

8. TEST RESULTS

8.1. Introduction

The measured performance of the preamplifier system is presented in this chapter. All measurements were made using an Audio Precision System-2 audio measurement system. A die photo annotated with the main circuit blocks is shown in Fig. 8.1.

8.2. Noise Performance

Fig. 8.2 presents noise measurement results for different gain settings along with simulation results and target specifications. Although, these measurements were performed with a supply voltage of $1.2V$, there is little noise sensitivity to supply voltage for the specified supply voltage range.

The measured IRN (Input Referred Noise) is approximately $-120dBA$ (dBV with A-weighting) and $-116dBV$, while the target was $-124dBA$ and $-122dBV$. The measured IRN and ORN (Output Referred Noise) versus gain curves are relatively linear as compared to the curved simulation results. This discrepancy and the increased noise level could be explained by more noise at the first stage than predicted by the simulations. Increased measured noise can also be attributed to larger than predicted resistor values, decreased noise model accuracy for devices operating in moderate to weak inversion, and to noise and interference sources not included in the simulations and yet present in the test chip and test system. Additional measurable opamp noise contributions due to device mismatch and unbalanced current mirroring is also possible. An increase

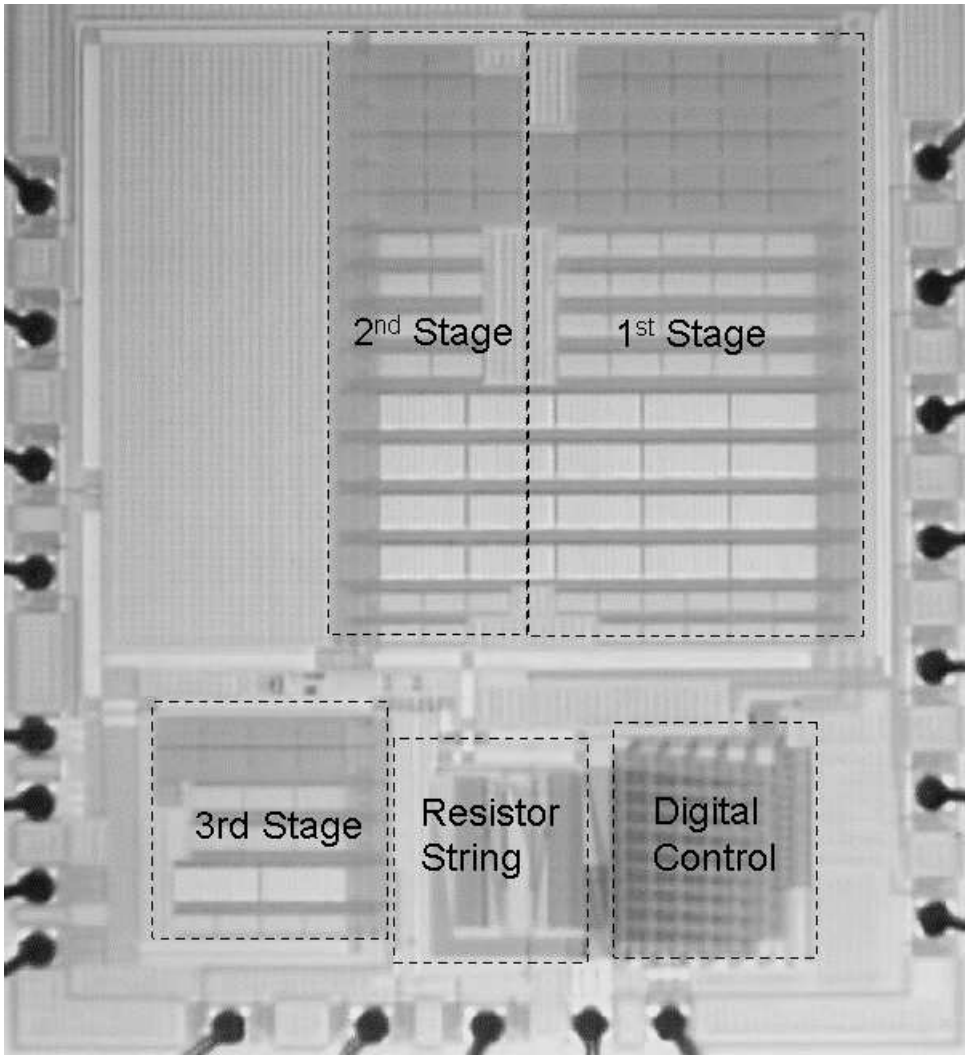

FIGURE 8.1. Annotated Die Photograph

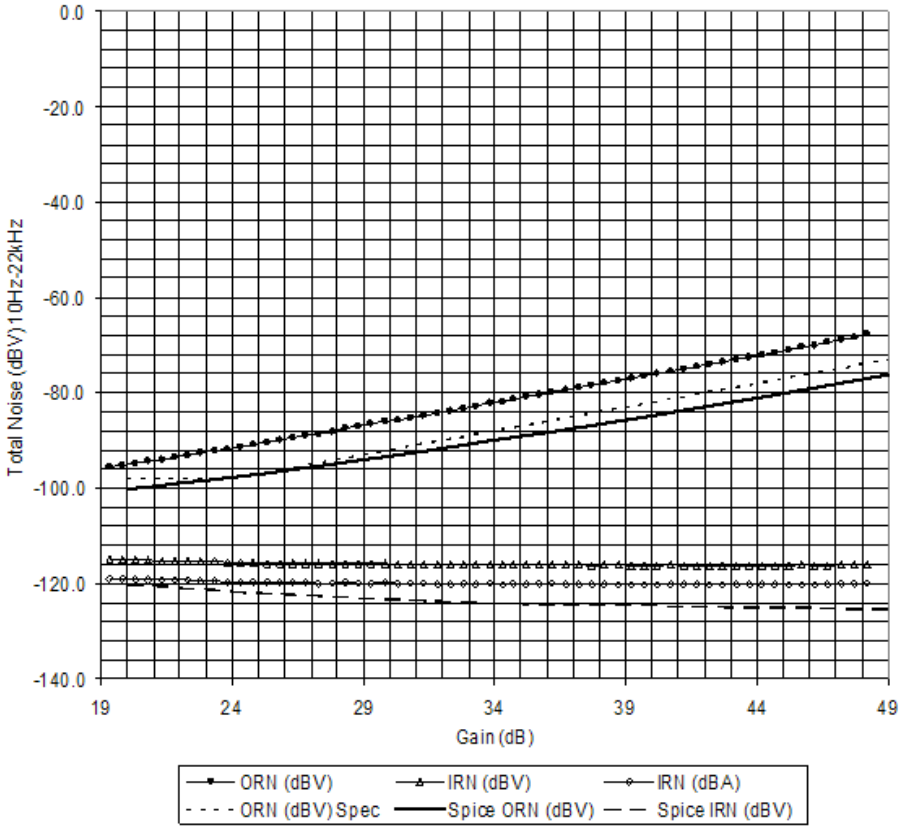

FIGURE 8.2. Measured Noise at Different Gain Settings.

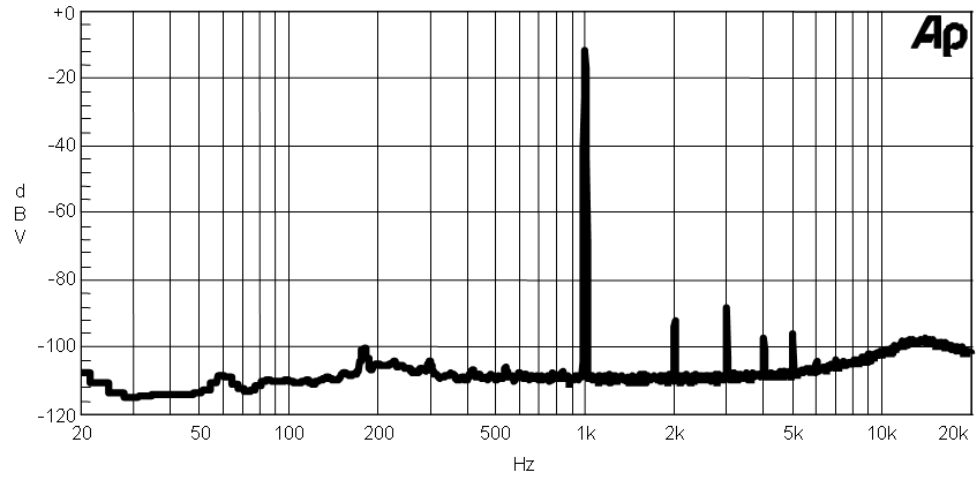

FIGURE 8.3. Output FFT with $V_{dd} = 0.8V$

in thermal noise due to the actual operating temperature of the test chip being more than the simulated temperature is expected.

8.3. Distortion

The output spectrum for supply voltages varying from $0.8V$ to $1.2V$ is shown in Figures 8.3 to 8.7. The maximum gain was selected (49dB setting) and the common-mode voltage was set to half the supply voltage in each case.

With a supply voltage of $0.8V$, the third harmonic dominates with a Spurious Free Dynamic Range (SFDR) of approximately $76dB$ as shown in Fig. 8.3. This odd order distortion is likely the result of mild signal clipping due to the reduced signal headroom.

For supply voltages of $0.9V$ and above, second harmonic distortion dominates for a consistent SFDR of approximately $88dB$ which is better than the

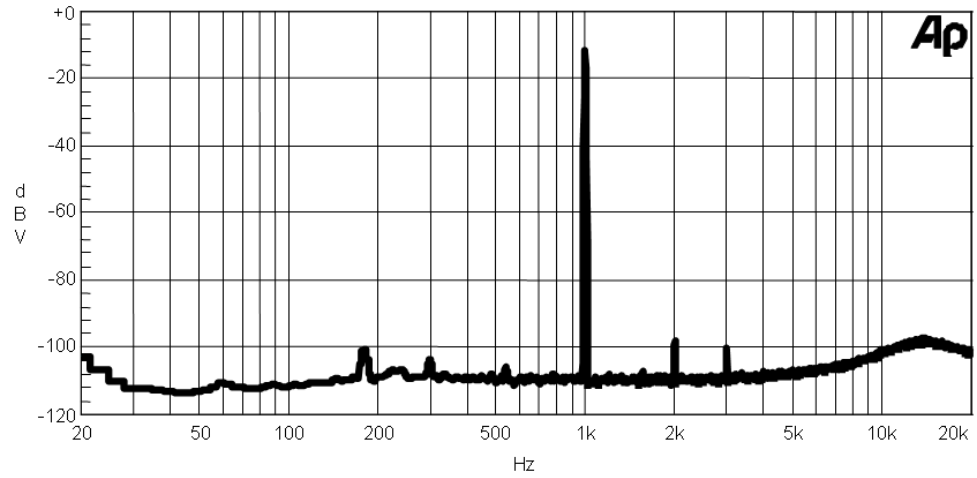

FIGURE 8.4. Output FFT with $V_{dd} = 0.9V$

$80dB$ level required by the specification. This even order distortion implies an asymmetric signal.

8.4. Performance Summary

The test results are summarized in Table 8.1.

TABLE 8.1. Measured Results

Parameter	Target	Measured
Input Referred Noise	$\leq -122dBV$ $10Hz - 20kHz$	$-116dBV$
Input Referred Noise	$\leq -124dBA$ $10Hz - 20kHz$	$-120dBA$
Distortion Level	$-80dB$ at $V_{dd} = 1.2V$	$-88dB$ at $V_{dd} \geq 0.9V$

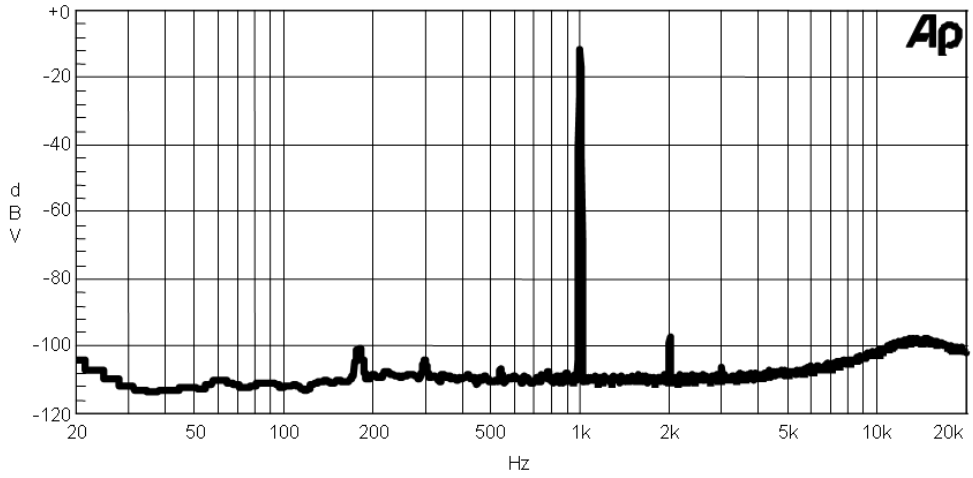

FIGURE 8.5. Output FFT with $V_{dd} = 1.0V$

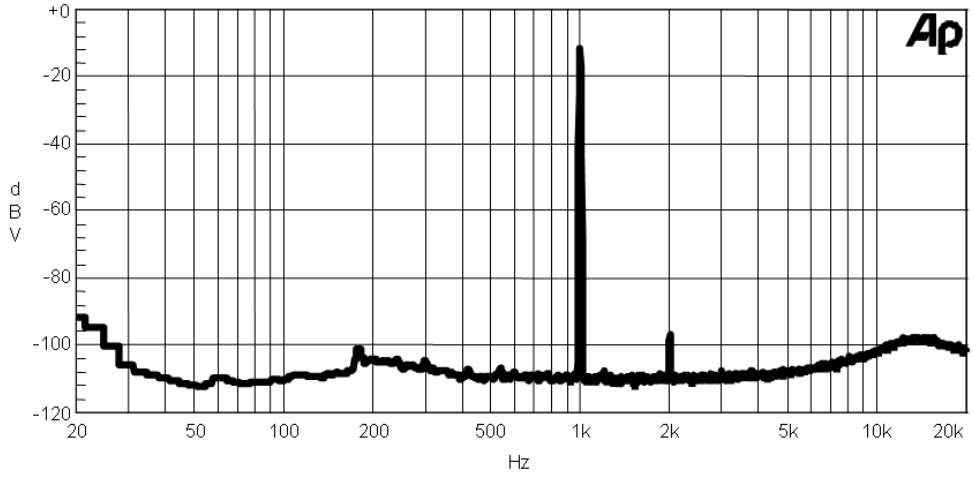

FIGURE 8.6. Output FFT with $V_{dd} = 1.1V$

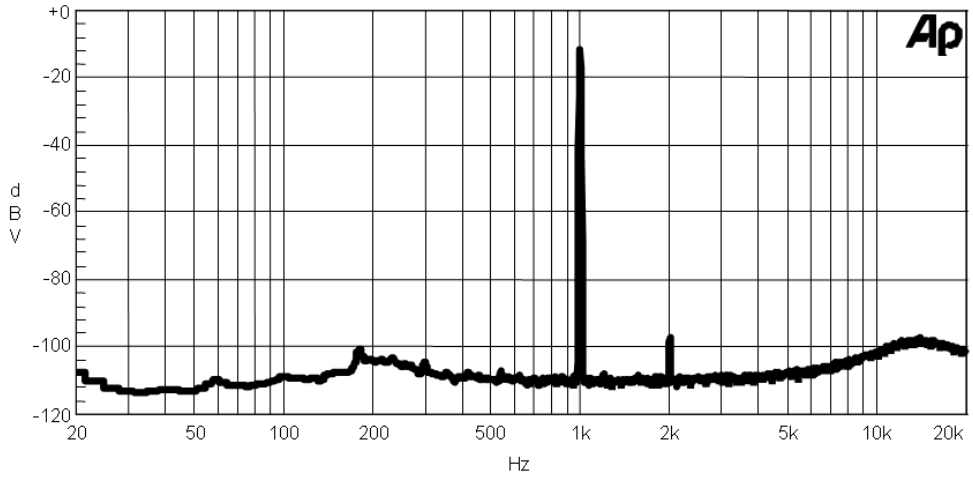

FIGURE 8.7. Output FFT with $V_{dd} = 1.2V$

9. CONCLUSIONS

For digital circuits, a reduction in the power supply voltage and minimum device geometry allows for a significant decrease in power consumption and die area. However, for low-noise analog circuits, a reduction in power supply can translate to a significant increase in power consumption and die area. Analysis and optimization methods are presented that can be used in order to minimize both power consumption and die area for low-noise analog circuits. Although the focus is on the design of a low-voltage microphone preamplifier system, many of the techniques presented may be useful for low-noise analog design in general.

A $0.9V$ microphone preamplifier and programmable gain amplifier system was designed using these techniques and fabricated with a $0.35\mu m$ CMOS process.

In the process of completing a research project, new areas of work will undoubtedly be uncovered. Future work in this area could include further exploration of: nested gain amplifiers, low-noise leveraged current mirror opamps, low-voltage chopping, DC servoing, low-voltage output buffering and finding the optimal point in the amplification system at which conversion to discrete time is made.

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