

AN ABSTRACT OF THE DISSERTATION OF

José Luis Ceballos for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on October 11, 2005.

Title: Enhanced-Accuracy Oversampled Data Converters.

Abstract approved:

Gábor C. Temes

Digital-to-analog converters (DACs) suffer from static and dynamic nonlinearity problems, which degrade their accuracy and performance. Mismatch errors in the analog components restrict the maximum achievable linearity.

This thesis presents various techniques for correcting these errors. It describes a correction process for the nonlinear behavior of DACs, on three different levels: architectural design, circuit design, and layout design.

The main results achieved are listed below:

- Novel topologies using stochastic approaches to linearize multibit converters are presented.
- A new method is introduced for avoiding the use of multibit DACs in the main loop of multi-path DS analog-to-digital converters (ADCs), which, combined with a novel noise leakage compensation technique, allows the use of low quality inner DACs.
- A novel correction algorithm is proposed, which is based on the acquisition of the individual DAC errors by means of correlation procedures. The extracted values are used for correction purposes. The technique is capable of background operation.
- Different circuits are proposed to improve the performance of current-steering DACs. Also, novel layout techniques are shown for reducing the spatial variations of the unit sources. Some of the presented techniques were combined in a prototype chip, designed and fabricated in a 0.35 μm CMOS process. Simulation and preliminary measurement results show that they are effective.

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Enhanced-Accuracy Oversampled Data Converters

by

José Luis Ceballos

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Doctor of Philosophy

Presented October 11, 2005

Commencement June 2006

Doctor of Philosophy dissertation of José Luis Ceballos presented on October 11, 2005.

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

José Luis Ceballos, Author

ACKNOWLEDGMENTS

First of all, I would like to express my immense gratitude to my advisor, Dr. Gábor Temes, who not only provided me with the perfect environment to develop my inquietudes, but also with real friendship, help and support in almost every aspect of my technical and personal matters. I am really proud, and the reader must believe me, that it is a huge honor to me to have worked with him and to consider him as a close friend. Thank you very much “*Super*”...

I am also grateful to my close lab-friends Jose “*Potugues-de-Portugal*” Silva, Pavan “*Kumi*” Hanumolu, and Matt “*Professor M.*” Brown, for giving me so many good moments during these years we have been together. In particular, I have to thank *Josécito* for his help during different stages of our (mine and my wife) life here in Corvallis, especially for being with us not only in the good times, but also during the bad ones...Obrigado. Thanks to *Pavancito* for sharing afternoons of knowledge, coffee and ideas, and Matt, What can I say about Matt and his “*thermometered barbecues*”? Thank you all!

I want to say thanks also to my friends Patrick Birrer and Husni El-Habal for the very good moments we enjoyed, and for our “culinary” meetings. My friends Pat and Ray Schmaltz occupy also a special place in this acknowledgement list. Most sincere thanks to you. Thanks to Charlie and Meredith Myers for sharing with us their delightful friendship. I'm also grateful to my dear friend Manfred Dietrich, for always helping me with his good humor, especially during “*gray days*”.

For their important contributions to this research, I wish to thank Dr. Xuesheng Wang, and Dr. Jesper Steensgaard.

I also want to acknowledge all my lab and class mates, with whom I have shared and enjoyed these years of hard work: in no particular order, I would like to acknowledge Gilcho “*Jilchito*” Ahn, Ting Wu, Peter Kurahashi, Mingyu Kim, Merrick Brownlee, Qingdong Meng, Volodymyr “*Vova*” Kratyuk, Melinda Valencia, Kerem Ok, Anurag Pulincherry, Jipeng Li, Dong-Young Chang, Kye-Hyung “*Mr.*” Lee, Dr. Yunjae Kook, Ranganathan “*Ranga*” Desikachari, Kiseok “*Kisokito*” Yoo, Yoshio “*Nishida-San*” Nishida, and Zhneyong “*Gordon*” Zhang.

I am also grateful to Ibi Temes for her kindness, and for many especially nice visits to the Temes' house. I felt like being at home...

This work was mainly possible thanks to the generosity of the Center for the Design of Analog and Digital Integrated Circuits (CDADIC), and Analog Devices Inc. (ADI). Special thanks to Paul Ferguson and Dennis Dempsey for their help during the design reviews and for their valuable feedback on many circuit design issues.

I would also like to thank Prof. Luca Lucchese, Prof. Mario Magaña, Prof. Un-Ku Moon, and Prof. Ron Guenther for serving in my graduate committee. Special thanks to Mario, for his honest friendship.

I wish to thank the EECS staff for their highly qualified support and help: Sarah O'Leary, Ferne Simendinger, Morgan Garrison, Clara Knutson, Brian Lindsey, Nancy Brown, Andy Lyons, and Tina Batten.

Of course and for sure I have forgotten someone (it is not unusual on my), but even though I can have a mediocre memory for names, fortunately I have a good long-term memory for friends... Sooner or later I will see many of you, and we will have fun again.

Last but not least, I am deeply grateful to all my family (*here and there, now and then...*) for believing on me when I did not, specially my wife, Marcela, for her unconditional love, for taking care of me, and for her constant help (and also for supporting my bad mood...). Mis más especiales y sinceras gracias son para vos, *Capuchin!*

José Luis Ceballos
Corvallis, Oregon, Oct. 2005

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To my wife, Marcela.

ENHANCED-ACCURACY OVERSAMPLED DATA CONVERTERS

CHAPTER 1. INTRODUCTION

1.1 Motivation

Multibit delta-sigma (D-S) digital-to-analog converters (DACs) are widely used in audio, wireless and wireline communication systems. They contain a digital interpolation filter, a noise-shaping loop which reduces the word length of the digital signal, a low-resolution internal DAC, and an analog smoothing filter. Such converters are capable of very high accuracy and linearity, up to 20 bits or even higher.

A major limitation of such converters is the achievable static linearity of the embedded DAC. For D-S DACs with narrow-band signals, the effective DAC linearity can be vastly improved by using a high oversampling ratio (OSR) combined with a dynamic element matching (DEM) method [25-27, 29]. However, for DACs processing wideband signals, such as those occurring in communication applications, the OSR is restricted to low values by the limited speed capability of the analog circuitry used. In this situation, DEM does not provide enough accuracy improvement for a high (say, 15 or more ENOB) linearity for the overall converter.

There are different techniques to overcome such limitations in order to obtain high resolution/accuracy converters, even in the unavoidable presence of imperfect -and maybe low quality- analog components. Two possible paths to follow are:

- 1) Novel multibit techniques based on the use of 1-bit DAC converters (inherently linear devices).
- 2) Correct digitally –mainly for robustness reasons- the inaccurate multibit DACs.

This thesis deals with both research directions; a possible architecture for the second set of ideas was implemented in silicon, proving its potential as a linearization technique. The other ideas are presented at the simulation level, including realistic nonideal models.

1.2 Contributions

As mentioned, different paths have been followed, at the theoretical and at the practical levels. The work that emerged from this investigation was proposed and published, being shortly summarized as follows:

- 1) Requantization in multibit delta-sigma ADCs: In this research, a novel topology was introduced [2-3], having shown the potential of protection against DAC mismatches.
- 2) Stochastic data converters: Firstly presented in [3], the concept was extended in [6]. This research focuses in the redundant use (spatial and temporal averaging) of low complexity components to obtain multibit highly linear DACs and ADCs.
- 3) Digital correction of DACs: Research published in [1] and [4]. This technique is based on the adaptive correction of the DAC, after the estimation of the DAC unit element errors has been obtained by means of correlation processes. It was implemented in silicon, following a modified error extraction procedure, here also proposed and described in detail.
- 4) Novel layout techniques, current cell topologies, and drivers for current-steering DACs [5]

The research also presented modifications to previously presented analysis of matching in the area of current mode DACs.

The topologies proposed have extra potential when used in harsh environments (e.g., space and radioactive applications).

The contributions of this work can be mainly divided into two categories:

- 1) Combination of several of the previous techniques to implement a digitally corrected DAC, with low sensitivity to unavoidable analog components imperfections.
- 2) Proposal of new solutions and directions in the field, as the stochastic approach.

1.3 Thesis Organization

Following this introduction, Chapter 2 provides some insight into the DAC nonlinear problems, and defines some metrics used in the characterization of such converters.

Chapter 3 presents different proposed solutions, from the algorithmic, the geometric and from the circuitual point of views. Several subsections will introduce the new ideas in each one of the previous items.

Chapter 4 deals with the analysis of the digitally corrected DAC, proposing also a new switching technique for the unit element errors estimation. Nonideal component effects together with extra topologies will also be addressed here.

Chapter 5 shows different aspects of the analog and the digital implementation in detail.

Chapter 6 describes the test setup and the laboratory experimental results of the fabricated prototype.

Finally, Chapter 7 concludes this thesis, summarizes the contributions of this work, and describes directions for future research paths to follow.

CHAPTER 2. DIGITAL-TO-ANALOG CONVERTERS AND THEIR LIMITATIONS

Digital-to-analog converters are signal processing blocks that convert digital representations (time-discrete and amplitude-quantized) into analog quantities (time and amplitude continuous signals). To do so, different types of converters have been designed and used during many years [8], using different devices and schemes depending on the specific applications. This thesis deals with current-steering DACs, a topology that was selected as a test vehicle for a novel correction algorithm, even though the concepts that will be here presented can also be applied to other classes of converters.

2.1 Current-steering DACs

A fully differential current-steering DAC is schematically depicted in Fig. 2.1. In it, each current source can be switched either to one or to the other resistive load, in accordance with the incoming digital control bits. The differential voltage output is measured across the load resistors. A single-ended version can be easily visualized from the scheme, using only one output branch. This topology has the advantages of a high speed of operation and a relative simplicity of construction.

Depending on the weights of the current sources, the converter can be:

- 1) Binary coded: currents scaled in ascending powers of two.
- 2) Thermometer: each current source will have the same weight, making the output dependent on how many unit elements are connected (linear relationship).
- 3) Segmented: Combination of the two previous approaches. One of the unit elements of the thermometer decoded MSBs (most significant bits) array will be the parent current source of a binary weighted converter that will provide the LSBs (least significant bits).

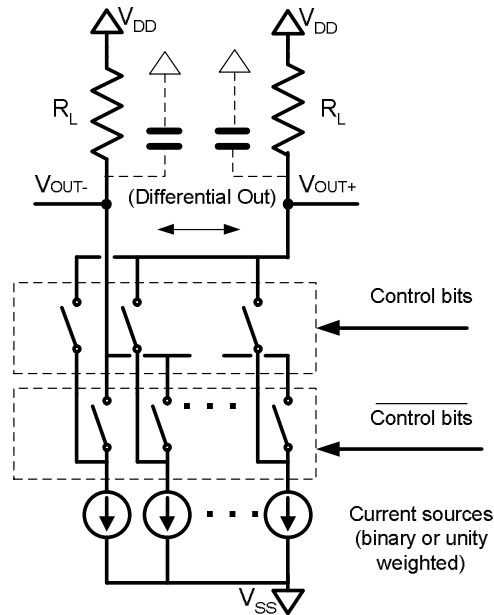


Figure 2.1: Schematic of a current-steering DAC

Each configuration presents advantages and disadvantages regarding linearity issues and complexity [11].

In this thesis the thermometer and the binary topologies will be implemented at the circuit level. Having all the currents the same value, the thermometer encoded converter will be useful at the time of the individual error detection and estimation; the correction of these errors will be performed using a binary weighted auxiliary current-steering DAC for simplicity of design.

A simplified schematic of a possible unit current source is depicted in Fig. 2.2. The main current source can have a cascode device to increase its output resistance, reducing the associated nonlinear effects [22]. The switches can work as saturated devices, being only intended to convey the current to one of the loads; this condition also increases the output resistance. The control signals can have a different power supply to reduce dynamic effects. More about the fine points of the converter and the cell will be presented throughout the following chapters of this work.

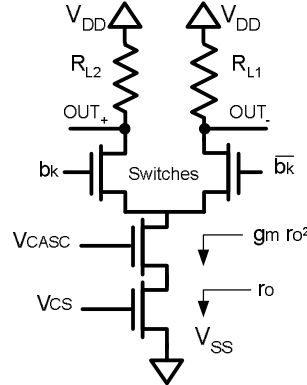


Figure 2.2: Schematic of the current source for current-steering DACs. The cascode device increases the output resistance. The switches are controlled by complementary signals with dedicated crossover point.

2.2 Oversampled and Nyquist Converters.

An important categorization is based on the tradeoff between speed and accuracy. Considering that, two main classes of converters can be devised:

- 1) Nyquist rate converters: Operating at the maximum frequency (half of the clock frequency, or Nyquist frequency)
- 2) Oversampled converters: Reduced bandwidth together with moving the quantization noise towards high frequencies enhances the final achieved accuracy.

The generalized ideas are depicted schematically in Fig. 2.3. In the Nyquist multibit DAC, all N input bits are processed. It is the fastest one. In the delta-sigma modulating system, a truncation takes place from the N bits at the input to M bits at the output; hence, the number of processed bits is less, but at a higher speed. Because the truncation is inside the feedback loop and is preceded by the low pass loop filter, the net effect is moving the noise power to the high-frequency part of the spectrum. In the band of interests (at low frequency generally), the quantization noise will be greatly reduced. The tradeoff between the two converters is clear: *speed vs. accuracy*. Figure 2.4 schematically depicts the power spectrum density of the quantization (truncation) noise for both cases.

As mentioned, the number of bits processed in the delta-sigma case is less than in the Nyquist one; this can be translated as reduced complexity. Moreover, if the DAC is reduced to its minimum expression (1-bit), no nonlinear DAC errors or inaccuracies will exist (unfortunately other effects will appear, such as stability issues, idle tones, etc. [9-10]). For those reasons, a 3-bits delta-sigma structure has been selected as the test vehicle in the digitally corrected DAC prototype.

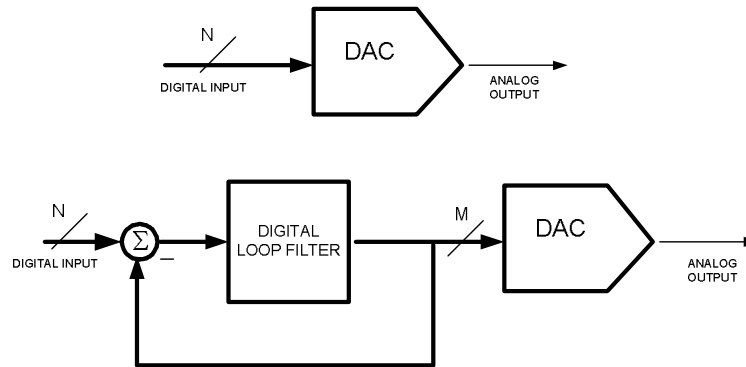


Figure 2.3: Nyquist and Oversampled delta-sigma (D-S) DAC systems.

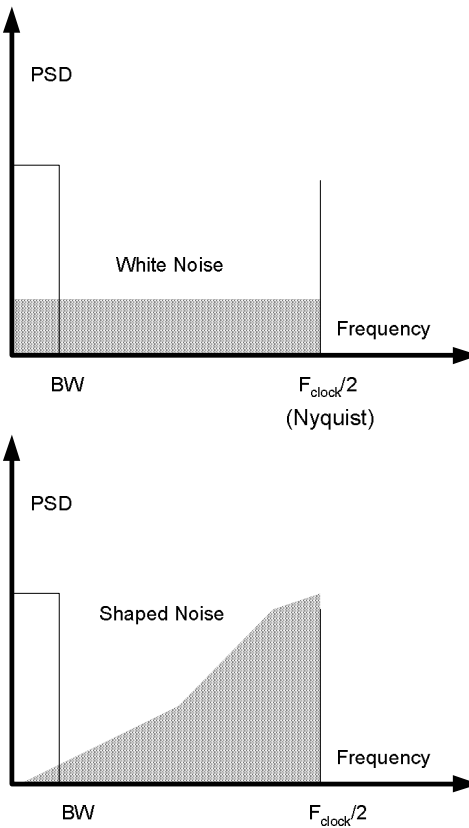


Figure 2.4: Power spectrum densities of the quantization noise for the Nyquist rate and for the D-S converters.

2.3 DAC Metrics and Known Solutions for Linearization of Multibit DACs

The most commonly used parameters/errors that characterize DACs are [8]:

- 1) *Offset*: Shift of the output characteristic.
- 2) *Gain error*: The slope is different than predicted.
- 3) *INL (Integral non linear error)*: The overall variation from the ideal linear characteristic.
- 4) *DNL (Differential non linear error)*: The difference in each step from its ideal (1 LSB) value.
- 5) *Settling time*: Time required to settle in the 0.5 LSB band (the sampling rate can be roughly calculated as $1/\text{settling time}$).
- 6) *Aperture Jitter error*: The error that appears due to sampling-time uncertainty.

A DAC is called monotonic if its analog output always grows with continuously increasing digital input codes. A converter is guaranteed to be monotonic if $DNL < 1 \text{ LSB}$ and $INL < 0.5 \text{ LSB}$. In the following chapters, an analysis that relates the INL error and the production yield will be presented, a modification of the work presented in [14].

There exist different techniques to linearize the DAC characteristics, being the most important:

- 1) Correlation and calibration (digital domain) [31].
- 2) Data Weighted Averaging [28-29].
- 3) Analog calibration [24].

Extra references: [17-20].

This dissertation will present different solutions to the linearization problem.

CHAPTER 3. PROPOSED NEW SOLUTIONS

3.1 Algorithms and Architectures

In this section different architectures will be presented, addressing the main problem of DACs nonlinear behavior in Nyquist and in oversampled converters. First of all, the concept of requantization in delta-sigma ADCs will be introduced, where the use of a 1-bit DAC combined with an internal multibit ADC allows high linearity and, at the same time, increases the converter's stability. Next, a novel design topology will introduce the so-called stochastic data converters. This architecture is mainly based on the fact that many similar and imprecise unit elements can be combined to perform a collective improved function. Finally, the digital correction of unit errors in nonlinear DACs will be introduced. It is based on the estimation of the individual elements errors, correcting their effect using a mixed-mode compensation circuitry. This last design procedure was studied in detail, and a silicon IC implemented; the next chapters will deal in detail with the fine points of this topology.

3.1.1 Requantization in Delta-Sigma ADCs

The first question to be asked is: What is requantization? The answer is: it is the use of another delta-sigma loop (this time digital, and embedded into the main loop), trying to convert the multibit digital output of the main delta-sigma ADC into a 1-bit representation. The next question should be: Why do so? Again, the answer is relatively easy to be understood. As it was pointed out previously, a 1-bit (2 levels) DAC is an inherently linear system; if the weights of the two levels differ, the net nonideal effects are offset and gain variation, none of them being of concern in delta-sigma systems.

The new problem is that, in order to convert the output from a multibit representation into a 1-bit one, some truncation (T) must be introduced somewhere; it is not important which kind of error is produced (i.e. shaped or unshaped noise), the important point is where it is introduced. Unfortunately, any error associated with the feedback DACs in delta-sigma ADCs will appear at the output indistinguishable from the real modulator's input. Is there any known solution? The answer again is yes. Previously reported work [34-35] has shown that the truncation error can be compensated in the digital domain, if a modified copy of that error is combined with the output of the feedback loop trying to get a first order cancellation of the introduced error in a new (final) output. A generalized structure of this kind of systems is depicted schematically in Fig. 3.1.

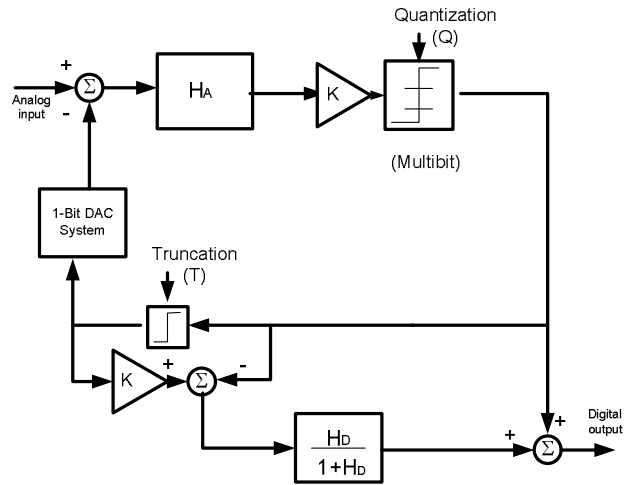


Figure 3.1: Schematic of a feedforward truncation cancellation.

For a conventional first order system, the internal filters are given by:

$$H_A = \frac{1}{(z-1)} \equiv H_D \quad (3.1)$$

$$\frac{H_D}{1+H_D} = \frac{1}{z} \quad (3.2)$$

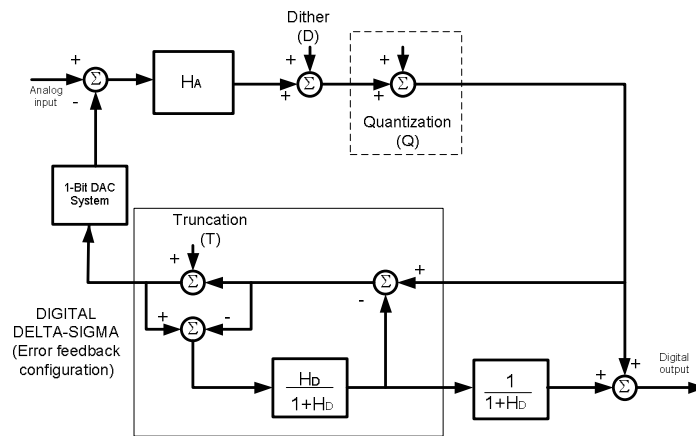
The constant K symbolizes the gain variation in the analog filter. It should be pointed out that, because of the 1-bit DAC, the characteristic equation of the loop is always given by $1+H_A$, independently of the gain K .

After simple mathematical manipulations, using $K=1$ for the sake of simplicity without loss of generality, it can be easily shown that the output of the linearized system is given by:

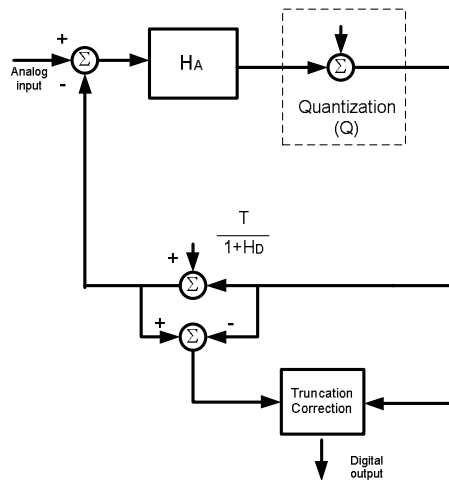
$$OUT = IN \frac{H_A}{1+H_A} + Q \frac{1}{1+H_A} - T \frac{H_A}{1+H_A} + T \frac{H_D}{1+H_D} \quad (3.3)$$

3.1.2 Proposed System

The main issue with the previous architecture lies in the fact that the transfer function seen by the truncation toward the output in both worlds –analog and digital- is not the same, causing part of the truncation noise to appear at the output, an effect known as noise leakage [11]. Again, is there any solution to this problem? Yes. The solution herein proposed can be visualized if one asks the following question: Is there any way in which the difference between the analog and digital transfer functions reflects the truncation noise leakage at the output but in a noise-shaped way? The system that performs such a function is schematically represented in Fig. 3.2., together with its linearized model.



(a)



(b)

Figure 3.2: a) Requantization delta-sigma ADC; b) Linear model

At this point requantization is introduced. Now, what is appearing at the output of the DAC is a high-pass filtered (shaped) truncation error. Using a feedforward approach similar to that used before for cancellation, the noise leakage will be shaped with a first order noise transfer function (NTF) in the final output, hence minimizing the analog NTF noidealities. Under the previous assumptions, the general linear input-output relationship can be shown to be:

$$OUT = IN \frac{H_A}{(1 + H_A)} + \frac{Q}{(1 + H_A)} + \frac{T}{(1 + H_D)} \left(\frac{H_D}{1 + H_D} - \frac{H_A}{1 + H_A} \right) \quad (3.4)$$

This in the ideal case reduces to:

$$OUT = IN \left(\frac{1}{z} \right) + Q \left(\frac{z-1}{z} \right) \quad (3.5)$$

From equation (3.4), the previous comments about shaping for the truncation noise (T) can be easily inferred.

It must be noted that the truncation error (T) appears at the output of the 1-bit DAC (the summing node of the main feedback loop) multiplied by a second order function, and following the 1-bit ADC *Lee's* criterion [10] this point of the circuit is the problematic one. The dithering noise (D) is used to uniformly distribute the use of the quantizer levels and to diminish idle tones. It can be previously shaped in order to move its power spectral density toward out-of-band frequencies.

3.1.3 Extending the Concept

It is clear that the use of multibit quantizers improves the performance of the modulator. Considering now this block, another interesting question can emerge: Can something be done in order to improve even more the performance of the system? Yes. The quantizer can be replaced by a more elaborated block that performs the quantization, but in such a way that it has the following signal transfer function (STF) and NTF:

$$\begin{aligned} STF &= 1 \\ NTF &= \left(\frac{z-1}{z} \right)^n \quad \text{with } n \geq 0 \end{aligned} \quad (3.6)$$

The previous equations can be “translated” colloquially as: the new quantizer must provide noise shaping and delay-free signal transference. A possible solution to this comes from the so-called low-distortion topology [30], schematically depicted in Fig. 3.3.

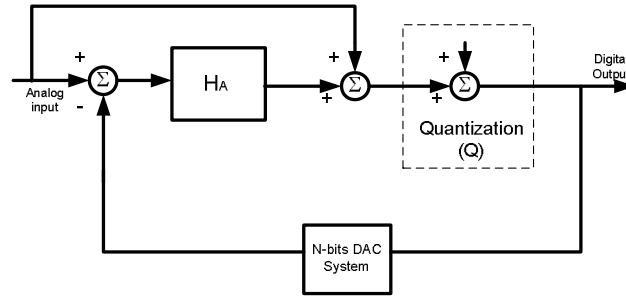


Figure 3.3: Low-distortion topology.

Under the previous assumptions, now the quantization noise can be shaped by a higher order loop. Hence the new delta-sigma can be viewed as a feedback loop that can be *added* to any stable n-th order conventional delta-sigma loop, with a delay-free NTF, as depicted in Fig. 3.4.

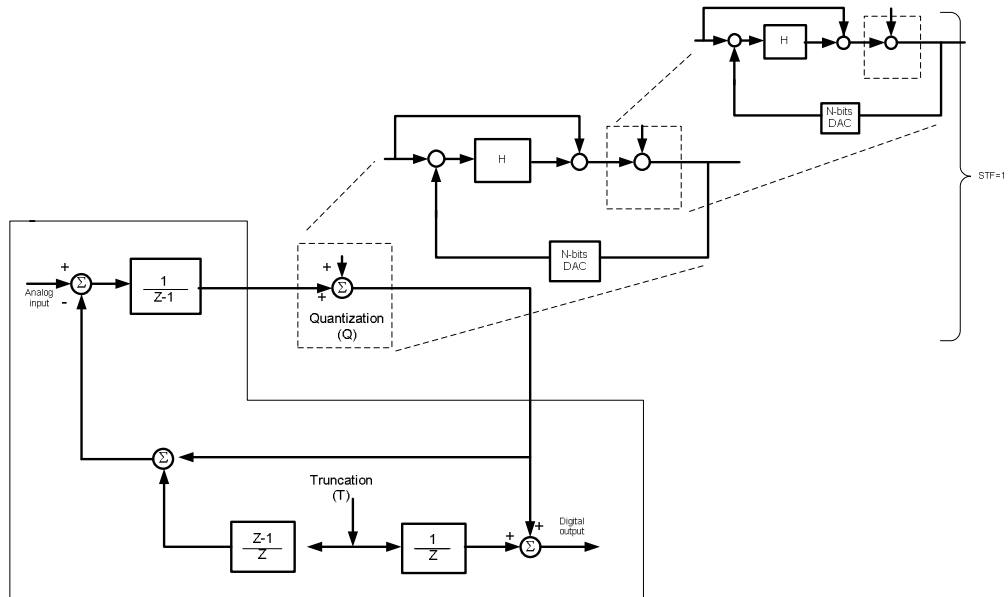


Figure 3.4: The embedded system

The system becomes an *n*th-loop modulator [41] with requantization. Moreover, because the *added* delta-sigma is in the forward path, the nonlinearities introduced by the inner DACs will

be reduced by the outer-loop gain (the requirements for the ADC and the DAC used in the inner-loop delta-sigma can be considerably reduced).

3.1.4 Remarks

Simulation results for a second-order 5-bit ADC with only a 8-bit linear internal DAC are shown in Fig. 3.5, where nonideal effects were taken into account.

This new topology was published in [3], and its study was then discontinued. A recent publication [36] has shown the silicon implementation of a very similar – but better- approach for the requantization cancellation procedure. The concept of nested delta-sigma converters (delay free unit STF modulators) which emerged from this research was also presented in [3].

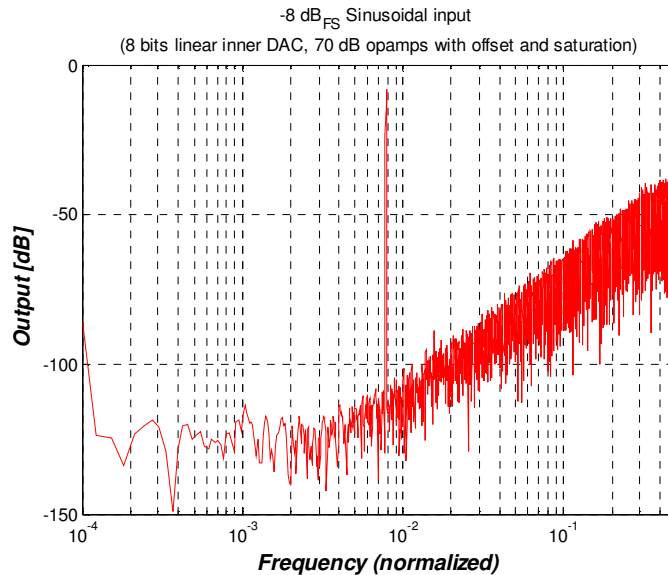


Figure 3.5 Typical 32768 point FFT. Proposed architecture having 2nd order noise shaping and a 5-bit quantizer ADC. Saturation and gain blocks included. Opamp characteristics: DC-gain=70dB, offset=1mV. Inner DAC is 8-bits linear. Also considered is 1% error in integrator's gain.

3.2 Stochastic Data Converters

In biological systems, often a large number of low-complexity unit cells combine to perform a fairly exact function. Applying this idea to the circuits and systems domain, in this subsection it is proposed to use a set of coarse quantizers (i.e., 2- or 3-level comparators) combined

to obtain robust and highly linear multibit analog-to-digital (ADC) [2, 6], and digital-to-analog (DAC) converters [6].

The original question of linearity can be reformulated as follows: Is there any combination of unit elements (coarse elements) which can provide a multiunit (fine) linear response? The answer is yes. It was already mentioned that a 1-bit DAC is inherently linear; consequently the addition (linear operation) of many 1-bit DACs will also provide a linear output. To get a coherent result, it is common sense to ask for the same input in each one of those unit elements. But, having this request is easy to visualize that no extra information or improvement will be obtained unless some extra measures are taken (same input acting over similar signal processing blocks; in that case the obtained result is similar to having the multiplication of only one of the individual outputs by the number of combined unit elements). The proposed solution is to use a statistical approach. The general idea will be first presented, applied to delta-sigma ADCs, and then the application to the DACs will be shown.

3.2.1 Stochastic Quantizers (SQ)

Figure 3.6 shows the generalized stochastic quantizer. It has M branches, each one containing a one-bit quantizer, an independent identically distributed (i.i.d.) random noise source (d_i) added to the sampled and held input signal, $x(t)$. Each digital output is followed by a digital integrator (up/down counter) controlled with a common modulo N counter. Those blocks will perform an accumulate-and-dump process (temporal averaging), while the parallel combination will provide a spatial averaging. Assuming the power of one individual quantizer to be q^2 , after averaging M times spatially and N times temporally, the equivalent quantizer noise power at the output, q_{av}^2 , will be:

$$q_{av}^2 \cong \frac{q^2}{N M} \quad (3.7)$$

Considering a linearized model, the output signal power will be equal to the input signal power, which means an increase in the signal to noise ratio (SNR) equal to $N.M$, or in other words, a reduction of the quantization noise power by the same factor. The noise will decrease as the number of quantizer branches or the modulo of the counter increases, as depicted in Fig. 3.6-b). The tradeoffs depend on speed and power/area relations. It should be noted that for a given complexity, the maximum reduction of quantization noise is achieved when $N = M$.

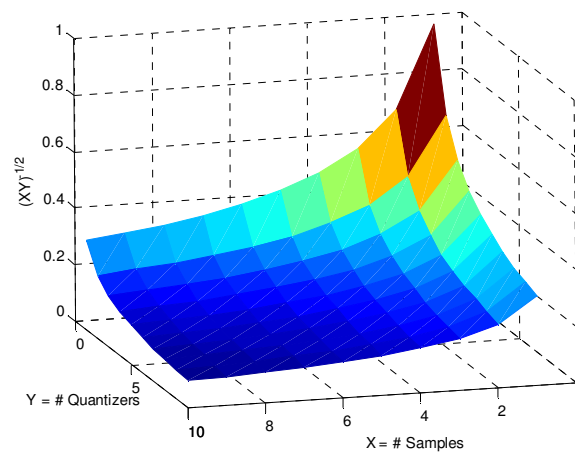
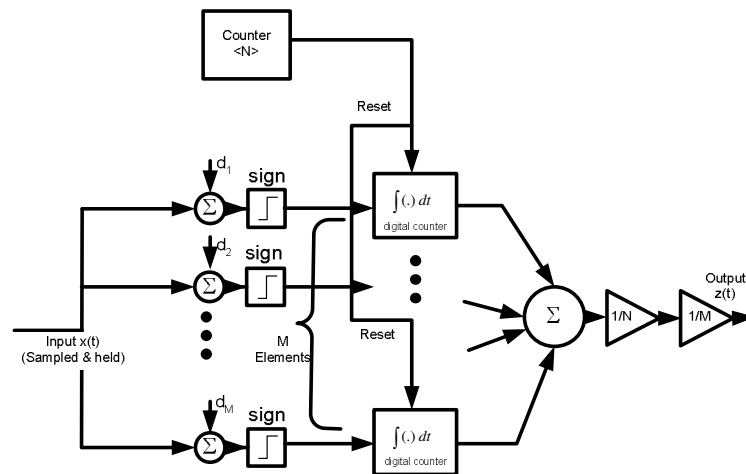


Figure 3.6: a) Time-Spatial averaging quantizer. The noise sources are uncorrelated and i.i.d. The integrators are up/down counters. Scaling factors are at the output. b) Normalized RMS noise as a function of the number of samples and the number of parallel branches.

Oversampling is a well known technique to reduce in-band noise power, hence only spatial averaging ($N=1$) will be considered here (i.e., the counters will be disregarded in the mathematical development that follows). First, the application will be presented for an open loop configuration, but after that the emphasis will be put on delta-sigma modulators.

Based on the scheme of Fig. 3.6, and assuming no time averaging ($N=1$), the overall system becomes a parallel combination of M one-bit quantizer branches. It should be pointed out that the simple $sign(x)$ quantizer could be replaced with a 3-level (1.5 bit) quantizer, obtaining

improved performance. Also, different *pdfs* (probability density functions) can be used to generate the random dithering and uncorrelating noise sources. The general case will be discussed next.

Assuming a linear operation over a continuous random variable (r.v.) d , with pdf $f_d(d)$:

$$y = x + a d \quad (3.8)$$

where a and x are constants¹, then the pdf of the new r.v. y is given by [37]

$$f_y(y) = \frac{1}{|a|} f_d\left(\frac{y-x}{a}\right) \quad (3.9)$$

Without loss of generality, considering $a=1$, it is known that $f_y(y)$ will be the convolution of $f_d(d)$ with a Dirac's delta centered at x , i.e, the new pdf will be equal to the original one but shifted.

On the other hand, the overall system output is given by

$$z = \frac{1}{M} \sum_{i=0}^{M-1} \text{sign}(x + d_i) = \frac{1}{M} \sum_{i=0}^{M-1} \text{sign}(y_i) \quad (3.10)$$

For large values of M , and using the law of large numbers, z tends to:

$$\overline{z} \cong \overline{\text{sign}(x + d_i)} = \overline{\text{sign}(y_i)} = \overline{w}; \quad w = \text{sign}(y_i) \quad (3.11)$$

The mean value, or first moment, of a r.v. is defined as

$$\overline{w} \equiv \int_{-\infty}^{\infty} w f_w(w) dw \quad (3.12)$$

Using the $\text{sign}(arg)$ definition (+1 if $arg \geq 0$, -1 otherwise), combined with the previous formulas,

¹ Here, x is the sampled input value.

$$\begin{aligned}
\bar{w} &\equiv - \int_{-\infty}^0 f_y(y) dw + \int_0^{\infty} f_y(y) dw = \\
&- \int_{-\infty}^0 f_d(y-x) dy + \int_0^{\infty} f_d(y-x) dy = \\
&- \int_{-\infty}^{-x} f_d(\alpha) d\alpha + \int_{-x}^{\infty} f_d(\alpha) d\alpha
\end{aligned} \tag{3.13}$$

results.

From (3.13), it can be easily inferred that for a uniform distribution, the output is linearly related to the input. For other kind of distributions, look-up tables may be used to optimize the use of the quantizers.

3.2.2 *Sigma Delta Modulators Using the Spatial Quantizer*

The first design to be presented is a delta sigma ADC, schematically depicted in Fig. 3.7. In this case, to avoid excessive delays, the fast feedback toward the input addition point is made individually from each comparator. The addition in the digital domain is performed out of the loop, where delays can be tolerated. A second order system using 16 3-level comparators was simulated using ideal and nonideal components. Total correspondence with a 3-bit system was obtained. The main drawback lied in the DAC: having mismatch in the components, the main effect of the architecture is the randomization of the elements usage, reducing the harmonic content at the expense of an increased noise floor. It should be noted that the shape of the *pdf* in this case has no importance (the high loop gain tends to linearize the nonlinear quantizer characteristic). Moreover, offsets are tolerated. If the matching of the unit elements is good, this zero-order mismatch shaping (simple randomization) could provide an acceptable system.

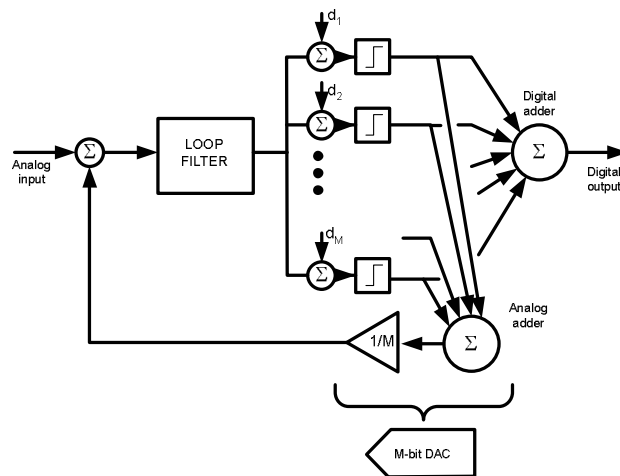


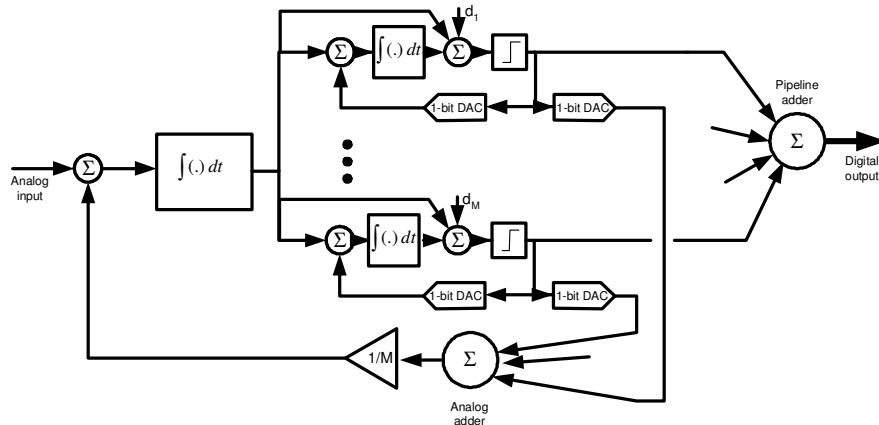
Figure 3.7: Stochastic Quantizer embedded in a delta-sigma ADC loop.

For this example, the improvement in the signal-to-noise ratio (SNR) is evident using (3.7). The output of the system for any bandlimited input is then given by:

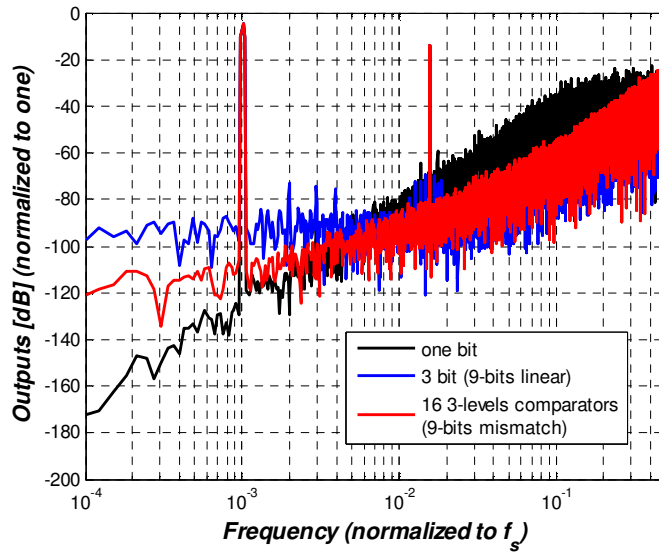
$$OUT = STF IN + NTF \left(\frac{Q}{\sqrt{M}} \right) \quad (3.14)$$

Here STF and NTF stand for the signal- and for the noise-transfer functions, respectively, and q is the quantization noise of a 3-level quantizer [9, 10].

A first modification could be to use, instead of a simple 3-level quantizer, a first order delta sigma modulator for each branch. Figure 3.8-a) shows the system together with its simulation results. Nonideal effects were taken into account: The system was simulated using realistic models for the opamps (offsets in the order of +/-5mV, DC gains of 70~80dB, plus nonlinear characteristics were implemented in Simulink[®]), 9-bit matching for all the components, etc. It is noteworthy in this case that because each element has a 1-bit first order shaping, the overall response is highly linear (compare with the intermodulation tones in the 3-bit delta sigma modulator, with a 9-bit linear feedback DAC). For comparison purposes, the response of a 1-bit ADC is also shown. As a conclusion, an improvement in linearity is obtained without the use of data weighted averaging (DWA) or any other mismatch shaping technique in the DAC.



(a)



(b)

Figure 3.8: Delta sigma ADC using spatial averaging with embedded noise shaping. a) Simplified schematic. Two sets of 1-bit DACs are used to simulate a real system. b) Frequency response for a second order system using a 3-bit conventional quantizer, using 16 1.5-bit spatial quantizers, and using a 1-bit quantizer delta sigma. Two tones ($-4.5\text{dB}_{\text{FS}}$ and -14dB_{FS}) used to observe nonlinear behavior. All elements are 9 bits linear.

As a corollary, because of the linearity obtained, it is now possible to extend the concepts to a delta sigma DAC structure, as depicted in Fig. 3.9-a. The first step is to simplify the digital structures; hence, a first delta sigma loop ($\Delta\Sigma_A$) is used to reduce the digital input word length. The dithering sources can be quantized and easily generated on-chip by means of pseudo random noise generators implemented with linear feedback shift registers (LFSR). The simulated response is shown in Fig. 3.9-b, together with a 3-bit and a 1-bit systems for comparison purposes. Also, the integrated noise powers are plotted for the three different cases.

Important points: error feedback can be used, resulting in reduced area and power consumption; no stability problems present as long as each equal individual one-bit branch is stable (possibilities of high order noise shaping); current sources can be used (obtaining consequently high speed developments).

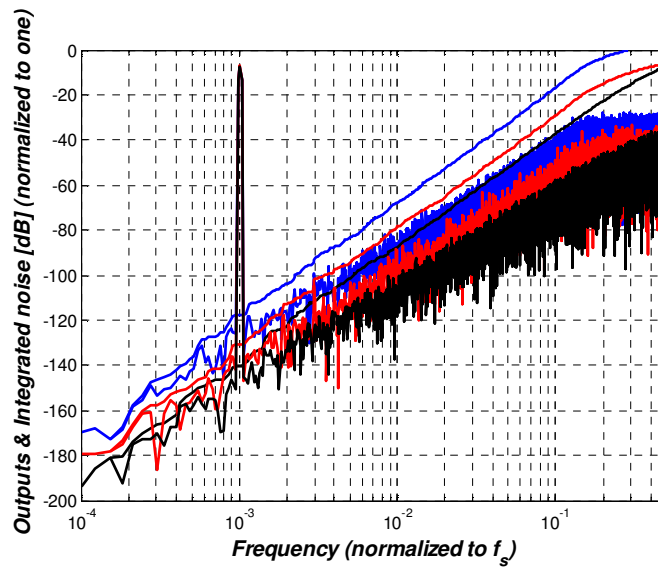
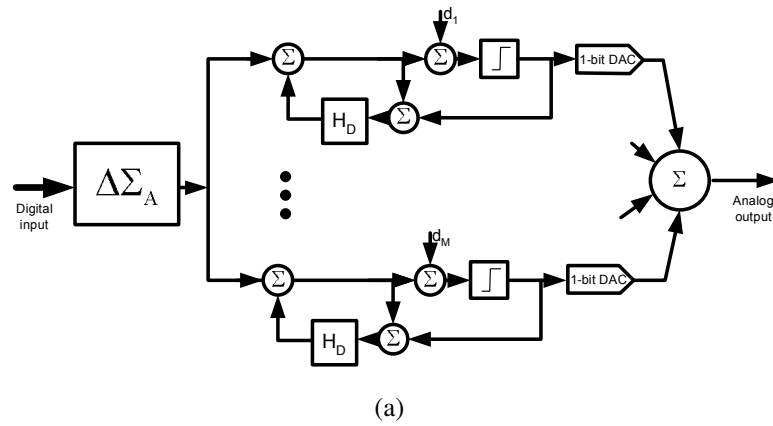


Figure 3.9: Delta sigma DAC using spatial averaging with embedded noise shaping. a) Simplified schematic. Analog elements have 9 bits matching. Noise sources quantized to 3 levels. b) Frequency response for a second-order system using a 3-bit conventional quantizer, using 16 1.5-bit spatial quantizers, and using a one-bit quantizer delta sigma. Tone at -7dB_{FS} . Also shown are the integrated noise powers for the three cases.

3.2.3 Remarks

The idea behind this procedure can be explained as follows: under certain assumptions the quantization noise can be considered as a wide sense stationary stochastic process (generally considered uniformly distributed and with zero mean), with ergodicity in its mean and variance values (i.e., similar time and spatial statistical properties). Based on this fact, assuming zero correlation among all the individual outputs and successive samples, and using the law of the large numbers, we have concluded the previous results for a large number of comparators with large dithering sources.

Both time and space constrains were taken into account, e.g., for the spatial ADC case, a $\log_2(M)$ bits length word is obtained as the output of the system, but with an equivalent quantization error of $\log_2(M^{1/2})$. The tradeoff is clear: *accuracy vs. time and/or area & power*.

On the other hand, an interesting and promising fact emerged from this research: highly linear devices can be devised using imperfect components.

As it was already mentioned, all the 1-bit inputs/outputs must be uncorrelated among themselves. The use of M noise sources at the inputs of the M comparators not only achieves this result, but also dithers the quantization noises, helping the loop filters to shape their power spectral densities (PSD). Generating the noise in the digital domain is an easy matter, something that is not so trivial in the analog domain.

As a final result, circuit robustness is obtained, which comes from the fact that there is no need of accurate voltage dividers to get the quantizer reference chain. Another extra advantage is that if one comparator (or a reduced amount of them) fails, the system will still be functional, with a little degradation on its characteristics

3.3 Digital Correction of DACs – Main Idea

In this section, an alternative approach is described for achieving enhanced DAC accuracy. It uses an adaptive digital correction of the internal DAC. The process is based on acquiring and refining digital estimates for the errors of all unit elements (capacitors or current sources) which form the internal DAC, and then applying the appropriate corrections to the output signal according to the known usage of these elements. Numerical simulations and practical results verified that even for large initial errors a very high conversion accuracy can be achieved using the proposed algorithm (to be discussed in Chapter 4).

3.3.1 The Correction of the DAC

As pointed before, an oversampled DAC system can be decomposed into different sub-blocks, as those depicted in Fig. 3.10: The interpolation filter will increase the sampling rate and at the same time will provide replica reduction (increasing the effective number of bits, or ENOB); the delta-sigma modulator will reduce the number of processed bits, keeping the high accuracy. The part that will be described in this subsection is the one composed by the Main-DAC and its associated correction loop. The front end of the whole system is generally a smoothing filter, to suppress out of band corruptive noise and replica power.

The idea of the correction loop is depicted schematically in Fig. 3.11. The main components of the system are the Main DAC (composed of $2^n = N$ unit elements), an Auxiliary (reduced scale) DAC, 2 banks of registers (B_{ANK1} to store the individual errors and B_{ANK2} to store the complete errors for the different codes), a Scrambler to randomize the use of the unit elements and associated logic.

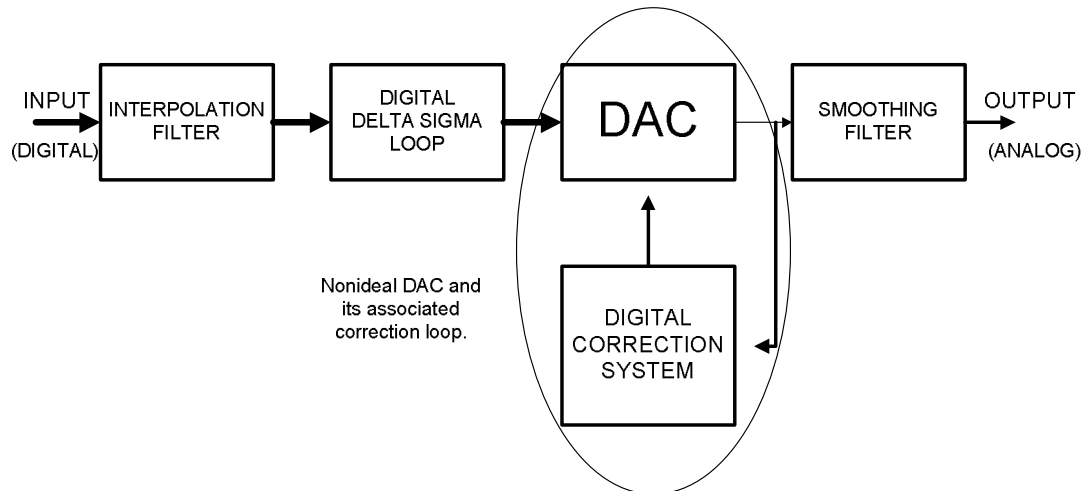


Figure 3.10: Digital to Analog system.

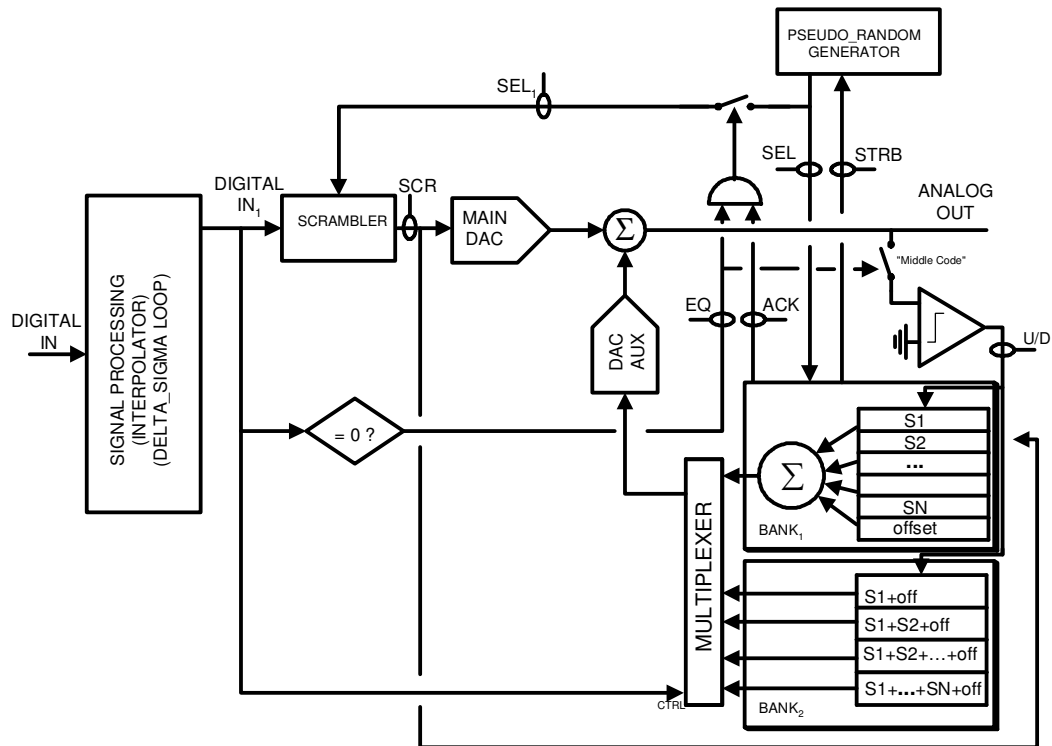


Figure 3.11: Schematic representation of the whole system. The Signal Processing block could contain an interpolator and a modulator to improve the ENOB (at expenses of speed)

The operation of the system can be described as follows: first, the digital input is preprocessed. Data are passed through an interpolation filter and a digital $\Delta\Sigma$ loop.

At the same time (in a parallel process) a Pseudo-Random Code is generated for a generic “middle code”. Considering a bipolar operation, the middle code is the zero code and it corresponds to the use of only half ($N/2$) of the total unit elements that compose the Main DAC. Also, this code will select the corresponding registers in $BANK_1$ (line SEL) to take part in the addition. This operation is realized in advance. Once the sum is completed then the system will wait until a middle code appears. At this point the digital value of the addition will be converted to an analog one (by means of the Auxiliary DAC), the Main DAC will use the corresponding elements (signal SEL will be copied to SEL_1 and will command the Scrambler) and a comparison will be performed.

It should be noted that the Scrambler will select the corresponding elements in the Main DAC only if SEL_1 is active, and this will occur if and only if the code is the middle one (signal EQ active) and at the same time the addition in $BANK_1$ is complete (signal ACK).

After this occurs, the 1-bit comparison will tell whether the corresponding registers in $BANK_1$ must be increased or decreased. In $BANK_2$ the registers will be modified as follows:

referring to Fig. 3.11, it is shown that the first register of BANK₂ will contain the error corresponding to the first element in the Main DAC, the second register will contain the error for the 1st and the 2nd elements added together, and so on, until the last register which will contain the error of the sum of all the unit elements. When a specific unit element is used, then in accordance with the comparator output, the registers in BANK₂ that “contain” this element will be increased/decreased. The idea behind this procedure is that if the residual error is reduced each time a comparison is carried out, then in steady state the registers in BANK₁ will contain a scaled version of the errors of the unit elements. If the registers in BANK₁ and BANK₂ have been updated in the same way and at the same time, then BANK₂ will contain the scaled version of the errors for the 2ⁿ possible combinations (digital codes without being scrambled) for the sum of unit elements of the Main DAC. If the code is not the middle one or the system is busy, then the Auxiliary DAC will feed the corresponding output from BANK₂ (passing through a Multiplexer), and the correction will be performed.

When the addition and the update of the registers in BANK₁ and BANK₂ is completed, then a signal (STRB) indicates that the registers are ready to perform another operation.

The total number of registers is 2N, and the delay in the Analog/Digital loop is minimized with the use of the MUX.

A simplified block diagram is presented in Fig. 3.12, showing the two parallel interconnected processes.

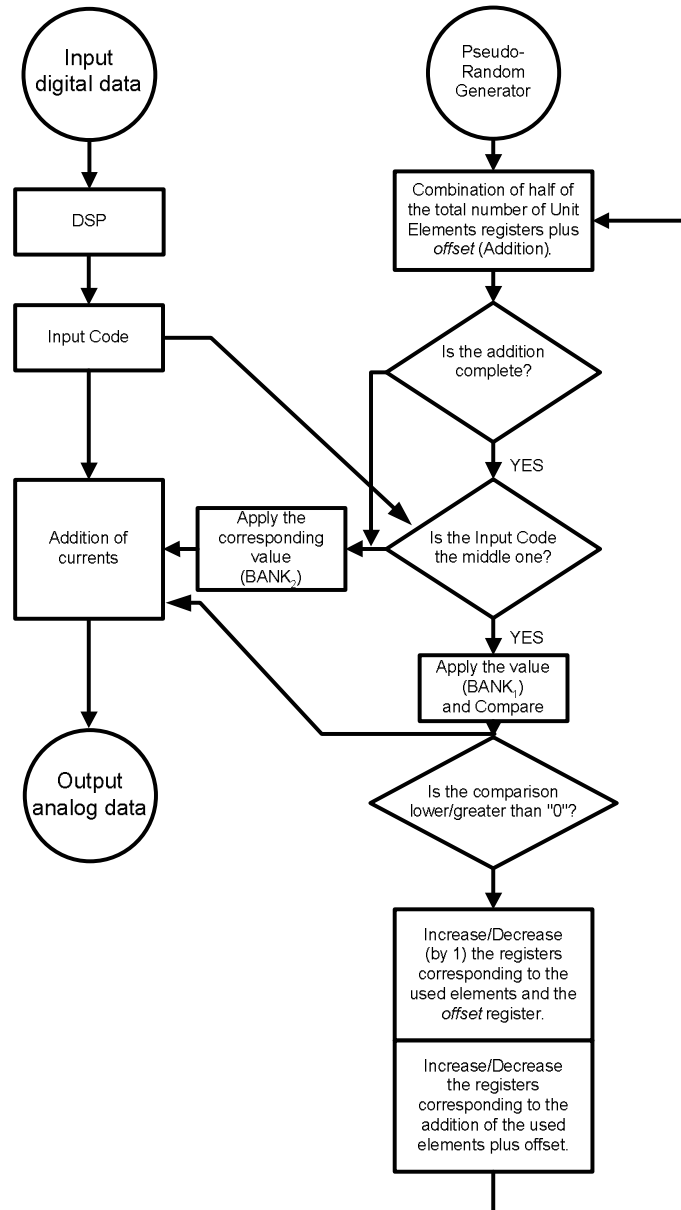


Figure 3.12: Flow graph that represents the operation of the system. 2 Processes running in parallel.

3.3.2 Other Topologies

Analog Implementation:

Another idea for the implementation is depicted schematically in Fig. 3.13. In this case, there are only N “registers” that are combined in the same way than was previously described: half of them will be considered for comparison/updating when the middle code appears (signal “0” used in conjunction with signals S_i from the SCRAMBLER block). The main difference now is that these “registers” can be analog memories (capacitances), and then the Main and the Auxiliary DAC can be combined in only one device. Each analog memory could be the gate capacitance of an auxiliary current source in parallel with one of the unit-element current sources of the Main DAC. Clearly the Auxiliary DAC is absorbed in the main one. In this configuration, because it always needs an addition (no MUX involved) a delay is added in the feedback path if the processing is mixed (A/D). If the processing is only analog, the system is faster.

Another advantage is that now it is possible to use Data Weighted Averaging (DWA) techniques –for low frequencies of operation – combined with the adaptation, i.e., once the system has converged, the coefficients can be frozen and the DWA algorithm can start.

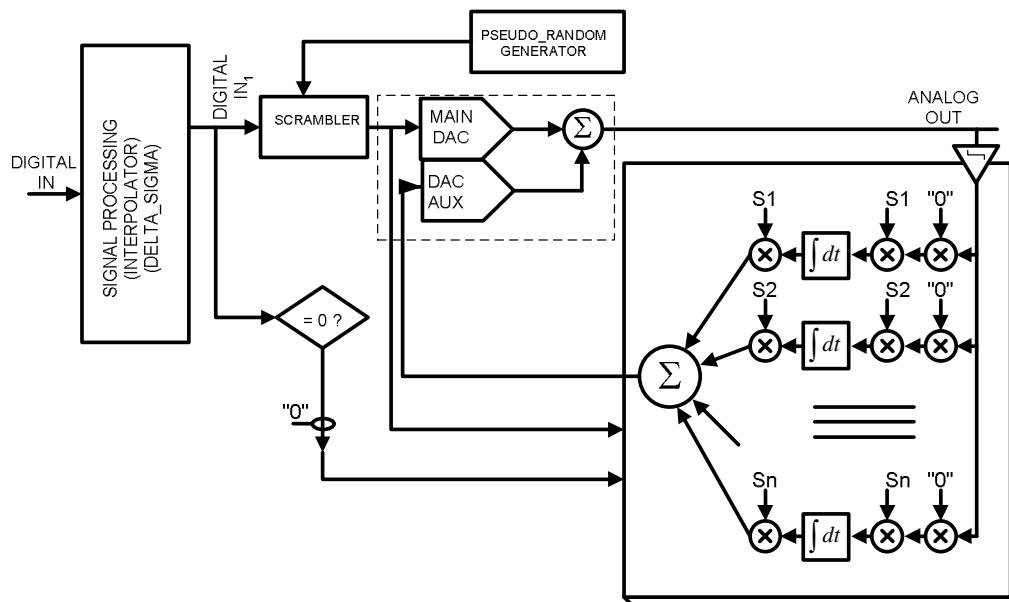


Figure 3.13: Another possible architecture, suitable for a totally analog implementation. The integrators could be implemented using switched current techniques to facilitate the additions (speed up the process).

Mixed-mode implementation:

Consider the schematic of Fig. 3.14. In this case we have the digital (robust) memories acting as before. We are using a MUX and a DEMUX to feed the digital value to the AUX-DAC and to apply its result to a second set of memories, this time analog (holding capacitances). The capacitors store the analog compensation value; they do not play any role as integrators. The OTAs that are connected to these devices deliver an amount of current that will be injected in the source of the cascode transistors, not modifying the output impedance of the overall current source. The switching sequence will select which unit elements are going to be connected in each output, and hence which ones will be updated. The refresh cycle can be periodic and does not have to be clocked at the same system frequency.

3.3.3 *Remarks*

The use of Return to Zero (RZ) clocking improves the glitch immunity (reduces inter symbol interference, or ISI), and at the same time provides a periodic middle code that can be used for comparison purposes.

In the analog implementation, the DC gain of the opamps plays an important role. Based on simulations, in order to get a linearity of 15 bits, a DC gain higher than 60dB is required (practical considerations will elevate that value to the 70~80dB range).

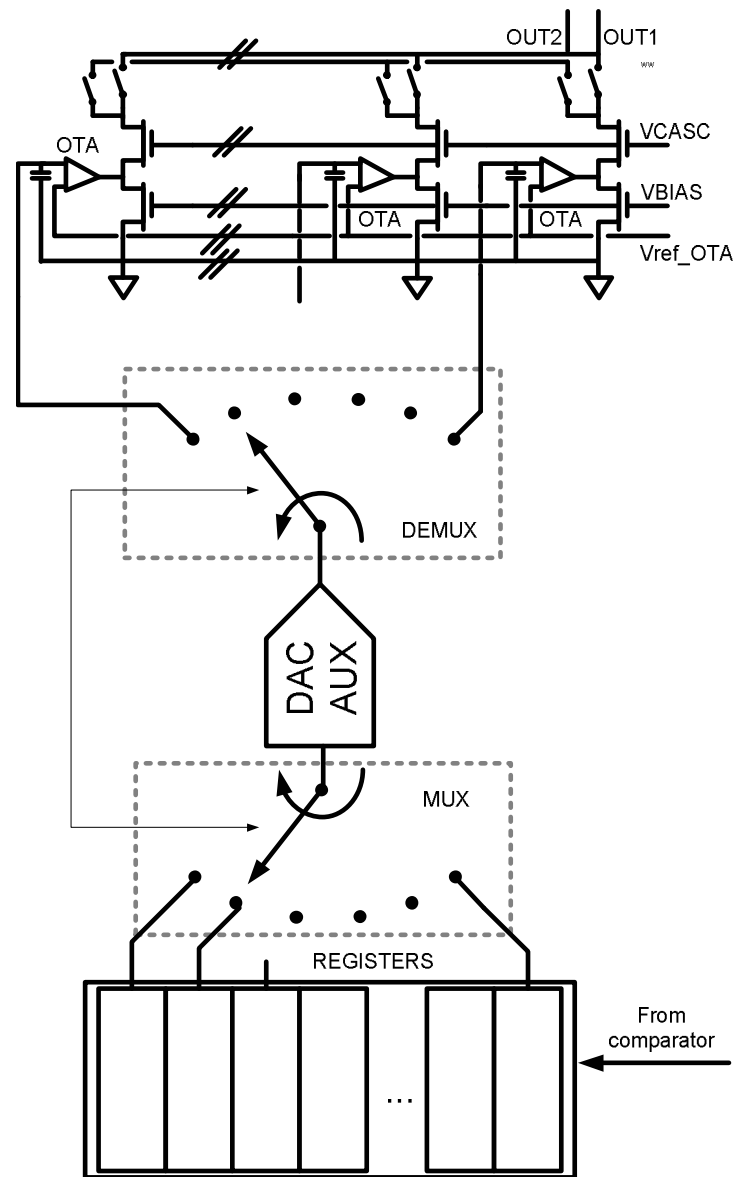


Figure 3.14: Mixed-mode implementation.

3.4 Layout Considerations

This subsection will deal in detail with the current sources matching properties for current-steering DACs. This is related with the fact that the fabricated prototype uses this type of architecture.

First of all, layout (geometrical design) techniques to overcome quadratic nonlinear effects will be addressed, proposing a new layout scheme.

After that, modified calculations to improve fabrication yield will be provided, together with their simulation results corroborating the idea. These are related with the work presented in [14]. Both developments were published in [5].

Considering unavoidable fabrication mismatches, it is known that the errors in a wafer are radial. When a small-dimension dice is obtained, this effect turns into an almost linear gradient that can be compensated with common centroid geometries [38].

When the dice is attached to the package, stress-induced mismatches will appear following a quadratic law [12]. One way to deal with this is to decompose each unit current source and spread those sub-elements in an array, in such a way that to get again the original current source, the parallel connection of some of them will be performed starting in the “middle” and successively adding currents switching alternatively among positive and negative values in order to keep low the DNL.

3.4.1 Contour Around a Line

The question here is: Is there another possibility of laying out the converter? Yes. As mentioned, there exist different ways to overcome quadratic effects [23]. By the time this research was published, almost simultaneously other authors [39] published articles with related approaches.

In order to obtain good linearity here it is proposed to follow a pattern that equalizes the errors for the current sources. The idea is based on the subdivision of the unit current sources (2^n) into ($2^{2(n+1)}$) elements as depicted in Fig. 3.15-a) for a 2-bit example (4 elements). Of course, this is not practical for large n , but for low values ($n=2, 3, 4$) the linearity can be greatly improved. The idea behind the “tile shape” is to think that each current source is a point in the matrix (valid for a large matrix), and then transform the quadratic errors into only a gain error selecting accordingly unit elements around the middle contour (all the composed unit current sources will have the same error as can be inferred from Fig. 3.15-b). The linear errors are automatically compensated because the structure is a common centroid one. The use of the four quadrants minimizes random effects [11].

Fig. 3.15-c) shows the combination of linear and quadratic errors simulated. Each one of the four unit values finished with the same error, and the total error was zero.

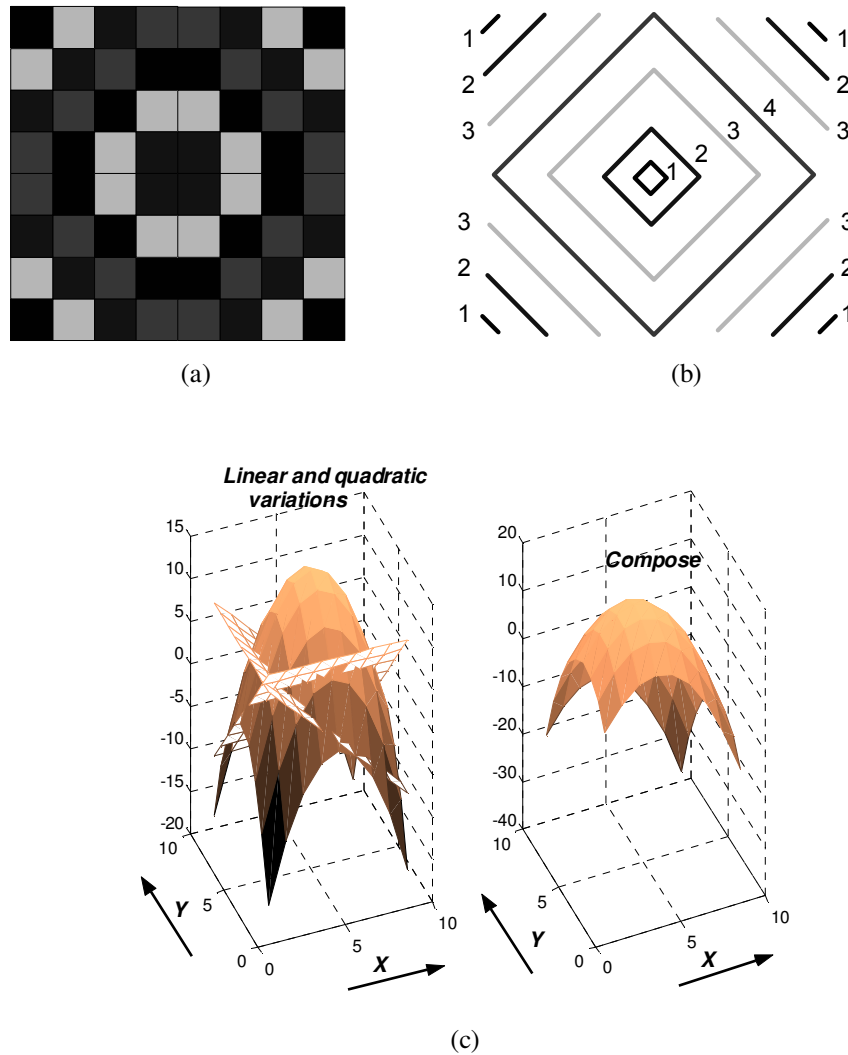


Figure 3.15: a) Possible layout that equalizes the quadratic errors in a 2-bit DAC. All linear errors are compensated by means of a common centroid structure. b) Idea behind the proposed scheme. c) Simulated structure

Because of the symmetry, the overall layout can be subdivided in 4 quarters, as depicted in Fig. 3.16. To ensure matching, rows and files of dummy devices should be added (reducing etching effects).

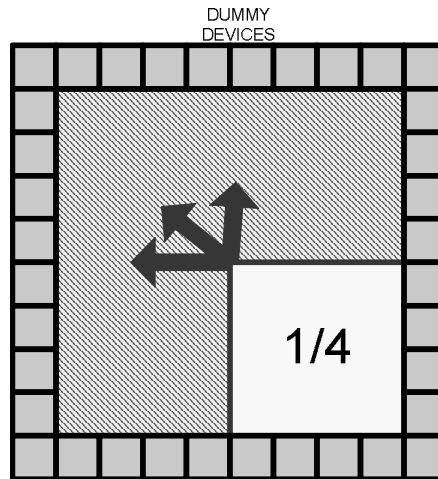


Figure 3.16: Simplified layout

At the layout level, all the bias voltages can be routed using the lower level of metal, after that another metal layer can be used to shield the devices; a third level of metal can handle the control lines.

3.4.2 Matching Considerations

3.4.2.1 Integral Non Linearity (INL) vs. Matching

Considering the INL-Yield (defined as the fabrication yield for an acceptable INL, which is generally taken as 0.5 LSB), then a modification of the work presented in [14] for the normalized deviation of the unit current sources gives,

$$\frac{\sigma(I_{LSB})}{I_{LSB}} \cong \frac{1/2}{C\sqrt{2^n} 2^{n_1}} = \frac{\sqrt{2^{-(n+2n_1+2)}}}{C} \quad (3.15)$$

With,

$$C = inv_normal\{0.5(1 + INL_Yield)\}$$

n = Number of bits of the converter.

$n+n_1$ = Linearity required = n_L

In this case, the INL-Yield will be calculated based on 0.5LSB deviation from the required (and possibly different than the original number of bits) linearity. Figure 3.17 presents the Monte Carlo simulations together with the equation result for 3-bit and 5-bit converters. Each converter having INL > 0.5 LSB of the required linearity (n_L) was considered as a failed component. The normalized yield was taken as the ratio between good samples and the total number of samples simulated. It must be pointed out that the accuracy of the formula increases when the number of bits (n) is also increased. Fig. 3.18 plots the $\sigma(I_{LSB})/I_{FS}$ (I_{FS} ≡Full scale current) for different linearity values, as a function of the number of bits (n), for $INL_Yield=99.7\%$

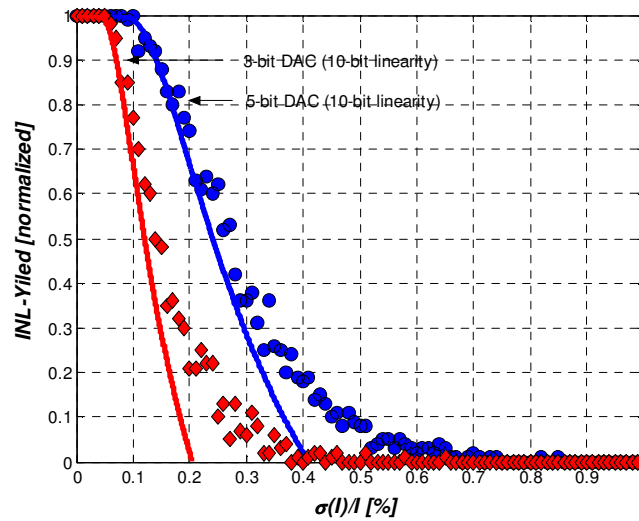


Figure 3.17: INL_Yield as a function of the normalized deviation of the unit current sources of the DAC (3-bit and 5-bit cases).

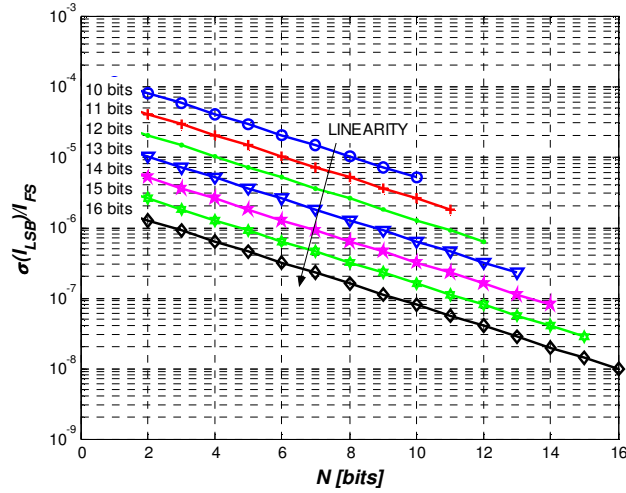


Figure 3.18: Unit current sources deviation normalized to the full scale current for different linearity, as function of the number of bits, for $INL_Yield = 99.7\%$.

For $n=1$ the analysis is invalid (1-bit DAC is inherently linear, hence the value of $\sigma(I_{LSB})/I_{FS}$ is irrelevant.

Using the work presented in [15-16], the minimum area for the unit current transistors can be determined (neglecting quadratic spatial terms) from:

$$\left(\frac{\sigma(I)}{I}\right)^2 \cong \frac{A_\beta}{WL} + \frac{A_{VT}}{WL(V_{GS} - V_T)^2} \quad (3.16)$$

Here A_β and A_{VT} are technological parameters. Data was collected from different publications. The trend of these parameters as a function of the channel length is presented in Fig. 3.19, from which the matching properties could be extrapolated toward smaller sizes. This should be done carefully, because matching is process dependent, and then the parameters depend on metallization, etching, etc. The β factor is related with the transconductance, while the V_T factor relates to the threshold potential of the devices. Based on extrapolated values for a 0.35 μ technology, and in the previous equations, Fig. 3.20 presents the dimensions (W and L) and also the area of the devices for an INL-Yield of 99.7% ($C \approx 3$) in a 10-bits DAC with 10 bits of linearity and a full scale current (I_{FS}) of 1mA.

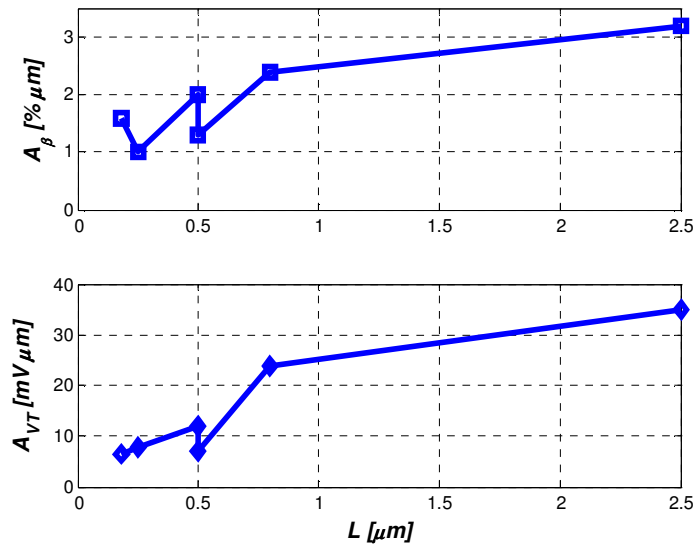


Figure 3.19: Matching parameters as a function of the technology length.

It must be pointed out that the β factor decreases only with the area, while the V_T factor decreases with both area and gate voltage. A good tradeoff presented in [12] is to select the *equality point* (where both error contributions have the same value). For the previous example this gives big values for W and L (in the order of tens of microns). Clearly, with these values the channel length modulating effect and/or the width effects will not affect the operation of the device (it will behave like a true quadratic device).

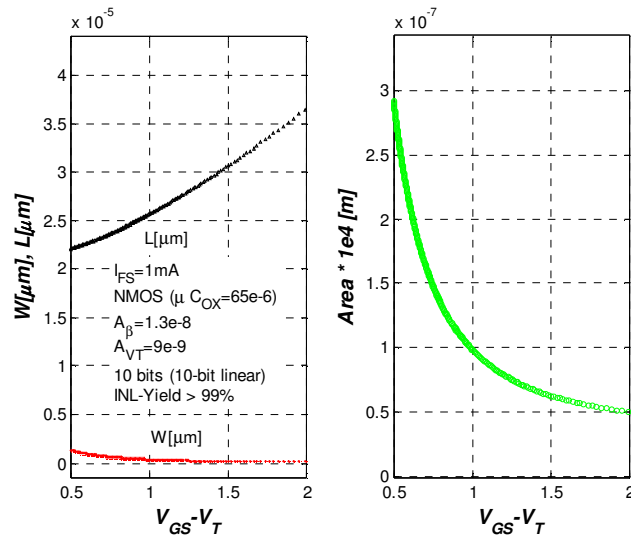


Figure 3.20: Length (L), Width (W) and Area (scaled by $10e4$) for the typical parameters of a 0.5μ technology.

3.4.2.2 Matching and Area

Considering the point at which both contributions (due to V_T and to β) are equal (*equality_point*), the total area depends only in the required linearity and can be approximately expressed as:

$$Area = 2^n WL \cong \frac{2A_\beta}{\left(\frac{\sigma(I_{LSB})}{I_{LSB}}\right)^2} 2^n = 3^2 2^{3+2nL} A_\beta^2 \quad (3.17)$$

From this it can be inferred that the active area needed will remain the same regardless of the number of bits used. The only parameter that dictates the total area (neglecting connections) is the required linearity. Fig. 3.21 presents a plot of this fact. The area grows by a factor of 4 for each linearity bit added.

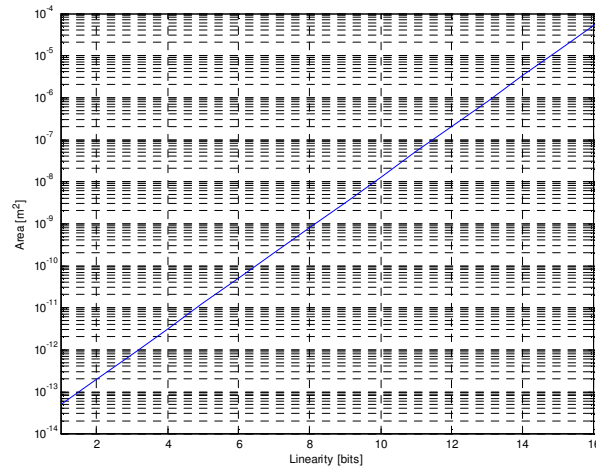


Figure 3.21: Area (Active) as a function of the linearity for a typical 0.5 μ m process.

The advantage of the DAC correction topology is evident. In that architecture, to get 15 bits of linearity, two 10-bit DACs are required (Main and Aux). The area is roughly twice the area of a 10-bit converter. On the other hand, using the previous equation, the required area should be 32 times the 10-bit area. Of course, no logic and additional circuitry was taken into account in this calculation, but they can be made relatively small compared with the final area. Another advantage that can be expected is that increasing the accuracy using big devices reduces the maximum achievable operating speed, which does not occur in the corrected system.

3.5 Circuit Design Point of View

This subsection will describe novel ideas about the implementation of the current sources and its associated drivers. The ideas behind are the improvement of the output resistance (diminishing code-dependent nonlinear effects), and the reduction of dynamic degradation due to switching glitches.

3.5.1 Active Cascode in Current Sources

If the output resistance is of concern, the current sources can be alternatively implemented using a novel active cascode configuration [5], depicted schematically in Fig. 3.22.

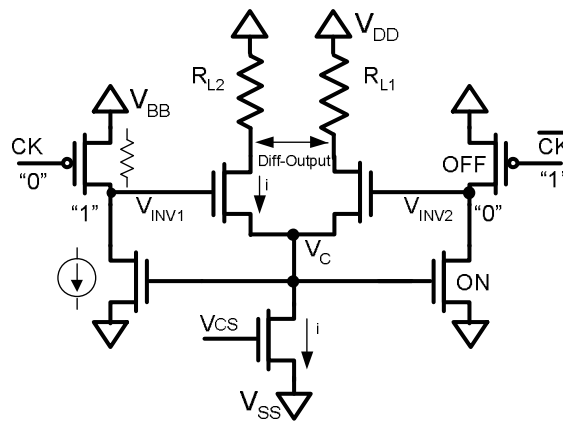


Figure 3.22: Schematic of the modified active cascode unit current cell.

The extra added circuitry is shown in the figure, together with an example, in which the left side behaves as an inverter, and the right side is disconnected (switched off). It is also intrinsic to the circuitry that the cross-over point could be set high, hence minimizing the drain variation of the current source (V_C remains more constant, when compared with a conventional scheme). Fig. 3.23 shows some transient Spectre[®] simulations, in which these effects can be appreciated in more detail (0.35 μm technology). Fig. 3.24 shows the effect of the active cascoding, with an increase of approximately six times for the output impedance (current source of 1mA, load of 50 Ω and fast switching). The operation speed is not greatly affected, since R_L sets the output dominant pole (a low-value resistor).

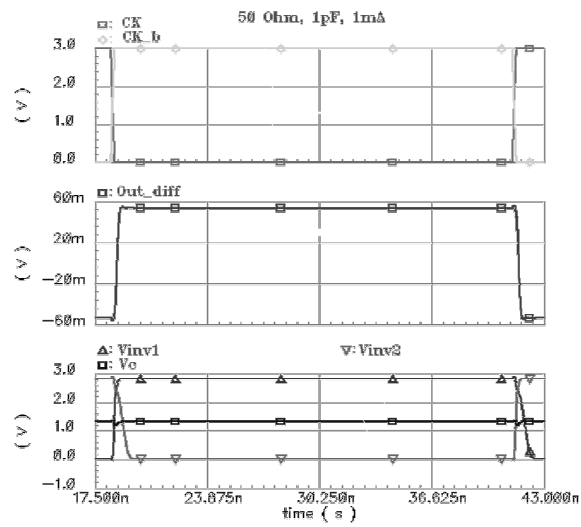


Figure 3.23: Transient simulation of the unit current source. The differential voltage is still fast. Important to note is the small variation in V_C (drain voltage of the current source)

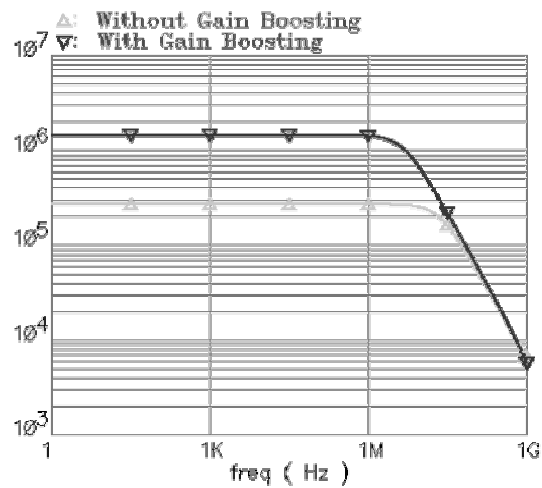


Figure 3.24: Increase of the output impedance using gain boosting. Approximately six times.

3.5.2 Latches and Crossover Point

The crossover point of the input control signals is another important issue in current-steering DACs. Depending on whether it is very high or very low, the switching characteristics are going to be influenced. As an example, Fig. 3.25 shows schematically different switching conditions (with ideal clock waveforms), which can cause glitches and degrade the dynamic linearity. If the crossing point is selected too low, then during a small amount of time both switching transistors will be OFF, and then the MOS implementing the current source will be in its linear region; when it is time to recover the normal operation, a delay and a glitch will be imposed. There exists an optimum point that minimizes delay and peak response, which was empirically found by simulation.

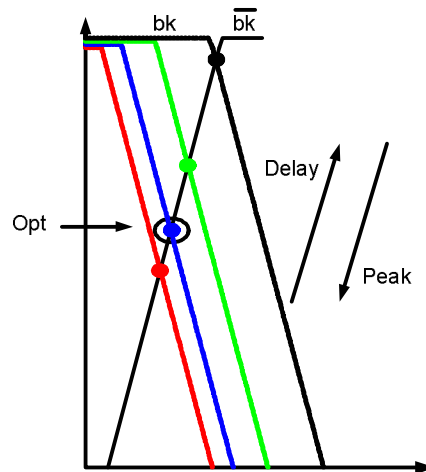


Figure 3.25: Unit current sources different crossing points

Considering the previous fact, a fast driver that controls this crossing was developed. The specially designed high-speed latch is shown in Fig. 3.26. All transistors are minimum dimension MOS except the large PMOS pull-up ones. A big pull-up will force a fast rise time, setting the crossing point high and vice versa (selecting to use large NMOS pull-down resistors the opposite situation can be gotten). A small delay after the fast rise time, the slow fall time will start (Fig. 3.26-b). The auxiliary inverters help to reduce feedthrough problems and stabilize the system at high frequencies. Two extra transistors were added to compensate feedthrough injection. These devices act as MOSCAPs neutralizers, having drain and source shortcircuited, half of the pull-up MOS

aspect ratio (W/L), and are clocked in a complementary way. Simulations and measured results have shown a large reduction of the glitch power.

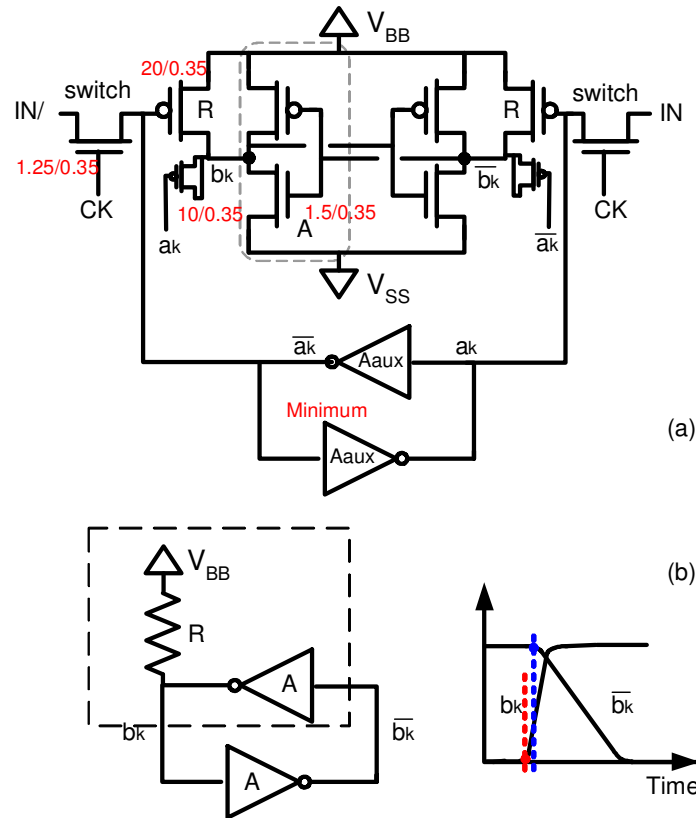


Figure 3.26: Proposed Latch.

The previous latch can have all the transistors of minimum dimensions, except the pull-up. It is highly efficient in terms of area and speed.

CHAPTER 4. DIGITALLY CORRECTED DAC

This section will deal with the architectural fine points of the digitally corrected current-steering DAC.

Starting with a possible implementation, errors due to resistors mismatch and to the comparator will be addressed. Analytical models and a mathematical analysis of the system will be presented. A novel switching sequence is then introduced, which is intended to speed up and to simplify the digital hardware. Finally, high level simulation results are presented, showing the feasibility of the proposed idea.

4.1 Possible Implementation

As a graphical example, Fig. 4.1 represents a possible fully differential implementation (2 bits). In this case, the unit elements are current sources of unit value (i). The comparison is carried out between the two (randomly) selected halves. As explained in previous sections there are two banks of memory: one for the storage of the individual errors, and the other for the ordered correction codes. There exist also an extra register (*offset*) whose function will be explained in detail in the next subsection; here it is only worth to mention that load mismatch and comparator offset can cause instability in a fully differential system. The manner in which the *offset* register is updated is related to the comparator output.

Because the binary 2-bit input word can only address 4 different codes, either S_A or S_E must be discarded (if symmetry is important, both of them can be disregarded in the final implementation). For the sake of generality in the explanation that follows, both of them will be kept.

In order to update the registers, the sum of half of the elements plus the offset is subtracted from the sum of the other half. The registers in $BANK_1$ are updated as described previously in Sec. 3.1.3. In $BANK_2$ now the registers are updated only considering the positive (or the negative) half, as depicted in the following example: if the positive half is composed of elements 1&3, that means the negative one is composed of elements 2&4. Under these assumptions, supposing the comparison dictates an increase in the positive half (signal U/D high), then S_A and S_B will be increased by 3, S_C and S_D will be increased by 1, and S_E will be decreased by 1. Registers S_1 , S_3 and *offset* will be increased by 1.

The output voltage value is the difference between the two halves. Each code will be corrected using $S_A \dots S_E$ respectively through the Multiplexer and the Auxiliary DAC (represented in the diagram of Fig. 4.1 as the current $I_{CORRECT}$).

This method has shown to be really efficient in terms of speed; its problem is complexity. Another possibility is to update only one element at a time (it can be updated the first one that was randomly selected). The price paid in speed is compensated with the simplicity of the implementation. Example 1: suppose that the element S_2 was the first element in the random selection, and that the comparison dictates an increase of its value. Consequently, S_2 and the *offset* register will be increased by 1. In $BANK_2$, S_A , S_B and S_C must be increased by 2, while S_D and S_E will be left unchanged. Example 2: suppose that the same element (S_2) was selected, but the comparison dictated a decrease. Now S_2 and the *offset* register will be decreased by 1. In $BANK_2$, S_A , S_B and S_C will be decreased by 2 and S_D and S_E will be left unchanged. The idea behind these examples is that the increases (decreases) in $BANK_1$ are in steps of 1, and in $BANK_2$ they are in steps of 2 (this can be done easily hard wiring a 0 to the right of the registers, expanding the digital word). Also in $BANK_2$ there exists the possibility of leaving unchanged the value of the counters, which can be again easily implemented using a Chip Enable (CE) connexion.

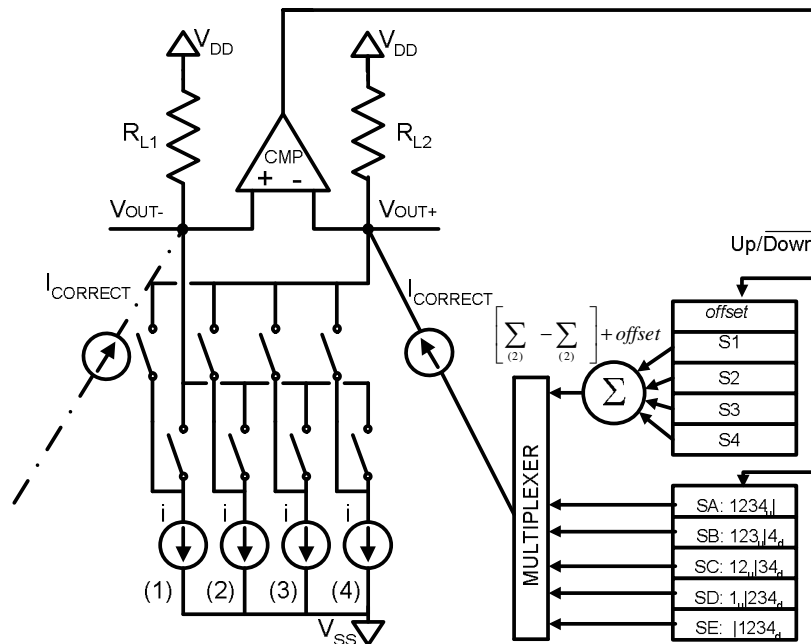


Figure 4.1: Fully differential architecture. 2-bit example. $S_1 \dots S_4$ store the individual errors and *offset* stores the offset due to mismatches in R_L and offset in the comparator. $S_A \dots S_E$ store the different combination errors (letter u (d), in $S_A \dots S_E$, points the relation with $S_1 \dots S_4$ for *increase* (*decrease*) the corresponding register)

4.2 Offset Issues and the Acquisition of Unit Element Errors

Offset compensation provides insensitivity of the system to load resistor mismatches and comparator offset. It is necessary, since as the unit-element random selection process is carried out, having a mismatch is going to impede the system to converge. Moreover, considering the offset in the comparator, this DC value could be integrated in the counters making the system unstable.

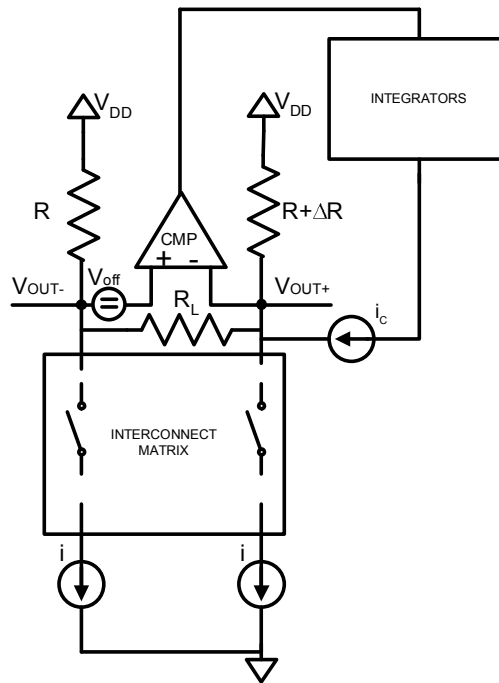


Figure 4.2: Schematic of a 1-bit DAC with nonidealities. R_L could represent the effect of a coaxial line connected across the differential output.

Consider only a 2-element current-steering DAC, as depicted in Fig. 4.2. The Interconnection Matrix only symbolizes the scrambling for the middle code. Consider the unit elements without error; hence the matrix does not have any effect in the dynamics of the system. The correction current, for the sake of simplicity, will be considered to be injected in only one side as depicted. The load resistance (R_L) can represent the impedance of a coaxial line connected between the outputs. Offset in the comparator (V_{off}) and resistor mismatch (ΔR) are considered.

Simple loop analysis gives the required correction current value (i_c):

$$i_c = V_{off} \left(\frac{2R + R_L + \Delta R}{R_L(R + \Delta R)} \right) - \frac{i\Delta R}{R + \Delta R} \cong V_{off} \left(\frac{2R + R_L}{R_L R} \right) - \frac{i\Delta R}{R} \quad (4.1)$$

Without the load resistor, the part of the correction current that depends on the comparator offset reaches its minimum. Considering an infinite gain comparator, the differential output after the compensation has settled will present a DC offset equal to the comparator offset.

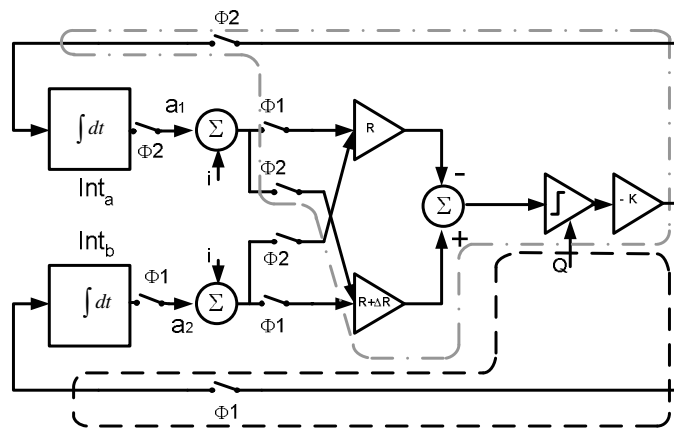


Figure 4.3: Block diagram for offset analysis

Another way to analyze the problem, now from the system point of view, is as follows. Consider no offset in the comparator, and a resistor unbalance, then an equivalent block diagram as the one depicted in Fig. 4.3 can be used. The outputs of the integrators are currents, and the gain blocks represent the resistors.

Because there are only 2 elements and a scrambling process, it can be supposed that there are 2 non-overlapping phases as depicted. Consider also that the update is made in the half that is connected to the mismatched resistor. This feedback scheme forces the error signal before the comparator to be zero, hence, in steady state, after the calibration converges, the quantizer can be thought as adding only granular noise with zero mean. Because the randomness of the process, it can be inferred that in steady state the average values of a_1 and a_2 are equal. If $avg(a_1) = avg(a_2)$, then the loop in both cases is the same. The average values can be calculated from:

$$-avg(a_1)R + i\Delta R = 0 \quad ; \quad avg(a_1) = avg(a_2) = i\Delta R/R \quad (4.2)$$

The previous result can be extended from 2 to n elements. Because of the exclusive character of the process, if an element is in one side then it cannot be in the other one. Neither can be updated, moreover, because of the uniform scrambling all the elements will be in average half of the time in each side. The idea is that instead of only one current i , there will be $(n/2)i$ current sources in each side.

Now, if the comparator has offset it can be replaced by an equivalent resistor error (ΔR_{eq}):

$$\frac{n}{2} i \Delta R_{eq} = V_{off} \quad (4.3)$$

Then the previous results can be used.

Because each register (counter) will contain a value that will depend on the offset, but they were intended initially to store the individual errors of the unit elements, the problem that arises is how much of the “real” error will be visible under the presence of such an offset value. Consequently, the offset must be minimized in the system. By means of circuit techniques (autozero, Correlated Double Sampling [32-33], etc.) it can be greatly reduced.

The offset and the errors can be acquired simultaneously from the beginning and at the same time. The idea is that if there is a scaled version of the offset (KV_{off}) common to all the registers of BANK₁, then the registers in BANK₂ will contain a number of scaled offsets that will be equal to the number of unit elements that the corresponding register must correct. As a conclusion, this scaled offset is going to introduce only an output scaling effect, but not any nonlinearity.

It is also possible to have an initial phase for offset acquisition at the beginning of the calibration process, and after that the correction and the offset can run together in background. The idea is to separate the offset estimation from the error estimation. In the start-up all the comparisons will be made only to acquire the offset value. At this time, a special *offset* register (integrator) will be updated, and with this value all the registers in BANK₂ (the bank that contains the thermometer estimations) will be also modified. When the real calibration starts, the value of the offset register will be added with the values of the registers used, and the comparison will be carried out as was pointed out previously. In order to estimate when the real comparison starts, an initial offset value (process and matching considerations) should be estimated, and then using the value of the LSB in the auxiliary DAC, the maximum number to be stored in the register can be calculated. Fig. 4.4 shows simulations of a system (with nonidealities), showing the offset acquisition (note the slope overload and the granular noise parts).

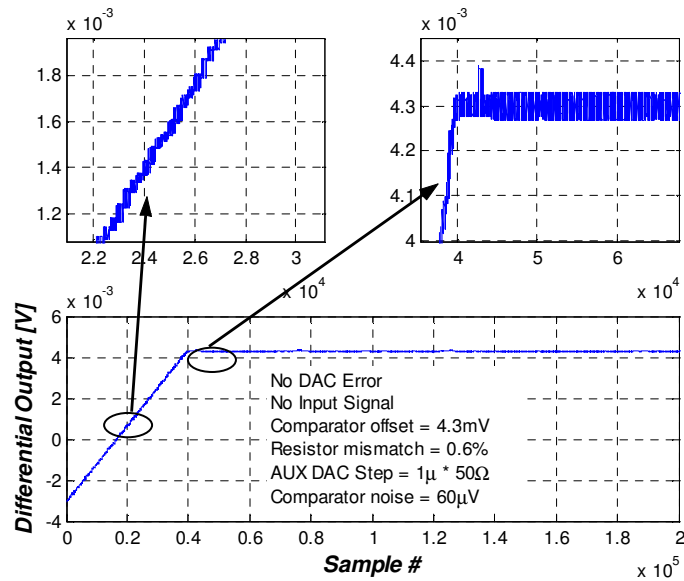


Figure 4.4: Simulation results. Details: Adaptation noise & steady-state noise. AUX-DAC is 10 bits linear.

4.3 Analysis

In this paragraph a linear model will be considered for the topology, taking into account only the output in the *Middle-Code* time points. It will be shown that the correction loop acts similarly to a *delta loop* [10] for the Main DAC error.

To start, it is convenient to define the following:

$E=[e_1, e_2, \dots, e_N]$ is the vector of individual errors in the Main DAC.

$\hat{E}=[\hat{e}_1, \hat{e}_2, \dots, \hat{e}_N]$ is the vector of individual error estimates.

$\Delta=[\delta_1, \delta_2, \dots, \delta_N]$ is the vector of differences defined as $\delta_i=e_i - \hat{e}_i$

\hat{E} and E are vectors with the special property that in each one, one half is subtracted from the other half randomly and there is also a one-to-one correspondence between their used elements.

An equivalent model for correction of the i -th error is shown in Fig. 4.5. In this case, it can be seen that all the others element error differences act as a noise signal in the forward path of a delta modulator. Considering digital integrators (counters) then dead zones can be introduced. The idea is to perform a wired truncation, discarding the LSBs of the counters, as depicted in Fig. 4.6. This has as advantage an increase in the insensitivity of the acquisition, as will be explained later. In the

following ideal model, no dead zones introduced by digital truncation effect were considered, as is the case for a purely analog processing scheme, but the variation in gain was taken into account. The gain G is due to the truncation and also models the scaling in the Auxiliary Digital-to-Analog converter. In both cases is much less than 1.

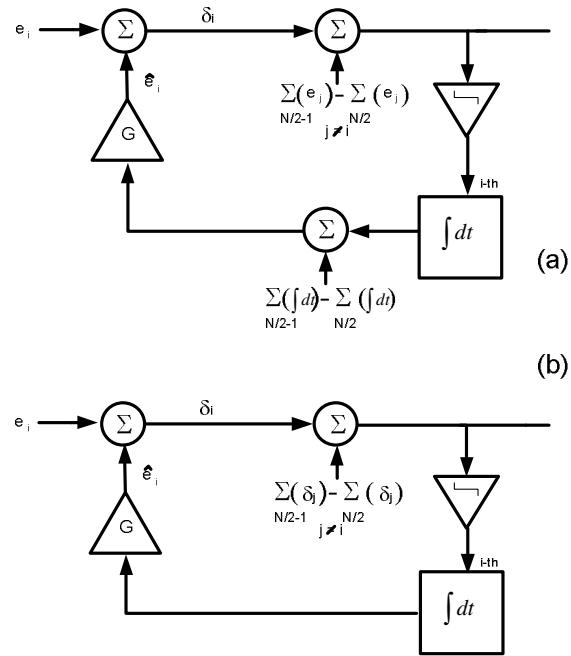


Figure 4.5 Equivalent linear model of the correction loop for the i -th error. Considering a linear system, the scheme of a) becomes the one of b)

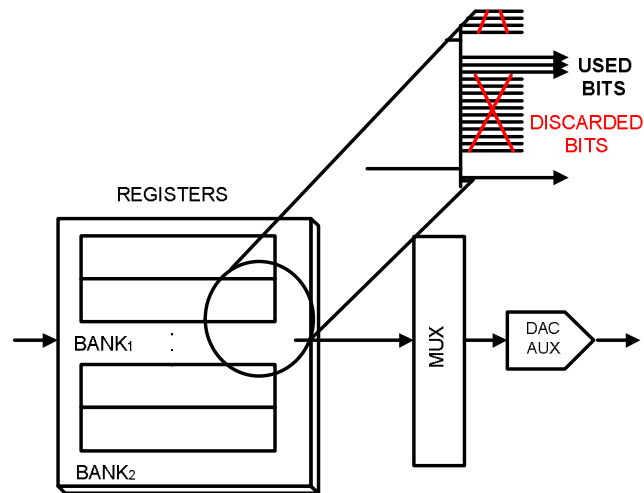


Figure 4.6: Schematic picture for the input of the MUX. Some MSB are considered and the other bits are not taken into account. This process is inherently a truncation that can be modelled as an extra (but negligible) error (floor).

Now, the output will have a zero mean (property of delta modulation), but with an error whose variance is proportional to the sum of all the other variances.

Consider now Fig. 4.7. It shows the convergence of the algorithm with zero input (only the errors are present). The figure also depicts two generic cases for a 2-bit (4 units) system: 1) correction of 1 element at a time, 2) correction of 2 elements at a time (meaning correcting half of the unit elements). It can be seen that the convergence time is lower in the case in which all the elements present in one half are corrected at the same time, but the errors (initial and the final deviation) are larger. Also it is shown the adaptation noise region and the granular noise region. The figures were obtained as an average of 30 realizations.

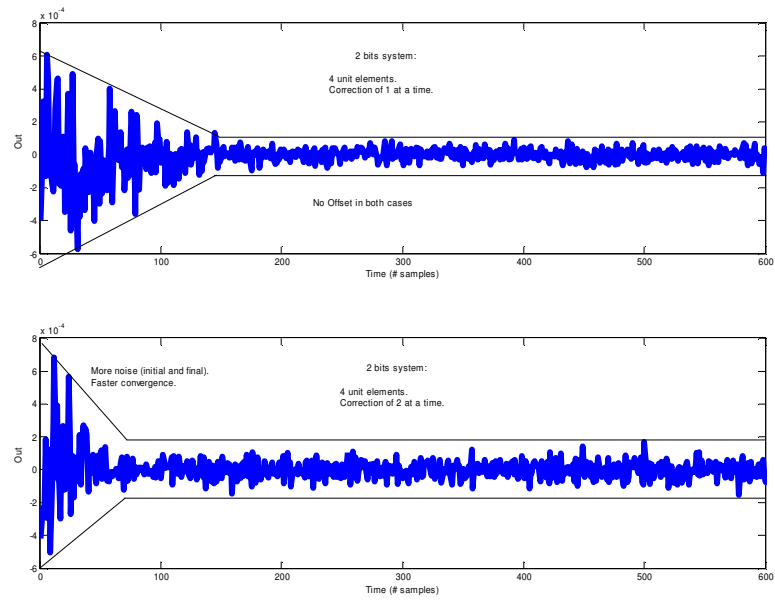


Figure 4.7: Simulated results for a 2-bit generic system. Average over 30 realizations.

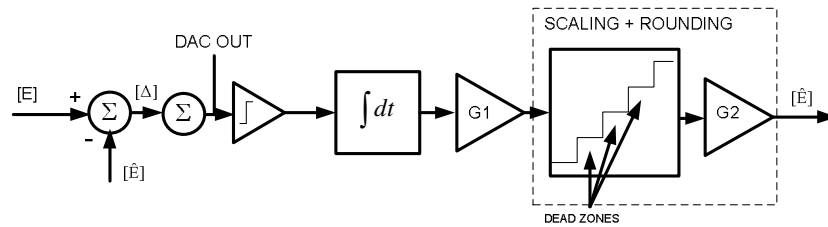


Figure 4.8: Schematic of the system under locking condition. G_1 : Truncation gain, G_2 : gain of the AUX-DAC.

Consider now the system is in steady state. The truncation process in the output of the counters and before the Auxiliary DAC has two effects: first of all it is a scaling, second it introduces dead zones. Both effects are beneficial for the loop operation.

With the process of scrambling all the combinations are possible. Then, it can be easily shown that

$$\overline{[\Delta]} = \overline{[E]} - \overline{[\hat{E}]} = \overline{[E]} - \overline{[\hat{E}]} = 0 - 0 = 0 \quad (4.4)$$

Meaning that the mean value at the input of the comparator will be also zero. Really, the feedback forces this condition, hence having $E\{E\}=0$ is a sufficient condition, but not necessary for the system operation. Considering a simplified schematic in steady state for the system, as depicted in Fig. 4.8, it can be inferred that if the dead zones are large enough to absorb the variations around the mean values, then the system will be in open loop. Any posterior variation can unlock the system, and force it to be in closed loop again, where the variation will be corrected.

As another point of view, the whole system can be thought as a code division multiple access (CDMA), but in closed loop, with the quantization noise equivalent to the channel noise.

As it was pointed out previously, the feedback loop forces the signal before the comparator to be zero. Under this condition an equivalent diagram as the one shown in Fig. 4.9 can be assumed. In this one, each ϕ_i signal can be -1 or +1, representing that randomly half of the unit elements are in the *positive side*, and the other half in the *negative* one. That can be mathematically expressed as:

$$\Phi_i = \pm 1 \quad \Phi_i^2 = 1 \quad ; \quad \sum_i \Phi_i = 0 \quad (4.5)$$

The output of this system (CMP_{in}), which represents the input to the comparator, in the middle-code points (for a 2-bit example) is given by:

$$CMP_{in} = (e_1 - \hat{e}_1)\Phi_1 + (e_2 - \hat{e}_2)\Phi_2 + (e_3 - \hat{e}_3)\Phi_3 + (e_4 - \hat{e}_4)\Phi_4 \quad (4.6)$$

with the following characteristics:

$$\begin{aligned} E\{CMP_{in}\} &= 0 \\ V\{CMP_{in}\} &= \sum_i V\{(e_i - \hat{e}_i)\Phi_i\} \end{aligned} \quad (4.7)$$

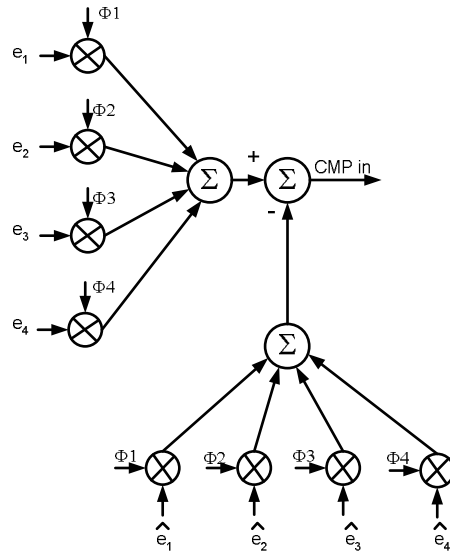


Figure 4.9: CMP_{in} is the input to the comparator in the middle code. 2-bit system

Here $E\{.\}$ and $V\{.\}$ are the expected value and the variance operators.

It can be shown that:

$$V\{(e_i - \hat{e}_i)\Phi_i\} = V\{\hat{e}_i\} \quad (4.8)$$

If the variance of \hat{e}_i is limited by the step of the AUX-DAC, and considering a Gaussian distribution (because of the integrators and additions of multiple random variables), then it is easy to understand why in Fig. 4.7 the correction of many elements at the same time has the biggest deviation from the mean value.

4.4 Switching Sequences - How to Speed-Up the Hardware

Up to now the use of full randomization has been considered for the selection of the unit elements in the case of appearance of the middle code. For a 3-bit DAC (8 unit elements) this is equivalent to consider 40,320 different permutations (brute force methodology). Having interest only in the middle code, and also needing some information about which is the first element (the one that will be updated), then there are 280 different combinations² which can be randomly selected for the switching. This can be implemented in ROM. Is there another possible (and preferably reduced) switching sequence? Yes. Maybe the most elegant solution is based on the following analysis. Suppose the following combinations for a 3-bit system (TABLE 4-I-A), in which each entry can be selected randomly, representing different combinations of residual errors (δ_i) in the middle code. These errors are represented as circles ($\delta_1 \dots \delta_8$) in Fig. 4.10.

TABLE 4-I
3-BIT SYSTEM SWITCHING SEQUENCES

A	B
1 $\delta_1 + \delta_2 + \delta_3 + \delta_4 - \delta_5 - \delta_6 - \delta_7 - \delta_8$	11 $\delta_5 + \delta_6 + \delta_7 + \delta_8 - \delta_1 - \delta_2 - \delta_3 - \delta_4$
2 $\delta_2 + \delta_1 + \delta_3 + \delta_4 - \delta_5 - \delta_6 - \delta_7 - \delta_8$	21 $\delta_6 + \delta_5 + \delta_7 + \delta_8 - \delta_1 - \delta_2 - \delta_3 - \delta_4$
3 $\delta_3 + \delta_2 + \delta_1 + \delta_4 - \delta_5 - \delta_6 - \delta_7 - \delta_8$	31 $\delta_7 + \delta_6 + \delta_5 + \delta_8 - \delta_1 - \delta_2 - \delta_3 - \delta_4$
4 $\delta_4 + \delta_2 + \delta_3 + \delta_1 - \delta_5 - \delta_6 - \delta_7 - \delta_8$	41 $\delta_8 + \delta_6 + \delta_7 + \delta_5 - \delta_1 - \delta_2 - \delta_3 - \delta_4$
5 $\delta_5 + \delta_2 + \delta_3 + \delta_4 - \delta_1 - \delta_6 - \delta_7 - \delta_8$	51 $\delta_1 + \delta_6 + \delta_7 + \delta_8 - \delta_5 - \delta_2 - \delta_3 - \delta_4$
6 $\delta_6 + \delta_2 + \delta_3 + \delta_4 - \delta_5 - \delta_1 - \delta_7 - \delta_8$	61 $\delta_2 + \delta_6 + \delta_7 + \delta_8 - \delta_1 - \delta_5 - \delta_3 - \delta_4$
7 $\delta_7 + \delta_2 + \delta_3 + \delta_4 - \delta_5 - \delta_6 - \delta_1 - \delta_8$	71 $\delta_3 + \delta_6 + \delta_7 + \delta_8 - \delta_1 - \delta_5 - \delta_3 - \delta_4$
8 $\delta_8 + \delta_2 + \delta_3 + \delta_4 - \delta_5 - \delta_6 - \delta_7 - \delta_1$	81 $\delta_4 + \delta_6 + \delta_7 + \delta_8 - \delta_1 - \delta_2 - \delta_5 - \delta_3$

The main supposition is that only the first element will be changed or updated. In this example, δ_1 is shifted and its place is used by one of the seven remaining elements. Looking carefully, it can be discovered that there are direct correspondences between some of the elements. As an example, the subtraction of entries 1 and 5 reveals a direct strong connection between

² $280 = 8 \binom{7}{3}$; fixing the position of the first element, the 3 remaining that are going to be in the positive side can be permuted in 7 different places.

elements δ_7 and δ_8 . These connections are symbolically represented by the arrows of Fig. 4.10., and they are made automatically when the system jumps from one entry to the next one (from entry 1 to 5 or vice versa in the current example). Similar results can be inferred for the other elements.

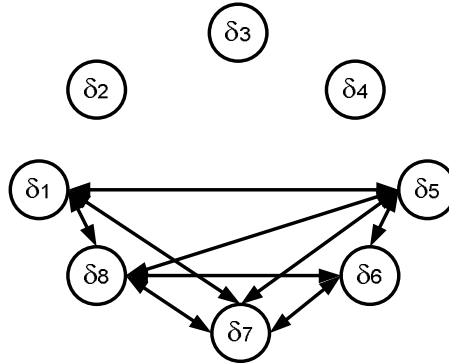


Figure 4.10: Possibilities of connection between the different entries (TABLE 4-I-A)

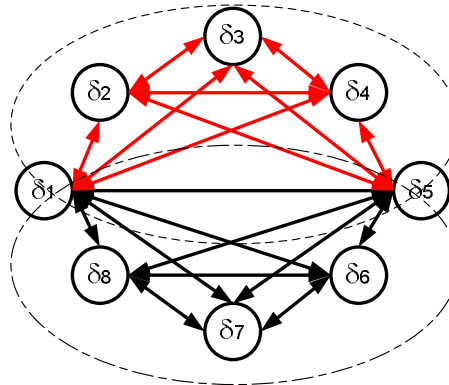


Figure 4.11: Putting together TABLE 4-I A & B. It can be seen that now the direct connectivity between elements is almost full, but still separated in two halves.

Based on the scheme of TABLE 4-I-A, and using a similar reasoning, the *connection* of elements $\delta_2 \dots \delta_4$ can be shown to be weak or indirect. The main reason is that no information can be obtained from the switching among entries 1 to 4, because the 2 halves are the same in all the cases. That means there is not a direct connection of these elements and the remaining ones. Still entries 2...4 are necessary, because they are forcing in an indirect way the values of $\delta_2 \dots \delta_4$ to be linked with the other elements, and also they equalize the usage of all the 8 units.. Now the idea is to introduce a new switching scheme that complements the previous one, as the one shown in TABLE 4-I-B. The new connections are depicted in Fig. 4.11. This scheme works very well and now there are only 16 different possibilities of switching. Moreover, because the fix number of possible random sequences

for the middle code, there is not anymore a necessity for register additions, hence no digital adder is needed and the system is simpler and faster. The price paid is an increase in the used digital memory. For a n -bit DAC (2^n unit elements), they are necessary $2 \cdot 2^n$ registers for the switching, plus 2^n registers for the different codes applied through the MUX (increase of $2^n = N$ registers compared with the full random scheme).

4.5 Simulation Results

In this section the simulation results for a fully differential correction topology will be presented. A 3-bit ($N = 8$) modulator was selected as a test vehicle. Zero-optimization procedure] was used to reduce the in-band quantization noise of the delta-sigma modulator. Oversampling Ratio (OSR) = 8 was used, and an eighth-order structure was employed. The initial errors, the estimated error and the residual error are shown in Fig. 4.12. The initial error corresponds to a variation of $\pm 0.4\%$ (8 bits) in the unit elements (of 2.5 mA). The final error is in the range of $1\mu\text{A}$ (the step of the AUX-DAC). Total current output of 20 mA and $50\ \Omega$ resistive load (output values between $\pm 1\text{V}$) were considered. Convergence is shown in Fig. 4.13, as a function of the sample number (considering RZ). The offset was previously acquired.

The histograms of Fig. 4.14 show the distribution (mean suppressed) for all the registers that store the individual values. Because of the use of the novel switching scheme the distributions are not exactly Gaussian. Considering full randomization, then the distributions shown in Fig. 4.15 corroborates this assumption (still there are small deviations but this is mainly thought to be due to the facts of having few elements and also truncation)

Based on the previous simulation results the dead zones were estimated.

Fig. 4.16 shows three cases for the output spectra for a three tone (low frequency) input signal, in order to visualize intermodulation effects: the initial case (without any correction), the ideal case and the corrected one. It must be pointed out that by means of simulations it was proved that the initial error does not matter; the performance reached has always been the same, and it is determined by the step size of the AUX-DAC.

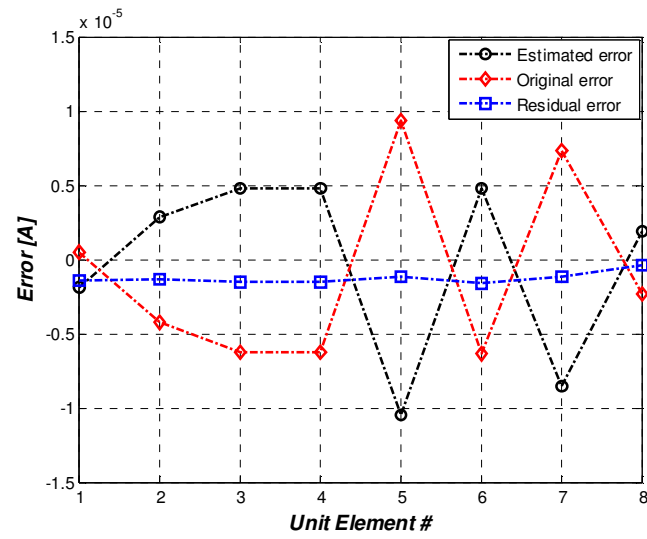


Figure 4.12: Errors in the 3-bit simulated system.

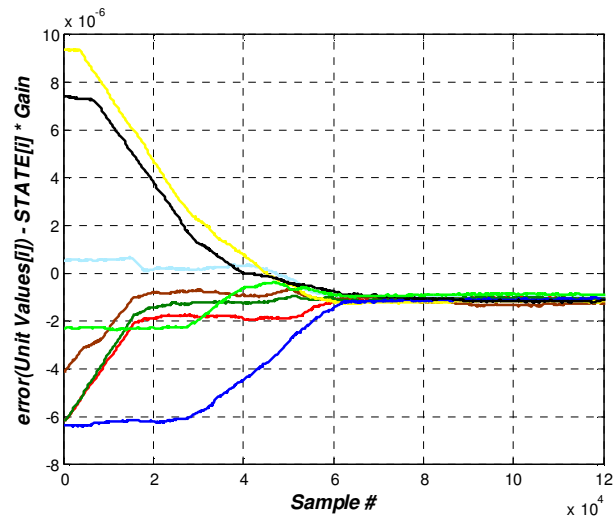


Figure 4.13: Convergence to steady state of the eight individual registers (values taken before truncation operation).

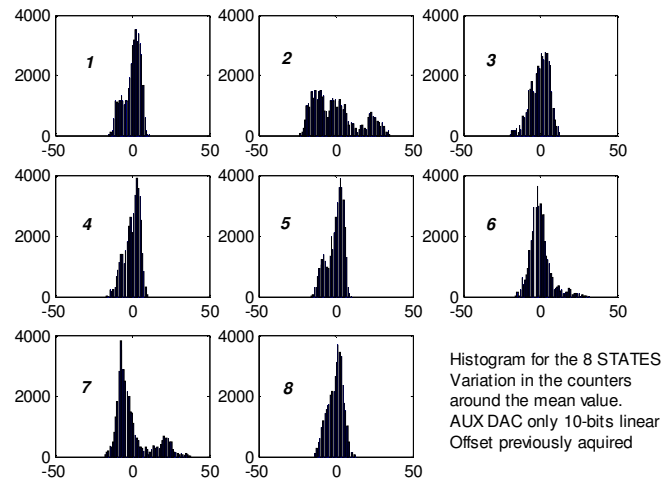


Figure 4.14: Histograms of counters output for the 8 unit elements around their mean value after convergence. New switching scheme.

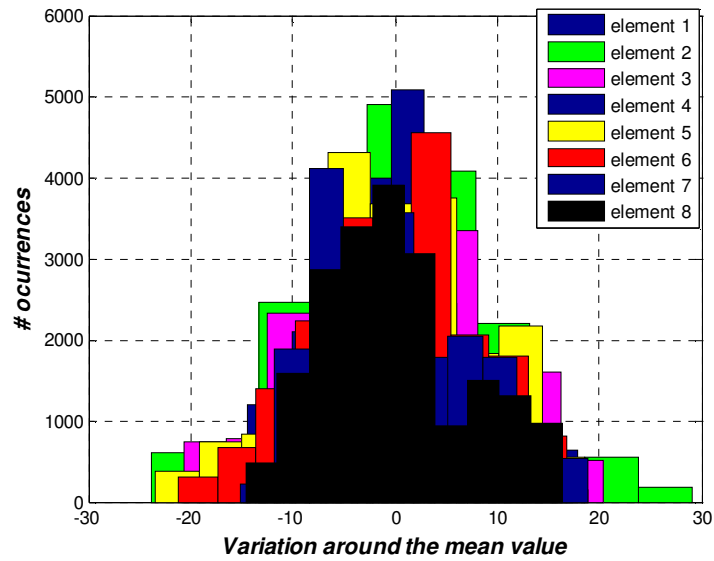


Figure 4.15: Histograms of counters output for the 8 unit elements around their mean value after convergence. Fully randomization. Quasi-Gaussian distributions.

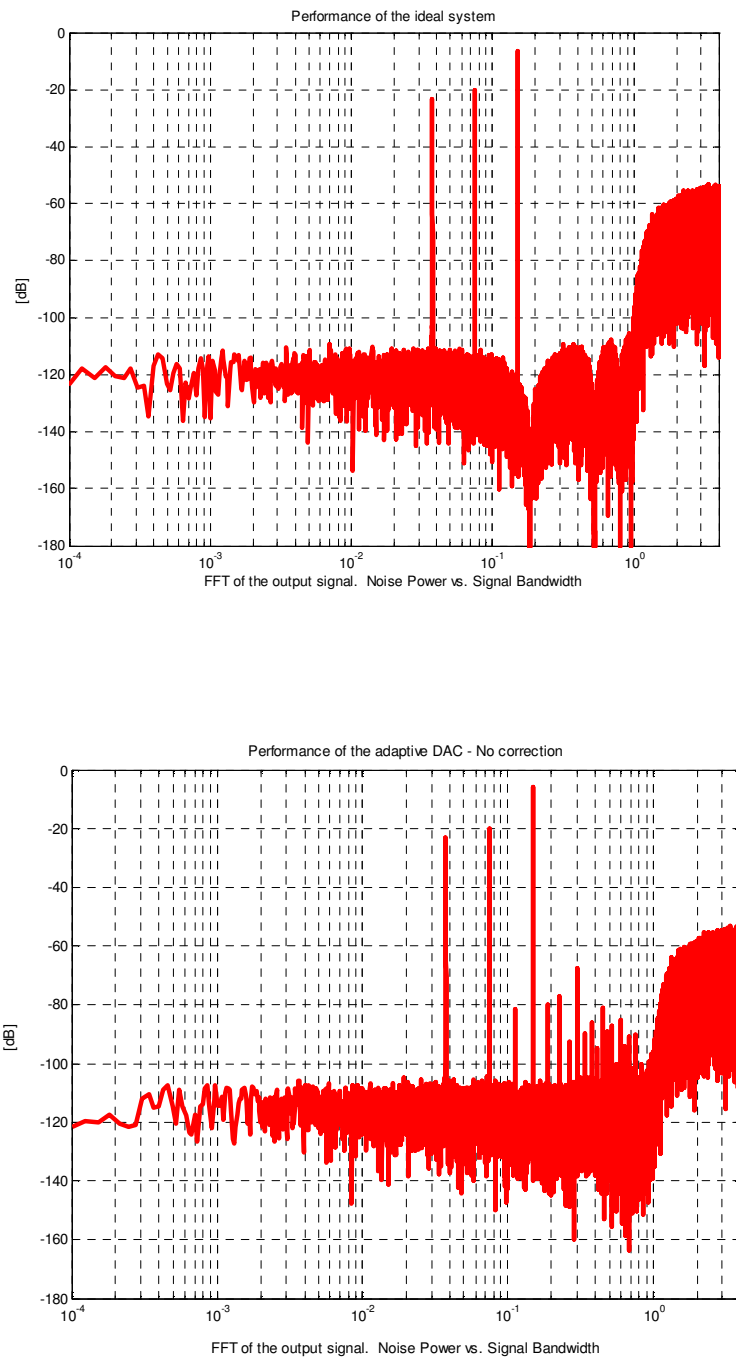


Figure 16: Simulated output spectra.

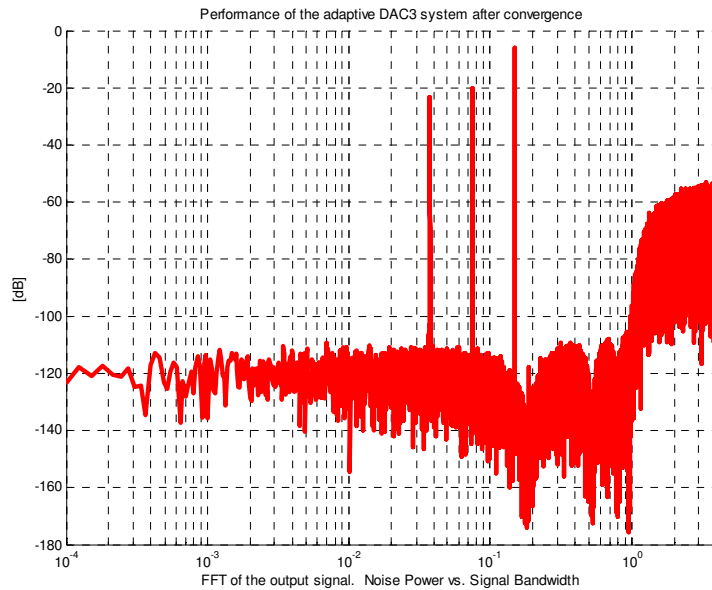


Figure 4.16 (continued): Simulated output spectra, with and without error, and corrected. 2^{20} points FFT for three sinusoidal inputs. *Hanning* window used to minimize *Gibbs* effect. Input frequencies are at very low frequencies compared with the band of interest, in order to observe intermodulation products due to the nonlinear characteristic of the DAC.

4.6 Nonideal Effects

4.6.1 Finite Output Resistance in the Current Sources

Consider the simplified schematic of the DAC of Fig. 4.17. Each half contains a determined number of current sources, *Selected-Left* (S_L) and *Selected-Right* (S_R), and also load resistors (R_L and R_R respectively). The current sources have a parasitic output resistance (R_{CS}) that will be considered equal in all the sources for the sake of simplicity.

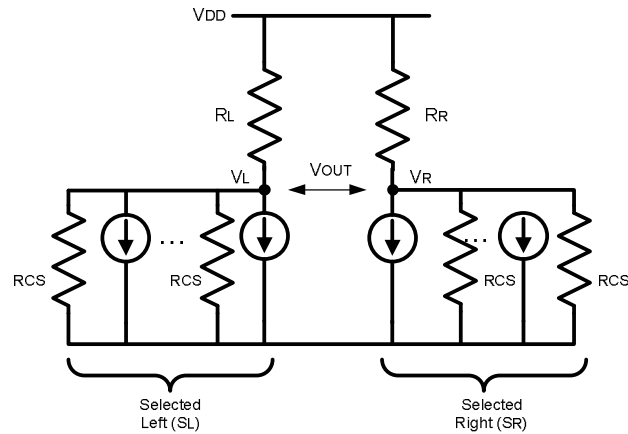


Figure 4.17: Simplified circuit of the DAC

Now, the following equations can be obtained:

$$V_{DD} - R_R \sum_{S_R} i - R_R \sum_{S_R} \left(\frac{V_R}{R_{CS}} \right) = V_R \quad (4.9)$$

$$V_{DD} - R_L \sum_{S_L} i - R_L \sum_{S_L} \left(\frac{V_L}{R_{CS}} \right) = V_L \quad (4.10)$$

Subtracting them, the differential voltage is

$$V_R - V_L = i R_R S_R - i R_L S_L - \left(\frac{V_R S_R}{R_{CS}} \right) R_R - \left(\frac{V_L S_L}{R_{CS}} \right) R_L \quad (4.11)$$

From which:

$$V_R \left(1 + \left(\frac{S_R}{R_{CS}} \right) R_R \right) - V_L \left(1 + \left(\frac{S_L}{R_{CS}} \right) R_L \right) = i R_R S_R - i R_L S_L \quad (4.12)$$

Because the number of unit elements is very small and using direct correspondence between terms, it can be written:

$$\begin{aligned} V_R \left(1 + \left(\frac{S_R}{R_{CS}} \right) R_R \right) &= i R_R S_R \Rightarrow V_R \cong i R_R S_R \left(1 - \left(\frac{S_R}{R_{CS}} \right) R_R \right) \\ V_L \left(1 + \left(\frac{S_L}{R_{CS}} \right) R_L \right) &= i R_L S_L \Rightarrow V_L \cong i R_L S_L \left(1 - \left(\frac{S_L}{R_{CS}} \right) R_L \right) \end{aligned} \quad (4.13)$$

Considering $R_L=R_S=R$, this reduces to

$$V_{diff} \equiv V_R - V_L = i R(S_R - S_L)\{1 - \frac{R}{R_{CS}}(S_R + S_L)\} \quad (4.14)$$

This is completely linear. There exist only a gain variation.

Different values of the parasitic resistor have been simulated, and shown not to be an important issue for the algorithm or for the linearity.

4.6.2 Comparator Noise

Referring to Fig. 4.18, the comparator noise can be modeled as white if a large bandwidth is considered, as is the case for a fast device. Because the noise is not present at the DAC output, it does not have any influence in the dynamic linearity. The noise, having zero mean, will not introduce any problem in the final values obtained. Depending in its value, it could slow down the convergence process. At the same time, the noise is acting as a dithering signal, improving the capabilities of detection of the 1-bit comparator.

A $60\mu\text{V}$ noise has been used in the simulations. With the 8 bit dead zones, the system presented simulated immunity for uniformly distributed noises of up to 1mV .

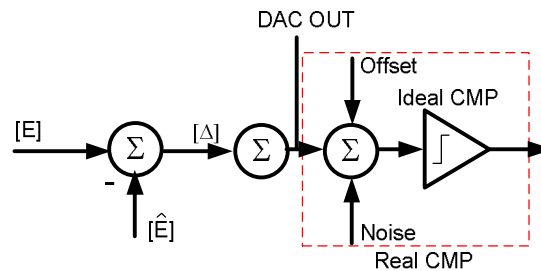


Figure 4.18: The comparator noise acts as a dithering signal.

4.6.3 Comparator Offset and Load Resistors Mismatch

This topic has been discussed previously. Typical simulation values were:

Comparator offset: 4.3 mV.

Resistor mismatch: 0.6 %

4.6.4 Nonlinear Auxiliary DAC (AUX-DAC)

The simulated 10-bit AUX-DAC had a 10-bit linear transfer characteristic. It must be noted that with less linearity the system still converges, but the error in the estimation could be bigger, e.g., with 9 bits of linearity, instead of 1LSB (=1 μ A), perhaps the system will converge with a residual error equal to 2LSBs.

4.6.5 Thermal Noise

Considering now only the thermal noise in the current sources and in the load resistor, the signal-to-noise ration (SNR) can be expressed as:

$$SNR[dB] = 20\log_{10} \left(\frac{2^n R i_{LSB}}{\sqrt{4 K T R B W + R^2 2^n \left(\frac{8}{3}\right) K T B W \sqrt{2k' \left(\frac{W}{L}\right) i_{LSB}}}} \right) \quad (4.15)$$

$$\propto 20\log_{10} \left(\frac{I_{FS}}{\sqrt{B W (K_1 + K_2 I_{FS})}} \right)$$

With:

$R = R_{LOAD}$

$K =$ Boltzmann constant

$T =$ Absolute temperature.

$BW =$ Bandwidth of interest (single pole equivalent)

$k' = \mu C_{ox}$

$i_{LSB} = I_{FS}/2^n$

Fig. 4.19 plots this relation for $C_{LOAD}=10$ pF, $R_{LOAD}=1$ k Ω and $R_{LOAD}=50\Omega$, with $W/L=1$ as a function of the i_{LSB} for a 3-bit converter. It must be noted that the quantization noise would limit the SNR to a 3-bit SNR. With the use of a delta-sigma ($\Delta\Sigma$) modulator this noise will be shaped, and then the i_{LSB} current will now limit the achievable SNR. Figs. 4.20 a) & b) plot this last fact for different BW ($R=50\Omega$, C_L variable) and different I_{FS} .

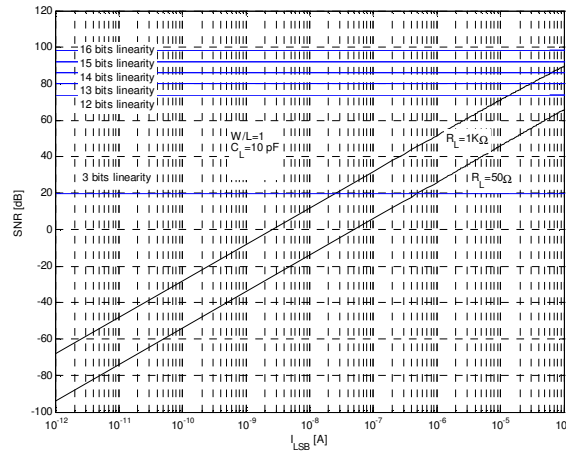


Figure 4.19: SNR as a function of the LSB current.

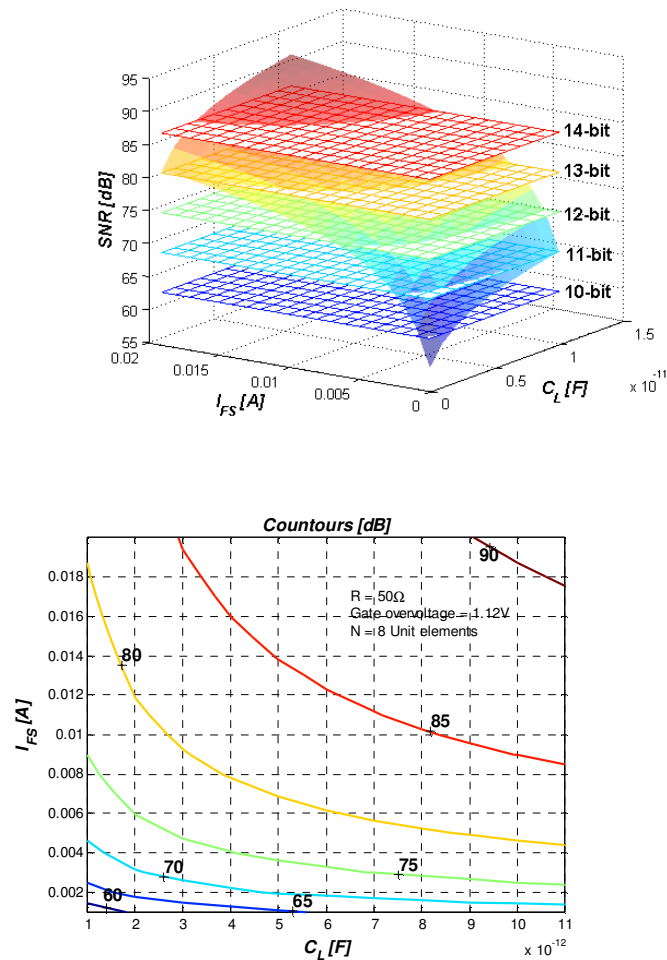


Figure 4.20: a) SNR as a function of the BW and I_{FS} . (Considering only thermal noise). b) Contour plots.

CHAPTER 5. ANALOG AND DIGITAL HARDWARE

This section will deal with the implementation of the converter.

Two main subsections, the analog and the digital hardware implementations, will explain in detail fine points and procedures for each part of the system.

The selected test vehicle of the idea is a 3-bit current-steering DAC, with on-chip 50 Ohms differential poly-resistor load ($25 + 25$), and 20mA full scale current.

The correction loop (Aux DAC, comparator, memories and associated logic) together with the main DAC was implemented in a 0.35 μ m, 2P-4M mixed-mode technology.

The layout uses the guidelines provided in Section 3-1, based on the analysis similar to that of Section 3.2. The topology uses the reduced switching sequence scheme of Section 4-1. The novel latch with feedthrough compensation of Section 3.3.2 was used in the design.

The whole silicon system is schematically depicted in Fig. 5.1. The digital section will process the pseudo-random noise generator used to select one of the 16 different possible middle codes, and also the delta-sigma 3-bit input sequence. The two DACs and the comparator form the analog part of the chip.

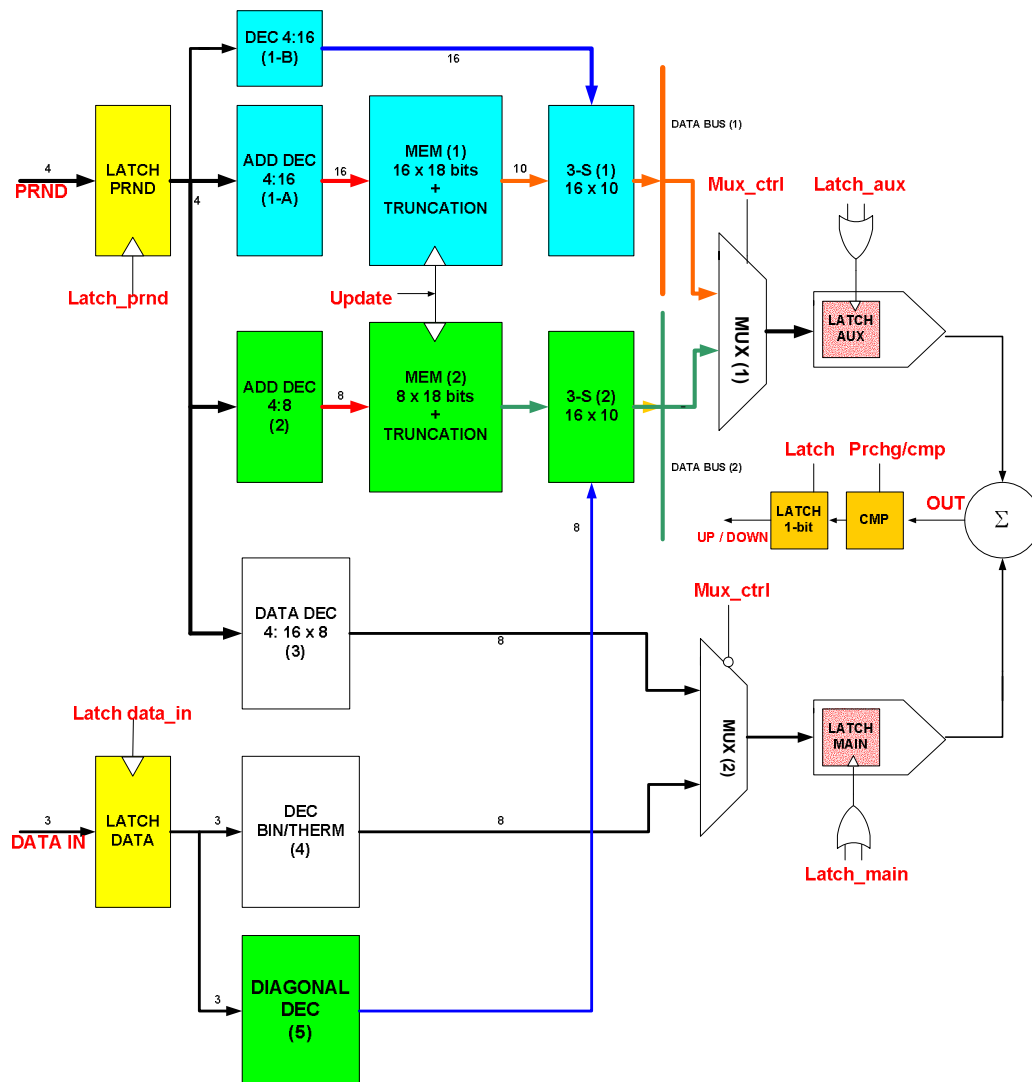
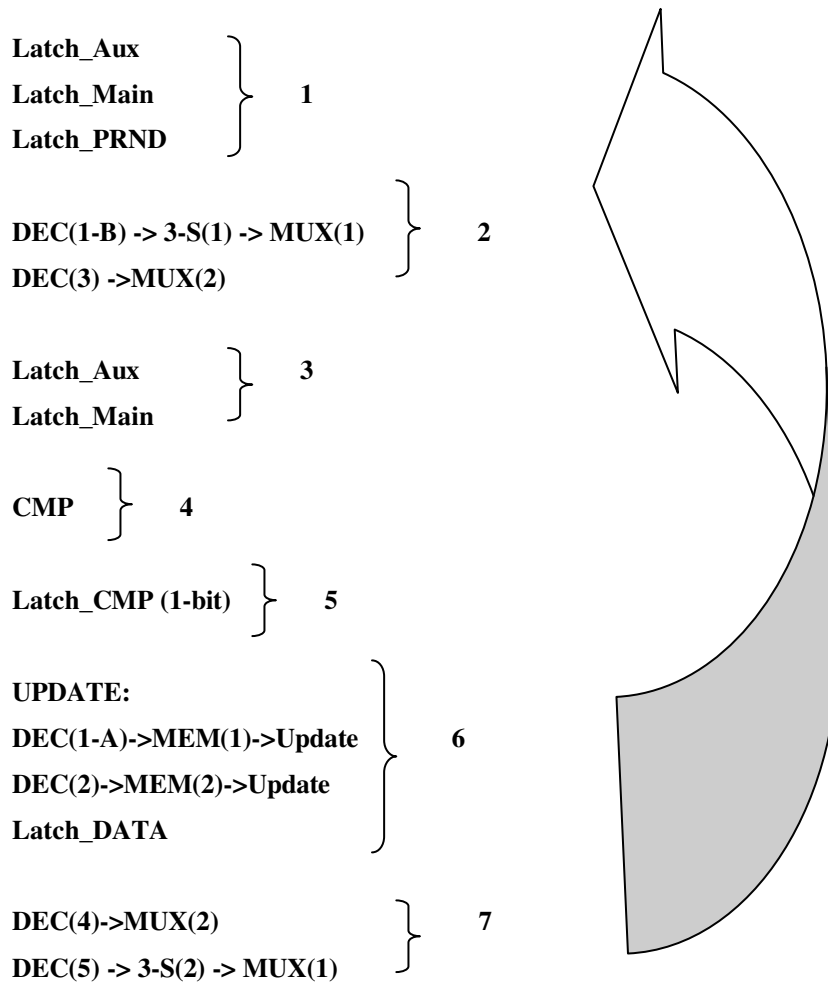


Figure 5.1: Implemented system.

The sequence of events is as follows:



and repeats cyclically. Everything is clock synchronized.

5.1 Analog Section

5.1.1 Comparator Design

The designed comparator is multistage and output-offset compensated [33]. Small signals must be resolved (μV), and then a high amplification factor (1000 or more) should be used in order to overcome the inherent latch offset, whose upper limit was estimated in the order of $10\text{mV}\sim 20\text{mV}$, mainly due to mismatched devices. All the individual offsets are series compensated by means of poly-poly capacitances. Fig. 5.2 shows the schematic of the device.

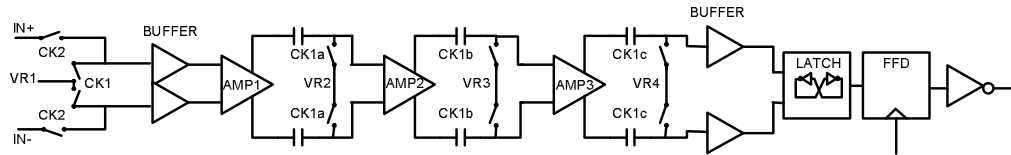


Figure 5.2: Schematic of the comparator

There exists a nonlinear relationship between the gain per stage, the number of stages, and the delay time (speed) in multistage comparators. For this design, a 3-stage was chosen. For a cascade of n single pole (s_p) transfer functions with DC-gain equal to A , it can be shown that the delay introduced (to the 50% of the output swing) is given approximately by:

$$t_d \cong \left[(n-1) + 0.7 \right] / s_p \quad (5.1)$$

The regenerative latch is considered to be fast enough to neglect own delay time.

The output is approximately given by (feed through and charge injection cancelled by proper clocking phases):

$$OUT \cong -A_1 A_2 A_3 IN + \left(\frac{V_{oss3}}{(A_3 + 1) A_2 A_1} \right) \quad (5.2)$$

The two input buffers should accommodate the input common mode voltage coming from the 25 Ω load resistors. The final buffers provided isolation between the regenerative latch and the analog preamplifiers. All the switches are PMOS devices placed in individual wells. Dedicated power lines (switches, analog amplifiers, digital latch and buffer) were used to minimize crosstalk.

For each individual comparator a circuit as that depicted in Fig. 5.3-a) was used. It uses gain enhancement current sources, having an approximate gain:

$$A_v \cong g_{mn} / g_{mp} = \sqrt{\frac{\mu_n (W/L)_n}{\mu_p (W/L)_p} \frac{1}{(1-k)}} \quad (5.3)$$

and an approximate bandwidth given by:

$$BW \cong g_{mn} / C \quad (5.4)$$

where g_{mn} and g_{mp} are the differential pair and the diode-connected PMOS transconductances respectively. C is the capacitive load at the output nodes. The diode connected transistors fix the output common mode voltage, and the PMOS current sources increase the overall gain.

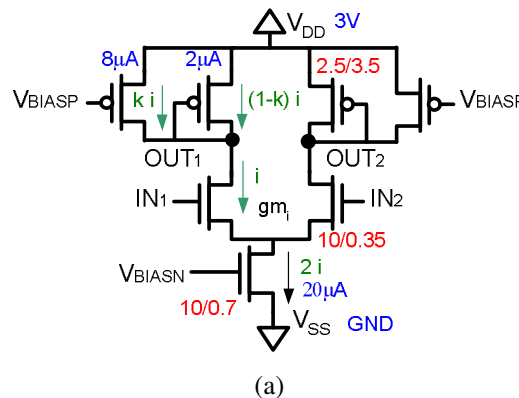
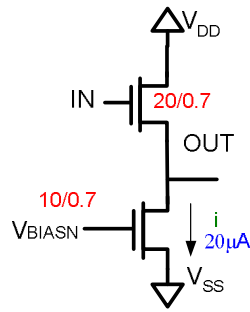
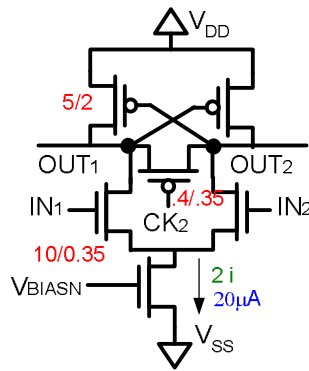


Figure 5.3: a) Gain enhancement analog amplifier



(b)



(c)

Figure 5.3 (continued): b) Buffers; c) Regenerative latch.

Dummy devices, common centroid layout and metal-1 metallization were used to reduce random fluctuations. The distribution of the mismatch was supposed to be Gaussian, and the offset of the latch was estimated using

$$V_{off} \cong \pm 3 \sqrt{\delta(V_{T0})^2 + \delta(V_{T0}')^2} = \pm 3 \sqrt{\frac{A_{VT}^2}{WL} + \frac{A\beta^2 (V_{GS} - V_T)^2}{4WL}}, \quad (5.5)$$

which is based on principles similar to those presented in Chapter 3.

The buffer and the regenerative latch schematics are shown in Fig. 5.3-b) and c) respectively, together with their implemented geometrical values.

Local decoupling capacitances were placed close to each individual amplifier. Double guard rings prevented latch-up and isolated the stages. Digital latches (differentially placed to equalize loading effects) were used to reduce metastability problems. Digital buffering was used to

convey the digital output signal to the rest of the chip. Fig. 5.4 shows the micrograph of the fabricated comparator, with some details.

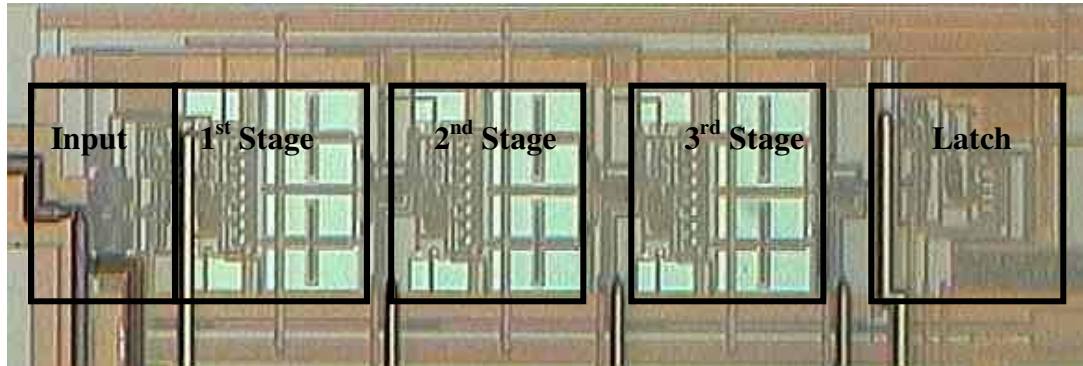


Figure 5.4: Comparator micrograph.

5.1.2 Main DAC

The main DAC was laid out using the considerations presented in Section 3-2 for linear matching and quadratic effects reduction. The latches are those presented in Section 3.3. The switches of the current sources were used in their saturation region, to increase the output resistance. To minimize glitches, they were laid out using cross-coupled common centroid techniques, with metal widths scaled accordingly to convey the unit current value. Considering the small number of unit elements, the parasitic output conductance did not require the use of cascoded devices.

Fig. 5.5 shows the picture of the Main DAC, the associated latches and switches. Equalization of metal-1 with dummy strips, and two rows of dummy devices were used to increase the matching.

Each current source was subdivided in 32 small units (spatial averaging). Metal-2 and vias were used to access the devices.

In order to equalize effects, the reference current was split in four, and injected in each corner by means of diode connected devices. Flipping and same current flow techniques were used to diminish anisotropic effects.

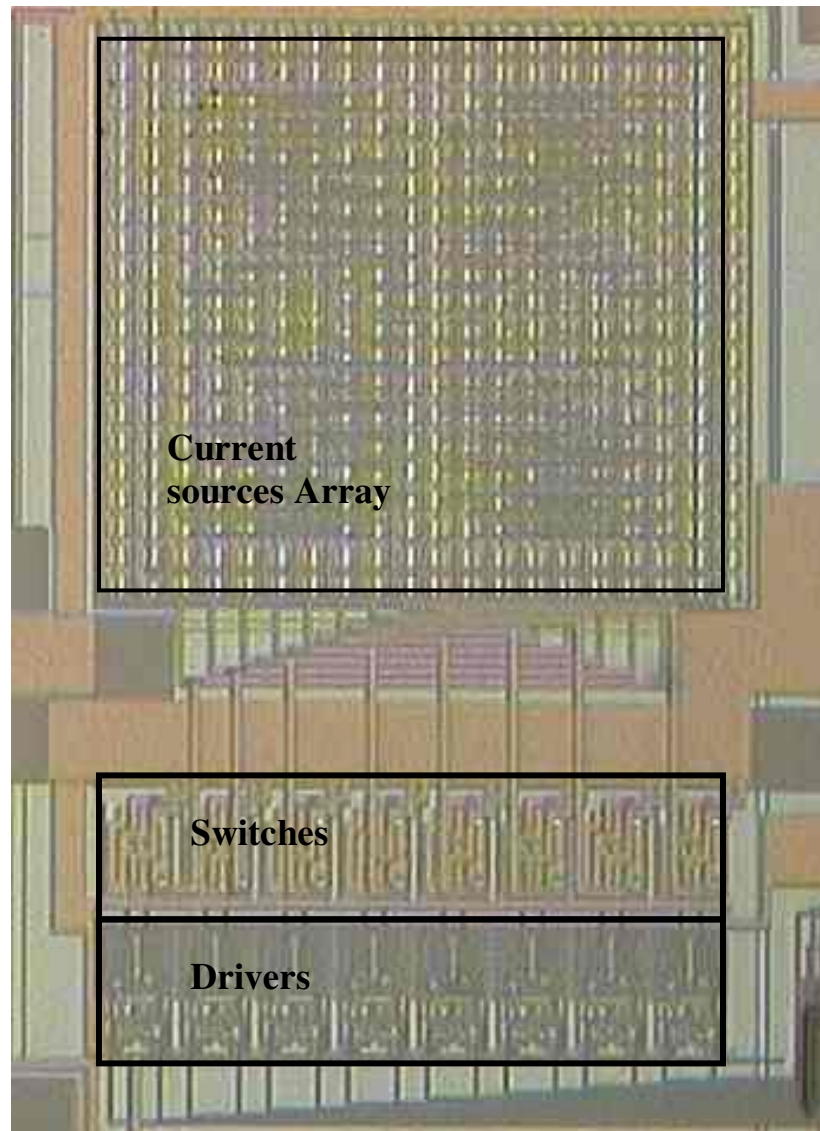


Figure 5.5: Main DAC micrograph.

5.1.3 Auxiliary DAC

The Aux-DAC is a 10-bit linear binary weighted DAC. Its micrograph is shown in Fig. 5.6. No quadratic compensation was used. By design it should have 10 bits of linearity (as the Main-DAC). The unit current sources have cascode devices in order to increase the output impedance, hence making the output code-independent. The same latches as before were employed here.

Because of the calculated small W/L ratio of the unit element, the meander shape layout of Fig. 5.7 was employed. The equivalent circuit is also shown; it must be pointed out that it is similar to the series connection of three equal-sized MOS devices, the top one working in its saturation region, and the others in their linear region. Parasitic diffusion interconnection resistance effects were estimated to be negligible based on the small current handled in each cell.

As before, the switch devices were used also as cascode transistors.

Selecting the supply voltage values of the control signals, the switch devices can remain in their saturation region having at the same time a reduced swing, but with a reduction of the glitch energy. This technique was not employed here.

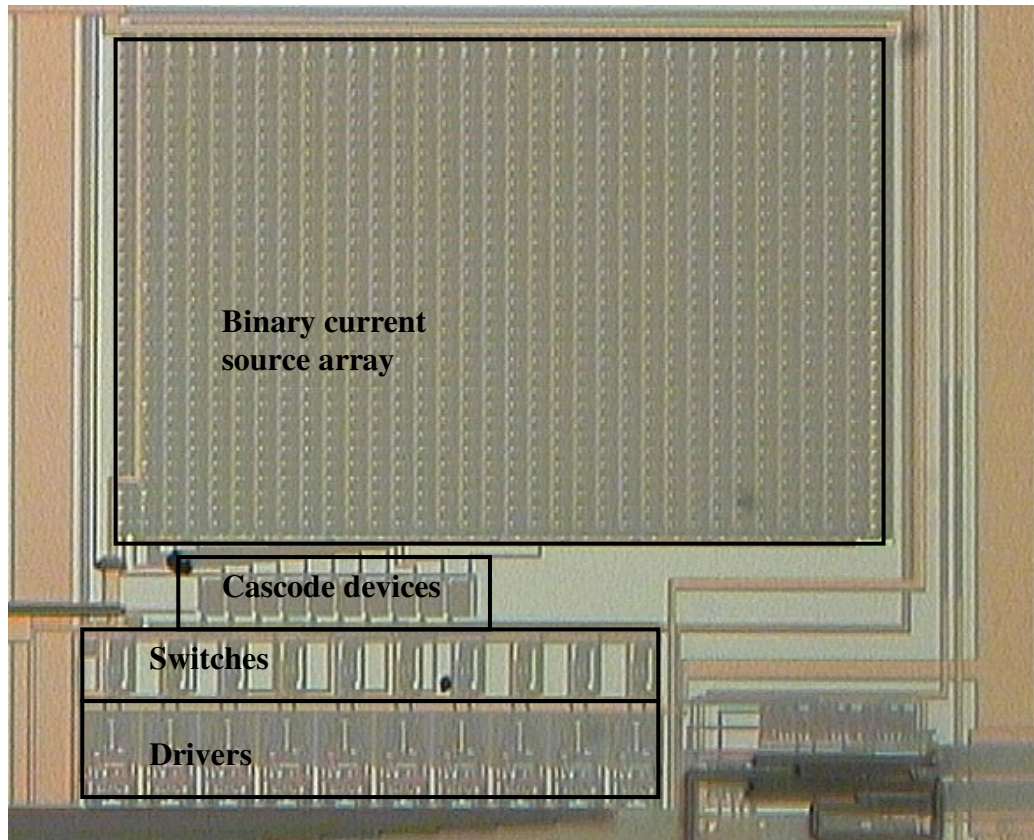


Figure 5.6: Aux- DAC micrograph.

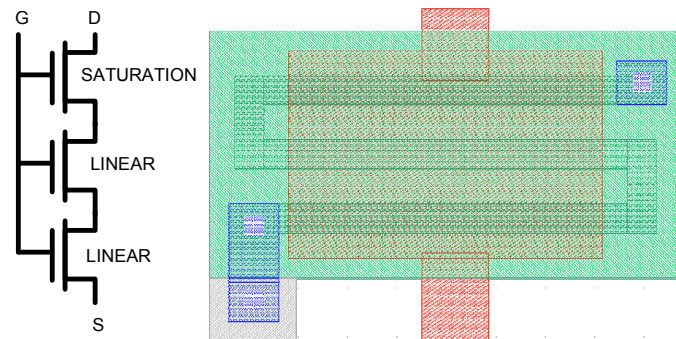


Figure 5.7: Layout of a small (W/L) transistor.

5.2 Digital Section

5.2.1 *General Considerations*

In this section a brief explanation of the digital blocks employed will be given.

Using schematics synthesis, small block layouts were generated and auto-routed. The main connections among them were carried out using full custom methodology.

Decoders were synthesized with traditional methodologies (Karnaugh maps, truth tables, etc. [7, 40])

To avoid antenna effects, long wires were segmented, going up and down in different metal levels.

To reduce parasitic resistance effects, whenever it was possible multiple vias were used.

Dedicated clock and reset lines were buffered across the chip.

The digital section almost enclosed the analog one (which was located in the middle of the IC for matching considerations)

The two banks of memory were implemented using 18-bits up/down counters, controlled by the comparator output.

To reduce limit cycles, as explained in section 3.1, truncation to 10 bits was introduced (the 8 LSBs were discarded)

High level simulations were carried out for each one of the individual blocks, and global mixed-mode simulations were performed to corroborate the functionality of the whole system.

5.2.2 Encoders and Memory

An important point is the update table that was the base for the correction system synthesis. This table can be read knowing which was the first element of the selected pseudorandom sequence; each file represents one of the 32 (16+8) registers in both memory banks. It is noteworthy that because the offset is included in each register, there are only 3 operations: increase, decrease or void.

TABLE V-I

OFFSET	S1	S2	S3	S4	S5	S6	S7	S8
1	S1+S2+S3+S4-S5-S6-S7-S8	2	2	2	2	0	0	0
2	S2+S1+S3+S4-S5-S6-S7-S8	2	2	2	2	0	0	0
3	S3+S2+S1+S4-S5-S6-S7-S8	2	2	2	2	0	0	0
4	S4+S2+S3+S1-S5-S6-S7-S8	2	2	2	2	0	0	0
5	S5+S2+S3+S4-S1-S6-S7-S8	0	2	2	2	2	0	0
6	S6+S2+S3+S4-S5-S1-S7-S8	0	2	2	2	0	2	0
7	S7+S2+S3+S4-S5-S6-S1-S8	0	2	2	2	0	0	2
8	S8+S2+S3+S4-S5-S6-S7-S1	0	2	2	2	0	0	2
9	S5+S6+S7+S8-S1-S2-S3-S4	0	0	0	0	2	2	2
10	S6+S5+S7+S8-S1-S2-S3-S4	0	0	0	0	2	2	2
11	S7+S6+S5+S8-S1-S2-S3-S4	0	0	0	0	2	2	2
12	S8+S6+S7+S5-S1-S2-S3-S4	0	0	0	0	2	2	2
13	S1+S6+S7+S8-S5-S2-S3-S4	2	0	0	0	0	2	2
14	S2+S6+S7+S8-S1-S5-S3-S4	0	2	0	0	0	2	2
15	S3+S6+S7+S8-S1-S2-S5-S4	0	0	2	0	0	2	2
16	S4+S6+S7+S8-S1-S2-S3-S5	0	0	0	2	0	2	2
17	S1+S2+S3+S4+S5+S6+S7+S8	2	2	2	2	2	2	2
18	S1+S2+S3+S4+S5+S6+S7-S8	2	2	2	2	2	2	0
19	S1+S2+S3+S4+S5+S6-S7-S8	2	2	2	2	2	0	0
20	S1+S2+S3+S4+S5-S6-S7-S8	2	2	2	2	0	0	0
21	S1+S2+S3+S4-S5-S6-S7-S8	2	2	2	2	0	0	0
22	S1+S2+S3-S4-S5-S6-S7-S8	2	2	2	0	0	0	0
23	S1+S2-S3-S4-S5-S6-S7-S8	2	2	0	0	0	0	0
24	S1-S2-S3-S4-S5-S6-S7-S8	2	0	0	0	0	0	0

5.3 CHIP

Fig. 5.8 shows the chip micrograph. Testing points were introduced. The active area is 2mm x 1mm; it can be reduced.

Digital Pads contain clamping diodes to VDD and VSS to protect circuitry against ESD.

The digital and the analog section are separated using a well connected to a quiet supply.

Metal shielding was used to prevent crosstalk and coupling of digital noise into the analog components and paths.

Dedicated power rails for digital and analog circuits, using different pads, were constructed using the parallel connection (using multiple vias) of the 4 metal layers available in the technology.

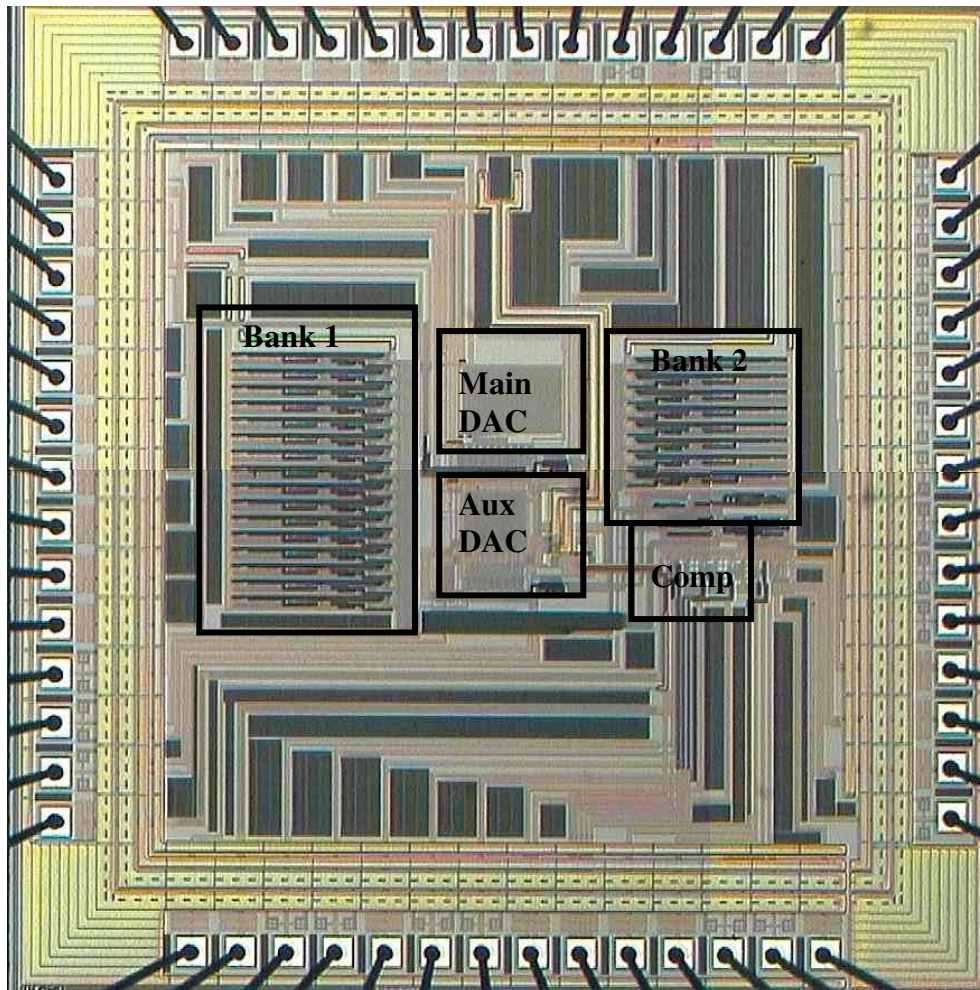


Figure 5.8: Chip Micrograph

CHAPTER 6. TEST SETUP AND EXPERIMENTAL RESULTS

This chapter will deal with the measurements setup and the experimental results of the fabricated prototype.

To obtain the delta-sigma sequence (3-bit) and the 4-bit pseudo random generation, an Arbitrary Wave Generator (AWG) and a Field Programmable Gate Array (FPGA) were employed respectively. Adaptation of the digital CMOS (5V) AWG output signals to the LVCMOS (3.3V) required voltage value was accomplished using special buffers (PODs) together with resistive voltage dividers. Data was collected with a high speed digital scope, with low-frequency high-resolution capabilities (13+ bits), and then post processed using Matlab.

6.1 Test Board Design

The main board was implemented using a 4-layer technology, as depicted in Fig. 6.1. Analog and digital signals were laid out in different planes, and a dedicated layer was used as (split) ground plane.

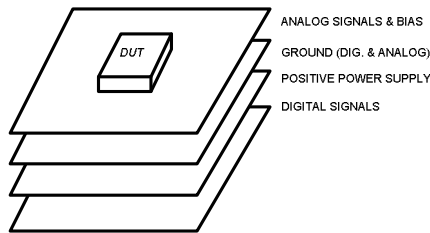


Figure 6.1: Board design.

A 9V battery was used as the reference generator, and buffered voltage dividers provided the different bias points. Decoupling capacitances (0.1uF//1uF) were located close to the chip, and electrolytic capacitors (10uF) were located close to the power supply inputs.

The board has corresponding switches for global reset and for freezing the acquired coefficients.

The chip was mounted in an LCC (leadless) socket; LCC was selected in order to reduce parasitic capacitances.

Fig. 6.2 shows the picture of the test setup.

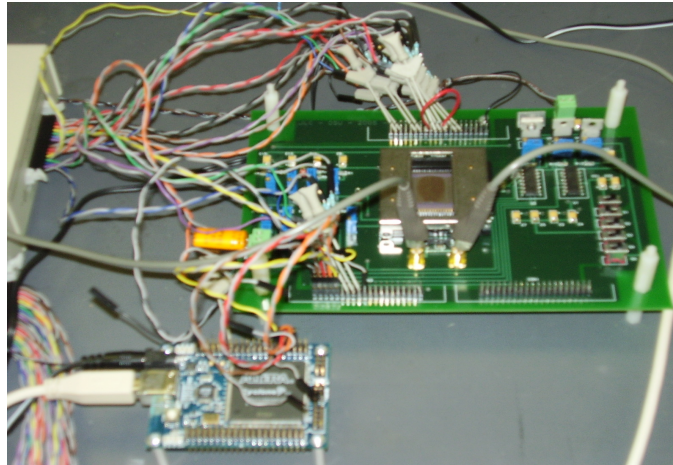


Figure 6.2: Test setup

6.2 Experimental Results

First of all, in order to estimate the errors, a sequence that provided return to zero was forced; a slow ramp was selected (Fig. 6.3), because then all the codes will be present at low speed, minimizing the dynamic errors and allowing enough convergence time before performing the comparisons.



Figure 6.3: Low speed ramp. The two complementary signals and their difference.

After that, a second order delta-sigma sequence was introduced. It has $OSR > 500$ and a $-2dB_{FS}$ amplitude. Fig. 6.4 is the analog output of the system

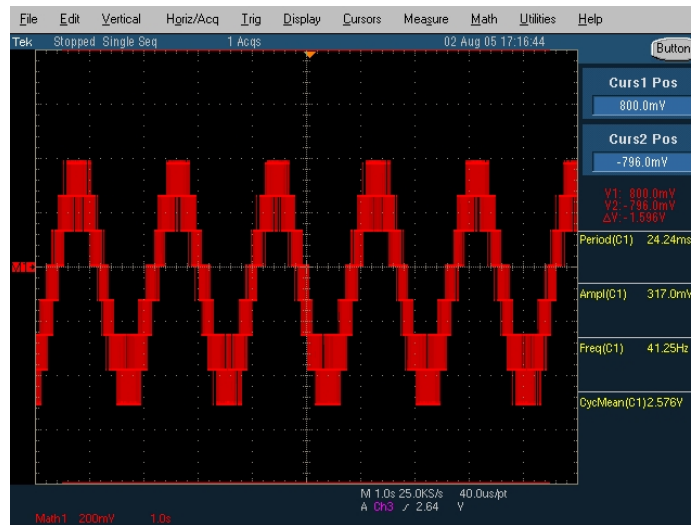


Figure 6.4: Analog differential output for low speed, $-2dB_{FS}$ sine signal.

It was observed that the feedthrough compensation of the latches worked properly: small differential output glitches (mV order) were observed in the fast transitions (ns order)

The correction provided a low-frequency spurious free dynamic range (SFDR) of approximately 83dB (close to 14 bits), as Fig. 6.5 shows. It was measured an average increase of 5dB (roughly speaking, an extra bit) when compared with the uncorrected system.

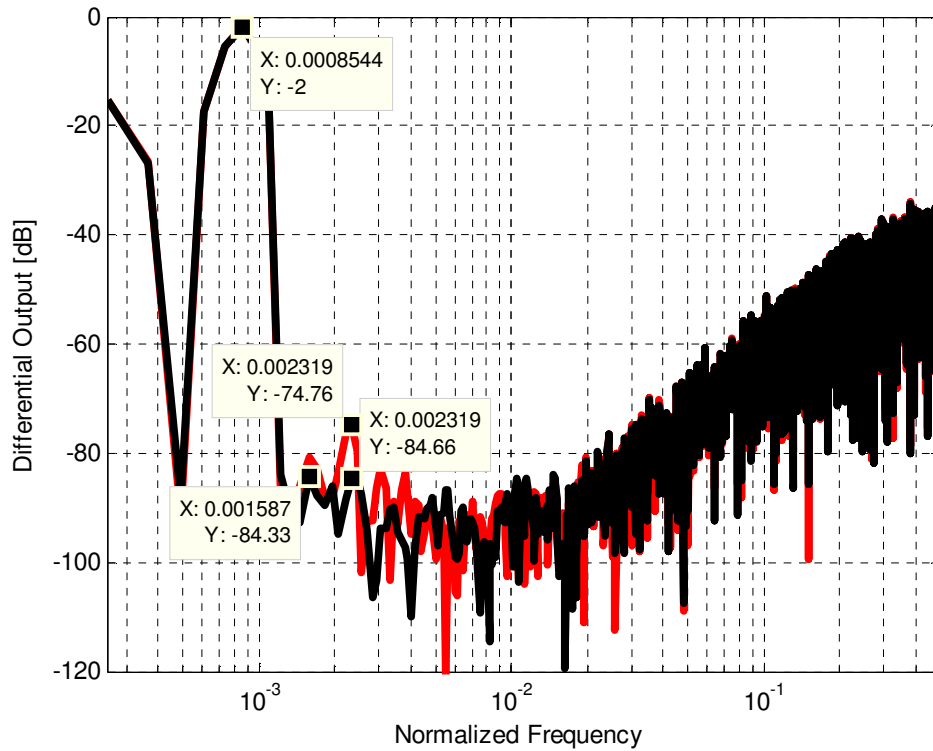


Figure 6.5: Output spectrum. -2dB_{FS} input. $\text{OSR} > 500$. Clock frequency = 100kHz.

To be noted is that:

- 1) The original linearity was good (~ 12 bits without correction), showing that the proposed layout technique was also functional
- 2) The Aux-DAC was not in the originally specified linearity; its estimated linearity is about 9-bits, reason why the final corrected output is between ± 2 LSB of the Aux-DAC range.

Fig. 6.6 shows the uncorrected system response with the OSR kept constant, and increasing the frequency. Dynamic mismatch appears, and it is believed to be due to mismatch in the digital paths, causing different transition instants for the current sources. Also there is present some dynamic inter-symbol interference (ISI), observed in the bends of the ideally flat characteristics.

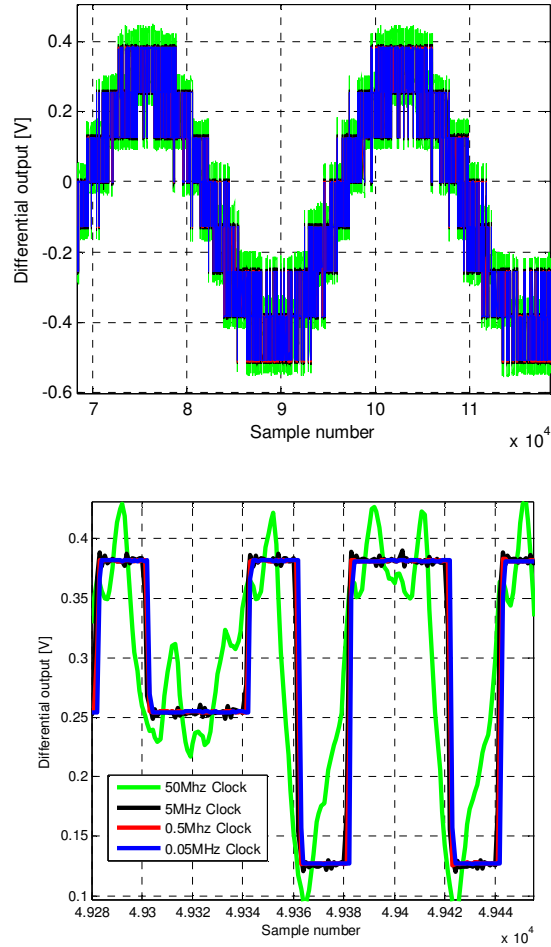


Figure 6.6: OSR constant. Clock frequency is: 50kHz, 500kHz, 5MHz and 50Mhz

An interesting point is that the correction worsens the dynamic behavior of the system at high frequencies; a plausible explanation is that more current sources are switched at the same time. The transition point can be observed in Fig. 6.8 to be around 3MHz. The analog correction then presents an attractive advantage when this fact is taking into account.

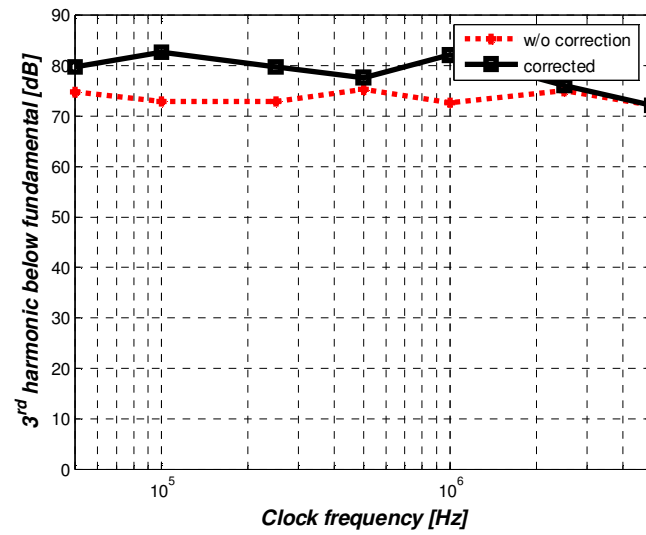
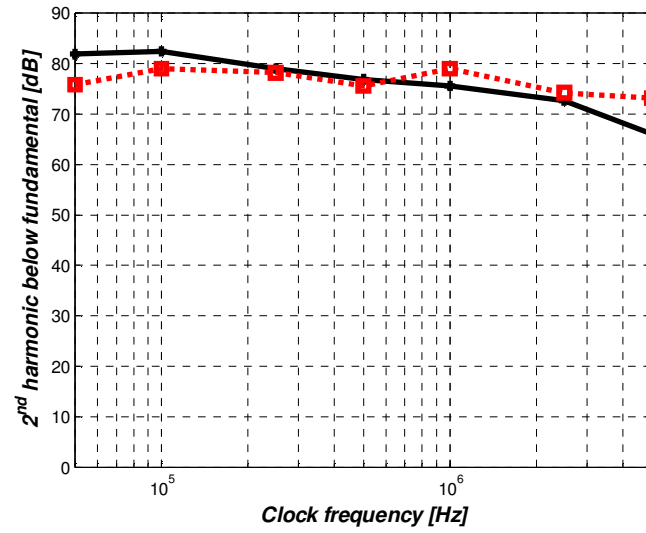


Figure 6.7: 2nd and 3rd harmonic tones compared to the fundamental (in dB)

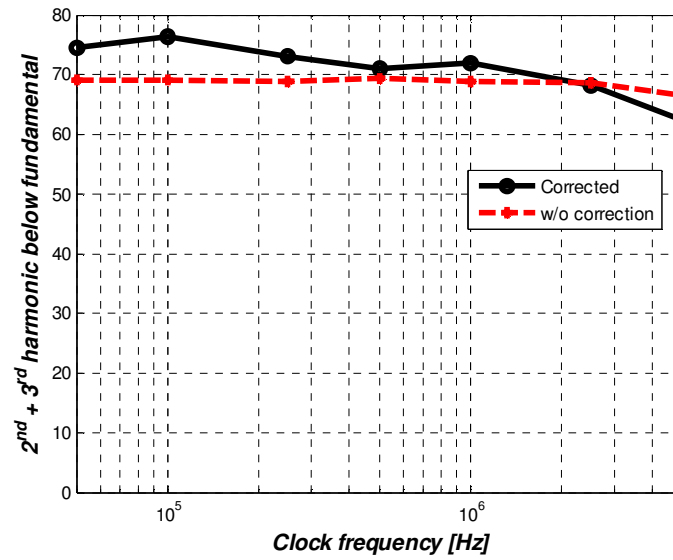


Figure 6.8: THD Estimation

Estimating the THD with the addition of the second and the third harmonic, Fig. 6.8 shows the improvement of using the proposed correction scheme.

CHAPTER 7. CONCLUSIONS

7.1 Conclusions

In this dissertation, the following topics associated with the linear performance in digital-to-analog conversion were studied in detail:

- The tradeoffs of increasing the linearity versus circuit complexity were described.
- Three different ways to overcome linearity issues related with imperfect components were presented. They achieve this considering the problem from different perspectives: circuit oriented (different topologies for current sources and latches), architectural (requantization, stochastic approach and online correction) and construction (layout techniques). The ideas herein proposed can significantly relax the requirements of the analog devices used in this type of converters.
- A prototype chip combining some of the described techniques was designed and fabricated in a conventional CMOS technology. Although the test results show basic functionality and higher linearity, its final accuracy is limited by the high noise present at the analog-to-digital interface between the analog output and the correlation engines.

7.2 Future Work

- Some of the novel ideas about stochastic analog-to-digital and digital-to-analog conversion need to be studied and implemented at the circuit level.
- Different switching sequences could be used to test for convergence speed and accuracy in the digitally corrected DAC different topologies. In addition, a new prototype using switched-capacitor techniques should be tried, in order to obtain less sensitivity to output switching noise in the correlation processes.
- New ways of overcoming dynamic mismatches are the next challenge.

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