A Two-Step Incremental Analog-to-Digital Converter

C.-H. Chen, Y. Zhang, Y. Jung, T. He, J. L. Ceballos and G. C. Temes

A new incremental ADC is proposed which extends the order of a conventional incremental ADC from *N* to (2*N*-1) by way of a two-step operation. For a given conversion time, the duration of each step can be optimized. For an *N*th-order IADC, the performance is equivalent to that of a (2*N*-1)-order converter. However, it only needs the same circuitry as the *N*th-order one. The new IADC is hence more accurate, and also much more power-efficient than the conventional ones.

Introduction: Incremental ADCs (IADCs) are useful for the high-accuracy conversion of signals at DC or narrow-band [1] [2]. To enhance the accuracy within the same conversion time, a higher-order modulator can be employed. Increasing the order, however, requires more op-amps, and hence more power. Also, high-order modulators are more prone to instability, and have more limited overloaded range. In this paper, the trade-off between the order and oversampling ratio (OSR) of an IADC is first discussed. Then, we propose an IADC with a two-step operation. All discussions will be specific to N = 2, but can easily be generalized to arbitrary values of *N*. The circuit functions as a second-order IADC (IADC2) during the first step. It is then reconfigured into a first-order IADC (IADC1) during the second step. The outputs of the two steps are combined. The performance of the two-step IADC is equivalent to a third-order IADC (IADC3), with the same circuitry as that of an IADC2. Assuming the same conversion time, the proposed ADC has a much better power efficiency.

Trade-Offs in Incremental ADCs: Fig. 1 shows a second-order incremental ADC with a feed-forward modulator, and its timing diagram. The oversampling ratio ($OSR = M$) is defined as the number of clock periods between two adjacent reset pulses. In a feed-forward modulator the last integrator's output W_2 equals the residue (error) voltage, and it is hence bounded by the range of the internal quantizer's error E. With a multi-level quantizer, W_2 is within the range $V_{FS}/(nLev-1)$, where V_{FS} is the full scale range and $nLev$ is the number of levels. The equivalent quantization error of the IADC2 (E_{IADC2}) and the effective number of bits ($ENOBs$) are given by eqs. (1) and (2):

$$E_{IADC2} = \frac{V_{FS}}{nLev-1}\frac{2}{M\cdot(M+1)} \tag{1}$$

$$ENOB = log_2\left(\frac{V_{FS}}{E_{IADC}}\right) \approx log_2(nLev-1) + 2\cdot log_2 M - 1 \tag{2}$$

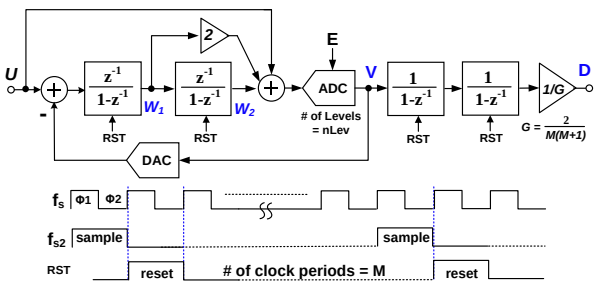

Fig. 1 *A second-order incremental ADC and its timing diagram.*

To achieve higher accuracy, either higher-order modulation or larger OSR can be considered. Fig. 2 shows the calculated SQNR versus OSR for 1-bit modulators, from first to fifth-order IADCs. Generally, increasing the order from *N* to (2*N* - 1) is much more effective than doubling the OSR to enhance the SQNR. However, higher-order modulators are less stable, and have narrower non-overload range.

The Proposed Two-Step Incremental ADC: Fig. 3 shows the proposed IADC and its timing diagram for two-step operation. During the first step of M_1 clock periods, it performs the same input sampling and quantization as the IADC2 of Fig. 1, with the feedforward coefficient set to a_1=2. This generates the residue voltage

$$W_2[M_1] = \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} U[i] - \sum_{k=1}^{M_1-1}\sum_{i=1}^{k-1} D_1[i] \tag{3}$$

(Here, and in the following, a reference voltage of 1 V is assumed for simplicity.) Next, the circuit is reconfigured to function as a first-order IADC during the second step of the quantization, as shown on Fig. 4. The second integrator now acts as an input sample-and-hold stage with an output $W_2[M_1]$. The first integrator samples the outputs of the second integrator and the feedback DAC for M_2 clock periods. At the end of this second step, the first integrator's output is given by

$$W_1[M_1+M_2] = (M_2-1)\cdot W_2[M_1] - \sum_{j=1}^{M_2-1} D_2[j] \tag{4}$$

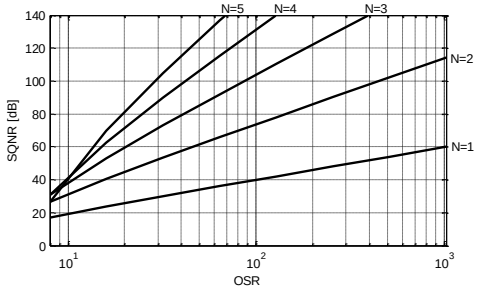

Fig. 2 *SNDR vs. OSR for an IADC with a one-bit quantizer.*

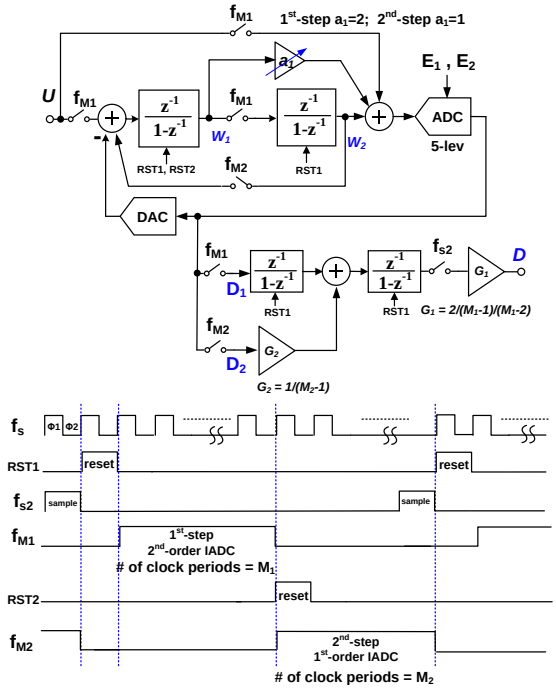

Fig. 3 *The proposed two-step incremental ADC and its control timing.*

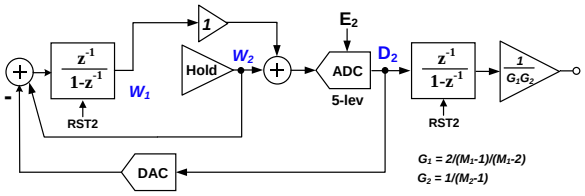

Fig. 4 *Equivalent circuit during the second step. Now a_1 = 1 is set. During the first step, the circuit of Fig.1 is used.*

Combining (3) and (4), the digital estimate of the average $\tilde{U}$ of the input is obtained:

$$\tilde{U} \approx \frac{2}{(M_1-1)(M_1-2)}\left[\sum_{k=1}^{M_2-1}\sum_{i=1}^{k-1} D_1[i] - \frac{1}{M_2-1}\sum_{j=1}^{M_2-1} D_2[j]\right] \tag{5}$$

The modulator insures $W_1 < \frac{V_{FS}}{nLev-1}$, and hence the quantization error E_{ADC} and $ENOB$ of the two-step ADC can be estimated from

$$E_{ADC} \leq \frac{2 \cdot V_{FS}/(nLev-1)}{(M_1-1)((M_1-2)(M_2-1)}; \;\; ENOB \approx log_2(\frac{nLev}{2} \cdot M_1^2 \cdot M_2) \qquad (6)$$

The re-configuration between the two steps can be easily implemented by multiplexing the two integrators with the timing control shown in Fig. 3. The total OSR is divided into two terms M_1 and M_2 ($M_1 + M_2 = M$). Selecting $M_1 = 2M/3$ and $M_2 = M/3$, the ENOB of (6) can be optimized to a value

$$ENOB_{opt} \approx log_2(nLev - 1) + 3 \cdot log_2 M - 3.8 \qquad (7)$$

For the same conversion time, a comparison of eqs. (2) and (7) shows that the two-step IDC's optimal ENOB is larger by $log_2 M - 2.8$ than that of an IADC2. The difference is positive for $M > 7$. Applying the two-step scheme to an *N*th order IADC, during the second step it is reconfigured as a (*N*-1)th order IADC, and achieves a (2*N* -1)th-order modulation. For general *N*, the optimum partition of conversion time is $M_1/M_2 = N/(N-1)$. A two-step IADC scheme was published earlier [3], but it needed an extra op-amp to perform sample-hold operation, and it used a 1st-order algorithmic ADC during the first step.

Simulation Results: The proposed two-step IADC was simulated for a 40 Hz signal bandwith, and with *M* = OSR = 96. A five-level quantizer was used. The optimal selection of M_1 and M_2 was then M_1 = 64 and M_2 = 32. The SQNR versus M_1 is shown on Fig. 5, confirming this choice. Fig. 6 shows the simulated PSD with a -3dBFS signal amplitude. The SQNR is 103 dB. With the same circuitry and OSR, the IADC2 of Fig. 1 results in 83 dB. The improvement is consistent with the increased ENOB of (7). The conventional third-order IADC gives SQNR = 103 dB. The proposed two-step second-order IADC is thus equivalent to a third-order IADC in performance. However, the required analog circuitry is same as for the IADC2. It only needs some simple additional digital circuits to perform the timing control.

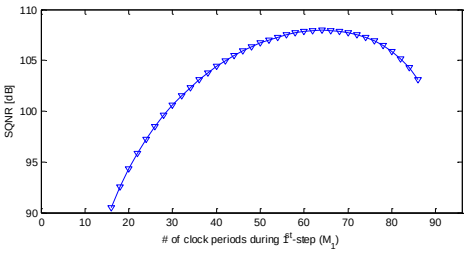

Fig. 5 *SQNR vs. M_1 for the two-step IADC. The total OSR is 96.*

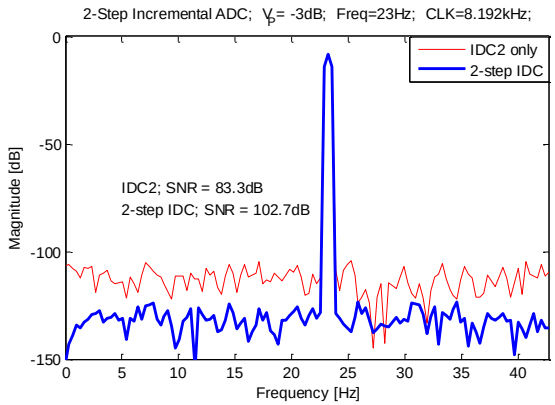

Fig. 6 *Simulated power spectral densities with a -3 dBFS signal.*

Conclusions: A two-step IADC is proposed to perform residue quantization. It functions as a IADC2 during the first step, and it is re-configured as a IADC1 during the second step. Its performance is equivalent to that of a third-order IADC, but it needs the same circuitry as a second-order one (plus some simple timing control). It is therefore much more power-efficient for high-accuracy data conversion.

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References

1 J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental ΔΣ converters," *IEEE Trans. Circuits Syst. I*, vol. **51**, pp. 678–690, Apr. 2004

2 C.-H. Chen, J. Crop, J. Chae, P. Chiang and G. C. Temes, "A 12-bit 7μW/channel 1kHz/channel incremental ADC for biosensor interface circuits," IEEE Int. Symp. on Circuits and Systems, 2012

3 G. Mulliken, F. Adil, G. Cauwenberghs, and R. Genov, "Delta–sigma algorithmic analog-to-digital conversion," IEEE Int. Symp. on Circuits and System (ISCAS), 2002.