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David J. Allstot

A novel frequency compensation method facilitates the design of multi-stage operational amplifiers. High-gain, wide-bandwidth, low-power, fast-slewing, fast-settling, and robust manufacturing are achieved without the use of Nested Miller or Nested G_m -C compensation techniques.

In this thesis, Miller compensation and pole-splitting behavior are examined for multi-stage operational amplifiers and it is shown that only n-2 frequency compensation networks are required to stabilize an n-stage operational amplifier. Moreover, these compensation circuits are simple local networks around internal inverting gain stages. Consequently, since no compensation networks are connected directly to the output node of the n-stage operational amplifier, high-performance and low power dissipation are achieved. For high dynamic range applications, a G_m feed-forward technique is used to independently reduce input noise and increase speed using smaller compensation capacitances. A low-voltage process-tracking compensation technique is also incorporated to maximize yields over process, voltage, and temperature variations.

Design of High-Performance Operational Amplifiers using an Embedded Compensation Technique.

by

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Design of High Performance Operational Amplifiers Using an Embedded Compensation Technique

Chapter 1. Introduction

According to Moore's Law (1965), the number of devices on a single chip and hence, the potential computing power doubles each year. This trend has continued for over 30 years and is still remarkably accurate. The desire for greater computing power has required new technology with scaled device feature sizes so that ever more devices can be packed onto a silicon die. As a result, it is necessary to scale down other parameters including power supply voltages and power consumption.

Associated with this trend in technology, new designs of circuits and systems architectures are needed, and the demands for higher accuracy, lower power consumption, and higher dynamic range are of prime importance. These performance criteria have led to merger of analog and digital electronics on a single chip.

New demands are presented for low-voltage high performance operational amplifiers which are the building blocks of analog signal processing. Conventional operational amplifiers can no longer meet all of the requirements associated with modern low-voltage technology demands. We have already encountered some major gain and speed trade-off in conventional operational amplifiers. Apart from that, some conventional high performance operational amplifiers are no longer operational in low-voltage environments. The limitations for desired performance appear by having at most two stages for simple frequency compensation. However, additional stages are now necessary to satisfy low-voltage high performance requirements.

In addition to requirements for new design topologies are demands for frequency compensation techniques that are suitable for this design context. Compensation techniques must not only stabilize the amplifier, but enhance the amplifier performance.

This implies that the conventional wisdom applied for two-stage operational amplifier frequency compensation techniques and modeling must be re-examined and studied in detail for multi-stage operational amplifiers.

Analog circuits often serve as both front-end and back-end parts of signal processing chains. The desire to obtain a high level of accuracy and dynamic range in mixed-signal applications makes the design for operational amplifiers more challenging.

1.1 Low-Voltage and Low-Power

There are several reasons to move towards low-voltage and low-power designs. The first is that battery powered portable personal computing systems are becoming popular. It is important to boost minimum battery lifetimes in equipment such as notebook computers and cellular phones; minimum power consumption and minimum power supply voltages are also of importance.

The second reason lies in the desire to achieve a high packing density of digital and analog circuits on a single chip, due to shrinking integrated circuit feature sizes. The smaller dimensions lead to an increase in the strength of the electric field on the chip to a level which could destroy the components on the chip. Recent CMOS processes are reported to have gate oxide breakdown voltages of 3 volts or less [1]. Lowering the power supply voltage below this level is a method of avoiding these breakdowns.

A third reason is related to the limited amount of power that the silicon substrate can dissipate without overheating. As the density of integrated circuit components increases the power consumption increases as well, resulting in overheating of the silicon chip. Designing for efficient low-power circuits is essential to keep total power dissipation under control and to maintain high long-term reliability.

1.2 Low-Power Frequency Compensation

When unity-gain feedback is applied to a marginally stable amplifier, chances are that the circuit will fall into spontaneous oscillations [1]. Frequency compensation specifications are required for robust stability by shaping the frequency response in such a way that the amplifier is stable under a large range of conditions. The large number of variables involved in obtaining a stable amplifier led designers to limit operational amplifiers to two gain stages, to keep the manufacturing process, temperature, and voltage variations effects on performance minimal.

Most popular among several frequency compensation techniques used for two-stage operational amplifiers is the RC pole-splitting pole-zero cancellation compensation network shown in Figure 1.1 [2]. This technique is of particular of interest for two

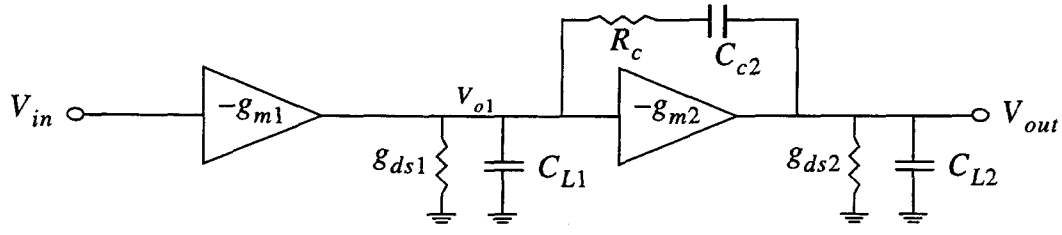

Figure 1.1. Small-signal representation of a two-stage amplifier with RC compensation network.

reasons. First, the capacitor provides pole splitting between the two stages and the resistor provides a zero in the left-half plane (LHP) to cancel the non-dominant pole. In addition, the resistor also blocks the positive feed-forward effect through the Miller capacitor and the corresponding right-half plane zero (RHP). Second, the resistor can be employed using either poly resistors or MOS devices operated in the non-saturation region where, in both cases, the resistor value can be designed to track process, voltage, and temperature variations to ensure proper pole-zero cancellation.

In a multi-stage designs, the same compensation topology can be used to meet the stability criteria. The basic requirement is to compensate the amplifier in such a way that it exhibits a single pole response until slightly above the unity-gain frequency. Successful frequency compensation is measured in terms of open-loop gain and phase margin specifications.

It has always been assumed that poles in an uncompensated operational amplifier are given by the RC time constants at nodes in the signal path. To the contrary, in multi-stage operational amplifiers, including the two-stage, the poles are no longer directly related to the RC time constants of nodes in the signal path due to the parasitic gate-to-drain capacitors coupling the cascaded gain stages.

It can be shown that in an n-stage uncompensated operational amplifier the poles of each stage in the signal path are automatically cancelled by LHP zeros of the preceding stage. These zeros are formed due to the parasitic gate-to-drain coupling capacitors between the stages (not including the RHP zeros by the same capacitors). The transfer function of the overall operational amplifier still exhibits n-poles in an n-stage system. However, the poles associated with the overall transfer function are "referred" back to the input stage and are no longer related to the RC time constant of each node in the signal path. Due to this argument, it can be shown that only n-2 compensation networks are required to obtain a stable response in an n-stage operational amplifier.

Currently, there exist multi-stage operational amplifiers where some type of nested compensation scheme is used such as the Nested Miller Compensation (NMC) technique [1][3]. The block diagram associated with NMC is shown in Figure 1.2. The structure starts off with an input stage and for every additional stage, a Miller capacitor is connected between its input and the output node, closing a wider negative feedback loop as shown. The drawback with NMC is that it uses only capacitors for pole splitting which introduce RHP zeros (positive feed-forward); hence, the maximum achievable bandwidth is reduced significantly. Also, the multiple compensation capacitors connected at the output node increase power consumption and reduce bandwidth, settling accuracy and slew-rate. Moreover, the stability criteria associated with this scheme force bandwidths of adjacent stages to be ratioed by two to avoid formation of complex conjugate pair poles and RHP zeros within the bandwidth.

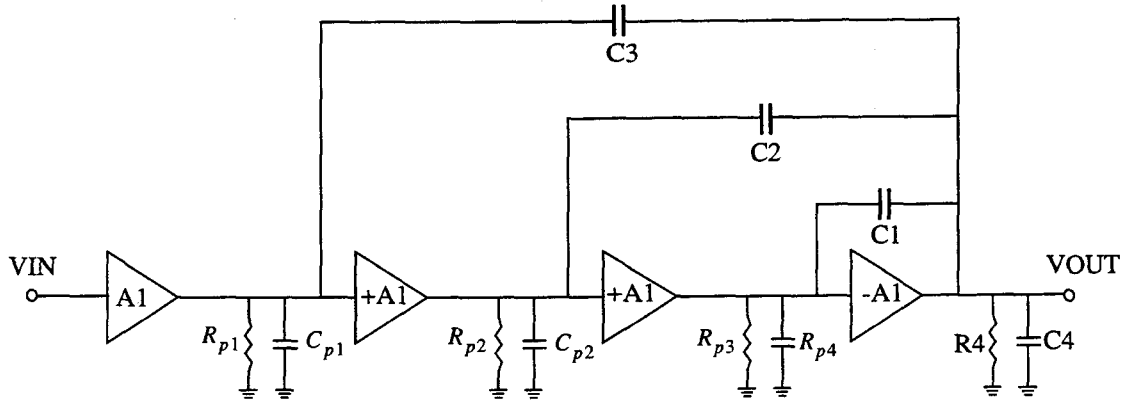

Figure 1.2. Four-stage amplifier with Nested Miller Compensation (NMC) technique.

Another multi-stage operational amplifier topology is the Nested Gm-C Compensation (NGCC) technique [3] shown in Figure 1.3. It is similar to NMC structure except that nested G_m feed-forward stages are used to provide negative feed-forward or LHP zeros to cancel LHP poles. This scheme increases the bandwidth, but the power-per-bandwidth ratio remains the same as in the NMC structure.

The above techniques are complex, and implementation in production depends upon many variables to ensure robustness with respect to repeatability and reproducibility in the manufacturing process. For example, in the NGCC structure, compensation capacitors are used to bypass high-frequency signals to the output node [1] to achieve high bandwidth, and negative feed-forwards are used to cancel the non-dominant poles. However, this method significantly degrades the settling time because of the inevitable pole-zero doublets introduced by the feed-forward elements [1].

A new frequency compensation method presented in this thesis overcomes the drawbacks associated with existing multi-stage topologies by introducing RC

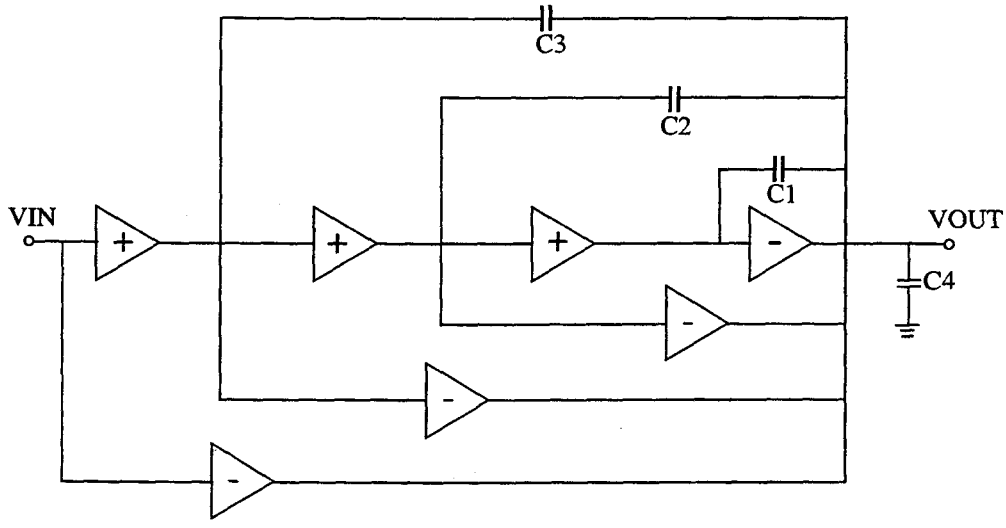

Figure 1.3. Four-stage amplifier with Nested G_m-C (NGCC) technique.

compensation networks around internal gain stages leaving the output node unaffected. By not loading the output stage with excessive compensation capacitance, the operational amplifier can exhibit high gain due to multi-stage structure, wide bandwidth, fast settling time and slew rate. The slew rate is determined by the output stage and the parasitic and load capacitances that it drives. In other words, by using local compensation networks around internal gain stages, the slew rate is not limited by the small output step sizes associated with them. Thus, the proposed method allows maximum bandwidth for a given technology feature size. Another advantage of this technique is that the use of bypass capacitors with series resistors blocks positive feed-forward and provides better control over pole-zero doublets to achieve fast settling times. Also, by not loading the output stage with compensation capacitance, the power-per-bandwidth ratio also improves. Finally, the proposed topology is compatible with techniques implemented for two-stage operational amplifiers to track process, temperature, and voltage variations.

Apart from the details, an important aspect of successful multi-stage operational amplifier design is a well-conceived design methodology. For example, a multi-stage operational amplifier design can be broken down into the design of stages that are familiar. Starting from the input, these stages can comprise a two-stage amplifier followed by simple single-stage amplifiers. By designing the two-stage amplifier to meet the single-pole response, additional stages can be used to boost both overall gain and bandwidth. The analysis will show that the dominant pole associated with the operational amplifier must always be associated with the input stage and not with the output stage.

Finally, a global feed-forward technique can be designed to boost slew rate and bandwidth, and reduce both the feedback compensation capacitors and noise to increase dynamic range. Output noise voltage density tends to increase with frequency due to

peaking closed-loop frequency response. The enhancement technique introduced in this thesis can reduce noise and increase the overall performance of the operational amplifier.

1.3 Design Methodology Explored in this Thesis

The goal of this thesis is to present well-supported guidelines, plots, tables, and expressions to ensure the successful design of multi-stage operational amplifiers.

The methodology starts with modeling the multi-stage operational amplifiers at the system level. This implies studying some of the important relationships that exist for high performance designs including dynamic range considerations, and minimization of amplifier noise, harmonic distortion, and intermodulation distortion. Other relationships include open-loop and closed-loop pole-zero placements and their relationships to frequency and time domain responses. Other goals include achieving fast settling times with respect to the open-loop frequency response which requires characterization of the stability in terms of gain and phase margins.

Next, comes the block level or ideal transistor modeling of such operational amplifiers. At this level, various characteristics must be studied including the key compensation components required to obtain the desired frequency and time domain responses. Because of this, the conventional wisdom on pole-splitting behavior must be re-examined. Also, due to the increased complexity in designing higher order operational amplifiers, the effect of component variation values on the overall performance characteristics must be studied.

Once the desired characteristics are specified, the circuit implementation for each block level model will be designed. Simulation results are obtained using HSPICE Level 23 device models for several performance specifications. The layouts associated with prototype designs are also presented.

The new compensation topology will be examined in higher-order systems such as four-stage operational amplifiers. Along with that, the new enhancement technique will be incorporated and presented. Finally, in the future work section, a discussion of multi-stage design based on technology considerations will be addressed. For example, as the minimum feature device sizes decrease, the use of more stages becomes optimal. This will eventually help us determine the optimum number of stages required for a given technology.

1.4 Thesis Outline

Following the introduction, six chapters will discuss high performance design for multi-stage operational amplifiers. Chapter 2 overviews some dynamic range considerations in terms of distortion and noise analysis. This chapter analyzes the equivalent input referred noise voltage of the amplifier and the non-linearities in terms of harmonic and intermodulation distortion.

Chapter 3 introduces a system-level approach by considering a linear time-invariant model for such amplifiers, and studies the stability and performance characteristics for both open-loop and closed-loop systems. The Nyquist criterion for stability is presented along with a quantitative stability in terms of: gain and phase margin. The maximum amount of feedback that can be used with a particular operational amplifier is addressed for two-, three-, and four-stage topologies.

Chapter 4 discusses the design of two- and three-stage amplifiers using a g_m block representation. The transfer functions of the uncompensated amplifier for each gain stage detailing the locations of the poles and zeros is derived and some important properties are addressed. Also, the pole-zero sensitivity due to variations in

compensation and component parameters for both two- and three-stage amplifiers are presented.

Chapter 5 introduces the circuit implementation of a fully-differential three-stage operational amplifier with common-mode feedback to maximize dynamic range. The design was simulated using HSPICE LEVEL 39 device models and the results are presented.

Chapter 6 introduces an enhancement technique to improve both stability and performance characteristics. Also, a realization of a four-stage operational amplifier is presented and some trade-off associated with these techniques are discussed.

Chapter 7 presents layouts of prototypes for a three- and four-stage operational amplifiers and describes some of the die area issues. Finally, this chapter concludes this thesis and discusses possible future work.

Chapter 2. Dynamic Range Considerations

This chapter considers the noise and distortion analyses in operational amplifiers and their effects on feedback implementations to facilitate the dynamic range of feedback amplifiers.

The noise phenomena to be considered are caused by small current and voltage fluctuations that are generated within the devices themselves [4]. The existence of noise is due to the fact that electrical charge is not continuous but is carried in discrete amounts equal to the electron charge. Thus noise is associated with fundamental processes in the integrated-circuit devices.

In section 2.1 various sources of electronic noise are considered and the equivalent circuits of common devices including noise generators are described. The noise analysis of complex circuits such as operational amplifiers are then performed.

The dynamic range is dependent on the noise floor that is associated with an operational amplifier. If the amplifier exhibits high noise the dynamic range of the feedback amplifier is reduced.

In section 2.2, two cases of distortion analysis are examined and their contributions to the dynamic range of the operational amplifier are considered. Trade-off between distortion and other amplifier performance parameters are analyzed.

2.1 Sources of Noise

Thermal Noise

Thermal noise in conventional resistors is due to the random thermal motion of electrons and is unaffected by the presence or absence of direct current since typical electron drift velocities in a conductor are much less than electron thermal velocities [4].

Since this source of noise is due to the thermal motion of electrons, it is natural to link it to the absolute temperature T. Thermal noise is in fact directly proportional to T; as T approaches zero, thermal noise also approaches zero.

In a resistor R, thermal noise can be presented by a voltage generator $\overline{v^2}$ in series as shown in Figure 2.1(a), or by a shunt current generator $\overline{i^2}$ as in Figure 2.1(b). The representations in Figure 2.1(a) and (b) are equivalent with

$$\overline{v^2} = 4kTR\Delta f \tag{2.1}$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \tag{2.2}$$

where k is Boltzmann's constant. At room temperature the term $4kT$ is about

$$4kT = 1.66 \times 10^{-20} V - C \tag{2.3}$$

Consider analysis of thermal noise in a simple circuit. Figure 2.1(c), shows a one-pole low-pass filter that includes the resistor noise voltage source. This network has a -3 dB corner frequency at

$$\omega_p = \frac{1}{RC} \tag{2.4}$$

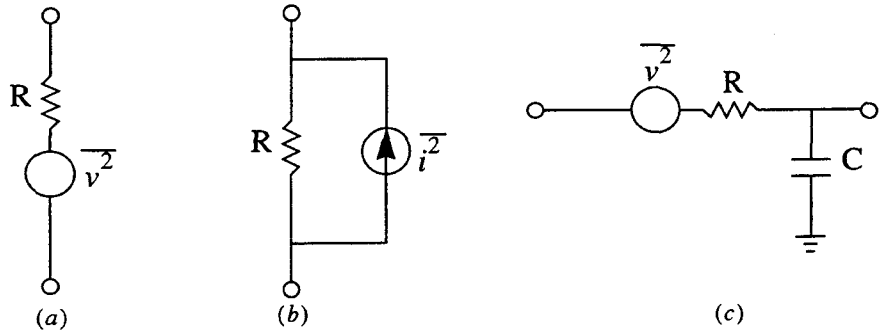

Figure 2.1. Noise sources. (a) Thevinin equivalent. (b) Norton equivalent. (c) One-pole low-pass filter.

or

$$f_p = \frac{1}{2\pi RC} \tag{2.5}$$

By replacing Δf with $\frac{\pi}{2} f_p$ which is the equivalent noise bandwidth of $\frac{1}{4RC}$ in equation (2.1), we get

$$\frac{\overline{v^2}}{\Delta f} = \frac{kT}{C} \tag{2.6}$$

This kT/C relationship clearly shows that smaller RMS noise is seen at the output of the network for larger capacitor values. The relationship in (2.1) is often represented in two different terms: 1) Power Spectral Density (PSD) meaning the square of the noise voltage per bandwidth

$$\frac{\overline{v^2}}{\Delta f} = 4KTR \tag{2.7}$$

2) or noise Voltage Spectral Density

$$\frac{\overline{v}}{\sqrt{\Delta f}} = \sqrt{4kTR} \tag{2.8}$$

For the one-pole low-pass filter of Figure 2.1(c), the noise Voltage Spectral Density is

$$\frac{\overline{v}}{\sqrt{\Delta f}} = \sqrt{\frac{kT}{C}} \tag{2.9}$$

Assuming Gaussian thermal noise, this property can also be described as the standard deviation of the noise voltage

$$\sigma_{\overline{v}} = \sqrt{\frac{kT}{C}} \tag{2.10}$$

Flicker Noise

Flicker or 1/f noise is found in all active devices as well as some discrete passive elements such as carbon resistors. In CMOS transistors flicker noise is usually associated with defects at the silicon-SiO_2 interface. Clearly, 1/f noise is very process dependent.

Flicker noise is associated with the flow of direct current and displays a Power Spectral Density of the form

$$\frac{\overline{i^2}}{\Delta f} = K_f \frac{I^{AF}}{K' f} \tag{2.11}$$

where

Δf	is a small bandwidth at frequency f
I	is a direct current
K_f	is a flicker noise coefficient which is process dependent
AF	is a constant in the range 0.5 to 2
K'	is constant for a particular device

The flicker noise Power Spectral Density has an approximate 1/f frequency dependence (alternatively called *"1/f"* noise). Flicker noise is most significant at low frequencies, and may dominate device noise at frequencies well into the megahertz range [4]. An important point to note is that the flicker noise is present with direct current I, whereas thermal noise is always present.

Noise in CMOS Circuits

In the structure of the CMOS transistors there is a resistive channel joining source and drain and the drain current is controlled by the gate-source voltage. The resistance associated with the channel exhibits thermal noise and the associated noise current $\overline{i^2}_d$ is connected between the drain and source in the small-signal equivalent circuit. Flicker noise also represents a drain-to-source current; combining the two currents, we obtain an equivalent noise current generator.

The resistance due to thermal noise in a small-signal equivalent model is given by

$$R = \frac{2}{3g_m} \tag{2.12}$$

where g_m is the small-signal transconductance of the device. By modifying (2.2), the thermal noise current generator is

$$\overline{i^2}_d = 4kT\left(\frac{2}{3}g_m\right)\left(1 + \frac{g_{mbs}}{g_m}\right)\Delta f \tag{2.13}$$

where g_{mbs} is the small-signal back-gate transconductance of the device and $\frac{2}{3}$ is an empirical correction factor. The equivalent noise voltage power is

$$\overline{v^2}_{eq} = \frac{\overline{i^2}_d}{g^2_m} = 4kT\left(\frac{2}{3g_m}\right)\left(1 + \frac{g_{mbs}}{g_m}\right)\Delta f \tag{2.14}$$

Figures 2.2(a) and (b) shows the equivalent current and voltage noise generators for an NMOS transistor. The equation for flicker noise is given by

$$\overline{i^2}_d = \frac{K_f I_D^{AF} \Delta f}{C_{ox} WLf} \tag{2.15}$$

where I_D corresponds to the DC direct current, C_{ox} is the gate oxide capacitance per unit area, and W and L are the width and length of the transistor. K_f and AF are the process parameters. The equivalent noise voltage can be written as (with A_F=1)

$$\overline{v^2_{eq}} = \frac{\overline{i^2_d}}{g^2_m} = \frac{K_f \Delta f}{2\mu C^2_{ox} W^2 f} \tag{2.16}$$

The overall noise current in a MOS transistor including thermal and flicker noise component is

$$\overline{i^2_d} = 4kT\left(\frac{2}{3}g_m\right)\left(1 + \frac{g_{mbs}}{g_m}\right)\Delta f + \frac{K_f I_D^{AF} \Delta f}{C_{ox} WLf} \tag{2.17}$$

and the overall noise voltage is

$$\overline{v^2_d} = 4kT\left(\frac{2}{3g_m}\right)\left(1 + \frac{g_{mbs}}{g_m}\right)\Delta f + \frac{K_f \Delta f}{2\mu C^2_{ox} W^2 f} \tag{2.18}$$

where $1 + \frac{g_{mbs}}{g_m}$ is approximately one. For example, for an NMOS transistor with source and bulk connected together, the g_{mbs} term goes to zero.

Figure 2.3 represents the frequency characteristics of the thermal and flicker noise power spectral densities. Notice that in the low-frequency regions the flicker noise dominates, whereas thermal noise dominates at high frequencies. The 1/f noise corner frequency can be determined as shown in Figure 2.3(c) by equating the two responses.

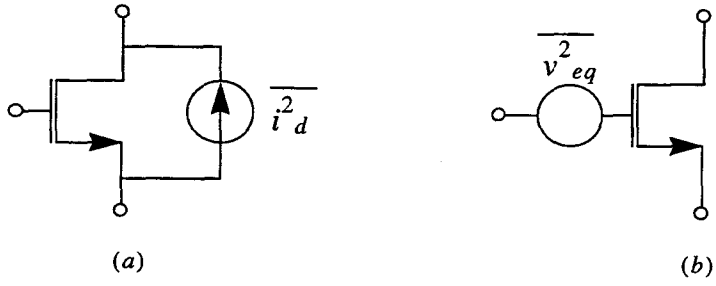

Figure 2.2. Equivalent (a) current and (b) voltage noise generators.

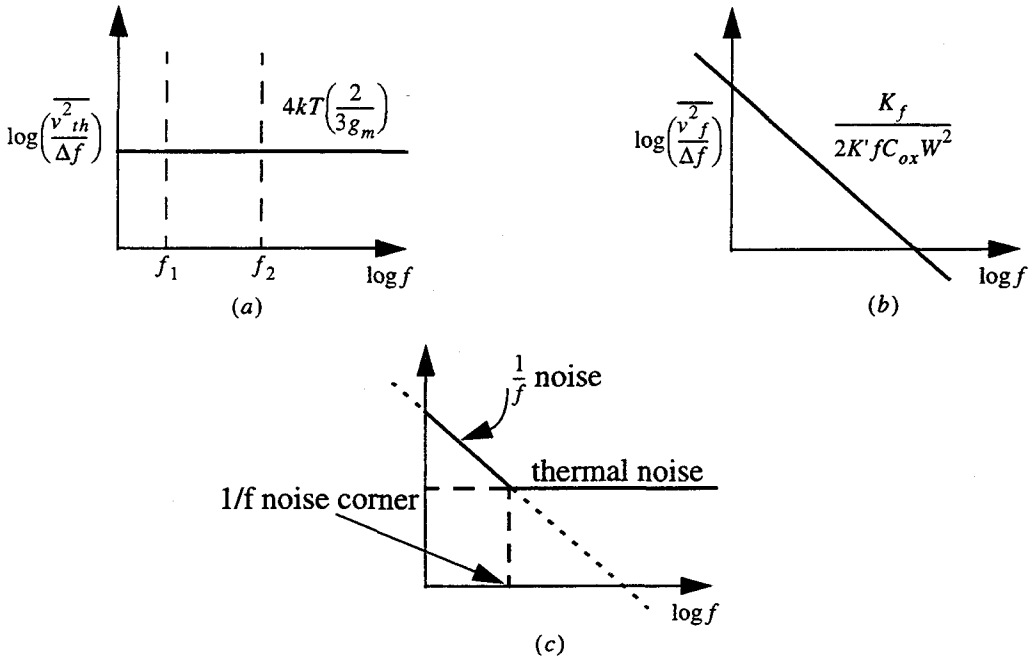

Figure 2.3. (a) Thermal noise. (b) Flicker noise. (c) Overall response.

Noise Analysis in CMOS Circuits

Consider the three-stage operational amplifier represented in Figure 2.4. Each block represents a single gain stage of the amplifier. The first stage is a differential pair followed by single-ended gain stages. In Figure 2.4(a), note that each stage is modeled using an equivalent input noise voltage source.

We first find the gains from each noise source to the output V_{out} as follows:

$$\overline{v^2_{out}} = \overline{v^2_{n1}} \cdot A^2_1 \cdot A^2_2 \cdot A^2_3 + \overline{v^2_{n2}} \cdot A^2_2 \cdot A^2_3 + \overline{v^2_{n3}} \cdot A^2_3 \qquad (2.19)$$

Similarly for Figure 2.4 (b),

$$\overline{v^2_{out}} = \overline{v^2_{eq}} \cdot A^2_1 \cdot A^2_2 \cdot A^2_3 \qquad (2.20)$$

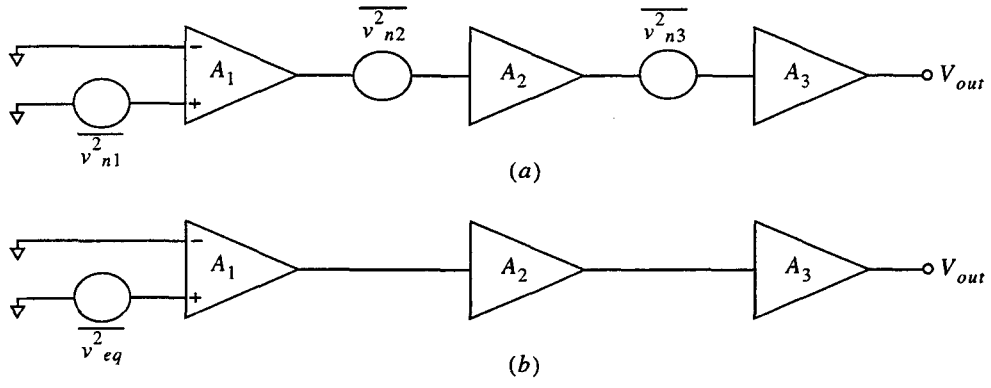

Figure 2.4. (a) Three-stage amplifier with equivalent noise voltage sources at the input to each stage; (b) equivalent input noise.

where $\overline{v^2_{eq}}$ is the total equivalent input noise of the operational amplifier. Note that gain stages A_2 and A_3 are considered to be noiseless in Figure 2.4(b). Finally, equating and solving gives

$$\overline{v^2_{eq}} = \overline{v^2_{n1}} + \frac{\overline{v^2_{n2}}}{A^2_1} + \frac{\overline{v^2_{n3}}}{A^2_1 \cdot A^2_2} \qquad (2.21)$$

(2.21) illustrates an important design consideration: The noise of succeeding stages is reduced by the gain of the preceding stages when referred to the input. Thus, the dominant noise source is usually the first stage of the amplifier. The remaining noise terms are negligible if the gains of the first and second stages are large. For first-order noise analysis, one needs only to analyze the noise of the input stage of an operational amplifier.

In this thesis, design emphasis is on achieving high-gain and high-speed. It was decided that a differential folded cascode pair (Figure 2.5) be used for its high-gain [5].

Note that each transistor has been modeled with an equivalent noise voltage source. In the following we assume perfect matching between all transistor pairs.

Due to amplifier symmetry, we need only analyze a differential half-circuit of the amplifier and multiply the results by two. We can start by finding the output conductance of this stage given by

$$g_{out} \cong \frac{(g_{ds4} + g_{ds1}) \times g_{ds6}}{g_{m6}} + \frac{g_{ds8} \times g_{ds10}}{g_{m8}} \qquad (2.22)$$

We then find the gains from each noise source to the output node, v_{o1}. For the gain from v_{n1} to v_{o1},

$$\left|\frac{v_{o1}}{v_{n1}}\right| = \frac{g_{m1}}{g_{out}} \qquad (2.23)$$

Next, for v_{n4}, notice that M4 is in the common-source configuration, and the load of the amplifier is the load of the cascode stage. So, the gain from v_{n4} to v_{o1} is

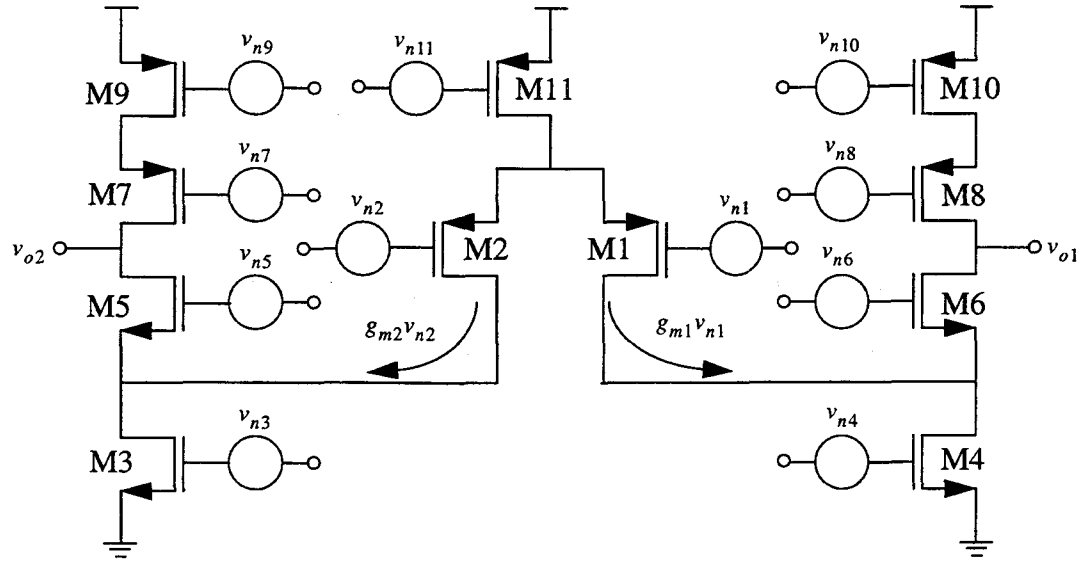

Figure 2.5. Fully-differential folded cascode input pair with noise sources.

$$\left|\frac{v_{o1}}{v_{n4}}\right| = \frac{g_{m4}}{g_{out}} \tag{2.24}$$

Next, for v_{n6}, notice that M6 acts as a source follower. The current through M6 is then equal to the voltage at the source of M6 multiplied by the conductance at that node. Thus,

$$i_{M6} = v_{n6} \times (g_{ds1} + g_{ds4}) \tag{2.25}$$

Finally, the gain from v_{n6} to v_{o1} is the current divided by the conductance seen at the output node given by

$$\left|\frac{v_{o1}}{v_{n6}}\right| = \frac{g_{ds1} + g_{ds4}}{g_{out}} \tag{2.26}$$

Following the same discussion, the gain from v_{n8} to v_{o1} can be inferred from (2.26) except that there is no additional branch for current to split, from M8 to be

$$\left|\frac{v_{o1}}{v_{n8}}\right| = \frac{g_{ds10}}{g_{out}} \tag{2.27}$$

Lastly, the gain from v_{n10} to v_{o1} can be found in the manner similar to equation (2.24) and can be written as

$$\left|\frac{v_{o1}}{v_{n10}}\right| = \frac{g_{m10}}{g_{out}} \tag{2.28}$$

Regarding the gain from v_{n11} to v_{o1}, note that v_{n11} modulates the bias current of M11 which is split equally into two equivalent branches. Hence, this noise is a common-mode signal which can be neglected. Combining the results from above, the equivalent noise power at the output node can be written as

$$\overline{v_{o1}^2} = \frac{1}{g_{out}^2}(g_{m1}^2\overline{v_{n1}^2} + g_{m4}^2\overline{v_{n4}^2} + (g_{ds1} + g_{ds4})^2\overline{v_{n6}^2} + g_{ds10}^2\overline{v_{n8}^2} + g_{m10}^2\overline{v_{n10}^2}) \tag{2.29}$$

The noise at the output node can be referred back as an equivalent input noise voltage

power $\overline{v_{eq}^2}$, by dividing (2.29) by the overall gain from v_{n1} to v_{o1} given in (2.23) as

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + \frac{g_{m4}^2}{g_{m1}^2}\overline{v_{n4}^2} + \frac{(g_{ds1}+g_{ds4})^2}{g_{m1}^2}\overline{v_{n6}^2} + \frac{g_{ds10}^2}{g_{m1}^2}\overline{v_{n8}^2} + \frac{g_{m10}^2}{g_{m1}^2}\overline{v_{n10}^2} \qquad (2.30)$$

Note that all terms with g_{ds} in the numerator can be neglected since $g_{ds} << g_m$, and $\overline{v_{eq}^2}$ can be simplified to

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + \left(\frac{g_{m4}}{g_{m1}}\right)^2\overline{v_{n4}^2} + \left(\frac{g_{m10}}{g_{m1}}\right)^2\overline{v_{n10}^2} \qquad (2.31)$$

For the usual DC biasing of this circuit in a typical design,

$$g_{m4} \approx 2 \times g_{m1} \qquad (2.32)$$

and

$$g_{m10} \approx g_{m1} \qquad (2.33)$$

Hence, (2.31) can be simplified to

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + 4\overline{v_{n4}^2} + \overline{v_{n10}^2} \qquad (2.34)$$

For the thermal noise power spectral density of the amplifier, we make the substitution

$$\frac{\overline{v_{th}^2}}{\Delta f} = 4kT\left(\frac{2}{3g_m}\right) = \frac{8kT}{3g_m} \qquad (2.35)$$

into (2.34) resulting in

$$\frac{\overline{v_{eq}^2}}{\Delta f} \cong \frac{8kT}{3}\left(\frac{1}{g_{m1}}\right) + \frac{32kT}{3}\left(\frac{1}{g_{m1}}\right) + \frac{8kT}{3}\left(\frac{1}{g_{m1}}\right) \Rightarrow 16kT\left(\frac{1}{g_{m1}}\right) \qquad (2.36)$$

As can be seen, the thermal noise spectral density is determined by g_{m1}. In other words, g_{m1} should be made as large as possible to minimize thermal noise taking into account the stability and power consumption of the overall amplifier.

Considering flicker noise which dominates at low frequencies, we substitute

$$g_m = \sqrt{\left(2\mu C_{ox}\left(\frac{W}{L}\right)\right)I_D} \tag{2.37}$$

into (2.31) resulting in

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + \left(\frac{(W/L)_4}{(W/L)_1}\right)\left(\frac{I_{D4}}{I_{D1}}\right)\overline{v_{n4}^2} + \left(\frac{\mu_p}{\mu_n}\right)\left(\frac{(W/L)_{10}}{(W/L)_1}\right)\left(\frac{I_{D10}}{I_{D1}}\right)\overline{v_{n10}^2} \tag{2.38}$$

The following assumptions can usually be made as mentioned earlier:

$$I_{D4} = 2I_{D1} \tag{2.39}$$

and

$$I_{D10} = I_{D1} \tag{2.40}$$

Substituting (2.39) and (2.40) in (2.38), we get

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + 2\left(\frac{(W/L)_4}{(W/L)_1}\right)\overline{v_{n4}^2} + \left(\frac{\mu_p}{\mu_n}\right)\left(\frac{(W/L)_{10}}{(W/L)_1}\right)\overline{v_{n10}^2} \tag{2.41}$$

Now, substituting the spectral density formulation of (2.16) into (2.41),

$$\frac{\overline{v_{eq}^2}}{\Delta f} = \frac{1}{2C_{ox}^2 f\mu_p}\left(\frac{K_{fp}}{W_1^2} + \frac{2L_1K_{fn}}{W_1L_4W_4} + \frac{L_1K_{fp}}{W_1L_{10}W_{10}}\right) \tag{2.42}$$

(2.42) can further be reduced by making the assumptions mentioned earlier as

$$W_4 = 2\frac{\mu_n}{\mu_p}W_1 \tag{2.43}$$

and

$$W_{10} = W_1 \tag{2.44}$$

resulting in

$$\frac{\overline{v_{eq}^2}}{\Delta f} = \frac{1}{2C_{ox}^2 f W_1^2}\left[\frac{K_{fp}}{\mu_p}\left(1 + \frac{L_1}{L_{10}}\right) + \frac{K_{fn}}{\mu_n}\left(\frac{L_1}{L_4}\right)\right] \tag{2.45}$$

From the above equation, flicker noise can be improved by increasing W_1, L_{10}, L_4. However, in multi-stage operational amplifiers we would like to maintain as short

channel lengths as possible (i.e. L_1=L_4=L_{10}) to obtain high speed performance. High gains can be achieved by cascading gain stages and thus, noise improvement can be achieved by increasing W_1.

Noise due to Miller Compensation Networks

In the previous section, we showed that the input stage contributes appreciably to the equivalent input referred noise. The noise performance is related to the input transconductance according to (2.36) and (2.45). An interesting expression for the noise of a Miller compensated amplifier follows from the observation that to maintain a constant unity-gain frequency, the transconductance of the input stage must be proportional to the Miller capacitance. This implies a relation between the noise of the circuit and the value of the Miller capacitor. To keep the frequency compensation optimal, increased Miller capacitance must be accompanied by higher input stage transconductance. A more detailed analysis is performed in Chapter 4.

Regarding noise performance in feedback circuits (i.e., unity-gain feedback), there are two separate approaches. The first is to estimate the effect of feedback on the signal-to-noise ratio of the circuit, and the second is to determine the effective load capacitance seen by the input due to the feedback configuration. Figure 2.6 shows the Bode plots of the amplifier. The overall unity feedback configuration reduces the output noise of the circuit. The gray area now presents the total output noise reduction factor of the unity-gain amplifier due to the frequency-dependent loop gain T(ω). However, the

feedback gain is reduced as well, meaning that the output signal to noise ratio does not improve with feedback for the overall circuit [1]. The input stage carries the smallest signals which are most easily corrupted by noise, while the large signals in the output stage produce the greatest distortion contributions as we review in the next section.

2.2 Distortion Analysis

Active devices are not linear and thus account for distortion of the output signal. Although linear network theory does not apply to these types of circuits, we can obtain workable results using it for many amplifier circuits.

In the past, several standard input test signals have been defined. By taking the ratio of the desired and undesired output signals, distortion figures that are measures of non-linearity can be obtained. Two of the most important figures are harmonic and intermodulation distortion. Harmonic distortion relates to a single sinusoidal input and

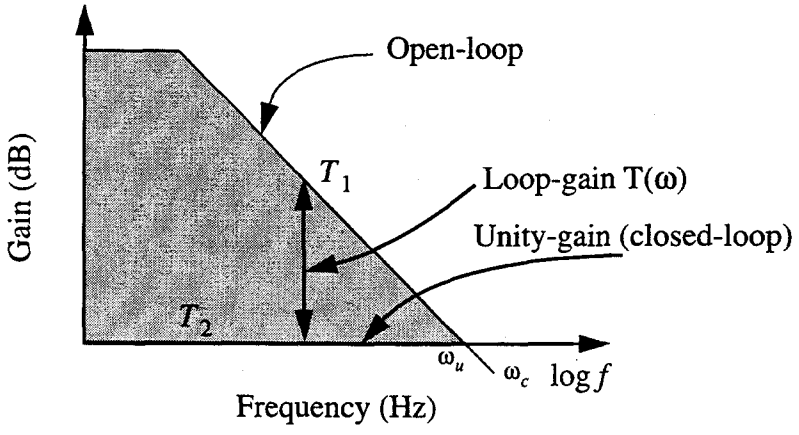

Figure 2.6. Unity-gain Bode plot showing the noise reduction due to the loop gain in a two-stage Miller compensated amplifier.

its effect on the output. Intermodulation distortion relates to a two tone sinusoidal signal applied to the input.

Harmonic Distortion

Applying a single sinusoid to a non-linear circuit results in a spectrum that consists of a peak at the fundamental frequency plus several higher order components. The fundamental frequency corresponds to the ideal output signal frequency, while the higher order harmonics account for the harmonic distortion. The ratio of the total energy in the harmonics to the energy present in the fundamental signal defines the total harmonic distortion, THD. If the amplitude of each of the components of the output signal is a_1, a_2, a_3,.... where a_1 is the amplitude of the fundamental frequency, then THD is

$$THD = \frac{\sqrt{a^2{}_2 + a^2{}_3 + \ldots}}{a_1} \tag{2.46}$$

To obtain the output non-linearity of a circuit, a Taylor series expansion of the transfer function around a quiescent operating point is performed. Suppose that the transfer function can be presented as

$$E_0 = f(E_i) \tag{2.47}$$

We can expand (2.47) in a Taylor series about the quiescent point as

$$E_{0Q} = f(E_{iQ}) \tag{2.48}$$

where $f(E_{iQ})$ can be written as

$$E_0 = E_{0Q} + (E_i - E_{iQ}) \cdot \left.\frac{dE_0}{dE_i}\right|_{E_i = E_{iQ}} + \frac{(E_i - E_{iQ})^2}{2!} \cdot \left.\frac{d^2 E_0}{dE^2{}_i}\right|_{E_i = E_{iQ}} + \ldots \tag{2.49}$$

We can also express (2.49) as

$$E_0 = E_{0Q} + A_1(E_i - E_{iQ}) + A_2(E_i - E_{iQ})^2 + \ldots \qquad (2.50)$$

The constants, A_1, A_2,... follow from the differentiations of the analytical function. In the case that no analytical description is available, a simple curve fitting procedure readily establishes the polynomial coefficients.

Now, suppose that a sinusoidal input signal around the quiescent point E_{iQ} is applied to the system as

$$E_i - E_{iQ} = \hat{E}_i \cos \omega t \qquad (2.51)$$

Substituting (2.51) into (2.50) results in

$$\begin{aligned} E_0 - E_{0Q} = & \left(\frac{1}{2}A_2\hat{E}_i^2 + \frac{3}{8}A_4\hat{E}_i^4 + \ldots\right) \\ & + \left(A_1\hat{E}_i + \frac{3}{4}A_3\hat{E}_i^3 + \ldots\right)\cos \omega t \\ & + \left(\frac{1}{2}A_2\hat{E}_i^2 + \frac{1}{2}A_4\hat{E}_i^4 + \ldots\right)\cos 2\omega t \\ & + \left(\frac{1}{4}A_3\hat{E}_i^3 + \frac{5}{16}A_5\hat{E}_i^3 + \ldots\right)\cos 3\omega t \end{aligned} \qquad (2.52)$$

Furthermore, (2.52) can be rewritten as

$$E_0 - E_{0Q} = a_0 + a_1 \cos \omega t + a_2 \cos 2\omega t + a_3 \cos 3\omega t + \ldots \qquad (2.53)$$

where the constants a_1, a_2, a_3,... represent the amplitudes of the harmonic components of the output signal. We can also determine the amplitude of the harmonic components as a function of the input signal amplitude. The term a_0 indicates a DC offset introduced by the non-linearity of the transfer function. The term depends solely on even-order harmonics which non-symmetrical transfer functions introduce. When the transfer function is not symmetrical around the quiescent point, the average value of the output signal shifts away from the quiescent output value E_0.

Substituting the constants $a_1, a_2, a_3, \ldots$ of (2.53) into (2.52) results in

$$HD_2 = \frac{a_2}{a_1} = \frac{\left(\frac{1}{2}A_2\hat{E}_i^2 + \frac{1}{2}A_4\hat{E}_i^4 + \ldots\right)}{\left(A_1\hat{E}_i + \frac{3}{8}A_3\hat{E}_i^3 + \ldots\right)} \approx \hat{E}_i\left(\frac{A_2}{2A_1}\right) \tag{2.54}$$

$$HD_3 = \frac{a_3}{a_1} = \frac{\left(\frac{1}{4}A_3\hat{E}_i^3 + \frac{5}{16}A_3\hat{E}_i^3 + \ldots\right)}{\left(A_1\hat{E}_i + \frac{3}{8}A_3\hat{E}_i^3 + \ldots\right)} \approx \hat{E}^2{}_i\left(\frac{A_3}{4A_1}\right) \tag{2.55}$$

Where $HD_2, HD_3, \ldots$ represent the fractional harmonic distortion figures in the output signal. Again from (2.52), the total harmonic distortion is

$$THD = \sqrt{HD^2{}_2 + HD^2{}_3 + \ldots} \tag{2.56}$$

Intermodulation Distortion

Intermodulation distortion (IM) is measured by inputting a signal that consists of two sinusoid of different frequencies and possibly different amplitudes. Due to the mixing effects, the non-linear amplifier will generate many frequency components at the output.

There are many definitions of intermodulation, but we use the definition with one input to be at the low frequency with high amplitude, and the other at high frequency and low amplitude. The usual ratio of their magnitudes is 4:1 [1]. Also, another common test is to apply two equal amplitude tones. Assuming that the input at the lower frequency is denoted by ω_a, and that higher frequency by ω_b, the output power spectrum has components at

$$\omega_a, 2\omega_a, 3\omega_a, \ldots$$

$$\omega_b, (\omega_b \pm \omega_a), (\omega_b \pm 2\omega_a), \ldots \tag{2.57}$$

The first line in (2.57) denotes the harmonics of ω_a which can usually be removed by a

low-pass filter. The second line denotes intermodulation products.

The analysis of intermodulation distortion follows from a similar analysis as for harmonic distortion. The input signal is

$$E_i = \hat{E}_a \cos\omega_a + \hat{E}_b \cos\omega_b \tag{2.58}$$

where $\hat{E}_a$ is the amplitude of the low frequency signal and $\hat{E}_b$ the amplitude of the high frequency signal. Substituting (2.58) into the Taylor series of (2.50) and performing a binomial expansion, we obtain the intermodulation products as:

$$E_o = \hat{A_1} E_b \cos\omega_b + A_2 \hat{E}_a \hat{E}_b \cos(\omega_b \pm \omega_a)$$

$$+ \frac{3A_3 \hat{E^2}_a \hat{E}_b}{4} \cos(\omega_b \pm 2\omega_a) + \ldots \tag{2.59}$$

From the above equation we can now define the intermodulation distortion in a fashion similar to the harmonic distortion given in (2.54) and (2.55).

$$IM_2 = 2\frac{A_2 \hat{E}_a \hat{E}_b}{A_1 \hat{E}_b} = 2\frac{A_2 \hat{E}_a}{A_1} \tag{2.60}$$

$$IM_3 = 2\frac{3A_3 \hat{E}_a^2 \hat{E}_b}{4A_1 \hat{E}_b} = \frac{3A_3 \hat{E}_a^2}{2A_1} \tag{2.61}$$

We will neglect higher order IM products as they are usually small in comparison to IM_2 and IM_3.

The factor 2 in (2.60) and (2.61) accounts for the two identical intermodulation products below and above ω_b. Analogous to the total harmonic distortion, we can express the total intermodulation distortion as

$$IM = \sqrt{IM^2{}_2 + IM^2{}_3 + \ldots} \tag{2.62}$$

Distortion due to Miller Compensation Network

An important aspect of Miller compensation is that it employs local feedback to shape the frequency response in such a way that the amplifier behaves as a one-pole response up to the unity-gain frequency. This suggests that the amplifier is stable and the non-linearity of the amplifier is reduced due to the loop gain.

Assuming that all other components are ideal, the non-linearity of active devices determines distortion. In a multi-stage environment, the internal stages do not have large swings which results in lower distortion. The output stage drives the highest levels usually limits distortion performance in the circuit.

Figure 2.7 shows the Bode plots of the open-loop and unity-gain closed-loop Miller compensated amplifier. The overall loop gain T(ω) reduces the distortion of the circuit. Clearly, loop gain contributes to lower distortion which is another motivation for multi-stage operational amplifiers.

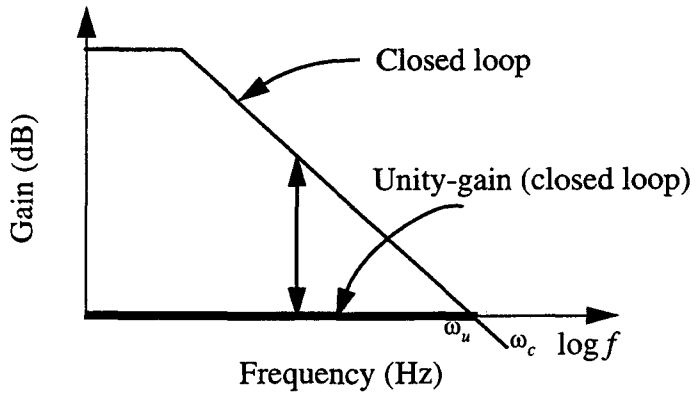

Figure 2.7. Bode Plot of the distortion reduction due to the local feedback in a two-stage Miller compensated amplifier.

Dynamic Range

Dynamic range is another measure of system performance determined by

$$DR = \frac{|V_{in(max)}|}{V_{in,\,noise(RMS)}} \tag{2.63}$$

where $|V_{in(max)}|$ is the maximum input voltage at a specific distortion level (e.g. THD=-40dB) and $V_{in,\,noise(RMS)}$ is the equivalent RMS input noise voltage.

Chapter 3. Frequency and Transient Response Considerations

An important aspect of successful amplifier design is system-level modeling of an equivalent transfer function to analyze stability and performance. This chapter begins by reviewing stability criteria and associated quantitative measures. The relationship of these measures for achieving maximum frequency and time-domain performance are discussed.

Operational amplifiers are usually used in a negative feedback configuration. Hence, it is essential to characterize the open-loop transfer function of the amplifier to assure adequate stability, and to predict the amplifier closed-loop response.

This chapter explores the design goals required for an operational amplifier to achieve maximum performance when subjected to process, temperature, and voltage variations. Two-, three-, and four-stage operational amplifier models are developed in the form of transfer functions. Past studies performed to understand the performance characteristics of two-stage amplifiers are extended to understand multi-stage operational amplifiers.

Optimum compensation of an operational amplifier is one of the most difficult aspects of design, especially when considering process, temperature, and voltage variations. That is perhaps why multi-stage operational amplifiers were seldom considered viable in the past. However, the systematic approach presented here enables the design of robust multi-stage operational amplifiers.

3.1 Open-Loop Frequency Response

Stability Analysis

Stability is achieved if and only if all poles of the system transfer function reside in the left half of the complex s-plane. Apart from that, it is also necessary to ensure stability when the amplifier is subjected to process, voltage, and temperature variations. The need to maintain sufficient stability is based on bandwidth and accuracy requirements of feedback amplifiers.

It is essential to characterize the open-loop frequency response of the operational amplifier prior to applying feedback for several reasons. In the open-loop transfer function, the positions of the poles are readily determined since the transfer function can be presented in a factored form. However, when feedback is applied to the amplifier, the positions of the poles versus return ratio can be determined by applying root locus theory to the closed-loop transfer function. Fundamental to the analysis of stability is the Nyquist stability criterion which examines phase and magnitude of the open-loop frequency response.

Nyquist Stability Criterion

A system is said to be unstable if for any frequency where the loop gain is greater than or equal to one, the excess loop phase shift is greater than 180°.

Gain and Phase Margin

It is inevitable that variations in temperature, process parameters, and voltage occur in integrated circuits. This may cause the operational amplifier to become unstable

if certain stability margins are not satisfied. Thus, it is desirable to have a measure of stability to maintain robust operational amplifier design. The Nyquist criterion yields just such quantitative metrics; the gain and phase margins as shown in Figure 3.1.

Implicit in Figure 3.1 is the question of how much feedback can be applied with a given set of physical components. Active devices exhibit a certain amount of phase lag at high frequencies [1] which accumulates when a number of gain stages are cascaded. Hence, cascading stages to increase gain simultaneously reduces the phase and gain margins of the circuit which implies a trade-off between gain and bandwidth.

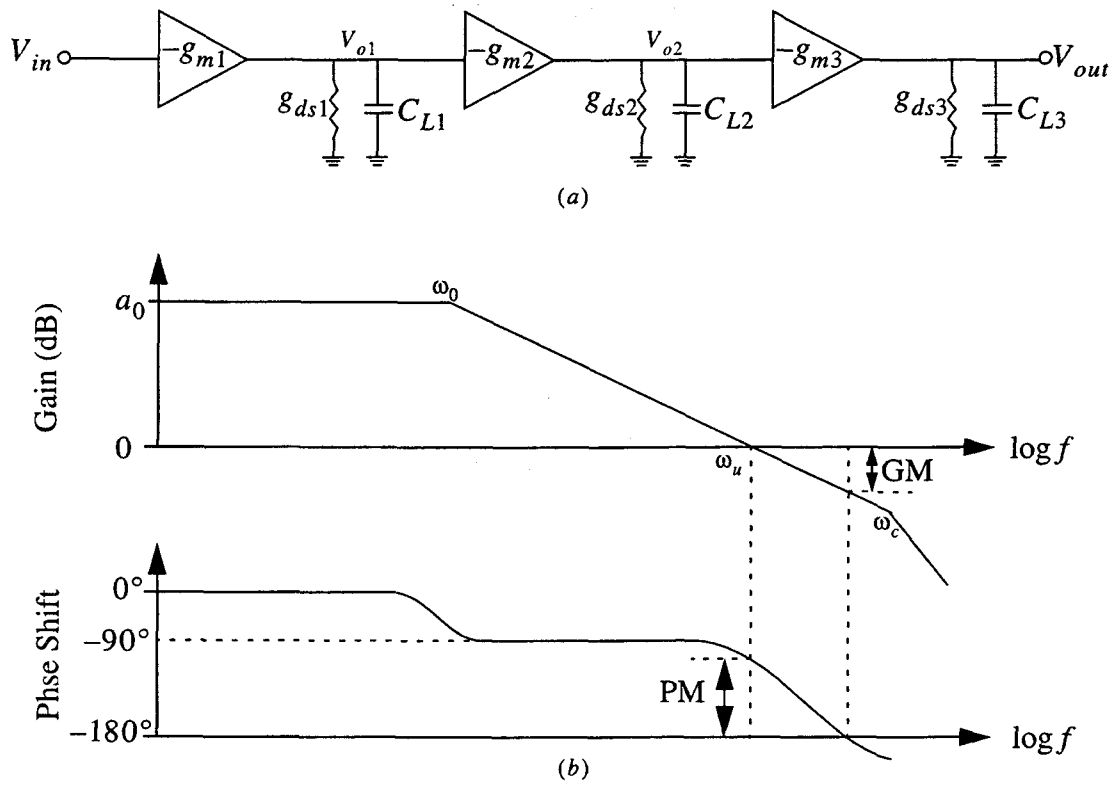

Figure 3.1. (a) Three-stage amplifier. (b) Frequency response of a stable operational amplifier in terms of the phase and gain margins.

The optimally compensated amplifier realizes gain a_0 across bandwidth ω_0 while optimizing the phase margin for fast settling times. At high frequencies, capacitors in integrated circuits (intended or parasitic) determine the maximum bandwidth obtainable as shown in Figure 3.1. Furthermore, at high frequencies, the frequency response depends only upon the capacitors without regard to resistors. The maximum obtainable bandwidth can be determined to the first order by multiplying the pole frequencies of each gain stage in the signal path. For example, for a three-stage amplifier as shown in Figure 3.1(a), the maximum frequency can be written as

$$|A| = \frac{a_0 g_{m1} g_{m2} g_{m3}}{\omega_c^{\,3} C_{L1} C_{L2} C_{L3}} \tag{3.1}$$

In terms of a Bode plot, (3.1) results in a -60dB per decade slope at ω_c. We solve for ω_c, knowing what the gain should be unity at that frequency:

$$\omega_c = \sqrt[3]{\frac{a_0 g_{m1} g_{m2} g_{m3}}{C_{L1} C_{L2} C_{L3}}} \tag{3.2}$$

The results described above can be applied to N stages. With N stages, the upper limit for the frequency response is 20N dB. This value relies on the assumption that the amplifier is ideal, meaning that the feedback network or any other part of the circuit does not introduce any additional poles and that there is no attenuation for high frequencies. At high frequencies, the phase lag of the Nth order asymptote approaches $90N°$ [1].

Optimal Frequency Response for Integrated Amplifiers

As integrated circuit technology improves, it becomes easier to achieve high performance at high frequencies. In terms of production, we must realize that optimally compensated amplifier may be sensitive to parameter variations. Changing operational amplifier parameters such as the load, transconductance, etc., can change the behavior of

the design. The important demands for an optimal operational amplifier frequency compensation are:

1. Absolute stability with sufficient phase and gain margins when subjected to variations in the load, compensation network, or other circuit parameters.
2. As high an open-loop gain as possible to cover a wide spectrum of high accuracy applications.

Without knowledge of a specific application it is wise to design operational amplifiers to have as much gain and bandwidth as possible. High open-loop gain at low frequencies implies high settling accuracy which is often desirable.

Another guideline is that additional poles and zeros are highly undesirable in the open-loop transfer function, especially if pole-zero cancellations are imperfect. The resulting doublets prolong settling time to be much longer than expected judging from the bandwidth. This restricts the applicability of the amplifier in circuits where settling is of prime importance or in applications where environmental variations are present.

Looking at Figure 3.1 closely, the maximum DC gain is determined by the number of stages in the circuit. Above the corner frequency ω_0, the gain decreases at a -20 dB/dec. The total phase shift at low frequencies is 90° which means a phase margin of 90°. At some frequency ω_c, the gain curve decreases at a faster rate due to the remaining poles in the amplifier. At that point the desired gain is higher than that of the transistors capable of driving into their own parasitic capacitances [1].

However, since a phase margin of 90° is more than sufficient, a good design technique is to increase the unity-gain frequency ω_u such that an acceptable phase margin less than 90° is achieved.

Conditional Stability

Figure 3.2 shows the case of a conditionally stable amplifier. The dashed line represents the absolutely stable amplifier shown in Figure 3.1 and the solid line represents the conditionally stable amplifier. In the case of the dashed line, ω_u and ω_0 are proportional to gain A in dBs of the amplifier by

$$\omega_u = \omega_0 \times A_0 \tag{3.3}$$

or

$$\omega_0 = \frac{\omega_u}{A_0} \tag{3.4}$$

This linear characteristic of equation (3.3) represents gain bandwidth product which relates to a single pole response with a -20 dB/dec roll-off. In the case of the solid line in this example, there are three poles at frequency ω_0, followed by two zeros just above the 0 dB frequency ω_u. As a result, the Bode plot rolls off with a slope of -60 dB/

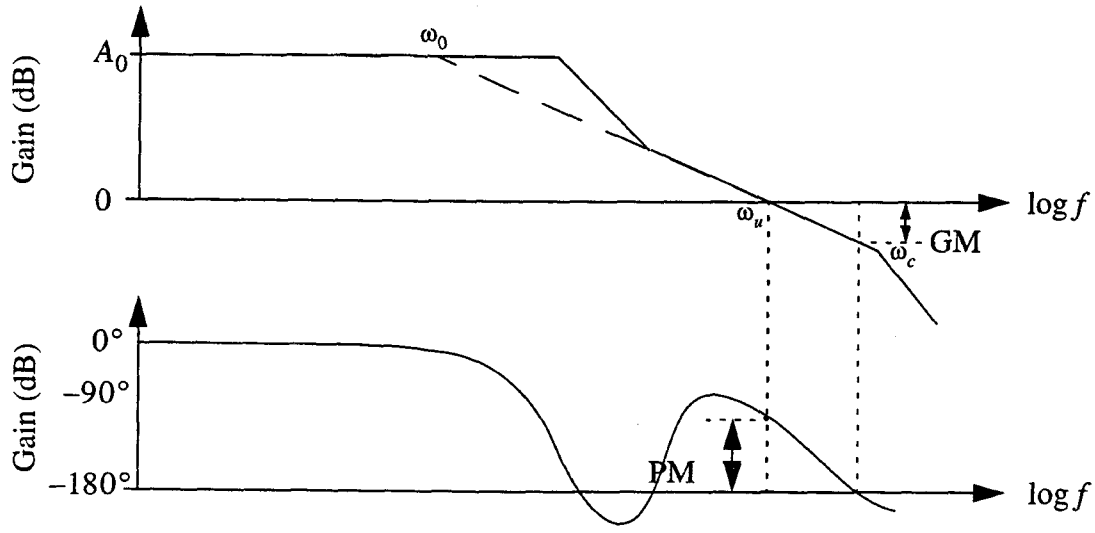

Figure 3.2. Frequency response of a conditionally stable amplifier.

dec, but after the two zeros it crosses the 0 dB axis at a -20 dB/dec roll-off. Although the phase shift becomes greater than 180° at certain frequencies in the passband, the phase margin requirement at unity gain is met. This operational amplifier response will have slow settling times because of all the pole-zero doublet pairs that are present in the pass-band. In general, such type of behavior is highly undesirable.

This type of operational amplifier could possibly be used for certain applications nevertheless. For example in audio amplifier, the useful band is limited to about 20 KHz and a high loop gain due to multi-staging with conditional stability could be useful to achieve low distortion figures.

3.2 Closed-Loop Frequency Response

Feedback Amplifiers

This section discusses operational amplifiers in closed-loop configurations and shows how they must be compensated to ensure stability and good settling characteristics. Before discussing compensation techniques, some properties of closed-loop feedback amplifiers will be reviewed.

Figure 3.3 represents feedback circuit in which $A(s)$ represents the open-loop transfer function of the amplifier and $\beta(s)$ represents the feedback transfer function. The fed back signal is subtracted from the input signal, and the resulting error signal is applied to the forward amplifier. For a negative feedback configuration, the closed-loop transfer function is

$$A_{CL}(s) = \frac{A(s)}{1 + \beta(s)A(s)} \tag{3.5}$$

Neglecting frequency dependent terms for simplicity gives

$$A_{CL} = \frac{A}{1 + \beta A} \tag{3.6}$$

The term $T_0 = \beta A$ is called the loop gain and is presented in Figure 3.4. Negative feedback is less to reduce the DC gain by $(1 + T_0)$ and increase the bandwidth by the same factor. Figure 3.4(b) represents the simple pole-zero root-locus versus T_0. As the closed-loop gain is reduced, the dominant pole P_1 moves to correspondingly higher frequencies resulting in increased bandwidth.

Another way of representing at the open-loop transfer function

$$A(s) = \frac{Z(s)}{P(s)} \tag{3.7}$$

where Z(s) and P(s) correspond to the zeros and poles of $A(s)$, respectively. The closed-loop response becomes

$$A_{CL}(s) = \frac{\frac{Z(s)}{P(s)}}{1 + \frac{\beta Z(s)}{P(s)}} = \frac{Z(s)}{\beta Z(s) + P(s)} \tag{3.8}$$

Note that the closed-loop poles are determined by both the open-loop poles and zeros. The analysis motivates the use of gain and phase margins as stability metrics. In

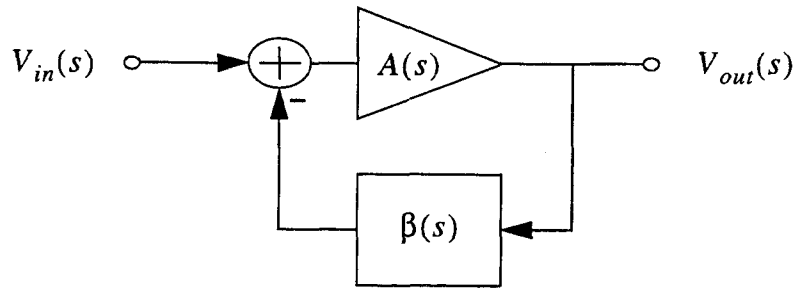

Figure 3.3. Block diagram of a negative feedback system.

most cases, the unity-gain configuration ($\beta = 1$) is chosen to determine performance since it represents the worst-case for stability. In other words, $\beta = 1$ corresponds to the minimum phase and gain margins specified. It is also important to examine performance with $\beta > 1$.

Transient Response

The transient response and settling-time performance of integrated amplifiers are important design parameters. For example, in switched-capacitor circuits, the charge from one or more capacitors must be transferred to a feedback capacitor within half a clock period. The settling time is the time needed for an amplifier to reach a specified percentage of its final value for a step input.

The settling time response consists of two components: linear and nonlinear settling. Figure 3.5 presents the unity-gain linear and nonlinear settling time characteristics. The linear settling-time portion is due to the finite unity-gain frequency and phase characteristics of the amplifier; it sets a minimum value for the overall settling time. The non-linear settling time is due to slew-rate limiting and is strongly dependent

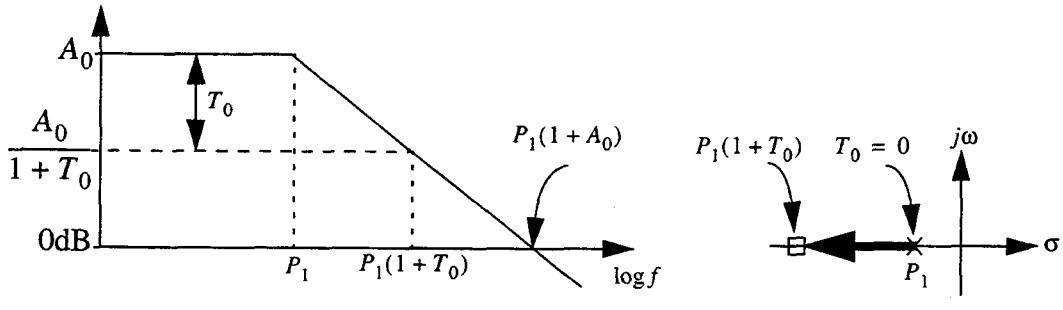

Figure 3.4. Frequency response of a one-pole feedback amplifier. (a) Magnitude plot. (b) Root-locus plot.

on the output step size. In this chapter, only linear settling time is considered by modeling the amplifier with finite gain and bandwidth. From Figure 3.5, it can be seen that the final value or the settling accuracy of the amplifier is

$$SA = V_{pk-pk}\left(1 - \frac{1}{A_0}\right) \tag{3.9}$$

where A_0 is the open-loop voltage gain. Another way of specifying the settling accuracy

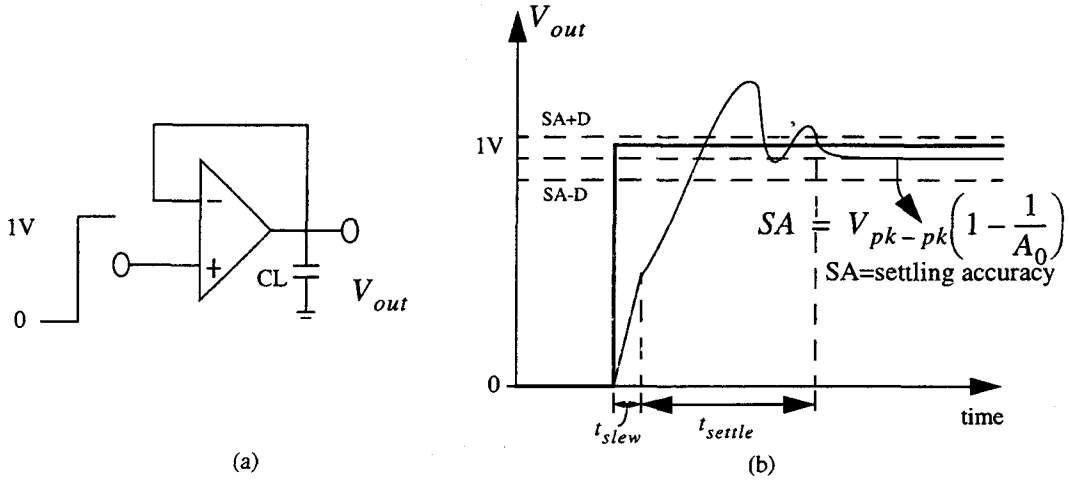

Figure 3.5. (a) Unity feedback configuration. (b) step response of the amplifier.

is to note that each binary digit in a digital system is equivalent to 6 dB. The equivalent number of bits of gain accuracy can be determined as

$$B = \frac{A_0(dB)}{6_{dB/bit}} \tag{3.10}$$

For example, 120 dB DC gain corresponds to 20 bits of gain accuracy. The maximum settling accuracy can be defined as

$$SA = V_{p-p}\left(1 - \frac{1}{2^B}\right) \tag{3.11}$$

From Figure 3.4, we saw the frequency response of a one pole amplifier with the corresponding phase margin of 90°. Since its characteristic root is at $s = -P_1$ the system is stable and has an exponential time response; the steady-state term is inversely proportional to gain. The linear settling time associated with this amplifier is related to the dominant RC time constant multiplied by the loop-gain. To determine settling time, consider a one-pole transfer function:

$$a(s) = \frac{a_0}{\left(\frac{s}{\omega_p} + 1\right)} \tag{3.12}$$

Evaluating (3.12) in unity-gain ($\beta = 1$), we get

$$A(s) = \frac{a_0}{\frac{s}{\omega_p} + (1 + a_0)} \tag{3.13}$$

Applying a unit-step input to (3.13), we obtain

$$V_{out}(s) = \frac{1}{s}A(s) = \frac{1}{s} \cdot \frac{a_0}{\frac{s}{\omega_p} + (1 + a_0)} = \frac{K_1}{s} + \frac{K_2}{\frac{s}{\omega_p} + (1 + a_0)} \tag{3.14}$$

The associated time response of (3.14) is

$$V_{out}(t) = K_1 u(t) + K_2 e^{-\omega_p(1 + a_0)t} \tag{3.15}$$

Equation (3.15) represents an exponential natural response with a time constant inversely proportional to the unity-gain frequency ω_u.

3.3 Operational Amplifier Transient Modeling

In the previous section, we considered basic settling time and DC accuracy characteristics of a one-pole amplifier. In this section, we higher order systems which leads us towards modeling multi-stage amplifiers. We begin by reviewing some characteristics of second-order systems [7]. If first- and second-order systems are well understood, the behavior of higher-order systems follows.

Consider the following second-order transfer function

$$T(s) = \frac{N(s)}{D(s)} = \frac{b_1 s + b_0}{s^2 + a_1 s + a_0} \tag{3.16}$$

The denominator D(s) of T(s) is the characteristic polynomial whose roots must all lie in the left half-plane to force the natural response terms to decay to zero. Both a_0 and a_1 must be greater than zero for stability. D(s) can be presented in factored form as

$$D(s) = s^2 + a_1 s + a_0 = (s + s_1)(s + s_2) \tag{3.17}$$

with roots

$$s_1, s_2 = \frac{-a_1 \pm \sqrt{(a_1^2 - 4a_0)}}{2} \tag{3.18}$$

Overdamped Response

If s_1 and s_2 are real and distinct, the output response to an applied step input can be written as

$$V_{out}(s) = \frac{K_1}{s} + \frac{K_2}{s + s_1} + \frac{K_3}{s + s_2} \tag{3.19}$$

which in the time domain corresponds to

$$V_{out}(t) = K_1 u(t) + K_2 e^{-s_1 t} + K_3 e^{-s_2 t} \tag{3.20}$$

From (3.20) it is evident that the exponential term with the larger time-constant (lowest frequency pole) dominates the settling time.

Underdamped Response

If the roots of D(s) are complex conjugates

$$s_1, s_2 = -a \pm j\omega \tag{3.21}$$

thus the transfer function can be written as

$$T(s) = \frac{b_1 s + b_0}{s^2 + a_1 s + a_0} = \frac{b_1 s + b_0}{(s + a - j\omega)(s + a + j\omega)} = \frac{b_1 s + b_0}{(s + a)^2 + \omega^2} \tag{3.22}$$

corresponding to an output response of

$$V_{out}(t) = u(t)[Ke^{-at}\cos(\omega t + \theta)] \tag{3.23}$$

Underdamped second-order systems have a natural response that is described by a frequency of oscillation ω and an exponential constant a. For an underdamped second-order system, a more useful form uses the undamped natural frequency ω_n and the damping ratio ζ :

$$s^2 + a_1 s + a_0 = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{3.24}$$

The quantities above are related as

$$a = \zeta\omega_n \tag{3.25}$$

and

$$\omega = \omega_n\sqrt{1 - \zeta^2} \tag{3.26}$$

For ζ between 0 and 1, the characteristic roots lie in the Left-Half Plane (LHP) on a circle of radius ω_n centered at the origin as shown in Figure 3.6. For $\zeta = 0$ the roots are on the imaginary axis, and for $\zeta = 1$ both roots are on the negative real axis. The undamped natural frequency ω_n is that at which oscillations would occur if ζ were zero. The damping ratio is related to the damping angle ϕ in Figure 3.6 by

$$\zeta = \cos\phi \tag{3.27}$$

Two-Pole Amplifier Response

In this section, we explore the behavior of the second-order transfer function applied to a two-stage amplifier compensated using only a capacitor rather than an RC network. Later, the effects of using RC compensation will be studied. From the previous discussions, we know that a single pole response gives a 90° phase margin which is more than sufficient for stability. By introducing a non-dominant pole, we can shape the

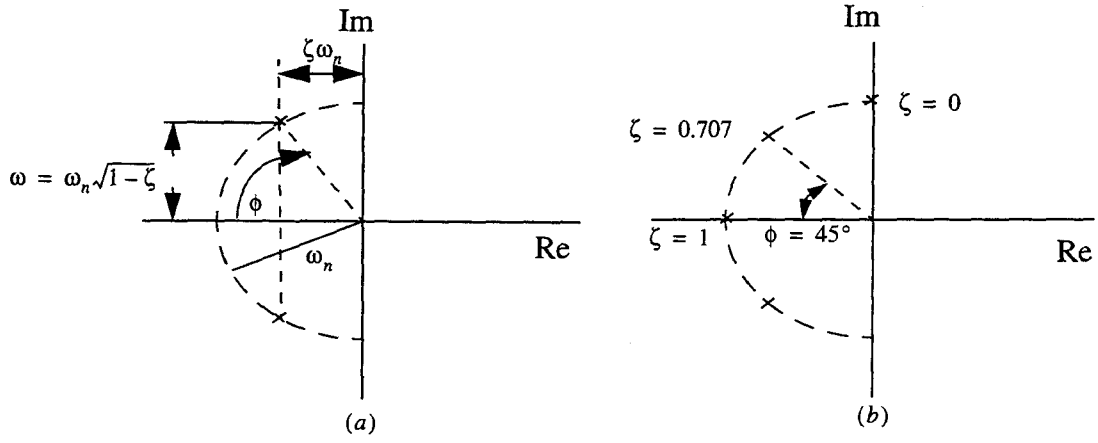

Figure 3.6. (a) Second-order system parameters. (b) Damping ratios corresponding to various root locations.

frequency response to achieve the desired phase and gain margins and minimum settling time.

We will first model the amplifier as a two-pole system knowing the open-loop gain and unity-gain frequency, the dominant pole frequency can be determined. Furthermore, by varying the non-dominant pole in the vicinity of the unity-gain frequency, the characteristics of the amplifier in terms of phase margin, gain margin, and settling time can be explored. This analysis will also help us visualize the movements of poles and zeros with respect to amplifier characteristics in the open and closed-loop configurations.

The open-loop transfer function of a two-stage amplifier is

$$a(s) = \frac{a_0}{\left(\frac{s}{P_d}+1\right)\left(\frac{s}{P_n}+1\right)} \tag{3.28}$$

where a_0 is the low-frequency gain (V/V), P_d, and P_n are the dominant and non-dominant poles, respectively. According to the Bode plot of Figure 3.1 and equation (3.3), in a one-pole system the unity-gain frequency is proportional to the dominant-pole frequency and the finite gain of the amplifier

$$f_u = f_d \times A \tag{3.29}$$

or

$$f_d = \frac{f_u}{a_0} \tag{3.30}$$

Equivalently, the gain is related to a dominant pole frequency as

$$f_d = \frac{f_u}{10^{A_{(dB)}/20}} \tag{3.31}$$

For example, if a bandwidth of 100 MHz with a gain of 120 dB is desired, the dominant pole of the amplifier must be placed at 100 Hz.

The unity-gain transfer function corresponding to (3.28) is

$$A(s) = \frac{a_0}{\frac{s^2}{P_d P_n} + s\left(\frac{1}{P_d} + \frac{1}{P_n}\right) + (1 + \beta a_0)} \tag{3.32}$$

We can study the effects of the non-dominant pole on the characteristics of the amplifier using (3.28) and (3.32) in MATLAB simulations [8]. By fixing the open-loop gain and the dominant pole frequency with respect to f_u, we can vary the non-dominant pole frequency and observe the characteristics of the amplifier. When the non-dominant pole approaches $-\infty$ of the s-plane, a 90° phase margin or a one-pole response is observed as expected. Since the transfer function in (3.32) is of second-order, the simulated unity-gain frequency is less than the exact frequency calculated from (3.29), but it approaches exponentially the desired frequency as $P_n \rightarrow -\infty$.

The analysis can be made more general by normalizing the settling time and the unity-gain frequency to the time constant associated with the desired unity-gain frequency. We can express the normalized settling time as

$$T_{sn} = \frac{T_s}{T_u} \tag{3.33}$$

where

$$T_u = \frac{1}{2\pi f_u} \tag{3.34}$$

The location of the non-dominant pole can be normalized to the desired unity-gain frequency as

$$P_n = \frac{f_n}{f_u} \tag{3.35}$$

Figure 3.7 shows the results of MATLAB simulations of (3.28) and (3.32) for gain accuracies of a_0=120 dB and f_u=100 MHz. For more accurate results based on minimum settling time refer to Appendix A. Figure 3.7(a) shows normalized settling times for 0.0001%, 0.001%, 0.01%, and 0.1% settling accuracies which correspond to

120 dB, 100 dB, 80 dB, and 60 dB gain accuracies, respectively. Note that the settling

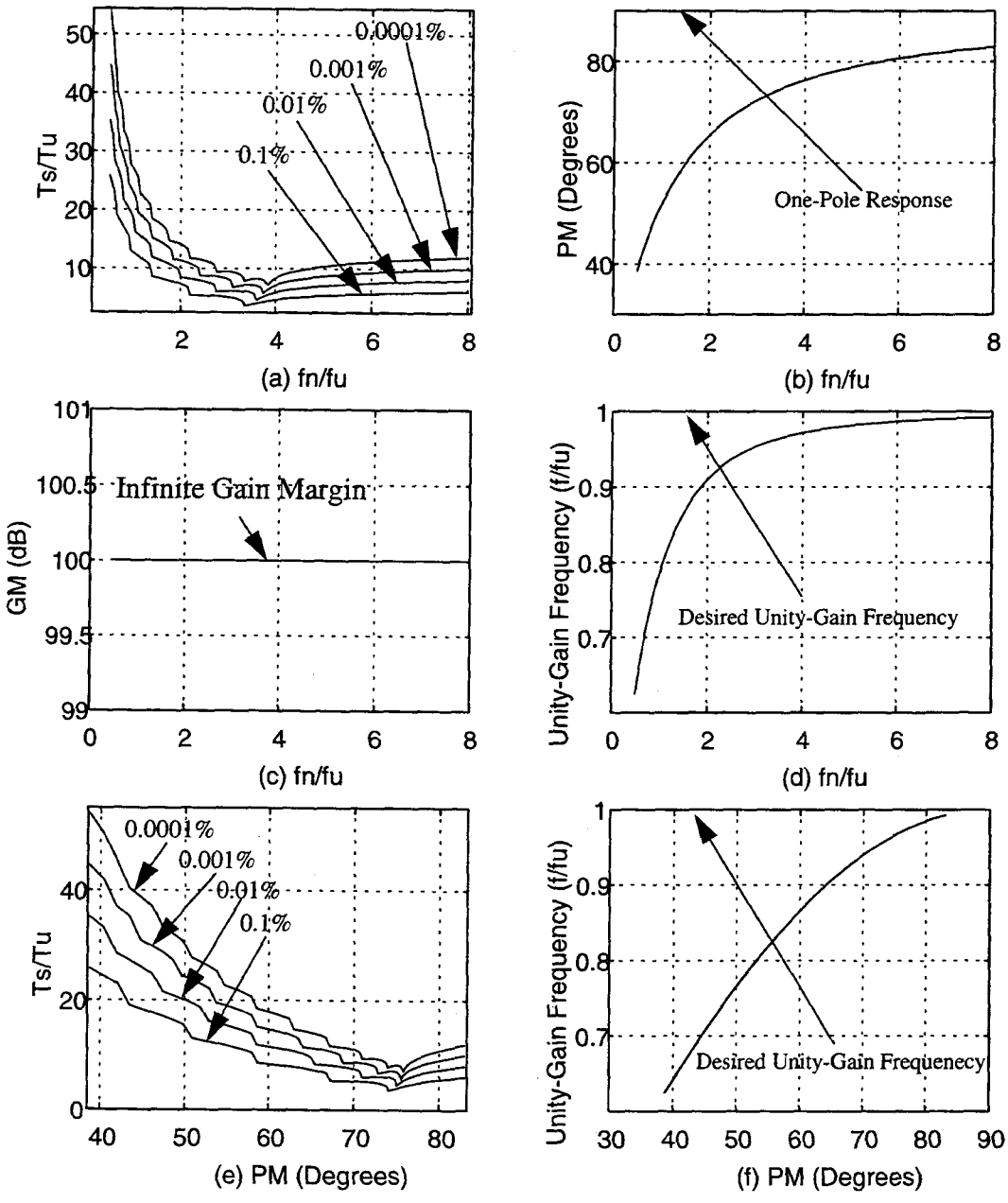

Figure 3.7. Two-pole operational amplifier for 0.0001%, 0.001%, 0.01%, and 0.1% settling accuracy. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time as versus of phase margin. (f) Unity-gain frequency versus of phase margin.

time at first decreases as the non-dominant pole P_n moves towards higher frequencies, and that there is an optimum settling time with the non-dominant pole P_n between $3.3 \times f_u$ and $3.8 \times f_u$; according to Figure 3.7(e), the corresponding optimum phase margins lie between $73°$ and $76°$. Also, note that beyond the optimum points, the settling times increase and approach one-pole responses as $f_n / f_u \to \infty$.

Figure 3.7(b) shows the unity-gain phase margin versus location of the non-dominant pole. As it moves to higher frequencies, the phase margin approaches $90°$. Figure 3.7 gives important results in for the phase margins and needed to obtain minimum settling times. Note that since the maximum total phase shift of a two-pole system is $180°$, the gain margin is infinite as seen in Figure 3.7(c).

Note from Figures 3.7(d) and (f) the normalized unity-gain frequency does not reach the desired f_u, but approaches it exponentially as $f_n / f_u \to \infty$. For example, for a $75°$ phase margin, the measured unity-gain frequency is only about $0.96 \times f_u$.

One should also notice that as we increase the settling accuracy, it takes longer to settle which depends on the damping factor. Increasing the damping factor results in higher phase margins at higher accuracy levels. From Figure 3.7(e), we can see that the phase margin for the optimum settling at 0.0001% is a higher than for 0.1% accuracy [9].

It is important to consider the movement of the poles after closing the feedback loop. We saw from (3.8) that the poles of the open-loop transfer function are added to the numerator zeros multiplied by the return ratio β. Figure 3.8(a) shows the root-locus versus β which corresponds to the pole-zero locations before and after feedback. Note that as the closed-loop gain is reduced for to β values between 0 to 1, the poles of the amplifier form a complex conjugate pair.

Figure 3.8(b) shows the step responses for $52°$, $65°$, $72°$, and $76°$ phase margins, and corresponding damping ratios of 0.5, 0.707, 0.87, and 1.00, respectively.

Combining Figures 3.7 and 3.8, we can understand the transient behavior of a compensated two-stage operational amplifier. However, it is important to note that the behavior of the two-stage amplifier has been idealized. We have not yet considered the use of RC compensation and the pole-zero doublet usually associated with it. Later on, we will review the effects of doublets on settling characteristics.

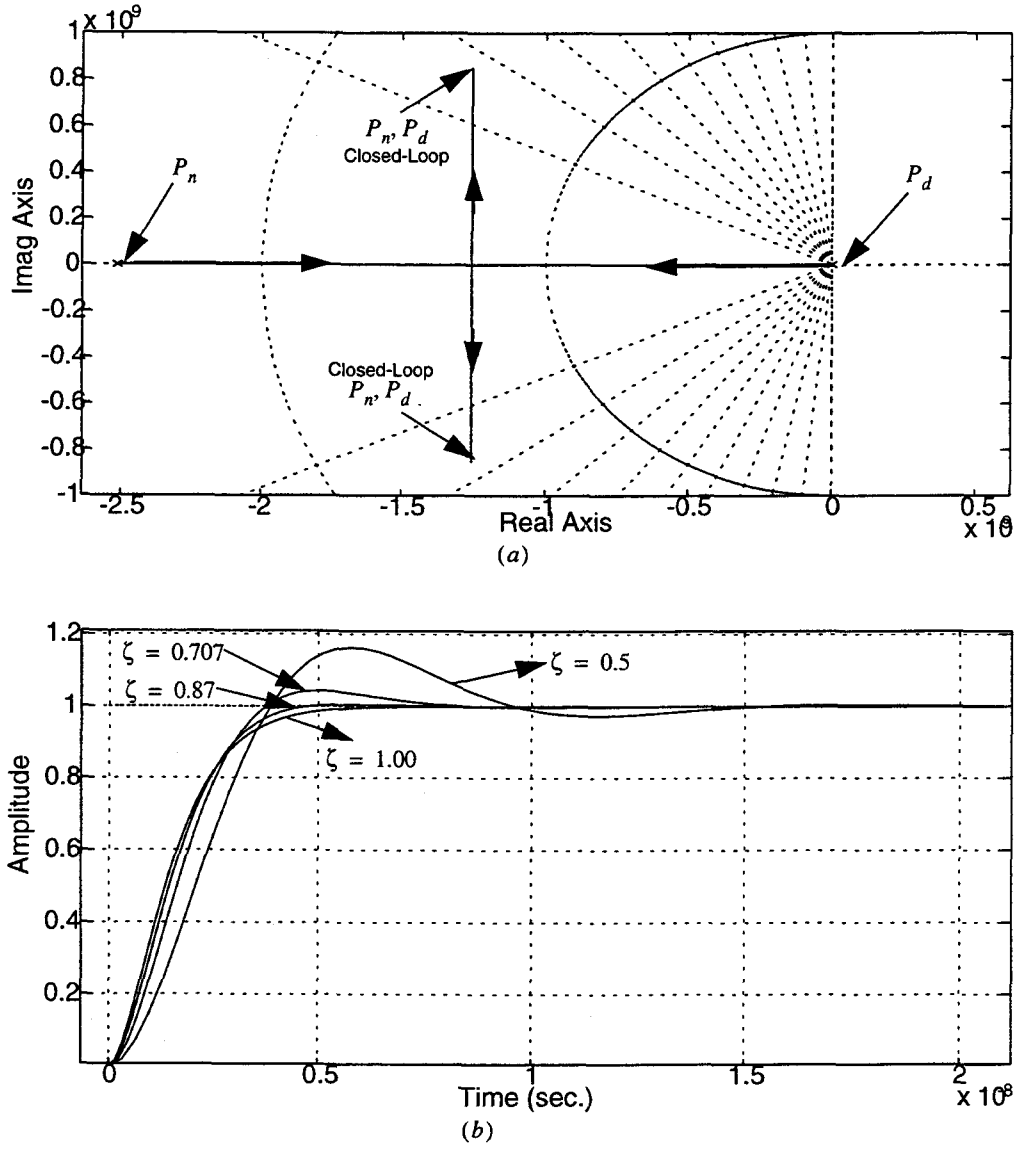

Figure 3.8. (a) Root-locus plot. (b) Step response for various damping ratios.

Three-Pole Amplifier Response

Two-stage amplifiers are well known and their characteristic responses have been published. In this thesis, we wish to compare multi-stage amplifier performance to that of the two-stage amplifiers.

We will initially assume that the amplifier is compensated with a single-pole response to unity-gain. A pole placement model that will be used for the three-pole amplifier is drawn in Figure 3.9; P_d is the dominant pole, P_{n_1}, and P_{n_2} are a complex conjugate pair formed from to the non-dominant pole and the pole associated with the RC compensation network. Chapter 4 will describe these pole-zero formations in details

In Figure 3.9, the dominant pole is placed according to the DC gain and desired

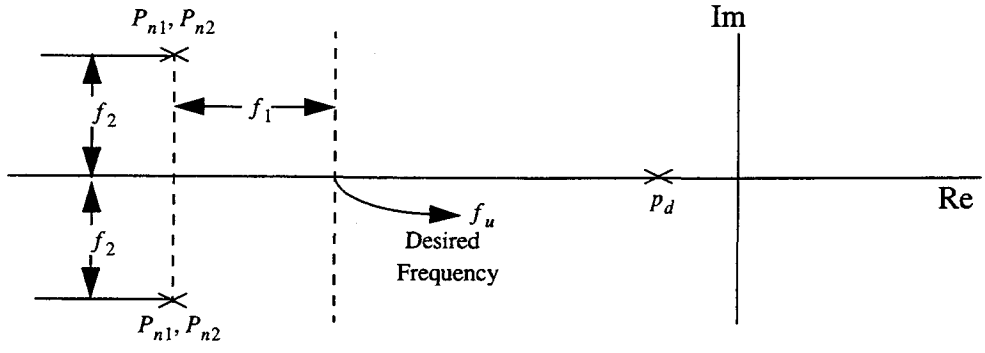

Figure 3.9. Three-pole system open-loop pole-zero plot.

unity-gain frequency. Important factors in Figure 3.9 are the distances represented from the complex pair to f_u; namely, f_1 and f_2 as shown. f_1 represents the real axis distance normalized to f_u, and f_2 represents the imaginary distance also normalized to f_u in the simulations.

Begin by considering the open-loop transfer function of a three-pole amplifier

$$a(s) = \frac{a_0}{\left(\frac{s}{P_d}+1\right)\left(\frac{s}{P_{n1}}+1\right)\left(\frac{s}{P_{n2}}+1\right)} \tag{3.36}$$

where P_{n_1} and P_{n_2} are a complex conjugate pair. (3.36) can also be written as

$$a(s) = \frac{a_0}{\left(\frac{s}{P_d}+1\right)\left(\frac{s^2}{P_{n1}P_{n2}}+s\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+1\right)} \tag{3.37}$$

Multiplying the roots in (3.36), we get

$$a(s) = \frac{a_0}{\left(\frac{s^3}{P_dP_{n1}P_{n2}}+s^2\left(\frac{1}{P_d}\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+\frac{1}{P_{n1}P_{n2}}\right)+s\left(\frac{1}{P_d}+\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+1\right)} \tag{3.38}$$

Now in a negative feedback configuration, (3.38) becomes

$$A(s) = \frac{a_0}{\frac{s^3}{P_dP_{n1}P_{n2}}+s^2\left(\frac{1}{P_d}\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+\frac{1}{P_{n1}P_{n2}}\right)+s\left(\frac{1}{P_d}+\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+(1+\beta a_0)} \tag{3.39}$$

Using (3.38) and (3.39), we can study the effects of the complex conjugate pair by simulating in MATLAB for $\beta = 1$. Simulations are performed for constant a_0 and f_u; P_d is determined using (3.29). As before, the settling times and unity-gain frequencies are normalized with respect to f_u.

The three-pole response gives a two variable simulation; namely, f_1 and f_2. First f_1 is varied over a range proportional f_u with f_2 constant. Next, f_2 is varied with f_1 constant.

The characteristic responses of the three-stage amplifier are shown in Figure 3.10 for 0.0001% settling accuracy. The plots for 0.001%, 0.01%, and 0.1% are similar except for a shift in settling time and are not shown here. For minimum settling times for 0.0001%, 0.001%, 0.01%, and 0.1% accuracy, refer to Appendix B. Note in each figure that there are five traces. Since the three-pole response is a two-variable system, f_1 is placed on the x-axis, and five values of f_2 ; namely, correspond f_{21}, f_{22}, f_{23}, f_{24}, and f_{25}. f_2 corresponds to imaginary component and is normalized f_u simulated with the following ratios

$$f_{21} = 1.0 \times f_u \tag{3.40}$$

$$f_{22} = 1.5 \times f_u \tag{3.41}$$

$$f_{23} = 2.0 \times f_u \tag{3.42}$$

$$f_{24} = 2.5 \times f_u \tag{3.43}$$

and

$$f_{25} = 3.0 \times f_u \tag{3.44}$$

We can analyze Figure 3.10 to determine the effects of the relative positions of the complex conjugate pair on the desired unity-gain frequency f_u. Figure 3.10(a) presents the settling time versus normalized f_1 and f_2 values. Note that the optimum settling time associated with each f_2 value is different and tends to occur at lower f_1 values as f_2 is increased. However, when f_2 is approximately greater than $3f_u$, the settling time curve does not have a global minimum as in other cases. Also, we see that the minimum settling time associated with it is at least 1.6 time constants greater than other global minimum settling times. This tells us that if f_2 becomes too large, we cannot achieve fast settling times. By looking closely at Figure 3.10, the optimum value of f_2 is equal or less than $f_{24} = 2.5 \times f_u$. Refer to Appendix B for more detailed

results. Note that for this particular frequency on the $j\omega$ axis, the minimum settling time

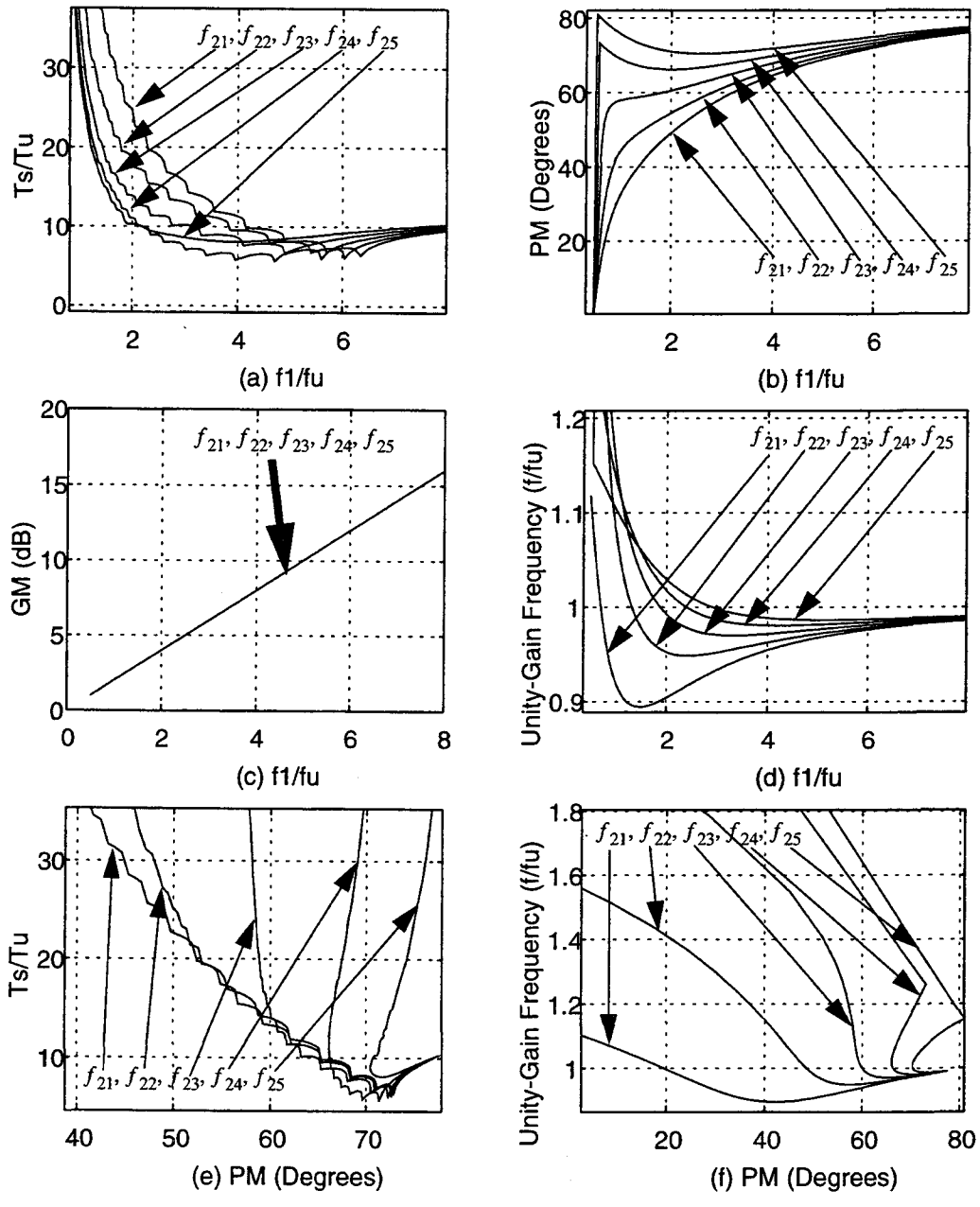

Figure 3.10. Three-pole system for 0.0001% accuracy. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time as versus phase margin. (f) Unity-gain frequency versus phase margin.

occurs with f_1 values that are achievable with known compensation topologies. We are interested in placing the complex poles not too far above the unity-gain frequency f_u so that the associated compensation capacitor does not become excessively large for high f_1 values. If the compensation capacitor becomes large, the g_m of the driver transistor must also increase to maintain a constant gain-bandwidth product. On the other hand, if the complex conjugate pair is close on the real axis, the f_1 values associated with the minimum settling time shift towards higher frequencies making it more difficult to obtain optimum settling with practical capacitor values.

Figure 3.10(b) presents the phase margin as a function of f_1. Notice that for the f_{23}, f_{24}, and f_{25} curves, phase margin is large at low f_1 frequencies. For the case of $f_{25} = 3.0 \times f_u$, the phase margin in Figure 3.10(b) is higher than $70°$ resulting in an over-damped response versus f_1.

Figure 3.10(c) presents the gain margin (GM) as a function of f_1; it is an important stability parameter when the system has more than two poles. As discussed earlier, the gain margin for a two-pole amplifier is infinite since it has a maximum total phase shift of $180°$. However, for higher-order systems, the total phase shift exceeds $180°$, and as a result, we must consider the gain margin. In practice, a minimum gain margin is 10-12 dB. From Figure 3.10(c), we see that the gain margin traces are identical for all cases of f_2. The value of f_2 does not effect the gain margin since it depends only on the gain of the amplifier when the total phase shift is $180°$. Note that for GM>10 dB, f_1 must be about $5.2 \times f_u$. From this result, it is essential that $f_{24} = 2.5 \times f_u$; the minimum settling time with the required gain margin is not easily achievable. Another candidate for minimum settling time with acceptable gain margin is $f_{23} = 2.0 \times f_u$.

We can now see the trade-offs between the settling time and the required gain margin when using the smallest possible f_1 values.

Figure 3.10(d) presents the actual normalized unity-gain frequency as a function of f_1. For small f_1 values, the unity-gain frequency is much larger than f_1! Although this choice also provides a good phase margin, one must be cautious of long settling times with these low f_1 values.

Figure 3.10(e) illustrates the settling time versus phase margin. We conclude that while for the case of two-stage amplifiers, the optimum phase margin lies between 73° and 77°, for three-stage amplifiers, the optimum phase margin lies between 65° and 72°. One should avoid phase margins below this range because, settling time increases dramatically.

Figure 3.10(f) illustrates actual normalized unity-gain frequency versus phase margin. It is important to notice that for phase margins between 65° and 72° associated with fast settling times, the unity-gain frequency approaches its desired value as was the case for the two-stage amplifier. Also notice that as the phase margin is further increased, the plots for different f_2 values fold back around the desired frequency.

In Figure 3.9, we considered the locations of the poles of the open-loop transfer function of a compensated three-stage amplifier. Next, investigate the locations of the poles in the closed-loop feedback configuration as a function of the return ratio (β). We expect the dominant pole in the two-stage or one-stage amplifier to move towards f_u. In the case of a three-stage amplifier, the separation on the $j\omega$ axis of the complex conjugate pole pair determines the pole movements versus β.

Figure 3.11 defines the general root-locus plot of the three-pole amplifier. Again, depending on the value of f_2, the movement of poles as the gain is reduced is

significant. For example, in the case where $f_2 = 1.0 \times f_u$, it is clear that as the gain is

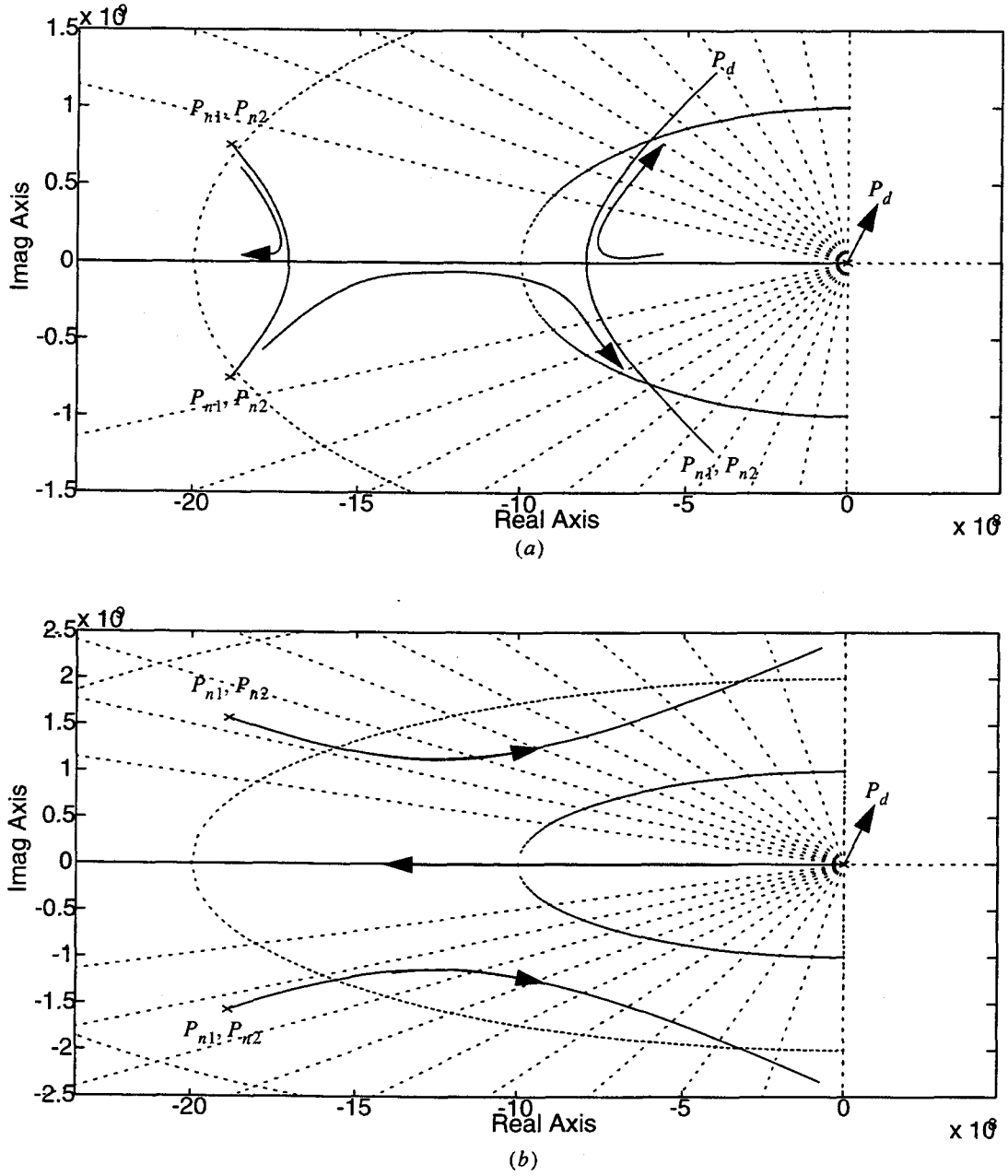

Figure 3.11. (a) Root-locus plot for $f_2 = 1.0 \times f_u$. (b) Root-locus plot for $f_2 = 2.5 \times f_u$.

reduced (β is increased) the original complex conjugate pair becomes real; as one of the

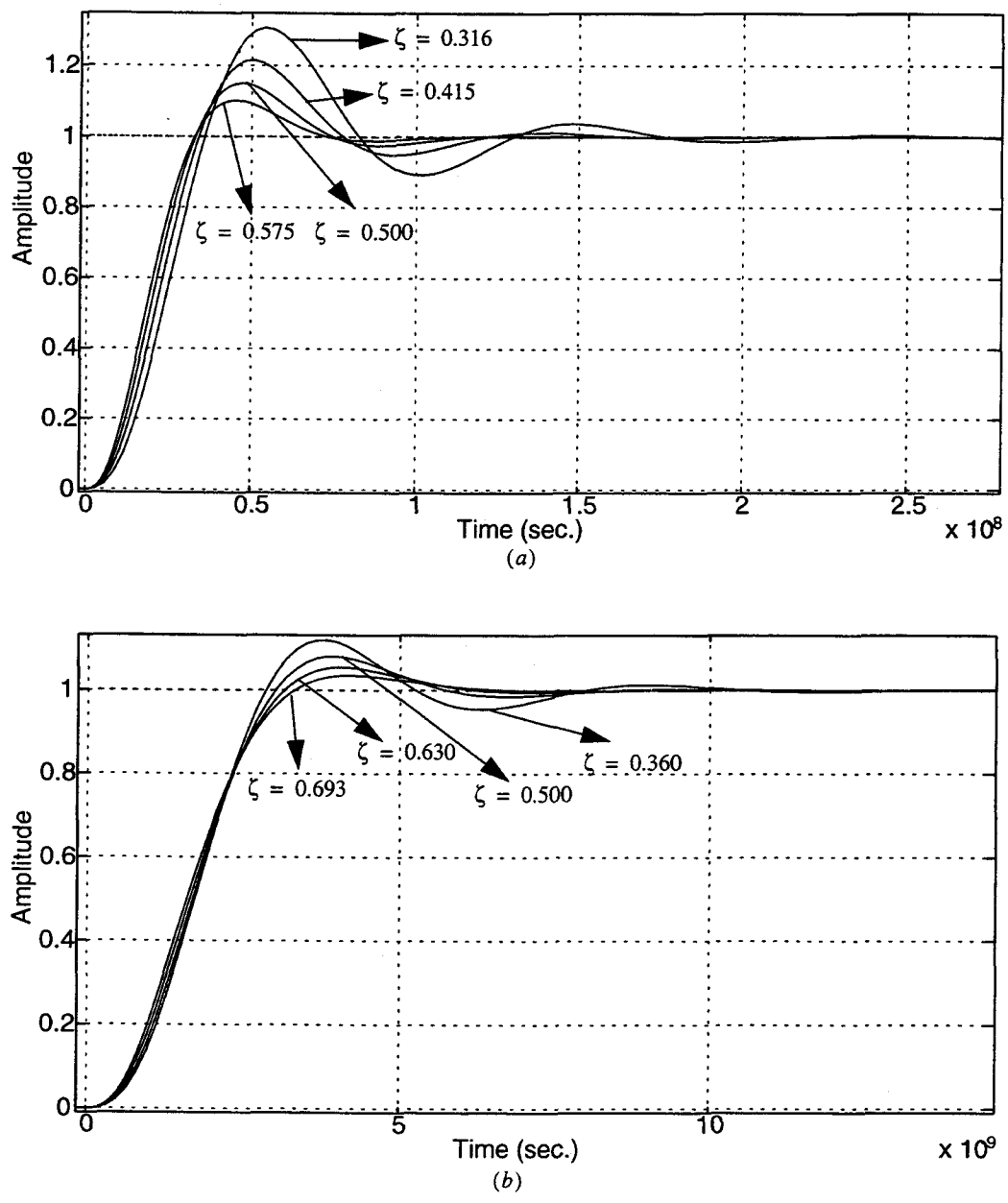

Figure 3.12. Step response plots as a function of f_1. (a) $f_2 = 1.0 \times f_u$. (b) $f_2 = 2.5 \times f_u$.

poles moves towards higher frequencies and the other moves towards the RHP eventually meeting with P_d to form another complex conjugate pair. Note that the new conjugate pair is at a much lower frequency than the original pair. It is clear from plots that if the gain is further reduced, the complex conjugate pairs would eventually cross in the RHP resulting in an unstable amplifier.

Figure 3.12 also illustrates the settling behavior for

$$f_2 = 1.0 \times f_u \tag{3.45}$$

and

$$f_2 = 2.5 \times f_u \tag{3.46}$$

Since for Figure 3.12(a) the complex conjugate pair is fairly close to the real axis, the corresponding settling time is higher than in Figure 3.12(b). Another important result from Figure 3.12 is that as the pole separation of the complex conjugate pair increases, the overshoot decreases and the response becomes increasingly over-damped. On the other hand, if the separation f_2 is too large, the response is over-damped even for low damping factors.

Four-Pole Amplifier Response

The two- and three-stage operational amplifier modeling can be extended to model a four-stage amplifier. The details of modeling such an amplifier are discussed in Chapter 5. For simplicity, we neglect the pole-zero doublet pairs. Furthermore, the amplifier is assumed to have a one-pole response to the unity-gain frequency. A compensated singularity model for a four-stage operational amplifier is shown in Figure

3.13. Compared to the three-pole amplifier model, it contains another pole on the real

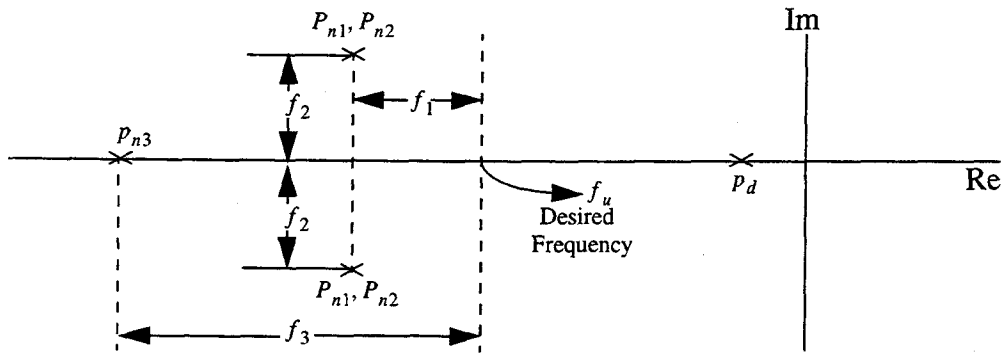

Figure 3.13. Three-pole open-loop system pole-zero plot.

axis at P_{n3}. In this study, and based on previous results, we assume

$$f_2 = 2.0 \times f_u \tag{3.46}$$

In this design, new the variable f_3 and the effects of it on the characteristics of the operational amplifier are studied. Similar to the case of the three-pole model, this is a two variable problem with f_2 fixed. The open-loop transfer function of the four-pole system is

$$a(s) = \frac{a_0}{\frac{s^4}{P_d P_{n1} P_{n2} P_{n3}} + s^3\left(\frac{1}{P_d P_{n1}}\left(\frac{1}{P_{n2}} + \frac{1}{P_{n3}}\right) + \frac{1}{P_{n2} P_{n3}}\left(\frac{1}{P_d} + \frac{1}{P_{n1}}\right)\right) + \\ s^2\left(\frac{1}{P_d P_{n1}} + \frac{1}{P_d P_{n2}} + \frac{1}{P_d P_{n3}} + \frac{1}{P_{n1} P_{n2}} + \frac{1}{P_{n2} P_{n3}}\right) + s\left(\frac{1}{P_d} + \frac{1}{P_{n1}} + \frac{1}{P_{n2}} + \frac{1}{P_{n3}}\right) + 1} \tag{3.47}$$

and the corresponding closed-loop transfer function is

$$A(s) = \frac{a_0}{\frac{s^4}{P_d P_{n1} P_{n2} P_{n3}} + s^3\left(\frac{1}{P_d P_{n1}}\left(\frac{1}{P_{n2}} + \frac{1}{P_{n3}}\right) + \frac{1}{P_{n2} P_{n3}}\left(\frac{1}{P_d} + \frac{1}{P_{n1}}\right)\right) +$$

$$\frac{}{s^2\left(\frac{1}{P_d P_{n1}} + \frac{1}{P_d P_{n2}} + \frac{1}{P_d P_{n3}} + \frac{1}{P_{n1} P_{n2}} + \frac{1}{P_{n2} P_{n3}}\right) + s\left(\frac{1}{P_d} + \frac{1}{P_{n1}} + \frac{1}{P_{n2}} + \frac{1}{P_{n3}}\right) +$$

$$\frac{}{(1 + \beta a_0)} \tag{3.48}$$

The analysis begins by assuming f_1 is constant, and f_3 is varied on the left-half plane. Next, f_1 is changed to a different value and the procedure repeats. The results of the MATLAB simulations are shown in Figure 3.14. For accurate results based on minimum settling times, refer to Appendix C.

Note that each plot in Figure 3.14 has six traces corresponding to six different values of f_1:

$$f_{11} = 1.0 \times f_u \tag{3.49}$$

$$f_{12} = 2.0 \times f_u \tag{3.50}$$

$$f_{13} = 3.0 \times f_u \tag{3.51}$$

$$f_{14} = 4.0 \times f_u \tag{3.52}$$

$$f_{15} = 5.0 \times f_u \tag{3.53}$$

and

$$f_{16} = 6.0 \times f_u \tag{3.54}$$

Note that the values of f_1 beyond f_{13} have very similar settling times as shown in Figure 3.14(a). The settling time decreases exponentially as f_3 approaches higher frequencies or higher phase margins as seen in Figure 3.14(a) and (e). Note that the settling times do

not increase as f_1 approaches higher frequencies as was shown for two- and three-pole

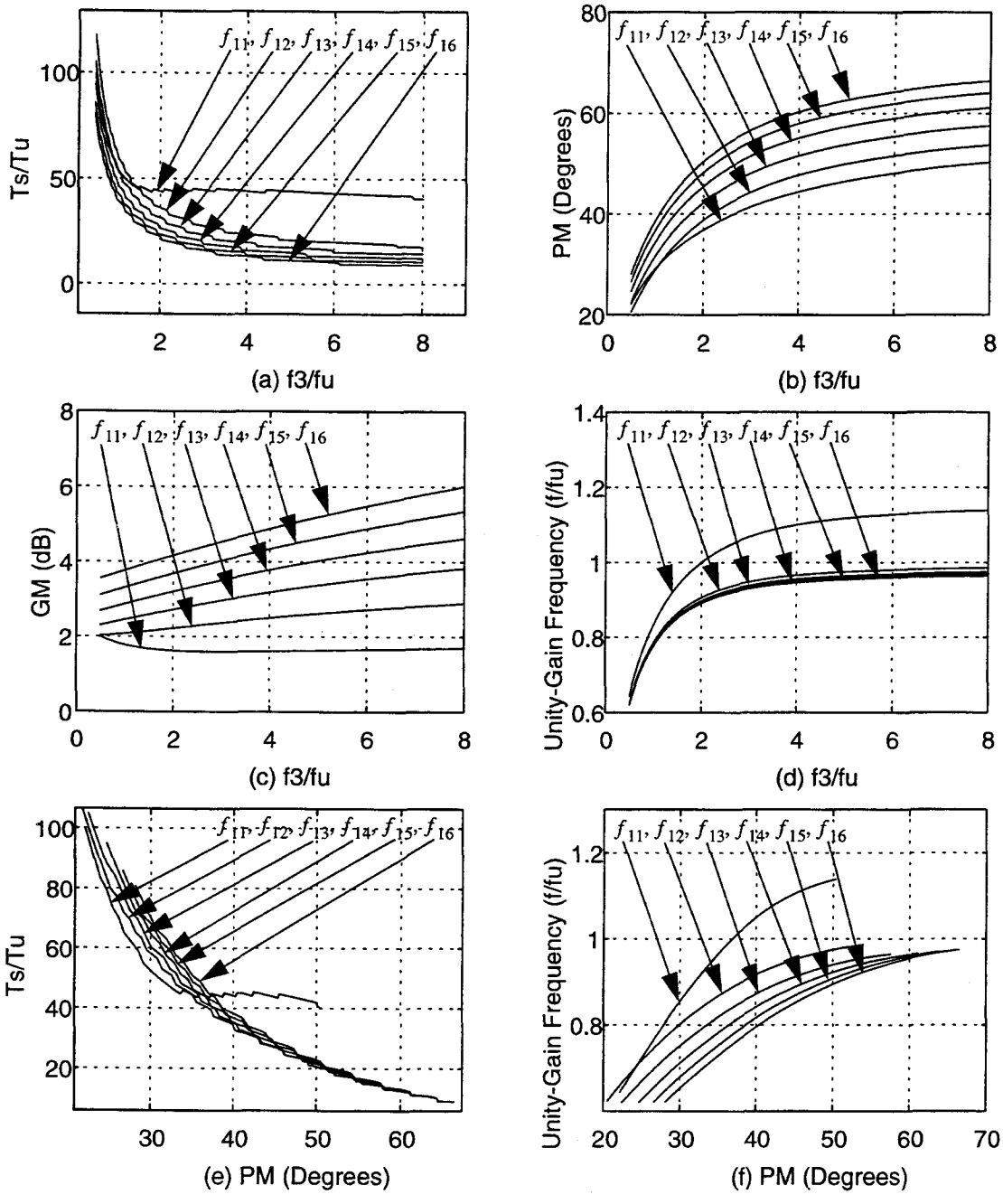

Figure 3.14. Four-pole system for 0.0001% accuracy. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time as versus phase margin. (f) Unity-gain frequency versus phase margin.

models. Note that the simulations were carried out to $f_1 = 8fu$ which is difficult to

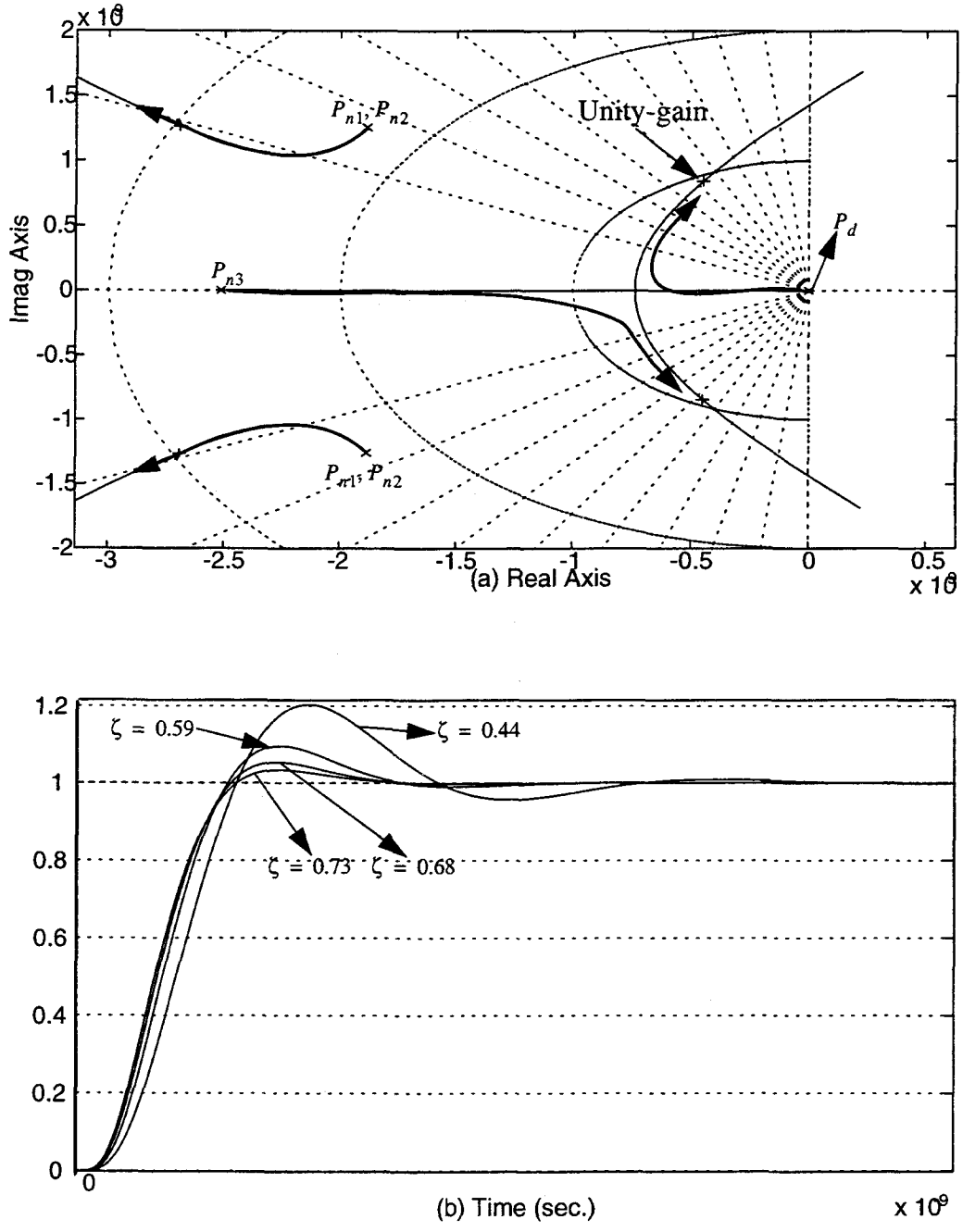

Figure 3.15. (a) Root-locus plot. (b) Step response for various damping ratios corresponding to $f_1 = 5.0 \times f_u$ and $f_1 = 2.0 \times f_u$.

achieve in real circuits. An important result is obtained from these plots. Note that there is not much difference in settling times between traces for $f_1 > 2fu$ which means that the complex conjugate pair P_{n1} and P_{n2} does not have to be placed at high frequencies as was the case in the three-stage design. However, due the increased number of poles, the gain margin is decreased versus f_1 as shown in Figure 3.14(c). In order to obtain for higher gain margins, the complex pair and the third non-dominant pole P_{n3} must be placed at higher frequencies than was simulated. Note that since we are only varying f_1 with f_2 and f_3 constant, we expect behavior close to a two-pole system. The remaining simulation results are seen in Figures 3.14(b), (d), and (f).

It is important to see the pole-zero migrations towards the unity-gain frequency as we close the loop on the amplifier. Since in total, we have four poles including the dominant pole, we would expect that the poles located on the real axis (P_d and P_{n3}) would eventually form a complex conjugate pair. Thus, the amplifier would exhibit two pairs of complex conjugates instead of one as in the two- and three-pole amplifiers. The corresponding root-locus plot of the four-pole amplifier is shown in Figure 3.15(a). An important observation can be made regarding the second complex conjugate pair. The complex conjugate pair forms in the lower frequency range and migrates towards the $j\omega$ axis, whereas the second complex conjugate pair approaches higher frequencies as the loop gain is reduced. Hence the damping ratio corresponding to the step response in Figure 3.15(b) is dominated by the lower frequency pair, and the damping ratio corresponding to the outer pair is close to one. This important result can be obtained by observing the natural frequency which corresponds to the relative distance between the pair and the $j\omega$ axis, slow settling times occur when the poles are close to the $j\omega$ axis.

Effect of Return-Ratio on Settling Time

As mentioned earlier, the closed-loop response of an amplifier can be written as

$$A_{CL}(s) = \frac{A(s)}{1 + \beta(s)A(s)} \tag{3.55}$$

where $\beta(s)$ is the return-ratio. Assuming low frequencies,

$$A_{CL}(s) = \frac{A}{1 + \beta A} \tag{3.56}$$

$\beta = 1$ in (3.56) corresponds to the unity-gain configuration of the amplifier, and $\beta = 0$ represents the open-loop transfer function. Most characteristics of an amplifier are measured either from the open-loop response and/or unity-gain configuration. Figure 3.16 presents the settling time versus β for two- and three-pole amplifiers assuming the positions of the poles are fixed. It is clear that as β increases from 0 to 1, the settling time decays exponentially. The increase in βcorresponds to higher bandwidth, lower gain, and faster settling. Figures 3.16(b) and (d) show settling times for two- and three-stage amplifiers, respectively.

Figures 3.16(a) and (c) show that the settling time decreases exponentially with β. This is true for a fixed phase margin in the unity-gain configuration. However, an important question arises as to the minimum settling time optimum phase margin for other β values. The minimum settling time in Figures 3.7, 3.10, and 3.14 for two-, three-, and four-stage amplifiers, respectively, apply $\beta = 1$. In order to determine the optimum phase margins for different β values, MATLAB simulations were performed; the results for 0.0001%, 0.001%, 0.01%, and 0.1% settling accuracy are shown in Figures 3.17-3.25 for two-, three-, and four-stage amplifiers, respectively. Refer to Appendices D, E, and F for two-, three, and four-stage exact minimum settling times. We first consider the two-stage amplifier responses of Figures 3.18-3.20 for β values of 0.75,

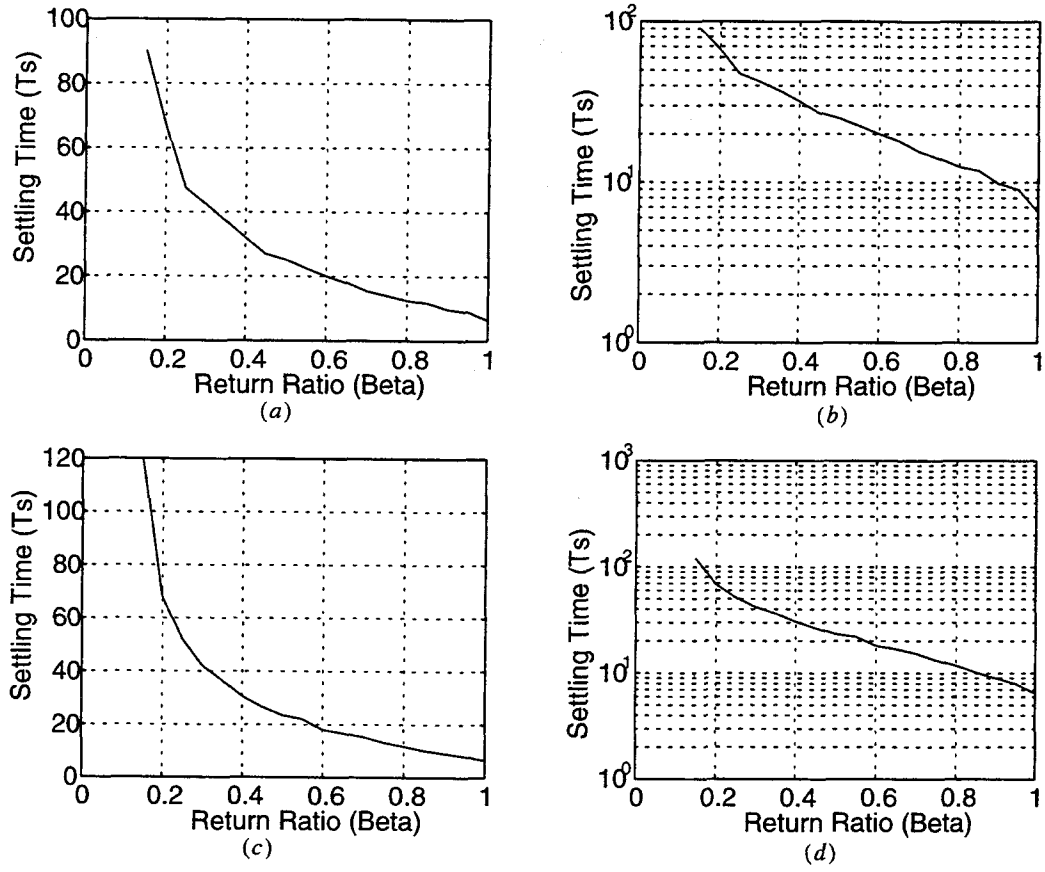

Figure 3.16. Settling time as a function of return ratio β. Two-stage amplifier phase margin at 74.5° , and three-stage amplifier phase margin at 69.5°. (a), (b) Settling time for two-stage amplifier. (c), (d) Settling time for three-stage amplifier.

0.50, and 0.25, respectively. Note that as β decreases, the optimum phase margin also decreases. According to Figure 3.7, for $\beta = 0.25$ the optimum phase margin is $48° - 52°$ rather than $70° - 75°$ for $\beta = 1$. This requires the non-dominant pole to be placed near the desired unity-gain frequency.

For the three-stage amplifiers corresponding to Figures 3.20-3.22, however, the behavior is quite different. Note that for β values less than 1, the minimum settling time

is moved to lower f_1 values compared to $\beta = 1.0$. As β decreases, the settling time becomes nearly constant. However, the optimum phase margin does not significantly change as was the case for the two-stage amplifier. A major draw-back for the three-stage amplifier response is that to get acceptable gain margin, the position of f_1 must remain at high frequencies, effectively not achieving optimum settling times.

Finally, for the four-stage amplifier (Figures 3.23-3.25), we observe that the behavior is close to the two-stage case. Since f_1 and f_2 are kept constant, the behavior is like a two-stage amplifier with f_3 being varied on the real axis. For the case of $\beta = 0.25$, the corresponding optimum phase margin is $38° - 40°$ with f_3 located about 1.5 times the desired unity-gain frequency.

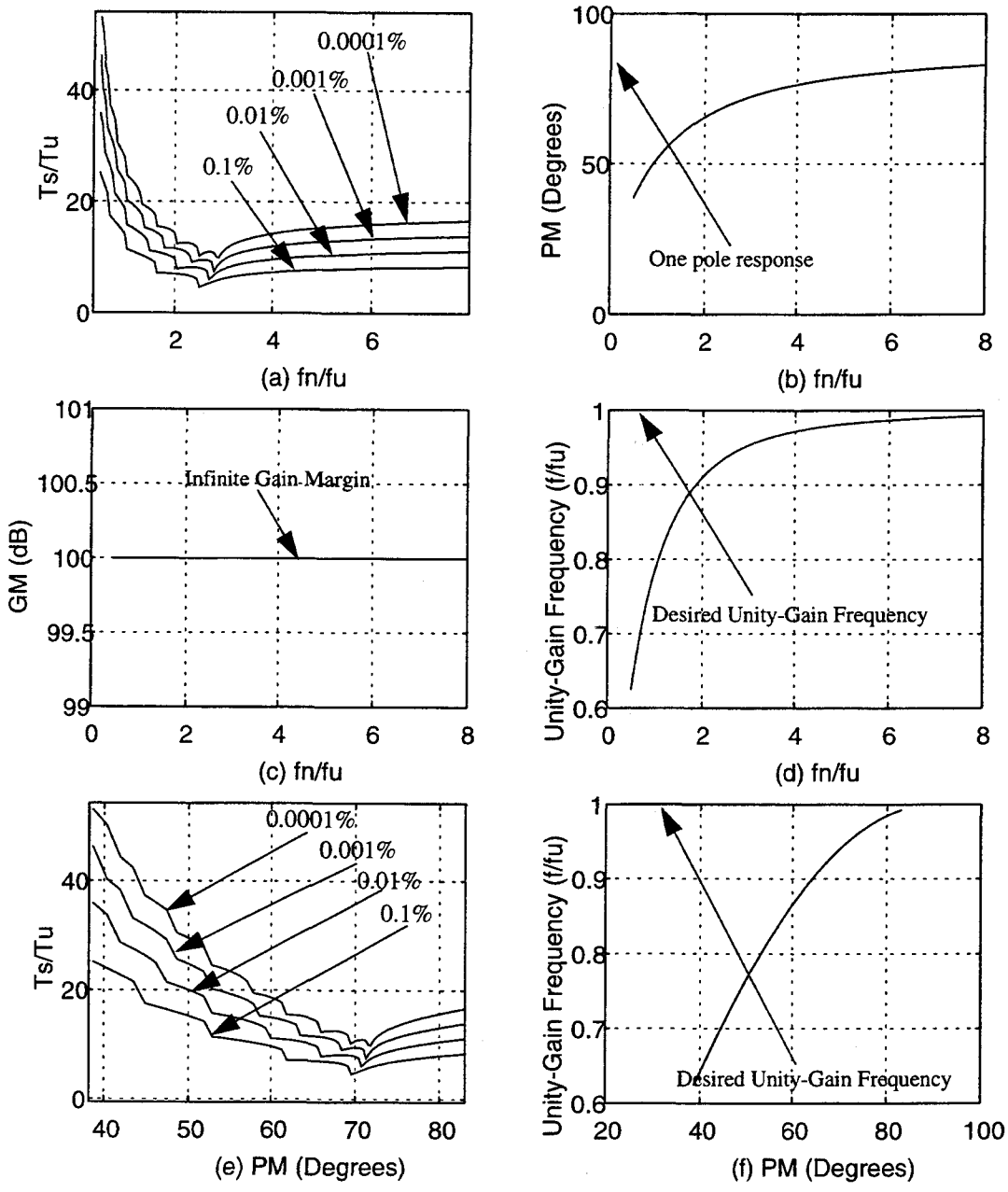

Figure 3.17. Two-stage amplifier with $\beta = 0.75$ for 0.0001%, 0.001%, 0.01%, and 0.1% settling accuracy. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time as versus phase margin. (f) Unity-gain frequency versus phase margin.

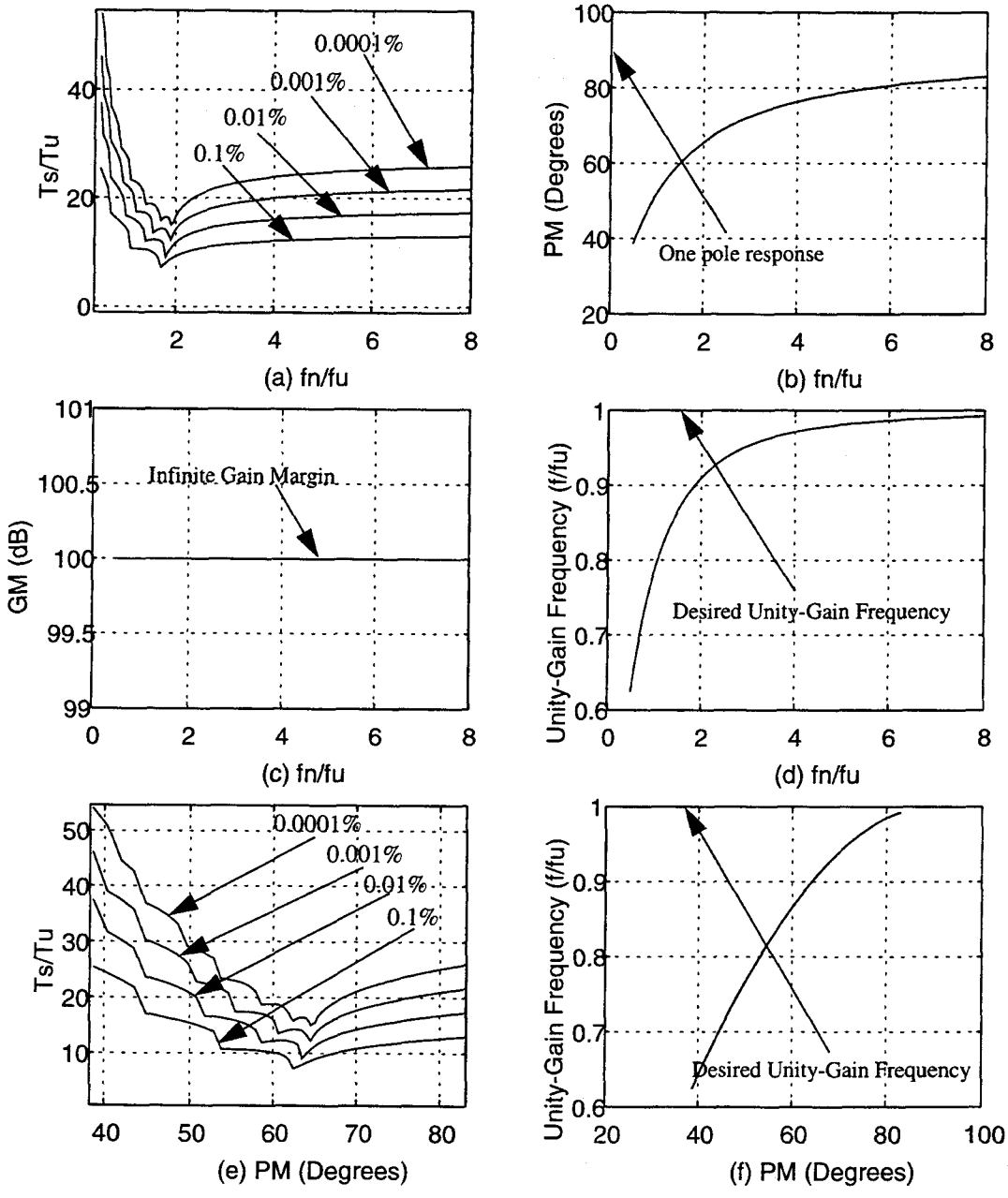

Figure 3.18. Two-stage amplifier with $\beta = 0.50$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

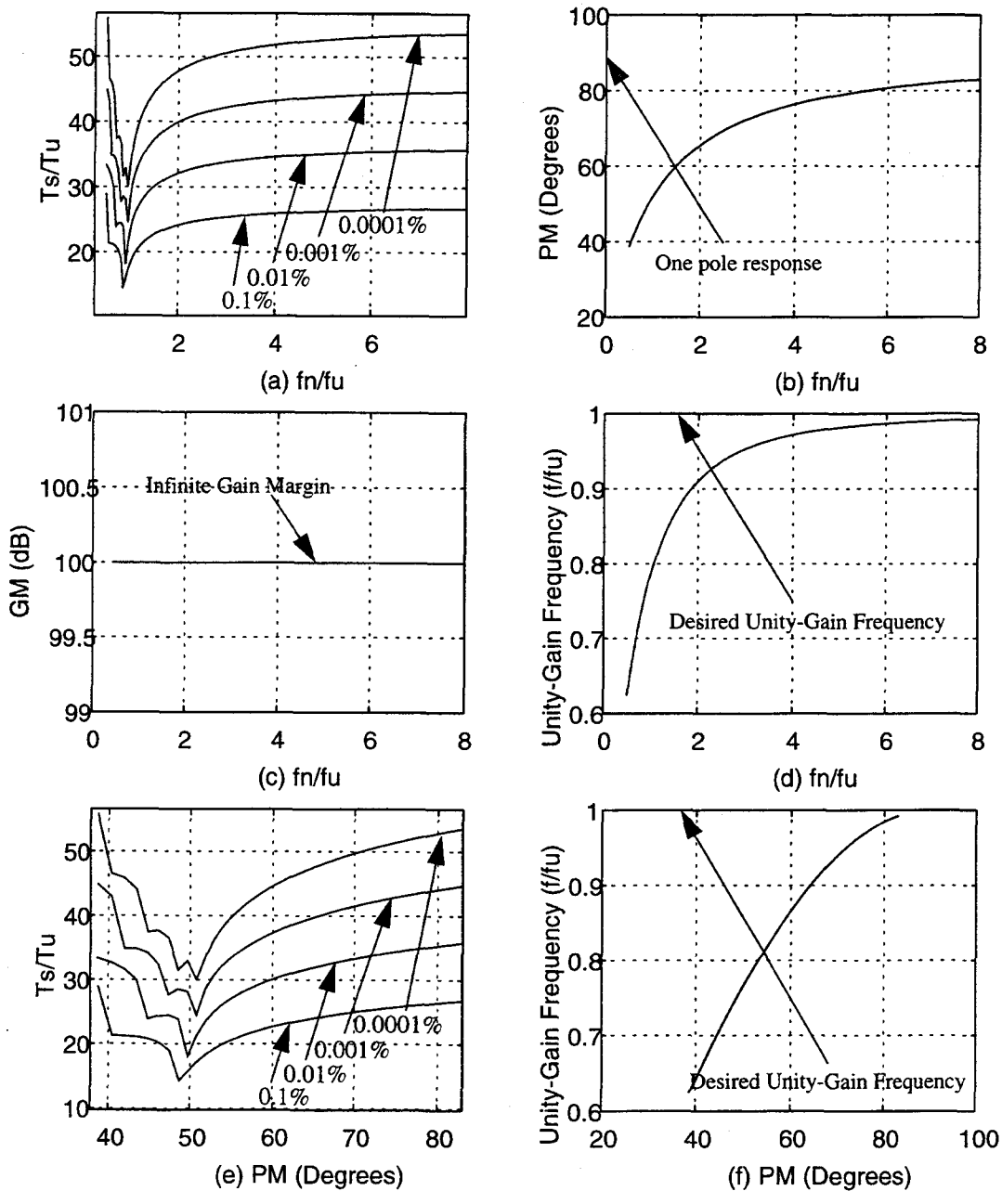

Figure 3.19. Two-stage amplifier with $\beta = 0.25$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

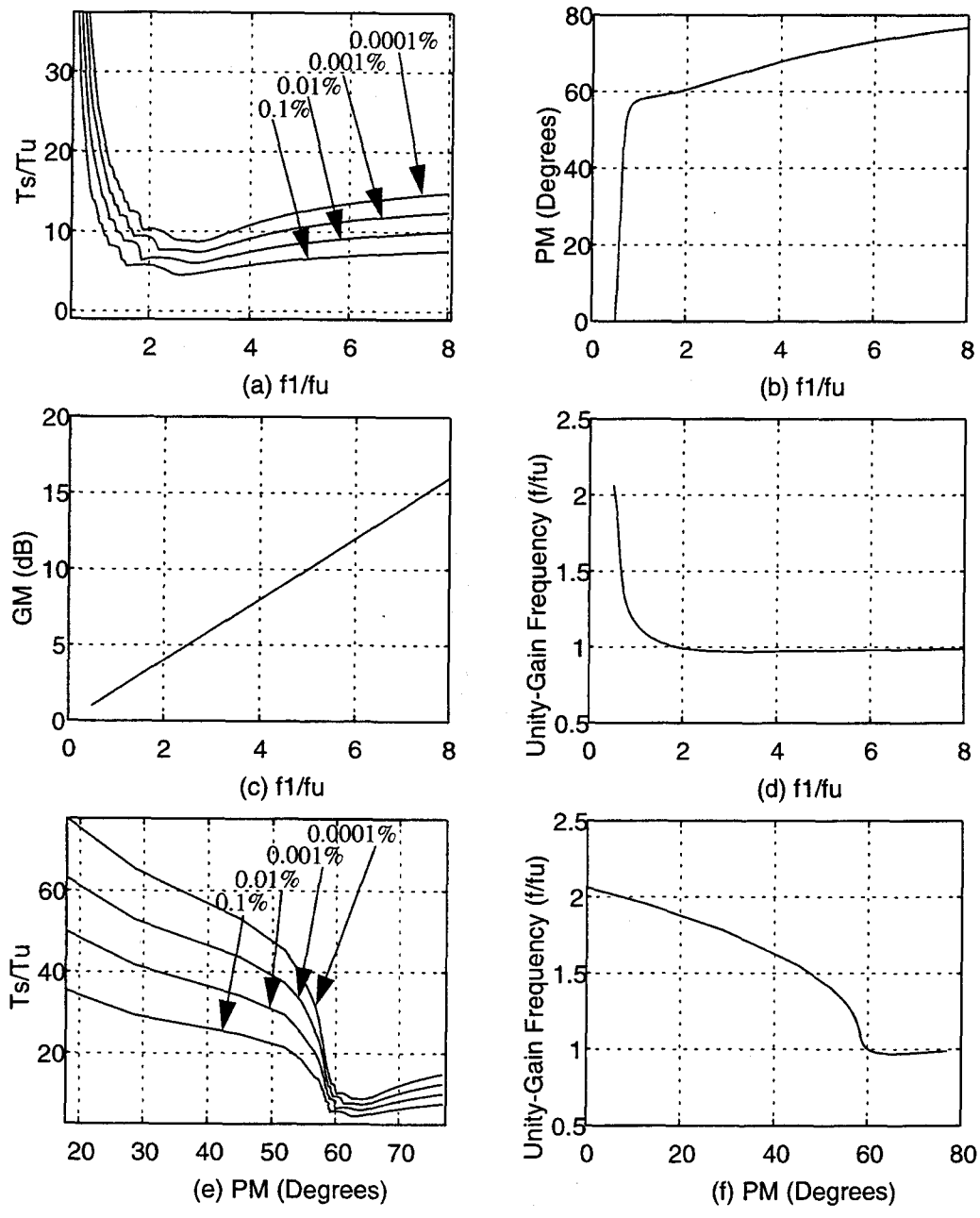

Figure 3.20. Three-stage amplifier with $\beta = 0.75$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

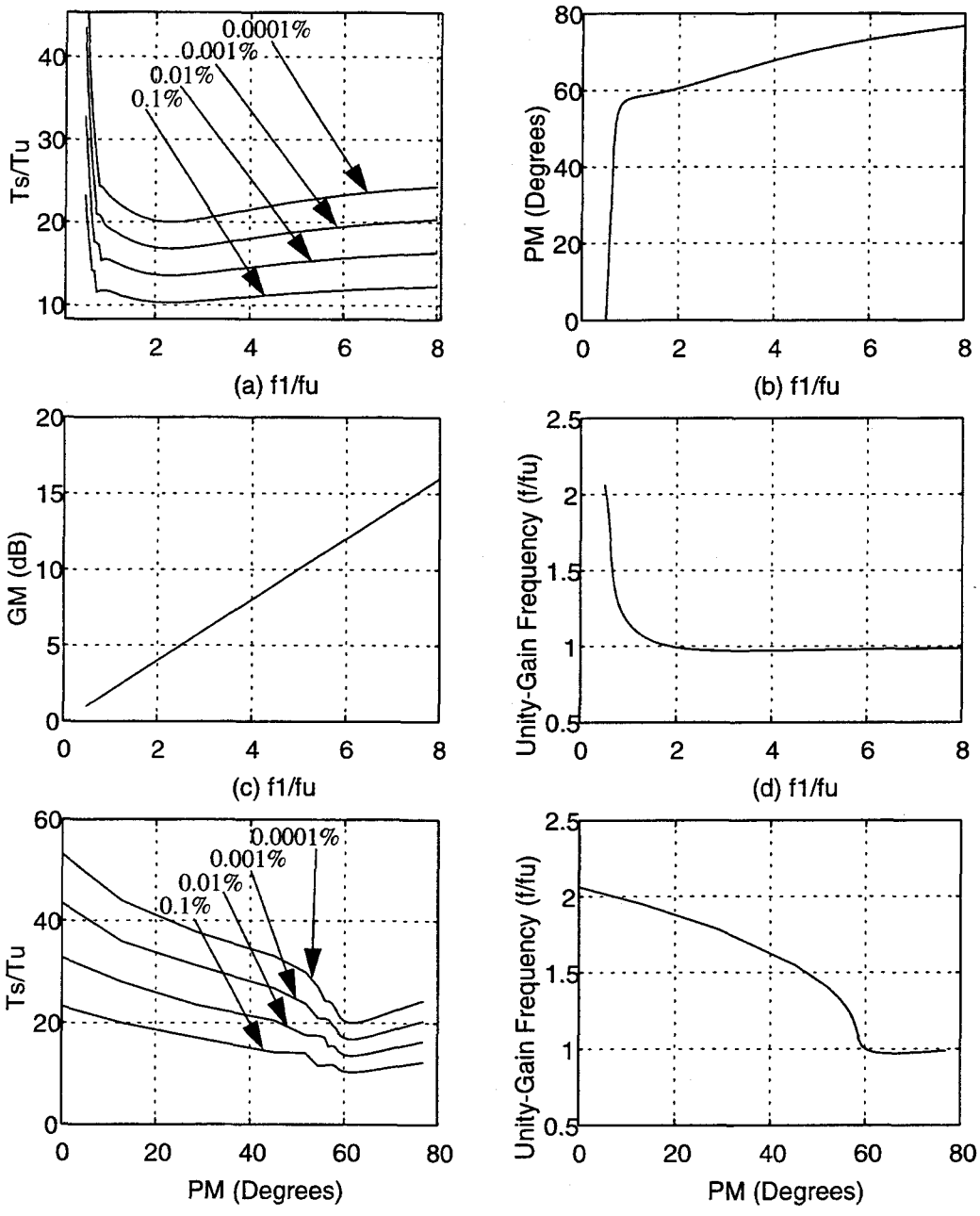

Figure 3.21. Three-stage amplifier with $\beta = 0.50$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

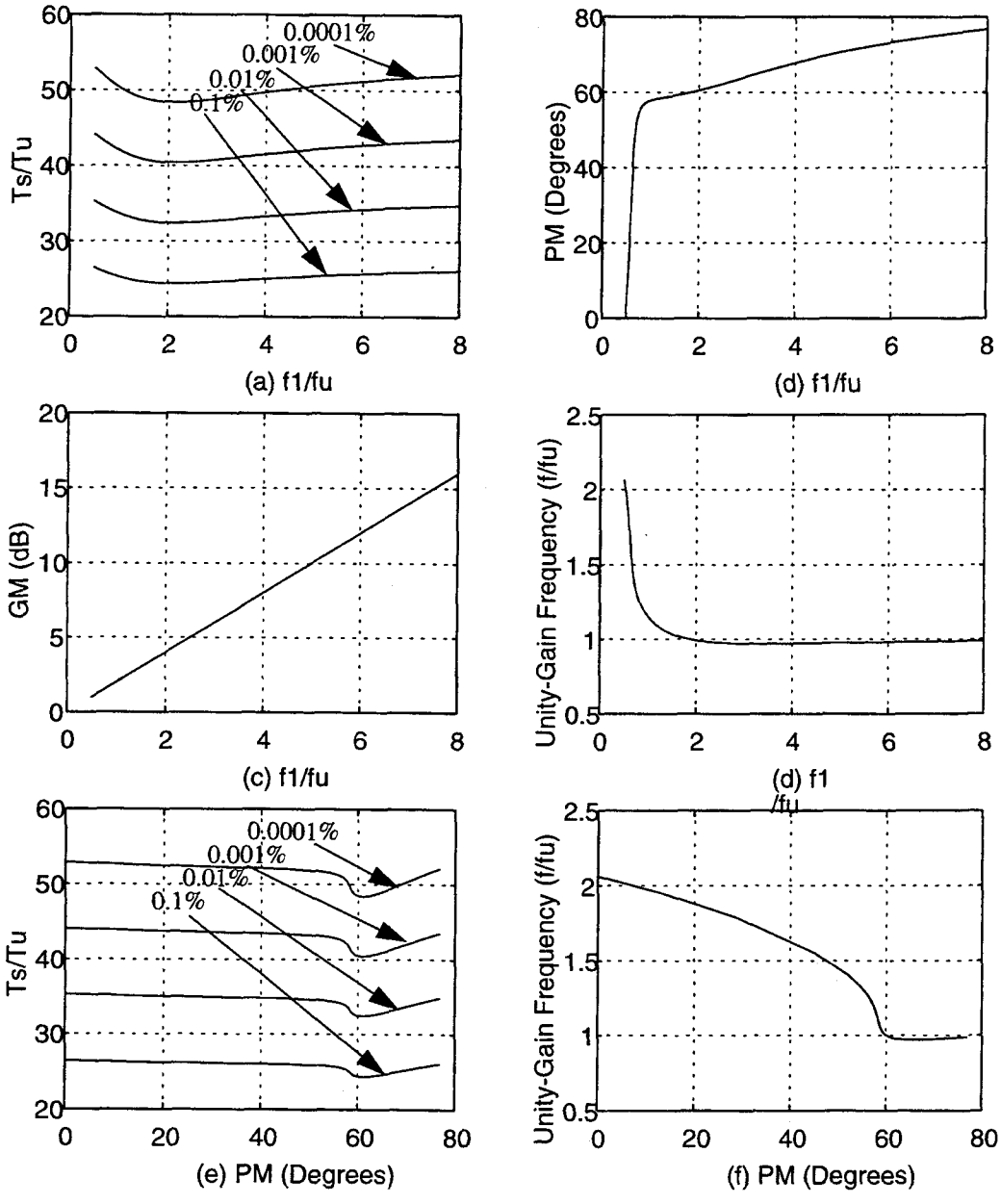

Figure 3.22. Three-stage amplifier with $\beta = 0.25$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

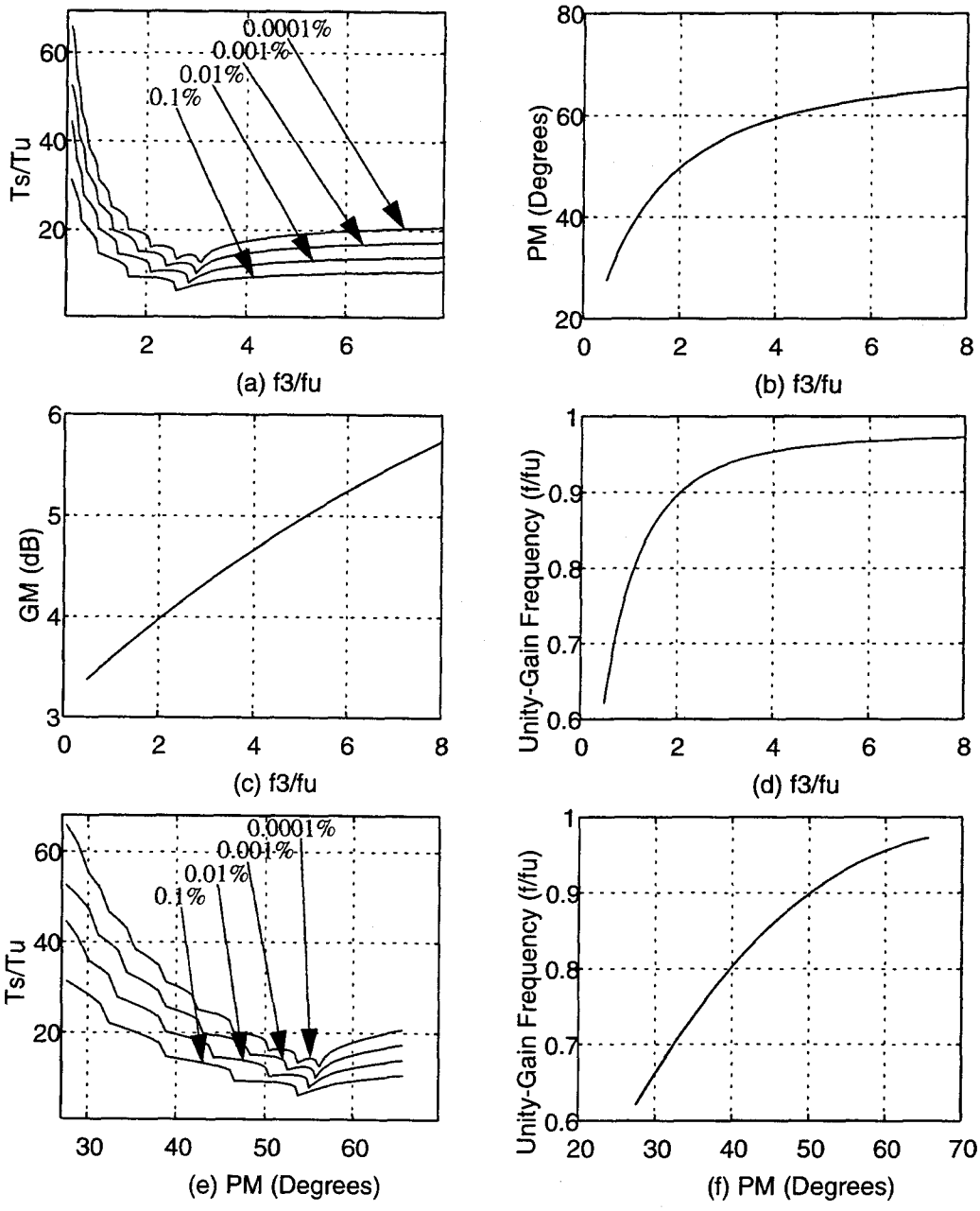

Figure 3.23. Four-stage amplifier with $\beta = 0.75$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

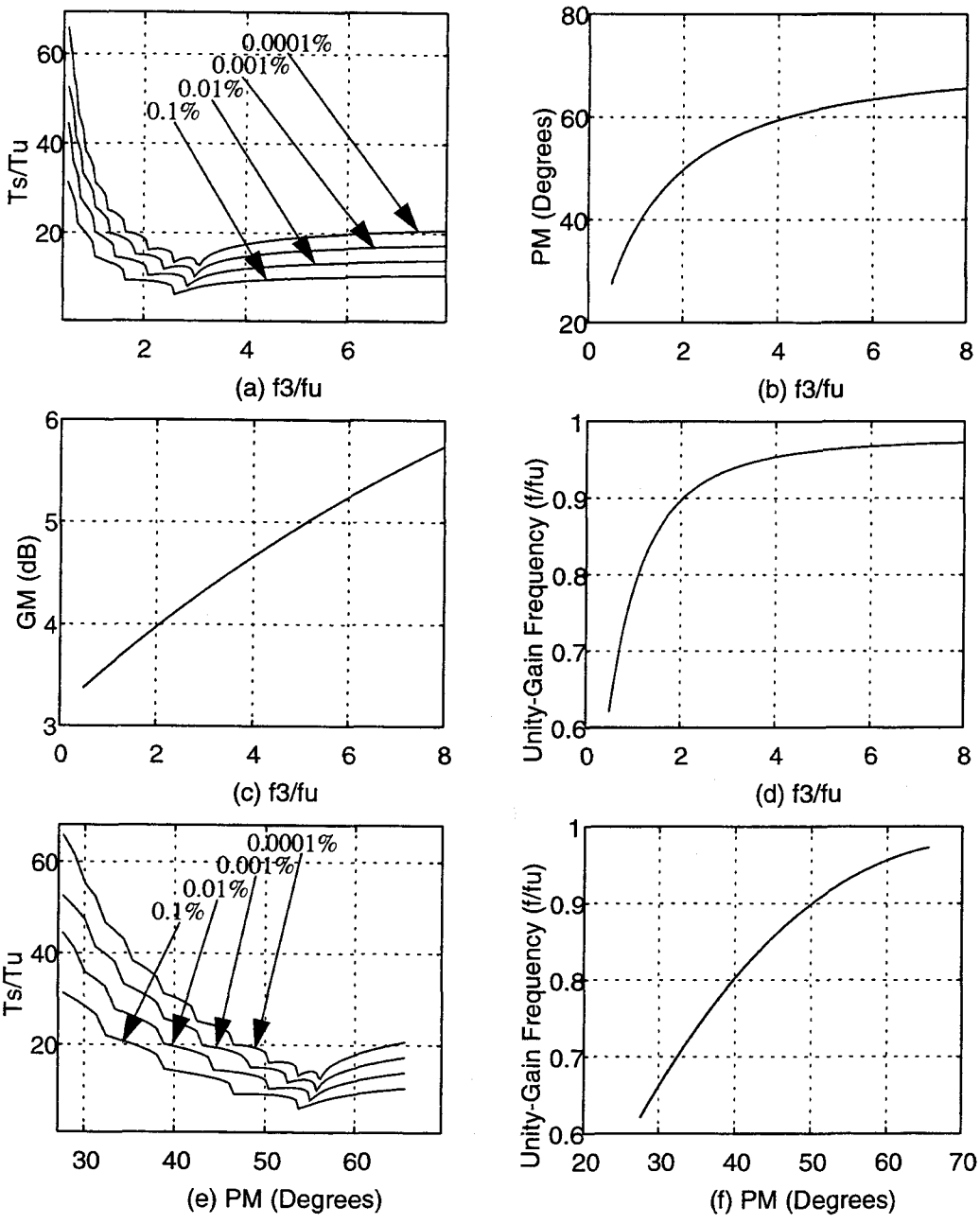

Figure 3.24. Four-stage amplifier with $\beta = 0.50$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

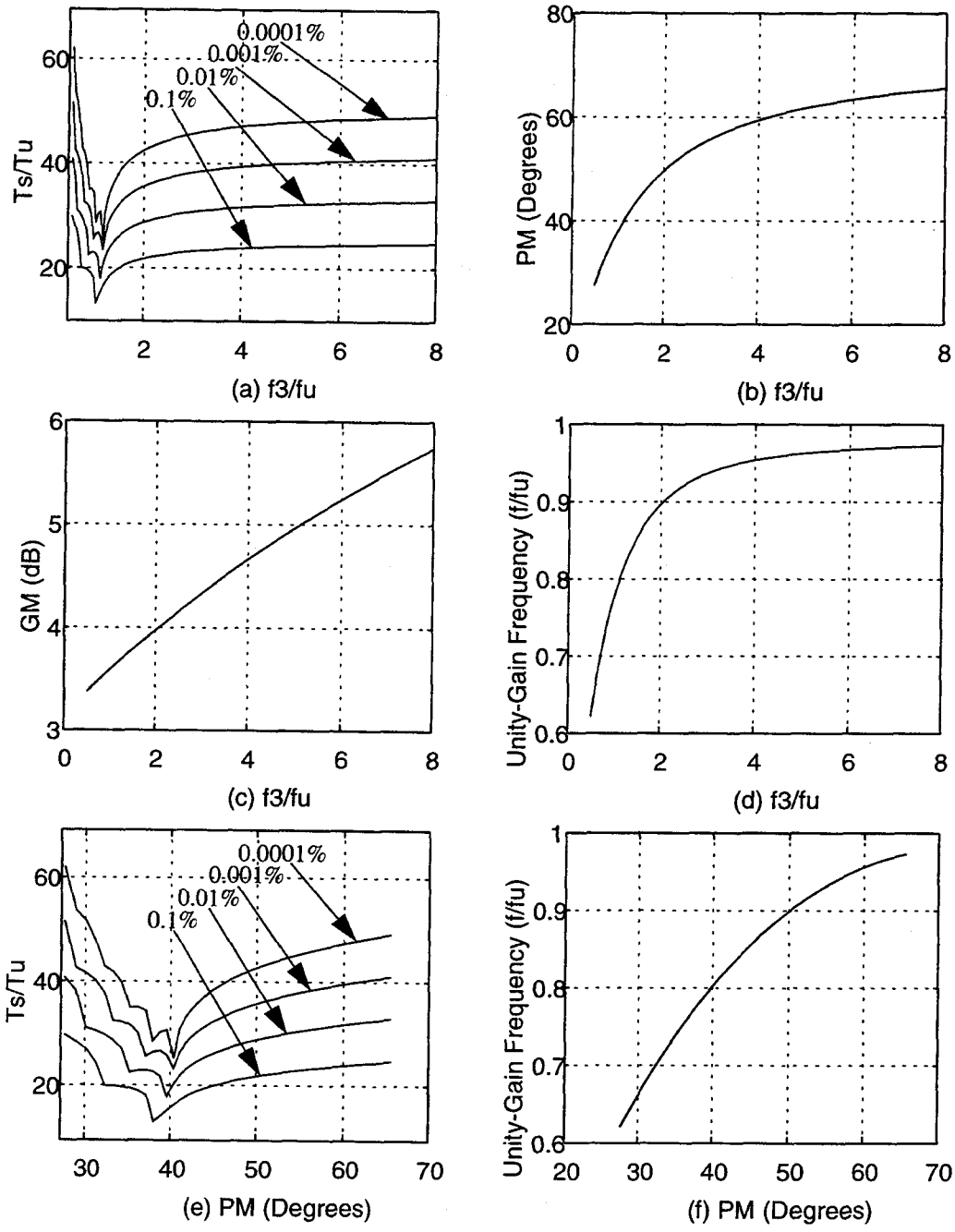

Figure 3.25. Four-stage amplifier with $\beta = 0.25$. (a) Settling time. (b) Phase margin. (c) Gain margin. (d) Unity-gain frequency. (e) Settling time versus phase margin. (f) Unity-gain frequency versus phase margin.

3.4 Pole-Zero Doublets in Multi-Stage Operational Amplifiers.

In the previous section, we studied important frequency and time domain characteristics of two-, three-, and four-stage amplifiers. We also observed how the locations of the poles affect the amplifier characteristics. In this section, a more detailed approach will be taken in modeling two-, three, and four-stage operational amplifiers. For example, the two-stage amplifier in section 3.3 was modeled by a two-pole response. In reality, two types of compensation schemes are often used in two-stage amplifiers; i.e., the compensation capacitor and the compensation RC network which add complexity to the analysis.

In the compensation capacitor scheme, a capacitor is used to split the dominant and the non-dominant poles so that the non-dominant pole is shifted beyond the unity-gain frequency. At the same time, the capacitor introduces a RHP zero (neglecting parasitic capacitors) which moves to lower frequencies and at high frequencies it adds 90° of phase shift to that introduced by the LHP poles.

In an RC compensation network, the capacitor is used to split the dominant and the non-dominant pole as above. The resistor is used to move the RHP zero to its original place and to introduce another zero which can be moved into the LHP to cancel the non-dominant pole. In this scheme, the two-stage amplifier becomes a three-pole system. One of the poles is cancelled with a zero in the vicinity of the unity-gain frequency, and another due to the resistor is located well beyond the unity-gain frequency.

The three- and four-stage operational amplifiers are similar to a two-stage amplifier in that they incorporate RC compensation. A pole-zero model of the three-stage amplifier is similar to Figure 3.9 except that there is an in-band pole-zero pair that is ideally but not actually cancelled. For a case of a four-stage amplifier, there are two such pole-zero pairs to be concerned with.

We wish to explore the effects of these pole-zero doublets (non-perfect pole-zero cancellations) on the characteristics of the operational amplifier. If the pole and zero were cancelled exactly, they would have no effect on the frequency and time responses. In a practical design, due to process, voltage, and temperature variations, exact pole-zero cancellation does not occur.

Pole-zero doublets can dominate the settling time response of an amplifier. The doublet pairs may not be visible on the operational amplifier phase and gain margins, but, settling time degrades severely in the presence of in-band doublets.

Figure 3.26 presents pole-zero plots of practical models for two- and three-stage amplifiers. The analysis for four-stage amplifiers is similar and is omitted. As opposed to previous models, doublet pairs P_{db} and Z_{db} have been considered. Ideally, these doublet pairs are exactly cancelled as mentioned in section 3.3. Note in Figure 3.26 that the doublet pair orientations are reversed in Figure 3.23(c) and (d) for the two-and three-stage amplifiers, respectively. The reason is that if we close the feedback loop with $\beta \rightarrow 1$, we see that the root loci versus β are different for the two cases.

Pole-zero doublets can be understood by considering at the root locus of the open-loop transfer function determined using MATLAB as in section 3.3. We assume that both amplifiers exhibit a one-pole response to the unity-gain frequency with the required

phase margin. Also, we assume that the doublets are initially cancelled, and by increasing the doublet spacings, the changes in amplifier characteristics is observed.

Recall from the previous section that we can select the pole position based on minimum settling times as shown in Figure 3.7 and 3.10.

For the two- and three-stage amplifiers, the fastest settling time corresponding to 0.0001%, 0.001%,0.01%, and 0.1% settling accuracy is found according to the position of the non-dominant poles, P_n for two-stage and, P_{n1} and P_{n2} for three-stage amplifiers. For the two and three-stage amplifiers, the open-loop transfer functions can be written as

$$a(s) = \frac{a_0\left(\frac{s}{Z_{db}} + 1\right)}{\left(\frac{s}{P_d} + 1\right)\left(\frac{s}{P_n} + 1\right)\left(\frac{s}{P_{db}} + 1\right)} \tag{3.57}$$

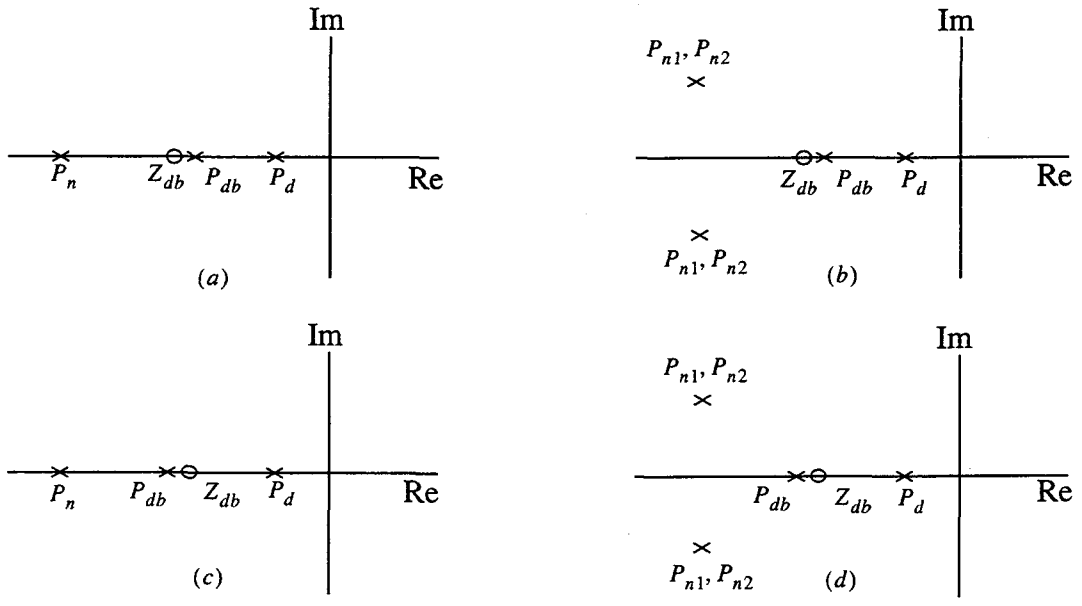

Figure 3.26. Two- and three-stage pole-zero response. (a) Two-stage with doublet. (b) Three-stage with doublet. (c), (d) The position of the doublet is reversed.

and

$$a(s) = \frac{a_0\left(\frac{s}{Z_{db}}+1\right)}{\left(\frac{s}{P_d}+1\right)\left(\frac{s}{P_{db}}+1\right)\left(\frac{s^2}{P_{n1}P_{n2}}+s\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+1\right)} \quad (3.58)$$

where Z_{db} and P_{db} represent the doublet.

The closed-loop transfer functions for (3.57) and (3.58) can be written as

$$A(s) = \frac{a_0\left(\frac{s}{Z_{db}}+1\right)}{\frac{s^3}{P_dP_nP_{db}}+s^2\left(\frac{1}{P_d}\left(\frac{1}{P_n}+\frac{1}{P_{db}}\right)+\frac{1}{P_nP_{db}}\right)+s\left(\frac{1}{P_d}+\frac{1}{P_n}+\frac{1}{P_{db}}+\frac{a_0}{Z_{db}}\right)+(1+a_0)} \quad (3.59)$$

and

$$A(s) = \frac{a_0\left(\frac{s}{Z_{db}}+1\right)}{\frac{s^4}{P_dP_{n1}P_{n2}P_{db}}+s^3\left(\frac{1}{P_dP_{db}}\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+\frac{1}{P_{n1}P_{n2}}\left(\frac{1}{P_d}+\frac{1}{P_{db}}\right)\right)+}$$

$$\frac{}{s^2\left(\frac{1}{P_dP_{db}}+\left(\frac{1}{P_d}+\frac{1}{P_{db}}\right)\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}\right)+\frac{1}{P_{n1}P_{n2}}\right)+s\left(\frac{1}{P_{n1}}+\frac{1}{P_{n2}}+\frac{1}{P_d}+\frac{1}{P_{db}}+\right.}$$

$$\left.\frac{}{\frac{a_0}{Z_{db}}\right)+(1+a_0)} \quad (3.60)$$

respectively. For the two-stage amplifier, we have a third-order system, and for the three-stage amplifier, we have a fourth-order system.

The root locus plots for the two- and the three-stage amplifiers for all cases presented in Figure 3.26 are shown in Figure 3.27. Depending on the orientation of the pole-zero pair, the root-locus plots can be substantially different. When unity-gain is

reached, the poles and zeros arrive at their final positions on the root locus plots. Note the differences in settling time behaviors for the cases where $P_{db} < Z_{db}$ and $Z_{db} < P_{db}$.

Next, we wish to evaluate for the two cases where $P_{db} < Z_{db}$ and $P_{db} < Z_{db}$, the behavior of the open-loop frequency and closed-loop transient responses. Figures 3.28(a) and (b) represent the locations of the doublet for the two cases. Assume that the pole frequency associated with the doublet is used as a reference for the relative distance between the pole-zero pair. In most cases, the pole position is determined by the compensation capacitor which can be varied to eliminate the doublet. By increasing the compensation resistance, we can also shift the doublet zero to lower frequencies. Since this is a two-variable problem, we assume that the doublet pole is constant at frequency f_o.

The two cases in Figure 3.28 are now analyzed to determine settling time. We begin with the zero exactly equal to the pole and gradually move it away by f_1. The results for settling times, phase margins, and unity-gain frequencies are then determined. Three different cases are chosen for the location of the doublets f_o with respect to the unity-gain frequency:

$$f_o = 0.5 \times f_u \tag{3.61}$$

$$f_o = 1.0 \times f_u \tag{3.62}$$

and

$$f_o = 1.5 \times f_u \tag{3.63}$$

The cases for (3.62) and (3.63) represent doublets that are present in practical systems. The plots for the values given in (3.61), (3.62), and (3.63) versus f_1 are shown in Figures 3.29-31 for the two-pole and in Figures 3.32-34 for the three-pole amplifiers.

From Figures 3.29 and 3.32(a)-(d), it is seen that the settling time behavior due to the doublet are nearly identical for two- and three-pole systems. Three important

results can be attributed to the doublet pairs. First, note the effect on settling versus f_o when the doublet pairs are moved from within the bandwidth to higher frequencies. A

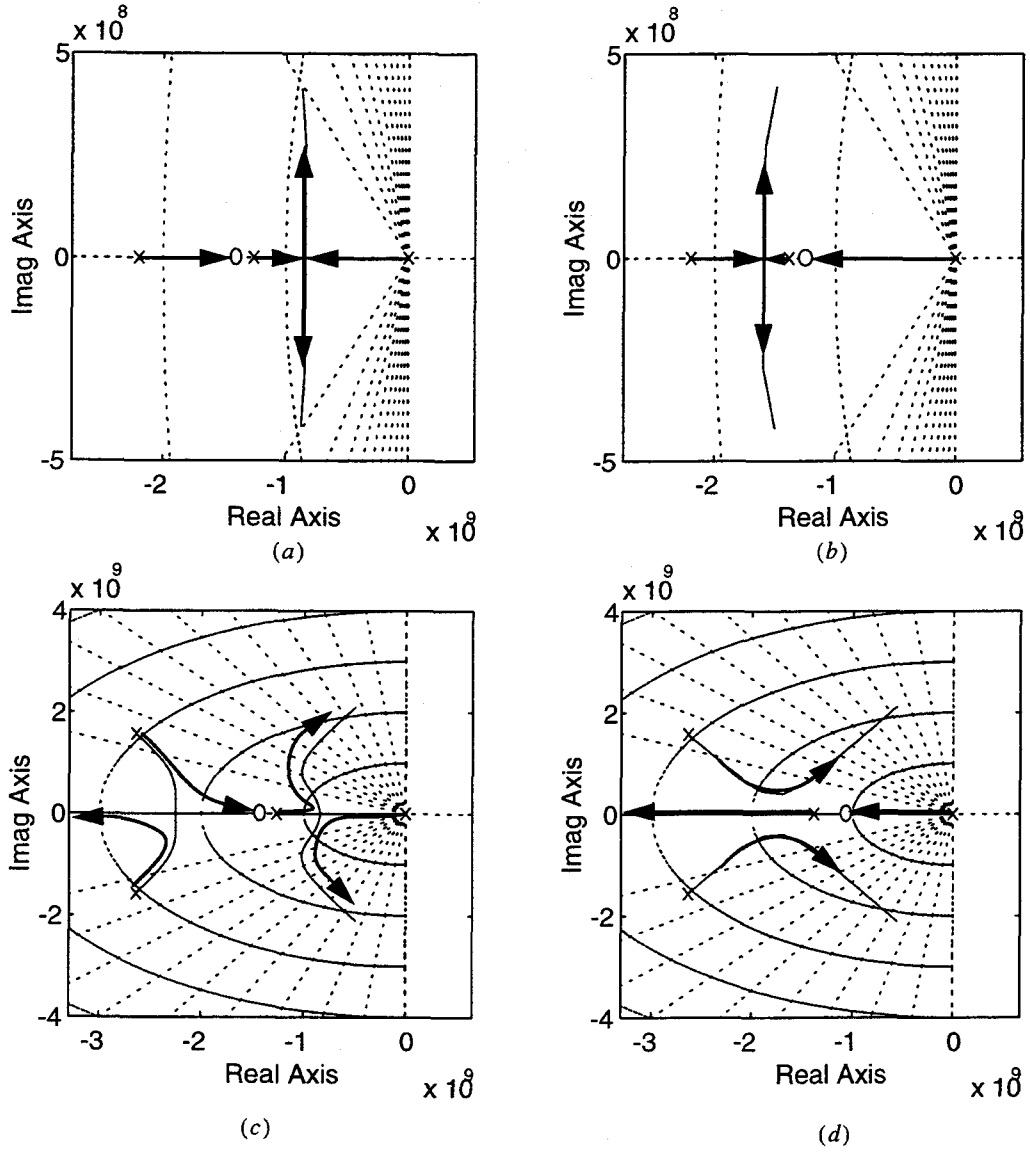

Figure 3.27. Two- and three-stage root-locus plots. (a) Two-stage amplifier with $P_{db} < Z_{db}$. (b) Two-stage amplifier with $Z_{db} < P_{db}$. (c) Three-stage amplifier with $P_{db} < Z_{db}$. (c) Three-stage amplifier with $Z_{db} < P_{db}$.

designer should try to place the doublet pairs as high in frequency as possible, because doublets at higher frequencies not degrade the settling time dramatically as for doublets in the lower frequencies. Second, for $P_{db} < Z_{db}$, the settling time increases at a slower rate as f_1 is increased, while for $Z_{db} < P_{db}$, the rate of increase is much higher. From these plots, it is better to under compensate the amplifier to minimize the settling time.

Figures 3.30 and 3.33(a)-(d) represent the changes in phase margin versus the spacings of the doublet pairs. As the phase margin decreases, the settling time increases proportionately. For the case where $P_{db} < Z_{db}$, the phase margin decreases more rapidly than for $Z_{db} < P_{db}$ and the settling time characteristics change accordingly. Note that for the cases where f_o is placed higher frequencies, the phase margin changes linearly with the location of the zero, resulting in a symmetrical change in settling characteristics for both $P_{db} < Z_{db}$ and $Z_{db} < P_{db}$.

Figures 3.31 and 3.34(a)-(d) represent the change in unity-gain frequency versus the doublet pair spacings. It is evident that achieving higher unity-gain frequency does not necessarily mean faster settling characteristics. As seen, the unity-gain frequency associated with f_o within the bandwidth is higher than the desired frequency, but the

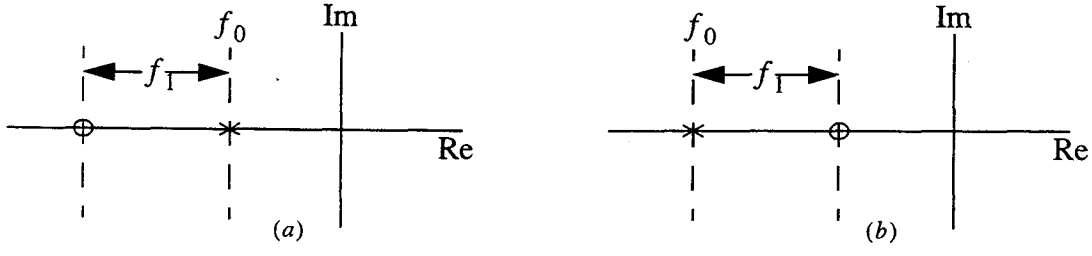

Figure 3.28. Pole-zero doublet locations. (a) Pole-zero doublet with $P_{db} < Z_{db}$. (b) Pole-zero doublet with $Z_{db} < P_{db}$.

settling time does not correspond to the higher f_u. One must use caution in achieving large unity-gain frequencies with the corresponding fast settling time as was discussed in section 3.3.

We can also conclude from these simulations that the effect of a doublet is independent of settling accuracy and the order of the system. For all cases, the settling time, phase margin, and unity-gain frequency behaviors are identical. Similar results can be obtained for a four-pole system, but due to the increase in the number of poles, the number of doublet pairs will increase to two. To maintain stability in the presence of process, temperature, and voltage variations, we expect the settling time to increase due to the higher number of doublets. It is possible to place the other doublet pair at higher frequencies to minimize slow settling effects. Thus, a higher number of stages can be used while still achieving fast settling times.

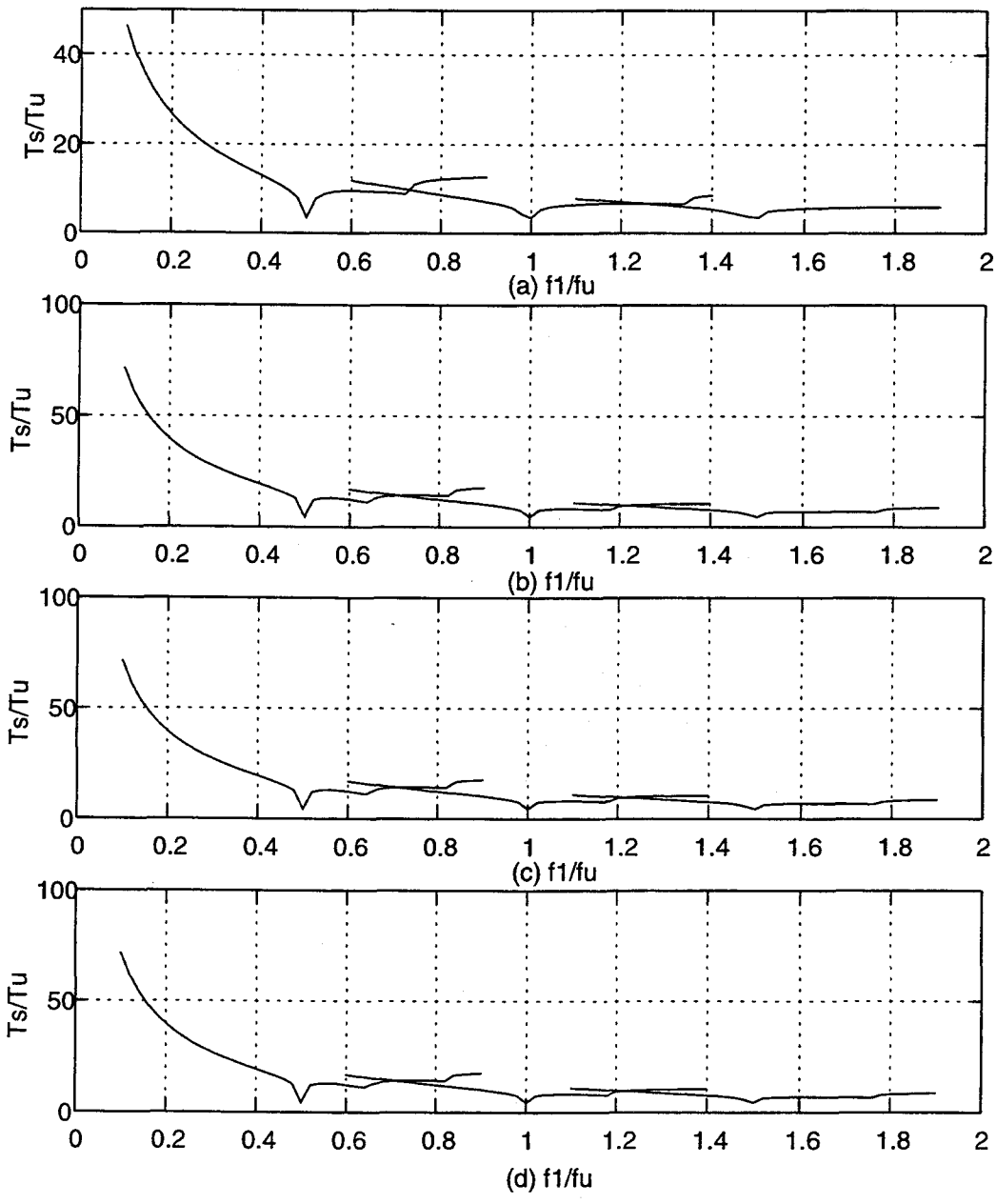

Figure 3.29. Pole-zero doublet responses for two-stage amplifier settling times. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) 0.0001%, (b) 0.001%, (c) 0.01%, and (d) 0.1% settling accuracies.

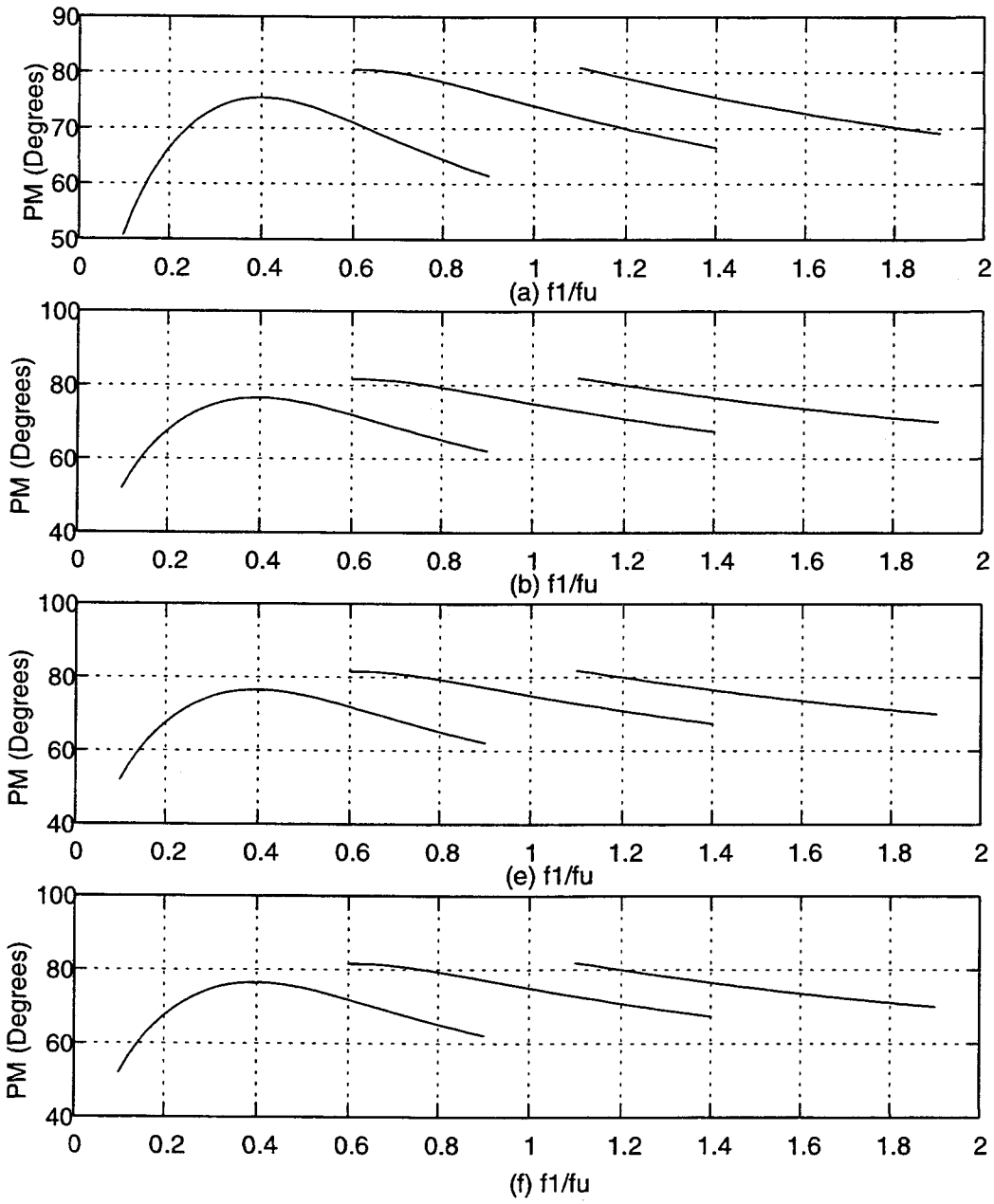

Figure 3.30. Pole-zero doublet responses for two-stage amplifier showing phase margins. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) For 0.0001% settling accuracy. (b) For 0.001% settling accuracy. (c) For 0.01% settling accuracy. (d) For 0.1% settling accuracy.

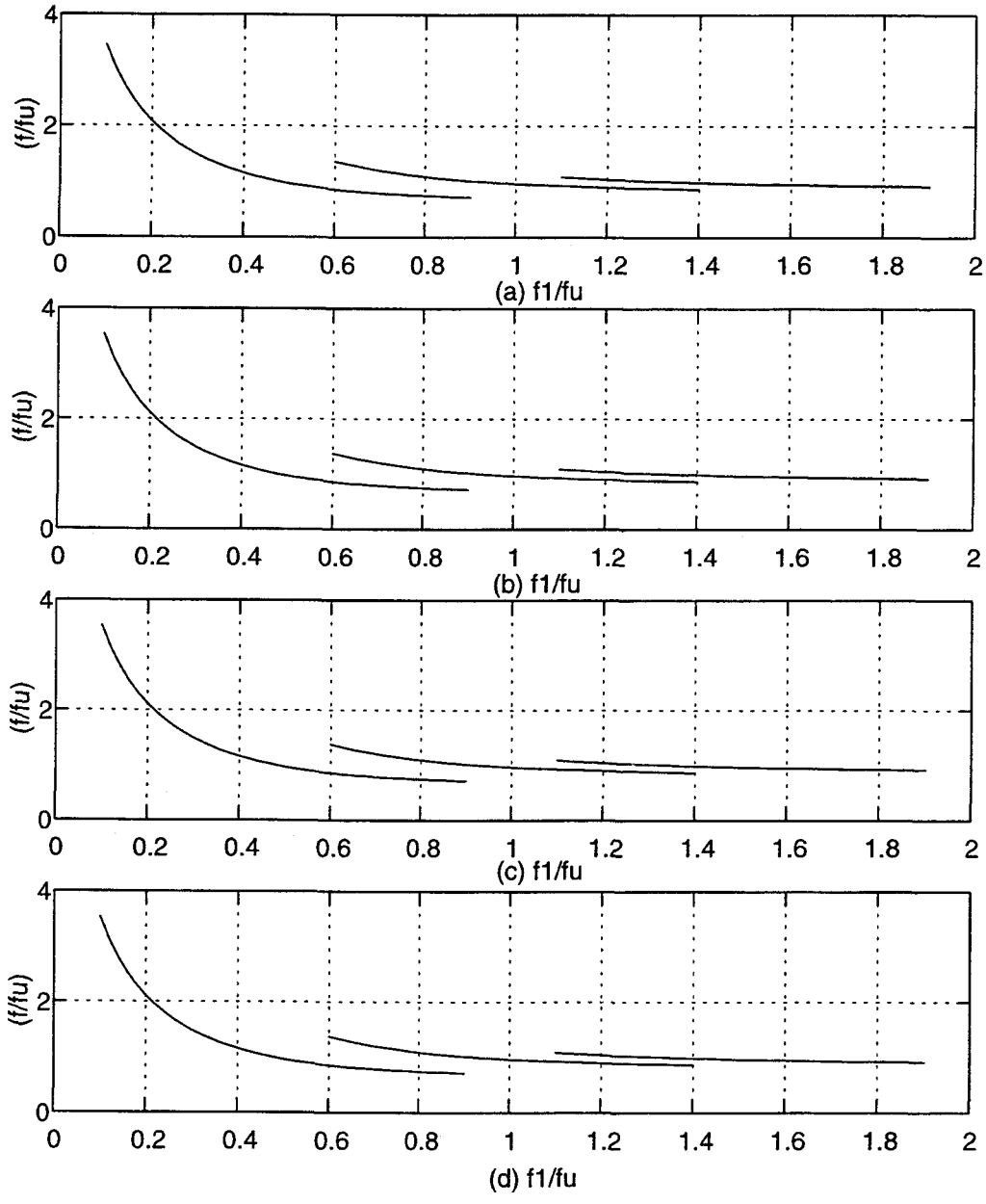

Figure 3.31. Pole-zero doublet responses for two-stage amplifier unity-gain frequencies. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) 0.0001%, (b) 0.001%, (c) 0.01% settling accuracy, and (d) 0.1% settling accuracies.

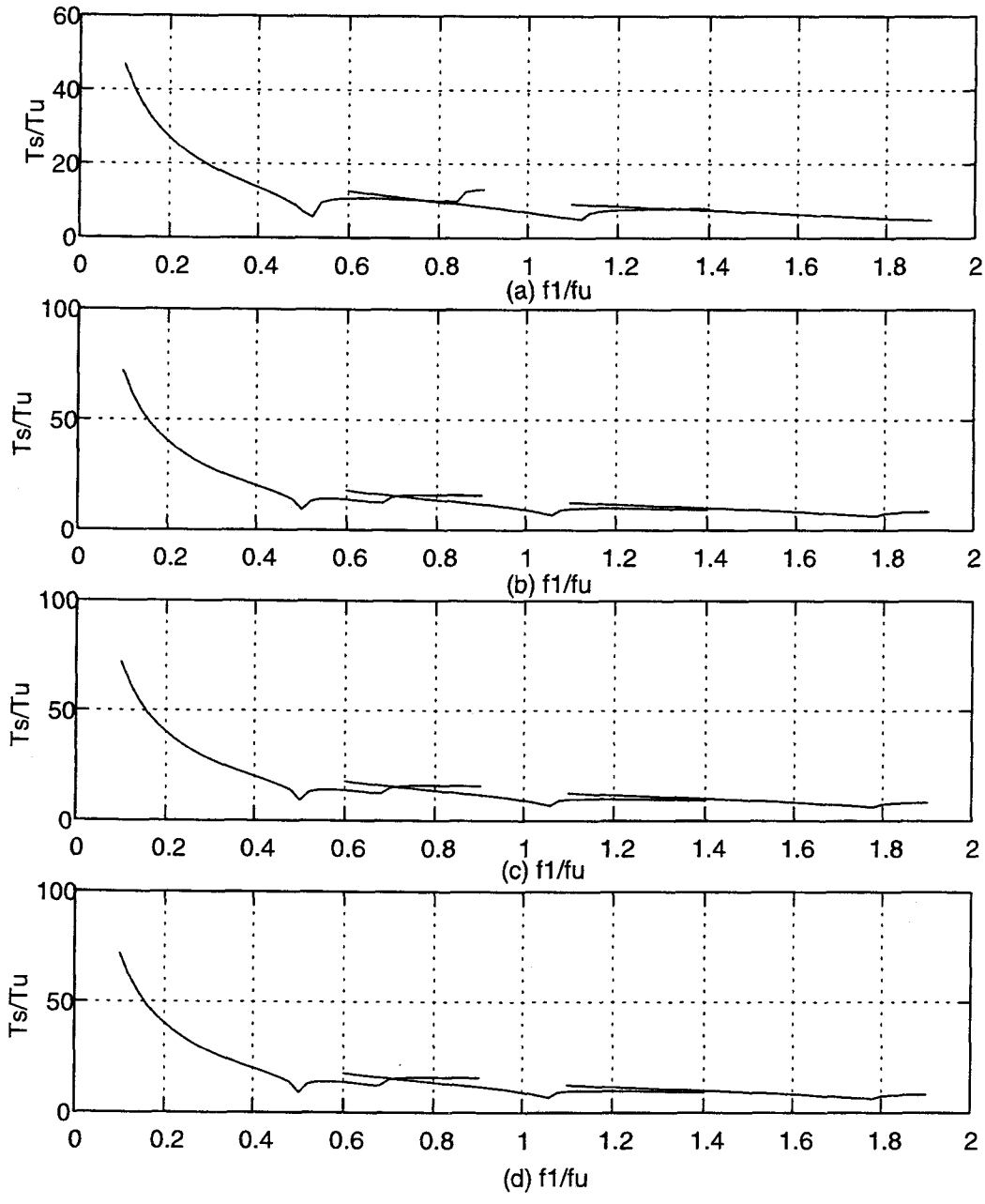

Figure 3.32. Pole-zero doublet responses for three-stage amplifier settling times. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) 0.0001%, (b) 0.001%, (c) 0.01%, and (d) 0.1% settling accuracies.

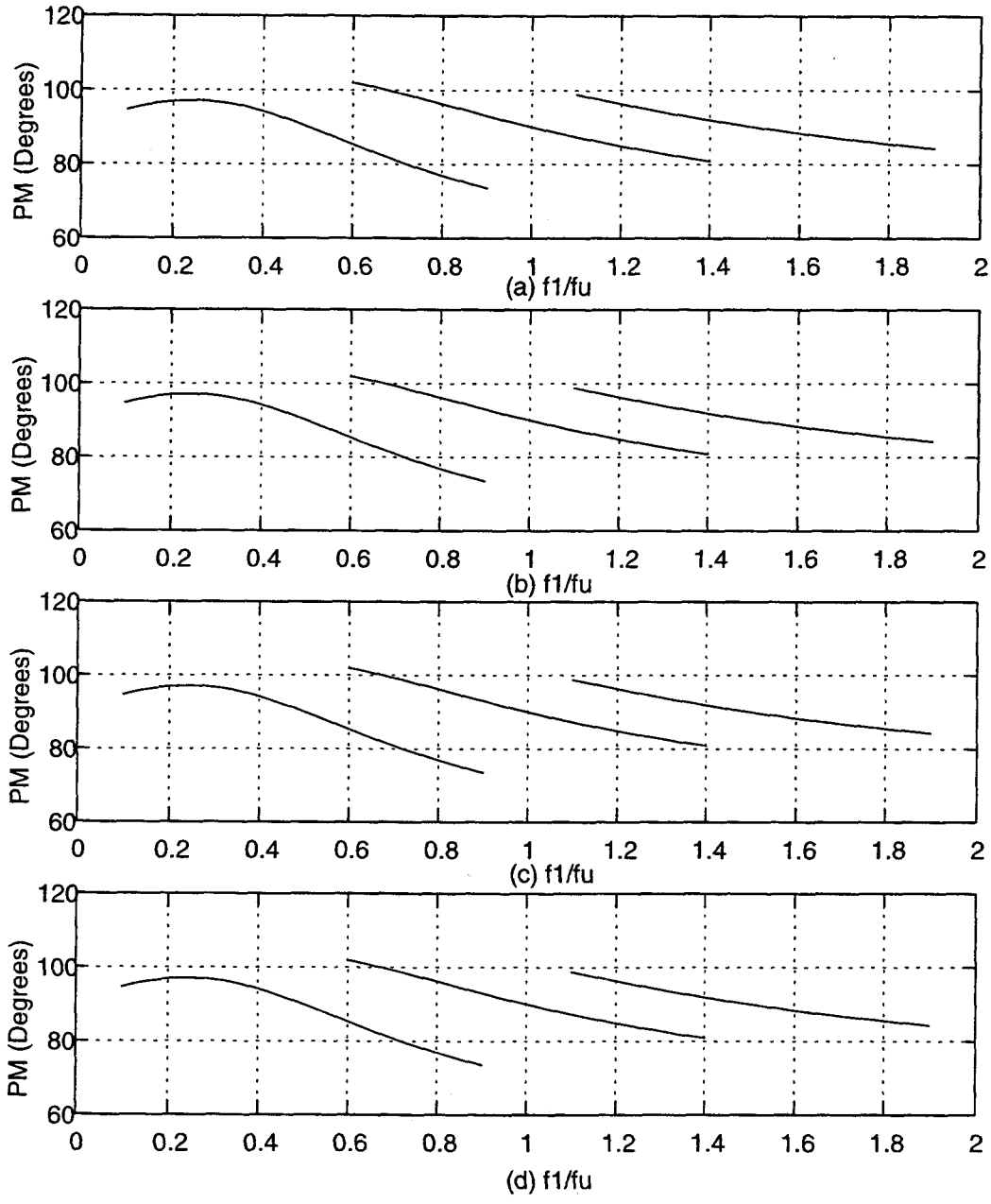

Figure 3.33. Pole-zero doublet responses for three-stage amplifier phase margins. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) 0.0001%, (b) 0.001%, (c) 0.01%, and (d) For 0.1% settling accuracies.

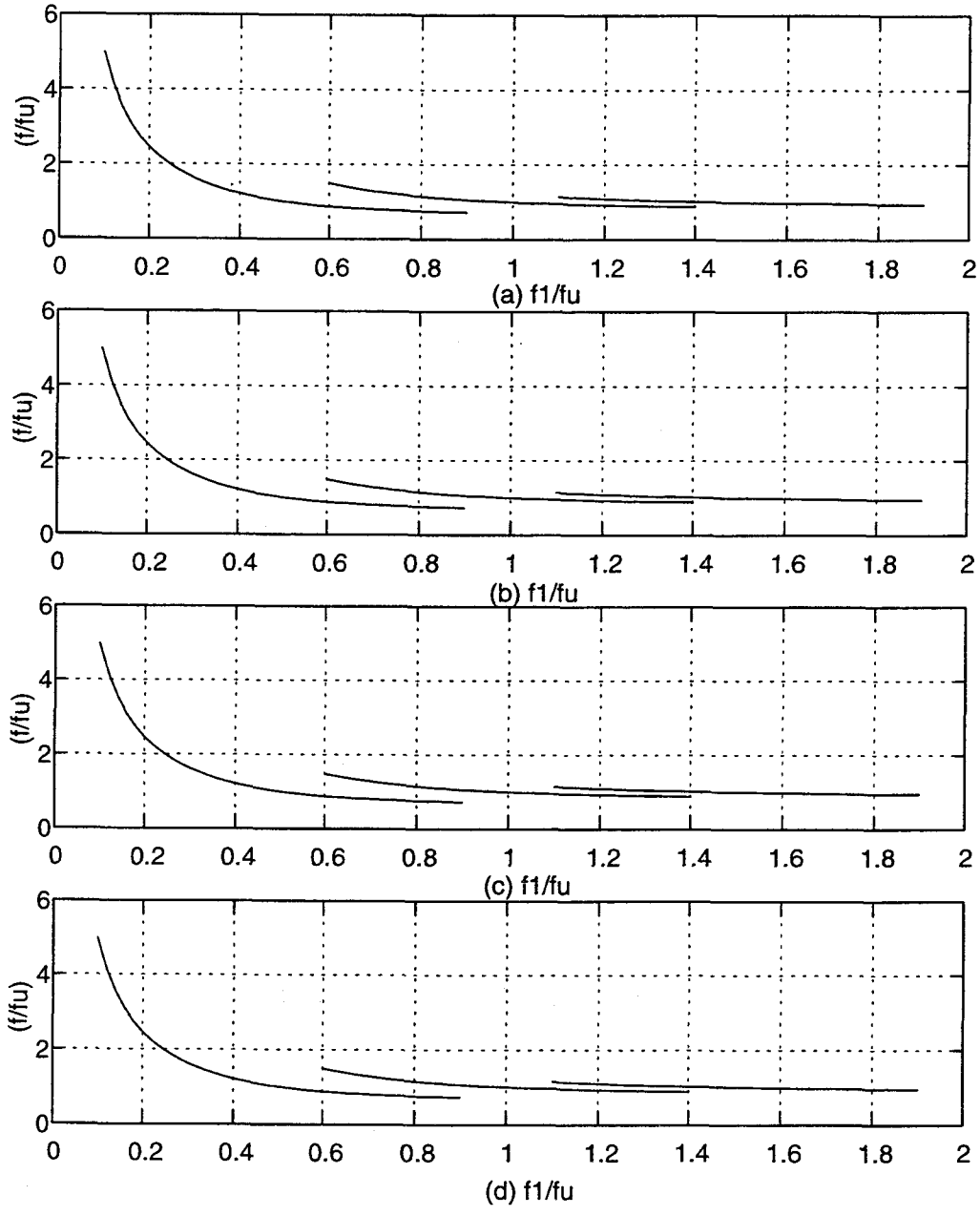

Figure 3.34. Pole-zero doublet responses for three-stage amplifier unity-gain frequencies. Plots include $P_{db} < Z_{db}$, and $Z_{db} > P_{db}$ for doublets at 0.5, 1.0, and 1.5 times the unity-gain frequency. (a) 0.0001%, (b) 0.001%, (c) 0.01%, and (d) 0.1% settling accuracies.

Chapter 4. Frequency Compensation Techniques and Considerations

Monolithic integrated circuits put severe limitations on the options available for frequency compensation. The only frequency dependent compensation elements available on integrated circuits are capacitors to shape the frequency response. However, their use is limited to the area available.

This chapter examines one of the most popular frequency compensation techniques; pole splitting and pole cancellation technique [10]. This type of frequency compensation, will be closely examined on a two-stage amplifier first and then on the three-stage amplifiers. Pole splitting and pole cancellation compensation in general, in this thesis employes an embedded RC compensation network to achieve the desired stability and performance criteria complying with Chapter 3.

4.1 Miller Compensation

One of the most popular compensation techniques for changing the amplifier characteristics is using capacitors across the inverting gain stages. An example of this approach is the Miller compensation capacitor, which uses a capacitor as the feedback impedance of a shunt stage [11]. Since the capacitor does not effect the DC gain of the transistor or the amplifier, ensures a high loop gain at low frequencies.

An even better compensation technique, is by employing an RC compensation network which uses a capacitor in series with a resistor as the feedback impedance of a shunt stage. Later on, we will observe that this type of approach holds the characteristic integrity of the Miller compensation capacitor and further improves the amplifier characteristics over Miller compensation scheme, allowing the multi-stage amplifiers to achieve higher performance characteristics.

Miller Capacitance (Miller Effect)

Miller compensation is associated with using a capacitor in local feedback around an inverting gain stage. Figure 4.1 shows a simple gain stage with finite gain A and Miller capacitance C_m. The output voltage

$$V_{out} = AV_{in} \tag{4.1}$$

and the charge on C_m is

$$Q = CV \tag{4.2}$$

Consider the input and output capacitances due to effect of Miller capacitance C_m which can be written as

$$C_{in} = \frac{Q_{in}}{V_{in}} \tag{4.3}$$

and

$$C_{out} = \frac{Q_{out}}{V_{out}} \tag{4.4}$$

The input charge Q_{in} is

$$Q_{in} = C_m V_{in} - C_m V_{out} = C_m(V_{in} - A(s)V_{in}) = C_m V_{in}(1 + A(s)) \tag{4.5}$$

thus, equivalent input capacitance can be written as

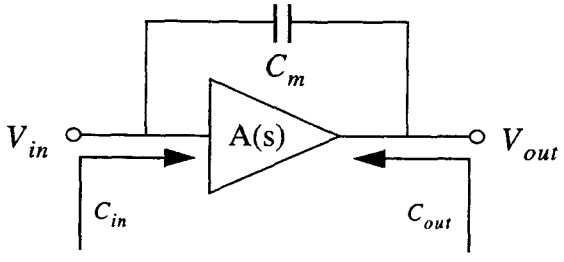

Figure 4.1. Miller capacitance in a single-stage amplifier.

$$C_{in} = C_m(1-A(s)) \tag{4.6}$$

and the equivalent output capacitance using similar analysis is

$$C_{out} = C_m\left(1-\frac{1}{A(s)}\right) \tag{4.7}$$

First assume that the gain of the amplifier is frequency independent with

$$A(s) = A_0 \tag{4.8}$$

The equivalent input and output capacitances are

$$C_{in} = C_m(1-A_0) \tag{4.9}$$

and

$$C_{out} = C_m\left(1-\frac{1}{A_0}\right) \tag{4.10}$$

The corresponding capacitance plots versus A_0 are shown in Figure 4.2. The input capacitance has a linear relationship and a zero value if $A_0 = 1$ as shown in Figure 4.2(a). This is also true for C_{out} as shown in Figure 4.2(b). Note that for large gain values $C_{out} = C_{in}$.

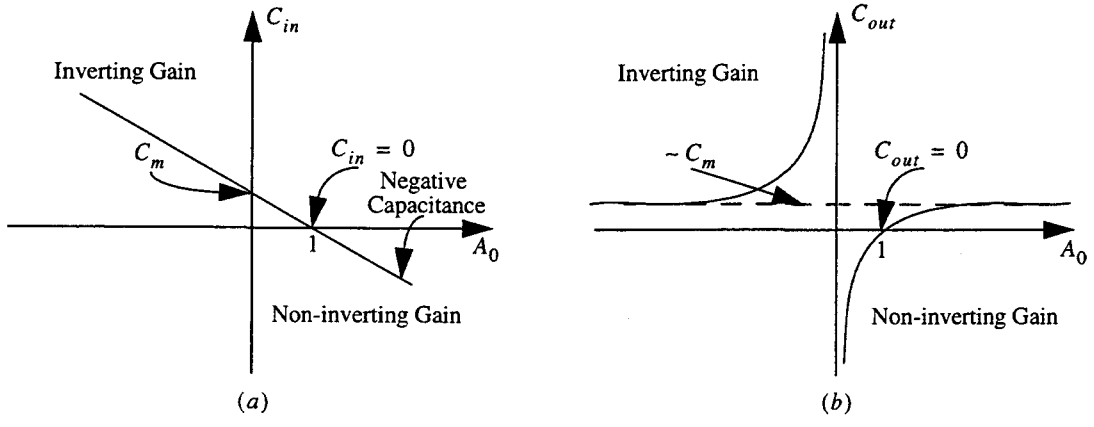

Figure 4.2. Input and output capacitances as a function of low-frequency gain. (a) Input capacitance. (b) Output capacitance.

Let us analyze equations (4.6) and (4.7) in more depth with A(s) frequency

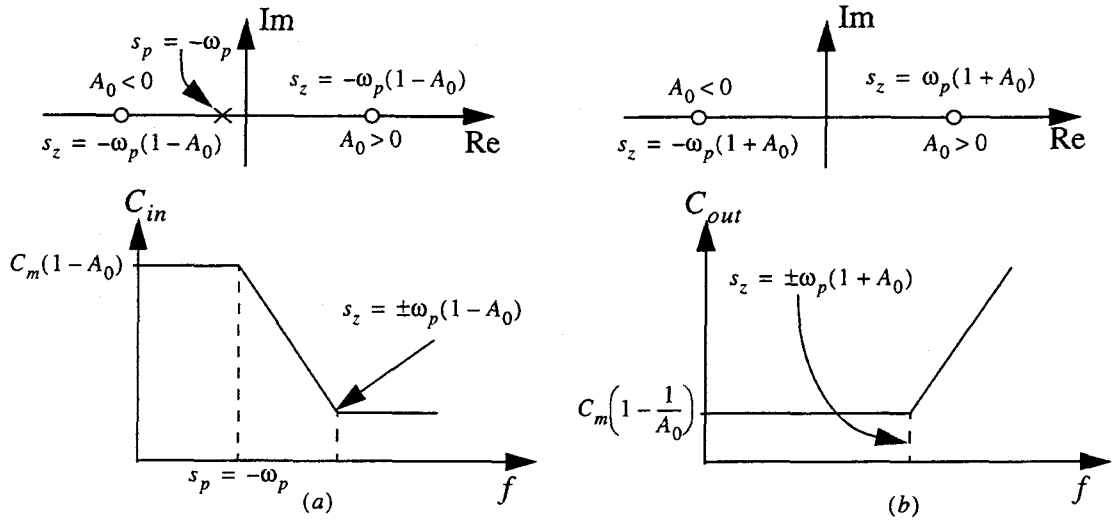

Figure 4.3. Frequency response of the input and output capacitances due to Miller capacitance effect. (a) Input capacitance. (b) Output capacitance.

dependent. We define A(s) to have a single pole response,

$$A(s) = \frac{A_0}{\left(\frac{s}{\omega_p} + 1\right)} \tag{4.11}$$

and determine C_{in} and C_{out} as

$$C_{in} = C_m \frac{\frac{s}{\omega_p} + (1 - A_0)}{\left(\frac{s}{\omega_p} + 1\right)} \tag{4.12}$$

and

$$C_{out} = -C_m\left(\frac{s}{A_0\omega_p} - \left(1 + \frac{1}{A_0}\right)\right) \tag{4.13}$$

The associated frequency responses are shown in Figure 4.3. Note that as the gain decreases versus frequency, the input and output capacitances change. Specifically, the output capacitance increases and input capacitance decreases resulting in a pole splitting behavior in a single-stage amplifier. This decreases the bandwidth of the amplifier due to the increase in output capacitance. However, this only holds for a single-stage amplifier with a simple Miller capacitance. In multi-stage amplifiers, however, the pole-splitting behavior described above does not hold for all gain stages in the signal path since the individual transfer functions are more complex. In multi-stage operational amplifiers, we will show that the output stage has the simplest transfer function, a single pole response, compared to the preceding stages which include multiple poles and zeros.

4.2 Two-Stage Amplifier Compensation

Consider the two-stage amplifier in Figure 4.4. Ideal transconductors representing the gain stages, and has an equivalent output conductance and load capacitance for each stage. Before compensation, the parasitic capacitors C_{c1} and C_{c2} are connected across the first and second stages respectively. The gain stage and feedback capacitor constitute an integrator.

We will begin by solving the nodal equations to determine the individual transfer functions, and the overall transfer function. Applying KCL at V_{o1} gives

$$V_{in}(sC_{p1} - g_{m1}) = V_{o1}[s(C_{p1} + C_{p2} + C_{L1}) + g_{ds1}] - V_{out}sC_{p2} \quad (4.14)$$

and applying KCL at V_{out} gives

$$V_{o1}(sC_{p2} - g_{m2}) = V_{out}[s(C_{p1} + C_{L2}) + g_{ds2}] \quad (4.15)$$

Thus, the transfer function of the second stage is obtained from (4.15) as

$$\frac{V_{out}}{V_{o1}} = \frac{(sC_{p2} - g_{m2})}{[s(C_{p1} + C_{L2}) + g_{ds2}]} \tag{4.16}$$

Solving (4.16), the transfer function of the first stage is

$$\frac{V_{o1}}{V_{in}} = \frac{(sC_{p1} - g_{m1})[s(C_{p2} + C_{L2}) + g_{ds2}]}{s^2(C_{p2}C_{L2}^2 + C_{p2}C_{L1} + C_{p1}C_{L2} + C_{L1}C_{L2} + C_{c1}C_{p2}) + s[g_{ds1}(C_{p2} + C_{L2}) + g_{ds2}(C_{p1} + C_{p2} + C_{L1}) + g_{m2}C_{p2}] + g_{ds1}g_{ds2}} \tag{4.17}$$

For simplicity, (4.17) can be written as

$$\frac{V_{o1}}{V_{in}} = \frac{(sC_{p1} - g_{m1})[s(C_{p2} + C_{L2}) + g_{ds2}]}{As^2 + Bs + C} \tag{4.18}$$

where

$$A = C_{p2}C_{L2}^2 + C_{p2}C_{L1} + C_{p1}C_{L2} + C_{L1}C_{L2} + C_{p1}C_{p2} \tag{4.19}$$

$$B = g_{ds1}(C_{p2} + C_{L2}) + g_{ds2}(C_{p1} + C_{p2} + C_{L1}) + g_{m2}C_{p2}] \tag{4.20}$$

and

$$C = g_{ds1}g_{ds2} \tag{4.21}$$

The overall transfer function is

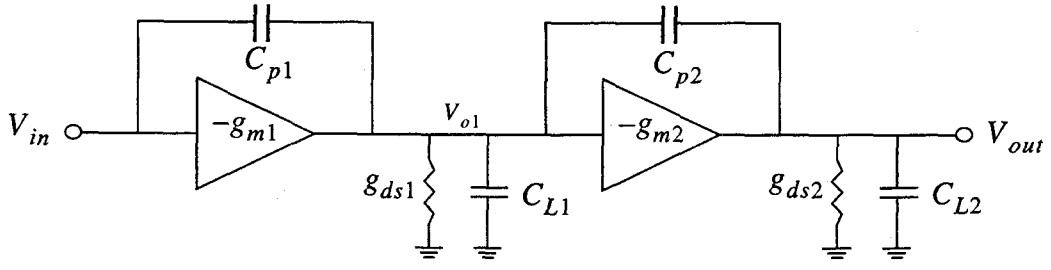

Figure 4.4. Small-signal representation of a two-stage amplifier.

$$\frac{V_{out}}{V_{in}} = \frac{(sC_{p2} - g_{m2})}{[s(C_{p1} + C_{L2}) + g_{ds2}]} \cdot \frac{(sC_{p1} - g_{m1})[s(C_{p2} + C_{L2}) + g_{ds2}]}{As^2 + Bs + C}$$

$$= \frac{(sC_{p2} - g_{m2})(sC_{p1} - g_{m1})}{As^2 + Bs + C}. \qquad (4.22)$$

From (4.22), we see that the LHP pole of the second stage is cancelled with the

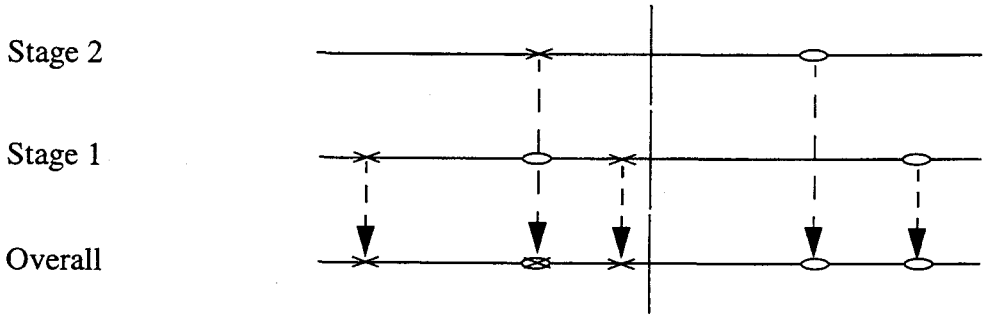

Figure 4.5. S-plane plots of the transfer functions of equations (4.16), (4.18), and (4.22).

LHP zero of the first stage! However, the overall transfer function still exhibits two poles and two zeros, but it is "referred" to the input-stage transfer function. This means that the input stage is dominant in determining the desired characteristics of the amplifier. However, if C_{p1} and C_{p2} are not included, the system poles would be associated with the RC time constants seen at each node in the signal path. Figure 4.5 shows the s-plane plots for each stage and the overall amplifier.

The denominator of (4.22) is second order in which at DC reduces to the expected result of

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}} \tag{4.23}$$

From (4.23), the product of output conductances should approach zero for high-gain. This implies that the transfer function of (4.23) has a dominant pole close to DC and a non-dominant pole at a higher frequency. The non-dominant pole can be found by assuming that the dominant pole frequency is zero which enables us to solve a first-order equation:

$$s \approx -\frac{(g_{ds1}(C_{pc2}+C_{L2})+g_{ds2}(C_{p1}+C_{p2}+C_{L1})+g_{m2}C_{p2})}{C_{p2}C_{L2}^2+C_{p2}C_{L1}+C_{p1}C_{L2}+C_{L1}C_{L2}+C_{p1}C_{p2}} \tag{4.24}$$

Simplifying (4.24) results in

$$s \approx -\frac{g_{m2}C_{p2}}{C_{p2}C_{L2}^2+C_{p2}C_{L1}+C_{p1}C_{L2}+C_{L1}C_{L2}+C_{p1}C_{p2}} \tag{4.25}$$

The two poles of the amplifier are widely separated and thus, the location of the non-dominant pole frequency is determined approximately by g_{m2} and the compensation capacitor C_{p2}. Thus, the location of the dominant pole is determined with respect to the input stage (assuming g_{ds1} and g_{ds2} are much smaller than g_{m2}). The combination of g_{m2} and C_{p2} control the separation of the poles.

Due to the complexity (4.22), it is difficult to find the characteristic roots of the polynomial. This is even more true for multi-stage amplifiers. Fortunately, one can simulate the pole-zero movements due to each component in the system using SPICE. This simulation can help us understand the role of each component in the frequency response of the amplifier. A simple program written in Perl allows us to change the component values and use SPICE to find the pole and zero of the transfer function. Figure 4.6 illustrates pole-zero movements according to (4.22) and Figure 4.4. Figure 4.6(a) shows the effect of increasing C_{p1}: We need to minimize C_{p1} since both poles

move to lower frequencies and are not split as desired. Figure 4.6(c) shows pole/zero

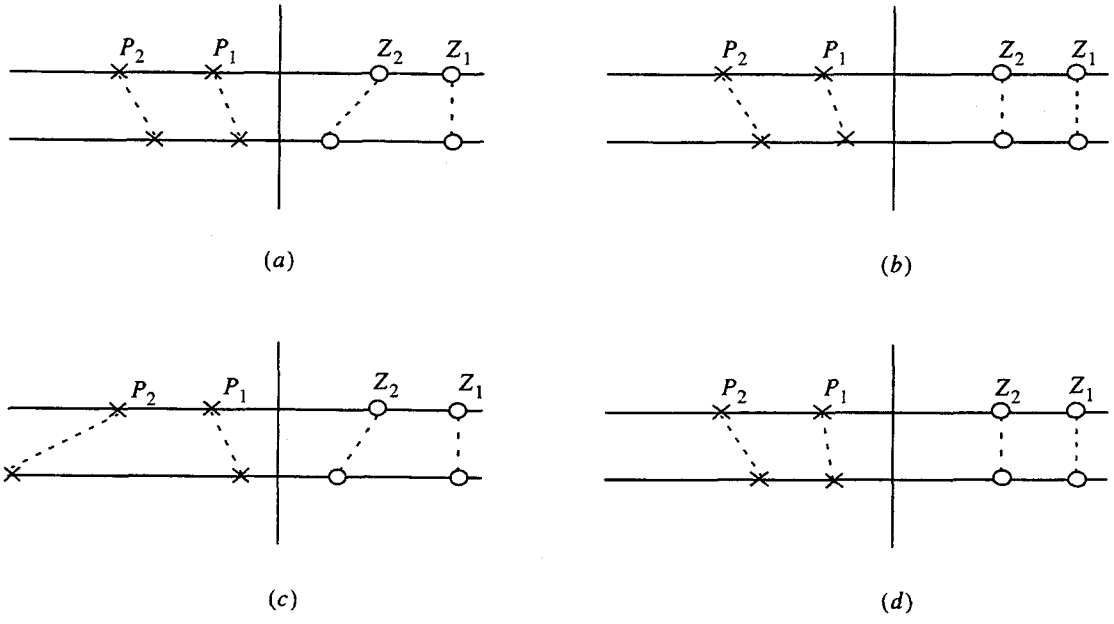

Figure 4.6. Pole-zero plots for the transfer function of (4.20) versus (a) C_{p1}, (b) C_{L1}, (c) C_{p2}, and (d) C_{L2}.

movements for C_{p2} increased. Note that the two poles split. Therefore, parasitic C_{p2} is replaced by the compensation capacitor C_{c2} to split the poles as desired. Figures 4.6(b) and (d) show the pole and zero movements when the load capacitances C_{L1} and C_{L2} are increased. From Figure 4.5(b), it is important to reduce the parasitic load capacitance of the first stage to avoid a decrease in bandwidth since the relative distance between the dominant and non-dominant poles decreases. Also, from Figure 4.5(d), C_{L2} represents the load capacitance that we drive the amplifier with. For large C_{L2}, C_{p2} must increase

proportionally in order to maintain stability; this at the same time reduces the bandwidth due to each component increased.

In general, a compensation capacitor alone is not sufficient to achieve high performance in an operational amplifier. As shown earlier, this compensation scheme also a RHP zero to lower frequencies as the compensation capacitor is increased. To improve the compensation, an RC network is used to move the RHP zero back to its parasitic location and to introduce a LHP zero which can be used to cancel the non-dominant pole. Figure 4.7 shows RC compensation for a two-stage amplifier.
The effect of the compensation resistance and on the pole-zero movements is drawn in

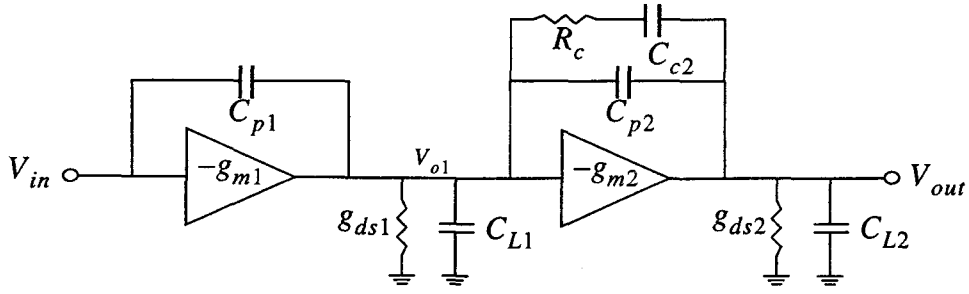

Figure 4.7. Small-signal representation of a two-stage amplifier with an RC Miller compensation network.

Figure 4.8 [12]. Note the new pole-zero pair introduced by the addition of resistor R_c. As R_c is increased, the RHP zero moves into the LHP and eventually cancels the non-dominant pole as shown in Figure 4.8. Caution must be exercised in choosing the compensation capacitance. If C_{c2} is too small, increasing R_c will cause the pole associated with the resistor to form a complex conjugate pair with the non-dominant pole

before as in Figure 4.8(b). Even though a complex conjugate pair with the LHP zero is stable response, it is undesirable C_{c2} becoming large may avoid forming the complex pair as shown in Figure 4.8(a). As we will see later, we can take advantage of this phenomenon to attain a stable amplifier with more gain stages. We can conclude that the migration of the resistor pole towards lower frequencies can be controlled by the compensation capacitor C_{c2}. For large C_{c2}, the resistor pole does not move as fast as the zero allowing it to cancel the non-dominant pole. C_{c2} keeps the resistor pole at high frequencies while it allows the zero to move to lower frequencies.

4.3 Three-Stage Amplifier Compensation

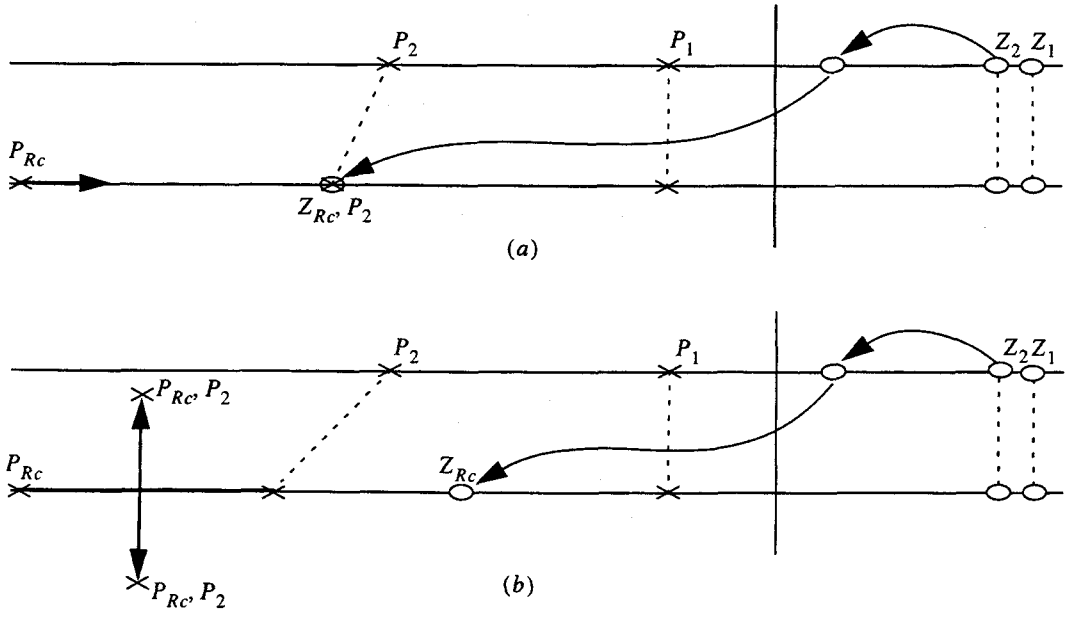

Figure 4.8. The effect of R_c on the poles and zeros after pole splitting by C_{c2}. (a) Where C_{c2} is quiet large. (b) Where C_{c2} is quiet small.

The g_m block diagram for a three-stage amplifier is shown in Figure 4.9. Where, ideal transconductors represent the gain stages each, with an equivalent output conductance and load capacitance. Across the gain stages, the parasitic intended compensation capacitances are connected. Note that the feedback capacitors are connected locally and not nested as in the Nested Miller configuration [2].

Next, we determine the transfer function of each gain stage along with the overall transfer function of the operational amplifier.

We begin with nodal analysis of each node. Starting at V_{o1},

$$V_{in}(sC_{p1} - g_{m1}) = V_{o1}[s(C_{p1} + C_{p2} + C_{L1}) + g_{ds1}] - V_{o2}sC_{p2} \quad (4.26)$$

at V_{o2}, we have

$$V_{o1}(sC_{p2} - g_{m2}) = V_{o2}[s(C_{p2} + C_{p3} + C_{L2}) + g_{ds2}] - V_{out}sC_{p3} \quad (4.27)$$

and finally at V_{out}, we obtain

$$V_{o2}(sC_{p3} - g_{m3}) = V_{out}[s(C_{p3} + C_{L3}) + g_{ds3}] \quad (4.28)$$

We can solve (4.28) to find the transfer function of the third stage as

$$\frac{V_{out}}{V_{o2}} = \frac{[s(C_{p3} + C_{L3}) + g_{ds3}]}{(sC_{p3} - g_{m3})} \quad (4.26)$$

Note that the output stage has one pole and one zero associated with it corresponding to

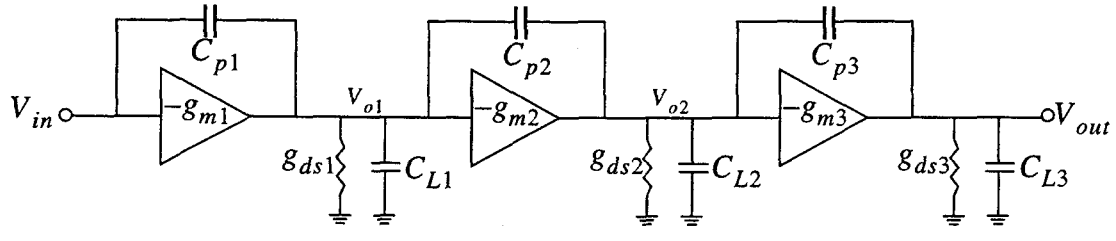

Figure 4.9. Small-signal representation of a three-stage amplifier.

the RC time constant at the output node. Next, we can solve (4.28) for V_{out} and substitute into (4.28) to find the transfer function of the second stage,

$$\frac{V_{o2}}{V_{o1}} = \frac{(sC_{p2} - g_{m2})[s(C_{p3} + C_{L3}) + g_{ds3}]}{s^2(C_{p2}C_{p3} + C_{L2}C_{p3} + C_{p2}C_{c3} + C_{L2}C_{L3}) +}$$

$$\overline{s[g_{ds2}(C_{p3} + C_{L3}) + g_{ds3}(C_{p2} + C_{L2} + C_{p3})] + g_{ds2}g_{ds3}} \quad (4.30)$$

We can simplify (4.30) by replacing coefficients with variables as in

$$\frac{V_{o2}}{V_{o1}} = \frac{(sC_{p2} - g_{m2})[s(C_{p3} + C_{L3}) + g_{ds3}]}{As^2 + Bs + C} \quad (4.31)$$

where

$$A = C_{p2}C_{p3} + C_{L2}C_{p3} + C_{p2}C_{p3} + C_{L2}C_{L3} \quad (4.32)$$

$$B = g_{ds2}(C_{p3} + C_{L3}) + g_{ds3}(C_{p2} + C_{L2} + C_{p3}) \quad (4.33)$$

and

$$C = g_{ds2}g_{ds3} \quad (4.34)$$

Next, we find the firs-stage transfer function by solving (4.31) for V_{o2} and substituting it into (4.26) to get

$$\frac{V_{o1}}{V_{in}} = \frac{(sC_{p1} - g_{m1})(As^2 + Bs + C)}{s^3[A(C_{p1} + C_{p2} + C_{L1}) - C_{p2}^2(C_{p3} + C_{L3})] +}$$

$$\overline{s^2[Ag_{ds1} + B(C_{p1} + C_{p2} + C_{L1}) - C_{p2}^2 g_{ds3} + g_{m2}C_{p2}(C_{p3} + C_{L3})] +}$$

$$\overline{s[Bg_{ds1} + C(C_{p1} + C_{p2} + C_{L1}) + g_{m2}g_{ds3}C_{p2}] + g_{ds1}C} \quad (4.35)$$

We simplify (4.35) to

$$\frac{V_{o1}}{V_{in}} = \frac{(sC_{p1} - g_{m1})(As^2 + Bs + C)}{Ds^3 + Es^2 + Fs + G} \quad (4.36)$$

where

$$D = A(C_{p1} + C_{p2} + C_{L1}) - C_{p2}^2(C_{p3} + C_{L3}) \tag{4.37}$$

$$E = Ag_{ds1} + B(C_{p1} + C_{p2} + C_{L1}) - C_{p2}^2 g_{ds3} + g_{m2}C_{p2}(C_{p3} + C_{L3}) \tag{4.38}$$

$$F = Bg_{ds1} + C(C_{p1} + C_{p2} + C_{L1}) + g_{m2}g_{ds3}C_{p2} \tag{4.39}$$

and

$$G = g_{ds1}C \tag{4.40}$$

Finally, we find an expression for the overall transfer function of the operational amplifier by multiplying the individual transfer functions as

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{o2}} \cdot \frac{V_{o2}}{V_{o1}} \cdot \frac{V_{o1}}{V_{in}} \tag{4.41}$$

Using the expressions obtained for each transfer function, we obtain

$$\frac{V_{out}}{V_{in}} = \frac{(sC_{p3} - g_{m3})}{[s(C_{p3} + C_{L3}) + g_{ds3}]} \cdot \frac{(sC_{p2} - g_{m2})[s(C_{p3} + C_{L3}) + g_{ds3}]}{As^2 + Bs + C} \cdot$$

$$\frac{(sC_{c1} - g_{m1})(As^2 + Bs + C)}{Ds^3 + Es^2 + Fs + G} \tag{4.42}$$

and, simplifying we get

$$\frac{V_{out}}{V_{in}} = \frac{(sC_{p1} - g_{m1})(sC_{p2} - g_{m2})(sC_{p3} - g_{m3})}{Ds^3 + Es^2 + Fs + G} \tag{4.43}$$

From (4.42), two cancellations were seen to occur. The pole of the output stage is cancelled by a zero of the second stage, and the two poles associated with the second stage are cancelled by the two zeros of the first stage! The overall transfer function produces a third-order polynomial as expected, but the poles in effect are "referred" to the input stage. Simulation results for the uncompensated three-stage amplifier of Figure 4.9 are shown in Figure 4.10. Note in Figure 4.10(a) the pole-zero cancellations

predicted by (4.42). The overall response in Figure 4.10(b) corresponds to (4.43). The

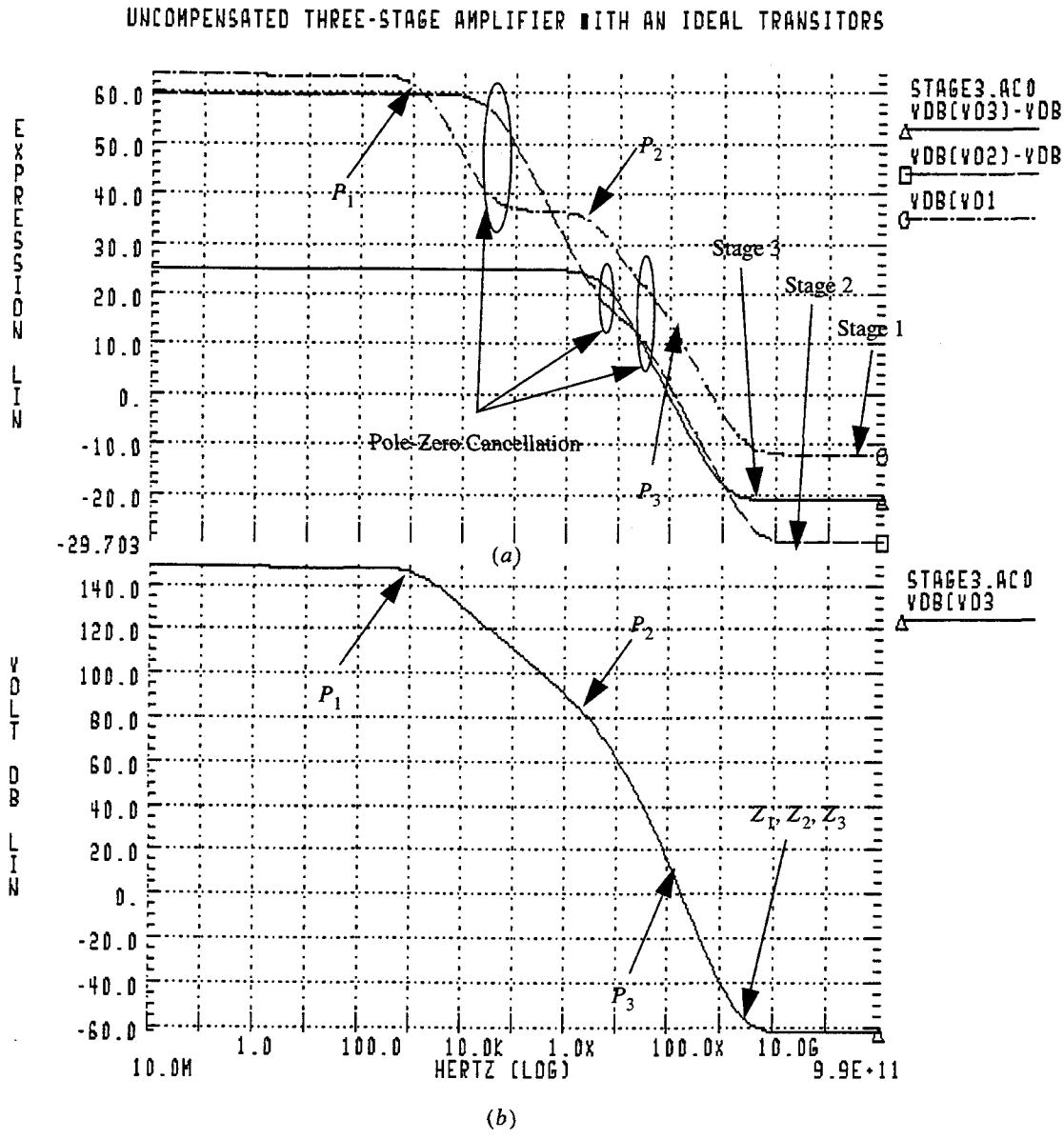

Figure 4.10. Frequency response of an uncompensated three-stage amplifier. (a) Individual gain stage responses, and (b) overall response.

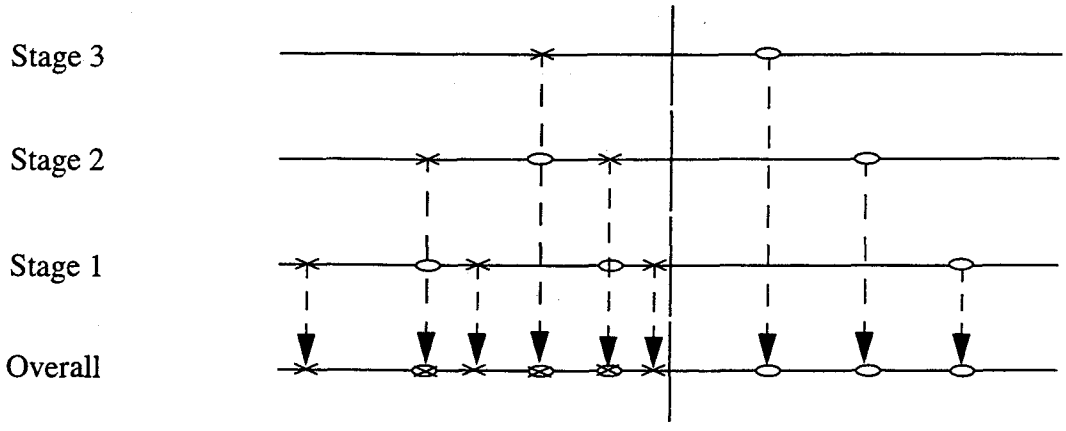

Figure 4.11. Pole-zero plots for the transfer functions of (4.30), (4.31), and (4.34), and (4.43).

pole-zero plots of individual transfer function and the overall transfer function are shown in Figure 4.11. Note that there are a total of three pole-zero cancellations in the overall transfer function.

From (4.43), it can be seen that the DC term is equivalent to the product of the output conductances of each stage. For a high-gain three-stage amplifier, the DC term of the transfer function is close to zero, resulting in a dominant pole close to s=0, and two non-dominant poles much higher frequencies. Thus, if we assume that the dominant pole is equal to zero, the third-order polynomial reduces to a second-order polynomial with two non-dominant poles in which both are at relatively higher frequencies than the dominant pole frequency.

Next, we to consider the role of the feedback (intended or parasitic) and the load capacitances of each stage on the pole-zero characteristics. There are six capacitors that need to be considered: Three correspond to load capacitances and three correspond to compensation/parasitic capacitances across each stage. The results on the overall transfer function with respect to all six parameters being increased one at a time are shown in

Figure 4.12. From these results, we obtain important insights into how three-stage amplifiers should be compensated. For example, in Figure 4.12(a) C_{p1} is not an intelligent choice for compensation since all poles migrate to lower frequencies and no pole splitting behavior is observed. As a result, we should the parasitic capacitance C_{p1}. However in Figure4.12(b), we see that by increasing C_{p2}, a the dominant pole is created

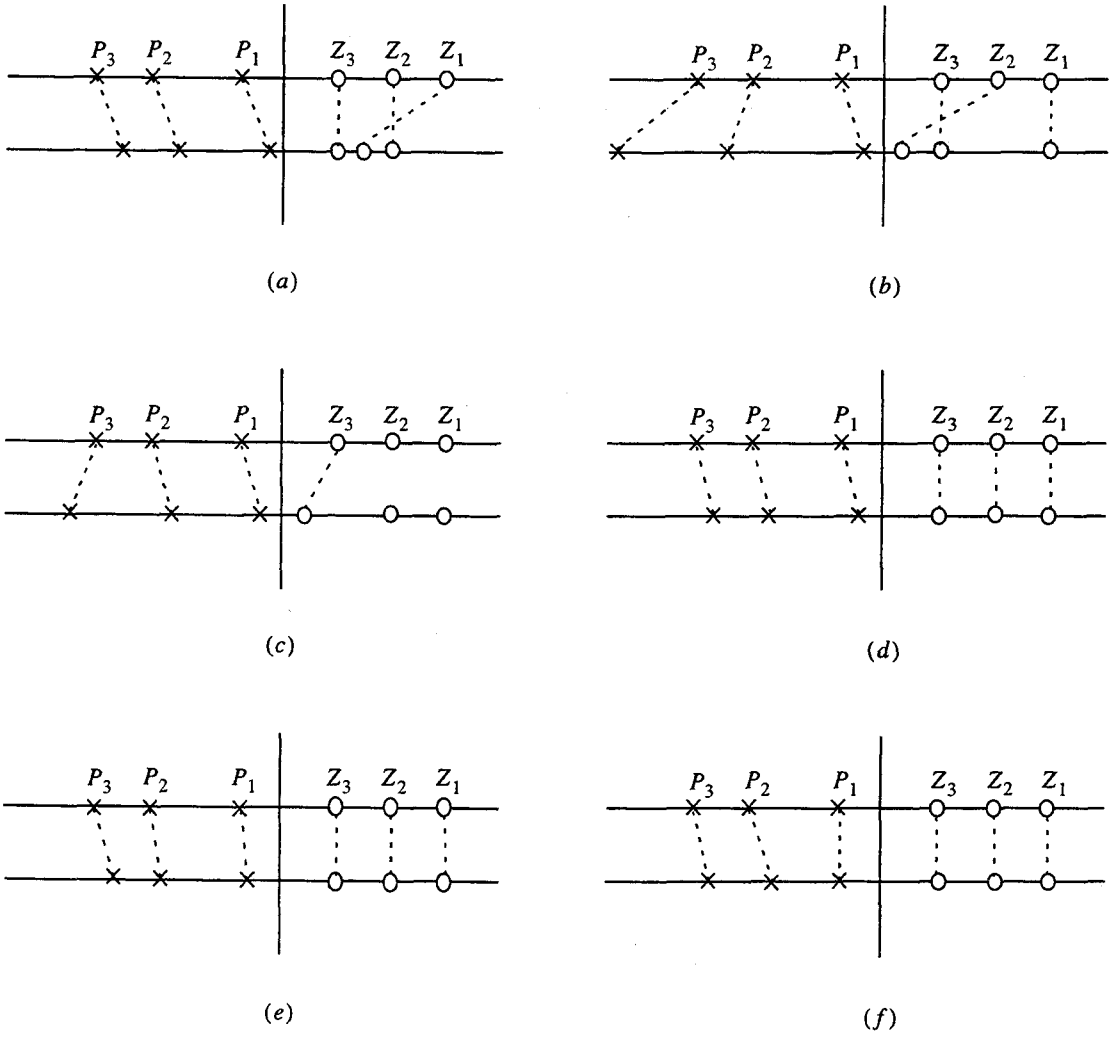

Figure 4.12. Pole-zero plots for the transfer function of overall transfer function of (4.43) versus (a) C_{p1}, (b) C_{p2}, (c) C_{p3}, (d) C_{L1}, (e) C_{L2}, and (f) C_{L3}.

with two non-dominant poles at higher frequencies. Clearly, C_{p2} this is a superb choice for compensation since pole-splitting behavior is observed. In Figure 4.12(c), increasing C_{p3} causes the pole splitting between the non-dominant pole and the most non-dominant pole. This is also desirable since the first non-dominant pole moves to lower frequencies along with the dominant pole. Figure 4.12(d) presents C_{L1} being increased, causes all poles to move to lower frequencies; hence, it is desirable to minimize C_{L1}. Figure 4.12(e) shows the response when C_{L2} is increased which is similar to Figure 4.12(d); the rate at which the poles move is slower than C_{L1}. Finally, an important result is obtained by increasing C_{L3} as shown in Figure 4.12(f). The dominant pole is unaffected while the non-dominant poles move to lower frequencies. This effect can be compensated by increasing C_{c2}. In conclusion, increasing C_{L3} effects only the non-dominant poles which degrade the stability performance, but bandwidth is remained constant. This is an important result in terms of driving large load capacitances and maintaining bandwidth by increasing C_{p2} to maintain stability.

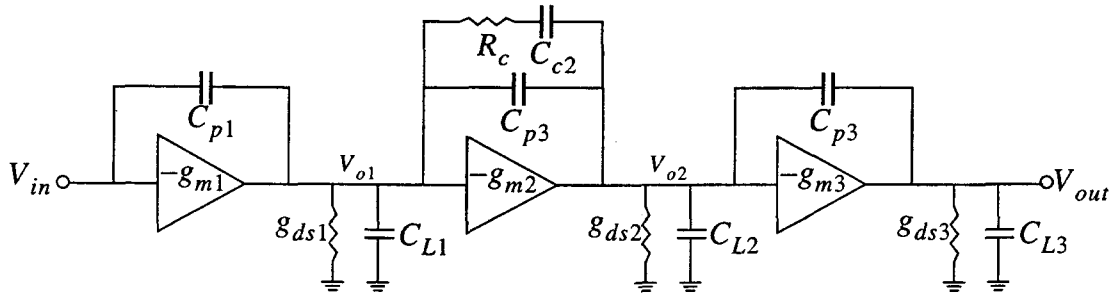

Figure 4.13. Small-signal representation of a three-stage amplifier with an RC compensation network.

For compensating a three-stage amplifier, one should use a compensation capacitance C_{c2} for pole splitting. From Figure 4.12(b), the RHP zero associated with the second stage to move to lower frequencies as for the two-stage amplifier. For this reason, an RC compensation network is again required. Figure 4.13 shows the compensation network for a three-stage amplifier where C_{p1} and C_{p3} are parasitic capacitances. The RC compensation network introduces another pole-zero pair with, the zero used to cancel the first non-dominant pole. Figure 4.14 shows the pole-zero movements when C_{c2} is fixed and R_c is increased.

From Figure 4.14, the zero due to R_c is used to cancel the first non-dominant pole. At the same time, the most non-dominant pole moves to a high frequency with the pole associated with the compensation resistor R_c and forms a complex conjugate pair. The complex pair can be made to occur at frequencies well beyond the unity-gain frequency if C_{p2} is chosen properly. Thus, the overall system has a one-pole response within the unity-gain bandwidth. In Chapter 5, we consider the analysis and design of this type of amplifier. Another important consideration is how large R_c can become. As R_c is increased, the poles form a complex conjugate pair, and if R_c is increased further, the complex pair moves to lower frequencies eventually, causing instability. In Chapter 3,

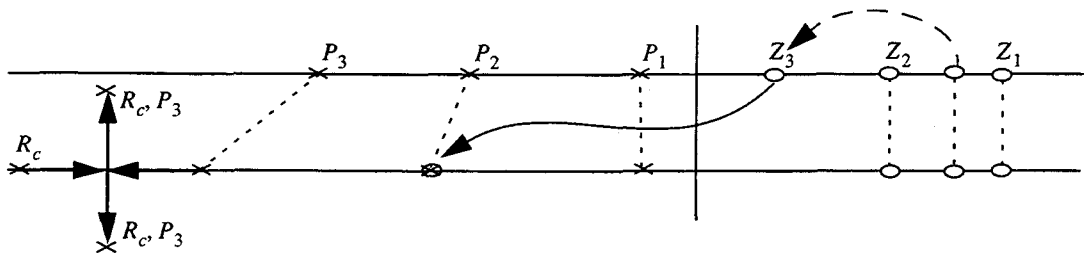

Figure 4.14. The effect of R_c on the poles and zeros after pole splitting by C_{c2}.

we analyzed the effects of a complex conjugate pair on the amplifier characteristics, and

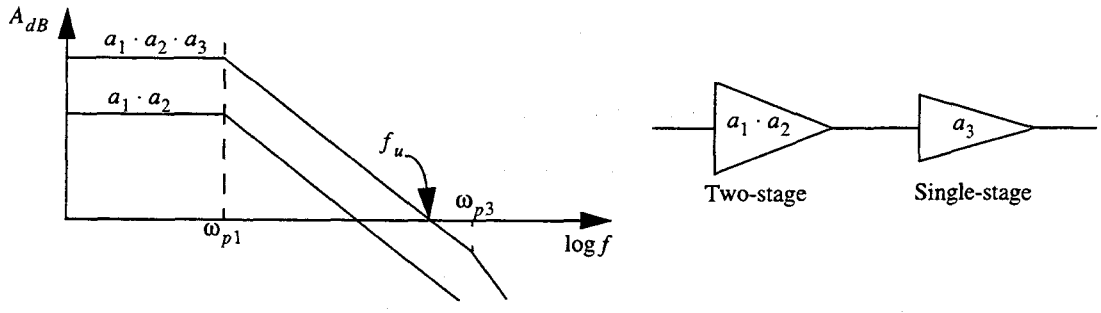

Figure 4.15. Two-stage followed with a single-stage amplifier.

concluded that the pair must be located at greater than three times the unity-gain frequency for the desired stability margins and settling times. A solution to the movement of the complex pair towards lower frequencies is to increase C_{c2}. Only a small value of R_c is needed to cancel the first non-dominant pole with the zero. If a large value of C_{c2} is used, the complex conjugate pair becomes real. The value of the feedback capacitor is proportional to g_m as mentioned in Chapter 2. In order to increase g_m to obtain higher bandwidth and maintain stability of the amplifier, C_{c2} must increase proportionally. There are area limitations as to how large C_{c2} can become. In the design process, C_{c2} must be adjusted with R_c to achieve the desired phase and gain margins. If the value of C_{c2} is increased to achieve higher stability with g_m constant, the bandwidth decreases pushing the dominant pole to a lower frequency. To overcome this effect, g_m must be increased. Optimum values can be obtained as shown in Chapter 3.

The design of a three-stage operational amplifier can be visualized with reference to by Figure 4.15. The operational amplifier can be viewed as a two-stage amplifier followed by a single-stage amplifier. A compensated two-stage amplifier has a one-pole response with the dominant pole at ω_{p1}. The pole associated with the second-stage of the two-stage amplifier is cancelled by a zero introduced by the compensation network. By assuming that pole associated with the third-stage is located at a much higher frequency, a one-pole response with a gain-bandwidth product proportional to the gain of the third-stage is realized. For example, if the two-stage amplifier gain bandwidth product is 10 MHz and the gain of the third-stage is 20 dB, the gain bandwidth product of the three-stage amplifier is 100 MHz, a factor of ten improvement in frequency compared to the two-stage case.

So far, we have studied the effects of compensation and parasitic components on the frequency responses. Next, we consider the effects of second- and third-stage sizes on the pole-zero responses. We begin by considering an almost compensated three-stage amplifier as represented by Figure 4.16. Note that the position of the complex conjugate pair with respect to the dominant pole causes inadequate unity-gain frequency, gain, and phase margins. Also, we included a pole-zero doublet pair assuming imperfect doublet cancellation. Consider g_{m3} as shown in Figure 4.13. It is desirable to have g_{m3} large to achieve high slew rates. So g_{m3}, we observe the behavior of the poles and zeros on the s-plane as shown in Figure 4.17. An important observation is that the dominant pole moves towards higher frequencies as g_{m3} is increased. This implies that as the unity-gain frequency increases, the complex conjugate pair does not move much, resulting in a degradation of phase and gain margins. The doublet spacings also increases. The position of Z_R can be changed by increasing the feedback resistor, but this pulls the complex pair towards lower frequencies which forces an increase in C_{c2}. Thus,

increasing the size of the output stage for better slew rate degrades the stability of the

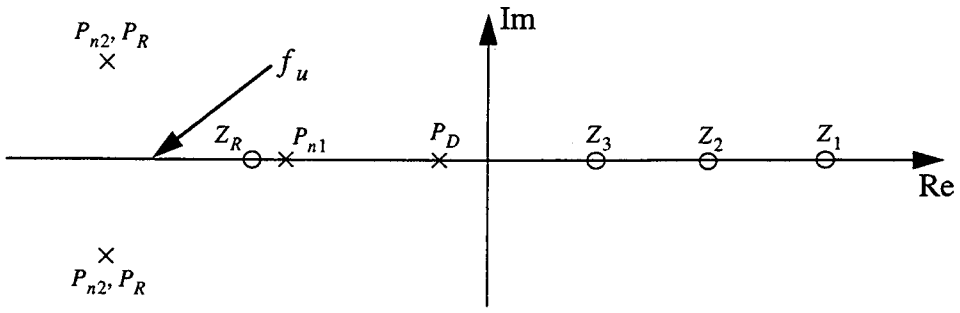

Figure 4.16. Pole-zero plot of an almost compensated three-stage amplifier.

amplifier.

Now let us analyze the effects of the g_{m2} on the pole-zero responses. The results of the simulations are presented in Figure 4.18. We can show that increasing g_{m2} has several advantages. First, the conjugate pair moves to higher real and imaginary frequencies which is beneficial. Also, doublet spacing decreases which is highly desirable. However, the dominant pole moves to lower frequencies resulting in reduced bandwidth. We can obtain some intuition on the advantages of judiciously sizing the second and third gain stages.

The frequency response of the compensated three-stage amplifier (not optimized) of Figure 4.13 is shown in Figure 4.19.

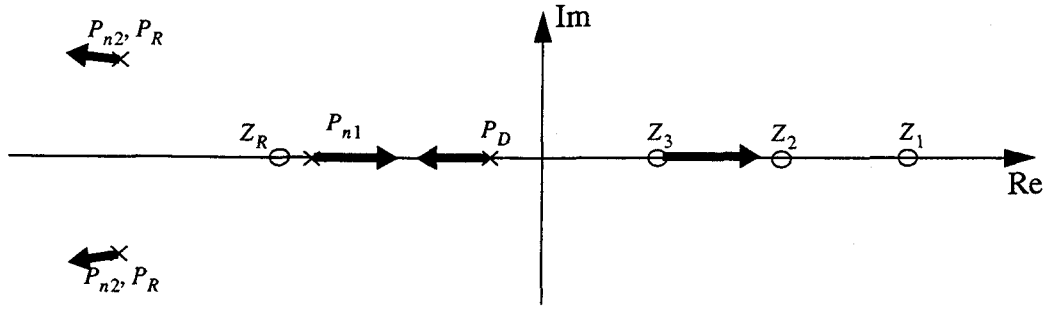

Figure 4.17. Pole-zero plots as a function of g_{m3}.

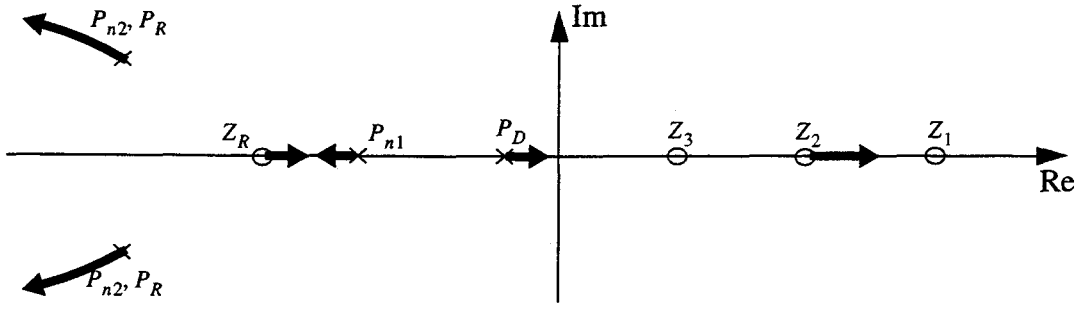

Figure 4.18. Pole-zero plot as a function of g_{m2}.

4.4 Summary

From this chapter, several important results can be summarized as followings:

- The feedback capacitor across the second stage, C_{c2}, is the best to use for pole-splitting between the dominant and non-dominant poles.
- The feedback resistor R_c in series with C_{c2} pushes the RHP zero back to its original location prior to compensation. It also introduces a pole-zero pair where, the zero is used to cancel the first non-dominant pole.
- The RC compensation network may cause a complex conjugate pair of poles to form beyond the unity-gain frequency if a proper C_{c2} value is used.
- C_{c2} can be used to move the complex pair to higher frequencies.
- Increasing C_{c2}, reduces bandwidth. As a result, the g_m of the first-stage must increase to maintain the desired gain-bandwidth product.
- For better slew rate, the output stage must be large, but this causes the dominant pole to move to higher frequencies which increases the bandwidth. Furthermore, this causes the relative spacing in between the dominant pole and the complex conjugate pair to decrease which decreases the stability measures.
- Second-stage transistor sizing improves the stability of the amplifier by moving the complex pair to higher frequencies along both the real and imaginary axes. It decreases the doublet spacing at the cost of lower bandwidth.
- The combination of second-and third-stage sizings increase stability with high performance if designed properly.

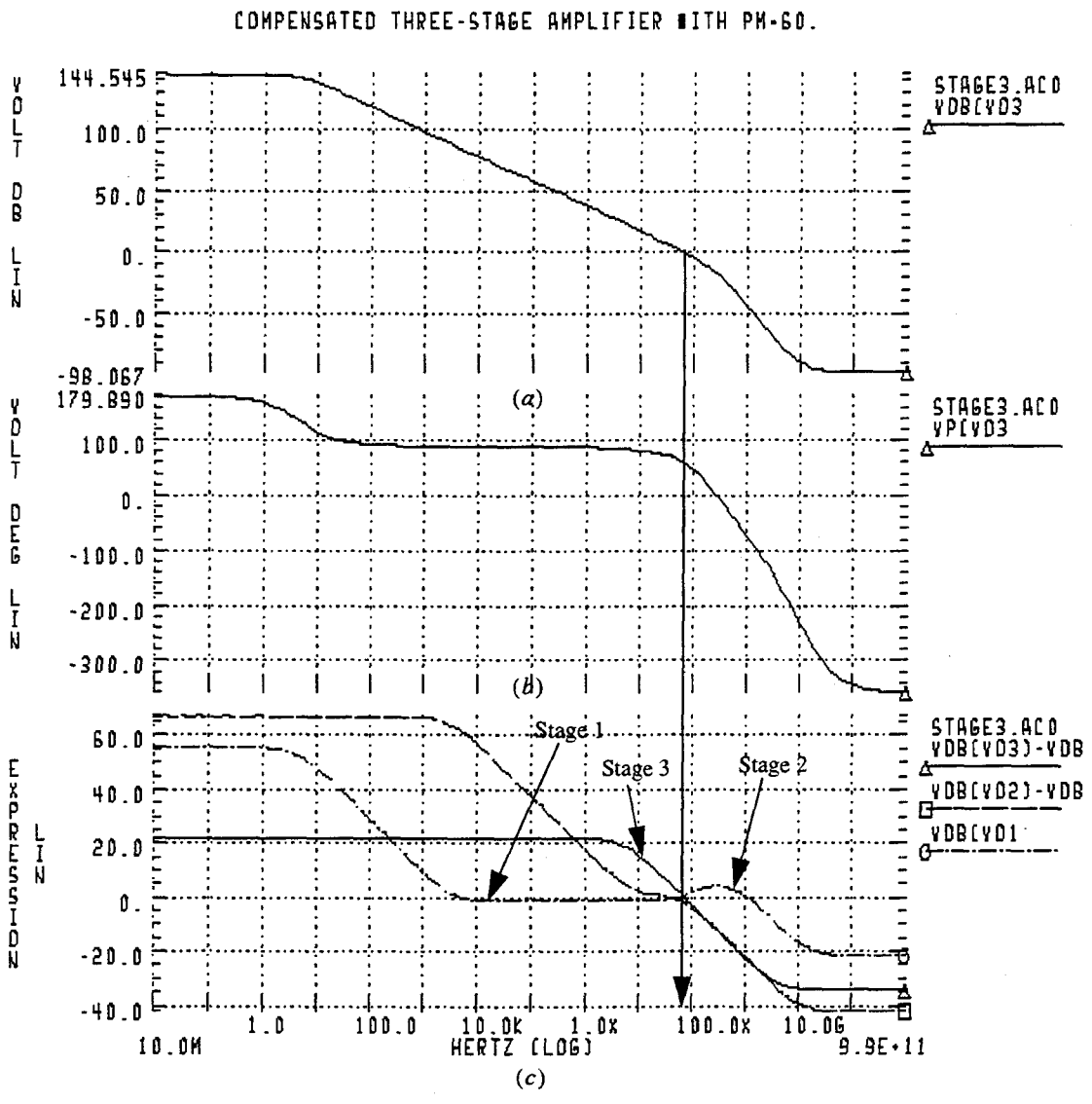

Figure 4.19. Frequency response of a compensated three-stage amplifier. (a) Magnitude response. (b) Phase response. (c) individual gain stage response.

Chapter 5. Three-Stage Amplifier Circuit Design and Realization

In typical situations, high open-loop gain of a two-stage amplifier with high-speed and high slew rate are not easily achievable because there exist strong trade-off among these performance parameters. One way to achieve high-gain in a two-stage operational amplifier is to increase the channel lengths, but this limits the bandwidth. In order to increase slew rate, the sizes of the second-stage devices must be made large to charge the load plus compensation capacitors. This increases power dissipation and power per bandwidth which is undesirable.

In this thesis, a new multi-stage amplifier is proposed which overcomes trade-offs of two-stage operational amplifiers. In this chapter, the design of a high-gain, high-speed, high-slew rate, and low power-per-bandwidth three-stage operational amplifier is discussed. Some basic relationships between gain, bandwidth, slew rate, and other parameters of the amplifier are considered, and simulation results are presented.

5.1 Overview of a Basic Amplifier Design

A one-stage amplifier and the current/voltage characteristics of the NMOS driver device are shown in Figure 5.1. Figure 5.1(a) shows a simple common-source amplifier with ideal current source load and load capacitance C_L. The small-signal output conductance comprises that of the current source plus that of the transistor. Since ideal current source has zero output conductance and the conductance C_L is zero, the only conductance, is that of the transistor. Figure 5.1(b) I-V plots versus V_{GS}. The

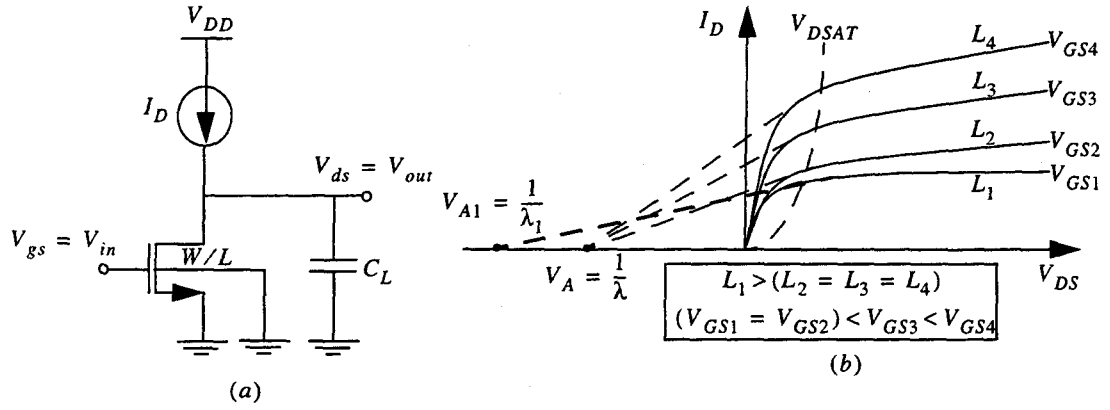

Figure 5.1. (a) NMOS Common-source amplifier. (b) I-V characteristics.

characteristics of Figure 5.1(b) comprise three regions of operation; namely, cutoff, non-saturation, and saturation. The first-order equations corresponding to the three regions

Table 5 .1 **Characteristic Equations for an NMOS Transistor.**

Cutoff	$V_{GS} \leq V_T$	$I_D = 0$
Non-Saturation	$(V_{GS} - V_T) > 0$ $(V_{GS} - V_T) > V_{DS}$	$I_D = \left(\frac{k'}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
Saturation	$(V_{GS} - V_T) \geq 0$ $(V_{GS} - V_T) \leq V_{DS}$	$I_D = k'\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right](1 + \lambda V_{DS})$

are listed in Table 5.1. The term $(1 + \lambda V_{DS})$ represents channel-length modulation with $\lambda = 1/V_A$ where V_A is the early voltage or equivalently the extrapolated intersection point of all saturation curves as shown in Figure 5.1(b). The term k' is

$$k' = \mu C_{ox} \tag{5.1}$$

where μ is the carrier mobility and C_{ox} is the gate-oxide capacitance per unit area. According to Figure 5.1(b), the boundary point between saturation and non-saturation is the saturation voltage V_{DSAT},

$$V_{DSAT} = (V_{GS} - V_T) \tag{5.2}$$

In most analog circuits the region of interest for MOS operation is the saturation region where in drain current is nearly constant with respect to changes in V_{ds}. Saturation region operation provides a small drain-to-source conductance g_{ds}.

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \cong \lambda I_D \tag{5.3}$$

When a small-signal v_{gs} is applied to the input, a corresponding small-signal current i_{ds} flows through the output. The corresponding small-signal transconductance g_m is

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = k'\left(\frac{W}{L}\right)(V_{GS} - V_T)(1 + \lambda V_{DS}) \cong k'\left(\frac{W}{L}\right)(V_{GS} - V_T) \tag{5.4}$$

(5.4) expresses g_m as a function of V_{GS}, but we can also express it as

$$g_m = \sqrt{\frac{2k'\left(\frac{W}{L}\right)I_D}{(1 + \lambda V_{DS})}} \cong \sqrt{2k'\left(\frac{W}{L}\right)I_D} \tag{5.5}$$

and

$$g_m = \frac{2I_D}{(V_{GS} - V_T)} \tag{5.6}$$

In Figure 5.1(a) the back-gate terminal is connected to ground so that $V_{SB} = 0$. In the case where $V_{SB} \neq 0$, the associated back-gate transconductance g_{mbs} is

$$g_{mbs} = \frac{\gamma}{2\sqrt{V_{SB} + 2\Phi_f}} g_m \tag{5.7}$$

where γ and $2\Phi_f$ are process parameters. In this thesis, all simulations are based on a CMOS N-well $0.6\mu m$ technology.

When $V_{SB} \neq 0$, the threshold voltage of an NMOS device takes the following form

$$V_T = V_{T0} + \gamma(\sqrt{V_{SB} + 2\Phi_f} - \sqrt{2\Phi_f}) \tag{5.8}$$

where V_{T0} is the threshold voltage with $V_{SB} = 0$.

From at Figure 5.1(a), we can determine an expression for the voltage gain of the amplifier. For the small-signal input voltage v_{in}, drain current is generated proportional to g_m which flows through the output conductance g_{ds} to produce v_{out}. Thus, the gain of the amplifier given by

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds}} \tag{5.9}$$

The negative sign corresponds to signal inversion or a 180° phase-shift between the input and output signals. From Figure 5.1(b), the slopes in the saturation region correspond to output conductances. Since $\lambda \propto 1/L$, longer channel lengths provide lower output conductance and higher voltage gain. (5.9) can further be used to express voltage gain versus bias current as

$$\frac{v_{out}}{v_{in}} \cong -\frac{\sqrt{2k'\left(\frac{W}{L}\right)I_D}}{\lambda I_D} \propto \frac{1}{\sqrt{I_D}} \propto \sqrt{L} \tag{5.10}$$

or versus saturation voltage as

$$\frac{v_{out}}{v_{in}} = -\frac{2I_D/(V_{GS} - V_T)}{\lambda I_D} \propto \frac{1}{(V_{GS} - V_T)} \tag{5.11}$$

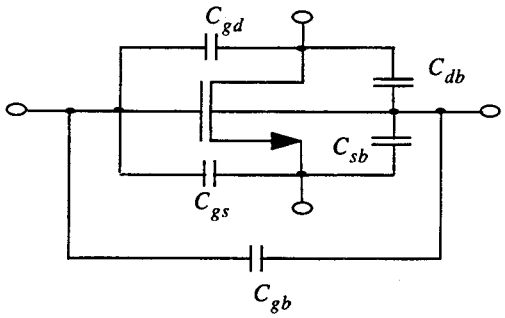

Figure 5.2. MOS parasitic capacitances.

From (5.11), as $(V_{GS}-V_T)$ goes to zero the gain of the amplifier approaches infinity. In reality, of course, this is not true. There is a limit to how small $(V_{GS}-V_T)$ can become before the device enters weak inversion layer at which point the equations in Table 5.1 are no longer valid. This effect does not occur in BJT devices.

We next consider the frequency dependent behavior of the single-stage amplifier of Figure 5. As shown in Figure 5.2 [13], there are five important parasitic capacitances associated with a MOS device: C_{gd}, C_{gb}, C_{gs}, C_{sb}, and C_{db}. The corresponding equations in saturation are

$$C_{gd} = C_{gd0} \cdot W \tag{5.12}$$

$$C_{gb} = C_{gb0} \cdot L \tag{5.13}$$

$$C_{gs} = C_{gs0} \cdot W + \frac{2}{3} C_{ox} W (L - 2L_D) \tag{5.14}$$

$$C_{sb} = \underbrace{\frac{C_j \cdot AS}{\left[1 + \frac{V_{DB}}{P_B}\right]^{mj}}}_{\text{Bottom-Wall}} + \underbrace{\frac{C_{jsw} \cdot PS}{\left[1 + \frac{V_{DB}}{P_B}\right]^{mjsw}}}_{\text{Side-Wall}} \tag{5.15}$$

and

$$C_{db} = \underbrace{\frac{C_j \cdot AD}{\left[1 + \frac{V_{DB}}{P_B}\right]^{mj}}}_{\text{Bottom-Wall}} + \underbrace{\frac{C_{jsw} \cdot PD}{\left[1 + \frac{V_{DB}}{P_B}\right]^{mjsw}}}_{\text{Side-Wall}} \tag{5.16}$$

where C_{gd0}, C_{gs0}, C_{gb0}, L_D, C_{jsw}, C_j, P_B, mj, and $mjsw$ are process parameters. AS, AD, PS, and PD are the areas and perimeters of the source and drain, respectively. Using the complete small-signal model, we can find the transfer function of the common-source amplifier as

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds}} \frac{\left(1 - s\frac{C_{gd}}{g_m}\right)}{\left[1 + s\frac{(C_{gd} + C_{db} + C_g)}{g_{ds}}\right]} \tag{5.17}$$

where C_g is the total gate capacitance of a similar stage loading the output. We can simplify (5.17) by assuming that

$$C_g > C_{gd} + C_{db} \tag{5.18}$$

where the gate capacitance of the following stage is approximately

$$C_g = C_{ox} \cdot W \cdot L \tag{5.19}$$

Hence, the pole frequency of the amplifier is approximately

$$\omega_P = \frac{g_{ds}}{C_g} \tag{5.20}$$

(5.20) can also be written as

$$\omega_P = \frac{\lambda I_D}{C_{ox} \cdot W \cdot L} \propto \frac{1}{L^2} \propto I_D \tag{5.21}$$

Finally, we find an expression for the gain-bandwidth product of amplifier as

$$\omega_T = \frac{g_m}{g_{ds}} \cdot \frac{g_{ds}}{C_g} = \frac{g_m}{C_g} \tag{5.22}$$

(5.22) can also be written as

$$\omega_T = \frac{\sqrt{2k'(W/L)I_D}}{C_{ox} \cdot W \cdot L} \propto \sqrt{I_D} \propto \frac{1}{L\sqrt{L}} \qquad (5.22)$$

The result of (5.23) is important in understanding gain/speed trade-off. Increasing L provides lower output conductance resulting in higher gain, the speed decreases as $1/(L\sqrt{L})$.

From the results above, gain and bandwidth are major design trade-off associated in a single-stage amplifier. In order to achieve both high gain and high bandwidth, one is therefore motivated to consider multi-stage amplifiers as discussed in Chapter 4.

5.2 Design Methodology of Multi-Stage Operational Amplifiers

In the last section, we explored trade-off that can effect performance of a single stage amplifier. A one-stage cannot provide both high gain and high bandwidth. As the signal processing applications increase, performance requirements of the analog blocks become more challenging. Traditional amplifier designs are no longer optimum for low-power and low-voltage applications.

In the previous chapters some important characteristics of operational amplifiers were reviewed. Next we outline important specifications of a high-performance operational amplifier:

- High gain for video or audio applications (100 dB-120 dB)
- High bandwidth for high-speed mixed-signal applications (> 100 MHz)
- Simple compensation technique
- Operating at low-voltages (1.8-3.0 V)
- Low power consumption ($20\mu W/(MHz \times pF)$)
- High slew rates (> 100-400 $V/\mu s$)

- Fast settling times for high settling accuracies
- Good noise performance

Based on what we have stated in previous chapters, we can outline high-performance operational amplifier design techniques

- Distribute gain among many gain stages
- Use the shortest channel lengths
- Avoid non-inverting single ended stages
- Achieve maximum swing at the output
- Achieve good stability in terms of phase and gain margins
- Use fully differential topologies for better noise, slew rate, CMRR, PSRR, and dynamic range performance
- Use large V_{DSAT} as to minimize transistor area
- Make the input stage pole dominant as discussed in Chapter4

Considering the requirements discussed above, it is clear that a multi-stage amplifier is needed to achieve these goals. We begin with a two-stage amplifier. A design for high gain of 120 dB requires each stage provide about 60 dB of gain which requires the use of cascode amplifiers for both stages. The cascode output stage limits the output swing voltage. To achieve such gains with common-source amplifiers, requires very long channel lengths thus yielding low-bandwidth. High-slew rate, and high-gain and bandwidth are impossible to achieve with two-stage amplifiers.

Now consider the advantages that a three-stage amplifier would offer:

- Use a folded-cascode input stage [14][15] to provide 40-50 dB of gain with short channel lengths. The output swing of this stage is small in a multi-stage topology.
- Use a cascode second stage to achieve another 50-60 dB of gain with short channel lengths, the output swing is also small for this stage.

- Use a common-source amplifier at the output with a gain of 20-30 dB for maximum slew rate and output voltage swing. According to Figure 4.15, this provides a 10X increase in gain/bandwidth over a two-stage amplifier.
- By designing so that the first stage is dominant, one can use large feedback compensation capacitors without loading the output stage. This provides efficient power-per-bandwidth and superb slew-rate performance.

The three-stage amplifier was able meet every requirement stated in the previous paragraph. We have already discussed the system-level simulation of a three-stage amplifier: In Chapter 2, we discussed its noise performance; in Chapter 3, its stability was compared to the two-stage amplifier, and finally in Chapter 4, a novel compensation technique was introduced similar to that used in a two-stage amplifier.

In Chapters 3 and 4, it was shown that an RC compensation network across the second stage provided a single-pole response past the unity-gain frequency with acceptable gain and phase margins. One important issue associated with multi-stage amplifiers is that the pole of the output stage is cancelled by a zero of the previous stage while the poles of the previous stage are cancelled with the zeros of its preceding stage, etc. Thus, the overall transfer function can be thought of as being referred to the input stage of the amplifier. By having the dominant pole on the first stage, we can determine its location based on the gain and load capacitance at that node. The gain-bandwidth product can then be determined by multiplying the gain-bandwidth product of the two-stage operational amplifier by the gain of the third stage.

5.3 Circuit Design of a Three-Stage Amplifier

We begin by analyzing the proposed circuit to determine its low-frequency gain. In Chapter 4, the design equations of uncompensated two- and three-stage operational

amplifiers were derived and computer simulations were used to study the effects of the compensation network and the parasitic and load capacitances. Figure 5.3 shows a design of a three-stage operational amplifier. It is fully-differential for better noise and dynamic range performance [16][17]. The gain is also increased 6 dB using a fully-differential configuration. We will analyze this circuit, using a differential-mode half circuit amplifier and add 6 dB of gain due to symmetry. The input stage is fully differential folded-cascode stage biased by constant current source MT. Half of the current in MT flows into M2. Another branch which includes transistors M3, M4, and M5 also provides current into M2. Generally M2 must handle the same current as MT. Hence, the current through the differential branch is equal to that in the cascode branch. This constraint provides maximum gain and speed for a given size. In small-signal analysis, at node V_1^-, the conductance due to the M3-M5 cascode branch is approximately g_{ds5}. The signal current generated from M1 can be written as

$$i_1 = g_{m1} v_{in}^+ \tag{5.24}$$

Current i_1 flows through the output load conductance resulting, in a gain of

$$\frac{v_{o1}^-}{v_{in}^+} = -\frac{g_{m1}}{g_{out}} \tag{5.25}$$

where g_{out} is the output conductance of the cascode stage given by

$$g_{out} \cong \frac{(g_{ds2} + g_{ds2}) \times g_{ds3}}{g_{m3}} + \frac{g_{ds4} \times g_{ds5}}{g_{m5}} \tag{5.26}$$

The second stage is a cascode stage with gain given by

$$\frac{v_{o2}^+}{v_{o1}^-} = -\frac{g_{m11}}{g_{out2}} \tag{5.27}$$

where g_{out2} is

$$g_{out2} = \frac{g_{ds11} \times g_{ds12}}{g_{m12}} + \frac{g_{ds13} \times g_{ds14}}{g_{m13}} \tag{5.28}$$

Finally, the gain of the common-source third stage is

$$\frac{v_{out}^{-}}{v_{o2}^{+}} = -\frac{g_{m19}}{g_{out3}} \tag{5.29}$$

where g_{out3} is

$$g_{out3} = g_{ds19} + g_{ds20} \tag{5.30}$$

The overall gain of the overall amplifier is therefore

$$\frac{v_{out}^{-}}{v_{in}^{+}} = \frac{v_{o1}^{-}}{v_{in}^{+}} \cdot \frac{v_{o2}^{+}}{v_{o1}^{-}} \cdot \frac{v_{out}^{-}}{v_{o2}^{+}} = -\frac{g_{m1}}{g_{out1}} \cdot \frac{g_{m11}}{g_{out2}} \cdot \frac{g_{m19}}{g_{out3}} \tag{5.31}$$

Note that for better gain/bandwidth performance, the output of each stage is connected to NMOS rather than PMOS devices. NMOS devices have higher mobilities than PMOS devices, resulting in higher g_m for a given area.

The first stage of the amplifier is designed to set the dominant pole. For the initial calculations, the gain and bandwidth of the overall amplifier determine the dominant pole position. The pole of the first stage is

$$\omega_{p1} = \frac{g_{out1}}{C_c} \tag{5.32}$$

Also the gain-bandwidth product or the unity-gain frequency can be determined by

$$\omega_T = \frac{g_{m1}}{C_c} \cdot \frac{g_{m19}}{g_{out3}} \tag{5.33}$$

where C_c is the compensation capacitor which dominates over other parasitic capacitances. From (5.33) the gain bandwidth product of the amplifier is equivalent to the gain bandwidth product of the two-stage amplifier multiplied by the gain of the third

stage. We know that the compensation capacitance is proportional to g_m of the input

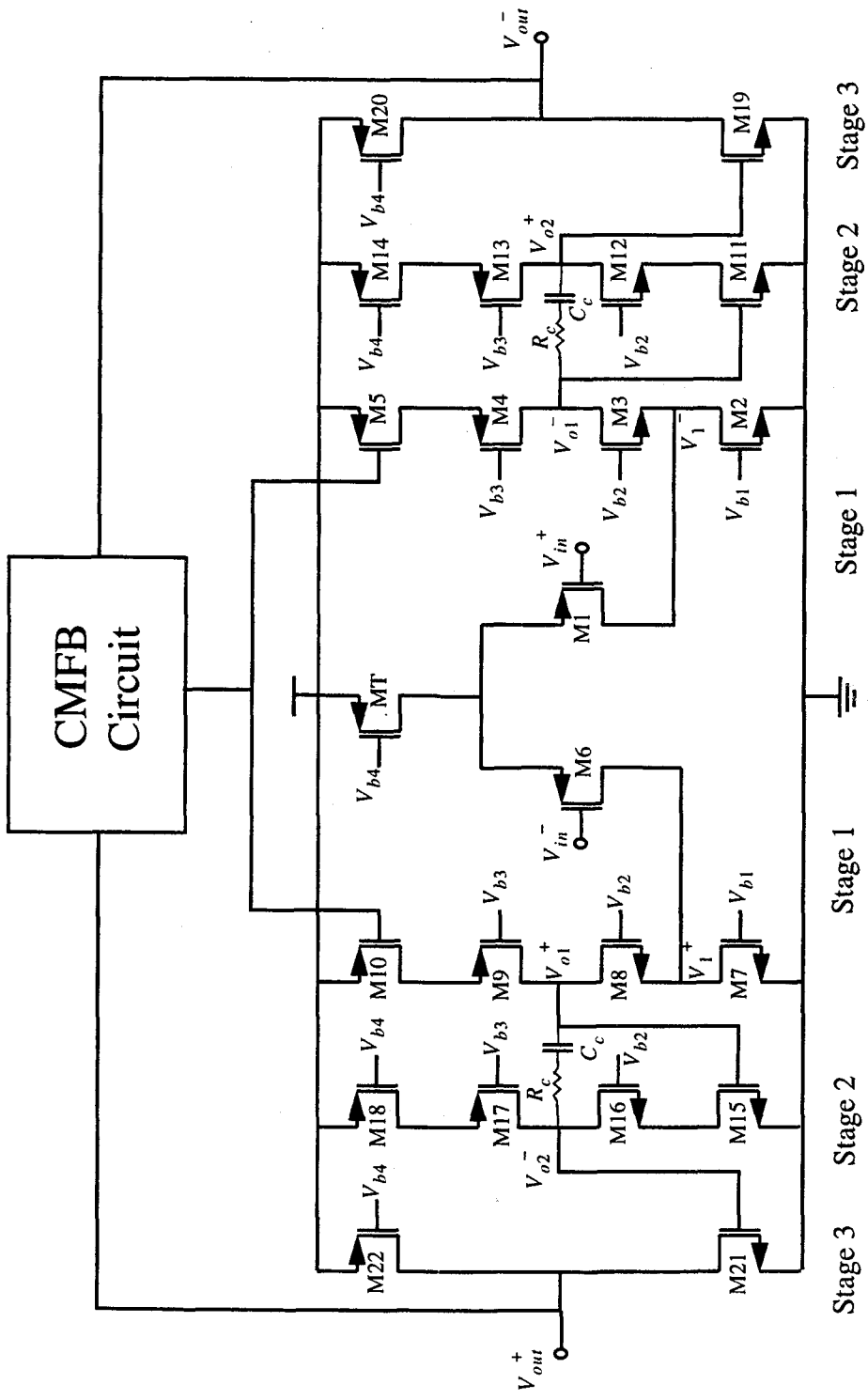

Figure 5.3. Three-stage fully differential amplifier using RC compensation and common-feedback.

stage. To achieve high bandwidth a large g_m is needed which corresponds to a large compensation capacitor.

We mentioned that a three-stage amplifier is a three-pole system with its overall transfer function "referred" to the input stage. The first non-dominant pole associated with the second stage can be cancelled by LHP zero introduced by the compensation resistor. The remaining non-dominant poles are associated with the third-stage and the compensation resistor. Note that these poles may form a complex pair which can be placed beyond the unity-gain frequency. Such caution must be used so that the complex pair lies in the region where acceptable phase and gain margins can be achieved (refer to Chapter 3 for details on the location of the complex pair with respect to the normalized unity-gain frequency). For fast settling time response and high gain and phase margins, there is an optimum placement of complex conjugate pair. If we increase the feedback capacitor, the complex pair eventually becomes real and splits on the real axis. Unfortunately this desirable outcome requires a very large compensation capacitor (50-100 pF) which may not be practical.

We have already studied the second- and third-stages in terms of their transconductance. The sizing of the third stage must meet slew rate requirements. The first and the second stages do not slew due to the small step sizes associated with their output nodes. For example, if the output swing is about 2V and the gain of the second and third stages is about 40 dB and 28 dB, respectively, the second stage output is only about 80 mV. Nevertheless, in order to have a large slew rate at the output, the second stage must be sized appropriately to maintain stability as discussed in Chapter 4. Slew rate is

$$SR = \frac{I_{D3}}{C_{L3}} \tag{5.35}$$

where C_{L3} is the load capacitance of the output stage.

It is usually necessary to add additional circuitry to determine the output common-mode voltage at mid-supply voltages. There are two general approaches to designing common-mode feedback circuits: a continuous-time approach and a switched-capacitor approach [18]. The continuous-time approach often limits the signal swings and if nonlinear, actually introduces differential-mode signals. The switched-capacitor requires multiple clocks and introduces clock-feed through glitches. In this thesis, a continuous-time Common-Mode Feedback circuit is used as shown in Figure 5.4. Note that V_{ref} is set to $V_{DD}/2$. Furthermore, the input signals V_{in}^- and V_{in}^+ are equal in magnitude but opposite in sign and they correspond to the output signals of the third stage. To analyze this circuit, we begin by assuming that the two differential pairs have infinite common-mode rejection which implies that their large-signal output currents depend only on their input differential voltages. Since the two pairs have the same applied differential voltages, the current in M1 will be equal to that, while the current in M3 is equal to that in M2. This result is independent of the nonlinear relationship between the input voltage and large-signal differential drain currents. As long as V_{in}^- is equal to the negative value of V_{in}^+, the current through diode-connected M5 will not change even when large differential voltages are present. Since the voltage across the M5 is used to control output node bias voltages, the bias currents in the output stage will be equal regardless of signal when no common-mode voltages are present. The above discussion is not valid if the output voltage is so large that transistors in the differential pairs turn off.

Next, consider what happens when a common-mode voltage other than $V_{DD}/2$ is present. This positive voltage will cause the currents in both M3 and M4 to increase which, causes the current and voltage in diode-connected M5 to increase. This is the bias voltage for the amplifier. Thus, both current sources will conduct larger currents which will cause the common-mode voltage to decrease, thus bringing the common-mode voltage back to $V_{DD}/2$. Thus, as long as the common-mode loop gain is large enough and the differential signals are not so large as to cause transistors in the differential pairs to turn off, the common-mode output voltage will be kept very close to mid-supply.

Transistors M7 and M8 are used to effectively double the common-mode gain of the circuit with little additional complexity. As reported in [Duque-Carillo, 1992], it has very good linearity (better than 0.01%).

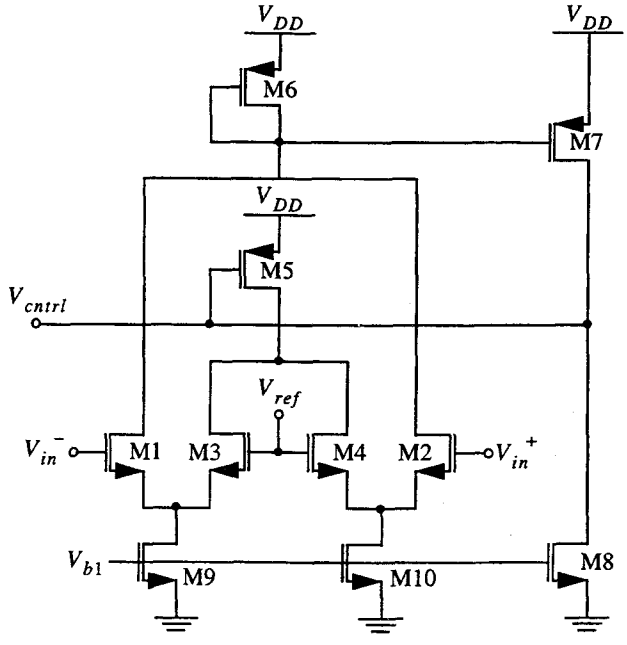

Figure 5.4. Continuous Common-Mode Feedback Circuit.

The bias circuits for the cascode stage NMOS and PMOS devices are shown in Figure 5.5. This topology accommodates low voltage and wide swing. Note that V_{b1} and V_{b4} are set by transistors M3 and M7 at $V_T + V_{DSAT}$ for NMOS and PMOS, respectively. The bias voltages are equivalent to the diode drop across transistors M3 and M7. Transistors M2 and M5 are sized in such a way that voltages V_{b2} and V_{b3} are biased at $V_T + 2V_{DSAT}$. This results in voltages across M3 and M7 equal to V_{DSAT}. Transistor M1 is used to create matching between M2 and M4 in terms of threshold voltages in the presence of body effect. Transistor M1 is in non-saturation due to $V_T + 2V_{DSAT}$ biasing voltage and causes the drain voltage across transistor M1 to be lower. Since there is no swing across M2 and M1, having M2 in non-saturation does not alter V_{b1} and V_{b2}.

5.4 HSPICE Simulation Results

Table 5.2 presents HSPICE simulation results for the three-stage operational of Section 5.4. This operational amplifier achieved high gain, high-speed, and high-slew

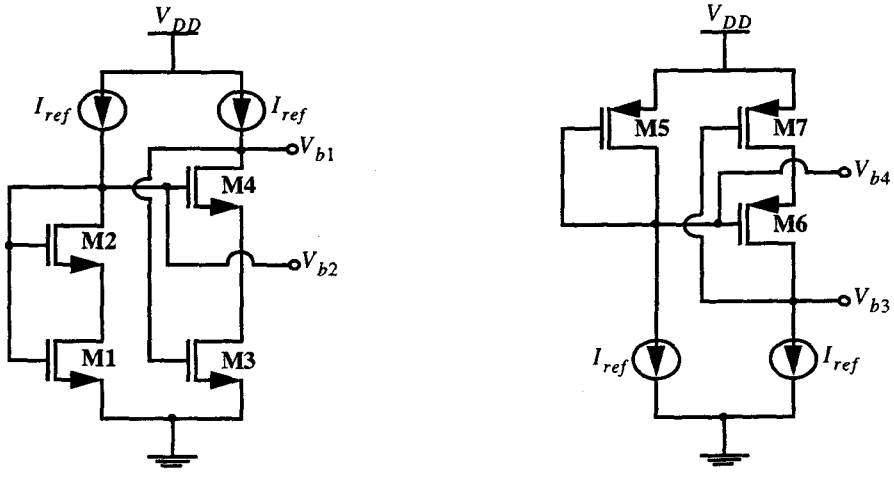

Figure 5.5. Low-voltage bias circuits for (a) NMOS, and (b) PMOS cascode devices.

rate results. Some of the important simulation plots are shown in Figures 5.6-5.10.

Table 5 .2 **Three-Stage Simulation Results**

Specifications	**Simulated Results**
Process	CMOS 0.6μm N-Well
Power Supply	2.5 V
V_{DSAT}	~ 300 mV
Gain	121.46 dB
Gain Bandwidth	137.5 MHz
Slew Rate	360 $V/\mu S$
Phase Margin	70.6°
Gain Margin	7.9 dB
Settling Time (0.1%)	15 ns
Settling Time (0.01%)	18 ns
Settling Time (0.001%)	56 ns
Settling Time (0.0001%)	78 ns
Input CMR	0.0-0.9 V
CMRR @ DC	145.4 dB
PSRR @ DC	137.5 dB
Input Noise @ 137.5 MHz	15.98 $nV/\sqrt{Hz}$
Input Noise @ 1KHz	6.2108 $nV/\sqrt{Hz}$
Input Noise Unity-Gain @ 137.5 MHz	30.04$nV/\sqrt{Hz}$
Input Noise Unity-Gain @ 1 KHz	18.32$nV/\sqrt{Hz}$
Power Consumption	11 mW
Power/Bandwidth	80 $\mu W/MHz$
Output Load (at each output)	5.0 pF
Compensation Capacitance	9.0 pF
Compensation Resistor	3.0 K-ohms
Power/(Bandwidth. Load Capacitance)	16$\mu W/(MHz \cdot pF)$

Table 5 .2 **Three-Stage Simulation Results**

Output Swing	1.9 V

Figure 5.6 presents the open-loop gain and phase frequency responses. Note that the gain exhibits a one-pole response above the unity-gain frequency. Figure 5.7 shows the step response for a 1 volt step applied differentially (0 V-0.5 V single-ended). Figure 5.8 is a plot of the equivalent input noise. Note that at high frequencies the input noise increases. The noise is constant over frequency range from 0 to approximately 57 KHz and increases at higher frequencies. Figure 5.8 shows the common-mode and differential gain frequency responses. From this plot, Common-Mode Rejection Ratio (CMRR) of the amplifier is obtained as

$$CMRR = 20\log\left(\frac{A_{diff}}{A_{cm}}\right) \tag{5.36}$$

where A_{diff} and A_{cm} represent the differential-mode and common-mode gains. Ideally, for a fully differential topology, infinite CMRR is obtained, but in a real circuit it is finite due to device mismatches. Finally, Figure 5.10 presents the differential and power supply frequency responses. The power supply gain is obtained by applying a small-signal input to the power supply of the amplifier. Power Supply Rejection Ratio (PSRR) [13] can be written as

$$PSRR = 20\log\left(\frac{A_{diff}}{A_{PS}}\right) \tag{5.38}$$

Figure 5.11 presents the unity-gain frequency response of the amplifier. Note that at the unity-frequency, the corresponding gain has approximately -5.35 dB attenuation. Finally, Figure 5.12 presents transient response of the amplifier with a sinusoidal input. Note that the output waveforms at unity gain, is about 5.35 dB attenuated from the unity-gain.

The output signal can follow the input signal at unity gain frequency given by the power-bandwidth product given by

$$SR = v_p \omega_u \tag{5.39}$$

where, v_p is the peak value of the input signal. Note from Table 5.2, the slew rate corresponds to $360V/\mu S$ with a unity-gain frequency of 137.5 MHz; this corresponds to an equivalent peak input signal of 0.41V. An input peak signal of 0.5 V was applied differentially shown in Figure 5.12

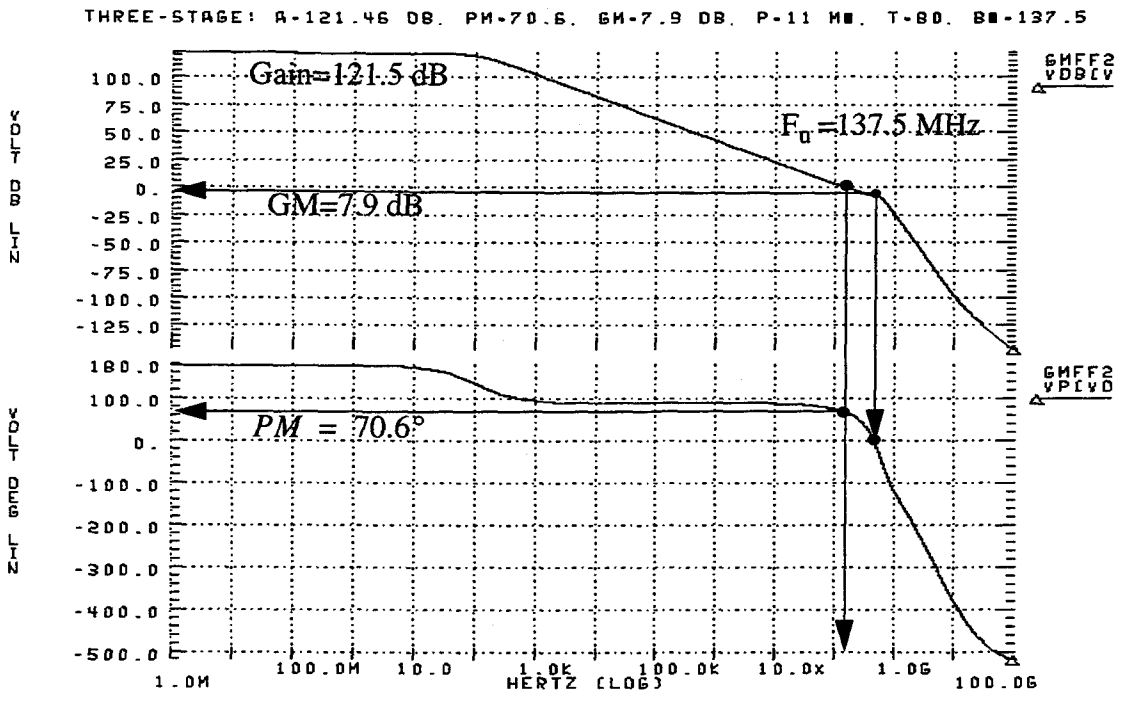

Figure 5.6. Three-stage open-loop differential gain and phase responses.

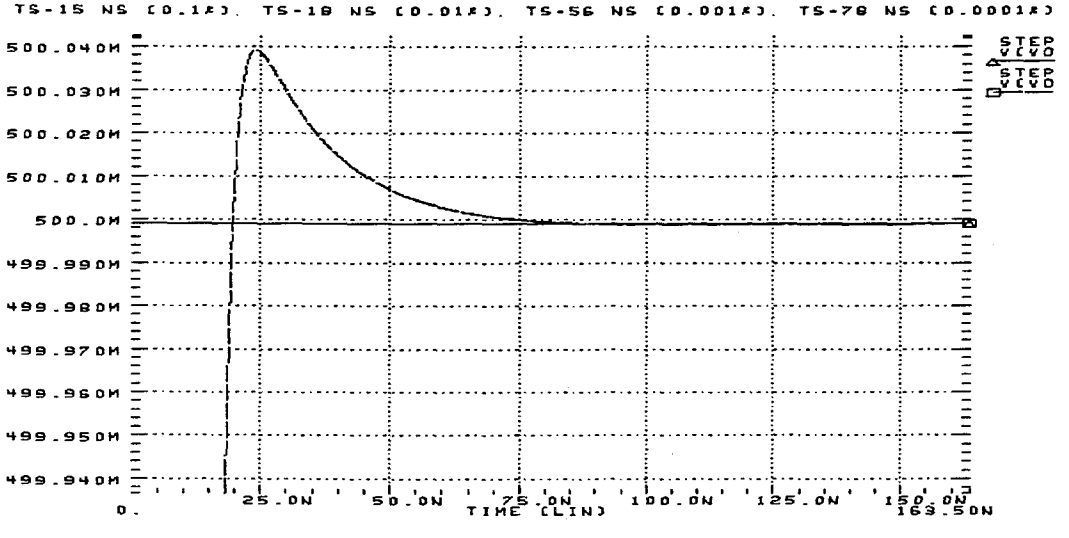

Figure 5.7. Three-stage differential step response for 1 Vp-p (-0.5 V to 0.5V).

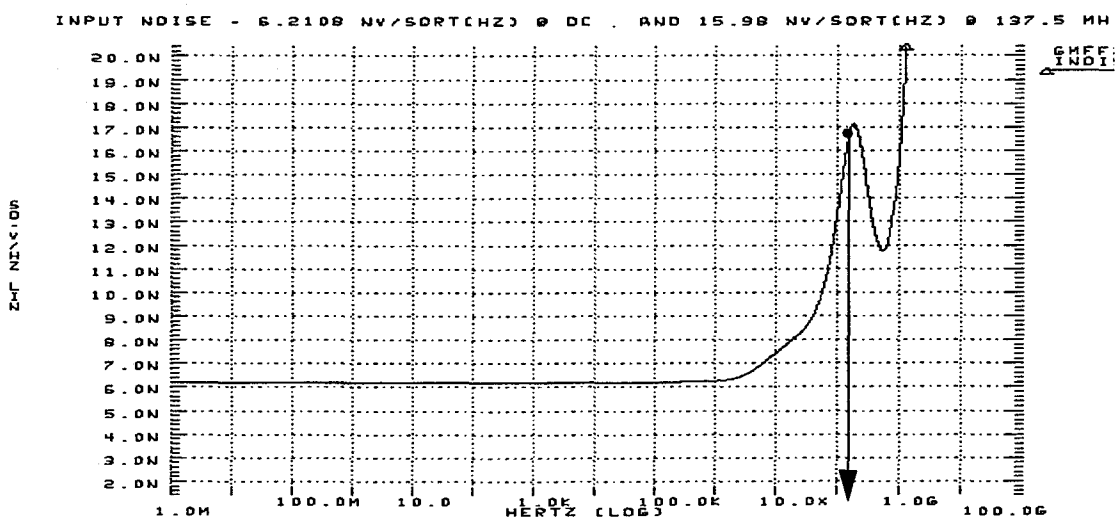

Figure 5.8. Three-stage differential input-referred noise power spectral density.

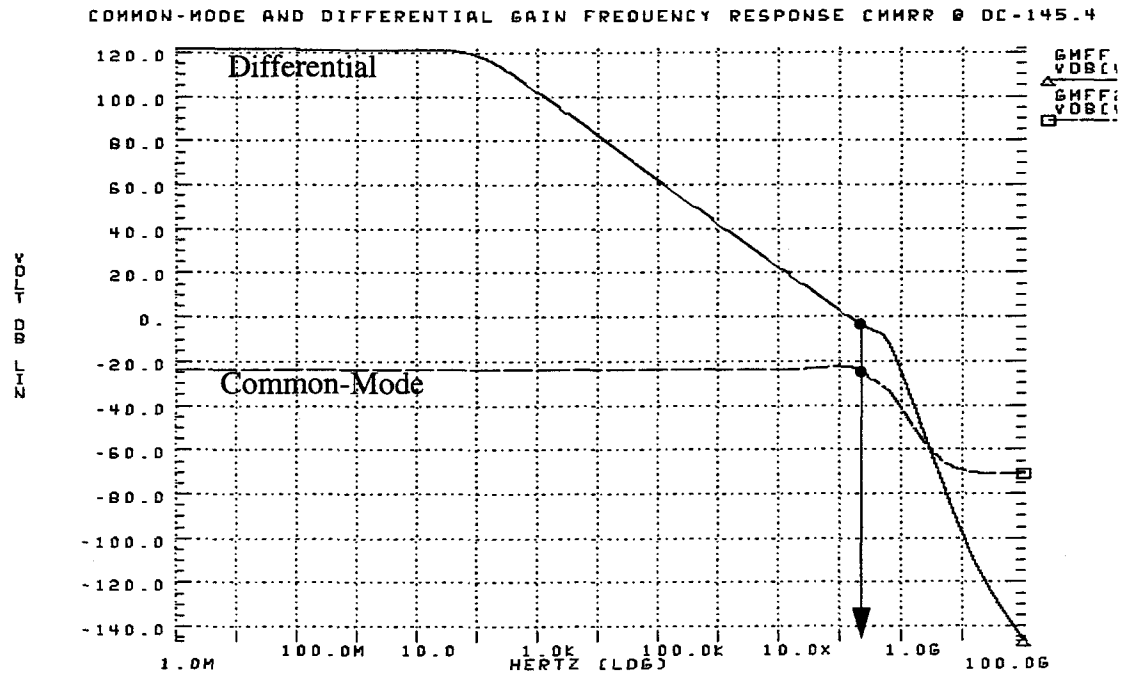

Figure 5.9. Three-stage common-mode and differential-mode gain frequency responses.

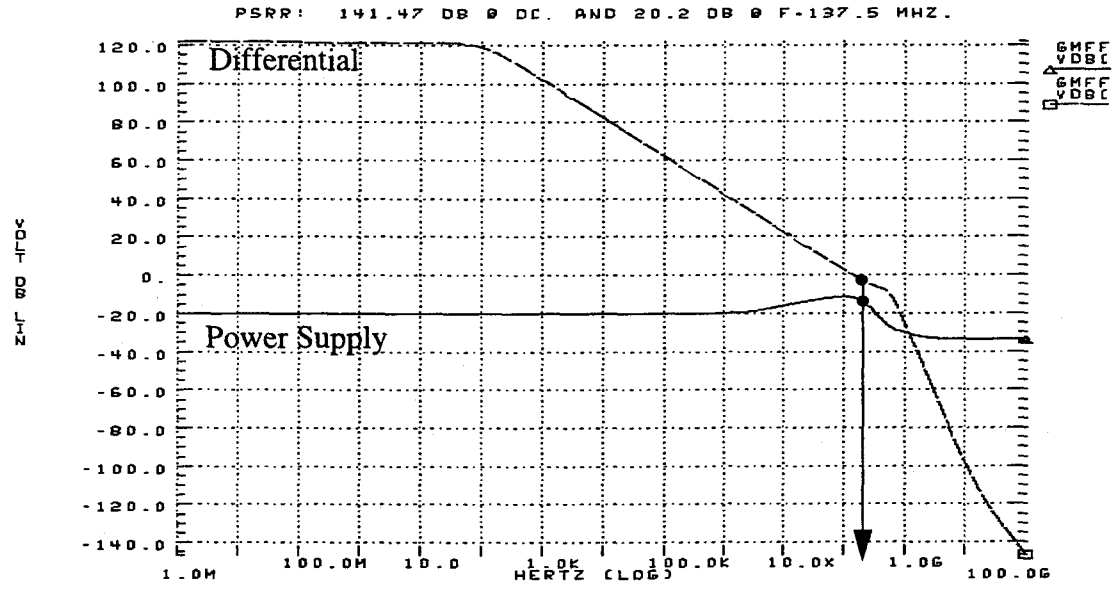

Figure 5.10. Three-stage power supply and differential-mode frequency responses.

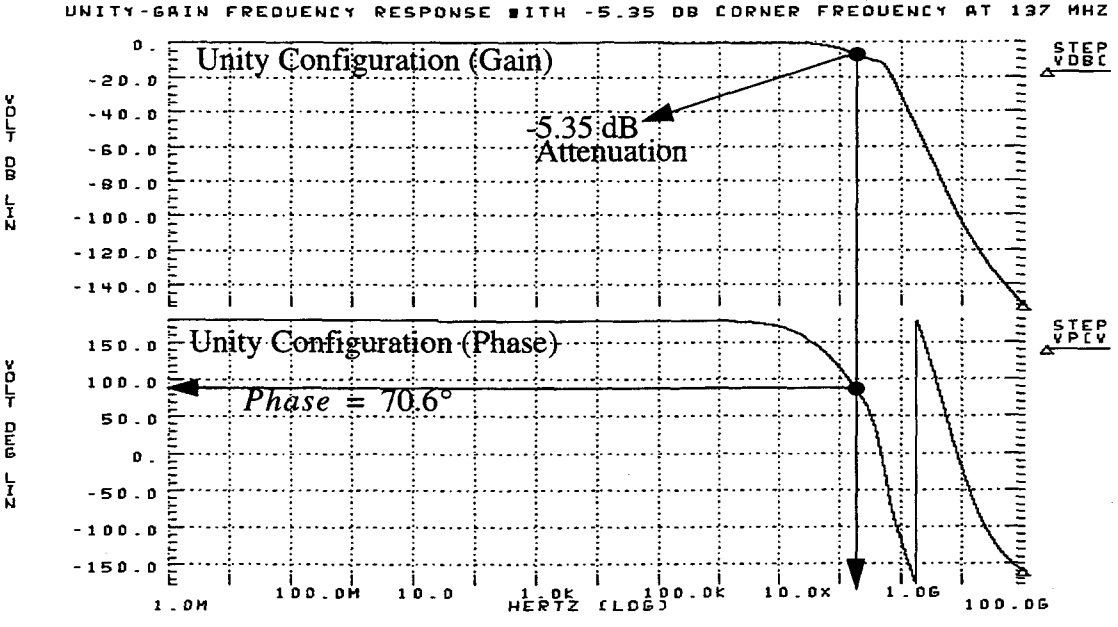

Figure 5.11. Three-stage unity-gain and phase responses.

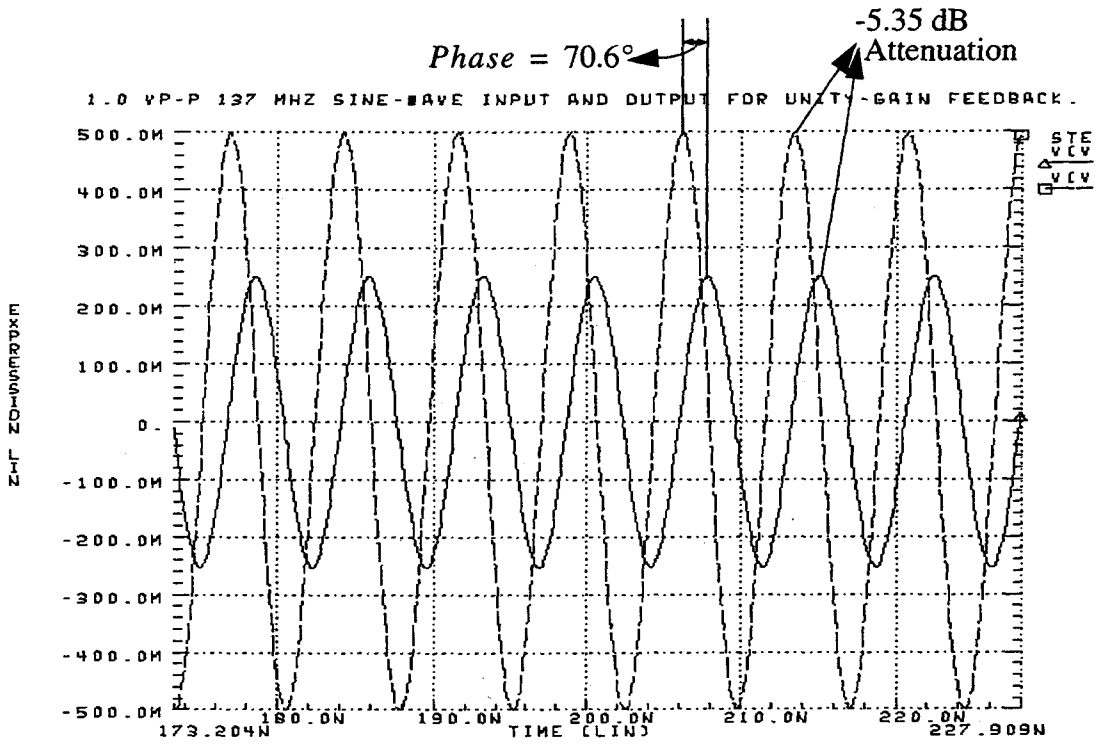

Figure 5.12. Three-stage unity-gain differential sinusoidal transient response.

Chapter 6. Higher Order Topologies for Multi-Stage Operational Amplifiers

In this chapter, an enhancement is presented for the three-stage operational amplifier topology. The motivations improve stability, increase the noise, slew rate, and bandwidth parameters, and most importantly to reduce the size of the compensation capacitor [19]. A four-stage amplifier design employing the improved technique will be discussed. Some of the issues determining the optimum number of gain stages for a given minimum feature size will also be presented.

6.1 A Three-Stage Operational Amplifier with Global G_m Feed-forward

In this section, the use of global G_m feed-forward in the new multi-stage operational amplifier topology is explored. G_m feed-forward in operational amplifiers has been developed previously [4]. Figure 6.1 shows a block diagram of a modified three-stage amplifier in which the signal is fed-forward from input to the output by the

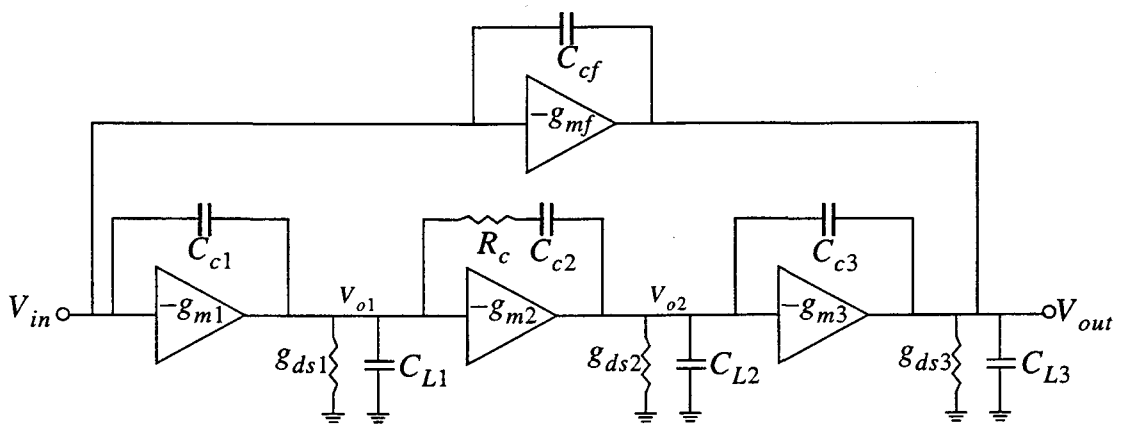

Figure 6.1. Three-stage operational amplifier using global G_m feed-forward block.

g_{mf} stage. The G_m feed-forward stage also includes the parasitic coupling capacitor C_{cf} connected from output to input. The g_{mf} also is used increase bandwidth, slew rate, and decrease the compensation capacitor C_{c2} size and its required die area. By using the G_m feed-forward stage, we are able to move the RHP zeros associated with the third and second stages to form a LHP complex conjugate pair. By increasing g_{mf} the complex conjugate zeros migrate toward lower frequencies as shown. Another important observation is that the zero associated with the compensation resistor R_c moves to lower frequencies possibly, passing the non-dominant pole P_{n1}. To achieve stability, either the resistor or compensation capacitor value must be decreased. Hence, the compensation capacitance can be reduced and still provide the stability margin required. Now, as the value of the resistor or capacitor is reduced, the non-dominant complex conjugate poles move toward higher frequencies on the real axis and lower frequencies on the imaginary axis. If this process continues, the poles of the complex conjugate pair eventually become real along with the zeros of the complex conjugate pair. If designed carefully, it is possible to cancel the poles of the complex conjugate pair with the zeros to provide

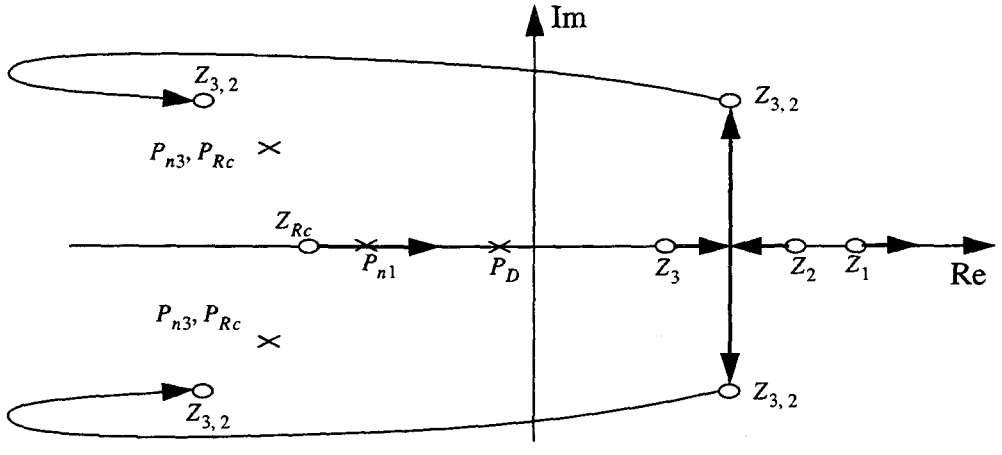

Figure 6.2. Pole-zero plot of a three-stage amplifier with G_m feed-forward.

a true one-pole response with a phase margin close to 90° or to make both pairs real, but it would be over designed for practical component constraints. Also, perfect pole-zero cancellation means the overall amplifier is dominated by the G_m block which corresponds to a one-pole response. Caution must be used in sizing the G_m block. If it gets too large, it will reduce the DC gain of the amplifier to the gain of the G_m block. The pole-zero migration due to G_m feed-forward is shown in Figure 6.2.

Other Performance Benefits

In regards to noise performance, according to Figure 6.1, if we assume that the g_m of the input-stage is kept constant, increasing g_{mf}, will cause overall input referred noise reduction if we assume the bandwidth is kept constant. The input referred noise voltage of the amplifier prior to G_m block is

$$Noise = \frac{8kT}{3g_{m1}}\Delta f \Rightarrow \left(\frac{8kT}{3g_{m1}}\right)\left(\frac{g_{m3}}{g_{ds3}}\cdot\frac{g_{m1}}{C_{c2}}\right) = \left(\frac{8kT}{3C_{c2}}\right)\left(\frac{g_{m3}}{g_{ds3}}\right) \quad (6.1)$$

and the input referred noise voltage with G_m block can be written as

$$Noise = \frac{8kT}{3(g_{m1}+g_{mf})}\Delta f \Rightarrow \left(\frac{8kT}{3(g_{m1}+g_{mf})}\right)\left(\frac{g_{m3}}{g_{ds3}}\cdot\frac{g_{m1}}{C_{c2}}\right) = \frac{8kTg_{m1}}{3(g_{m1}+g_{mf})C_{c2}}\cdot\frac{g_{m3}}{g_{ds3}} = \frac{1}{2}\left(\frac{8kT}{3C_{c2}}\cdot\frac{g_{m3}}{g_{ds3}}\right) \quad (6.2)$$

Note that by increasing g_{mf} we can independently reduce the input referred noise of the operational amplifier.

In regards to slew rate, since the G_m block is connected to the output node, more current is generated and injected into the output load capacitance thus, increasing the slew rate. However, the gain of the third stage is reduced due to the equivalent output impedance seen by the third-stage and the G_m block.

Circuit Design

The G_m feed-forward block comprises two possible configurations. In one, the driver devices driver share the tail current with the input stage and its load devices are independent of the input stage. In the other a single common-source amplifier does not share the tail current of the input stage. Both techniques offer advantages. For the first type, according to (6.1) and (6.2), the equivalent input referred noise voltage is reduced since the effective g_m of the input stage increases as discussed earlier. It also in increases the slew rate of the amplifier providing parallel path to the output. This technique does not facilitate the desired pole-zero placements. The second method is more effective in reducing the area of the compensation capacitor and the equivalent input and output noise voltages. If these techniques are used in combination, the performance of the amplifier can be improved significantly.

The complete circuit is shown in Figure 6.3. Transistors MF1-MF4 represent the G_m feed-forward stages. Note that the second type mentioned above has not been implemented here.

HSPICE Simulation Results

For comparisons, a simple three-stage amplifier without G_m feed-forward was re-designed for a 20 pF load capacitor; the results are shown in Table 6.1. Simulation

Table 6 .1 Three-Stage Simulation Results.

Specifications	Simulated Results
Process	CMOS 0.6μm N-Well MOSIS
Power Supply	3.0 V
V_{DSAT}	~ 300 mV
Gain	133.7 dB
Gain Bandwidth	105.0 MHz

Table 6 .1 (Continued)

Slew Rate	200 $V/\mu S$
Phase Margin	63.6°
Gain Margin	7.7 dB
Settling Time (0.1%)	12.0 ns
Settling Time (0.01%)	14.8 ns
Settling Time (0.001%)	62.0 ns
Settling Time (0.0001%)	96.0 ns
Input CMR	0.0-1.5 V
CMRR @ DC	155.69 dB
PSRR @ DC	148.77 dB
Input Noise @ 105.0 MHz, Single-Ended	9.11 $nV/\sqrt{Hz}$
Input Noise @ DC, Single-Ended	3.96 $nV/\sqrt{Hz}$
Output Noise @ 105.0 MHz, Single-Ended	9.31 $nV/\sqrt{Hz}$
Output Noise @ DC, Single -Ended	19.27 $mV/\sqrt{Hz}$
Power Consumption	20.8 mW
Power/Bandwidth	198.4 $\mu W/MHz$
Power/(Bandwidth . pF)	9.92 $\mu(W/(MHz \cdot pF))$
Output Load (at each output)	20 pF
Compensation Capacitance	84 pF
Output Swing	2.4 V
Temperature of operation	25.0°C

results G_m feed-forward as in Figure 6.3 are shown in Table 6.2. Note that the DC gain of the amplifier with G_m block is reduced due to the parallel connection at the output node and the power consumption is increased. However, the main advantage of the enhanced amplifier is the reduction in compensation capacitor equal to the load capacitance as compared to 4 times greater for the previous design. Also note that the slew rate has been increased, and the input and output noise voltages have been reduced.

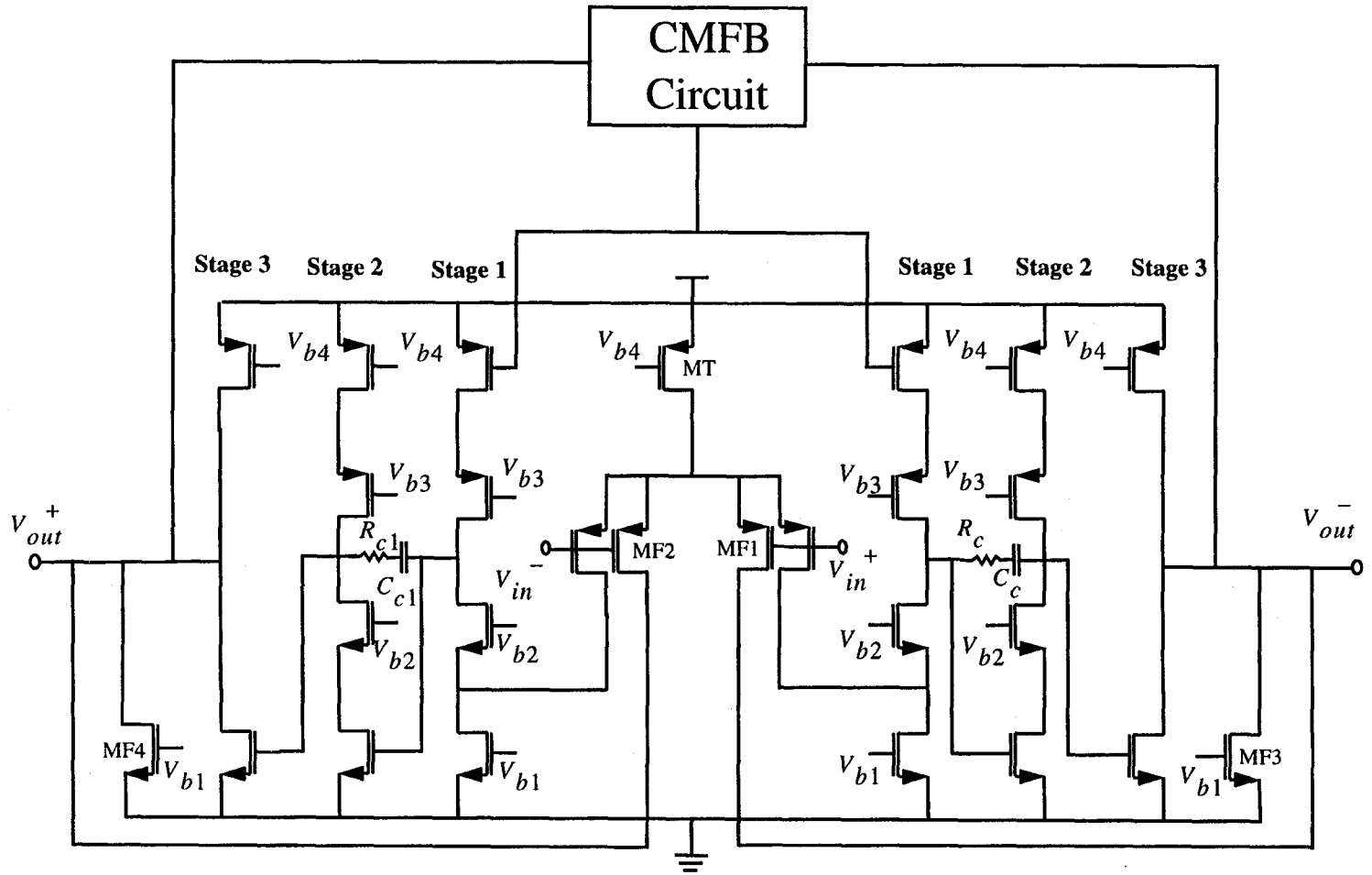

Figure 6.3. Three-stage fully differential amplifier with G_m feed-forward stage.

Table 6 .2 Enhanced Three-Stage Simulation Results.

Specifications	Simulated Results
Process	CMOS 0.6μm N-Well MOSIS
Power Supply	3.0 V
V_{DSAT}	~ 300 mV
Gain	127.1 dB
Gain Bandwidth	115.0 MHz
Slew Rate	300 $V/\mu S$
Phase Margin	69.7°
Gain Margin	13.42 dB
Settling Time (0.1%)	9.8 ns
Settling Time (0.01%)	37 ns
Settling Time (0.001%)	72.5 ns
Settling Time (0.0001%)	94.4 ns
Input CMR	0.0-1.5 V
CMRR @ DC	150.8 dB
PSRR @ DC	145.7 dB
Input Noise @ 210.0 MHz, Single-Ended	6.64 $nV/\sqrt{Hz}$
Input Noise @ DC, Single-Ended	3.89 $nV/\sqrt{Hz}$
Output Noise @ 210.0MHz, Single-Ended	6.8 $nV/\sqrt{Hz}$
Output Noise @ DC, Single-Ended	8.9 $mV/\sqrt{Hz}$
Power Consumption	35.2 mW
Power/Bandwidth	321.0 $\mu W/MHz$
Power/(Bandwidth . pF)	16.0$\mu(W/(MHz \cdot pF))$
Output Load (at each output)	20 pF
Compensation Capacitance	20 pF
Output Swing	2.4 V

6.2 Four-Stage Operational Amplifier

Extending out compensation topology, we now consider the design of a four-stage operational amplifier. The g_m block diagram of a compensated four-stage amplifier is shown in Figure 6.4. As before there is no compensation network connected at the output node loading the amplifier. This type of compensation ensures high-slew rate, high-speed, and low-power operation. In Figure 6.4, C_{p1} and C_{p4} are parasitic capacitances associated with the first and fourth stages, respectively while R_{c2}, C_{c2}, R_{c3}, and C_{c3} are the RC compensation elements for second and third stages, respectively. This scheme follows the technique used for three-stage amplifiers; i.e., an n-stage operational amplifier requires only n-2 RC frequency compensation networks.

The pole-zero representation of an uncompensated four-stage operational amplifier is shown in Figure 6.5. As described in Chapter 4, the pole of the fourth stage is cancelled by the zero of the third stage, and the second-order poles of the third-stage are cancelled by the second-order zeros of the second-stage, and the third-order poles of the second-stage are cancelled with the third-order zeros of the first-stage. Thus, the

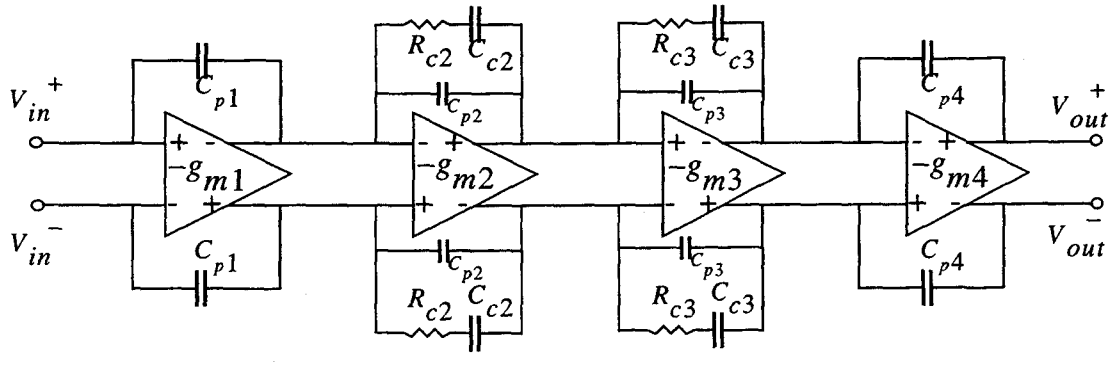

Figure 6.4. Small-signal representation of a four-stage amplifier with two RC compensation networks.

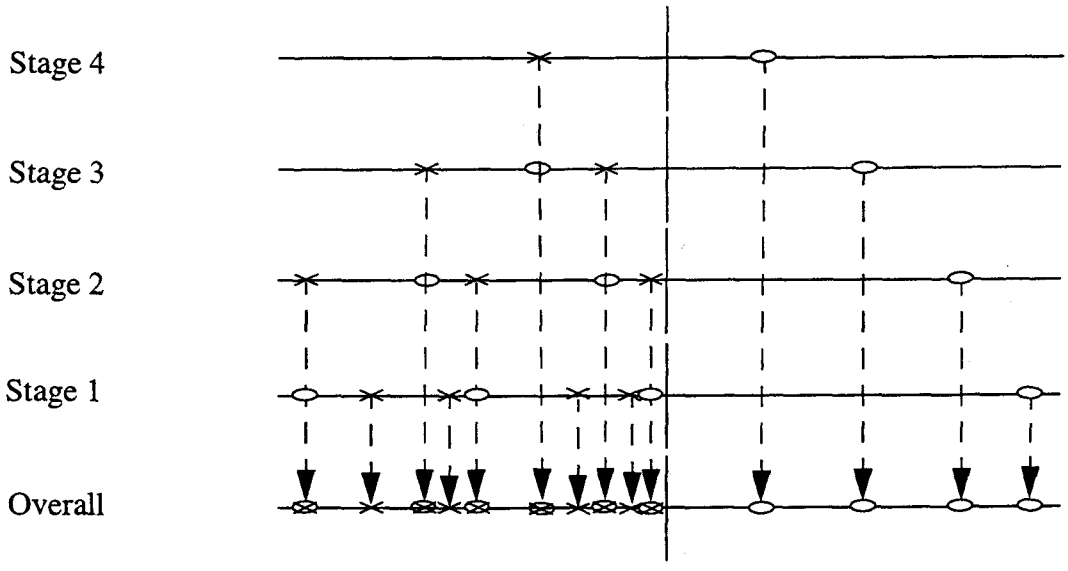

Figure 6.5. Individual gain stage pole-zero plots for a four-stage operational amplifier.

overall fourth-order transfer function is "referred" to the input stage only as described earlier.

A four-stage operational amplifier can be motivated by looking at Figure 6.6 where it is broken down into three cascaded components; namely, a two-stage amplifier followed by two single-stage amplifiers. We assume that the two-stage operational amplifier has a one pole response (second pole cancelled with a zero) with a pole at ω_{p1} and the third and fourth stages have poles at ω_{p3} and ω_{p4}. A four-stage operational amplifier has much higher gain-bandwidth product than a three-stage amplifier. By design, the pole ω_{p3} associated with the third stage ω_{p3} is cancelled with a zero from with the second RC compensation network. The fourth stage pole ω_{p4} needs to be placed well above unity-gain frequency to achieve sufficient stability. This can be illustrated using a two-stage amplifier with a gain-bandwidth product of 10 MHz. For

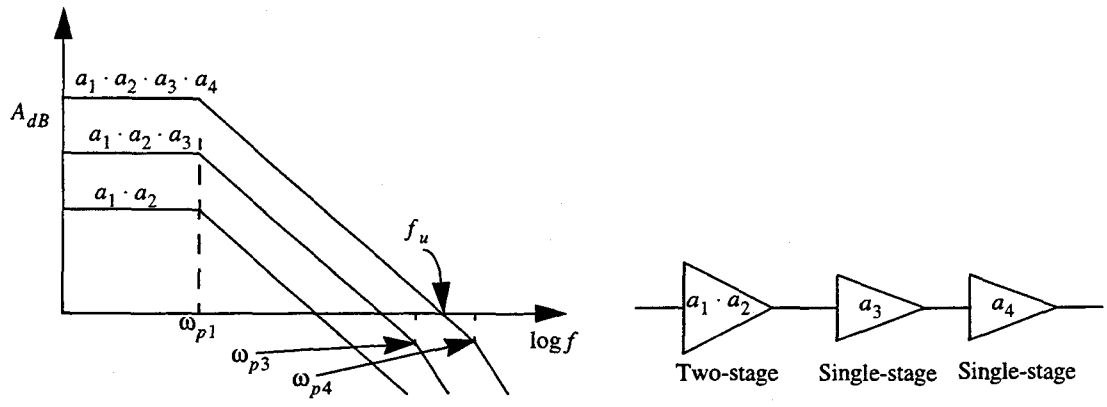

Figure 6.6. Two-stage followed with two single-stage amplifiers.

20 dB gain in the third stage, the effective gain-bandwidth product becomes about 100 MHz, and for another 20 dB gain in the fourth stage, the overall gain-bandwidth product becomes approximately 1 GHz. The problem with this design approach is that it may not be possible for a given technology to position the fourth pole well above the unity-gain frequency (2-4 GHz). A simple solution would be to start from the output stage and consider a gain-bandwidth product that is reasonable. We can determine the gain-bandwidth product of the two-stage amplifier by dividing it by the fourth- and third-stage gains. This results in reduction of the input-stage g_m which degrades the dynamic range performance such as the input referred noise voltage.

We see that the optimum number of stages used in operational amplifiers is technology dependent. For the technology used in this thesis (CMOS 0.6μm N-Well process), three is the optimum number of stages for good noise and stability performance. However, as the technology feature sizes decrease, four-stage operational amplifiers become optimal.

As usual, the design of a four-stage operational amplifier requires a one-pole response beyond the unity-gain bandwidth. To achieve this, two RC compensation networks are used to split the two non-dominant poles from the dominant pole and to cancel them with zeros. Introducing C_{c2} splits the dominant pole from the remaining poles as shown in Figure 6.7(a). The zero associated with the compensation resistor R_{c2} is used to cancel the first non-dominant pole. Note that the fourth pole system moves to higher frequencies and forms a complex conjugate pair with the pole associated with R_{c2}. To cancel the second non-dominant pole, a second RC compensation network is needed. Unfortunately, C_{c2} is the only compensation capacitor that provides true pole splitting behavior. However, a small value of C_{c3} compared to C_{c2} can be used with resistor R_{c3}

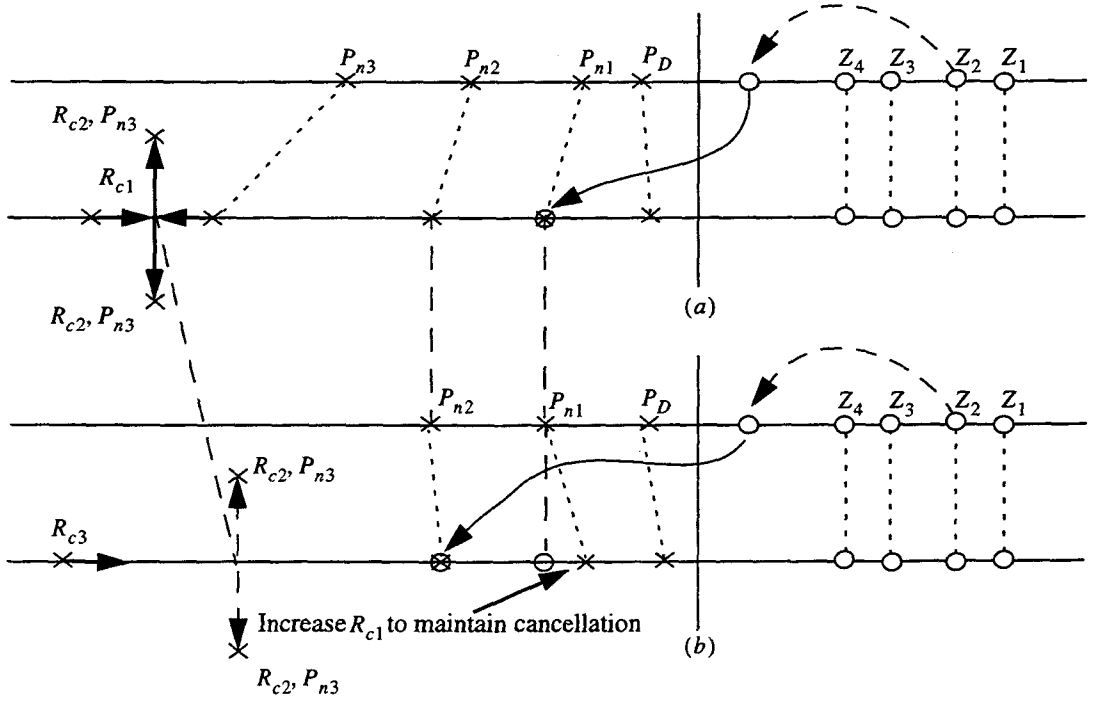

Figure 6.7. Pole-zero plots of the compensation process for a four-stage operational amplifier. (a) R_{c2} and C_{c2} being increased. (b) R_{c3} and C_{c3} being increased.

to be employed for cancellation of the second non-dominant pole. According to the bottom plots of Figure 6.7(b), as C_{c3} is introduced, the pole-zero cancellation due to the first RC compensation network is altered. Since C_{c3} causes all of the poles to move to lower frequencies as shown, small values of C_{c3} are desirable whereas large values of C_{c2} ensures proper pole-splitting. However, if a very small value of C_{c3} is used, the R_{c3} value will become large and cause the most non-dominant pole P_{n3} to move to lower frequencies. Reasonable trade-off can be employed in determining the capacitor and resistor values. Once the two non-dominant poles are cancelled, the remaining poles are due to the fourth stage, R_{c1}, and R_{c2}. Note that the pole associated with R_{c2} is on the real axis.

Simulation Results

The schematic of the complete amplifier is shown in Figure 6.9. Due to the high-gain achievable using this topology, large V_{DSAT} values of about 0.35V were used to reduce transistor sizes. The simulation results are listed in Table 6.2.

Table 6 .3 Four-Stage Simulation Results.

Specifications	Simulated Results
Process	CMOS 0.6μm N-Well MOSIS
Power Supply	3.0 V
V_{DSAT}	~ 350 mV
Gain	134.4 dB
Gain Bandwidth	169.82 MHz
Slew Rate	117.9 $V/\mu S$
Phase Margin	58.5°
Gain Margin	12.9 dB

Table 6 .3 Four-Stage Simulation Results.

Settling Time (0.1%)	49.2 ns
Settling Time (0.01%)	60.5 ns
Settling Time (0.001%)	78.9 ns
Settling Time (0.0001%)	140.6 ns
Input CMR	0.0-1.5 V
CMRR @ DC	155.4 dB
PSRR @ DC	149.7 dB
Input Noise @ 210.0 MHz, Single-Ended	3.20 $\mu V/\sqrt{Hz}$
Input Noise @ DC, Single-Ended	1.08 $\mu V/\sqrt{Hz}$
Output Noise @ 210.0MHz, Single-Ended	17.9 $nV/\sqrt{Hz}$
Output Noise @ DC, Single-Ended	31.6 $mV/\sqrt{Hz}$
Power Consumption	55.40 mW
Power/Bandwidth	326.1 $\mu W/MHz$
Power/(Bandwidth . pF)	16.3 $\mu(W/(MHz \cdot pF))$
Output Load (at each output)	20 pF
Compensation Capacitance (1st and 2nd)	100 pF, 20 pF
Output Swing	1.9 V
Temperature of operation	25.0°C

From results of Table 6.2, the four-stage operational amplifier is stable and has acceptable performance characteristics. However, this amplifier has unacceptable noise and slow settling time performance as compared to the three-stage operational amplifier discussed earlier.

Since the operational amplifier is driving a large 20 pF load, a large compensation capacitance of about 100 pF is required. From the previous results, we can generalize that the value of the compensation capacitor used for splitting the poles around second-stage for an n-stage operational amplifier is roughly

$$C_{c1} \approx (4 \rightarrow 5) \times C_L \qquad (6.1)$$

This relationship along with other guidelines that we have developed in this thesis set a good starting point for multi-stage operational amplifier design. However, further improvements are highly desirable, especially reducing the compensation capacitor to roughly equal to the load capacitance.

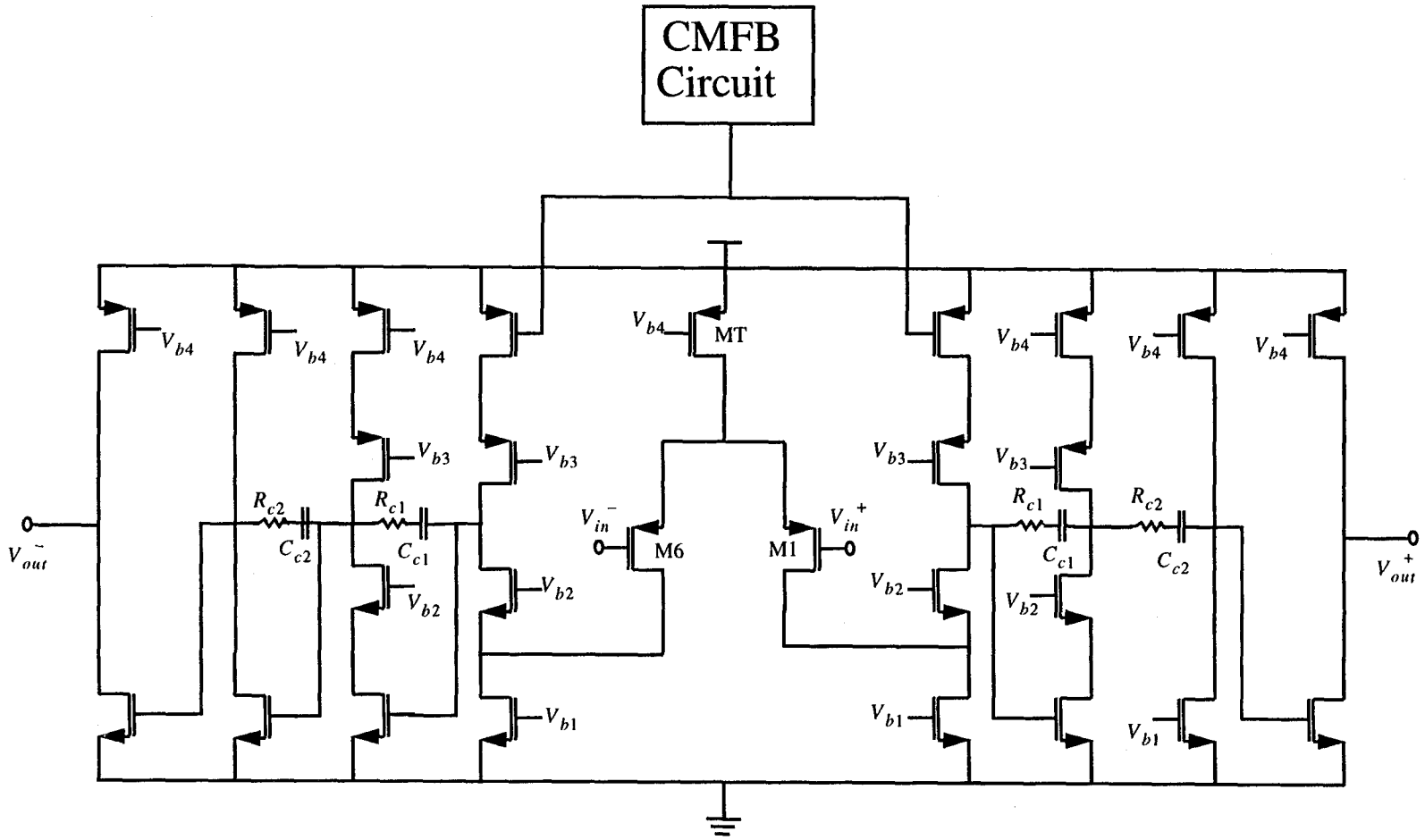

Figure 6.8. Complete four-stage fully-differential operational amplifier.

6.3 Enhanced Four-Stage Operational Amplifier

Once again to enhance the four-stage operational amplifier performance, we will employ G_m feed-forward block connected in parallel with the basic amplifier. The block diagram of a fully-differential four-stage operational amplifier is shown in Figure 6.9. The main difference versus the three-stage, is that the G_m feed-forward blocks must be cross-coupled to provide negative feed-forward effect to match the phase of the four gain stages.

Once again we take advantage of the RHP zeros. By applying the G_m feed-forward, all four RHP zeros form complex conjugate pairs: the first stage with the second stage and the third stage with the fourth stage, respectively. However, the complex conjugate pairs associated with the first and second stages appear in the left half plane and become real: one of the zeros moves towards the pole associated with the

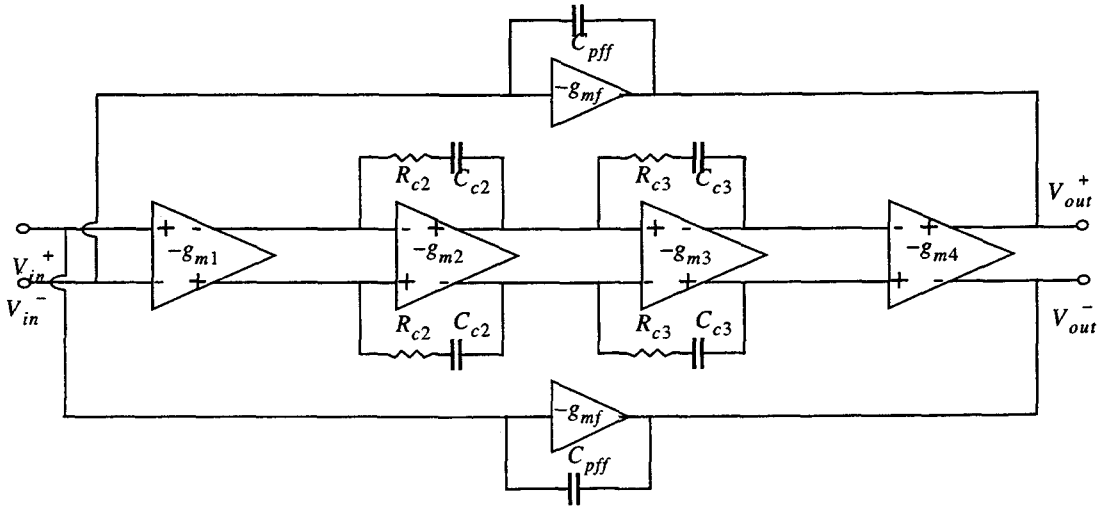

Figure 6.9. Four-stage amplifier with the feed-forward block (parasitic coupling not shown for the four-stage amplifier).

second compensation resistor R_{c3} and the other moves to higher frequencies. On the other hand, the complex conjugate zero pair associated with the third and fourth stages move toward the left-half plane as g_{mf} is increased. At the same time, the LHP zeros associated with the compensation resistor networks move to lower frequencies allowing us to reduce the feedback capacitors. The pole-zero movements are summarized in Figure 6.10.

HSPICE Simulation Results

The enhanced four-stage operational amplifier in Figure 6.11 was simulated using HSPICE LEVEL 39 device models. This circuit is very similar to the three-stage amplifier in terms designing the G_m block. The simulation results are listed in Table 6.4. Note the improvement of bandwidth, slew rate, compensation capacitances, and most importantly, the noise performance. We saw earlier that the noise of the four-stage amplifier is high. However with this technique, we are able to independently reduce the

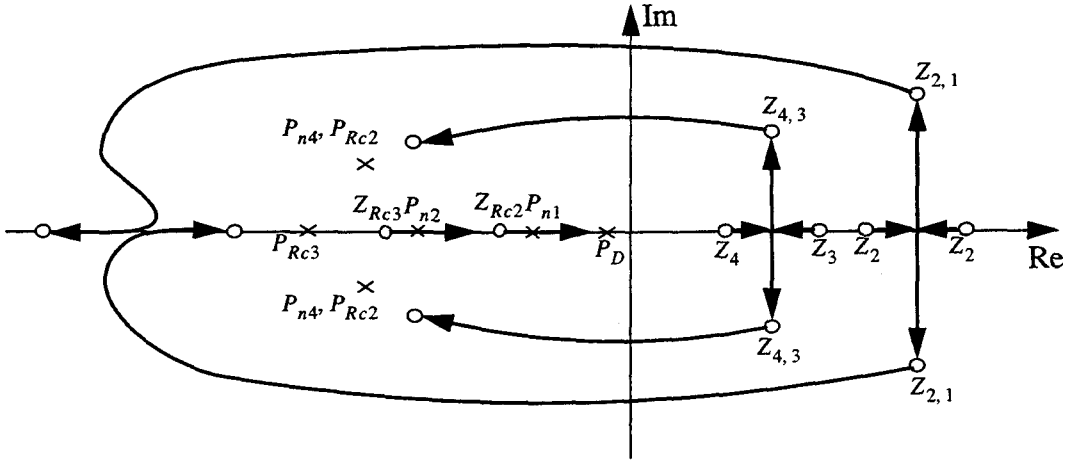

Figure 6.10. Pole-zero plots for a four-stage amplifier with G_m feed-forward stage.

noise by increasing g_{mf}. The associated trade-off is in reduced stability. Due to the excess bandwidth capability of a four-stage amplifier in $0.6\mu m$ CMOS, we were not able to achieve optimum performance but, as technology feature sizes decrease, optimal four-stage, and five-stage operational amplifiers will become feasible.

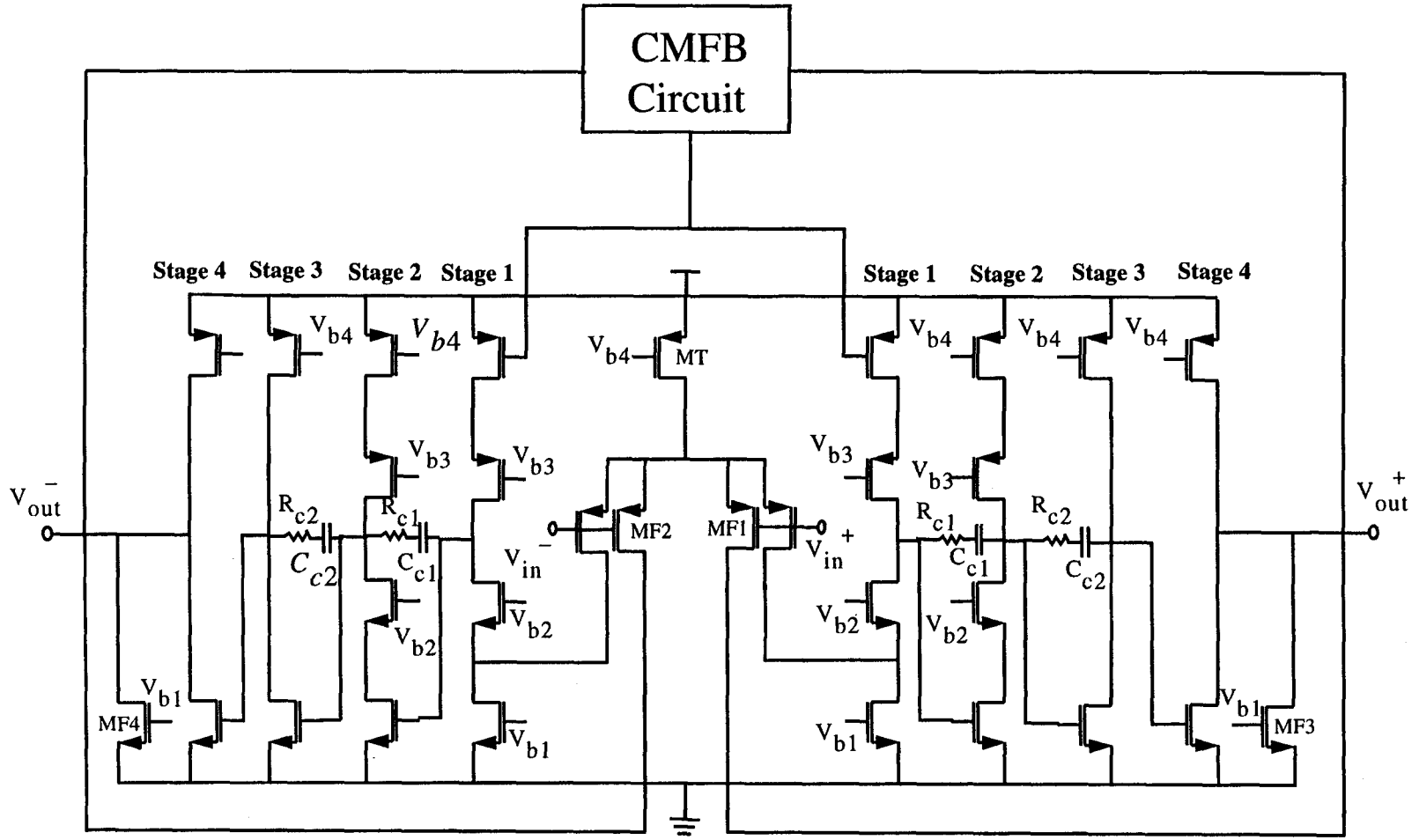

Figure 6.11. Complete enhanced four-stage fully-differential operational amplifier.

Table 6 .4 Enhanced Four-Stage Simulation Results.

Specifications	Simulated Results
Process	CMOS 0.6μm N-Well MOSIS
Power Supply	3.0 V
V_{DSAT}	~ 350 mV
Gain	126.5 dB
Gain Bandwidth	380.2 MHz
Slew Rate	425.5 $V/\mu S$
Phase Margin	40.0°
Gain Margin	7.50 dB
Settling Time (0.1%)	49.2 ns
Settling Time (0.01%)	68.1 ns
Settling Time (0.001%)	82.1 ns
Settling Time (0.0001%)	110.3 ns
Input CMR	0.0-1.5 V
CMRR @ DC	150.4 dB
PSRR @ DC	145.7 dB
Input Noise @ 210.0 MHz, Single-Ended	0.72 $\mu V/\sqrt{Hz}$
Input Noise @ DC, Single-Ended	0.68 $nV/\sqrt{Hz}$
Output Noise @ 210.0MHz, Single-Ended	4.0 $nV/\sqrt{Hz}$
Output Noise @ DC, Single-Ended	8.0 $mV/\sqrt{Hz}$
Power Consumption	76.8 mW
Power/Bandwidth	201.85 $\mu W/MHz$
Power/(Bandwidth . pF)	10.1$\mu(W/(MHz \cdot pF))$
Output Load (at each output)	20 pF
Compensation Capacitance	20 pF
Output Swing	1.9 V
Temperature of operation	25.0°C

Chapter 7. Conclusions and Future Work

A novel frequency compensation technique for n-stage operational amplifiers requiring only n-2 passive compensation networks has been developed. The new approach incorporates RC compensation networks embedded around internal stages to relieve the output stage from driving compensation capacitors. Several high-speed, high-gain, multi-stage operational amplifiers have been reported using Nested compensation networks [1][3][4]. These techniques are complex, and multiple compensation networks load the output stage and limit the power/speed efficiency in wideband CMOS applications.

The new design approach has advantages in production over the other designs with respect to the complexity of multiple nested compensation networks. By characterizing these new amplifier topologies, this thesis aims to provide a good understanding multi-stage amplifier design. The designs presented employ n-2 (for n-stages) compensation networks, and have other advantages over the two-stage topology, in achieving high bandwidth and slew rates. It was also shown that even with large compensation capacitors, the internal stages do not limit slew limit due to the associated small output step sizes. The enhancement techniques using global G_m feed-forward technique discussed in Chapter 6 can be used to reduce the sizes of the compensation capacitors. Also, we saw that cascode stages can be used for internal stages to achieve high-gain since only small output swings are required internally.

Accurate doublet cancellation is of paramount importance in multi-stage operational amplifier designs as described in Chapter 3. Techniques have been reported for tracking process, temperature, and voltage variations for accurate pole-zero cancellation. These techniques can easily be used for the new operational amplifier

topologies. For example, the compensation resistors can be either a MOSFET device operating in the triode region, or polysilicon resistors [20][21].

For low-voltage applications, common-mode range of the amplifier is a limiting parameter, but low-voltage V_T calibration techniques can be used to increase the common-mode range by more than 200 mV [20].

In conclusion, the new operational amplifier topology is easily adaptable to tracking and other high-yield schemes commonly used in production.

7.1 Realization of Three- and Four-Stage Operational Amplifiers

An initial characterization has been performed of three- and four-stage prototypes has been implemented in a $0.6\mu m$ CMOS N-Well process from MOSIS. The designs assumed 20 pF loads, and correspond to the three- and four-stage operational amplifiers described in Chapter 6. The compensation capacitor was about 84.0 pF for the three-stage amplifier, and 100pF and 10 pF for the four-stage amplifier. The compensation resistor associated with the three-stage amplifier was about 1900 Ohms and for the four-stage operational amplifier about 1100 and 1930 Ohms.

The corresponding prototype layouts for the three- and four-stage fully-differential operational amplifier is shown in Figure 7.1. There are also some single-ended layouts for three- and four-stage amplifiers are also shown. The area of the three-stage fully-differential design was measured to be $302.7\mu m \times 505.8\mu m$ and the area of the four-stage amplifier was $520.8\mu m \times 536.7\mu m$.

From the layouts of Figure 7.1, a major concern is the area required for the capacitors. Two 50 pF capacitors connected in parallel consumed an area of about $361.8\mu m \times 158.3\mu m$. Since two such capacitors are used for each differential pair, the total area consumed by the capacitors is about one-half of the overall area of the four-

stage amplifier. Note that these layouts do not include the global G_m feed-forward

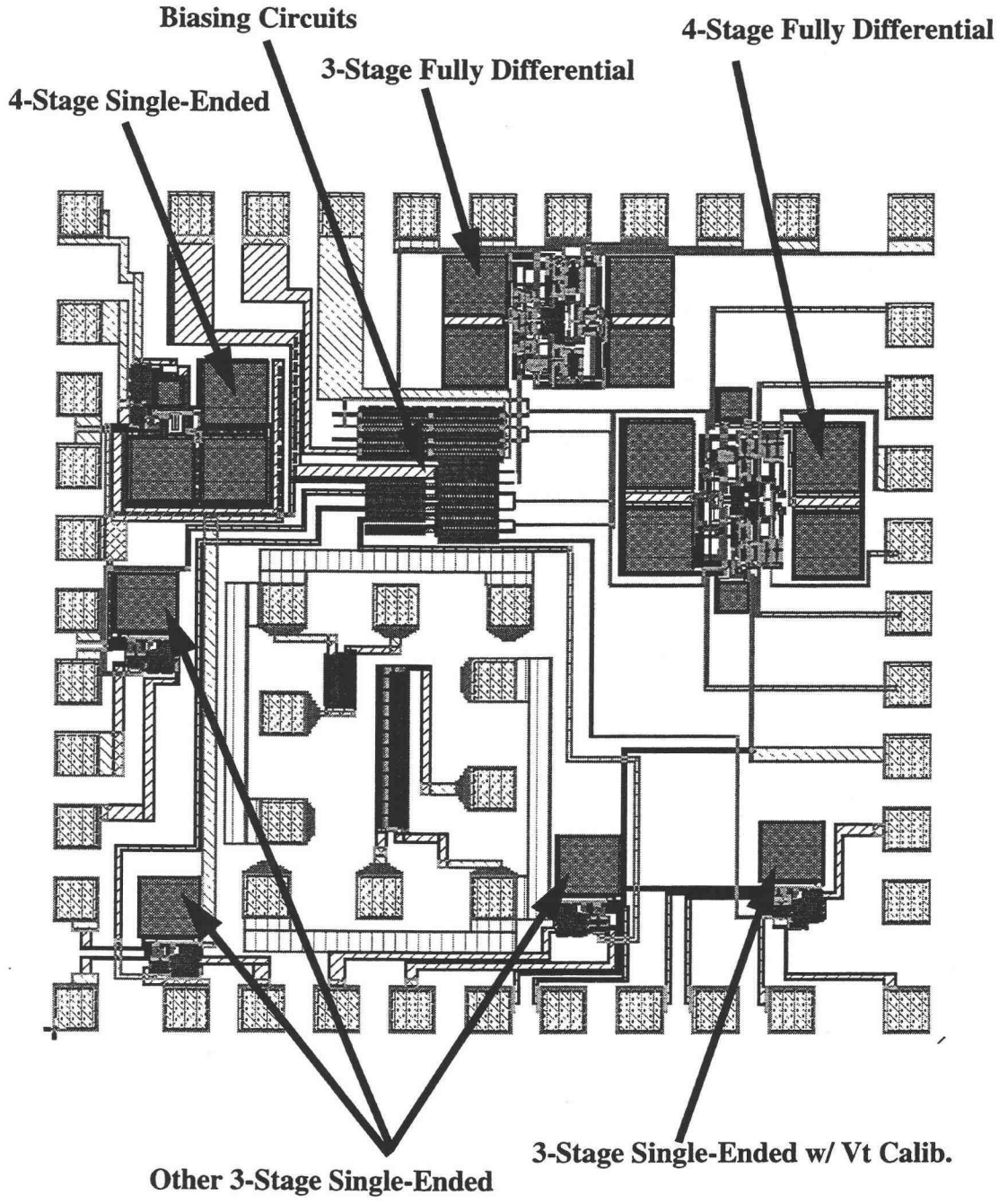

Figure 7.1. Prototype layout of three- and four-stage amplifiers.

designs described in Chapter 6 which effectively reduce the areas associated with the capacitors.

7.2 Future Work

Multi-stage operational amplifiers using embedded RC compensation networks have several advantages over other topologies. Since this technique follows from the widely used two-stage operational amplifiers, the production robustness of these multi-stage operational amplifiers would be very similar. In order to provide low-power tracking RC compensation, several design approaches have been introduced [20][21]. Tracking RC compensation circuitry provides stability and maintains fast settling properties over process, temperature, and voltage variations. In this thesis, pole-zero tracking circuitry was not discussed in detail. However, it is possible to incorporate charge-pump assisted MOSFET resistor tracking pole-zero circuitry [20] for low-voltage applications or polysilicon resistor tracking circuitry [21] into these multi-stage operational amplifiers.

An important issue to investigate is the maximum number of gain stages that can be used before the operational amplifier fails. In Table 6.2, for a four-stage amplifier, the equivalent input noise spectral density was about 320 $\mu V/\sqrt{Hz}$ at 210 MHz, whereas in a three-stage amplifier the input noise was only 9.0 $nV/\sqrt{Hz}$. The reason behind this is that as the number of stages increases, the sizing must become smaller to reduce the input stage bandwidth. As the number of stages increases, pole-splitting becomes more different. The compensation capacitor poles cannot move the dominant pole to lower frequencies, which forces the compensation capacitor to become large for small input stage sizes.

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APPENDICES

Appendix A. Two-Pole Amplifier Response.

Table 7 .1 Two-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	f_n/f_u	T_s/T_u	PM	f/f_u
0.0001	3.85	7.2131	75.8687	0.9697
0.001	3.75	5.7303	75.5284	0.9682
0.01	3.60	4.5239	74.9877	0.9658
0.1	3.35	3.5186	74.0499	0.9612

Appendix B. Three-Pole Amplifier Response.

Table 7 .2 Three-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	f_1/f_u	f_2/f_u	T_s/T_u	PM	GM	f/f_u
0.0001	6.35	1.0	6.3837	72.8899	12.7000	0.9784
0.0001	6.05	1.5	6.0570	72.6474	12.1000	0.9786
0.0001	5.60	2.0	5.9313	72.3159	11.2000	0.9793
0.0001	4.70	2.5	5.6297	71.3854	9.4000	0.9814
0.0001	3.85	3.0	8.0927	71.5585	7.7000	0.9893
0.001	6.20	1.0	5.0014	72.5185	12.4000	0.9775
0.001	5.95	1.5	5.0768	72.4032	11.9000	0.9781
0.001	5.50	2.0	5.0014	72.0781	11.0000	0.9789
0.001	4.55	2.5	4.6244	71.0480	9.1000	0.9808
0.001	3.70	3.0	6.8361	71.3483	7.4000	0.9903
0.01	6.05	1.0	4.1469	72.1361	12.1004	0.9765
0.01	5.75	1.5	4.0464	71.8996	11.5004	0.9769
0.01	5.30	2.0	4.0212	71.5904	10.6004	0.9779
0.01	4.30	2.5	3.7196	70.4786	8.6003	0.9806
0.01	3.70	3.0	5.5543	71.3536	7.4002	0.9903
0.1	5.70	1.0	3.1919	71.2182	11.4039	0.9740
0.1	5.40	1.5	3.1416	70.9953	10.8037	0.9746
0.1	4.90	2.0	3.0913	70.5899	9.8034	0.9760
0.1	3.80	2.5	2.8651	69.3543	7.6028	0.9811
0.1	3.75	3.0	4.2726	71.4746	7.5024	0.9899

Appendix C. Four-Pole Amplifier Response.

Table 7 .3 Four-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	f_1/f_u	f_2/f_u	f_3/f_u	T_s/T_u	PM	GM	f/f_u
0.0001	1.0	2.0	8.00	40.5391	50.3159	1.6800	1.1368
0.0001	2.0	2.0	8.00	17.5175	53.7005	2.8889	0.9853
0.0001	3.0	2.0	8.00	14.3508	57.5181	3.8265	0.9642
0.0001	4.0	2.0	8.00	12.1140	61.0762	4.6250	0.9652
0.0001	5.0	2.0	8.00	10.3798	64.0237	5.3395	0.9697
0.0001	6.0	2.0	7.95	9.0478	66.3528	5.9880	0.9740
0.001	1.0	2.0	8.00	33.6527	50.3163	1.7000	1.1386
0.001	2.0	2.0	8.00	15.2053	53.7013	2.8889	0.9853
0.001	3.0	2.0	8.00	12.0888	57.5186	3.8265	0.9642
0.001	4.0	2.0	8.00	10.1536	61.0767	4.6250	0.9652
0.001	5.0	2.0	7.95	8.5703	63.9835	5.3290	0.9696
0.001	6.0	2.0	7.15	7.0372	65.6208	5.7893	0.9724
0.01	1.0	2.0	8.00	26.7664	50.3208	1.7001	1.1386
0.01	2.0	2.0	7.90	11.5359	53.6255	2.8816	0.9851
0.01	3.0	2.0	8.00	9.8018	57.5239	3.8267	0.9642
0.01	4.0	2.0	7.90	8.1179	61.0007	4.6079	0.9650
0.01	5.0	2.0	7.25	6.5345	63.3616	5.1777	0.9686
0.01	6.0	2.0	8.00	6.2329	66.3998	6.0002	0.9741
0.1	1.0	2.0	8.00	19.8549	50.3662	1.7006	1.1386
0.1	2.0	2.0	8.00	9.1986	53.7589	2.8902	0.9853
0.1	3.0	2.0	8.00	7.4896	57.5774	3.8282	0.9642
0.1	4.0	2.0	7.85	6.0067	61.0128	4.6009	0.9649
0.1	5.0	2.0	8.00	5.4035	64.0828	5.3414	0.9697

Table 7 .3 Four-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	f_1/f_u	f_2/f_u	f_3/f_u	T_s/T_u	PM	GM	f/f_u
0.1	6.0	2.0	6.10	5.9313	62.0958	4.9095	0.9650

Appendix D. Two-Pole Amplifier Response ($\beta \leq 1$).

Table 7 .4 Two-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	β	f_1/f_u	T_s/T_u	PM	f/f_u
0.0001	0.75	2.90	9.8772	71.8570	0.9503
0.001	0.75	2.80	7.4644	71.3096	0.9473
0.01	0.75	2.70	6.0319	70.7355	0.9440
0.1	0.75	2.50	4.6244	69.5261	0.9365
0.0001	0.50	1.90	15.0294	64.5762	0.9032
0.001	0.50	1.90	12.2396	64.5768	0.9032
0.01	0.50	1.80	9.0478	63.5599	0.8954
0.1	0.50	1.70	7.1880	62.5199	0.8866
0.0001	0.25	0.95	30.0336	50.7964	0.7749
0.001	0.25	0.95	24.4793	50.7970	0.7749
0.01	0.25	0.90	18.0704	49.7228	0.7628
0.1	0.25	0.85	14.3257	48.6570	0.7499

Appendix E. Three-Pole Amplifier Response ($\beta \leq 1$).

Table 7 .5 Three-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	β	f_1/f_u	f_2/f_u	T_s/T_u	PM	GM	f/f_u
0.0001	0.75	2.95	2.0	8.7462	64.0245	5.9000	0.9503
0.001	0.75	2.95	2.0	7.4142	64.0250	5.9000	0.9473
0.01	0.75	2.85	2.0	6.0319	63.6475	5.7003	0.9440
0.1	0.75	2.60	2.0	4.5490	62.7414	5.2025	0.9365
0.0001	0.50	2.25	2.0	20.0057	61.3698	4.5000	0.9032
0.001	0.50	2.30	2.0	16.7635	61.5534	4.6000	0.9032
0.01	0.50	2.20	2.0	13.5465	61.1946	4.4002	0.8954
0.1	0.50	2.25	2.0	10.2793	61.4281	4.5022	0.8866
0.0001	0.25	2.10	2.0	48.3805	60.8347	4.2000	0.7749
0.001	0.25	2.05	2.0	40.4134	60.6627	4.1000	0.7749
0.01	0.25	2.05	2.0	32.4212	60.6679	4.1002	0.7628
0.1	0.25	1.95	2.0	24.3788	60.3849	3.9019	0.7499

Appendix F. Four-Pole Amplifier Response ($\beta \leq 1$).

Table 7 .6 Three-pole amplifier results based on minimum settling time.

Settling Accuracy (%)	β	f_1/f_u	f_2/f_u	f_3/f_u	T_s/T_u	PM	GM	f/f_u
0.0001	0.75	6.60	2.0	7.95	7.5398	65.4672	5.7295	0.9723
0.001	0.75	6.60	2.0	7.60	6.3586	65.1661	5.6482	0.9717
0.01	0.75	6.60	2.0	7.00	5.1271	64.5886	5.5035	0.9704
0.1	0.75	6.60	2.0	6.05	4.0212	63.5005	5.2610	0.9675
0.0001	0.50	6.60	2.0	3.10	12.7172	56.1905	4.3647	0.9388
0.001	0.50	6.60	2.0	3.00	10.1285	55.7461	4.3303	0.9365
0.01	0.50	6.60	2.0	2.85	7.9922	55.0396	4.2783	0.9326
0.1	0.50	6.60	2.0	2.60	6.2078	53.7743	4.1920	0.9248
0.0001	0.25	6.60	2.0	1.15	25.1830	40.3449	3.6395	0.8070
0.001	0.25	6.60	2.0	1.15	23.2428	40.3455	3.6395	0.8070
0.01	0.25	6.60	2.0	1.10	17.7940	39.6037	3.6197	0.7982
0.1	0.25	6.60	2.0	1.00	13.0188	38.0812	3.5829	0.7786