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An active-matrix electroluminescent (AMEL) design tool has been developed for the simulation of AMEL display devices. The AMEL design tool is a software package that simulates AMEL device operation using a lumped parameter circuit model. The lumped parameter circuit model is developed primarily to address AMEL power dissipation issues. The AMEL design tool provides a user-friendly approach for investigating the AMEL display device through the AMEL lumped parameter circuit model. The AMEL design tool is programmed in C with a standard Microsoft Windows interface.

Three techniques for power reduction have been identified and investigated: increasing the high voltage NDMOS transistor breakdown voltage, parasitic capacitance optimization, and development of a low voltage phosphor.

Active Matrix Electroluminescent Device Power Considerations

by

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Chapter 1

INTRODUCTION

1.1 Introduction to Display Technology

Electronic systems are pervasive in today's world. In the electronic consumer and industrial marketplace, there is a need for information display devices. These display devices provide the user with necessary information and feedback in order to complete the human interface to the electronic system.

In computer systems, several display technologies have emerged in an attempt to satisfy the many different information display requirements. Among these display technologies, two have identified themselves as leaders in the display industry: cathode ray tube (CRT) and liquid crystal display (LCD) technologies.

Cathode ray tube technology is the most developed and mature display technology in the market today. With over fifty years of television production, the CRT has found its way into over 98% of the households in the United States. The CRT has been accepted as having the highest image quality and lowest cost for video for computer display equipment currently on the market. Among CRT shortcomings are large, bulky packaging and high power requirements.

LCD technology has also become widely embraced in the display industry today. LCD displays have found huge success in the portable computer market for a number of reasons. LCD displays have low power requirements. Current LCD packaging is lightweight and is only few millimeters thick. In addition, the display quality is comparable to CRT display technology. LCD technology has undesirable characteristics as well. LCD displays in general have poor viewing angle and a slow image response.

There are a number of applications in the market today that LCD and CRT display technologies fail to address; for example, head-mounted display (HMD) technology. The HMD device gives users the ability to receive portable information by simply moving their eye to the display device mounted on their head. This display market requires a display technology with high resolution, small dimensions, very high pixel pitch, and high brightness.

Planar Corporation, the worlds largest manufacturer of electroluminscent displays, has developed a high resolution display solution for a number of markets, including the HMD market. Planar has developed an active matrix electroluminescent (AMEL) display.

1.2 Introduction to AMEL Technology

AMEL display devices were developed primarily to address the HMD market. Planar's specific approach combines the driving circuitry and the EL stack on the same substrate. Planar's traditional approach is to deposit an EL thin-film stack onto a glass substrate and to connect it to external driving circuitry. This act of combining the EL stack with the driving circuitry in an active matrix approach reduces the overhead of

interconnect circuitry and at the same time greatly increases the performance of the EL device.

The active matrix approach makes it possible to acquire the extremely high pixel pitch required for HMD devices. Planar's AMEL design is characterized by a 24 μm pixel pitch, one of the highest pixel densities in the display industry to date. A standard VGA-sized display using Planar's AMEL technology would have approximate dimensions of 1.5 cm by 1.1 cm. In addition, the device is very thin, its entire thickness is less than 40 mil [1]. This small package size is desirable and necessary for HMD devices.

Planar has developed this AMEL display primarily for the HMD market. Unfortunately, there are a number undesirable and unresolved issues regarding the AMEL device. These issues must be resolved before AMEL displays can be used in HMD products.

The AMEL device currently suffers from a number of reliability and processing-related issues. For example, there are several burn-out conditions that may occur after the device is initially power on. These driver and pixel burn-out conditions affect the overall reliability and lifetime of the AMEL device. There are also a number of processing issues causing the device to malfunction. These processing issues affect device yield and product quality.

There have been significant improvements in the AMEL device brightness in recent months. Unfortunately, present state-of-the-art AMEL displays still suffer from insufficient brightness.

Finally, AMEL displays are designed primarily for portable systems with limited power resources. AMEL displays currently consume a large amount of power (~775 mW). It is very desirable to reduce the overall power requirements of the display. This would allow the portable system to run longer on a portable power source.

1.3 Thesis Overview

The primary purpose of this thesis is to focus on, and attempt to reduce, the power dissipated in the AMEL device. One of the most common environments for an AMEL display is in an optical headset with a belt-mounted computer. It is essential that the AMEL display dissipate a minimal amount of power. Minimal power dissipation will, for example, allow a belt-mounted computer to run longer on a portable power source.

An AMEL design tool is developed for the simulation of AMEL display devices. AMEL design tool yields additional information regarding power dissipation and is contributing to the design of improved AMEL pixel layouts for VGA displays. In addition, use of this AMEL design tool is also contributing to the development and characterization of optimal device parameters for maximum light output and minimum power dissipation.

The AMEL design tool is a software package that performs transient circuit simulation of the AMEL device. This tool allows the user to explore variation in AMEL display parameters, such as excitation voltage or ITO layer resistance, using an intuitive user interface. The software tool is a key component for the development of high reliability and low power AMEL devices.

Previous research regarding AMEL devices and their power dissipation is presented in Chapter 2. Chapter 3 presents the hardware model developed for AMEL devices in addition to several circuit experiments. Chapter 4 focuses primarily on the software modeling developed and used in this thesis work. Chapter 5 presents results found during this thesis work. Finally, Chapter 6 concludes the thesis work and suggests topics for future work in the field of AMEL display technology.

Chapter 2

LITERATURE REVIEW

This chapter reviews AMEL displays and prepares the reader for a technical discussion of power dissipation in AMEL devices. The first section begins by presenting the AMEL device structure and drive techniques. Next, gray scale and full-color drive techniques are discussed. The chapter concludes by reviewing some additional research regarding AMEL drive and power reducing techniques.

2.1 AMEL Device Structure

The packaged, standard VGA-sized AMEL device is shown in Fig. 1. This display has approximate dimensions of 1.5 cm by 1.1 cm.

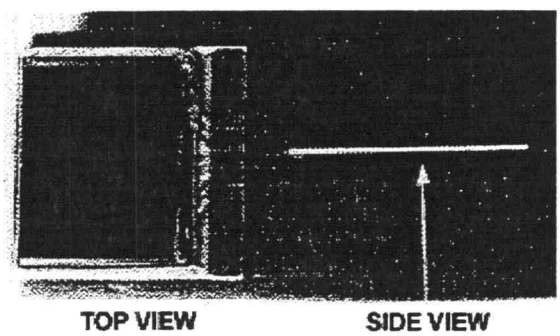


Figure 1 Packaged AMEL device.

The AMEL device architecture is shown in Fig. 2.[1] The AMEL display consists of a grid of pixels. The pixels are addressed through the use of rows and columns. The data shift registers control the rows of the AMEL display. The line drivers control the columns of the AMEL display.

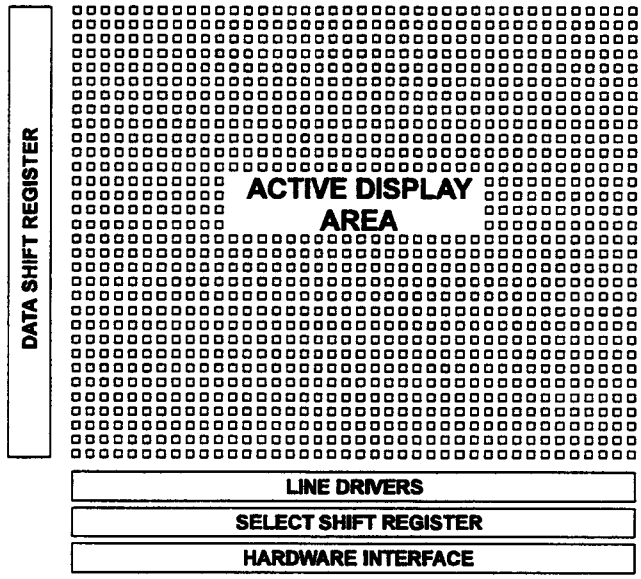


Figure 2 AMEL device architecture.

The circuit diagram of a single AMEL pixel is shown in Fig. 3. Each AMEL pixel is composed of two NMOS transistors driving an electroluminescent (EL) stack deposited directly onto the pixel surface. The AMEL pixel schematic is similar to the schematic of a single DRAM memory cell. The hold capacitor in the AMEL pixel stores a voltage for the AMEL pixel operation. This hold capacitor voltage controls the high voltage NDMOS transistor. The AMEL pixel is illuminated with an excitation voltage. The high voltage NDMOS transistor either allows the EL stack to float or short-circuit's the EL stack to ground, depending on the voltage stored on the hold capacitor. When the EL stack is allowed to float, the pixel does not emit light and the pixel is described as being in the 'off' mode of operation. When the EL stack is short-circuited to ground through the high voltage NDMOS transistor, the EL stack emits light and the AMEL pixel is described as being in the 'on' mode of operation.

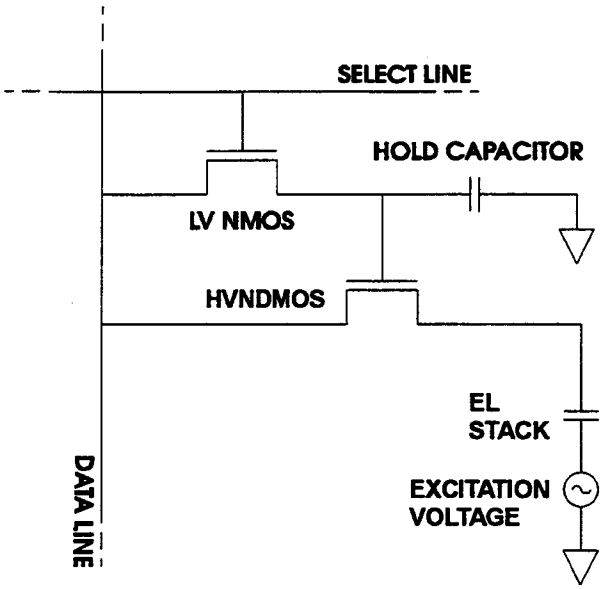


Figure 3 Simplified pixel schematic.

The pixels are arranged in a regular pixel structure, as shown in Fig. 4.[13] They are connected to the driving circuitry through common rows and columns. The rows and columns connect the pixels to the data shift register and the line drivers, respectively.

The data shift register drives the pixel select lines. A single seed bit is shifted through the shift register to address each line of the display individually. Once a line is enabled, the line drivers present the pixel data for an entire row onto the data lines. The data is stored on the hold capacitors of pixels in the selected row.

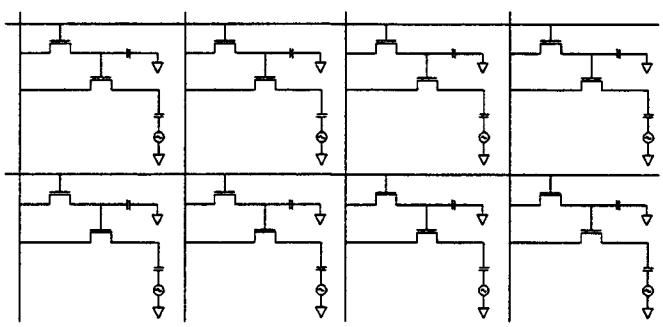


Figure 4 AMEL regular pixel structure.

A hardware interface connects the AMEL display to external driving circuitry. This external driving circuitry takes video information from a video source and conditions it for use with the AMEL display. The video image data are typically stored into frame buffers and transferred to the AMEL device through the hardware interface. Once the pixel data are stored at each pixel location, all of the data lines are driven low and an excitation voltage is applied to the device. This process simultaneously drives all pixels either 'on' or 'off', depending on the voltages stored in the pixel's hold capacitor.

The AMEL display is fabricated using silicon-on-insulator (SOI) technology. The low voltage pixel circuitry and the driving hardware are implemented on the silicon substrate. The high voltage electronics are implemented on an insulated silicon layer deposited directly onto the silicon substrate. The EL stack is deposited onto the insulated silicon layer and connected to the high voltage devices. A transparent conductor, indium-tin oxide (ITO), layer is deposited onto the EL stack and sealed. This top conductor acts as a common electrode to the high voltage excitation. This AMEL stack structure is shown in Fig. 5.[1] The user views the image through the transparent ITO and seal layers.

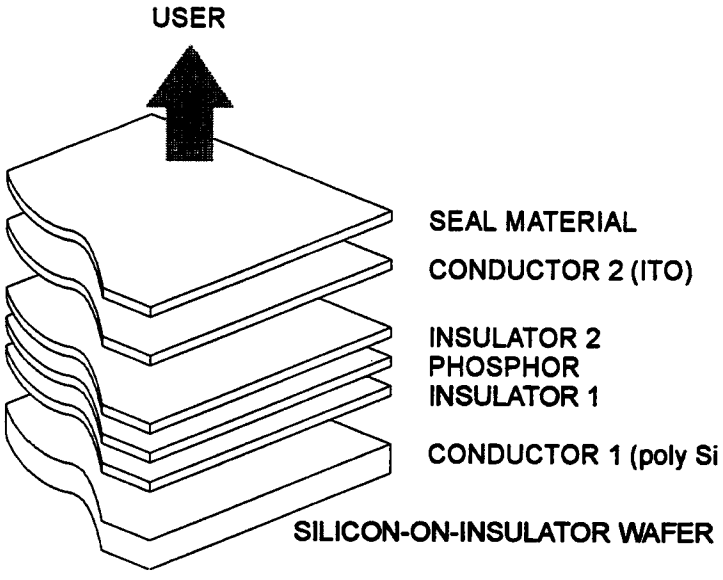


Figure 5 AMEL device structure.

A diagram of the SOI cross-section is shown in Fig. 6. The bulk silicon layer is separated from a suspended silicon layer by a non-conductive insulator layer. The low voltage driver and pixel electronics are contained in the bulk silicon layer. The high voltage transistor and supporting electronics are located in the suspended silicon layer. This device architecture was chosen because of its ability to control large excitation voltages.

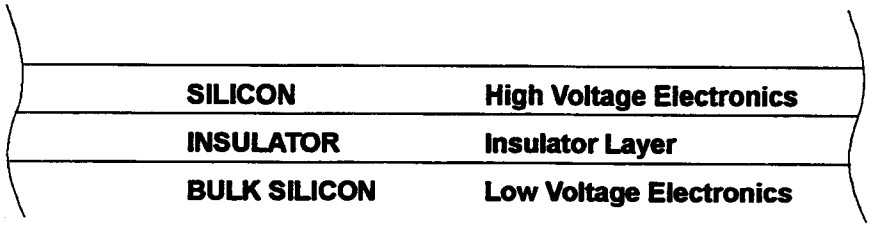


Figure 6 Silicon-on-insulator process technology.

2.2 AMEL Drive Approach

The standard AMEL drive approach consists of two phases: pixel addressing and pixel illumination. The timing for this standard AMEL drive technique is shown in Fig. 7. During the address phase, the excitation voltage is held at ground and each pixel is loaded with pixel data through the low voltage NMOS transistor. Once the pixel data are loaded, the AMEL display is illuminated. During the illumination phase, the low voltage NMOS transistor is turned 'off' and the high voltage NDMOS transistor is either 'on' or 'off', depending on the hold capacitor's voltage. The excitation voltage is applied to every pixel on the AMEL display simultaneously for the duration of the illumination phase. Using this approach, each pixel is capable of two possible intensities: maximum light output or no light output. This type of display is referred to as a 'black and white' display.

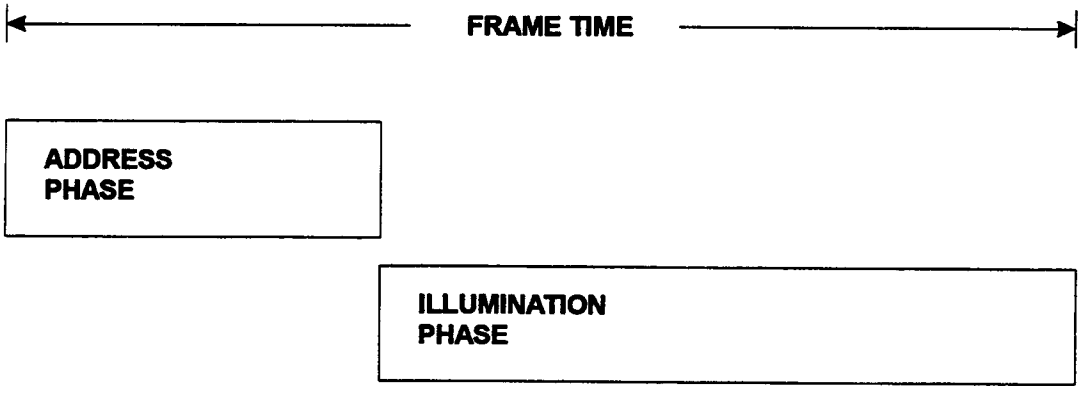


Figure 7 Standard single bit drive approach.

2.2.1 ADDRESS PHASE

Before the display is illuminated, the low voltage pixel state must be loaded onto each pixel's hold capacitor. A simplified AMEL pixel schematic is shown in Fig. 3. The

display is addressed on a line-by-line basis until the entire display is loaded with pixel data. When a pixel is addressed, the select line is driven high and the low voltage NMOS transistor is driven 'on'. Pixel data are presented to the pixel from the data line. When a pixel is addressed, pixel data are stored on the pixel's hold capacitor. Once a pixel's state has been loaded onto the pixel's hold capacitor, the pixel is ready for illumination. After the entire display's pixel state information has been updated the device is ready for illumination.

2.2.2 ILLUMINATION PHASE

The illumination phase directly follows the address phase. During the illumination phase, the EL stack is driven using a high voltage excitation while the high voltage NDMOS transistor holds the second terminal of the EL stack to ground. From the pixel schematic shown in Fig. 3, it is apparent that the data line must be driven low so that it acts as a virtual ground. Using the data line as a ground line during the illumination phase greatly simplifies the pixel layout. Rather than route ground lines to each pixel, the line drivers are capable of driving the data line low as a virtual ground. The HVNMOS transistor connects the EL stack to ground through the line drivers. Once the data lines are grounded, the high voltage excitation is applied to the ITO layer. This high voltage wave drives all pixels simultaneously. Each pixel will either emit light or remain dark, depending on the previously loaded pixel data.

Using this illumination technique only two pixel intensity levels are possible: full 'on' and full 'off'. There are several design approaches for implementing gray scale for an AMEL display.

The current implementation technique for generating gray scale is presented in the Section 2.3.

2.3 Gray Scale Technique for AMEL Devices

A pixel can only be driven 'on' or 'off' using the drive technique discussed in the previous section. This is referred to as a 'black and white' display. In this configuration, each pixel has a single bit of information reserved for the pixel intensity. While this type of display is useful for displaying text, it is undesirable for displaying black and white or color images. A design improvement would employ additional bits of information per pixel. The current AMEL implementation uses a 6 bit per pixel temporal gray scale approach that allows pixels to be driven at different brightness levels. This characteristic of driving pixels to arbitrary brightness levels is very desirable for display applications.

Modification of the drive approach effects power dissipation in the AMEL device. One such modification involves modifying the drive technique to allow additional gray shades per pixel, commonly referred to as increasing the pixel depth. It is important to weigh the gains of increasing the pixel depth and the associated additional power requirements. Increasing the pixel depth gives the user the ability to display more complicated gray scale images as compared to standard black and white images. More importantly, increasing the AMEL pixel depth opens additional markets for the AMEL display. This potential for an additional market share in the HMD industry has led to additional research and development in order to implement high quality AMEL displays with an increased pixel depth.

The temporal gray scale drive approach involves controlling the number of pulses applied to all pixels during each frame. The brightness of any given pixel depends on the number of pulses applied to it. To adjust the number of pulses applied to each pixel, a series of 'sub-frames' are displayed. Each sub-frame contains a variable number of pulses. To determine a pixel's brightness, the pixel is driven 'on' during a specific number of sub-frames to give it the correct brightness level.[14] Shown in Fig. 8 is a 64-level gray scale example. In this example, each sub-frame has exactly twice as many pulses as the previous sub-frame. This approach is analogous to the binary number system. In order to represent 256 unique integers with only 8 bits, each bit is worth twice as much as the previous bit. The temporal gray scale technique uses the binary approach. The intensity level of a pixel varies linearly as a function of the number of pulses applied to the pixel. The AMEL drive circuitry uses the binary approach to drive each pixel with an independent and exact number of pulses. As a result of this drive technique, any image or pattern can be displayed where each pixel can independently display 1 of a possible 64 intensity levels for any given frame.

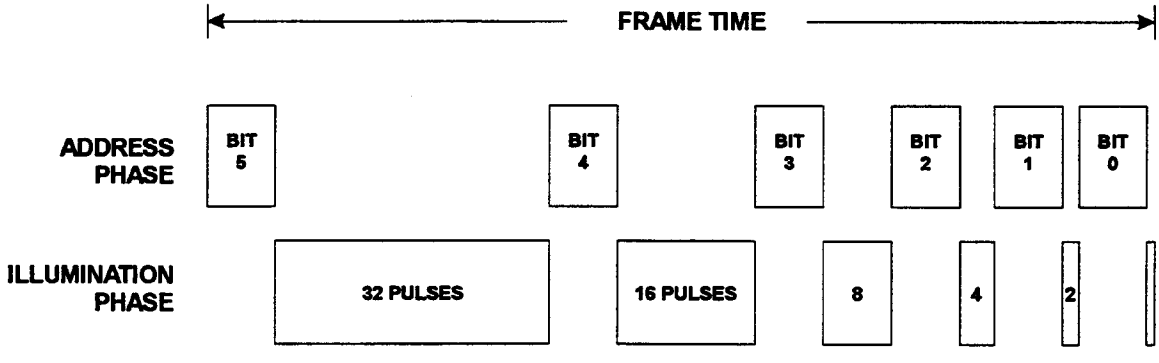


Figure 8 Temporal gray scale drive technique.

2.4 AMEL Color Approach

A full-color AMEL device is the most desirable and marketable display type. Several color approaches have been attempted for the display of full-color images using AMEL devices. To date, the most successful approach uses a liquid crystal shutter.[6] This technique separates the primary colors temporally in an attempt to display full-color images. This approach successfully displays color images. Unfortunately, the gray scale technique also uses a temporal approach. As a result, the number of intensity levels are limited for the color display due to timing constraints. In addition, the display must output an image for each of the primary colors, red, green, and blue in 1 frame time. This increased image rate results in a 300% power dissipation increase. In addition, the requirement to add the liquid crystal shutter increases the total power used in the display system when compared to a standard gray scale display.

A timing diagram for the temporal AMEL color drive approach is shown in Fig. 9. This color drive approach builds on the current temporal gray scale drive approach discussed in the previous section. The color temporal technique separates the image into the primary colors red, green, and blue. Once the image is separated, the three images are displayed in rapid succession. The liquid crystal shutter is located between the AMEL device and the user. The liquid crystal shutter filters light from the AMEL device into the three primary colors. For each frame, the appropriate liquid crystal filter is selected electronically for the duration of the sub-frame.

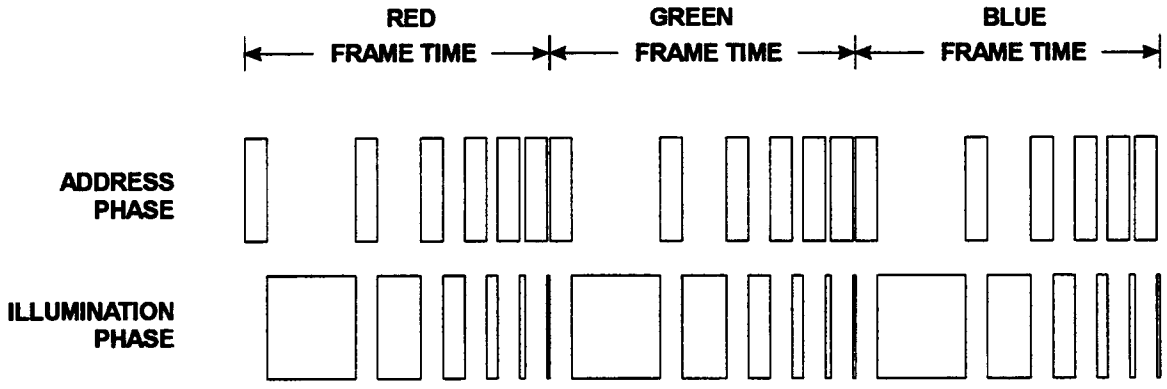


Figure 9 Temporal AMEL color drive approach timing diagram.

A less successful color approach utilizes a color filter to separate the primary colors spatially. This approach has been unsuccessful to date, but with additional research this approach could be implemented successfully in the future. The pixel layout for this technique is shown in Fig. 10.

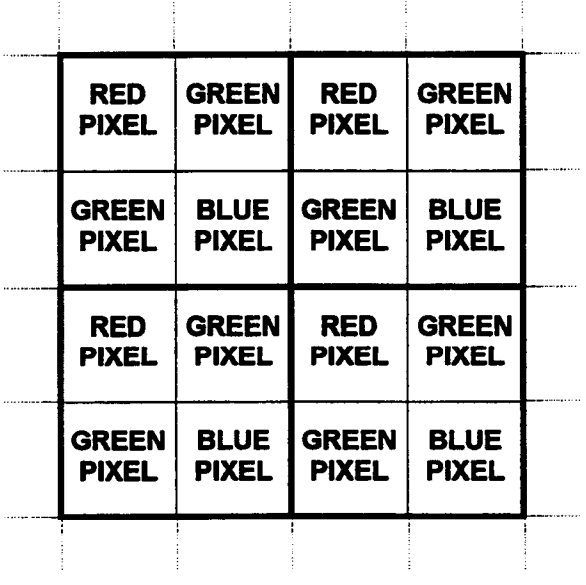


Figure 10 Spatial AMEL color display pixel layout.

Current AMEL pixels experience 'blooming' when illuminated. This blooming sends a portion of the light output of a pixel out through adjacent pixels. This effect is

unnoticeable on gray scale displays. Unfortunately, when illuminating any given pixel, a percentage of its light output is observed on adjacent pixels. This diffuse light reduces spatial color output quality. When the user attempts to display a specific color, pixels illuminated for any specific primary color also illuminate other primary colors as a result of blooming. This side-effect makes the color filter approach impossible until further improvements of the filter, and the pixel light output have been achieved.

The spatial color approach is desirable for long-term AMEL color display technology. The power requirements for the spatial color approach are much less than for the temporal approach. The spatial approach technique uses the same frame rate as used in the temporal gray scale approach. In contrast, the temporal color approach requires a frame rate approximately three times the temporal gray scale approach. As a result, the spatial technique requires considerably less power than the temporal technique. This reduced power requirement makes the spatial color approach a desirable choice for AMEL displays.

Finally, one additional requirement of a filtered color display is the availability of a white phosphor. At this point in development, a true white phosphor is unavailable for AMEL devices. Until a true white phosphor is developed, the AMEL color display output quality is sub-optimal.

2.5 AMEL Analog Drive Approach

A new analog drive approach for AMEL displays for power reduction and improved video performance has been proposed [7]. This approach minimizes the design

complexity of the AMEL device. This new approach is based upon operating the AMEL array in a different manner. This proposed drive approach reduces power dissipation, requires less external circuitry, and is scalable to different AMEL resolutions and display formats. Fig. 11 is a schematic of the proposed analog drive approach.

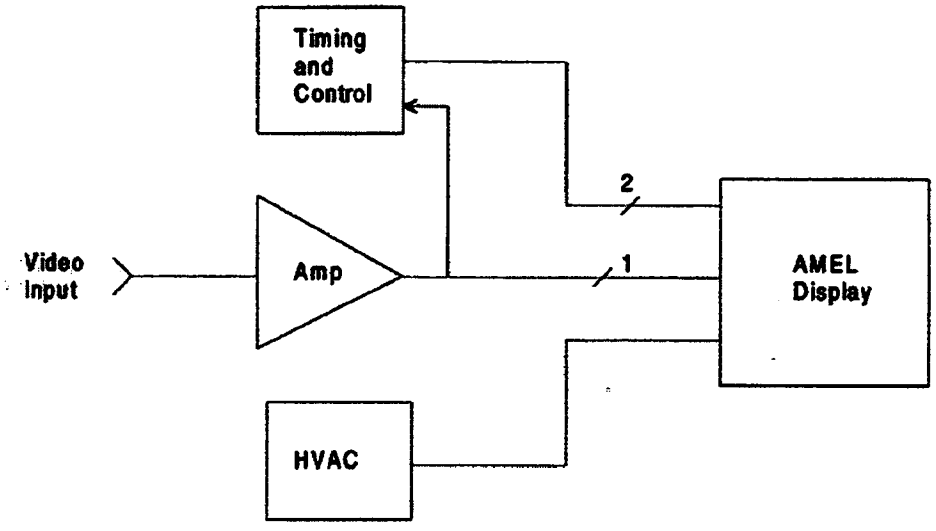


Figure 11 Proposed AMEL analog drive approach.

In this drive technique, the incoming video data is buffered and presented directly to the AMEL device. The intensity level is stored as a voltage at each pixel. The HVNDMOS essentially becomes a comparator. A comparison takes place between the stored pixel voltage and an externally applied ramp signal. The operating waveforms for the proposed analog drive approach are shown in Fig. 12.

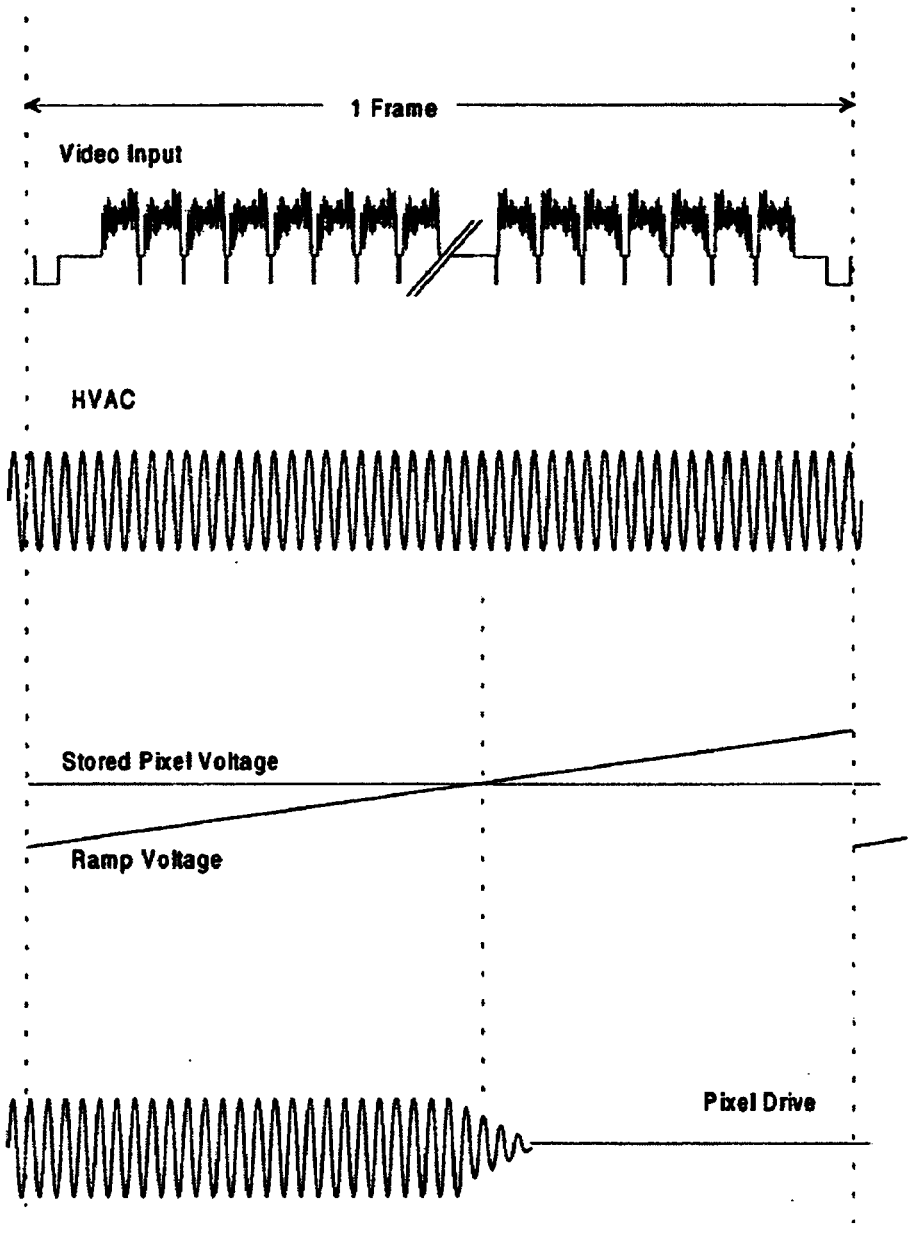


Figure 12 Drive waveforms for the proposed AMEL analog drive approach.

Using this drive approach. A pixel is held on until the ramp voltage becomes large enough to switch off the HVNDMOS transistor in the pixel. Both power and size are reduced using this technique due to the elimination of the external A/D converters and other high-speed driver circuitry. This approach also reduces the data rate to the display and requires less interface interconnection to the device.

Chapter 3

AMEL MODEL DEVELOPMENT

3.1 Determination of a Lumped Parameter AMEL Model

The first step in reducing the overall power dissipation is to create a model for the AMEL display. Shown in Fig. 13 is a circuit schematic of a single AMEL pixel.[1, 12] A VGA display contains approximately 300,000 pixels. The regular pixel architecture of the AMEL display lends itself to simulation using a lumped parameter model.

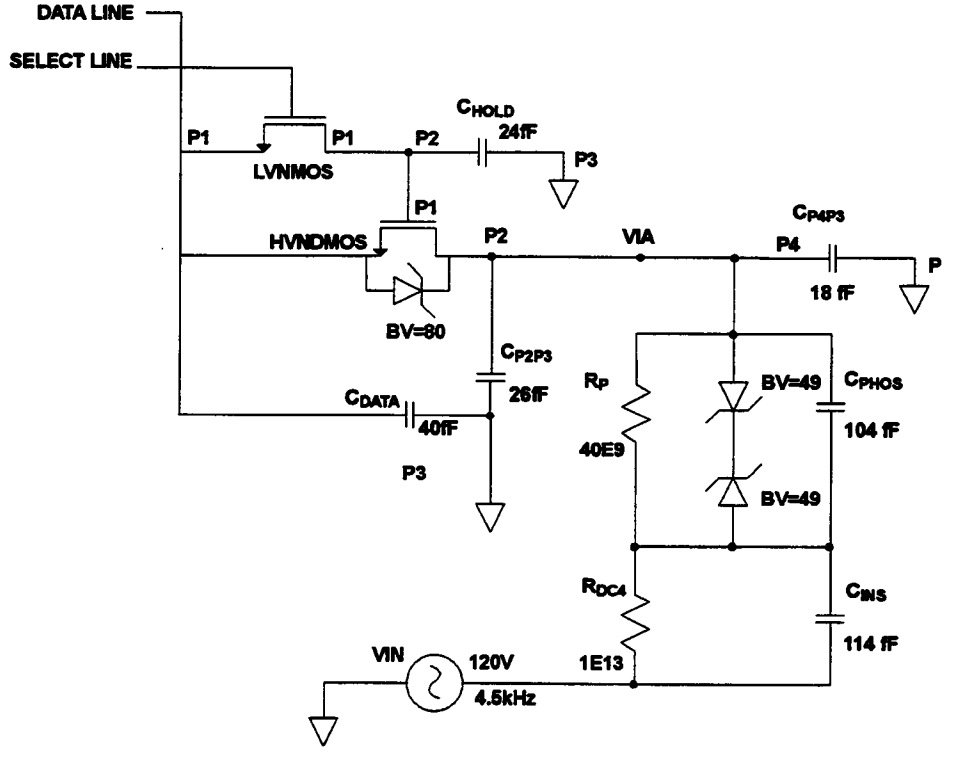


Figure 13 AMEL pixel schematic.

In Fig. 13 the AMEL pixel schematic is shown. The P1 layer is poly silicon and contains all of the low voltage active devices and select lines. The P2 layer is TiW and contains the data lines. The P3 layer is the shield layer and is also TiW. Finally, the P4 layer contains the contacts and is TiW.

Looking at the schematic shown in Fig. 13, a number of circuit simplifications can be employed for circuit simulation. First, the low voltage NMOS transistor and the hold capacitor can be removed since this simulation is not concerned with the hold capacitor or its ability to hold pixel data. Second, the HVNDMOS transistor is assumed in be either in an 'on' or 'off' state as a direct result of the voltage on the hold capacitor.

There are a number of parasitic capacitances associated with the AMEL pixel layout. These parasitic capacitances, shown in Fig. 13, are C_{P4P3}, C_{P2P3}, and C_{DATA}. The low voltage data line parasitic capacitance, C_{DATA}, contributes a negligible amount to the overall AMEL power dissipation and, thus, can be ignored. The remaining two parasitic capacitances, C_{P4P3} and C_{P2P3}, are a direct result of the pixel layout. C_{P4P3} is a parasitic capacitance caused by the fourth metal layer coupling to the third. C_{P2P3} is a parasitic capacitance caused by the second metal layer coupling to the third. These parasitic capacitances have an effect on the overall AMEL power dissipation and are combined and included in the simulation model.

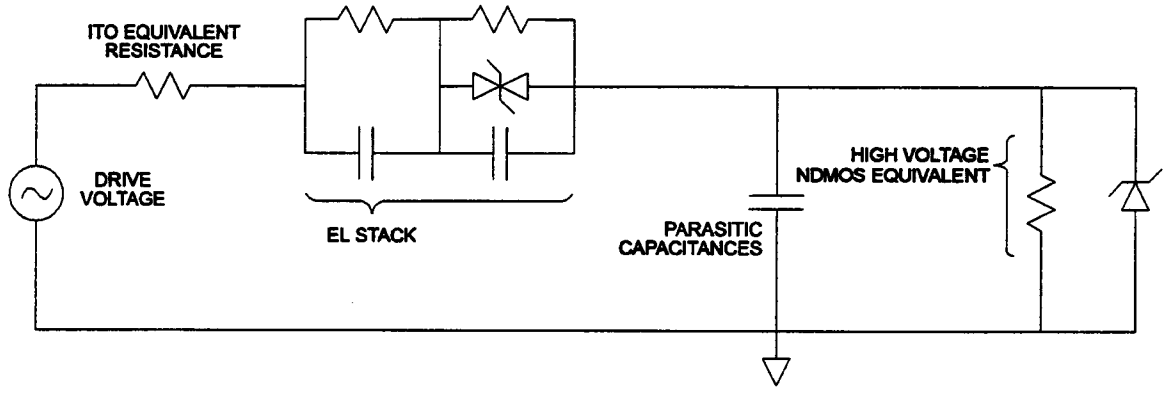


Figure 14 AMEL lumped parameter simulation model.

A lumped parameter model for the AMEL pixel architecture of Fig. 13 is shown in Fig. 14. A number of simplifications and modifications are employed in going from Fig. 13 to Fig. 14. First, the equivalent circuit model of Fig. 14 uses lumped parameters to simultaneously simulate the entire AMEL display rather than a single pixel at a time. Therefore, during simulation all pixels are either 'on' or 'off'. As a result, no inter-pixel dependencies are accounted for in this model. Second, HVNDMOS transistor is modeled as resister and a Zener diode in parallel. The resistor models the intrinsic 'on' or 'off' resistance of the HVNDMOS transistor. The resistance is equal to either the HVNDMOS transistor's 'on' resistance or 'off' resistance. A switch is used to control whether the 'on' or 'off' resistance is present in the circuit. As a result, the same model can be used to evaluate both 'on' and 'off' power dissipation. The Zener diode models impact ionization that occurs when the HVNDMOS transistor breaks down. Next, the electroluminescent phosphor stack is modeled, as shown in Fig. 14, using two capacitances in series to account for the phosphor and insulator capacitances and back-to-back Zener diodes to model the phosphor breakdown. Two resisters are also included in the stack to model the DC leakage through the insulator and phosphor. Finally, the electroluminescent

phosphor stack terminates through a transparent, conductive indium tin oxide (ITO) layer into the high voltage AC supply.

As evident from Fig. 14, when the pixel is in its 'off' state, the HVNDMOS transistor prevents the phosphor from reaching the phosphor breakdown voltage and emitting light. When the voltage across the HVNDMOS transistor exceeds its breakdown voltage, current flows through the HVNDMOS transistor as a result of impact ionization. However, the voltage across the phosphor does not exceed the phosphor breakdown voltage and, as a result, no light is emitted during the pixel's 'off' state.

Values for all of the simulation circuit elements are calculated for the current AMEL fabrication process and drive technique.

3.2 Estimation of AMEL Parameter Values

For the AMEL lumped parameter model to accurately predict AMEL device performance and power dissipation the model parameters must be chosen accurately. This section explains the determination of each parameter in the AMEL lumped parameter model.

3.2.1 Excitation Waveform

The AMEL input waveform used for both experimental measurements and simulation waveforms is a sinusoid. The standard excitation voltage for the standard yellow AMEL device is 120 V at 4.5 kHz. [4]

When the AMEL device is incorporated into a portable system where a 120 V sinusoidal waveform at 4.5 kHz is unavailable, generation of the input excitation is more

difficult. The current AMEL device implementation generates a stepped sinusoidal voltage waveform. This stepped excitation voltage yields very similar AMEL power dissipation as when compared with the 4.5 KHz sinusoidal waveform is used. Power dissipation for both sinusoidal and stepped sinusoidal excitation voltages are discussed in a Section 5.2.

3.2.2 ITO EQUIVALENT RESISTANCE

The ITO layer is a transparent conductor that connects the excitation voltage to the top side of the EL phosphor stack, as shown in Fig. 5. In the current process, the ITO layer has a resistance of 20 Ω / sq.

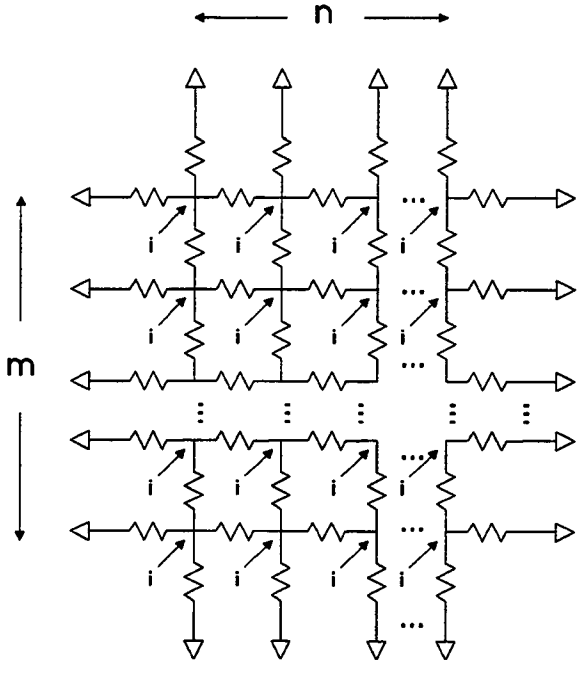


Figure 15 AMEL ITO layer equivalent circuit model.

To determine the lumped parameter ITO equivalent resistance, the model shown in Fig. 15 is employed. In the AMEL structure, each pixel appears as a current source

that terminates into the ITO layer. The architecture shown in Fig. 15 lends itself to this pixel architecture. The circuit model is an n * m matrix where n and m are the horizontal and vertical number of pixels, respectively. For a VGA-sized AMEL device, there are approximately 300,000 current sources in the equivalent circuit shown in Fig. 15.

3.2.3 EL STACK PARAMETERS

The EL phosphor stack is modeled as shown in Fig. 16. Both insulator layers can be combined into a single capacitance. [1,11]

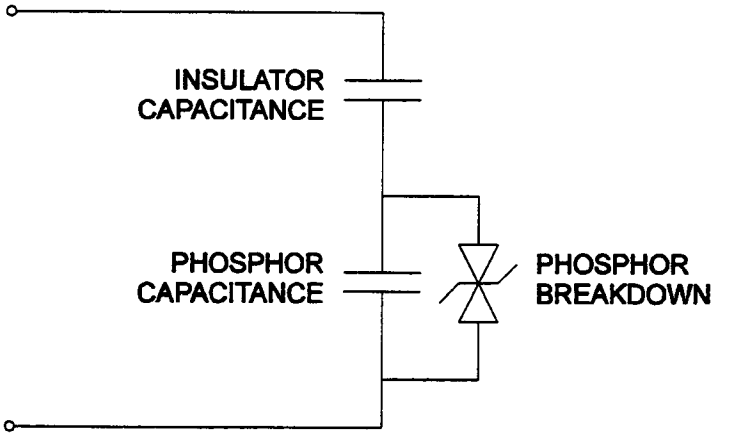


Figure 16 EL phosphor stack circuit model.

The AMEL lumped parameter EL stack equivalent parameter values can be experimentally measured or calculated by multiplying the EL stack equivalent for a single pixel by the number of pixels in the display. The fill factor is defined as the percentage of the pixel that emits light. The stack components can be calculated as follows:

$$insulator1 = 8.84 \cdot 10^{-14} \cdot (insulator1dielectric) \cdot (pixel\_pitch^2) \cdot \frac{(fill\_factor)}{(insulator1thickness)}$$

$$insulator2 = 8.84 \cdot 10^{-14} \cdot (insulator2dielectric) \cdot (pixel\_pitch^2) \cdot \frac{(fill\_factor)}{(insulator2thickness)}$$

$$insulator = \frac{insulator1 \cdot insulator2}{insulator1 + insulator2}$$

$$phosphor = 8.84 \cdot 10^{-14} \cdot (phosphor\_dielectric) \cdot (pixel\_pitch^2) \cdot \frac{(fill\_factor)}{(phosphor\_thickness)}$$

The EL stack insulator and phosphor capacitances are measured experimentally using either a Q-V or C-V measurement as shown in Fig. 17 and Fig. 18, respectively.

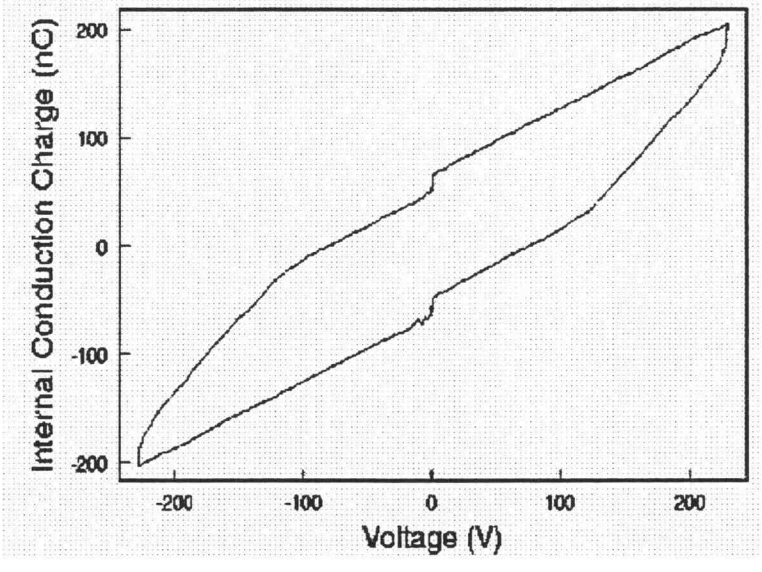


Figure 17 EL stack charge-voltage (Q-V) curve.

It is impossible to directly measure the phosphor or insulator capacitance in an EL stack because it is impossible to measure the voltage between the two capacitances under normal conditions. Therefore, the capacitances must be measured simultaneously. It is possible experimentally measure the phosphor and insulator capacitances using a charge-

voltage (Q-V) measurement, by taking advantage of the phosphor breakdown property. When the EL stack is driven by excitation voltages below the phosphor breakdown voltage the EL stack capacitance measured is that of the phosphor and insulator capacitances in series, the total EL stack capacitance. Conversely, when the EL stack is driven by excitation voltages above the phosphor breakdown voltage the EL stack capacitance measured is that of the insulator capacitance. The phosphor capacitance does not appear in series when the excitation voltage is above the phosphor breakdown because the phosphor breaks down and is essentially short-circuited. This short-circuiting effect makes is possible to measure both the total and insulator capacitances in the EL stack. The total EL stack capacitance is defined as the slope of the Q-V plot at points on the graph below the phosphor breakdown voltage where the phosphor breaks down. The EL stack insulator capacitance is defined as the slope of the Q-V plot at points on the graph above the phosphor breakdown voltage. Once the total EL stack capacitance, C_T, and the EL stack insulator capacitance, C_I, have been measured, the EL stack phosphor capacitance, C_P, can be calculated as follows:

$$C_p = \frac{C_I C_T}{C_I - C_T}. \tag{3.1}$$

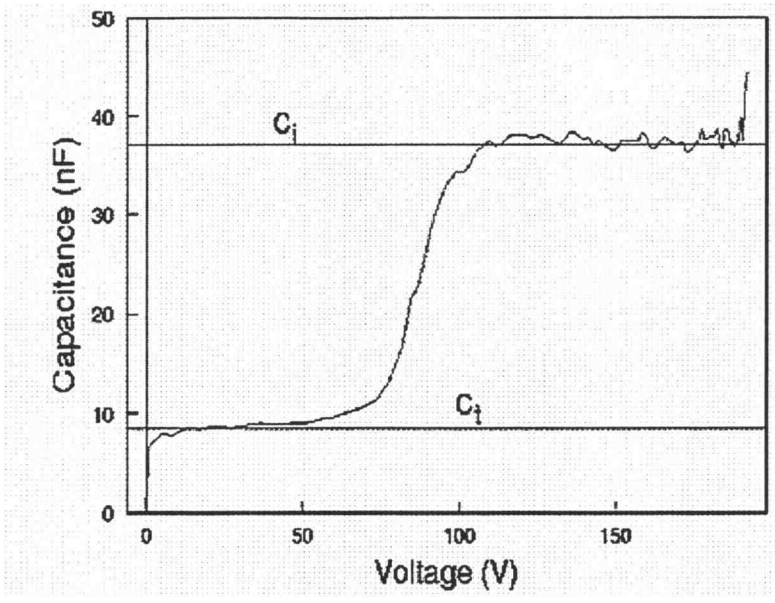


Figure 18 EL stack capacitance-voltage (C-V) curve.

Measurement of the EL stack insulator capacitance and total EL stack capacitance is also possible by using the capacitance-voltage (C-V) measurement. When the EL stack is driven by excitation voltages below the phosphor breakdown voltage the EL stack capacitance measured is that of the phosphor and insulator capacitances in series, the total EL stack capacitance. Conversely, when the EL stack is driven by excitation voltages above the phosphor breakdown voltage the EL stack capacitance measured is that of the insulator capacitance. The total EL stack capacitance is defined as the average capacitance on the C-V plot of points on the graph below the phosphor breakdown voltage where the phosphor breaks down. The EL stack insulator capacitance is defined as the average capacitance on the C-V plot of points on the graph above the phosphor breakdown voltage. Once the total EL stack capacitance, C_T, and the EL stack insulator capacitance, C_I, have been measured, the EL stack phosphor capacitance, C_P, can be calculated from Eqn. 3.1.

For the AMEL lumped parameter circuit model, the phosphor breakdown voltage needs to be measured experimentally. To ensure an accurate breakdown voltage for use with the AMEL lumped parameter model, the phosphor breakdown must be measured experimentally. The phosphor breakdown voltage is obtained by measuring the voltage across the phosphor at the point where the EL stack begins to emit light. This voltage can vary with excitation frequency and wave shape. As a result, it is important to measure the phosphor breakdown with the excitation used for AMEL device operation.

3.2.4 PARASITIC CAPACITANCE

There are a number of parasitic capacitances in the AMEL device pixel layout. The parasitic capacitances C_{P4P3} and C_{P2P3}, shown in Fig. 13, are relevant to the lumped parameter model and are caused by the third metal layer coupling to the second and fourth metal layers. These parasitic capacitances are in parallel. For the current AMEL process, the total parasitic capacitance for a single pixel is 44 fF. This total parasitic capacitance is caused by C_{P4P3} and C_{P2P3} in parallel. The total parasitic lumped parameter equivalent capacitance is this value is multiplied by the number of the pixels in the display to yield a lumped parameter value of 13.5 nF.

3.2.5 HVNDMOS EQUIVALENT RESISTANCE

The HVNDMOS transistor's 'on' and 'off' resistances are derived directly from the fabrication process. The current fabrication process yields an HVNDMOS 'on' resistance of approximately 1 Ω and a large 'off' resistance, on the order of 1 MΩ.[4] These resistances are optimal for the current AMEL device and do not contribute to any sub-optimal performance. The interesting parameter with regard to the HVNDMOS transistor

is its breakdown due to impact ionization. This breakdown effect from the HVNDMOS transistor causes sub-optimal performance in the AMEL device particularly with regard to power dissipation, thermal generation, and contrast ratio.

The HVNDMOS equivalent circuit model used is shown in Fig. 19. The resistor models the 'on' or 'off' resistance of the HVNDMOS transistor, depending on the state of the device. The Zener diode models the breakdown voltage of the transistor.

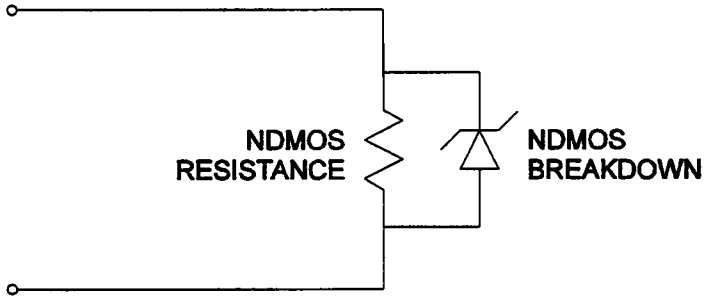


Figure 19 HVNDMOS circuit model.

3.2.6 HVNDMOS BREAKDOWN VOLTAGE

The HVNDMOS transistor breaks down due to impact ionization under large reverse biases. In addition, the HVNDMOS transistor acts like a diode when forward biased. The HVNDMOS transistor equivalent circuit model is shown in Fig. 19. The Zener diode accurately models the breakdown of the HVNDMOS transistor.

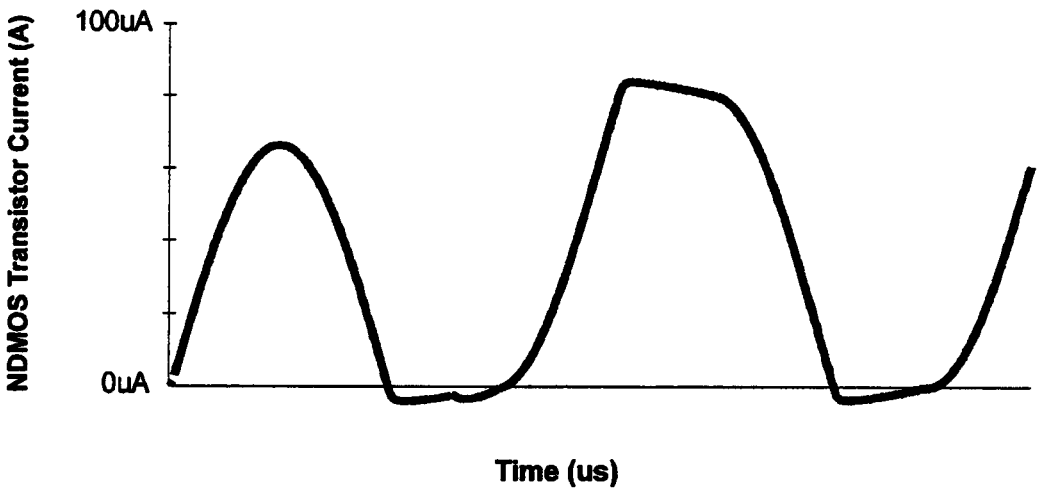


Figure 20 HVNDMOS transistor 'off' current.

As a result of the breakdown within the HVNDMOS transistor, current flows through the AMEL device even when the device is 'off', as shown in Fig. 20. This unwanted current flow contributes to the sub-optimal performance of the AMEL device. This current flow results in power dissipation in the HVNDMOS transistor. This unwanted power dissipation during a pixel's 'off' state is shown in Fig. 21 as a function of the breakdown voltage.

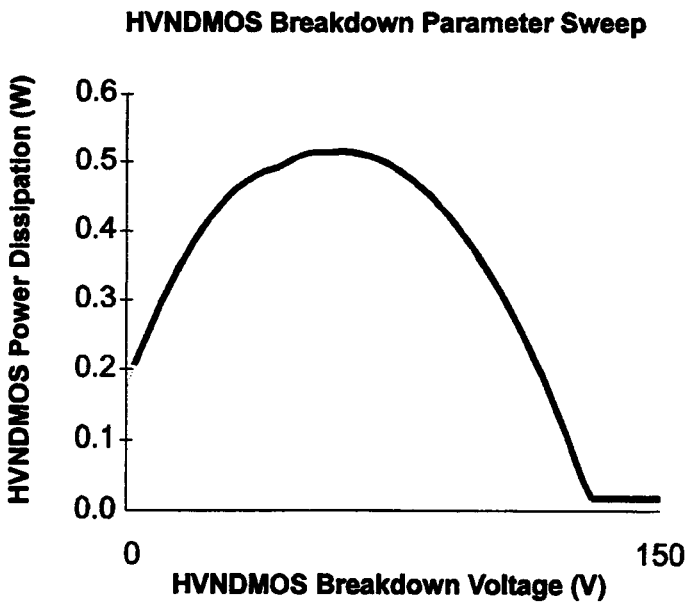


Figure 21 HVNDMOS transistor 'off' breakdown parameter sweep.

Fig. 21 shows that increasing the breakdown voltage to a large enough value reduces the HVNDMOS power dissipation dramatically. Unfortunately, increasing the HVNDMOS transistor breakdown voltage is difficult. Increasing the HVNDMOS transistor breakdown would come at the cost of trading off other desirable features. The HVNDMOS transistor breakdown depends on a number of variables. One of the parameters that the HVNDMOS transistor breakdown depends upon is the epitaxial silicon layer thickness. Redesigning the current AMEL device for another epitaxial silicon layer thickness would come at the cost of lower yields and initial reliability problems. Another parameter that the HVNDMOS transistor breakdown depends upon is the pixel area. In future AMEL devices, the pixel dimensions will continue to decrease as the overall pixel density continues to rise. As the pixel dimensions continue to decrease, the HVNDMOS transistor breakdown decreases as well.

3.3 Parameter Summary

A summary of parameter values used for simulation of the standard yellow AMEL device is provided in Table 1.

AMEL Standard Yellow Device Parameters

PARAMETERS	
Breakdown Voltage	
HVNDMOS (V)	80
Phosphor (V)	49
Display	
Width (pixels)	640
Height (pixels)	480
Parameters	
Pixel Pitch (um)	24
Fill Factor	40%
Pulses / Burst	32
Burst / Second	60
Excitation Voltage	
Magnitude (volts)	120
Frequency (Hz)	4500
Period (sec)	2.22E-04
Sinusoidal	

PARAMETERS	
Circuit Parameters	
ITO (ohms)	80
HVNDMOS On (ohms)	1.00E+00
HVNDMOS Off (ohms)	1.00E+06
Parasitic Cap (nf)	13.5

CALCULATIONS	
Stack Capacitance	
Insulator (nF)	35.04
Phosphor (nF)	32.07
Total Stack (nF)	16.75

ON POWER (mwatts)	
Total	894
EL Stack	735
HVNDMOS	1
ITO	158
Light	710

OFF POWER (mwatts)	
Total	574
EL Stack	24
HVNDMOS	497
ITO	53
Light	14

Table 1 AMEL Device Parameter Summary

3.4 Double Layer Phosphor Extension

In addition to the standard model described in the previous section, a double layer phosphor AMEL model has been developed and is included in the software simulation package. This model is essential when investigating an EL stack with double phosphor layers.

The extended AMEL model is shown in Fig. 22. The standard model has been extended to include a second phosphor capacitance in parallel with two breakdown diodes. With this model it is possible to simulate the voltage, current, and power characteristics of each element in the AMEL device.

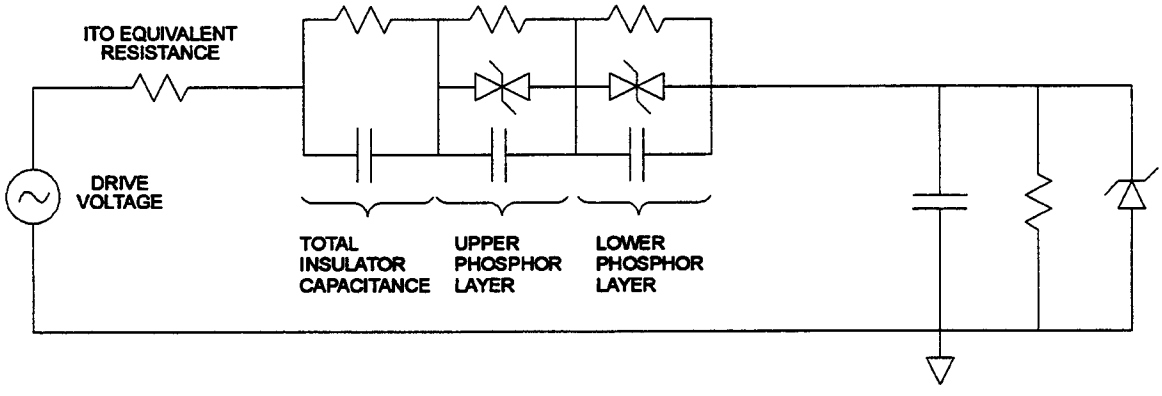


Figure 22 Double phosphor layer circuit model.

This double layer phosphor AMEL circuit model is particularly useful for determining the optimal drive waveform of the AMEL device. Under different excitation waveforms it is possible to adjust the ratio of the light output between the two phosphor layers. A sample power dissipation graph separating each phosphor layer is shown in Fig. 23. The amount of power dissipated in one phosphor layer can be adjusted with respect to the other layer.

This ability to adjust the light output ratio of the two phosphor layers is particularly important when designing EL stacks. Different phosphor layers yield different spectral outputs. Using a dual layer phosphor it is possible to engineer the light spectral density output toward the desired light output spectrum.

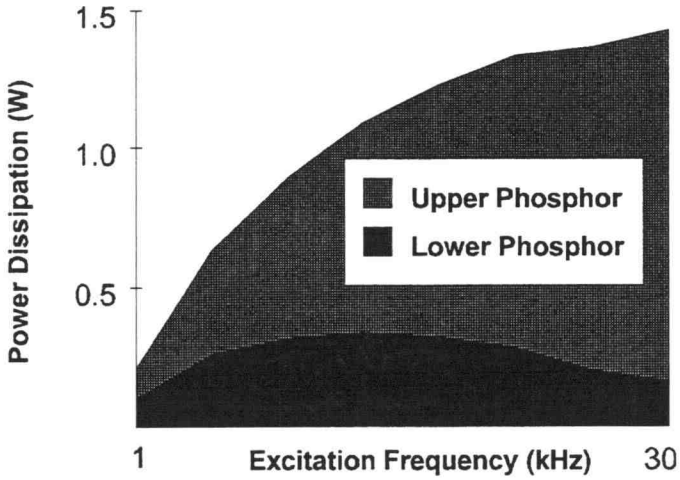


Figure 23 Power dissipation in phosphor layers.

This dual phosphor layer extension to the standard AMEL simulation model is important for designers attempting to develop a 'white' phosphor stack that produces a light output spectrum that appears white to the viewer.

3.5 Overall Model Accuracy

Once all of the parameter values from the previous section have been carefully chosen and verified, the result is an accurate circuit model for the AMEL display. Shown below in Fig. 24 and Fig. 25 both the simulated and experimental waveforms for the AMEL display in both 'on' and 'off' states. The lumped parameter model accurately represents the behavior of the AMEL device in both its 'on' and 'off' states.

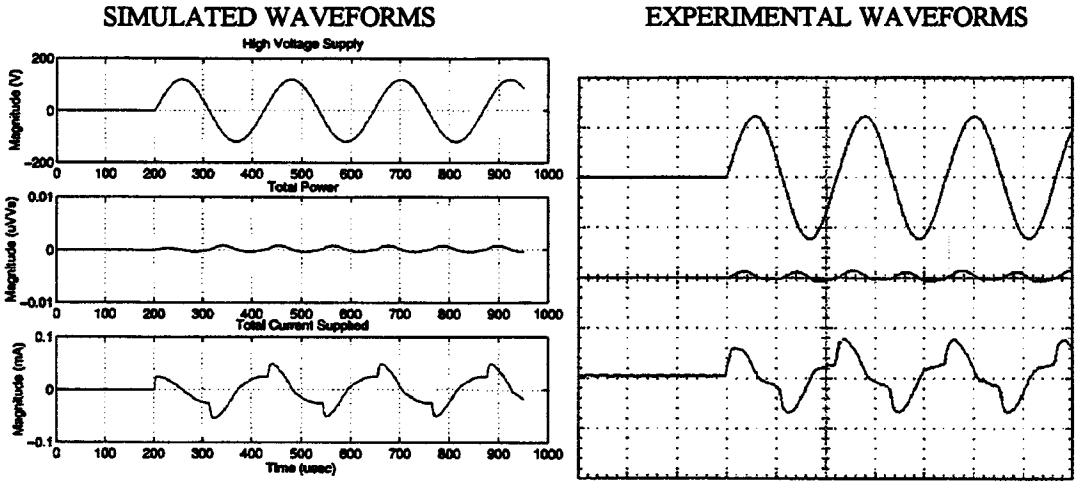


Figure 24 AMEL 'off' waveform comparison.

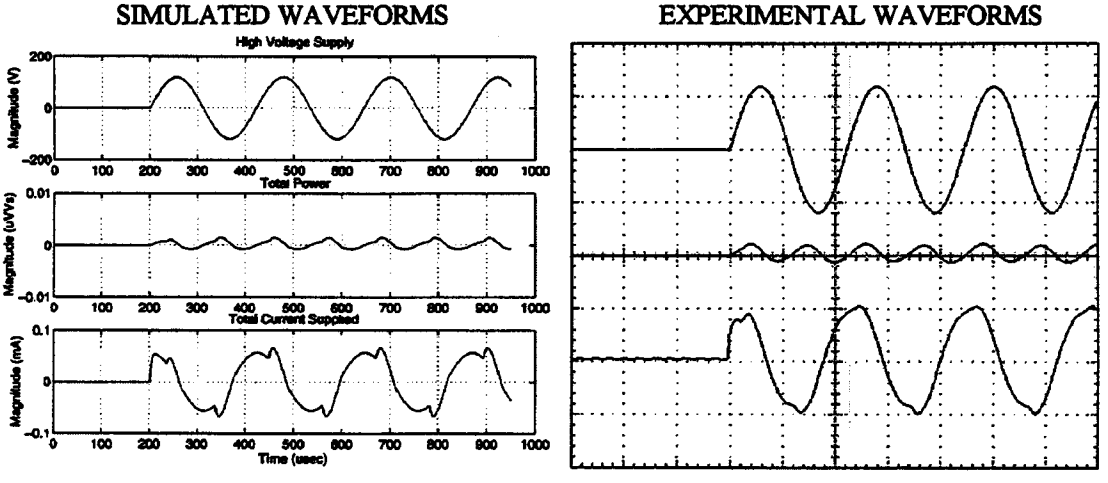


Figure 25 AMEL 'on' waveform comparison.

Finally, Table 2 shows the total power dissipation comparison for both 'on' and 'off' device simulations. Once again, the model accurately describes the behavior of the AMEL display.

Measurement	Simulated	Measured
Total On Power	940mW	944mW
Total Off Power	593mW	594mW

Table 2 AMEL simulation and experimental comparison.

3.6 Techniques for Power Reduction

There are many approaches for reducing power in an AMEL device. In this thesis, the lumped parameter model is developed as an approach for investigating and reducing AMEL device power dissipation.

The AMEL lumped parameter model is an attempt to reduce the complex AMEL device into a simplified circuit model that can be analyzed and optimized. This simplified model has reduced the entire device architecture to a handful of circuit elements for the purpose of power reduction. These AMEL device parameters are: excitation voltage, excitation frequency, excitation wave shape, ITO equivalent resistance, EL stack insulator capacitance, EL stack phosphor capacitance, EL stack phosphor breakdown voltage, total layout capacitance, and HVNDMOS equivalent resistance, HVNDMOS breakdown voltage. These device parameters can be readily investigated and optimized for power reduction with regard to AMEL device operation.

3.6.1 Excitation Waveform

Through the development of the AMEL device, the excitation waveform has proven to be an important part of AMEL display implementation. While the sinusoid is the excitation waveform of choice, it is unavailable in most HMD applications and must

be generated from a portable DC power source. In current AMEL display development, a stepped sinusoid wave is generated by digital electronics from a 12 V DC source when the AMEL display is used in portable systems.[6]

The stepped sinusoid and triangular waveforms have been identified as potentially useful primarily because of waveform generation electronics considerations. The digital electronics for generating the stepped sinusoid and triangular waveforms can be included into the existing hardware easily without using much additional hardware or circuit board space. In addition, modified sinusoidal wave shapes have been investigated in an attempt to increase the total light output, while at the same time reduce the overall power dissipation for the AMEL display.

One particular concern in AMEL display technology is power recovery. Due to the capacitive nature of the AMEL display, a percentage of the total power delivered to the display is returned to the source as reactive power. Excitation waveform generation hardware must also recover reactive power. Finally, the excitation wave generation hardware design should be efficient. The excitation wave generation hardware creates large AC waveforms from a small DC portable power source. Efficient wave generation is essential for extended operation from a single portable power source.

An excitation waveform design for efficient generation and recovery is presented in Fig. 26. This custom waveform is generated using a general two-step generation approach. The waveform is generated efficiently and the hardware is also designed for power recovery.

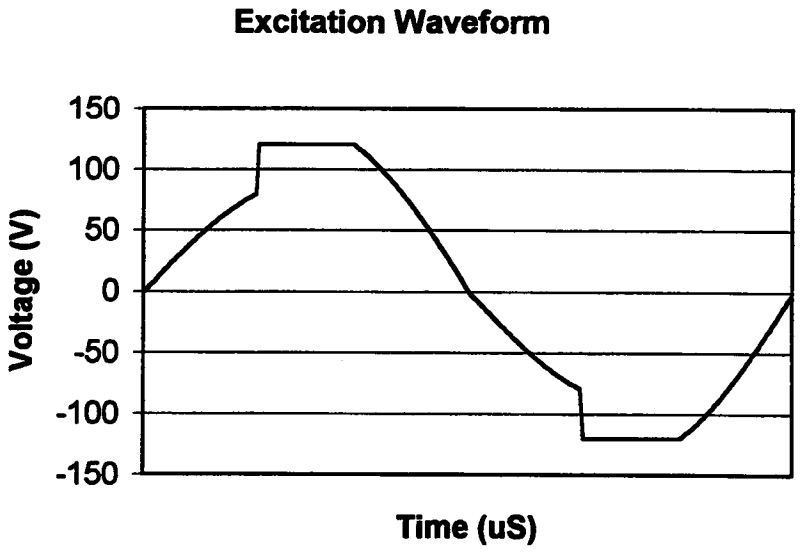


Figure 26 Efficient excitation waveform with power recovery.

Simulation results for the all the waveforms described in this section are presented in Section 5.2.

3.6.2 PHOSPHOR DEVELOPMENT

One of the largest research efforts in present day AMEL display technology is to develop new and improved phosphors for AMEL displays. Researchers are continually developing new display phosphors for use with AMEL displays. There is potential for improved light output efficiency, light output chromaticity, display contrast ratio, and lower power dissipation when new phosphors are introduced into AMEL displays.

A low voltage AMEL phosphor is currently under development. This phosphor breaks downs at a lower voltage than standard display phosphors. The EL stack breakdown voltage is typically 90 V or more. This new low voltage phosphor has an EL

stack breakdown voltage of approximately 60 V.[8] With a reduced phosphor breakdown voltage, overall power dissipation decreases due to reduced excitation voltages.

3.6.3 DEVICE PARAMETERS

Investigating and characterizing the device parameters and breakdown voltages in the AMEL lumped parameter model can yield additional power savings. The AMEL simulation software discussed in Chapter 4 is developed to investigate device parameters and decrease overall AMEL device power dissipation.

Chapter 4

SIMULATION SOFTWARE

4.1 Simulation Design Approach

A software simulation tool, referred to as an AMEL design tool, has been developed that performs transient circuit simulation of the AMEL lumped parameter circuit model, shown in Fig. 14, for any given set of input parameters using an intuitive user interface. In addition, the software tool generates a simulation report that includes overall 'on' and 'off' power dissipation.

The equivalent circuit model shown in Fig. 14 can also be simulated using any standard SPICE simulation software package. However, using a custom, piecewise-linear iterative solution to this non-linear differential simulation problem generates simulation results much faster.[9] The optimized C software tool developed generates accurate simulation results at a speed on the order of 100 transient simulations per second. This high-speed simulation is essential when sweeping or optimizing circuit parameters.

Table 3 shows the total power dissipation for a standard simulation run using a typical sinusoidal voltage excitation. The simulator also generates instantaneous voltage and current outputs, not shown here. At first glance, it is apparent that a standard VGA AMEL display device dissipates approximately 1 W when the device displays a 'full on' pattern and dissipates approximately 0.6 W when the device displays a 'full off' pattern.

Also, Table 3 shows the power dissipation of each circuit element in the simulation. This is particularly useful when identifying problem areas in the AMEL device layout or circuit design.

On Power

Power	Dissipation (mW)
Total	982
EL Stack	832
ITO Layer	149
HVNDMOS	0
Light	672

Off Power

Power	Dissipation (mW)
Total	570
EL Stack	22
ITO Layer	53
HVNDMOS	493
Parasitic	2
Light	13

Table 3 Standard simulation output.

The simulation results show that the total 'off' power dissipation is comparable to the total 'on' power dissipation. This 'off' power dissipation is unacceptably high. A more desirable 'off' power dissipation should be on the order of 1/10 or even 1/100 of the total 'on' power dissipation.

For the simulated 'on' power the majority of the power, approximately 80%, is dissipated in the EL stack. This power dissipation is primarily output as light from the display. It is obvious that in order to decrease the overall power dissipation without sacrificing light output, the focus of power reduction should be with regard to the total 'off' power.

4.2 Transient Approximation Engine

Using the Forward Euler's Approximation Method, a fast AMEL simulation tool is created.[9] The AMEL equivalent circuit used in this simulation is shown in Fig. 14. The companion model, shown in Fig. 27, is required for the approximation algorithm.

The main idea behind the companion model is that the companion circuit represents the original circuit as a single point in time. Each capacitor is replaced with a resistor and voltage source in parallel. The voltage source represents the voltage stored on the capacitor at that instant of time. The resistor represents the appropriate resistance to model the current flow into or out of the capacitor at that instant of time. To progress forward in time, the circuit elements are updated using the current resistor, voltage, and simulation time step values.

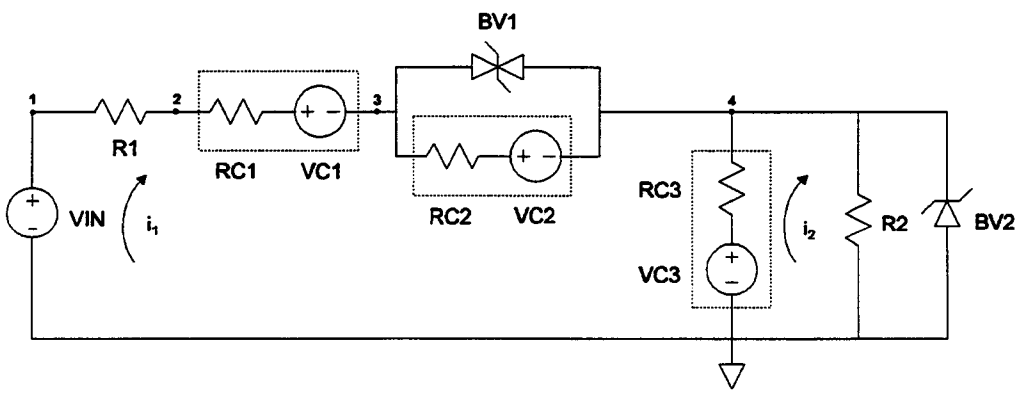


Figure 27 AMEL equivalent circuit companion model.

4.2.1 Instantaneous Voltage and Current Waveforms

The circuit shown in Fig. 27 represents the AMEL equivalent circuit at time t. The voltages vc_1, vc_2, and vc_3 are the capacitor voltages at time t. The resistances rc_1, rc_2,

and rc_3 are the companion model resistances that simulate the correct current flow into or out of the capacitors c_1, c_2, and c_3 at time t. Finally, vin is the excitation voltage at time t. For the actual circuit simulation, the Zener diodes can be removed from the circuit and placed in the simulation software as conditional statements.

The simulation executes with the following initial conditions:

$$rc_1 = \frac{T}{c_1}, \quad rc_2 = \frac{T}{c_2}, \quad rc_3 = \frac{T}{c_3}, \quad vc_1 = 0, \quad vc_2 = 0, \quad vc_3 = 0$$

$$T = Simulation\_Timestep,$$
$$bv_1 = Phosphor\_Breakdown,$$
$$bv_2 = HVNDMOS\_Breakdown.$$

Next, performing standard Kirchoff Voltage Law loop analysis, the loop currents are:

$$i_1 = \frac{v_{in} - vc_1 - vc_2 - vc_3 - \dfrac{(vc_3)(rc_3)}{rc_3 + r_2}}{r_1 + rc_1 + rc_2 + rc_3 + \dfrac{rc_3^2}{rc_3 + r_2}}, \qquad i_2 = \frac{vc_3 + (i_1)(rc_3)}{rc_3 + r_2}.$$

For each iteration, the following operations are performed to update the capacitor voltages:

$$vc_1 = (vc_1 + vcr_1 \cdot i_1), \quad vc_2 = (vc_2 + vcr_2 \cdot i_1), \quad vc_3 = (vc_3 + vcr_3 \cdot i_1).$$

Also, during each iteration, the operating region of the phosphor is identified and updated:

$$if((vc_2 + vcr_2 \cdot i_1) > bv_1) \quad \{ \quad vc_2 = bv_1 - vcr_2 \cdot i_1 \quad \},$$
$$if((vc_2 + vcr_2 \cdot i_1) < bv_1) \quad \{ \quad vc_2 = -bv_1 + vcr_2 \cdot i_1 \quad \}.$$

Finally, the operating region of the HVNDMOS transistor, modeled as a Zener diode, is identified and updated:

$$if(v_4 > bv_2) \quad \{ \; vc_3 = bv_2 - vcr_3 \cdot (i_1 - i_2) \; \},$$

$$if(v_4 < 0) \quad \{ \; vc_3 = -vcr_3 \cdot (i_1 - i_2) \; \}.$$

The previous current equations and conditional statements yield instantaneous voltage and current waveforms for all nodes in the equivalent circuit. Shown in Fig. 28 and Fig. 29 are transient voltage and current waveforms. These waveforms are generated from the algorithm described above.

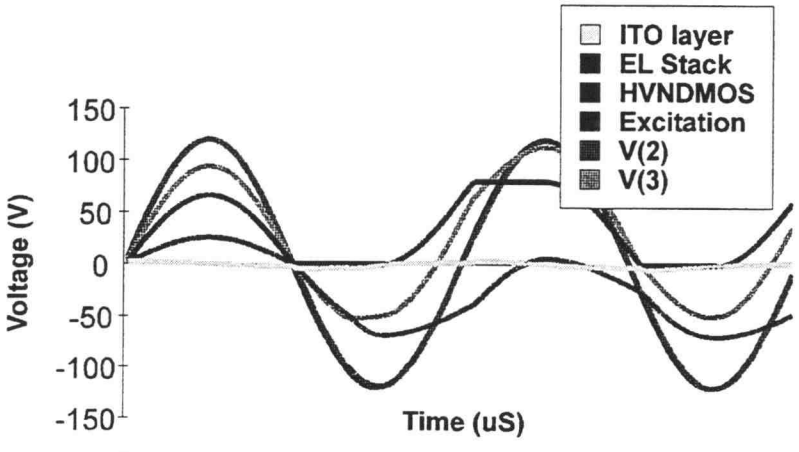


Figure 28 Transient simulation voltage waveforms.

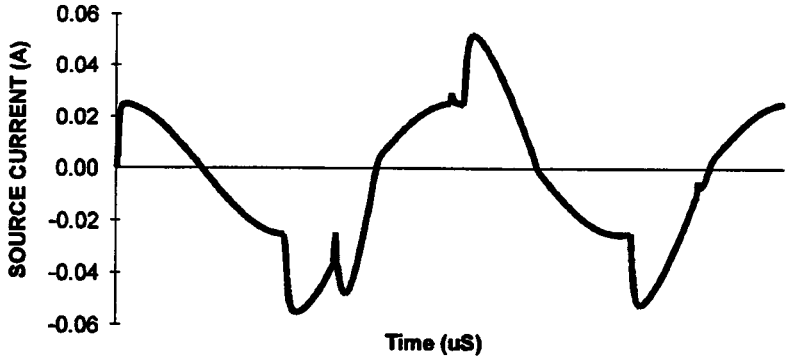


Figure 29 Transient simulation current waveform.

Once the instantaneous waveforms have been calculated, the power dissipation for the circuit can be obtained. C source code for the simulation algorithm is included in Appendix C. In addition to the circuit simulation software written in C, simulation algorithm is implemented in Excel. The use of Excel, allows a simple user interface to be added to the simulation. Furthermore, the use of Excel allows for cross platform accessibility. A screen capture of the AMEL simulation spreadsheet is shown in Appendix B.

4.3 Power Calculations

Once instantaneous voltage and current waveforms are calculated, the calculation of AMEL power dissipation is possible. The following definitions are used in the power calculation:

Pulses=number of pulses per burst,
Burst=number of bursts per second,
T=period of excitation,
j=total number of iterations.

The power calculation formulas used are as follows:

Description	Power Calculation
Total power dissipation	$\frac{\left(2\sum_{i=1}^{j} v_1 \cdot i_1\right) \cdot pulses \cdot burst \cdot T}{j}$
ITO layer dissipation	$\frac{\left(2\sum_{i=1}^{j} (v_2 - v_3) \cdot i_1\right) \cdot pulses \cdot burst \cdot T}{j}$
EL stack dissipation	$\frac{\left(2\sum_{i=1}^{j} (v_3 - v_4) \cdot i_1\right) \cdot pulses \cdot burst \cdot T}{j}$
Parasitic dissipation	$\frac{\left(2\sum_{i=1}^{j} v_4 \cdot (i_1 - i_2)\right) \cdot pulses \cdot burst \cdot T}{j}$
HVNDMOS dissipation	$\frac{\left(2\sum_{i=1}^{j} v_4 \cdot i_2\right) \cdot pulses \cdot burst \cdot T}{j}$

4.4 AMEL Design Tool Overview

Until now, the AMEL research and development effort has lacked a user-friendly simulation environment. The development of an AMEL design tool attempts to make AMEL simulation accessible to both engineers and researchers. This AMEL software package replaces previously inaccessible or cryptic simulation environments with a fast, easy to use, and software package for IBM PC and compatible computers under Windows 3.1® or Windows 95®.

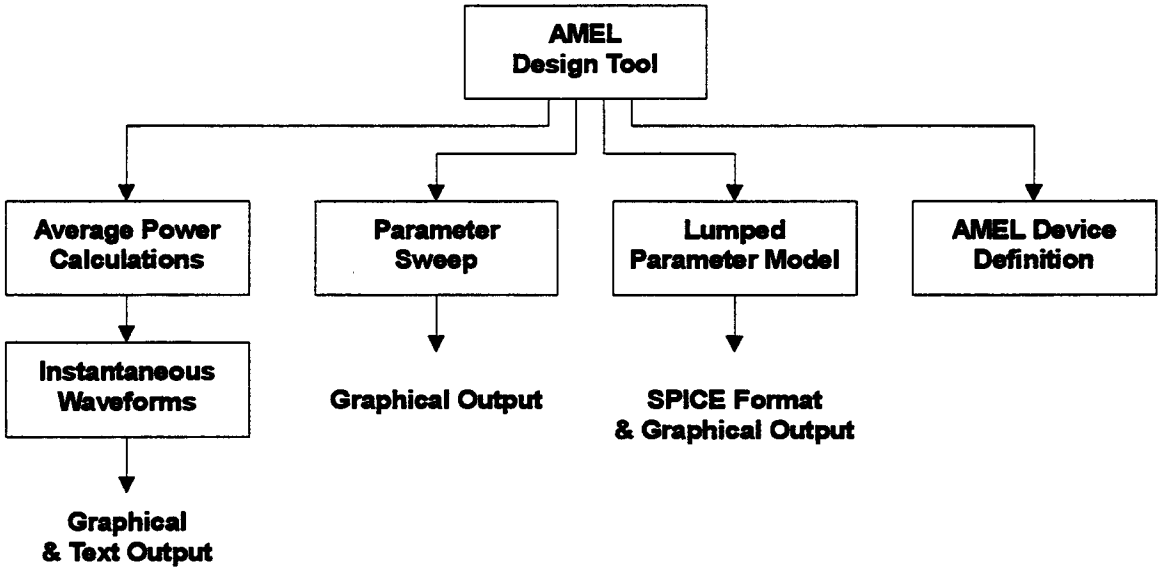


Figure 30 AMEL design tool hierarchy.

The AMEL design tool has several primary functions. A hierarchical view of the AMEL design tool's functionality is shown in Fig. 30. First, the software estimates the total power dissipation in each of the components of the AMEL display for both 'on' and 'off' excitations. Secondly, the software gives the user the ability to run parameter sweeps of all the device parameters in the simulation model. This quick and powerful tool provides an excellent approach for finding possible optimizations in the AMEL display. The user can export any simulation or AMEL display profile to a SPICE file and simulate the device using standard circuit simulation software. The user also has the ability to view and export instantaneous simulation waveforms, as shown in Fig. 32. Finally, the software allows developers to store and trade circuit and phosphor configurations of current, future, or hypothetical AMEL displays.

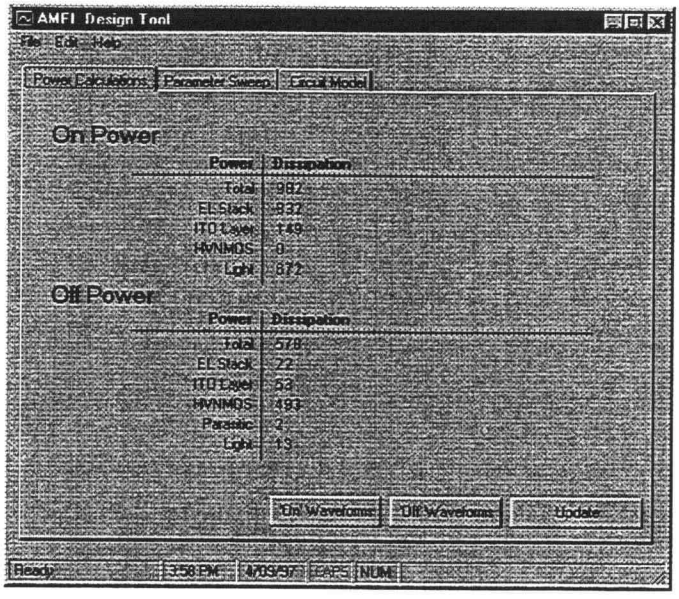


Figure 31 AMEL design tool estimated power dissipation.

4.4.1 AVERAGE POWER CALCULATIONS

Shown in Figure 31 is a sample estimation of power dissipation for the current AMEL display. From this screen, the user can view and export instantaneous simulation voltage and current waveforms for both 'on' and 'off' power dissipation.

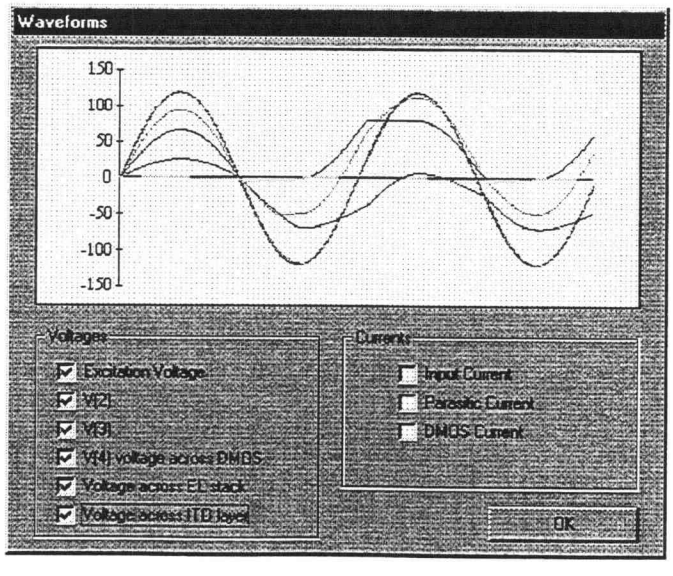


Figure 32 AMEL design tool instantaneous waveform window.

4.4.2 PARAMETER SWEEPING

A sample parameter sweep simulation is shown in Fig. 33. The simulator can sweep any of the following parameters: input voltage magnitude or frequency, either phosphor layer's capacitance or breakdown voltage, insulator capacitance, HVNDMOS resistance or breakdown voltage, parasitic capacitance, or ITO resistance. This ability to sweep any of the model parameters gives the software maximum flexibility to uncover potential power reduction routes. When a parameter sweep simulation is executed, the following are potential simulation outputs: total power dissipation, HVNDMOS dissipation, parasitic capacitance dissipation, phosphor dissipation, EL stack dissipation, insulator dissipation, light output, light output efficiency, and ITO layer dissipation. This user-friendly approach to AMEL parameter sweep simulations makes the AMEL design tool a desirable approach when investigating AMEL display operation.

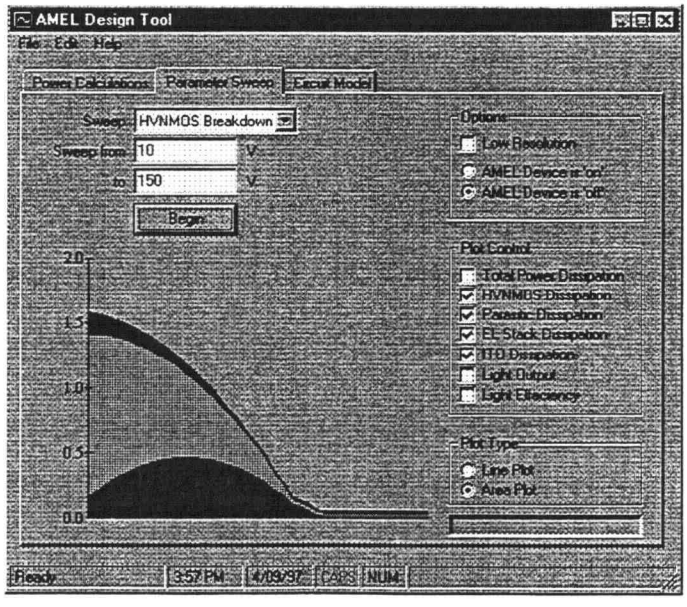


Figure 33 AMEL design tool parameter sweep.

In the AMEL design tool, the light output is defined as the amount of power dissipated across the phosphor. The actual amount of power dissipated in the phosphor as light depends on the efficiency and the excitation voltage and waveform. In the AMEL design tool, the light output efficiency is defined as the amount of power dissipated in the phosphor divided by the total power dissipated in the device. The light output and light output efficiency outputs are available to the user as additional information to contribute to efficient EL stack dissipation in AMEL display designs.

4.4.3 INTERNAL CIRCUIT MODEL

Shown in Fig. 34 is the internal circuit model used by the simulation software. This object-oriented circuit model updates automatically to reflect the correct component and parameter values with respect to the user input. The user can export this model directly to SPICE for simulation or to any windows application such as Microsoft Word for presentation.

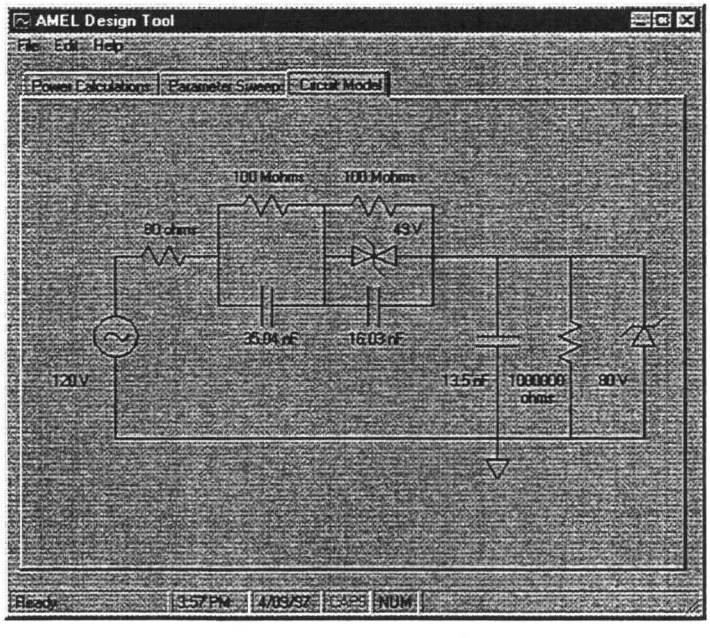


Figure 34 AMEL design tool circuit model.

4.4.4 AMEL Device Description

The AMEL design tool user interface has a number of parameter input screens. They are appropriately subtitled AMEL specifications, excitation, ITO layer, EL stack, display characteristics, and description. Each input window contains a number of input fields associated with the AMEL display. Combined, the six parameter input screens contain the entire AMEL display profile and all parameters required for a complete and accurate AMEL display simulation.

The first of the parameter input screens is shown in Fig. 35. This window describes the layout of the display. The two input fields describe the number of AMEL display pixels. The input window queries the user for the width and height of the AMEL display, in terms of the number of pixels in each dimension. From this input, the simulation can take parameters calculated for a single pixel and multiply the parameters to generate a lumped parameter model for the entire AMEL display.

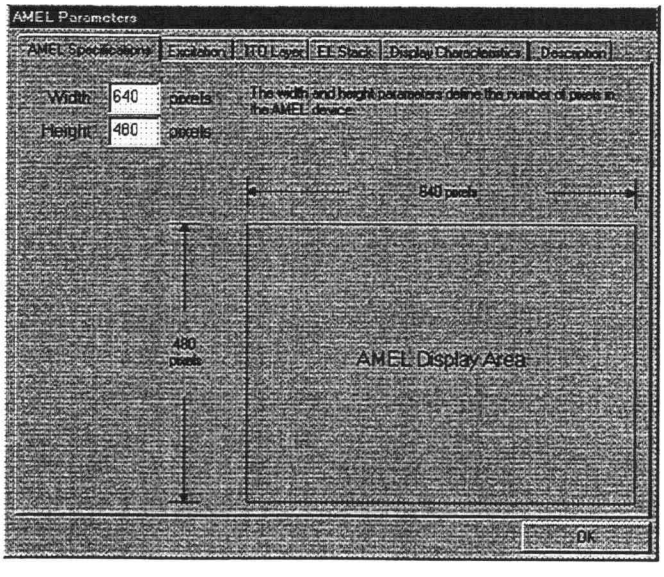


Figure 35 AMEL design tool total pixel input window.

The excitation input window is shown in Fig. 36. This input window describes the high voltage input excitation wave. The user can select from a number of standard input wave shapes including sinusoidal, square, and triangular waveforms. The input also requires the waveform's magnitude and frequency. In addition, the software can simulate a stepped-input wave shape. This stepped-input wave shape generation is excellent for simulating excitation waveforms generated with digital logic or other stepped-input wave shape generators. More creative input waveforms generated by other applications such as Matlab or MathCAD can also be imported through this window for simulation. This flexibility with regard to the input excitation is essential for simulation of common input waveforms.

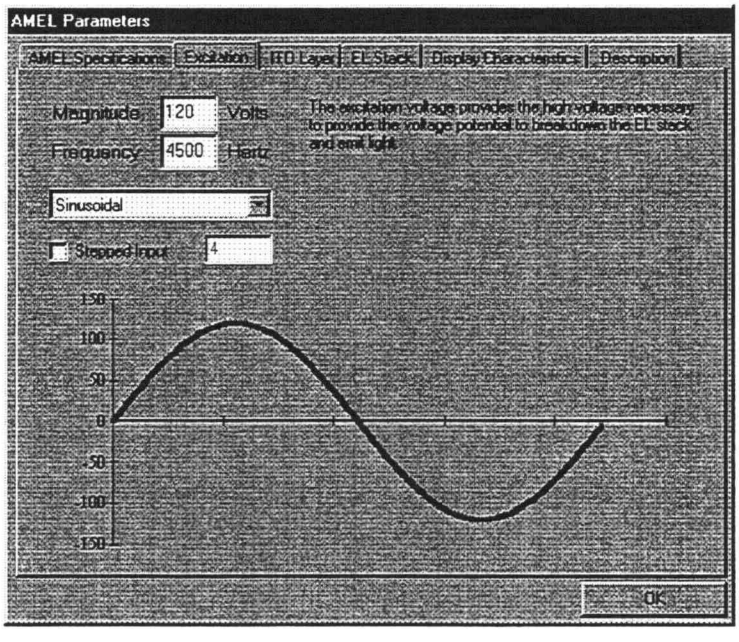


Figure 36 AMEL design tool excitation input window.

Shown in Fig. 37 is the ITO layer input window. This parameter window describes the ITO equivalent resistance used in the AMEL display simulation. This parameter is input in Ω / sq. The equivalent ITO resistance is the resistance seen from the EL stack looking towards the excitation voltage. The ITO transparent conductor connects the EL stack to the pixel excitation voltage. This is a non-ideal resistive transparent conductor. This layer has an associated resistance used for the lumped parameter simulation. The software calculates the equivalent resistance for use in the lumped parameter model, as described in the Chapter 3.

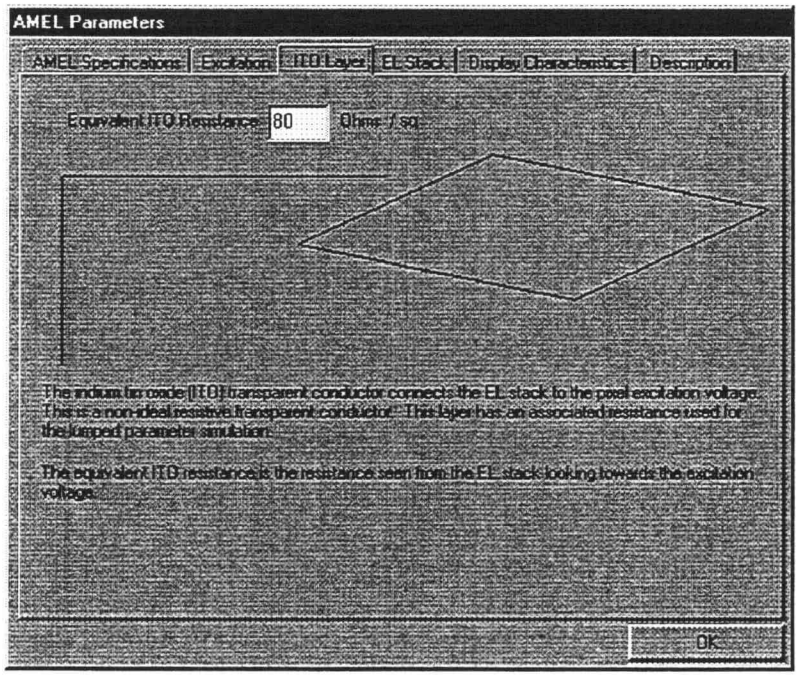


Figure 37 AMEL design tool ITO layer input window.

The AMEL design tool uses the EL stack parameters to generate a lumped parameter capacitance for the AMEL display. The EL stack input window is shown in Fig. 38. Using this input window, the user can describe the phosphor and insulator layers

used in a particular AMEL display. This simulation software generates capacitances for the insulator and phosphor layers as described in the previous chapter for use with the AMEL lumped parameter model. This software supports both single and double layer phosphor stacks. The software also gives the user the ability to enter the stack capacitances directly. This option is useful when the phosphor and insulator capacitances are measured experimentally and an accompanying simulation is required.

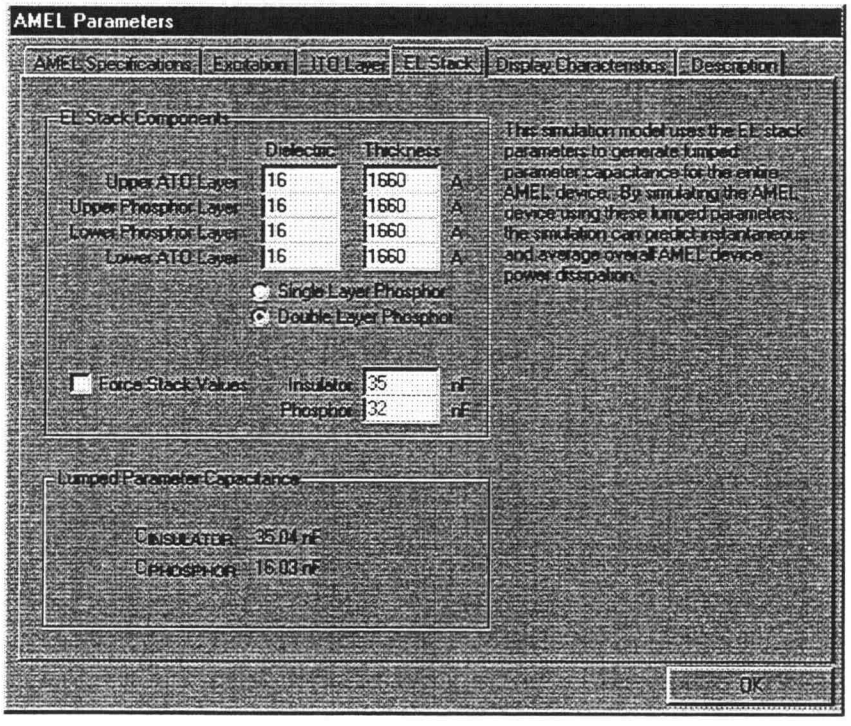


Figure 38 AMEL design tool phosphor stack input window.

The display characteristics input window is shown in Fig. 39. This input window contains the remaining simulation parameters not addressed in the previous input windows. The EL stack breakdown is the voltage potential across the phosphor that causes the phosphor to break down and emit light. The HVNDMOS transistor breakdown

voltage defines the voltage that the HVNDMOS transistor breaks down due to impact ionization. The display parameters define additional AMEL device characteristics. The pixel pitch defines the physical pixel width and pixel height. The fill factor defines the percentage of the pixel area that emits light. The pulses per burst and burst per second define the pixel drive scheme. The parasitic capacitance is the total parasitic capacitance in the pixel layout. Finally, the AMEL display is switched to 'on' or 'off' depending on the desired simulation. For a simulation where the entire display is turned 'on' the user selects 'device is on'. Conversely, if the user desires an 'off' simulation, 'device is off' is selected.

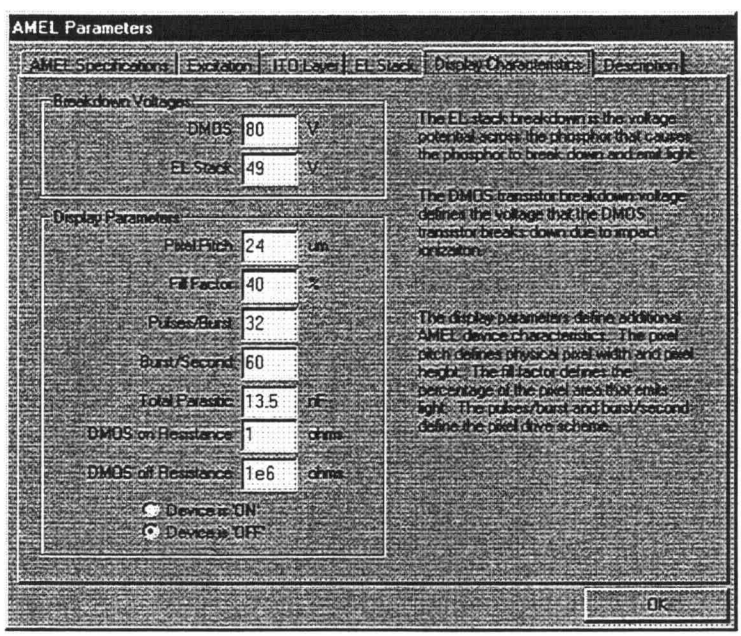


Figure 39 AMEL design tool parameter input window.

Overall, the AMEL design tool is of great utility for AMEL developers. The intuitive software makes simulating and predicting AMEL device power dissipation accessible to engineers. In addition, it makes investigating potential AMEL device power

reductions straight forward. The software is an excellent development tool for both predicting and optimizing power dissipation within the AMEL display. The fast power dissipation and parameter sweep simulation capabilities make this tool excellent for both existing and future AMEL display designs.

Chapter 5

RESULTS

5.1 Power Dissipation Reduction

This section presents the results of three techniques for power reduction of AMEL displays. The first approach is to modify the HVNDMOS transistor breakdown voltage. This breakdown modification is a device level approach to improving the power dissipation of the AMEL display. The second approach is to increase the amount of parasitic capacitance in each pixel. Increasing the parasitic capacitance at the AMEL display model is a circuit parameter optimization approach. The final approach of further development of lower breakdown phosphors is also a device level approach.

The following sections describe both simulated and experimental results with respect to the AMEL display.

5.1.1 HVNDMOS Breakdown Reduction Technique

As a discussed in Section 3.2.6, as a result of the breakdown within the NDMOS transistor, current flows through the device even when the device is off. This unwanted current flow contributes to the sub-optimal performance of the device. The power dissipation for the current AMEL display is shown in Table 3. The power dissipation in the HVNDMOS is approximately 490 mW. This power dissipation is undesirable. This unwanted power dissipation is plotted with other device power dissipation during a

pixel's 'off' state in Fig. 40. The current operating point is shown in the figure at a breakdown of approximately 80 V at point A. Reducing the breakdown voltage from point A results in the phosphor breaking down and emitting light during the pixel's 'off' state. The phosphor emitting light is an undesirable effect of continuing to reduce the breakdown voltage and makes the AMEL display operate incorrectly. Conversely, increasing the HVNDMOS transistor's breakdown voltage will decrease the device power dissipation. Notice the current operating point results in the highest power dissipation possible without breaking down the phosphor and allowing the display to emit light. An obvious technique for decreasing the power dissipation is to increase the HVNDMOS breakdown voltage until the device ceases to break down during a pixel's off state.

Unfortunately, as discussed before, increasing the HVNDMOS transistor breakdown would come at the cost of trading off other desirable features. Redesigning the current device would come at a cost of lower yields and initial reliability problems. These engineering difficulties make other approaches to power reduction more desirable.

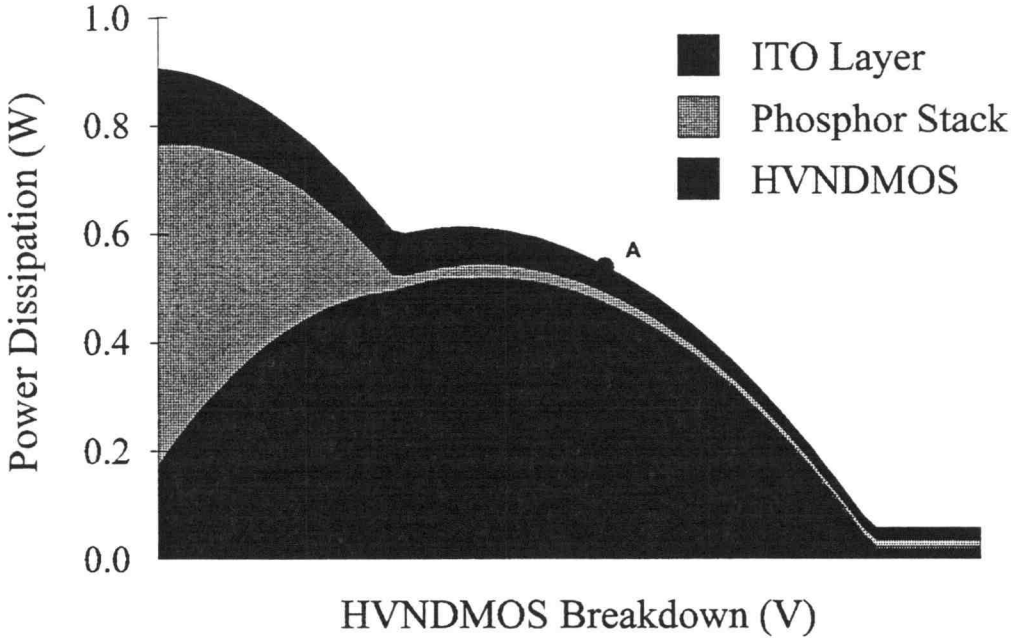


Figure 40 HVNDMOS breakdown voltage parameter sweep.

Increasing the breakdown of the HVNDMOS transistor to approximately 140 V will keep the HVNDMOS transistor from breaking down during the pixel's 'off' cycle. This reduces the HVNDMOS power dissipation to less than 20 mW during a pixel's 'off' cycle. This reduction in HVNDMOS power dissipation reduces the AMEL displays total power dissipation to approximately 50 mW. This very low power dissipation for the AMEL display's 'off' cycle is desirable.

5.1.2 Parasitic Reduction Technique

An important technique for power reduction was identified as a result of optimizing AMEL model parameters. In particular, the power reduction was characterized as a result of optimizing the total parasitic capacitance for the device during the AMEL display's 'off' state.[4] There is a potential for large power savings without the undesirable effects of changing the HVNDMOS transistor breakdown voltage. A parameter sweep of the total parasitic capacitance in the AMEL lumped

parameter circuit model for 'off' power dissipation is shown in Fig. 45. The total 'off' power dissipation is predicted to decrease as a result of increasing the total parasitic capacitance.

This parasitic capacitance technique is desirable for power reduction. Increasing the total parasitic capacitance within each pixel is possible without additional undesirable effects or trade-off's. In addition, the increased parasitic capacitance is short-circuited when the device is in its 'on' state. The short-circuited parasitic capacitance during the device's 'on' state is very important. If the parasitic capacitances are not short-circuited, they would contribute to an increased total power dissipation for the AMEL display during its 'on' state. The short circuit as a result of the HVNDMOS transistor driven 'on' is an important effect within the pixel structure that contributes to the feasibility of this power reduction technique. Without the short circuit effect, this technique for power reduction would be undesirable.

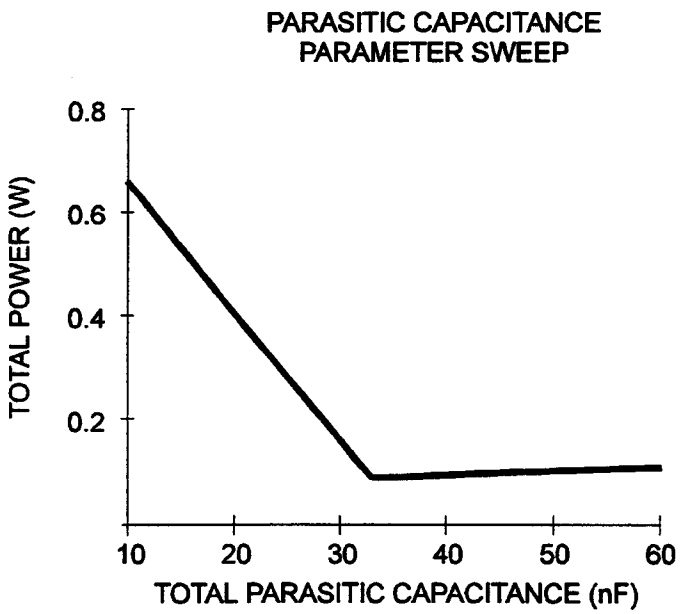


Figure 41 Parasitic parameter sweep for 'off' power dissipation.

A simplified AMEL device circuit model that is useful for discussing AMEL power reduction is shown in Fig. 42. While the AMEL display is driven 'off', the phosphor does not break down and emit light. In an attempt to characterize the parasitic capacitance trend shown in Fig. 41, the simplified circuit model is obtained by replacing the EL stack circuit model with a single capacitor. This accurately models the EL stack during the device's 'off' state with the assumption that the phosphor never reaches break down so that the Zener diodes modeling the phosphor's break down can be removed. Special care is used to verify the correct region of operation of the AMEL display before using the simplified circuit model. This simplified circuit model does not include the ITO layer resistance and, as a result, the power dissipation values from this circuit model do not correlate with that obtained from the AMEL lumped parameter circuit model. Thus, simplified circuit model is only used the discussion of power reduction through modification of the total parasitic capacitance. The ITO layer resistance is removed for this discussion because the only effect of the ITO layer during the device's 'off' state is a small voltage drop. All of the large resistances have been removed from the circuit diagram because they only have a small effect on the circuit and are primarily in the model for circuit convergence and to model the small leakage currents in the AMEL display.

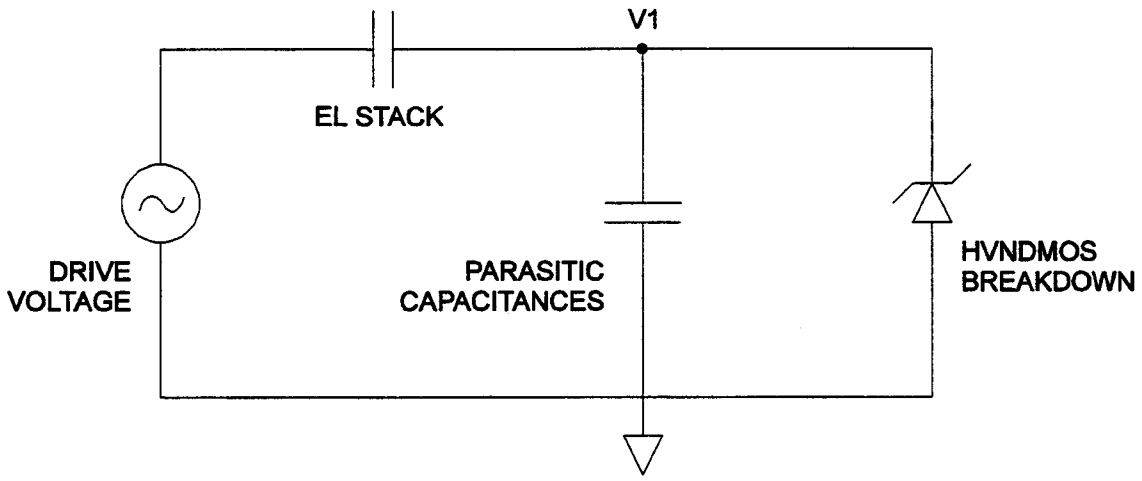


Figure 42 Simplified AMEL circuit model for power reduction discussion.

Circuit analysis of the simplified 'off' AMEL circuit model shown in Fig. 42 is straight forward. The EL stack capacitance and parasitic capacitance form a capacitive voltage divider at node V1. In order to minimize the 'off' power dissipation the HVNDMOS must not break down. The HVNDMOS transistor does not break down if the voltage at V1 does not exceed the HVNDMOS transistor's breakdown voltage.

The current total parasitic capacitance for the AMEL display is 13.5 nF, which corresponds with a parasitic capacitance of 40 fF per pixel. The simulation minimizes the total 'off' power dissipation by increasing the parasitic capacitance to 35 nF or higher for the AMEL display.

The circuit shown in Fig. 43 is developed to experimentally verify the parasitic behavior described above. The sole purpose of the test fixture is to vary the total parasitic capacitance of the device and to obtain total power dissipation measurements. Due to the nature of the AMEL device, it is impossible to connect additional parasitic capacitance into the AMEL display without redesigning the AMEL device layout. The

node V1 in Fig. 42 is buried within the AMEL device. To connect to this internal node, device fabrication modifications are needed. The circuit shown in Fig. 43 is used as an alternative way to test the viability of increasing parasitic capacitance in order to reduce 'off' power dissipation. This test fixture approximates the standard AMEL lumped parameter model without requiring modifications to the existing AMEL device. When using this test fixture, the AMEL device is driven 'on'. The parasitic capacitance and the Zener diode modeling the HVNDMOS transistor's breakdown are shorted by the HVNDMOS transistor. The test fixture is inserted between the input excitation voltage and the high voltage connection to the AMEL display. The resulting circuit resembles an AMEL display driven 'off'.

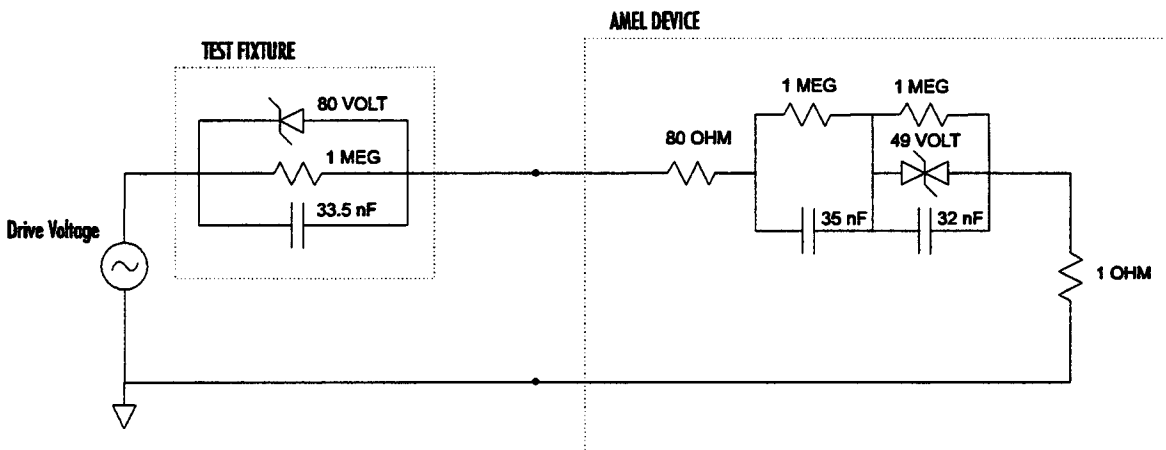


Figure 43 AMEL VGA-sized parasitic test circuit.

Experimental results of increasing the parasitic capacitance as a means of reducing the 'off' power dissipation of an AMEL device are shown in Fig. 44. These experimental results are obtained using an EL dot sample and scaled for the entire display. The experimental results match the predicted results shown in Fig. 41. This

experiment proves that increasing the total parasitic capacitance does indeed decrease the total 'off' power dissipation in the AMEL display.

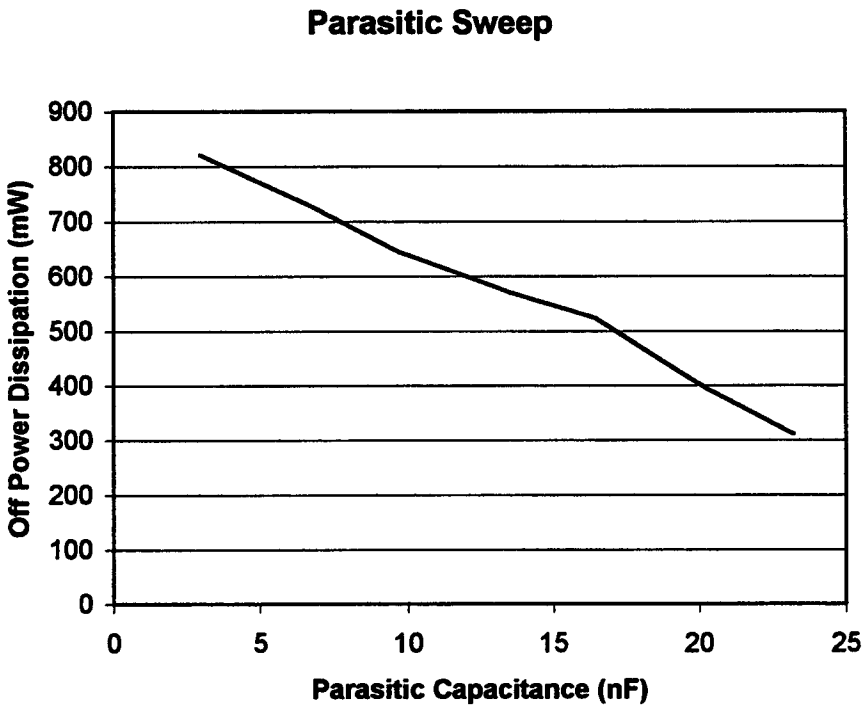


Figure 44 Experimental parasitic capacitance parameter sweep.

The pixel layout contains many possible locations where additional capacitance may be added. No physical location in the layout has yet been determined as the ideal location for the addition of parasitic capacitance.

5.1.3 PHOSPHOR DEVELOPMENT REDUCTION TECHNIQUE

When analyzing an AMEL device there is an obvious drawback to electroluminescent technology. The phosphor stack in the EL device requires large excitation voltages in order to break down the phosphor and emit light. Large excitation

voltages cause large power dissipation from many sources in the AMEL display and driving circuitry. Since AMEL devices are targeting portable display solutions, the AMEL display power source will, most likely, be portable. As a result of the portable power source, large AC excitation waveforms are generated from portable DC power sources. This voltage magnitude and wave shape transform results in large power dissipation. In addition, the AMEL display dissipates large amounts of power in the ITO layer, the EL stack, and the HVNDMOS transistor. A large percentage of the power dissipated is reactive power. Additional power is dissipated during the power recovery process. The standard AMEL display dissipates on the order of 5 W during standard operation.

This large power dissipation due to large excitation voltages makes reducing the phosphor breakdown desirable. Unfortunately, reducing the phosphor breakdown voltage while maintaining a high level of brightness is exceedingly difficult. Research is ongoing in this area of phosphor development.

Low breakdown voltage phosphor has been developed. EL stack breakdown voltages of approximately 60 V are common. This low voltage stack compares to a standard phosphor with an EL stack breakdown of approximately 80 V. Reducing the phosphor breakdown voltage will reduce the display's total power dissipation while maintaining a comparable amount of light output and light output quality.

A low voltage phosphor under development has exhibited EL stack breakdown voltages of 60 volts. This AMEL display requires an excitation magnitude of approximately 80 V as compared to 120 V when using a standard phosphor. This

reduction in voltage results in a total 'on' power reduction from 950 mW with a standard phosphor to 450 mW with the low voltage phosphor. The total 'off' power dissipation is reduced from 500 mW with a standard phosphor to 30 mW with the low voltage phosphor. Unfortunately, the total light output and light output quality is reduced when using the low voltage phosphor as compared to the standard phosphor. This degradation in output quality is a result of the difficulty of developing a high quality low voltage phosphor.

5.2 Excitation Waveform

As discussed in Section 3.2.1, the excitation waveform is an important part of AMEL display design. A comparison of stepped sinusoidal and triangular waveforms is shown in Fig. 45. The comparison shows that using an excitation wave with a small number of steps is inefficient. As the number of steps in the excitation is increased the power dissipation decreases asymptotically towards the power dissipation for the non-stepped waveform. In addition, Fig. 45 shows that triangular excitation average power dissipation is slightly less than that for the sinusoidal excitation. However, the average power dissipation in the phosphor is reduced in addition to the decrease in average power dissipation of the device. Therefore, using a triangular excitation in place of a sinusoidal excitation is not an effective means of achieving a power reduction.

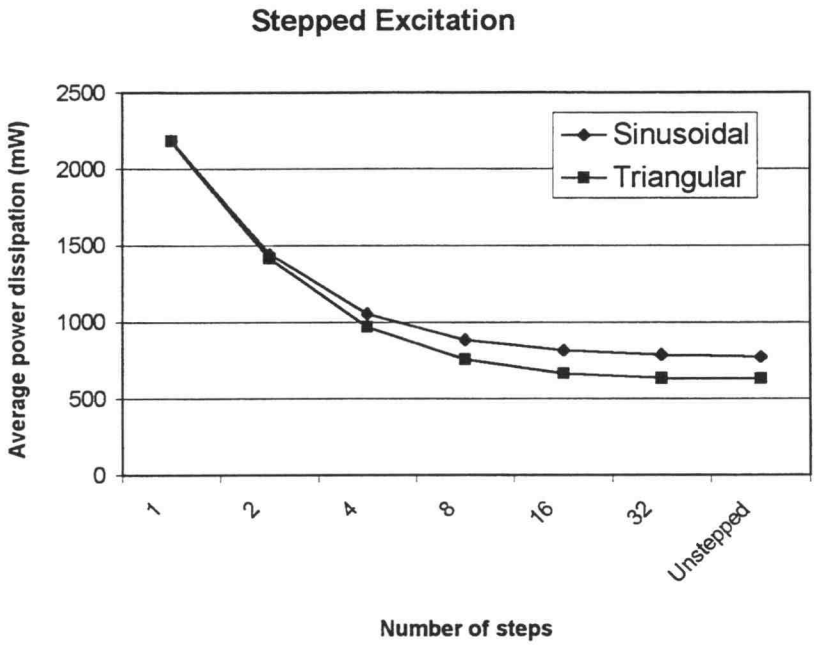


Figure 45 Stepped excitation waveform comparison.

The sinusoidal, triangular, and efficient two-step excitation waveforms are compared in Table 4 and Table 5. The triangular excitation waveform exhibits the lowest average power dissipation. The efficient two-step waveform exhibits the highest average power dissipation. The actual amount of power dissipated from each of the excitation waveforms in itself does not help select the desired excitation waveform; this requires comparing the excitation waveforms with respect to their ability to supply power to the EL stack.

EXCITATION WAVEFORM	AVERAGE POWER (mW)
Sinusoidal	776
Triangular	631
Efficient Two-Step	928

Table 4 Excitation waveform average power comparison.

Table 5 compares the efficiency of each excitation waveform. The waveform efficiency is defined as the amount of power dissipated in the EL stack divided by the total power dissipated in the AMEL display. This comparison shows the sinusoidal excitation waveform to be the most desirable drive waveform for the AMEL display. Unfortunately, generation of a sinusoidal waveform for use with the AMEL device is hardware intensive and inefficient. The triangular excitation waveform suffers from the same waveform generation problem.

EXCITATION WAVEFORM	EFFICIENCY (%)
Sinusoidal	84.73%
Triangular	84.03%
Efficient Two-Step	81.19%

Table 5 Excitation waveform efficiency comparison.

The efficient two-step waveform has an efficiency comparable to that of the sinusoidal or triangular waveform listed in Table 5. The efficient two-step waveform is much easier and efficient to generate than the sinusoidal and triangular waveforms. Without additional design work, the waveform generation hardware for the efficient two-step waveform will recover reactive power dissipated in the AMEL display. Thus, efficient two-step excitation waveform is the desired waveform for portable HMD applications because of its efficient operation and power recovery advantages in portable systems.

5.3 Summary

The power reduction techniques are summarized in Table 6. The power reduction techniques described in this chapter are listed and compared for 'on', 'off', and average power dissipation.

POWER REDUCTION TECHNIQUE	ORIGINAL (mW)	ENHANCED (mW)	SAVINGS (%)
ON POWER			
HVNDMOS Breakdown	982	982	0%
Parasitic Optimization	982	982	0%
Low Voltage Phosphor	982	450	54%
OFF POWER			
HVNDMOS Breakdown	570	56	90%
Parasitic Optimization	570	87	85%
Low Voltage Phosphor	570	30	95%
AVERAGE POWER			
HVNDMOS Breakdown	776	519	33%
Parasitic Optimization	776	534.5	31%
Low Voltage Phosphor	776	240	69%

Table 6 Power reduction summary.

When comparing power reduction techniques, it appears that using a low voltage phosphor is the most desirable technique for reducing total power dissipation. Unfortunately, the current low voltage phosphor suffers from reduced light quality and light output and is still in development and unavailable for manufacturing. Development of low voltage phosphors is ongoing and the future availability of high quality low voltage phosphors is unknown. When high quality low voltage phosphors become

available, implementation into AMEL displays will contribute to additional power dissipation savings.

Increasing the HVNDMOS breakdown voltage is also a desirable approach to power reduction, although the trade-off's associated with modification of the HVNDMOS breakdown voltage makes other approaches to power reduction more desirable.

Finally, the inclusion of additional parasitic capacitance is a desirable technique for power reduction. This parasitic capacitance optimization has the potential for large power savings without associated undesirable effects inherent in changing the HVNDMOS transistor breakdown voltage or the unknown timeline of a high quality, low voltage phosphor. In addition the parasitic capacitance optimization technique is appropriate for future AMEL display designs. As AMEL pixel pitch increases, the need for parasitic capacitance optimization will increase, due to a decrease in HVNDMOS breakdown voltage as the pixel pitch decreases. In essence, parasitic capacitance optimization circumvents the need to increase the HVNDMOS transistor breakdown voltage. With these advantages, the parasitic capacitance optimization technique is the most desirable short-term technique for reducing power in the AMEL device.

Chapter 6

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

6.1 Conclusions

An AMEL lumped parameter simulation model has been developed and has proved to play an important role in the development of reliable, low power AMEL display devices. The AMEL lumped parameter model successfully models the AMEL device behavior.

An AMEL design tool software package has been developed. The AMEL design tool combines the AMEL lumped parameter simulation model with a user-friendly interface designed to explore and investigate AMEL display behavior. Investigation, through the use of this intuitive software package, has contributed to the development three main power reduction techniques: increasing the HVNDMOS transistor breakdown voltage, parasitic capacitance optimization, and development of a low voltage phosphor.

The parasitic capacitance optimization approach has the potential for large power savings without associated undesirable effects inherent in changing the HVNDMOS transistor breakdown voltage or the need to develop a high quality, low voltage phosphor. Parasitic capacitance optimization is advocated as the power reduction technique of choice for current AMEL display devices.

6.2 Recommendations for Future Work

There are a number of areas ripe for continued research in the area of AMEL display devices, as listed below.

- Pixel layout optimization. Research should focus on the HVNDMOS transistor and its layout with respect to the current pixel design. Display improvements are possible through continued pixel research, primarily with regard to the HVNDMOS transistor. Additional research in this area may stimulate new pixel designs and AMEL display improvements.

- Continued phosphor development. Improvements in phosphor quality and efficiency drive the electroluminescent industry.

- Development and characterization of waveform generation hardware. This development would focus on efficient waveform generation and power recovery techniques.

REFERENCES

1. R. Khormaei, Ph. D. Thesis, Oregon State University, 1995. p. 16, 17, 25, 33-35.

2. R. Khormie, K. Ping, M. Rhodes, B. Aichitson, C. N. King, T. Keyser, G. Becker, D. Kagey, M. Spitzer, "A 1280 x 1024 Active-Matrix EL Display.", Society for Information Display, Digest of Technical Papers, 1995.

3. M. Aberg, Ph. D. Thesis, Helsinki University of Technology, 1993. p. 6.

4. Private communications with Larry Arbuthnot, Planar Systems, Inc., Nov. 1995.

5. Y. A. Ono, Electroluminescent Displays, World Scientific, Singapore, 1995. p. 112-116.

6. Private communications with Terrance Larsson, Planar Systems, Inc., Sept. 1996.

7. A. Ipri, "Improved Active Matrix Electroluminescent Display Using an Analog Drive Method.", 1997.

8. Private communications with Eric Dickie and Dick Coovert, Planar Systems, Inc., Sept. 1996.

9. J. Choma, "Electrical Networks: Theory and Anaylsis.", 1985. p. 197-214.

10. N. Weste, K. Eshraghian, Principles of CMOS VLSI Design, 1993.

11. J. F. Wager, A. A. Douglas, "Electrical Characterization and Modeling of ACTFEL Devices.", Oregon State University, 1992.

12. Private communications with A. Ipri and R. Stewart, David Sarnoff Research Center, Inc., Jan. 1996.

13. Planar Systems, Inc. "Active Matrix Electroluminescent Preliminary Description", Internal Document, 1994.

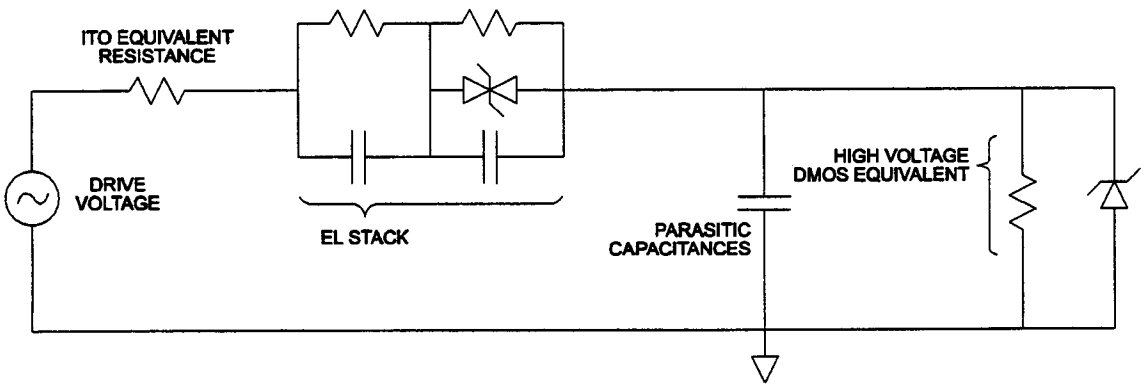
14. A. Douglas, T. Flegal, "An Improved Performance TEL VGA Gray-Scale Display", Society for Information Display, Digest of Technical Papers, 1995.

15. David Sarnoff Research Center, "Analog AMEL Display Feasibility Study.", 1995.

APPENDICES

APPENDIX A: AMEL LUMPED PARAMETER SPICE MODEL

DEVICE MODEL



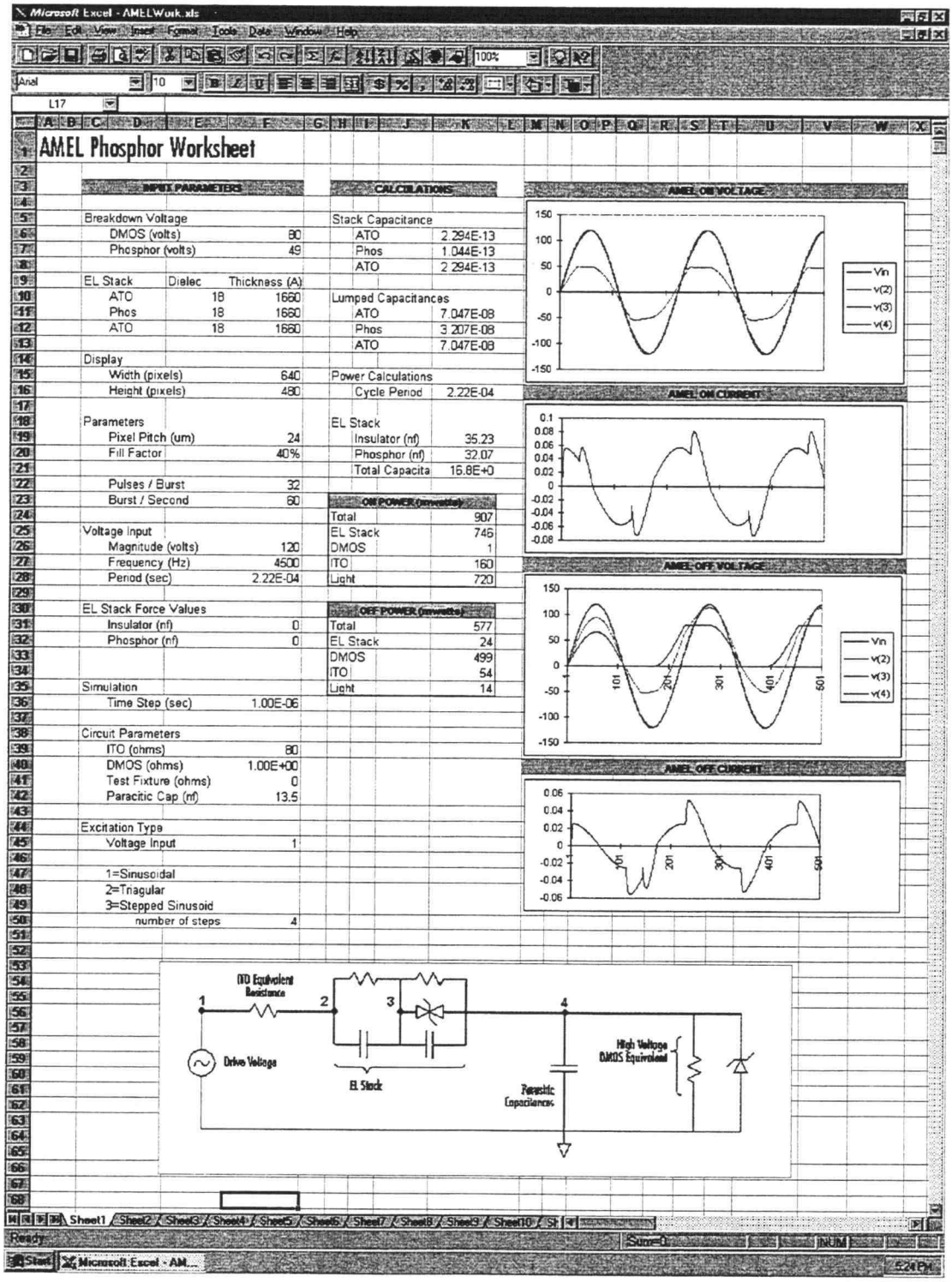
PSPICE SOURCE CODE

```
AMEL 640x480 Device Model For Standard Yellow Phosphor

cpara   70 0    13.50n                  # Parasitic capacitances
ci      70 20   35.00n                  # Insulator capacitance
cp      20 10   32.00n                  # Phosphor capacitance
ri      70 20   100meg                  # SPICE addition for convergence
rp      20 10   100meg                  # SPICE addition for convergence
dzp1    20 60   phosbreak               # Phosphor breakdown voltage
dzp2    10 60   dmosbreak               # DMOS breakdown voltage
dmosbreak 0  70  dzene2                 # High voltage DMOS breakdown
rdmosres  70  0  1                      # High voltage DMOS resistance
rrow    10 100 180                      # ITO Layer
vrow    100 0  sin(0 120 4.5k 200u)     # Excitation Voltage

.model phosbreak d bv=49
.model dmosbreak d bv=80
.tran  1us 500u
```

APPENDIX B: AMEL TRANSIENT SIMULATION SPREADSHEET



APPENDIX C: AMEL TRANSIENT SIMULATION ENGINE

```
//=============================================================================//
//  AMEL_High_Speed_Simulation                                        JAN '97  //
//  Programming By Douglas Beck                                                //
//=============================================================================//

//===----------------------- Simulation Parameters -----------------------===///

  int   phosbreak=49;              //  Phosphor Breakdown Voltage          //
  int   dmosbreak=80;              //  High Voltage DMOS Breakdown         //
  float dmosres=1e6;               //  High Voltage DMOS Resistance        //
  float vinmax=120;                //  Excitation Voltage Magnitude        //
  float freq  =4500;               //  Excitation Voltage Frequency        //
  float insulator=35e-9;           //  Total Insulator Capacitance         //
  float phosphor =32e-9;           //  Total Phosphor  Capacitance         //
  float paracitic=13.5e-9;         //  Total Paracitic Capacitance Total   //

//===---------------------- Precalculation Parameters ----------------------===///

  int   ITOres=180;                //  ITO Resistance                      //
  float T=1e-6;                    //  Time Step                           //
  float vc1=0,vc2=0,vc3=0;         //  Capacitor Companion Model Voltages  //
  float vcr1=T/insulator;          //  Capacitor Companion Model Resistance//
  float vcr2=T/phosphor;           //  Capacitor Companion Model Resistance//
  float vcr3=T/paracitic;          //  Capacitor Companion Model Resistance//
  int   iteration=0;               //  Iteration Count                     //
  float vin,v2,v3,c4,i1,i2;        //  Variable Declaration                //

//===----------------------- Main Simulation Loop -------------------------===///

  while(iteration<500)
  {
    vin=sin((2*3.1415)*((float)              // Input Sinusoidal Waveform  //
        (iteration*T)*freq))*vinmax;
    i1=(vin-vc1-vc2-vc3-((vc3*vcr3)/             // Current and voltage    //
       (vcr3+dmosres)))/(ITOres+vcr1+vcr2+vcr3   // definitions with no    //
       +((vcr3*vcr3)/(vcr3+dmosres)));            // Zener Diode exceeding  //
    i2=((vc3+(i1*vcr3))/(vcr3+dmosres));         // their breakdown voltage//
    v2=vin-ITOres*i1);
    v3=dmosres*i2+(vc2+i1*vcr2);
    v4=dmosres*i2;

    if(v4>dmosbreak)                             // Current and voltage    //
    { vc3=dmosbreak-vcr3*(i1-i2);                // definitions when DMOS  //
      v4=dmosbreak;                              // has exceeded it's      //
      i1=(vin-vc1-vc2-dmosbreak)/(ITOres+vcr1+vcr2);    // breakdown voltage//
      v2=vin-(ITOres*i1);
      v3=dmosbreak+(vc2+i1*vcr2); }

    if(v4<0)                                 // Current and voltage        //
    { vc3=-vcr3*(i1-i2);                     // definitions when DMOS      //
      v4=0;                                  // forward biased             //
      i1=(vin-vc1-vc2)/(ITOres+vcr1+vcr2);
      v2=vin-(ITOres*i1);
       v3=vc2+i1*vcr2; }

    vc1=(vc1+vcr1*i1);  vc2=(vc2+vcr2*i1); vc3=(vc3+vcr3*(i1-i2));
    if((vc2+ii*vcr2)>phosbreak)  vc2= phosbreak-vcr2*ii;
    if((vc2+ii*vcr2)<-phosbreak) vc2=-phosbreak+vcr2*ii;
    iteration++;
  }
```