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Oversampled delta-sigma modulation is one of the widely used A/D conversion techniques for narrow bandwidth signals. In this study several new lowpass and bandpass delta-sigma modulator architectures as well as novel pseudo-N-path integrators that can be used in implementing these architectures are proposed.

By using multiplexing techniques the new lowpass delta-sigma modulator architectures exchange higher clock rates with hardware complexity. For a given oversampling ratio (*OSR*), the multiplexed first-order delta-sigma modulator achieves a higher resolution. Guaranteed stability is a very desirable feature of these structures. The multi-loop delta-sigma modulator architecture similarly reduces the number of integrators needed to achieve high-resolution conversion for a given *OSR*. To ensure stability a quantizer with (N+1) bits must be used, where N is the number of loops, or in other words, the order of the delta-sigma modulator. Digital correction or randomizing techniques can be used to eliminate the performance reduction due to digital-to-analog (D/A) converter nonlinearity error [59], [64].

Bandpass delta-sigma modulators are useful for applications such as AM radio receivers, spectrum analyzers, and digital wireless systems. Using $z \rightarrow -z^N$ or $z \rightarrow z^N$ mapping, a low pass delta-sigma modulator can be transformed to a bandpass one. One

of the methods to implement the loop filters in bandpass delta-sigma modulators is to use Pseudo-N-Path (PNP) switched-capacitor (SC) integrators. The advantage is that the center frequency occurs exactly at an integer division of the sampling frequency because of the number of physical paths. To achieve maximum resolution, integrators that do not suffer from clock feedthrough peaks are needed. The proposed differential and single-ended novel PNP integrators address this problem [76]. To keep the opamp specifications less stringent while achieving high resolution, these PNP integrators have been further improved with gain compensation techniques [53].

Novel Switched-Capacitor Circuits for Delta-Sigma Modulators

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Ayse G. Yesilyurt, Author

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This thesis is dedicated to my father, Mehmet Zeki Begisi, who passed away in September 1995, before seeing a "doctor" in the family.

Novel Switched-Capacitor Circuits for Delta-Sigma Modulators

1. INTRODUCTION

Digital circuits have been extensively used in the last fifteen years in signal processing circuits due to their superior performances in noisy environments. The trend in circuit design is to do signal processing in the digital domain as much as possible. However, most of the time the input signals are available only in analog forms. One solution to this problem is designing a transducer interface to output digital signals. Because this option is in most cases very costly or practically infeasible for high accuracy applications, another solution became popular, which is to convert the analog signals to digital signals before digital signal processing.

There are many techniques to perform analog-to-digital (A/D) conversion. Some of these techniques, such as flash and pipelined A/D conversion trade off accuracy for speed. On the other end of the scale, an algorithmic A/D converter produces very accurate results compromising the speed of conversion. Another important consideration in A/D conversion is to design systems with minimal analog circuitry which is the primary source of performance degradation. It is also important to design systems that can tolerate VLSI technology variations and component values. Delta-sigma A/D conversion technique provides high accuracy at moderate conversion speeds with high tolerance to technological imperfections and component values. The technique suits best the signals with limited bandwidth. In the last decade, audio applications of delta-sigma A/D and D/A converters became very popular particularly in Compact Disk (CD) systems. Since a relatively larger and more complex portion of delta-sigma modulators are digital circuits,

the integrated circuits (IC) are fabricated in CMOS technology, which is optimized for digital circuits. A few additional masks are added to this technology to implement components such as capacitors that analog portion of the circuits need. The prototype ICs of this study are fabricated on 1.2 μm, double-poly, double-metal, n-well ORBIT process.

Most studies published on delta-sigma converters since the introduction of this technique focused on lowpass applications [4]-[42]. There have been some work on narrowband bandpass applications in the last decade [43]-[57]. Bandpass delta-sigma modulators are useful for applications such as AM radio receivers, spectrum analyzers, digital wireless systems etc. In this study, along with several novel lowpass delta-sigma modulator structures [59], [64], narrowband bandpass delta-sigma modulator structures [52] have been proposed. All of these structures require pseudo-N-path (PNP) integrators that do not suffer from clock feedthrough peaks as most available ones in the literature do [67]. As a solution, several novel PNP integrators that do not have in-band noise-peaks problem have been introduced. To achieve highly accurate bandpass delta-sigma modulators with less stringent opamp specifications, gain compensated PNP integrators have been proposed [52].

Chapter 2 is a brief introduction to basics of oversampling technique, delta-sigma noise shaping loop, and delta-sigma modulators . In Chapter 3, two novel delta-sigma modulator architectures for lowpass applications, multi-feedback and multi-loop delta-sigma modulators are discussed. In Chapter 4, the PNP integrators, that are necessary for the architectures presented in Chapter 3 and 5 are introduced. Noise performance of the PNP integrators are examined in the context of various bandpass filters. In Chapter 5, the system-level and circuit-level requirements and implementation details of two different 6^{th} order bandpass delta-sigma modulators with pseudo-2-path integrators are included. The lowpass-to-bandpass mapping of delta-sigma conversion and design issues along with gain and offset compensated versions of the PNP integrators are also discussed in this chapter. The notch loop, a test vehicle that is designed to prove the usefulness of PNP integrators

is examined in Chapter 6. The measurement results obtained from the silicon test chips are also presented in this chapter. Chapter 7 includes conclusions drawn from the simulations and experiments, and suggestions for future work.

2. DELTA-SIGMA A/D CONVERSION

2.1. Basic Architecture of Digital Signal Processing Systems

Implementation of very complex digital signal processors that can provide higher resolution and programmability became economical with VLSI technology improvements that decrease the achievable minimum geometry, and hence the chip area. The trend has been to do as much of the signal processing as possible digitally. This, in turn, generated the need to accurately convert signals, that exist in the world in their analog form, back and forth.

Fig. 2.1 shows main blocks of a general digital signal processing architecture. An antialiasing filter, a Sample-and-Hold (S/H) circuit, an Analog-to-Digital (A/D) converter make the data acquisition unit. Digitally processed data is then converted back to analog form, sampled and held, and filtered by the reconstruction filter. Sampling is a necessity for digital processing of analog signals. To avoid loss of recovery of original data, analog signals need to be sampled at frequencies (f_S) at least twice as much as their bandwidth, f_B (Nyquist rate). The anti-aliasing filter eliminates aliasing distortion by band-limiting the signal spectrum. The S/H circuit converts the band-limited analog signal to a discrete-time and continuous-amplitude signal that, is, then, converted to a discrete-time and discrete-amplitude, i.e. a digital signal by the A/D converter. After the digital signal processing, it is necessary to return this digital output to an analog form to interface with the outside world. The Digital-to-Analog (D/A) block converts its digital input to a discrete-time and discrete-amplitude one. The following S/H block samples this signal and holds it for a sampling period. This operation distorts the output signal spectrum depending on its order (sinc, sinc^2 etc.). To obtain a smooth analog signal and to eliminate the distortion imposed by the S/H block an analog reconstruction filter is used.

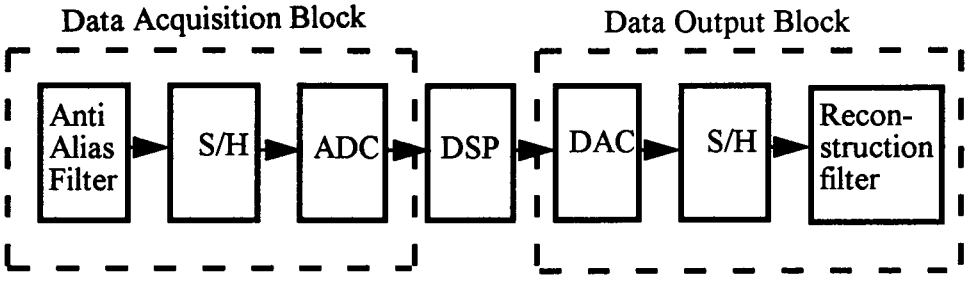


Fig. 2.1. Block diagram of a general digital signal processing architecture.

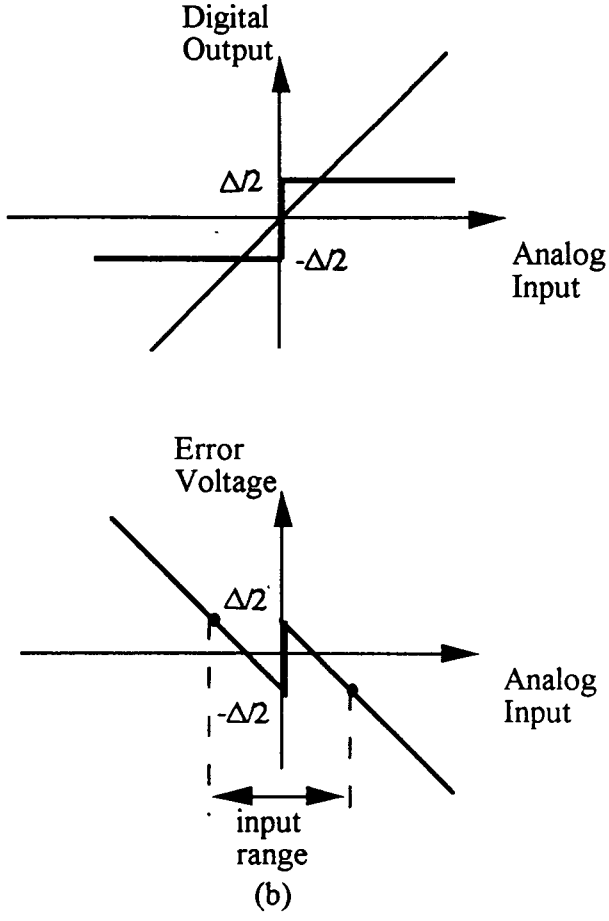


Fig. 2.2. (a) Two level quantizer. (b) Error voltage for the two level quantizer.

2.2. Nyquist and Oversampled A/D Converters

The major contributor of noise in an A/D converter is the quantizer. The quantization error can be modeled as a uniformly distributed random variable varying between -Δ/2 and Δ/2 (Fig. 2.2a). The mean power of the quantization noise, N_Q^2, can be calculated as $\Delta^2/12$. One way of reducing this power is using a finer quantizer, i.e. for the same input range a smaller quantizer step, Δ (Fig. 2.2b), which is the method used in Nyquist-rate A/D converters.

Another method is oversampling the signal, as it is done in oversampled A/D converters. Sampling the signal at rates higher than Nyquist rate, then filtering out the undesired band effectively reduces the quantization noise power in the band of interest (Fig. 2.3a and 2.3b). The ratio of the power of the in-band noise with oversampling to the power of noise without oversampling is equal to $1/(OSR)$, where OSR is oversampling ratio. The same performance improvement can also be provided by using a quantizer with a $1/(OSR)^{1/2}$ smaller step. This means that it is possible to trade complexity (more levels in quantizer) for speed (higher clock rates).

Parallel (flash), coarse (2-step), subranging, pipelined, successive approximation, cyclic, algorithmic A/D are examples of Nyquist-rate A/D converters. All these methods put stringent demands on the analog circuitry of both the converters and the surrounding circuitry. Designing narrow band antialiasing filters with minimum phase distortion, or S/H circuits that are fast, as accurate as the overall system, linear, and capable of driving large capacitance is very difficult. Accurate comparisons, sampling and holding of signals throughout the system, linearity, subtraction or addition, multiplication, amplification, matching of capacitors, resistors or transistors which are not readily available in digital CMOS processes might be needed to achieve the desired resolution for a given Nyquist-rate converter. Although they can provide fast conversions, the desired accuracy may

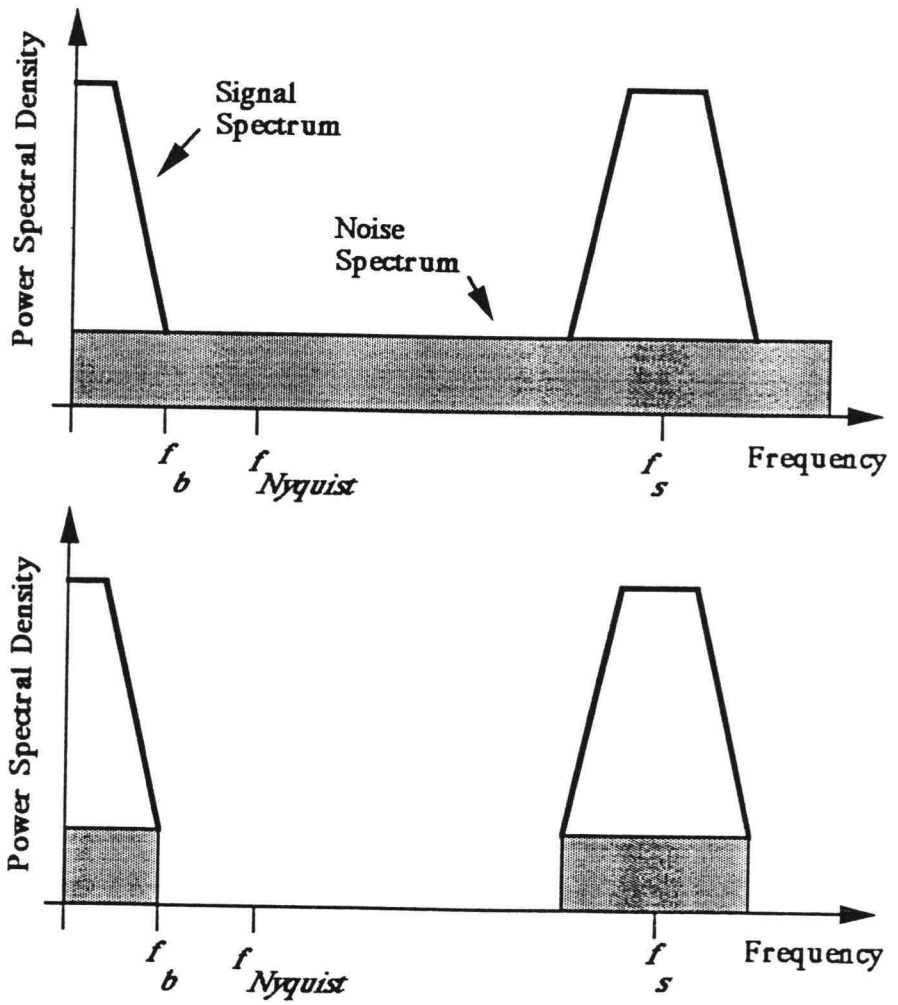


Fig. 2.3. Signal and noise power after oversampling and lowpass filtering.

come at the expense of analog circuit solutions that consume precious silicon-area and power, or may be only achieved by expensive trimming or self-calibration.

Oversampled A/D converters, on the other hand, can be designed with much relaxed analog circuitry requirements. Increased sampling frequency eases the demands on the anti-aliasing filter to a great extend because the transition band can be much wider than of the Nyquist-rate converter. This reduces the order of the analog filter and makes it less complex and less prone to phase distortion. Sampling is readily achieved by the quantizing circuitry, there is no need for a separate S/H block. Another significant difference that makes the analog circuitry a lot less complex is the reduced resolution of the quantizer in oversampled A/D converters. Even a one-bit quantizer (one comparator only!) can be used provided that it is in a feedback loop with a filter, and followed by digital circuitry that can construct a more precise sample at the Nyquist rate. All these reductions in analog circuitry increase the complexity of the following digital circuitry. However, as mentioned before, VLSI technologies lend themselves better to design cheap, fast and complex digital circuits than to handle difficult analog circuit requirements. Although the amount of digital circuitry, and consequently its adverse affects such as ground bouncing are increased, due to less stringent requirements, analog circuitry of the oversampled data converters is more robust in compared to precision requiring Nyquist-rate converters.

There are basically two kinds of architectures of oversampled A/D converters: *Predictive* and *noise shaping*. The 1st order delta modulator (Fig. 2.4) is an example of the former architecture. It consists of a single-bit quantizer whose input is the difference between the signal and its predicted estimate, in other words, averaged version of quantizer output. This technique reduces the quantizer error due to the reduced step size of the quantizer, which needs to handle a much smaller signal range [1]. However, there

are two serious disadvantages of this architecture: accumulation of errors due to circuit imperfections and non-idealities, and the quantizer's inability to catch up due to small step sizes in case the input changes rapidly (slope overloading). Overcoming these problems requires more complex circuitry [2].

A 1st order delta-sigma modulator [3] is an example of the noise shaping oversampled modulators (Fig. 2.5). The integrator in the loop precedes the quantizer unlike the 1st order delta modulator. This arrangement allows the signal spectrum to be remained relatively unchanged, although the quantization noise spectrum is shaped and removed from the frequencies where the signal band is. In addition, this architecture does not suffer from slope overloading problem with rapidly changing inputs.

A digital lowpass filter, *the decimation filter*, follows the modulator to remove the quantization noise which is concentrated in higher frequencies, to recover the signal, and to lower the rate of oversampling (pp.18-23 of [4]). Fig. 2.6 shows the filter response. Although removal of quantization noise spectrum does not require a very sharp filter response, removal of out-of-band portion of the signal to avoid aliasing usually does. To avoid building filters at high oversampling rates, decimation is usually done in two stages. Removal of quantization noise occurs at the first stage operating at higher frequencies. Attenuation of out-of-band components of the signal takes place in a lowpass filter preceding an accumulate-and-dump circuit that samples down the signal in the intermediate frequency to its Nyquist rate. For the first stage decimator, the transfer function of

$$H(e^{j\omega\tau}) = \left[\frac{sinc(\pi f N\tau)}{sinc(\pi f\tau)} \right]^{(L+1)} \qquad (2.1)$$

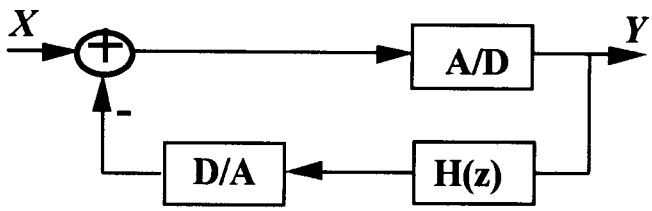


Fig. 2.4. 1st order delta modulator.

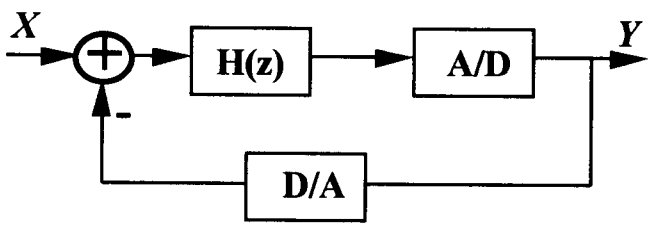


Fig. 2.5. 1st order delta-sigma modulator.

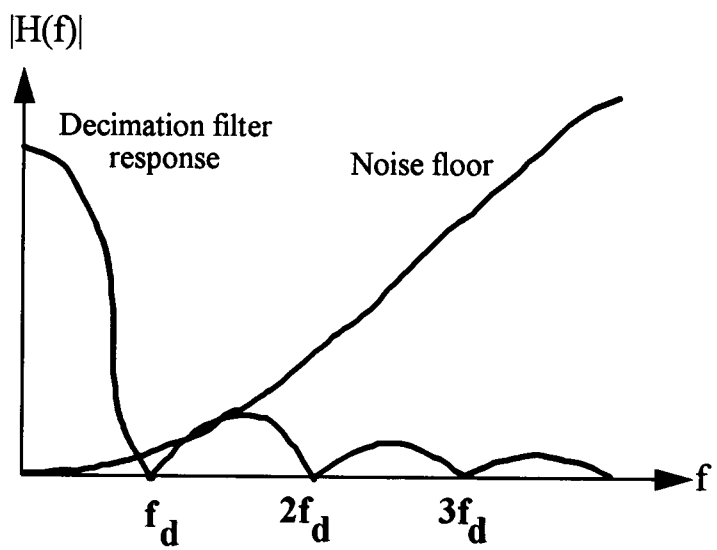


Fig. 2.6. Decimation filter response.

is found to be most appropriate, where $N = f_S / f_D$, f_D is the intermediate decimation frequency, f_S is the sampling frequency, and L is the order of the delta-sigma modulator. Due to the shape of the sinc filter response, some of the quantization noise does remain in the final signal spectrum and reduces the Signal-to-Noise Ratio (*SNR*), in other words, accuracy of the overall system. This reduction increases as the intermediate frequency is lower than four times the Nyquist rate. It is also observed that lower intermediate frequencies increases the droop of the frequency response of the filter at the edge of the signal band. Droops over 3 dB are more difficult to compensate for. Intermediate frequencies of four times the Nyquist rate and sinc^K decimation is convenient for many delta-sigma applications. A detailed analysis of decimators can be found in the references [4] and [5]. Decimation for bandpass delta-sigma converters are discussed briefly in Section 2.6.1.

2.3. Noise Shaping Oversampled A/D Converters

As explained in Section 2.1, noise shaping oversampled converters not only take advantage of oversampling to reduce the quantization noise, but also shape its spectrum to minimize its power in the signal band. To achieve a similar performance, they require less complex circuitry than predictive converters, since they do not suffer from many of the disadvantages that they do. Therefore, delta-sigma converters became very popular in the last decade [6]-[11]. There have been many studies on system analysis, architecture, stability, decimation and design issues of noise shaping oversampled A/D converters in literature [4]-[42].

2.4. Signal and Quantization Noise Transfer Functions

In delta-sigma conversion, the quantizer is placed in a "delta-sigma loop", where the input signal of the quantizer is obtained by first calculating the difference, "*delta*", of the present input and the delayed output, then, passing it through a filter, "*sigma*". The loop

filter is chosen to shape the quantization noise to minimize its power in the band of interest, and, on the other hand, to have almost no effect on the signal. Fig. 2.7 shows a delta-sigma noise shaping loop, where $x(n)$ represents the input of the delta-sigma loop, $u(n)$ is the input of the quantizer, $e(n)$ is the quantization error of the nth sample, and $y(n)$ is the output of the delta-sigma loop. In other words, the system is assumed to be linear although it has a grossly non-linear component, the quantizer. This assumption holds as long as the correlation of the quantization error and the input signal remains small, i.e. for "busy" input signals. The system equation in the z-domain can be written as

$$= \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) = H_s(z)X(z) + H_e(z)E(z) \tag{2.2}$$

where

$$H_s(z) = \frac{H(z)}{1+H(z)} \tag{2.3}$$

and

$$H_e(z) = \frac{1}{1+H(z)} \tag{2.4}$$

Let us assume $H(z)$ is a lowpass filter, and the input signal is a lowpass signal. Then, the signal transfer function will be almost equal to 1 at low frequencies, while the noise transfer function is a highpass one. This implies that the input signal leaves the delta-sigma loop unchanged, while the quantization noise is removed from the lowpass band, (or, in other words, "shaped") dramatically improving the *SNR*.

For the 1-bit quantizer case, the maximum *SNR* of a lowpass delta-sigma system [12] can be given as

$$SNR \text{ (in dB)} = 3n(2L+1) - 10\log \frac{2\pi^{2L}}{3(2L+1)} \tag{2.5}$$

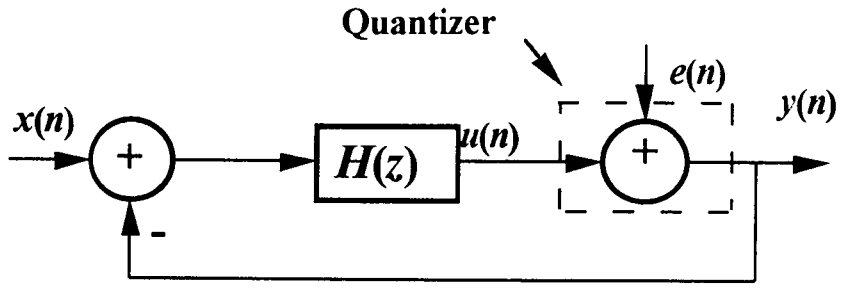


Fig. 2.7. Delta-sigma noise shaping loop.

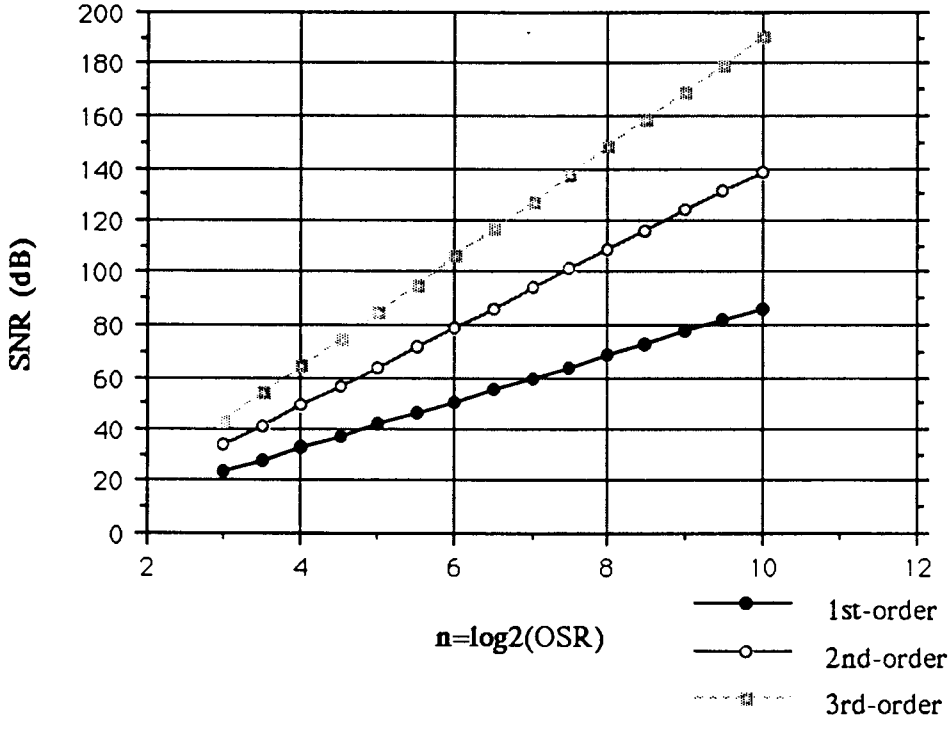


Fig. 2.8. SNR performances of 1st, 2nd, and 3rd order delta-sigma loops.

where L is the order of the loop filter, i.e. $H(z) = \frac{1}{(1-z^{-1})^L}$ and $n = log_2(OSR)$ where L is the order of the loop filter, i.e. $H(z) =$ and $n = \log_2(OSR)$. Fig. 2.8 shows the *SNR* performances of 1st, 2nd, 3rd order delta-sigma loops predicted from (2.5). It can be seen that for each doubling of the sampling rate, an additional $(L + 0.5)$-bits resolution can be achieved. Although the results look very promising, some aspects of the analysis are incomplete even on a theoretical level beyond the impact of circuit non-idealities. For example, this analysis does not address the question of how to choose the loop filter without destabilizing the delta-sigma loop. The realizability of the filter and the stability of the delta-sigma loop are two important concepts. The realizability is ensured by $H_n(\infty) = 1$. However, there are no proven criteria for all cases guaranteeing the stability of the loop, but rather only rules-of-thumb [13]-[15]. One of them is to choose the noise transfer function such that $|H_n(e^{jw})| < 2$ [16]. Without a reliable criterion, the best approach is to simulate the loop with the selected filter extensively, and try to detect signs of instability.

2.5. Architectures for Low-Pass Noise-Shaping Oversampled A/D Converters

Since the first introduction of delta-sigma converters, many architectures have been proposed. They differ in their achievable resolution (*SNR*) for a given sampling rate, their complexity in modulator and decimation filter, performance sensitivity to component matching and circuit imperfections, their stability, whether they need trimming or external components, and their signal range.

2.5.1. 1st Order Delta-Sigma A/D Converters

As shown in Fig. 2.5, these converters are very simple and made of very few components. Their *SNR* can be predicted from (2.5) and shown in Fig. 2.8. These converters are one of the most robust, least sensitive to circuit imperfections, and, under

regular circumstances, stable. However, their performance only increases by 1.5 bits per doubling of sampling frequency. For DC or slow-varying signals they produces single tones, which can be heard in an audio system, and are much more disturbing to ear than the white quantization noise.

2.5.2. 2nd Order Delta-Sigma A/D Converters

They are one of the most commonly used delta-sigma architectures (Fig. 2.9) by the semiconductor industry. Additional integrators and feedback help shape the quantization noise with a 2nd order low-pass transfer function, thus noise in the signal band is less than in the first order architecture case. Each doubling of sampling frequency brings additional 2.5-bit resolution. As shown in Fig. 2.8, with *OSR*=128, they have the potential to achieve 16-bit resolution. On the other hand, increased complexity of modulator demands a more complex digital filter. Component matching and circuit imperfections become more critical in determining the system performance. Increases in the loop overall gain and the number of delays (should not exceed two clock periods) of the loop have significant impacts in modulator stability. To avoid saturation, maximum signal range needs to be scaled or limited at the outputs of the integrators [17],[18]. Increasing the order of the loop filter helps reduce the correlation between the signal and the quantization error. Therefore, usually randomization is not necessary.

2.5.3. Higher-Order Delta-Sigma A/D Converters

Although Fig. 2.8 predicts that increasing the filter order in the delta-sigma loop would achieve higher and higher performances at slower *OSR*, circuit implementations of 3rd and higher order delta-sigma converters are observed to be much more prone to quantizer overloading than 1st and 2nd order architectures. When overloaded, a large-amplitude low-frequency limit cycle might occur and inner loop feedbacks become very small comparing to the integrator output of the previous stage. The feedback to the input

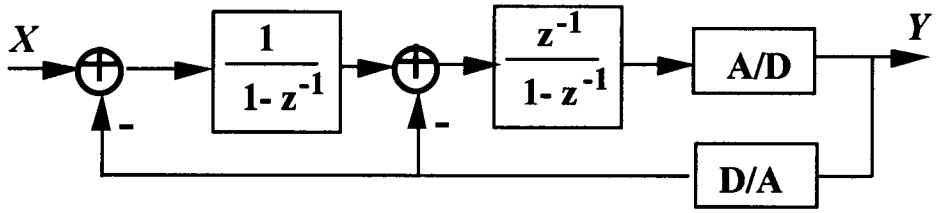


Fig. 2.9. 2nd order delta-sigma modulator.

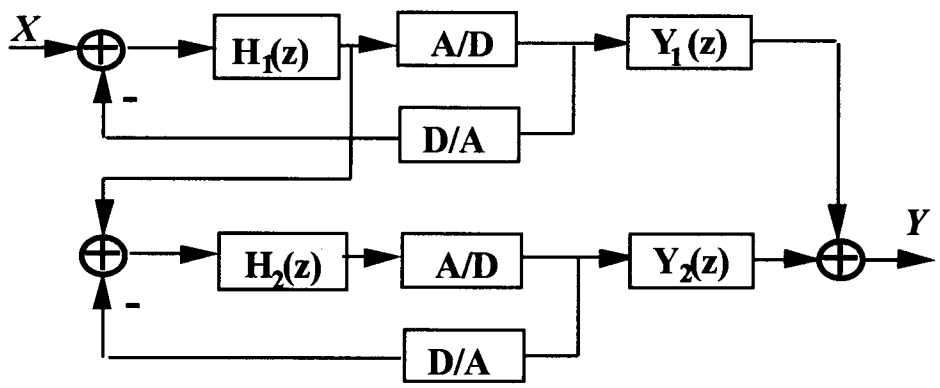


Fig. 2.10. Two-stage cascaded 1st order delta-sigma modulator.

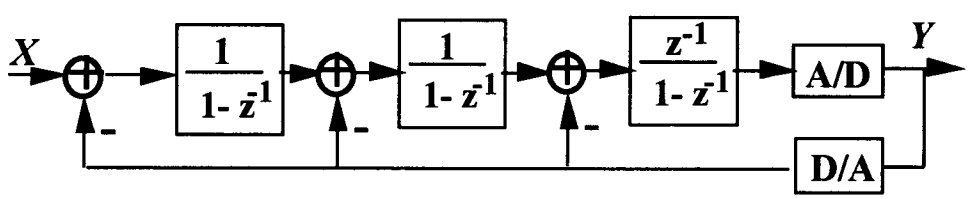


Fig. 2.11. 3rd order delta-sigma modulator.

with only one delay tries to stabilize the system and it cannot succeed. Resetting the output of integrators when a certain level is exceeded does make the overall system stable; however, the resolution tends to be lower than predicted from Fig. 2.8. A multi-level quantizer can be used [17] to overcome the overloading problem, but this causes increased sensitivity to circuit imperfections, such as loop gain.

Other architectures that can achieve higher-order performance are the ones that utilize nonmonotonic transfer functions [21]-[22]. Poles are placed in various locations in the signal band to lower in-band noise. Zeros are located strategically to minimize the high-frequency noise.

2.5.4. Cascaded (MASH) Delta-Sigma A/D Converters

As it is discussed in previous sections, stability becomes a significant concern as the order of the modulator is increased. Robust stability of the 1st order delta-sigma loop is very desirable, however its resolution is not as high as what is needed in some applications. With the help of couple of simple FIR filters, outputs of several 1st order modulators can be combined to achieve higher resolution [23], [24]. Fig. 2.10 demonstrates the architecture of cascaded two 1st order modulators. This architecture achieves higher resolution by arranging the Y_1 and Y_2 digital filters such that the first stage quantization error, E_1, is canceled, only a 2nd order filtered version of second stage quantization error, E_2 remains [25]. The necessary condition for this to be achieved is

$$\frac{Y_1}{H_1} = \frac{Y_2 H_2}{1+H_2} \quad .$$

This requires the analog circuitry to match the performance of the digital circuitry. Any errors cause some of the 1st order shaped quantization error noise to show up at the *digitally corrected* output and degrade the expected resolution. It has been shown [24] that phase error of the first filter affects resolution negatively especially at oversampling

ratios higher than 100. Opamp DC gain and slew rate requirements are higher than single-stage modulators; however, opamp bandwidth requirements are lower. D/A converters level spacing should be matched as closely as possible.

In the literature, there have been many examples of modulators that use cascaded stages of different order delta-sigma modulators (2-1 or 2-2 etc.) [23],[26]-[32]. Some of these techniques have been the starting achitectures of the bandpass delta-sigma modulators that were examined in this study and will be discussed in Chapter 5.

2.5.5. Higher-Order Single-Bit Quantizer Delta-Sigma A/D Converters

The architectures shown on Fig. 2.11, 2.12, and 2.13 are examples of higher-order modulators [33]-[36]. Their resolution can be higher than the other architectures, however, structures with filter orders higher than 2 are only conditionally stable. Therefore, some precautionary circuits such as limiters, reset switches are needed to avoid instability. They also tend to be more sensitive to circuit parameters.

2.5.6. Architectures with Multi-bit Quantizers

One of the initial motives of delta-sigma modulator architectures was to make the design of complex and demanding analog circuitry for A/D conversion easier (single comparator). However, as delta-sigma architecture evolved, benefits of reducing the quantization noise exponentially by increasing the number of bits of the quantizer began to outweigh the added complexity. One important problem that needs to be addressed in such architectures is the errors occurring in the D/A converters. Being directly subtracted from the input signal, these errors have a significant impact on the system performance.

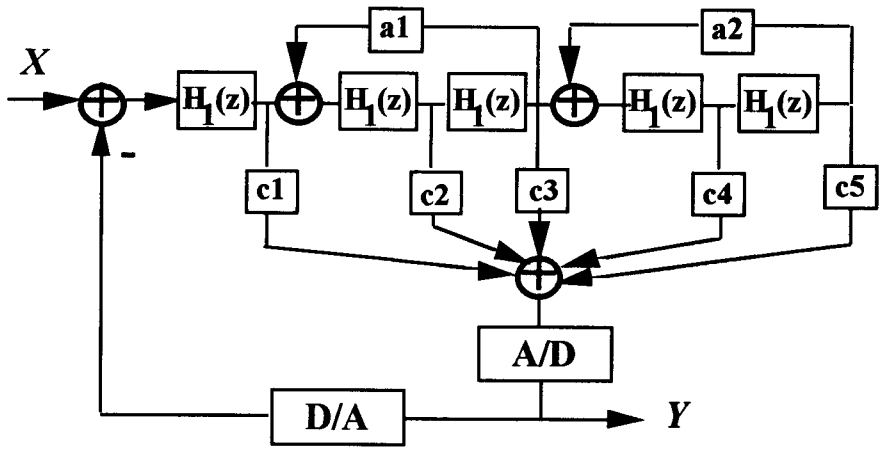


Fig. 2.12. 5th order feedback delta-sigma modulator.

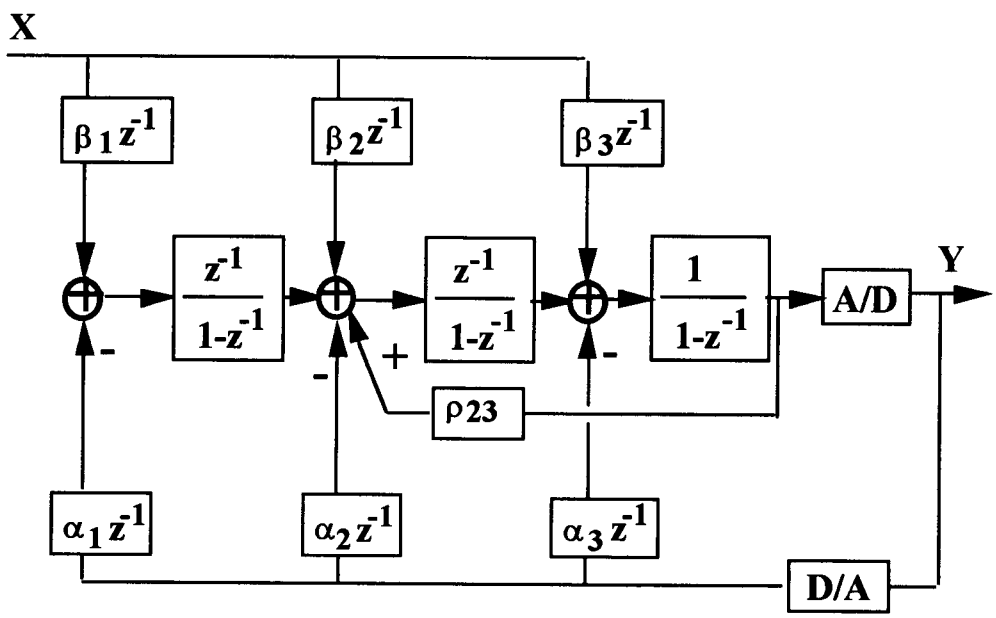


Fig. 2.13. A single-stage 3rd order delta-sigma modulator.

The most disturbing component of the D/A error is the nonlinearity, which must be less than half of the overall accuracy of the system not to have any adverse effects on the *SNR*.

There are several methods to deal with this problem other than costly solutions such as using external components or trimming of D/A. "*Barrel-shifting*", or randomly selecting the components of the D/A converter such as capacitors and resistors to minimize the correlation between the D/A error and the input signal is one of them [37]. Digital correction schemes with a RAM acting as a look up table followed by a digital delta-sigma truncator is another [38],[39]. Ref. [40] offers a solution to the D/A error problem by combining the desirable linearity features of a single-bit quantizer and reduced quantization error of multi-bit quantizers. Some others such as the Hairapetian architecture combine multi-bit and single-bit quantizers trying to achieve stability and high accuracy concurrently [41]. There are also examples of delta-sigma modulators which use three-level quantizers to avoid D/A nonlinearity error [42].

2.6. Architectures for Bandpass Noise-Shaping Oversampled A/D Converters

Bandpass delta-sigma modulators are a relatively newer concept than low-pass delta-sigma modulators. In the last decade, however, some studies have concentrated on its basic theory, finding the most desired and stable architectures and solving decimation problems [43]-[48].

Bandpass delta-sigma A/Ds can possess advantages similar to those of the lowpass modulators: inherent linearity, relatively simple analog circuitry, low sensitivity to component value variations, and reduced anti-aliasing filter complexity. In addition, by moving the A/D interface closer to the antenna, bandpass delta-sigma A/Ds may help increase flexibility in RF communication and wireless system design, reduce the number of components, and improve IF-strip testability.

Applications proposed for bandpass delta-sigma modulation have been digital radio for AM-receivers [49]-[52], narrow bandwidth systems such as spectrum analyzers, an most recently wireless system solutions [52]-[57]. In digital radio applications bandpass delta-sigma modulators eliminate the need for quadrature analog mixers and dual baseband A/D converters. Instead, quadrature mix to baseband can be performed in digital domain where it can be handled with much better efficiency. With bandpass delta-sigma modulators I/Q matching is no longer a problem. For wireless applications, a recent study has shown that bandpass delta-sigma modulators can be used as a quadrature demodulation technique that is not sensitive to errors due to 90° phase inaccuracy and path mismatch, and they can shift the bandpass spectrum directly to baseband [54].

2.6.1. Decimation for Bandpass Delta-Sigma A/D Converters

The first decision to be made in the system-level design of a bandpass delta-sigma A/D converter is choosing the ratio between the band center frequency, ω_0, the sampling frequency, ($\omega_s = 2\pi$) Selecting ω_0 close to π results in lower sampling rates (Fig 2.14). On the other hand, there are advantages of choosing ω_0 close to 0: the *OSR* is higher, and the anti-aliasing filter design is easier due to the larger transition band.

Another important design consideration is the decimation filter which follows the delta-sigma loop. The decimator needs to perform narrow bandpass filtering on a high-speed bit stream. In addition, due to the narrow relative bandwidth of the signal a sharp cut off is necessary. These requirements can be realized by implementing the digital filtering in two stages similar to the case of low-pass delta-sigma modulators; first stage operating at the sampling rate, and a second stage operating at a fraction of the sampling rate ("decimated").

Fig. 2.15 shows the general block diagram of a bandpass delta-sigma A/D converter. The decimator is the sub-block that removes the out-of-band quantization noise and translates the signal to the baseband. Because the input bit stream is clocked at the 'fast'

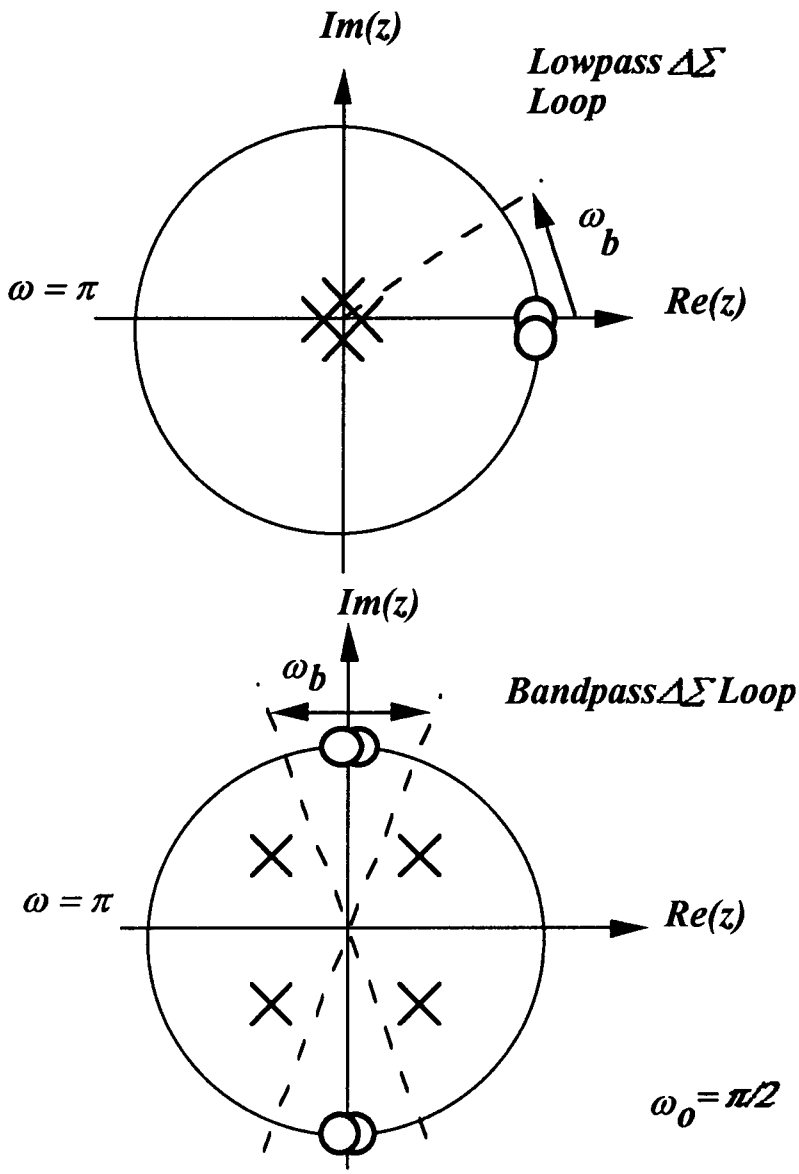


Fig. 2.14. Pole-zero locations of the noise transfer functions of the lowpass and bandpass delta-sigma loops.

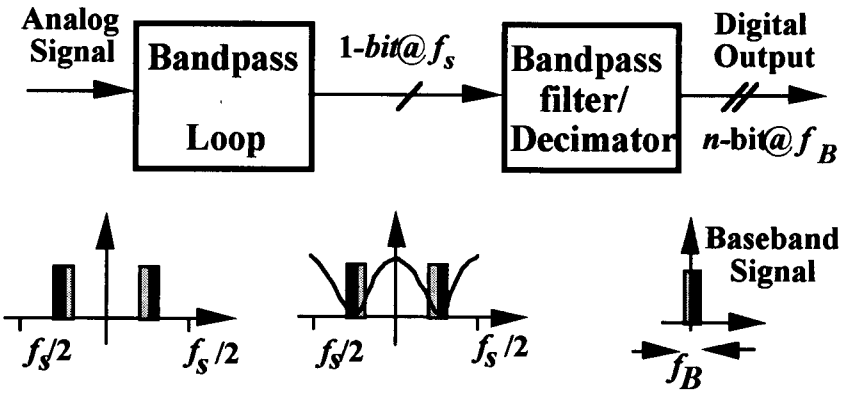


Fig. 2.15. Bandpass delta sigma modulator block diagram.

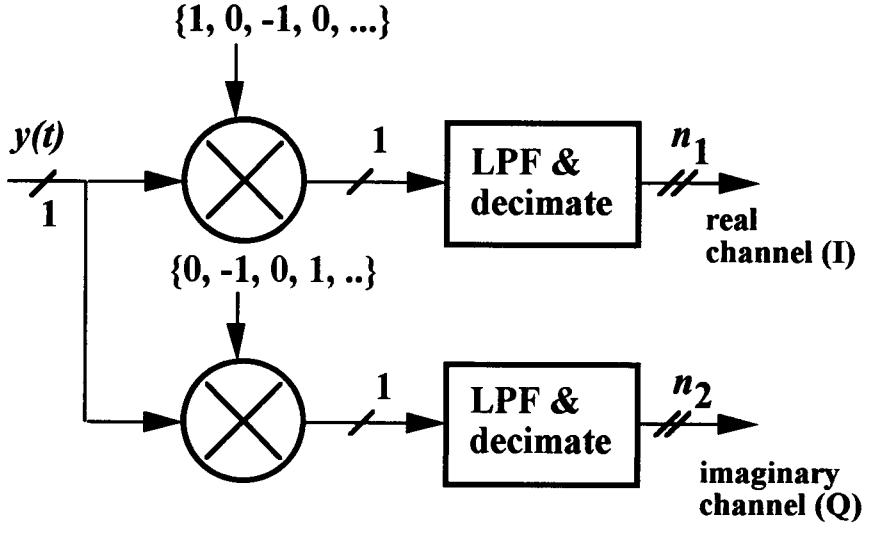


Fig. 2.16. Bandpass decimator in the case of $\omega_0 = \pi/2$.

sampling rate, complications in circuitry must be avoided. To do the decimation, the output of the delta-sigma loop is mixed with $\exp(-j\omega_0 t)$, and the passband at DC is then lowpass filtered using sinc^k filtering[44]-[48]. Simple fractions of π allow the decimator to be designed with less complications. Since ω_0 was chosen to be $\pi/2$ for the particular A/D converters that have been designed as examples in this chapter, the details of the decimator for this case are included here. For $\omega_0 = \pi/2$, the mixing signal will be {1, -*j*, -1, *j*,...}(Fig. 2.16). At any time, only one lowpass filter and decimator is in use, therefore multiplexing is possible to save hardware.

2.6.2. Pole-Zero Locations of Noise Transfer Function in Bandpass Architectures

Fig. 2.14 shows the *z*-plane representation of the poles and zeros of the $|H_n(z)|$ for lowpass and bandpass cases. The band where the noise shaping is performed is moved from low frequencies to $\pi/2$. In the bandpass delta-sigma loop, the magnitude of the $H_n(z)$ reaches its maximum value at frequencies of 0 and π, and its minimum at $\pi/2$ and $3\pi/2$, whereas the $H_n(z)$ is at its highest at $\omega=\pi$, and at its minimum at $\omega=0$ for the lowpass case. The bandwidth over which the magnitude of $H_n(z)$ is minimized is determined by the oversampling ratio, $OSR = \pi/\omega_B$.

2.6.3. Direct Realization of the Loop Filter

The first integrated circuit solutions [49]-[50] to the bandpass delta-sigma A/D design problem used the direct realization technique. The noise transfer function was implemented with a cascade-of-resonators structure (Fig. 2.17). The reason this structure was chosen instead of a cascade-of-integrators was its insensitivity to coefficient variations that are implemented with integrated capacitors. Most recently reported results [51] indicated that parasitic capacitors and layout problems has moved the upper notch which is set by the second resonator off the unit circle.

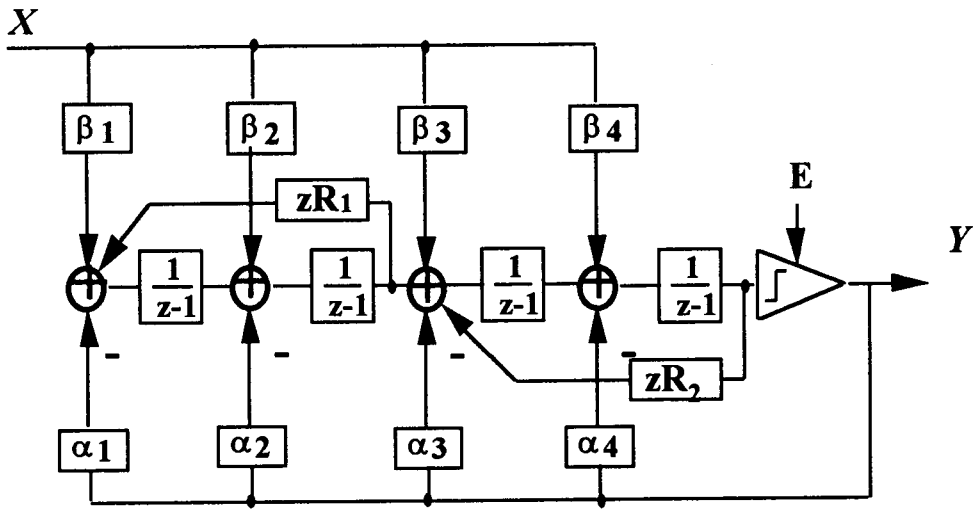


Fig. 2.17. Cascade of resonators architecture.

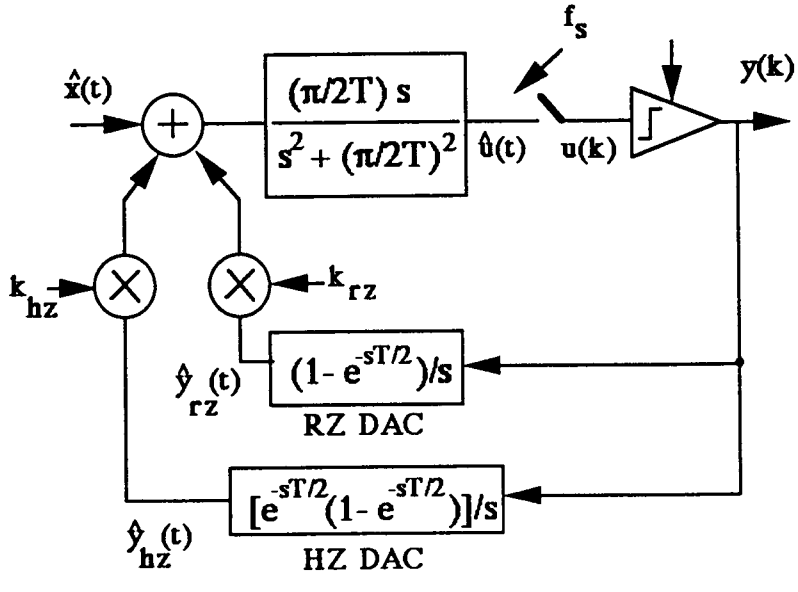


Fig. 2.18. 2nd order multi-feedback delta-sigma modulator with an LC resonator loop filter.

For wide-band applications, the component value accuracy is not very stringent and the tolerances are practical. However, narrow-band applications can benefit from a different design technique, using *N*-path integrators, which are discussed in Chapter 4.

2.6.4. Realization with LC Resonators

A recent study [58] demonstrated in simulation that the discrete SC filter of the bandpass delta-sigma loop can be implemented by LC resonators (Fig. 2.18). In this continuous time modulator, the overall loop impulse response is obtained by convolving the s-domain loop filter with the DAC impulse response. Three different DAC feedbacks, that are non-return to zero, return to zero and half delay return to zero impulse responses, can be arranged in the loop to make sure the overall system's s-domain response resembles that of a well-analyzed well-known discrete-time version's. Because all but one of the delays in the loop are realized in the continuous domain, control of the loop delay is critical and can be the limiting factor of loop's stability.

2.6.5. Realization with Pseudo-*N*-Path Integrators

One of the most important aspects of bandpass delta-sigma A/D converter design is guaranteeing the location of the zeros of the noise transfer function, $H(z)$. If they move away from the unit circle (wrong magnitude) the notch becomes shallower. If they move slightly inside of the unit circle, the modulator output suffers from limit cycles and consequently intermodulation may occur [56]. If the angle of the zeros move, the center frequency changes. The predicted SNR performance, therefore, degrades if the zeros change their location due to component value variations. Pseudo-*N*-Path (PNP) integrators ensure the location of the center frequency since it is determined by the clock frequency and the number of paths.

PNP integrators have been used to design narrow-band bandpass filters for more than a decade as it is discussed in Chapter 4. Their main handicap has been the clock feedthrough noise that shows up in the middle of the passband as a single tone if there is any asymmetry between the paths. The clock feedthrough noise is kept usually at -60 to -80 dB at best in *N*-path filters. The novel PNP integrators in Chapter 4 eliminate this problem by circulating the charge among several capacitors, using identical paths for circulating signals (no path mismatches) and repeating the circulation at a frequency that does not cause an aliasing component of the clock feedthrough within the passband.

3. NOVEL DELTA-SIGMA A/D MODULATOR ARCHITECTURES FOR LOW-PASS APPLICATIONS

3.1. Motivation

High-accuracy and high-resolution delta-sigma modulators are important building blocks in digital audio and telecommunication systems [4], [41]. It is known that higher resolution can be achieved for a delta-sigma modulator by increasing either the oversampling frequency, or the order of noise-shaping characteristic, or the number of levels in the internal quantizer.

The new structures which will be described here use multiplexing techniques to simulate the performance of higher-order modulators without the complexity and stability problems. For example, by adding a few switches to a 1st order delta-sigma modulator structure and doubling the clock frequency it is possible to obtain an SNR performance which would have been obtained from a 2nd order modulator with half of the oversampling ratio. This translates to savings in hardware complexity in exchange for a faster clock. With the additional benefits of guaranteed stability and availability of precise and fast clocks these two structures can be economic alternatives to the conventional delta-sigma modulators, especially for narrow-bandwidth applications.

3.2. A Multiplexed 1st Order Delta-Sigma Modulator Structure

3.2.1. System Description

The architecture of a multiplexed 1st order delta-sigma modulator is shown in Fig. 3.1. In this example, $N = 3$ is used. Block A contains a stable 1st order delta-sigma modulator (a 2nd order delta-sigma modulator can also be used) with a pseudo-N-

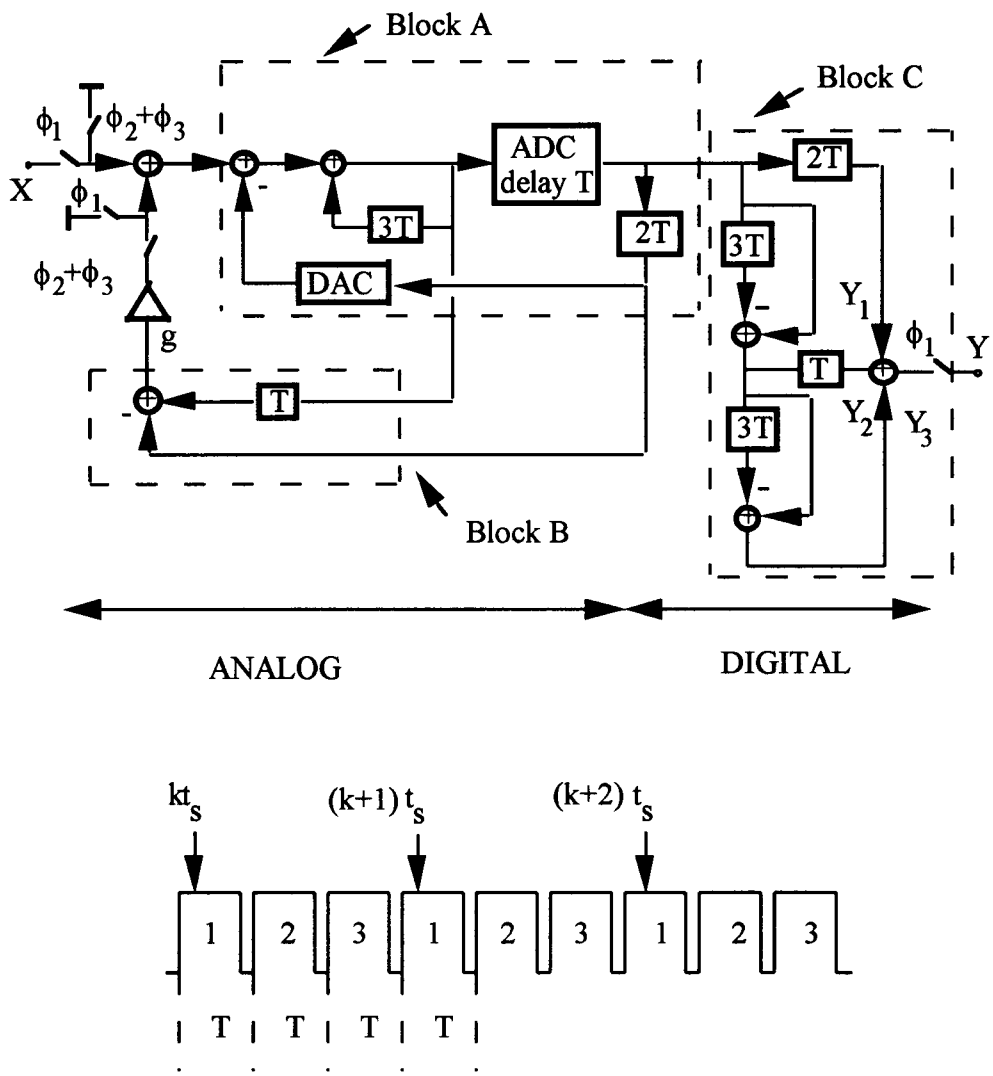


Fig. 3.1. 3-phase multiplexed delta-sigma modulator and its timing diagram.

path integrator [59] instead of an ordinary accumulator. Block B is introduced for generating the quantizer error e_n defined as the differential signal between the output and input signals of the quantizer during the period $\phi_3 = 1$. The quantizer error serves as the input signal when $\phi_2 + \phi_3 = 1$. During the $\phi_1 = 1$ period, this extra feedback path is disconnected, and the input signal x is sampled.

The operation of the proposed system is similar to that of the cascaded 1st order delta-sigma modulator (MASH), although the conversion rate of the input signal x is N times slower than that of typical MASH structures for the same clock frequency. However, the order of the proposed structure is increased by N in comparison with the order of delta-sigma modulators used in block A. It should be noted that the input signal x as well as the quantizer errors e_n ($n = 1, 2, 3, ..., N\text{-}1$) are always processed through the *same* block A. The digital block C effectively cancels the quantizer errors $e_1, e_2, ..., e_{N-1}$ if the output is sampled in the same phase ϕ_1 as the input signal.

3.2.2. A/D and D/A Converter Realizations

To increase the resolution of the delta-sigma modulators of Fig. 3.1, the single-bit quantizer can be replaced by a multi-bit one. A detailed analysis of the system in Fig. 3.1 indicates that optimum performance is obtained if the single-bit quantizer is employed when $\phi_1 = \phi_2 = ... = \phi_{N-1} = 1$, and the multi-bit one is used when $\phi_N = 1$. In practice, the same multi-bit A/D converter (ADC) and D/A converter (DAC) can be used for the realization of both multi-bit and single-bit ADC and DAC by simply using the most significant bit (MSB) of the multi-bit converter for the single-bit conversion [41]. However, in such a case as has been discussed in Chapter 4 and shown in the next section, the nonlinearity noise of the multi-bit DAC slightly reduces the predicted *SNR* performance.

3.2.3. Analysis

Assuming that the quantization error is modeled as an uncorrelated additive white noise, and applying a linear analysis in the z-domain to the system shown in Fig. 3.1, the output signals $Y_1(z)$, $Y_2(z)$, $Y_3(z)$ valid during phase $\phi_1 = 1$ can be obtained:

$$Y_1(z) = [\, X(z)\, z^{-1} + (1 - z^{-3})E_1(z)\,]\; z^{-2} \tag{3.1a}$$

$$Y_2(z) = [\, (-E_1(z))\, z^{-1} + (1 - z^{-3})E_2(z)\,]\; z^{-1}(1 - z^{-3}) \tag{3.1b}$$

$$Y_3(z) = \{[\, -E_2(z) + \Delta(z)\,]\, z^{-1} + (1 - z^{-3})E_3(z)\,\}\,(1 - z^{-3})^2 \tag{3.1c}$$

where $z = e^{sT}$; $X(z)$ is the input signal; $Y_1(z)$, $Y_2(z)$, and $Y_3(z)$ are the signals before the final summation; $E_1(z)$, $E_2(z)$ are the quantization noises of the single-bit ADC for $\phi_1 = 1$ and $\phi_2 = 1$ respectively; $E_3(z)$ is the quantization noise of the multi-bit ADC and $\Delta(z)$ is the nonlinearity noise of the multi-bit DAC during $\phi_3 = 1$, all transformed into the z-domain.

Using equations (3.1a, b, and c) the final expression for the output signal becomes

$$Y(z) = Y_1(z) + Y_2(z) + Y_3(z) = X(z)\, z^{-3} + \Delta(z)\, z^{-1}(1 - z^{-3})^2 + E_3(z)\,(1 - z^{-3})^3 \tag{3.2}$$

Thus, as in previously proposed structures [40], [41], [60], the quantization noises e_1 and e_2 of the single-bit quantizer are canceled in the final output. It should be noted that the nonlinearity noise of the DAC is also subject to 2nd order noise shaping. The proposed system is stable because the self-contained 1st (or possibly 2nd) order delta-sigma modulators in block A is itself stable (or conditionally stable).

The improvement in accuracy for the proposed delta-sigma modulators for a fixed signal bandwidth and fast clock rate can be best observed from the maximum *SNR* predictions. Under ideal conditions, the equation is

$$SNR_{max} \approx 3(2LN + 1)\, log_2\, (f_c / N2f_o) - 4(2LN - 1) + 20\, log_{10}\, (2^k - 1) \qquad (3.3)$$

where f_c is the clock frequency, f_o is the bandwidth of the signal and L is the order of the delta-sigma modulator in block A. Also, N is the number of conversion phases, and k is the number of bits used in the quantizer.

In Fig. 3.2, the SNR given by the equation (3.3) versus the ratio $f_c/(2f_o)$ of the proposed delta-sigma modulator system with a 1st order circuit in block A and a one-bit quantizer is plotted. The number of phases N is chosen as a parameter. Fig. 3.2 demonstrates the improvement obtainable by increasing the number of the phases for a constant clock frequency and signal bandwidth as well as given hardware complexity. Note that for practical reasons the ratio $f_c/(2f_o)$ is normally chosen to be greater than 32.

For a given application the optimal values of N and $f_c/(2f_o)$ can be selected using equation (3.3) or from the Fig. 3.2. It should be noted that the SNR values shown in Fig. 2.2 can be further increased by an additional 9.5 dB, 16.9 dB, 23.5 dB or 29.8 dB, if 2-bit, 3-bit, 4-bit or 5-bit internal quantizers are used, respectively.

3.2.4. Simulation Results

Extensive system simulations were performed to verify the improved system performance of the multiplexed 1st order noise-shaping structure. In Fig. 3.3 the power spectral densities of the system in Fig. 3.1 with 1-bit DAC, ideal 5-bit ADC and DAC, and nonideal 5-bit A/D converter and DAC with an rms nonlinearity equal to 0.1 LSB are plotted. The 5-bit quantizer is used only during period $\phi_3 = 1$. Fig. 3.3 demonstrates the increase in resolution achievable by using a multi-bit quantizer during the last phase ($\phi_N = 1$). The degradation due to the DAC nonlinearity is small because nonlinearity noise is high-pass filtered by a 2nd order noise-shaping function. Note that this operation simulates that of the A/D converter described in [41].

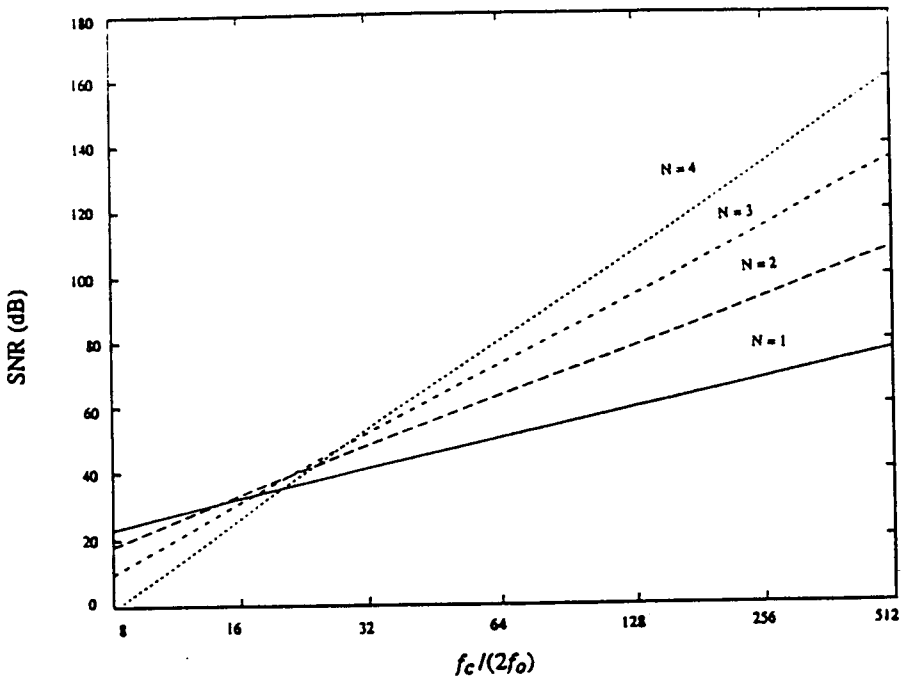


Fig. 3.2. SNR of the modulator in Fig. 3.1. versus $f_c/(2f_0)$ with N as a parameter.

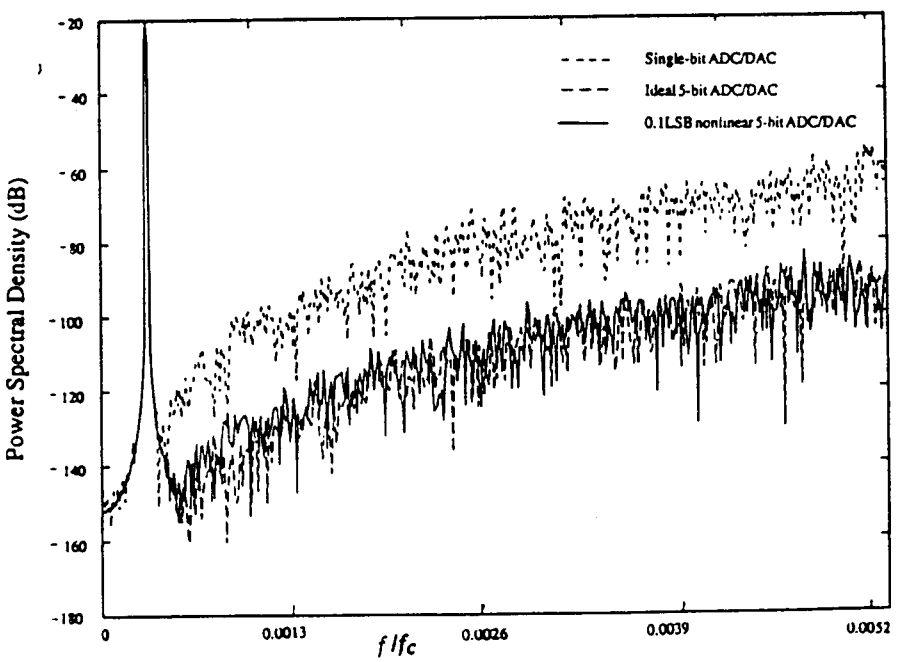


Fig. 3.3. Power spectra of the system in Fig. 3.1. with single- and multi-bit quantizers.

Fig. 3.4 compares the signal-to-noise plus distortion (S/N+D) performances of a 3-phase multiplexed 1st order modulator with various quantizers; one-bit, ideal 5-bit and 0.1 LSB rms nonlinear 5-bit ADC and DAC. These SNR results were obtained for the oversampling ratio ($f_c/(2f_o)$) of 96.

The effects of feedback gain errors in a cascaded delta-sigma modulator architecture have been examined in the literature [28]-[29]. The proposed 1st order multiplexed delta-sigma modulators structure is also sensitive to gain errors in the feedback path. Fig. 3.5 shows the degradation of SNR of a 2-phase multiplexed 1st order delta-sigma modulators with a single-bit quantizer as the feedback gain varies from 0.5 to 1.5. The sharp decrease for slight changes of the feedback gain appears to be one of the major drawbacks of this structure. Another important problem is the need to match the analog and digital parts of the system accurately for a perfect cancellation. There exist other options for multiplexed 1st order delta-sigma modulators which exhibit much lower sensitivity to mismatching errors.

3.3. Multi-Loop Delta-Sigma Modulator Structures

3.3.1. System Description

Fig. 3.6a shows a general Nth-order multi-feedback delta-sigma modulators structure. One can observe that similar blocks are used to construct each stage [64]. Therefore, multiplexing techniques can be employed to achieve the same operation. The N-phase multi-loop delta-sigma modulators structure shown in Fig. 3.6b is the multiplexed equivalent of the system of Fig. 3.6a. The integrators of the multi-feedback delta-sigma modulators stages have been replaced by a single N-path integrator. The input of the ADC is sampled and held when the phase ϕ_N is high. The input to the loop is arranged to

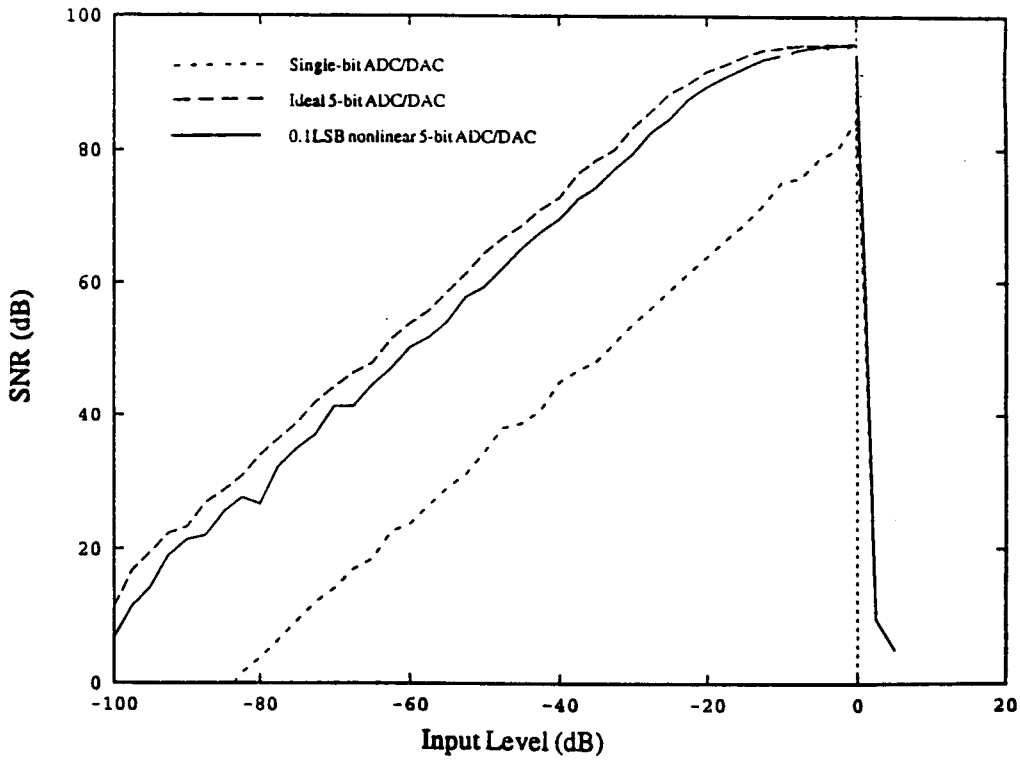


Fig. 3.4. SNR versus Input Level of the system in Fig. 3.1. with $f_c/(2f_0) = 96$.

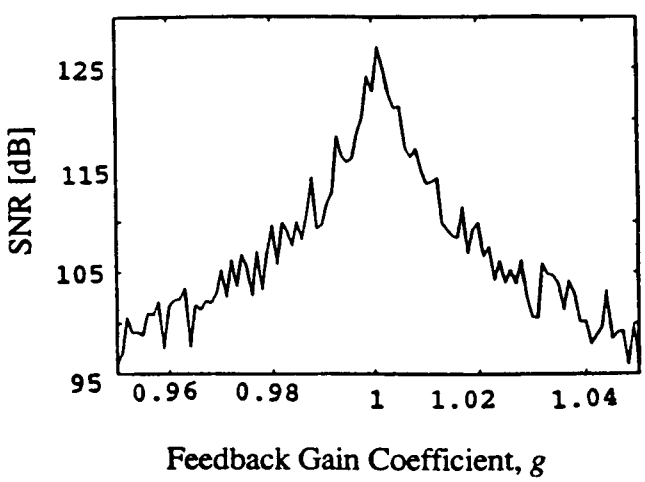
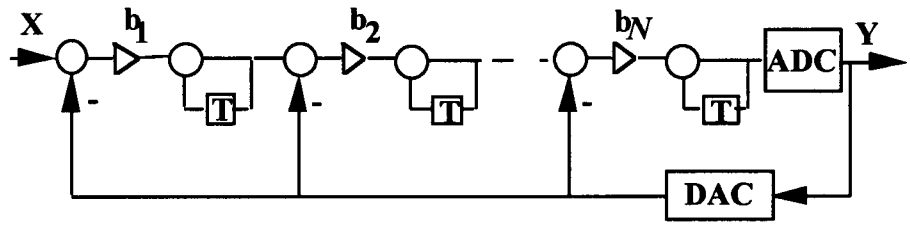
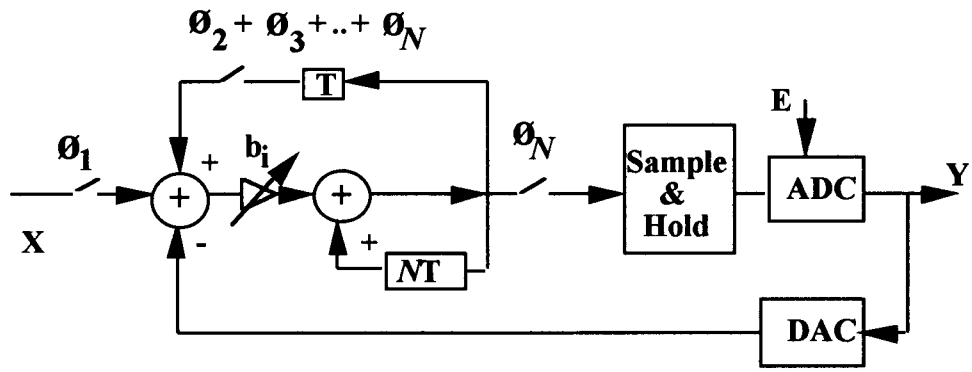
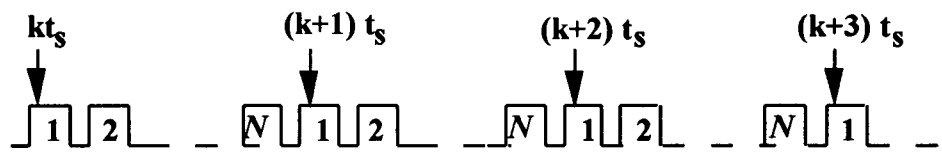


Fig. 3.5. SNR versus Feedback Gain Coefficient of the system in Fig. 3.1.



(a)





(b)

Fig. 3.6. (a) *N*th-order multi-feedback delta-sigma modulator.
(b) *N*-phase multi-loop delta-sigma modulator.

be either the system input X (phase ϕ_1) or a delayed output of the N-path integrator (phases ϕ_2 to ϕ_N). Thus, the N-phase multi-loop delta-sigma modulators structure emulates one of the stages of the Nth-order multi-feedback structure in each phase. Since the output of the A/D converter is determined by the sample of output of the N-path integrator taken at phase ϕ_N for all N phases, the system output can be sampled in any of the N phases.

3.3.2. Analysis

Assuming that the quantization error is modeled as an uncorrelated additive white noise, the output of the ADC appears one clock period delayed, and applying a linear analysis in the z-domain to the system shown in Fig. 3.6b, the following equations can be obtained:

$$X(z) - Y(z) = W(z)^{(1)} (1 - z^{-N}) \qquad \text{(phase } \phi_1\text{)}$$

$$(W(z)^{(1)} - Y(z)) z^{-1} = W(z)^{(2)} (1 - z^{-N}) \qquad \text{(phase } \phi_2\text{)}$$

$$(W(z)^{(2)} - Y(z)) z^{-2} = W(z)^{(3)} (1 - z^{-N}) \qquad \text{(phase } \phi_3\text{)}$$

$$\vdots$$

$$(W(z)^{(N-1)} - Y(z)) z^{-(N-1)} = W(z)^{(N)} (1 - z^{-N}) \qquad \text{(phase } \phi_N\text{)}$$

$$Y(z) = W(z)^{(N)} z^{-1} + E(z) \qquad \text{(A/D equation)}$$

where $z = e^{sT}$; $X(z)$ is the system input; $W(z)^{(i)}$ is the output of the N-path integrator at phase i; $E(z)$ is the quantization noise; $Y(z)$ is the system output; and N is the total number of phases.

Solving the equations above, the following transfer function can be obtained:

$$Y(z) = X(z) z^{-N} + E(z)(1 - z^{-N})^N \qquad (3.4)$$

The maximum *SNR* of multi-loop delta-sigma modulators with a single-bit quantizer is identical to the one of multi-feedback delta-sigma modulators, and under ideal conditions can be calculated from [61]:

$$SNR_{max} \approx \left[3(2L+1)/2\pi^{2L}\right](f_s/f_o)^{2L+1} \qquad (3.5)$$

where f_S is the sampling frequency, $2f_o$ is the signal bandwidth, and L is the order of the modulator, which here equals the number of the phases employed. By choosing the oversampling ratio ($f_S / 2f_o$) and the order of the modulator approximately, the desired *SNR* performance can be achieved.

One important point is that for multi-feedback systems with orders higher than two, there is no sufficient and necessary stability test valid for all known modulators. To guarantee overall system stability, (N + 1)-bit quantizers must be employed for an Nth-order modulator [62]. The maximum *SNR* of a multi-loop delta-sigma modulator with a multi-bit quantizer under ideal conditions is given by

$$SNR_{max} \approx \left\{\left[3(2L+1)/2\pi^{2L}\right](f_s/f_o)^{2L+1}\right\}(2^m - 1) \qquad (3.6)$$

where m is the number of quantizer bits. Unfortunately, linearity errors in the D/A converter degrades considerably the expected performance of a delta-sigma modulators with multi-bit quantizers. However, a number of techniques have been introduced for the cancellation of such D/A nonlinearity errors [40], [41], [60], [63].

3.3.3. Simulation Results

The performances of the multi-loop structure and the multi-feedback structure were compared for 2nd order and 3rd order modulators. The oversampling ratio was chosen to be 64 for these simulations.

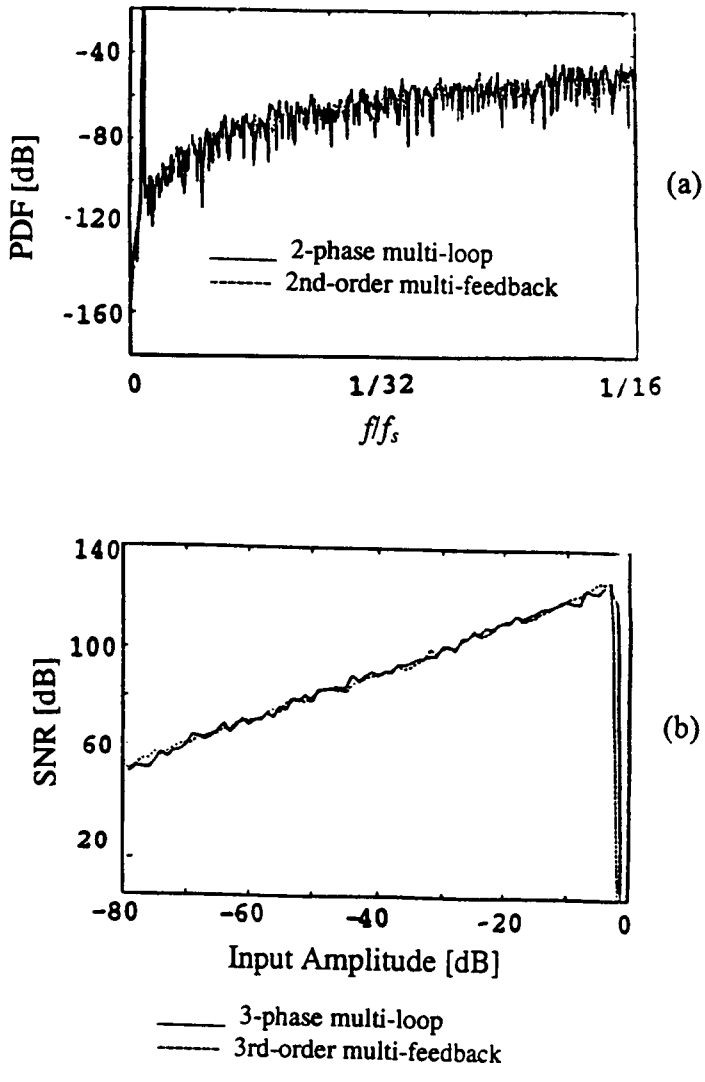


Fig. 3.7. (a) Power spectra of 2-phase multi-loop and 2nd order multi-feedback delta-sigma modulators for a -20 dB sinusoidal input.
(b) SNR versus Input Amplitude curves of the 3-phase multi-loop and 3rd-order multi-feedback delta-sigma modulators with 4-bit quantizers ($OSR = 64$).

Gain coefficients of 0.5 and 1 were used in the first and second integrators of the 2nd order multi-feedback delta-sigma modulator, respectively. The gain coefficient of the 2-path integrator in the 2-phase multi-loop delta-sigma modulator was chosen as 0.5.

For the 3rd order case, 4-bit quantizers are employed to ensure system stability in both 3rd order multi-feedback and 3-phase multi-loop delta-sigma modulators. All integrator gains are selected equal to 1. Fig. 2.7a and 2.7b reveal that performance of the two systems are very close.

3.4. Conclusions

In this chapter, two new delta-sigma A/D structures employing time-multiplexing techniques were proposed [64],[59]. For a given oversampling ratio, the multiplexed 1st order delta-sigma modulator structure achieves a higher resolution conversion by increasing the number of its clock phases. This concept can easily be extended to higher-order (e.g. 2nd order) delta-sigma modulators. The necessity to match analog and digital parts for a perfect cancellation and the sensitivity to the feedback gain errors are the main problems of these systems. However, the principle is also applicable to more robust converter structures.

The multi-loop delta-sigma modulator structure offers savings in hardware while it is able to achieve high-resolution conversion for a given oversampling ratio. Especially for narrow-bandwidth signals, this technique provides an effective way of obtaining high-resolution conversion by increasing the oversampling frequency. The same concept can be adapted to bandpass delta-sigma A/D applications with narrow signal bandwidths. Since there is no cancellation of quantization errors, accurate matching of analog and digital parts is not required. The output of the system is valid for any of N phases. To improve

the performance further, correction or randomizing techniques eliminating the D/A nonlinearity error should be used.

4. NOVEL PSEUDO-N-PATH (PNP) INTEGRATORS

4.1. Introduction

The idea of N-Path Integrators [65] was prompted by requirements of impractically high DC opamp gain and overly high sensitivities to capacitance variations in narrowband switched-capacitor (SC) filters. As shown on Fig. 5.52 of the [66], the pole-Qs of the identical bandwidth lowpass and bandpass filters can be calculated as follows:

$$Q_{LP} \approx (B/2) / 2|\sigma_1|$$
$$Q_{BP} \approx (\omega_0 \pm B/2) / 2|\sigma_1| \approx \omega_0 / 2|\sigma_1|$$

For a narrowband filter, the $\omega_0 \gg B/2$ is the case, therefore, $Q_{BP} \gg Q_{LP}$. The DC gain of the opamps that are used to construct these filters is usually selected as $200Q$. For bandpass filters, opamp requirements become more stringent as ω_0 to $B/2$ ratio increases. Sensitivities to capacitor variations are also proportional to the pole-Q, and are shown to increase by the ω_0 to $B/2$ ratio increase [66].

An N-path filter consists of N lowpass filters, clocked in such a way that each of them are connected to the system's input and the output only during one of the N clock phases (Fig. 4.1) [66]. Each path has the same transfer function assuming that all lowpass filters are identical. However, the sampling rate of the path filters is only f_s/N, where f_s is the sampling rate of overall filter. The advantage is the ability to use the f_s/Nth passband (Fig. 4.2). In a single path filter, this would be impossible due to aliasing of all frequencies below $f_s/2N$. On the other hand, in an N-path filter, the Nyquist rate is $f_s/2$, and the

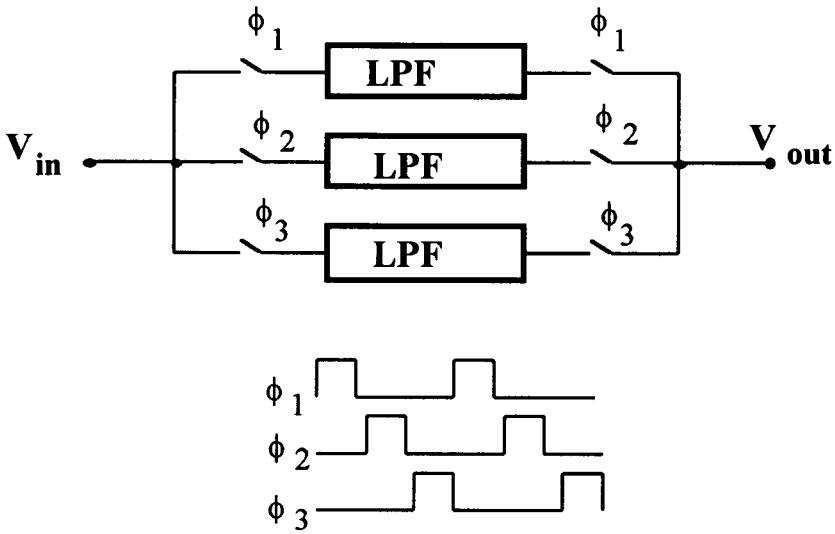


Fig. 4.1. General block diagram of a 3-path filter.

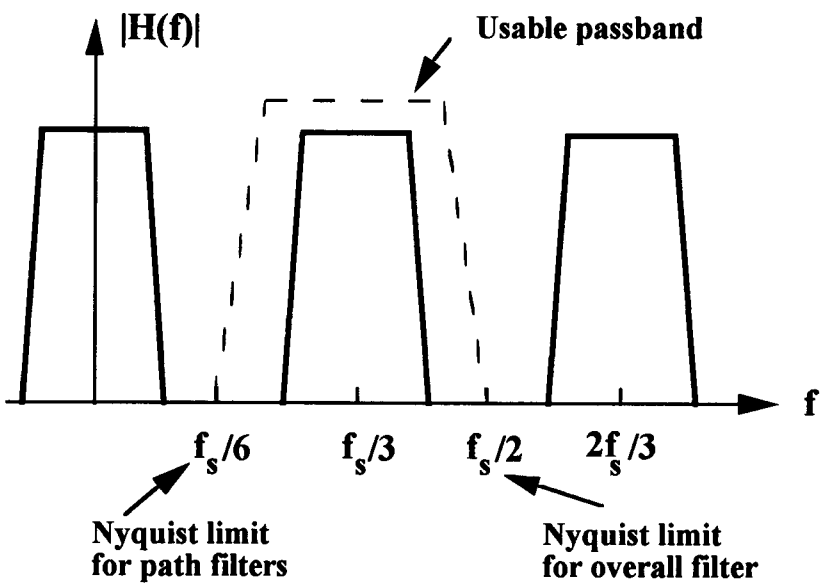


Fig. 4.2. Frequency response of a 3-path filter.

passband centered at f_s/N is safely within this range. An antialiasing filter is still required to keep undesired bands from aliasing back to the passband.

The conventional structure of an N-path circuit consists only of one physical path for signal transmission, consequently the problem of capacitor mismatch is overcome. On the other hand, $N(N+1)$ clock phases are needed in this classical approach for performing one cycle of operation. To limit the number of required clock phases and to increase the speed of the system, the RAM-type and hybrid-type PNP circuits were proposed [68]-[70].

However, both of these concepts have significant practical disadvantages: In a filter containing RAM-type PNP integrators (Fig. 4.3), the peak of clock feedthrough noise is located at the center frequency of its passband due to imperfectly balanced paths [67]. The hybrid-type PNP filter does not have a noise peak mentioned above. However, each integrator requires an active feedback branch (Fig. 1 of [70]). Therefore, the total number of opamps has to be doubled, and some number of switches and one extra capacitor are needed.

These serious practical drawbacks of previously proposed PNP SC filters can be avoided by employing novel integrators proposed in this chapter.

4.2. PNP SC Integrator Structures Based on the $z \rightarrow z^N$ Transformation

4.2.1. Single-Ended Structures

Fig. 4.4 shows the general structure of the proposed PNP integrator [59]. N= 3 is assumed for simplicity. In this scheme, the topology of the feedback network Y is the same as in the conventional PNP integrator (Fig. 9 of [69]). However, unlike in earlier structures, the capacitors play essentially identical roles in the operation, instead of one capacitor singled out to generate all output voltages. Various types of input coupling

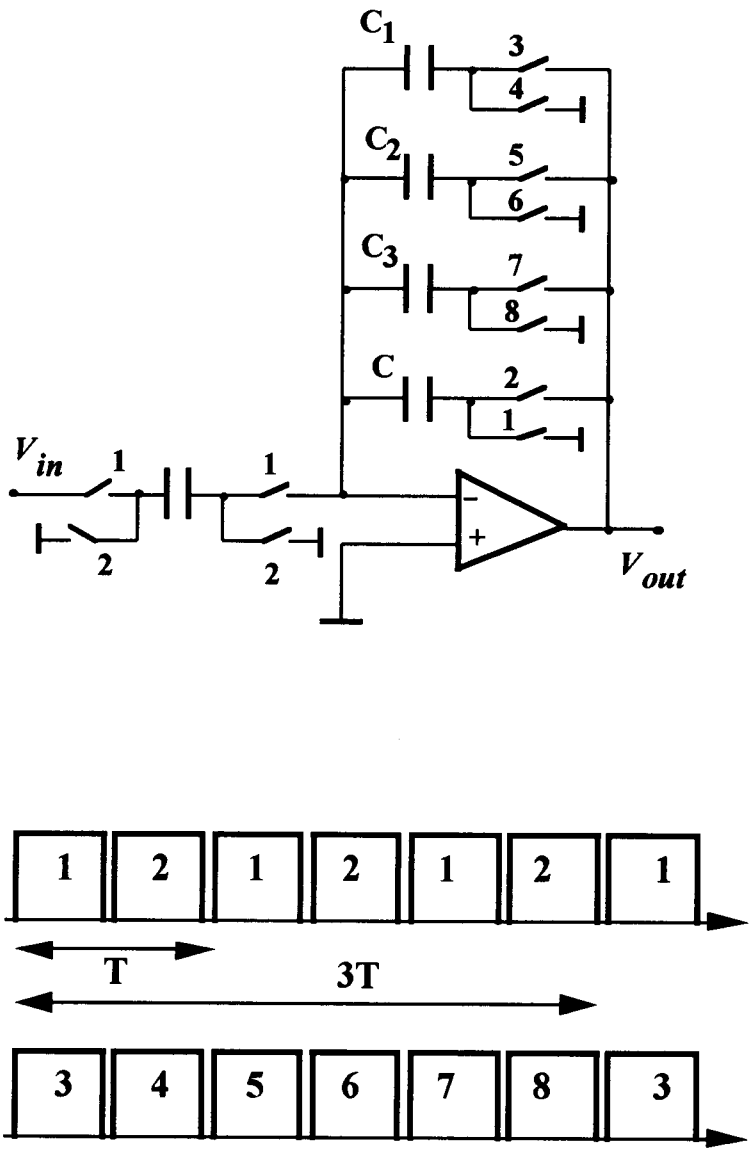


Fig. 4.3. RAM-type pseudo-3-path integrator.

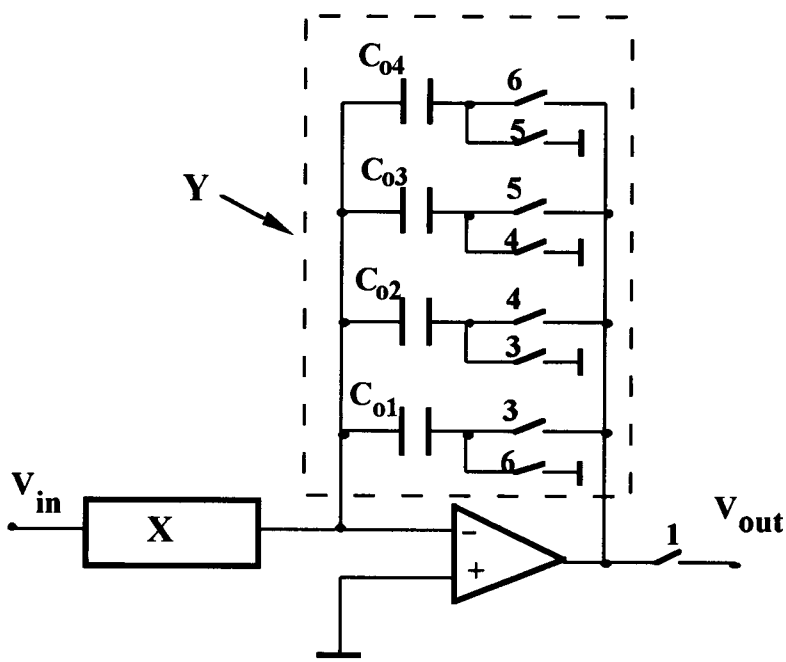


Fig. 4.4. PNP SC integrator based on $z \rightarrow z^N$ transformation.

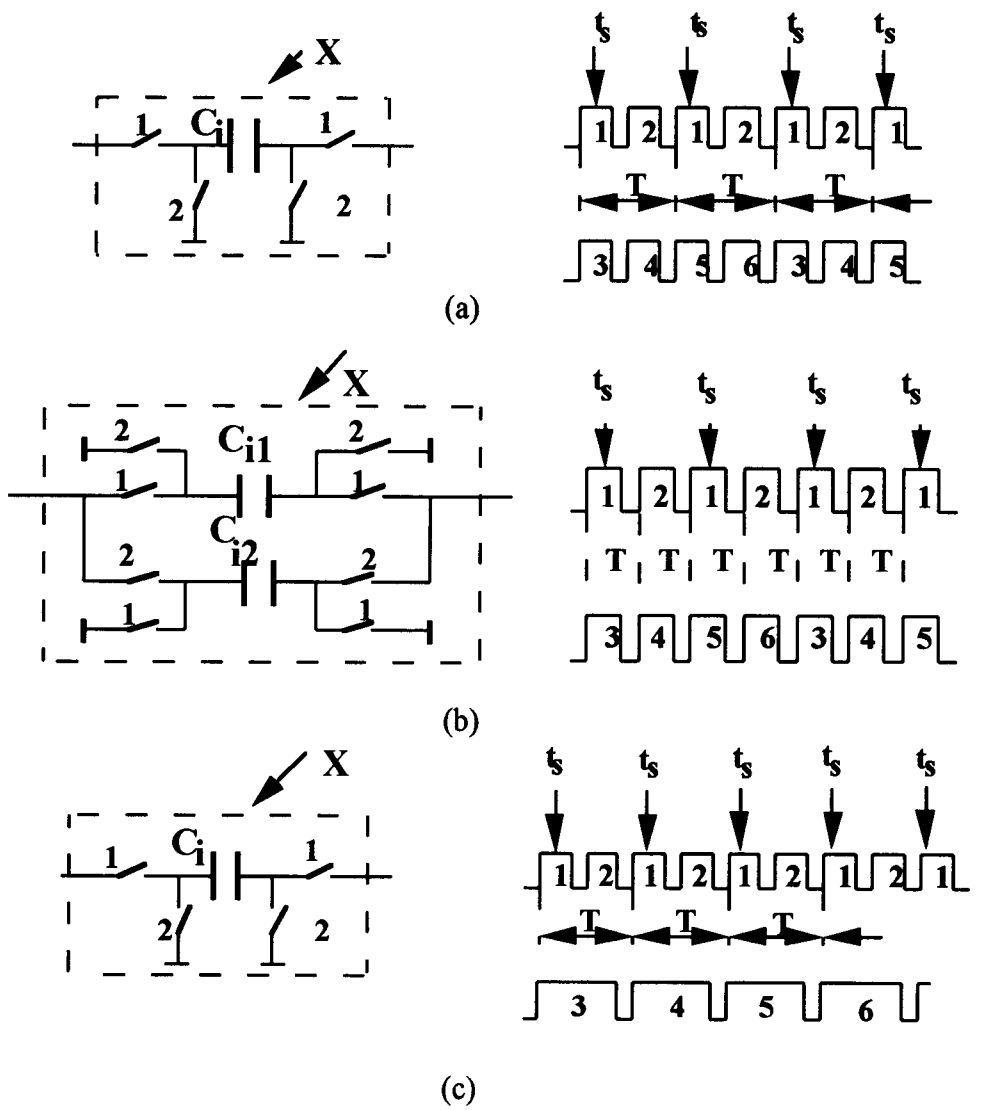


Fig. 4.5. Input networks and timing diagrams for the block of Fig. 4.4.
(a) Type I, (b) Type II, (c) Type III.

capacitor networks can be used which trade off speed versus complexity. Assuming that the DC gain of the opamp is infinite, and all circulation capacitors are perfectly matched, and $C_{o1} = C_{o2} = C_{o3} = C_{o4} = C_o$, the voltage transfer functions of these integrators are all given by

$$H(z) = \frac{V_{out}}{V_{in}} = -\frac{C_i}{C_o\,(1-z^{-3})} \tag{4.2}$$

Thus, the passband centers of the bandpass filter employing the proposed integrators are located at integer multiples of the path clock frequency $f_s/3$, where $f_s = 1/T$ is the input/output clock frequency. Three input network realizations for the proposed PNP integrator structure will be discussed here. The ***Type I*** input coupling capacitor network and its timing diagram are shown in Fig. 4.5a. From the clock phase diagram and Fig. 4.4 it can be seen that only ***two*** circulating delay lines exist in this circuit given by

$$C_{o1} \rightarrow (C_{o4}) \rightarrow C_{o3} \rightarrow (C_{o2}) \rightarrow C_{o1} \ .....$$
$$C_{o3} \rightarrow (C_{o2}) \rightarrow C_{o1} \rightarrow (C_{o4}) \rightarrow C_{o3} \ .....$$

The capacitors shown without parentheses are used for integrating charges, while the capacitors in parentheses are used only as storage elements.

As outlined, during one full cycle of operation lasting $6T$ each branch of the block Y is used three times for transferring the signal charge (i.e., with the frequency $f_{N1} = 1/2T = f_s/2$). Thus, any mismatches of capacitors and switches causing asymmetry between the paths will result in clock feedthrough noise peaks at frequencies $kf_{N1} = kf_s/2$ where $k = 0,1,2,...$ Therefore, the main passband centered at the frequency $f_s/3$ is not affected by the clock feedthrough noise, and only $N(N+1)/2$ clock periods (i.e., half of the ones required for circulating-delay PNP integrators) are needed for performing a charge updating operation.

The ***Type II*** input coupling capacitor network and its timing diagram are shown in Fig. 4.5b. This network consists of two parallel input paths which operate in a push-pull manner. An inspection of the SC circuit and its clock phase diagram shows that during one full cycle of operation (of duration $12T$) each branch of the block Y is employed three times with a frequency $f_{N1} = 1/4T = f_s/4$. There are therefore *four* circulating delay lines in the Type II circuit with charge routes given by

$$C_{o1} \rightarrow C_{o4} \rightarrow C_{o3} \rightarrow C_{o2} \rightarrow C_{o1} \ .....$$
$$C_{o2} \rightarrow C_{o1} \rightarrow C_{o4} \rightarrow C_{o3} \rightarrow C_{o2} \ .....$$
$$C_{o3} \rightarrow C_{o2} \rightarrow C_{o1} \rightarrow C_{o4} \rightarrow C_{o3} \ .....$$
$$C_{o4} \rightarrow C_{o3} \rightarrow C_{o2} \rightarrow C_{o1} \rightarrow C_{o4} \ .....$$

For ideal operation, the conditions $C_{o1} = C_{o2} = C_{o3} = C_{o4} = C_o$ and $C_{i1} = C_{i2} = C_i$ should be satisfied.

Any mismatches between the feedback and input capacitors will result in clock feedthrough noise peaks at frequencies where $kf_{N1} = kf_s/4$ where $k = 0, 1, 2,....$ Again, it should be noted that the filter has out-of-band noise peaks, although the number of the noise peaks in the $0 \sim f_s$ frequency range is doubled. Additionally, this circuit requires only $N(N+1)/4$ clock periods for each charge updating operation. Thus, it is *four* times faster than the circulating-delay PNP circuits.

The ***Type III*** input network and its timing diagram are shown in Fig. 4.5c. It has the same circuit diagram as the Type I input network, but a different clocking scheme. It combines the lower speed of the Type I circuit with the out-of-band noise peak behavior of the Type II circuit. The main advantage of this circuit is such that during $\phi_2 = 1$ the charges in the opamp feedback capacitors remain unchanged. Therefore, this period can be used to produce an error-correction voltage for the compensation of opamp offset voltage and finite gain [71].

4.2.2. Differential Structures

Because the error voltages which are generated by mechanisms such as clock feedthrough, charge injection are canceled to the first degree in differential circuits, differential integrators are needed to achieve the demands of accurate and sensitive designs. Fig. 4.6 depicts the structure and the timing diagram of the differential version of the single-ended integrator shown Fig. 4.4. The Type I input capacitor arrangement is also used here. The mode of operation is identical to the one of single-ended version. Symmetry of circuitry and layout is essential to maintain clock feedthrough and charge injection error voltages as common-mode signals. All feedback and storage capacitors in addition to the input capacitors along with the parasitic capacitors on the signal path must be matched. If the conditions $C_{o1} = C_{o2} = C_{o3} = C_{o4} = C_o$, $C_{o1}' = C_{o2}' = C_{o3}' = C_{o4}' = C_o$ and $C_{i1} = C_{i2} = C_i$ are met, the transfer function is the same in (4.2).

4.3. PNP SC Integrator Structures Based on the $z \rightarrow -z^N$ Transformation

4.3.1. Single-Ended Structures

Fig. 4.7a shows the novel single-ended stray insensitive 2-path integrator. In this scheme, the topology of the feedback is such that during phase *'b'* the operation gives the negative of the output voltage V_o with respect to phase *'a'*. It allows the realization of a stray insensitive circuit with a voltage transfer function given by

$$\frac{V_o(z)}{V_i(z)} = -\frac{C_i}{C_o(1+z^{-2})} \qquad (4.3)$$

if $C_{o1} = C_{o2} = C_{o3} = C_{o4} = C_{o5} = C_o$ and $C_{i1} = C_{i2} = C_i$.

From the timing diagram in Fig. 4.7b, it can be observed that one full cycle of operation requires a time interval $6T$, where T is the sampling period. Because the main

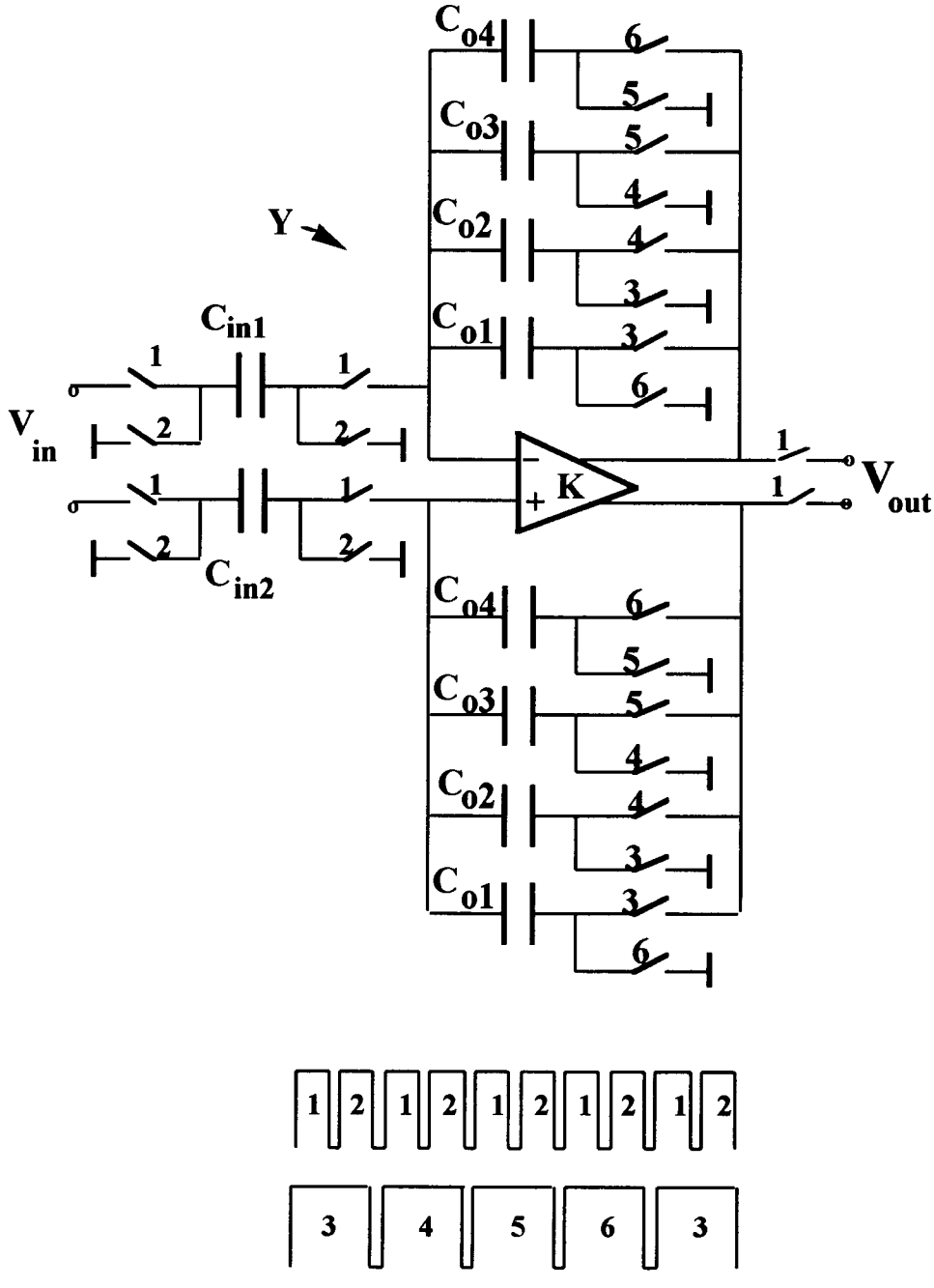


Fig. 4.6. Differential version of the pseudo-3-path integrator in Fig. 4.4.

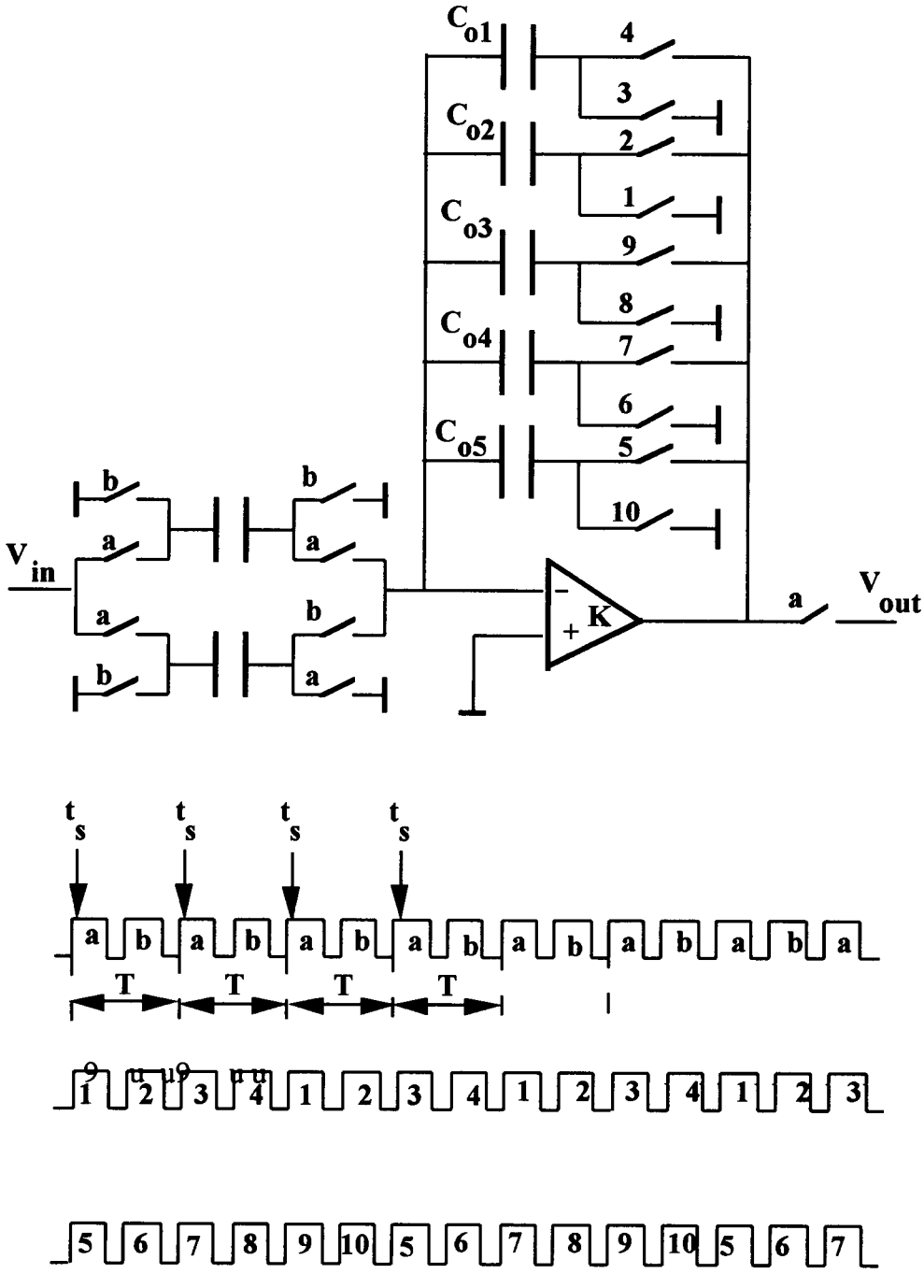


Fig. 4.7. Single-ended stray-insensitive cell for $z \rightarrow -z^{2}$ transformation.

passband is centered at the frequency $f_c = 1/4T$, the clock feedthrough noise spectra at the frequencies $f_N = k/6T$ (k = 0, 1, 2,...) do not affect the signal. This property of the circuit is necessary for any (ultra-narrow) passband application. The circuit of Fig. 4.7a is not offset free in principle but an error-correction voltage can be easily produced for the compensation of opamp finite gain and offset voltage [71]. Using the above concept, it is possible to realize other SC circuits whose voltage transfer functions can be written as the product of the $H(z)$ and $\pm z^{-1}$ and $\pm z^{-2}$.

4.3.2. Differential Structures

One obvious disadvantage of the single-ended PNP integrator discussed in the Section 4.3.1 is the large number of non-overlapping phases which are required. The reason for this is that the polarity of the charge packages has to be reversed to obtain the $1 + z^{-2}$ denominator of the transfer function. Differential structures offer an inherent solution to this problem. By simply connecting terminals of a capacitor to the opposite inputs of the differential opamp in the next clock phase, the charge polarity can be reversed. In Fig. 4.8 a differential 2-path PNP integrator and its timing diagram is shown [53]. If $C_{A1} = C_{B1} = C_{C1} = C_{A2} = C_{B2} = C_{C2} = C_o$ and $C_{i1} = C_{i2} = C_i$, the transfer function is the same as in (4.4). One full cycle of operation is completed a time interval $3T$, where T is the sampling period. Similar to the single-ended structure, the main passband is centered at the frequency $f_c = 1/4T$, the clock feedthrough noise spectra at the frequencies $f_N = k/3T$ (k = 0, 1, 2,...). In one clock phase (e.g. during $\phi_2 = 1$), an additional capacitor can be configured to store the offset voltage and be used to compensate for it in the next clock phase. Two novel integrators which address these problems are discussed further in Chapter 5 in the design example of 6th order bandpass delta-sigma modulators.

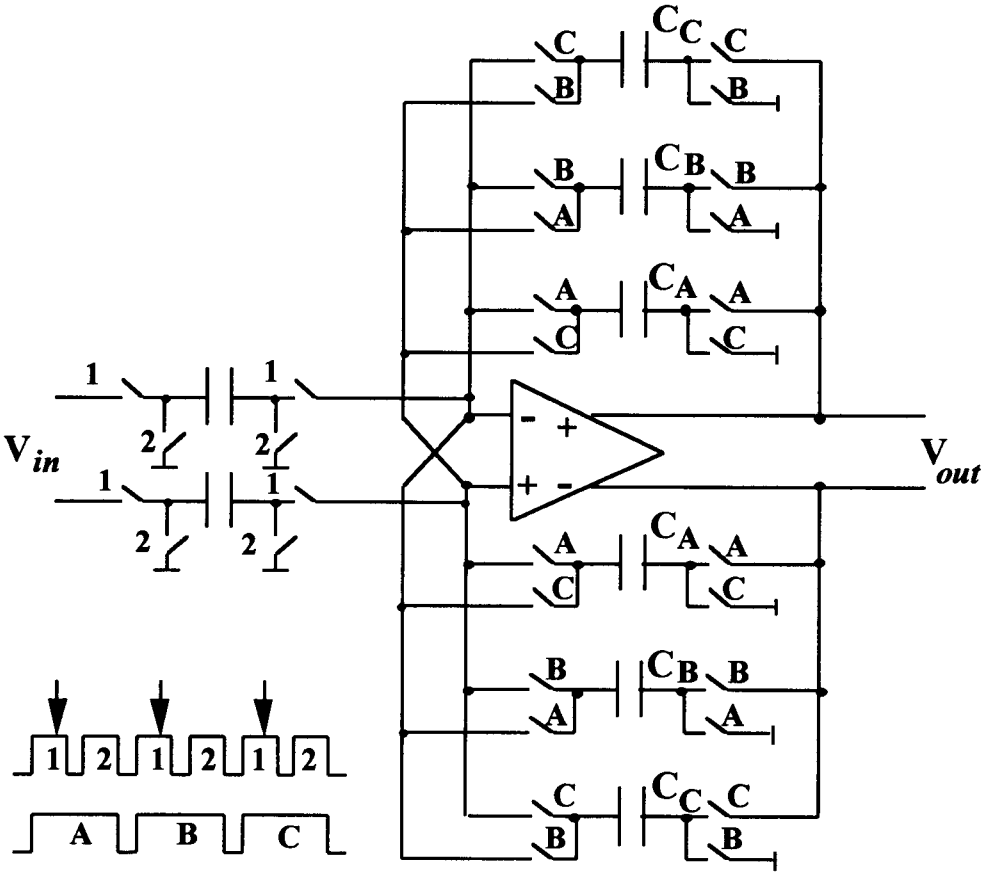


Fig. 4.8. Differential pseudo-2-path integrator cell.

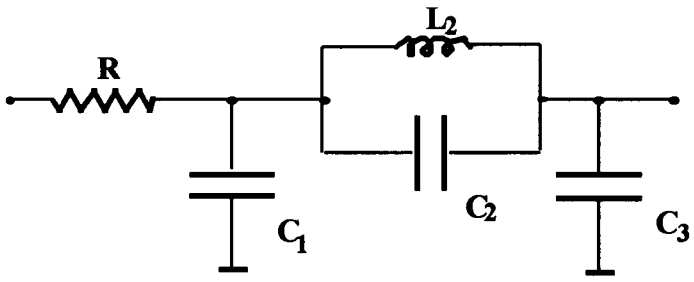


Fig. 4.9. Elliptic 3rd order lowpass prototype.

4.4. Filter Design Examples

To confirm the theory, various elliptic *N*-path bandpass filters were designed and simulated in SWITCAP2. The lowpass prototype shown in Fig. 4.9 is used as a starting point. The capacitor and inductor values are selected as such that the filter has a passband ripple of 0.178 dB and a minimum stopband attenuation of 31.47 dB. The sampling frequency was selected as 6 kHz. The single-ended and differential PNP integrators discussed in Sections 4.2 and 4.3 were used in transforming the lowpass filter to a bandpass one . In the simulated filters, the switches were replaced by more realistic models as suggested in Fig. 3-6 in SWITCAP manual [72].

The simulated gain response of the filter containing integrators shown in Fig. 4.4 with a DC opamp gain of 50 dB is shown in Fig. 4.10 and the clock feedthrough noise spectra obtained with Type I, II and III input circuits are depicted in Fig. 4.11a, b and c, respectively. In the simulations the asymmetry between the two circulating paths were included by randomly selecting capacitors ±2.5 % away from their nominal values. As it can be observed from Fig. 4.11 that Type I input arrangement results in noise peaks at

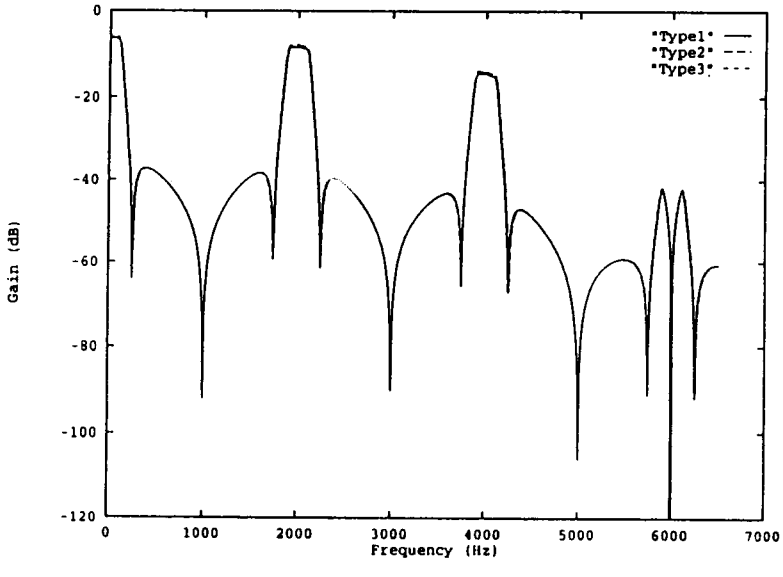


Fig. 4.10. Simulated gain responses of SC filters with Type I, Type II and Type III integrators (opamp DC gain = 50 dB)

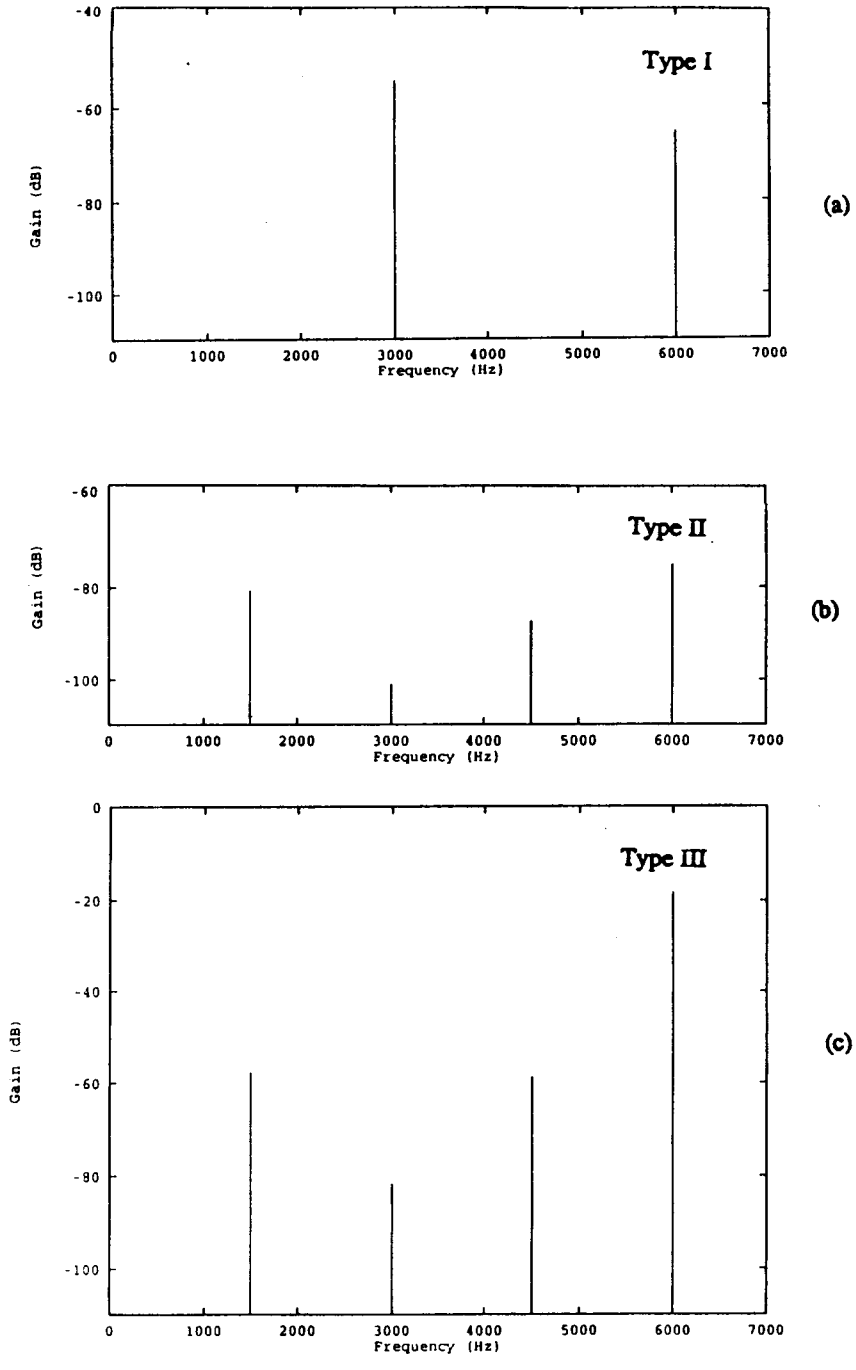
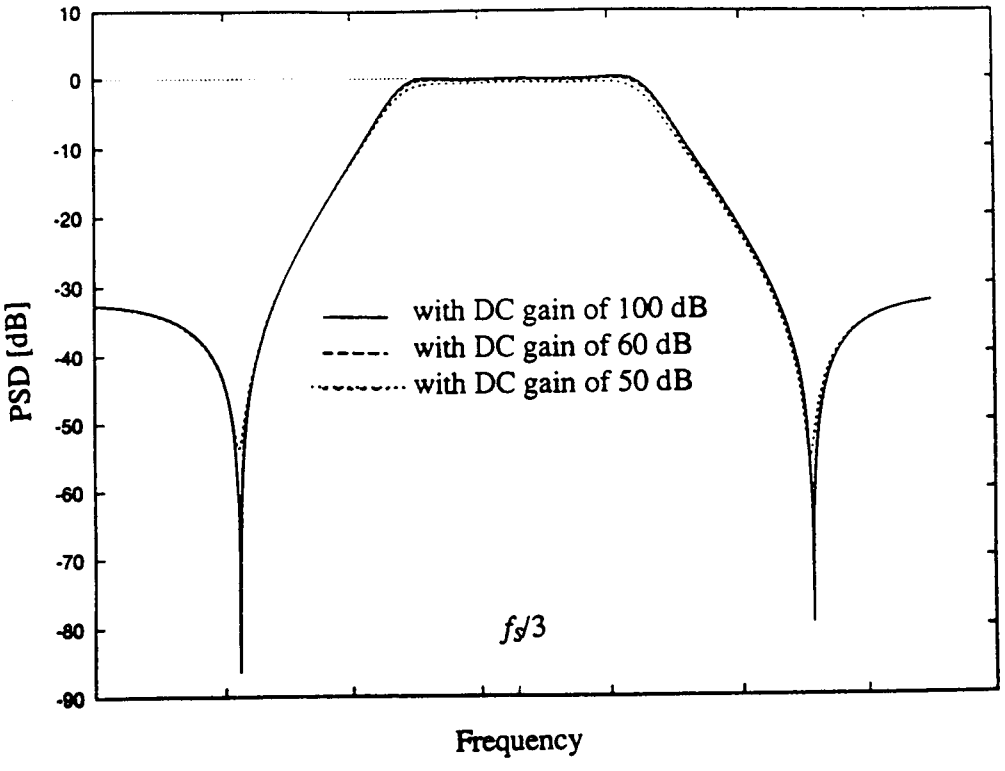
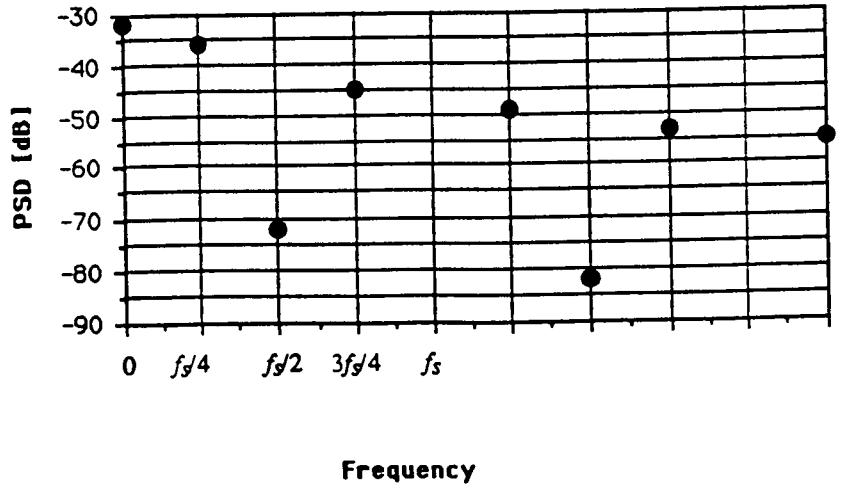


Fig. 4.11. (a) Simulated clock feedthrough noise spectrum of the SC filter with Type I integrators. (b) Simulated clock feedthrough noise spectrum of the SC filter with Type II integrators. (c) Simulated clock feedthrough noise spectrum of the SC filter with Type III integrators.



(a)



(b)

Fig. 4.12. (a) Simulated gain responses of the SC filter with the integrator in Fig. 4.6.
(b) Simulated clock feedthrough noise spectrum of the same filter.

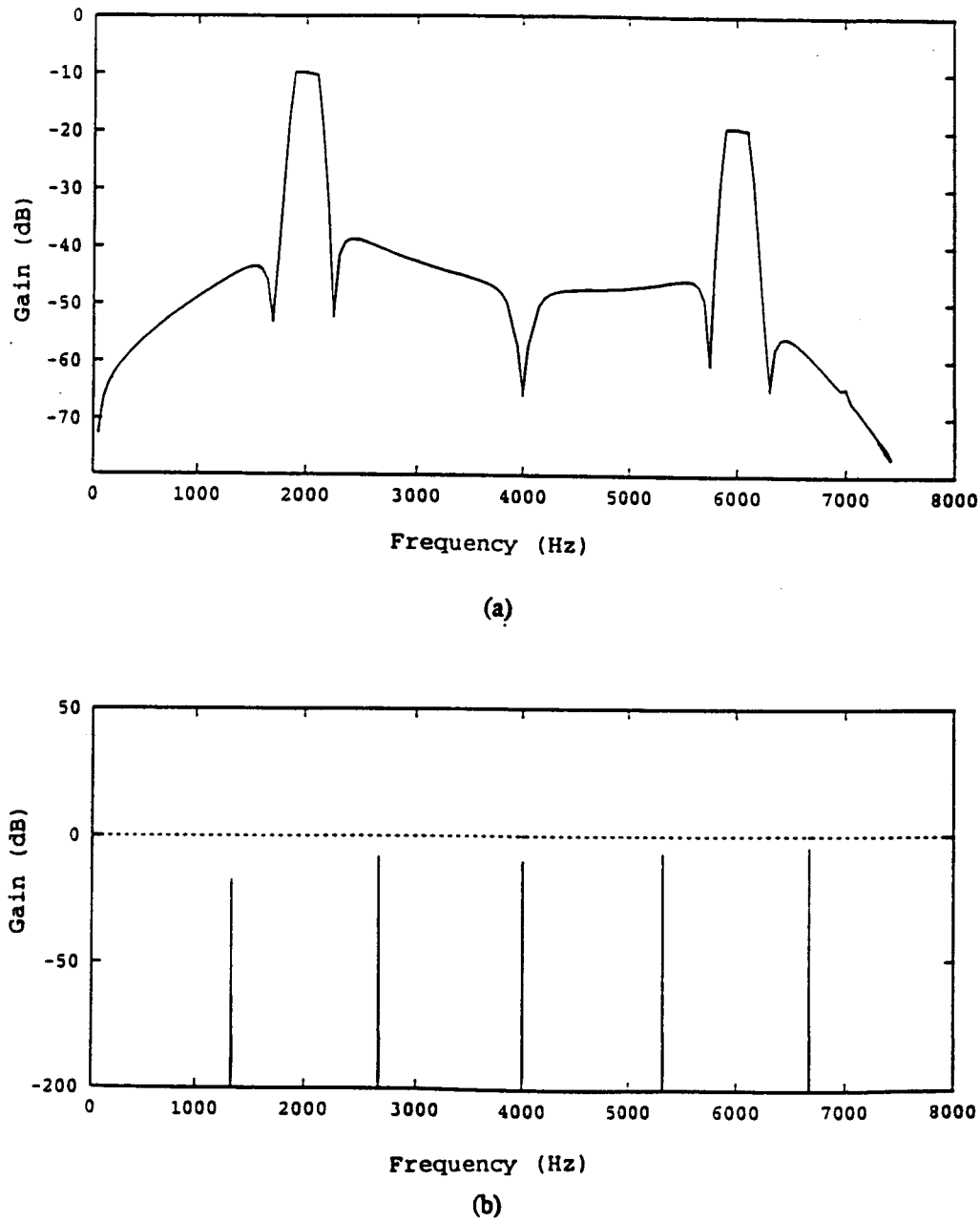


Fig. 4.13. (a) Simulated gain responses of the SC filter with the integrator in Fig. 4.7.
(b) Simulated clock feedthrough noise spectrum of the same filter.

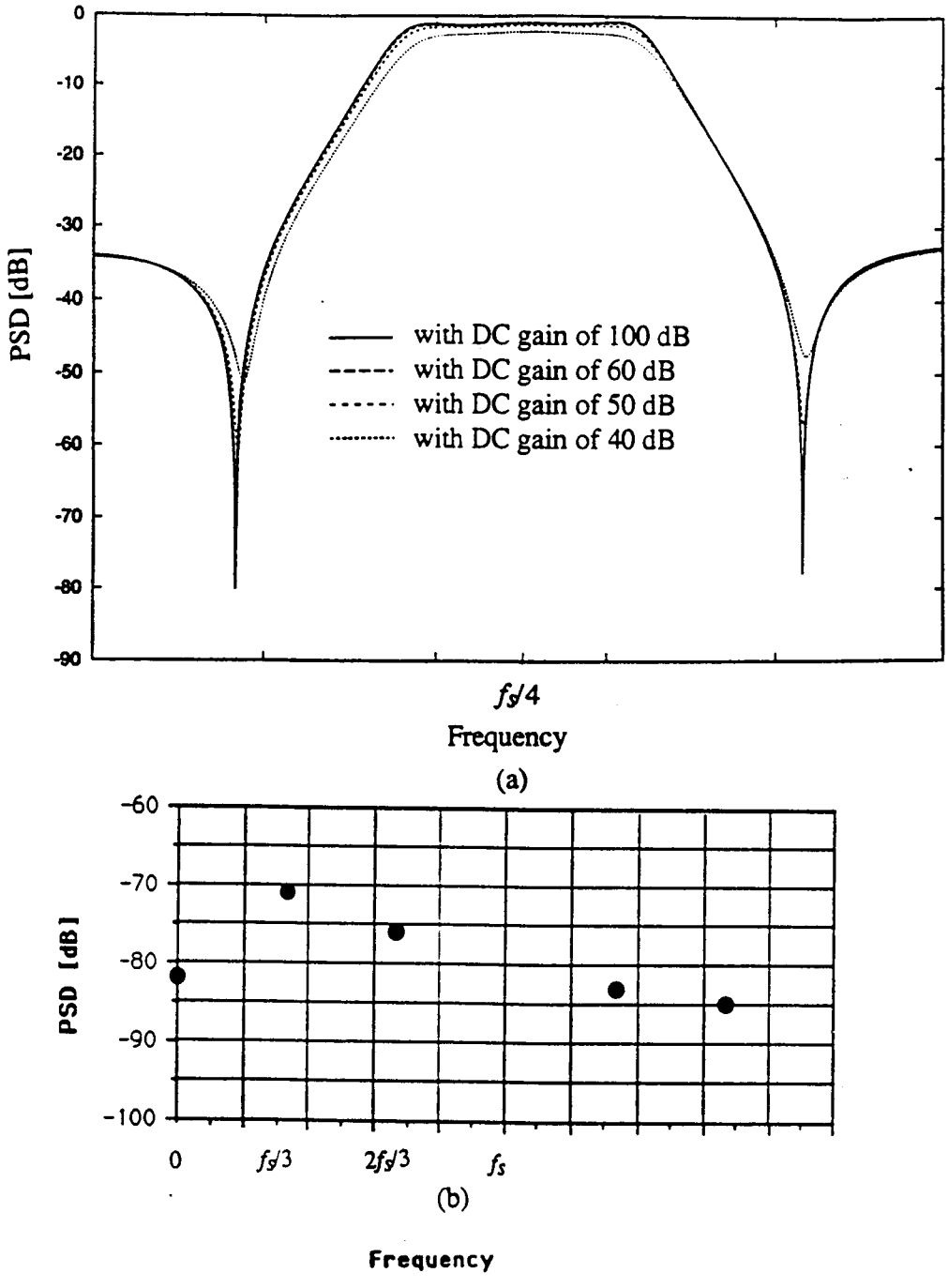


Fig. 4.14. (a) Simulated gain responses of the SC filter with the integrator in Fig. 4.8.
(b) Simulated clock feedthrough noise spectrum of the same filter.

$kf_S/2$, Type II and Type III arrangements generate noise peaks at $kf_S/4$, all away from the passband centered at $f_S/3$.

Fig. 4.12a shows the simulated gain response of the filter designed with the differential 3-path integrator in Fig. 4.6 with DC opamp gains of 50 dB to 100 dB and capacitor mismatches ±1% of their nominal values. The clock feedthrough noise peaks occur at $kf_S/4$ similar to the single-ended case.

The simulated gain response of the filter designed with the differential 3-path integrator in Fig. 4.7a is depicted in Fig. 4.13a. It is assumed that DC opamp gain is 50 dB and the capacitors are mismatched randomly by ±2.5% of their nominal values. The clock feedthrough noise peaks occur at $kf_S/3$ as they are shown in Fig. 4.14b.

In Fig. 4.14a the simulated gain response of the filter with integrators in Fig. 4.8 with DC opamp gains of 40 dB to 100 dB is shown. The capacitor mismatches are assumed to be ±1% of their nominal values. As it can be observed from Fig. 4.14b, the clock feedthrough noise peaks occur at $kf_S/3$ similar to the single-ended case.

These results point out the most desired property of the SC filter: The clock feedthrough noise peaks occur outside of the main passband. In this sense, the circuit is similar to the classical PNP filter, yet two times faster.

4.5. Conclusions

In this chapter it has been shown that the proposed [76] PNP integrators are very attractive with their simplicity, immunity to the clock feedthrough noise, and speed improvements. In addition to offering new solutions to SC bandpass filter realizations, these integrators can be useful in designing multiplexed lowpass, and bandpass sigma-delta modulation systems. The finite-gain opamp compensation techniques discussed in Chapter 5 can improve the performance of these systems while reducing the required opamp DC gain.

5. BANDPASS DELTA-SIGMA MODULATORS WITH NOVEL PNP INTEGRATORS

5.1. Introduction

Bandpass delta-sigma modulators have been introduced for the realization of band-reject shaping of quantization noise. It was shown theoretically that bandpass delta-sigma modulation can result in a high signal-to-noise ratio (*SNR*) at a relatively low sampling frequency in comparison to lowpass delta-sigma modulation [44], [45]. Data converters based on bandpass delta-sigma modulation has become a research focus in communications because of their inherent linearity and low sensitivity to component variations. Moreover, the in-phase and quadrature components (I and Q) of their output signal are easy to separate [44], [45]. In this chapter, a new method of implementation of bandpass delta-sigma A/D converters is presented [52]. It utilizes Pseudo-*N*-Path (PNP) switched-capacitor (SC) integrator structures that avoid noise peaks in the main passband such as the ones introduced in Chapter 4.

A multi-bit 6^{th} order modulator and a 6^{th} order two-stage cascaded modulator were designed as examples. Both schemes appear to be very effective for the realization of the narrow-band bandpass delta-sigma modulators needed for communication applications, especially if the proposed PNP SC integrators are employed.

5.2. Pseudo-*N*-Path Bandpass Delta-Sigma A/D Converters

Pseudo-*N*-path SC filters were introduced originally for narrow-band filters [66]. This concept can be extended to bandpass delta-sigma modulation. In principle, lowpass delta-sigma modulation can be converted to bandpass delta-sigma modulation by using a spectral transformation such as $z \rightarrow z^{N_1}$ or $z \rightarrow -z^{N_2}$ where N_1 and $N_2 \geq 2$ are integers.

In such a way, a discrete-time prototype lowpass delta-sigma modulator can be transformed into a bandpass delta-sigma modulator by replacing each memory element by an appropriate N-path delay line. Since the commonly used noise transfer function realized by lowpass delta-sigma modulator is $(1 - z^{-1})^n$, the bandpass delta-sigma modulation noise-shaping function will be either

$$H_1(z) = (1 + z^{-N_1})^n \tag{5.1a}$$

or

$$H_2(z) = (1 - z^{-N_2})^n \tag{5.1b}$$

where $n = 1, 2, 3,...$ is the order of the lowpass delta-sigma modulator, and nN_1 or nN_2 is the order of the bandpass delta-sigma one.

A detailed analysis based on (5.1a) and (5.1b) indicates that in both functions unit-circle noise transmission zeros are realized. For $H_1(z)$, the zeros are at

$$exp[-j(2k+1)\,\pi/N_1], \qquad k = 0, 1, 2,..., N_1-1$$

for $H_2(z)$, they are at

$$exp[-j\,2(k+1)\,\pi/N_2], \qquad k = 0, 1, 2,..., N_2-1.$$

To obtain an easy separation of I and Q, the band center frequency f_c is usually selected as $f_s/4$, where f_s is the input sampling ratio. Then, noise transmission zeros are needed at $z_{1,2} = \pm j$. This can be achieved for $H_1(z)$ if $N_1 = 2$, and for $H_2(z)$ if $N_2 = 4$ is chosen. Thus, there exist a 2-path noise-shaping function $H_1(z) = (1 + z^{-2})^n$ or a 4-path one $H_2(z) = (1 - z^{-4})^n$. In Fig. 4.1, for $n = 1$ the magnitudes of the transfer function $H_1(z) = 1 + z^{-2}$ and $H_2(z) = 1 - z^{-4}$ ($z = e^{j2\pi fc/f}$) are plotted to show the properties of

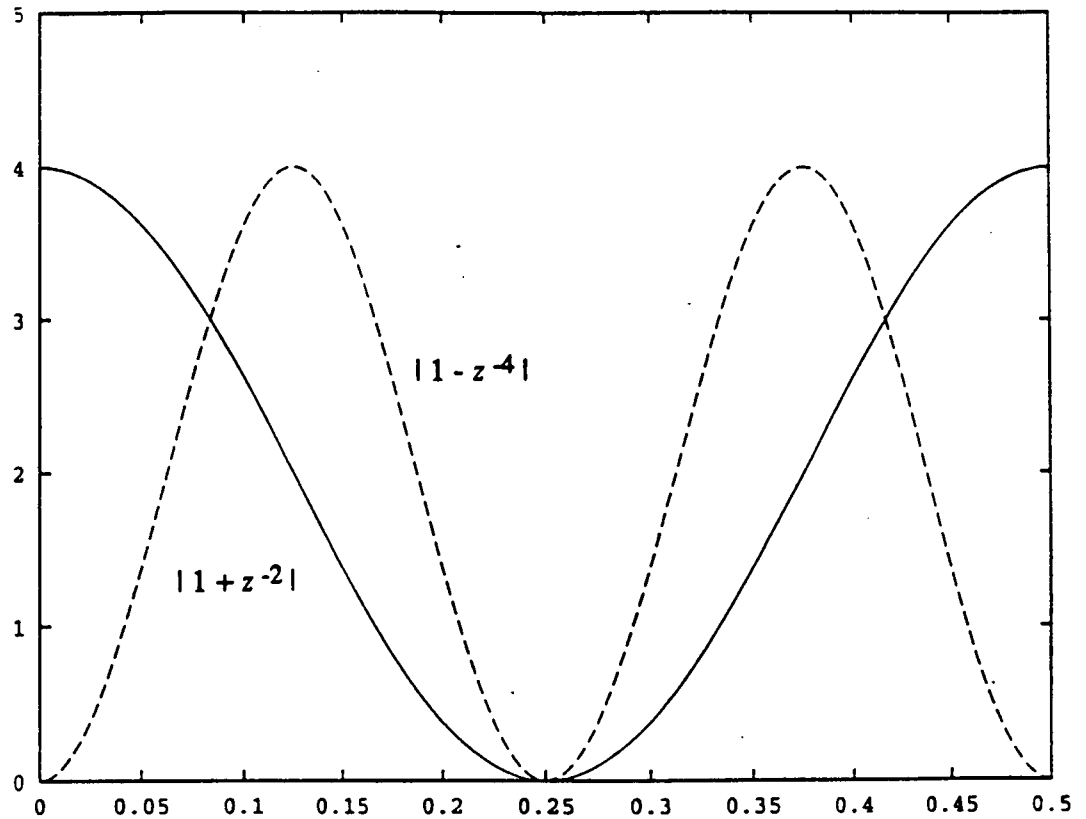


Fig. 5.1. Magnitudes of the transfer functions $H_1(z) = 1 + z^{-2}$ and $H_2(z) = 1 - z^{-4}$.

both transformations. The plots in Fig. 5.1 demonstrate that in the bandwidth of interest around f_c, a wider useable passband can be obtained by using the 2-path $z \rightarrow -z^{N_2}$ transformation.

It can be also observed from these plots that the *SNR* performance of the bandpass delta-sigma modulation depends critically on the exact location f_c of the coincident noise transmission zeros. The major advantage of the N-path configuration is that the condition $f_c = f_s/4$ is satisfied exactly due to the realization of the $z \rightarrow \pm z^N$ transformation via frequency division.

5.3. Design Example-I: A 6th Order Bandpass Delta-Sigma Modulator with Multi- and Single-Bit Feedback Architecture

The 6th order bandpass delta-sigma A/D converter shown in Fig. 5.2 can be realized by using the PNP integrators in Fig. 4.5. The structure employs a combined single-bit/multi-bit feedback loop which achieves a multi-bit resolution . The noise generated by the nonlinearity of the multi-bit D/A converter is attenuated by the first two noise shaping stages of the system [41]. The scaling factors of 0.5 are introduced to prevent overloading the quantizer which can make the feedback loop unstable. Scaling allows the single-bit quantizer to have a full scale output swing $\pm V_{ref}$, which is the same as the swing of the multi-bit quantizer. Fig. 5.3 shows the amplitude histograms for the three integrator outputs. It verifies that under random input signal conditions, the outputs have about the same maximum swings, and they all have a small variance without long "tails" in their distributions. For robust stability, this is very advantageous. Also, the third stage uses a multi-bit feedback signal; this helps improve the stability and also gives the whole system a multi-bit resolution. Assuming a 4-bit internal quantizer, the z-transform representation of the output of the system is

$$Y = [\, X/4 - E_4 (1 + z^{-2})^3 + \Delta_4 (1 + z^{-2})^2] \, z^{-2} \qquad (5.3)$$

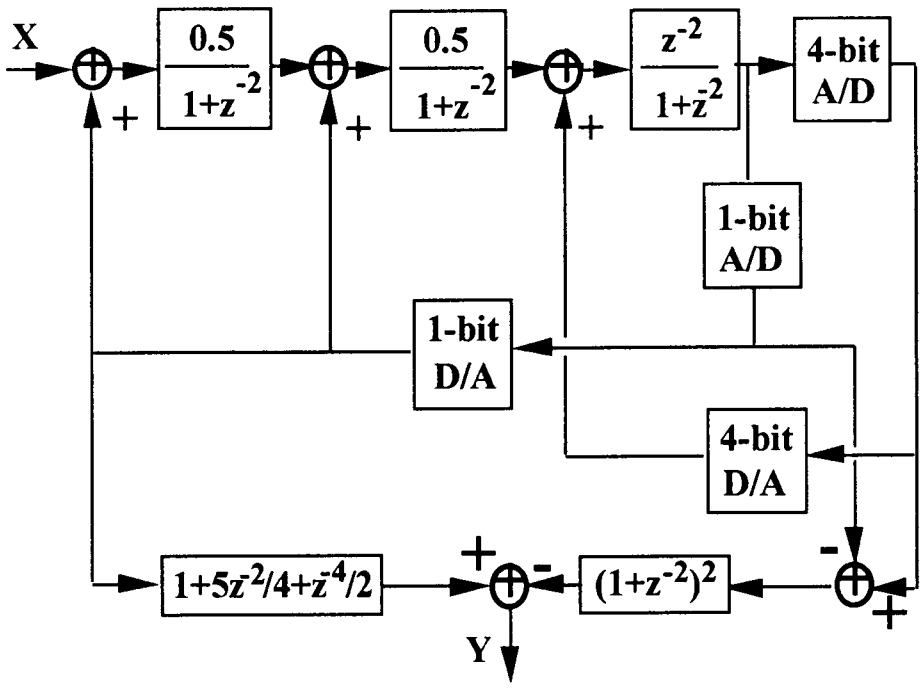


Fig. 5.2. The block diagram of a 4-bit 2-path 6th order bandpass delta-sigma modulator.

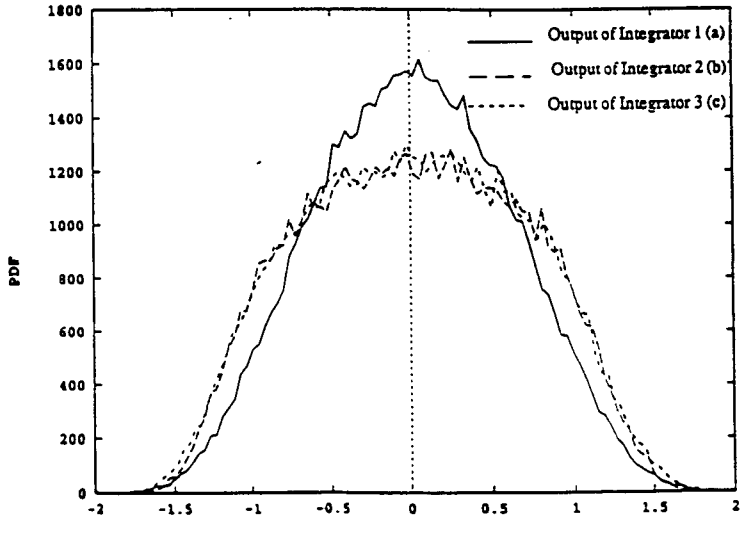


Fig. 5.3. The amplitude histograms (a), (b), (c), for the output of the first, second, and third integrator, respectively.

where $X(z)$ is the z-transform of the sampled input x, E_4 is the quantization error generated by the 4-bit ADC, and Δ_4 is the error signal caused by the nonlinearity of the 4-bit DAC. Fig. 5.4 shows the output spectrum for a sinusoidal input signal. The *SNR* versus input level characteristics obtained by simulations of the system are plotted in Fig. 5.5. To calculate *SNR*, the time difference equations were simulated, and the frequency spectrum of the system for a particular input level was extracted using FFT algorithms with a Hann window. The signal power was calculated by detecting the single tone. The noise power was calculated by adding all the spectral components' contributions except for where the signal was located and the couple of bins around it (windowing causes the single tone to spill over to the nearby frequencies). The oversampling ratio, defined as the ratio of the sampling rate to the signal bandwidth, was assumed to be 32, and the band center was at $f_c = f_s/4$. It can be seen that for a 4-bit DAC with 6-bit accuracy the effect of the DAC nonlinearity is negligible. The bandwidth was $f_c/16$; the curves indicate a 90 dB dynamic range, corresponding to a 15-bit conversion accuracy.

5.4. Design Example-II: A 6th Order Cascaded (MASH) Bandpass Delta-Sigma Modulator with Multi- and Single-Bit Quantizers

5.4.1. Lowpass Prototype

As it has been mentioned in Section 2.4.4, cascaded modulators have been popular for their robust stability and potential for high accuracy . Fig. 5.6 shows the block diagram of a lowpass 2-stage multi-bit MASH delta-sigma modulator [77]. The input to the second delta-sigma loop is the difference between the input and the output signals of the single-bit quantizer in the first loop. Assuming that the quantization error can be treated as an additive white noise, the output of the overall system can be written in the z-domain as:

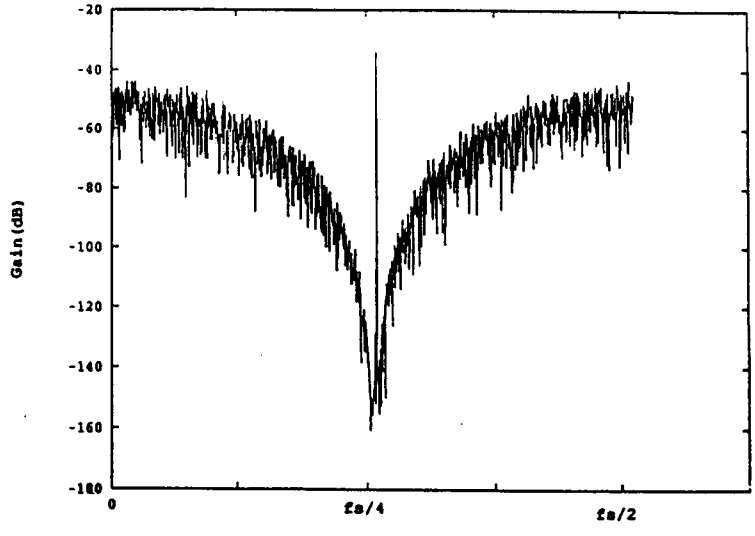


Fig. 5.4. The output spectrum of the modulator in Fig. 5.2. for a sine wave input signal.

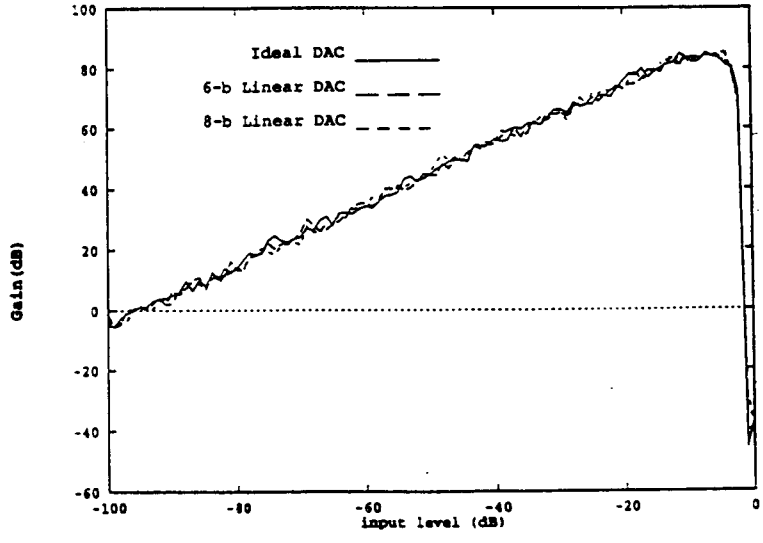


Fig. 5.5. The SNR vs. Input Amplitude curves for internal DAC, and for DACs with 6- and 8-bit linearity of the modulator in Fig. 5.2.

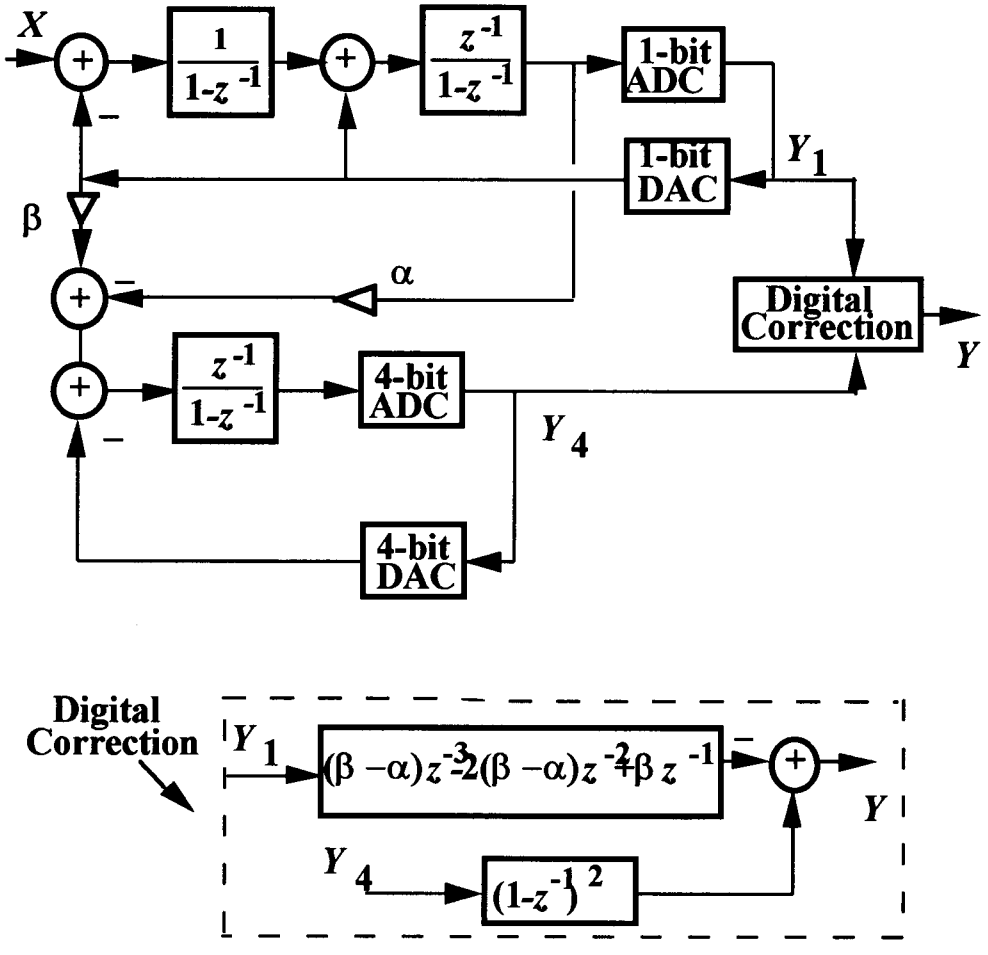


Fig. 5.6. General block diagram of a lowpass 2-stage cascaded delta-sigma modulator.

$$Y(z) = Y_1(z) + Y_n(z) = -\alpha z^{-2} X(z) + (1-z^{-1})^3 E_n(z) - z^{-1}(1-z^{-1})^2 D_n(z) \qquad (5.4)$$

Digital correction plays a significant role in obtaining the desired transfer function. The success of the cascade technique very much depends on how exactly the undesired components of the transfer function are canceled. Therefore, there are potential problems with matching the analog loop filters to each other, and to the digital FIR filters, and the finite opamp gain and capacitor mismatches can cause changes in their transfer function.

5.4.2. Lowpass-to-Bandpass Mapping

System-level simulations were performed to select between various delta-sigma modulators obtained from lowpass delta-sigma architectures using a lowpass-to-bandpass transformation. In the simulations, the integrators were assumed perfect; however, the nonlinearity of multi-bit D/A converters were included in the simulations. The results revealed that the 2-stage multi-bit cascade structure was the most suitable for this design for the goals of this study.

There are two possible lowpass-to-bandpass transformations applicable here: $z \rightarrow -z^N$ (N=2), and $z \rightarrow z^N$ (N=4). $z \rightarrow -z^N$ (N=2) shapes the quantization noise to allow a wider useable band around the center frequency. Therefore it became the choice of transformation for this design (Fig. 5.7)

The resulting delta-sigma modulator structure is shown in Fig. 5.8. Selecting

$$H_1(z) = \frac{1}{1+z^{-2}}$$

$$H_2(z) = \frac{z^{-1}}{1+z^{-2}}$$

$$H_5(z) = -[\beta z^{-2} - 2(\beta-\alpha) z^{-4} + (\beta-\alpha) z^{-6}]$$

$$H_6(z) = (1+z^{-2})^2 \qquad (5.5)$$

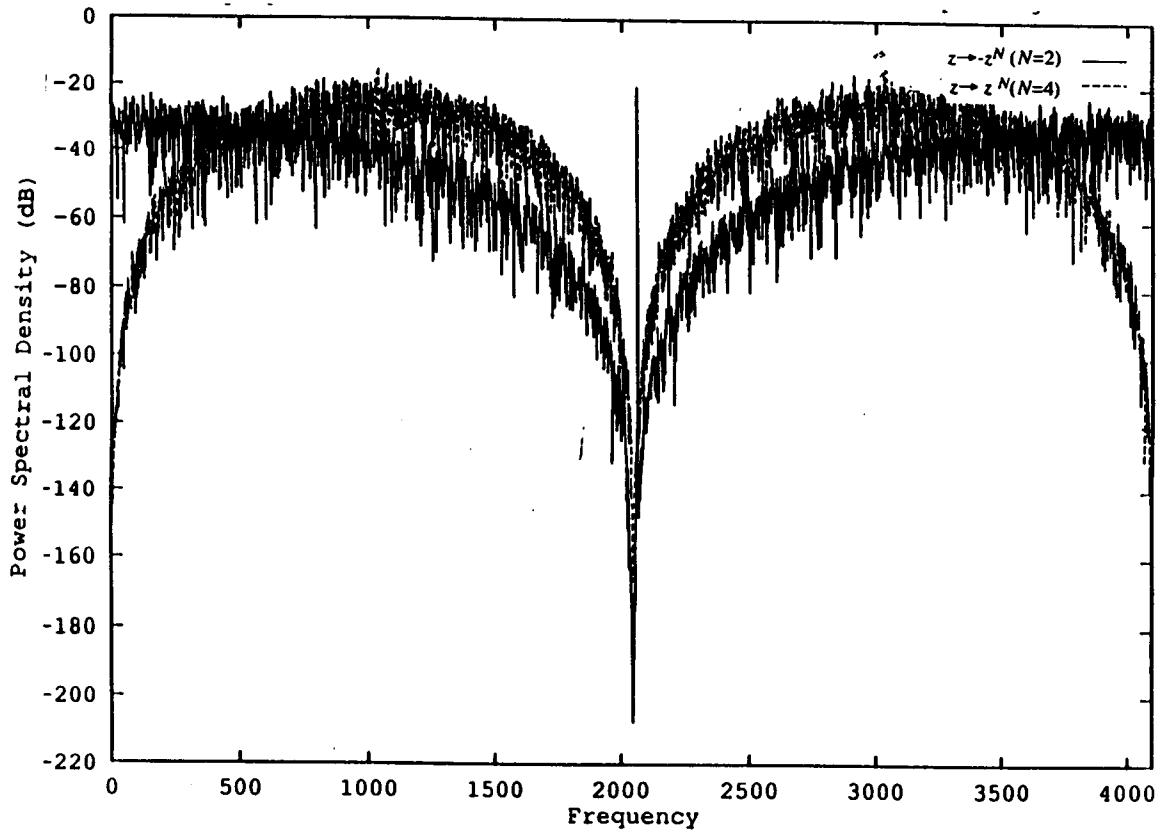


Fig. 5.7. Power spectra obtained from 2-stage multi-bit cascaded modulators with $z \rightarrow -z^N (N = 2)$, and $z \rightarrow z^N (N = 4)$ lowpass-to-bandpass transformations.

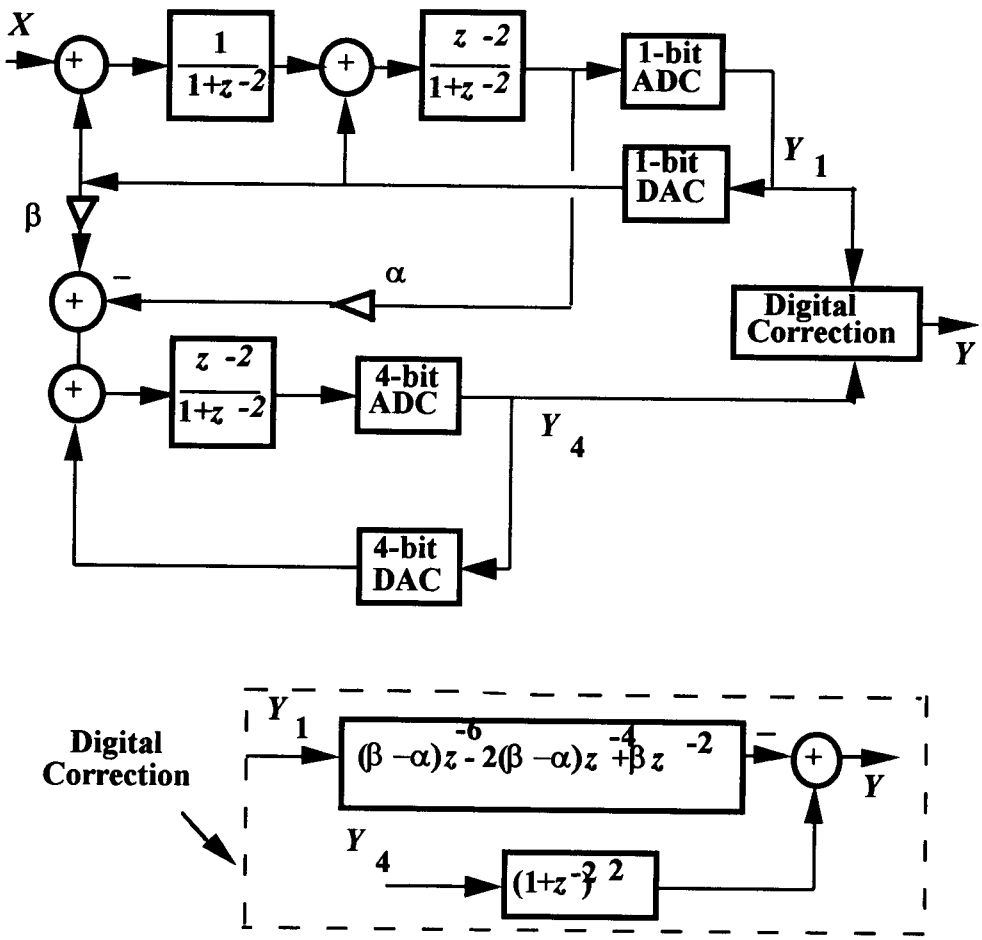


Fig. 5.8. Bandpass 6th order 2-stage multi-bit cascaded delta-sigma modulator.

and assuming that the quantization error can be modeled as an additive white noise, the output of the bandpass 2-stage multi-bit delta-sigma modulator can be written in the *z*-domain as:

$$Y(z) = Y_I(z) + Y_n(z) = -\alpha z^{-4} X(z) + (1+ z^{-2})^3 E_n(z) + z^{-2}(1+ z^{-2})^2 D_n(z) \qquad (5.6)$$

The effects of α and β gain coefficients on the overall system characteristics were also investigated. Fig. 5.9 shows the *SNR* performances of systems with various values for α and β. The 3-bit D/A is assumed to be 5-bits linear, and the *OSR* is 32. The maximum *SNR* is achieved for the $\alpha = 0.5$ and $\beta = 1$ case. Therefore, these coefficients were used in this design.

5.4.3. Pseudo-2-Path Integrators

To choose the most suitable integrator for this study among various pseudo N-path integrators [59], [74], and [75], a series of system-level simulations was performed. In this phase, additional circuit nonidealities of the circuits such as finite opamp gain, finite common-mode rejection ratio (*CMRR*), and mismatched capacitors were included in the simulations as well to get a more realistic picture. The PNP integrator shown in Fig. 4.8 fared the best in terms of its finite opamp gain requirements and the tolerances to capacitor mismatches. The *SNR* performance of the system in Fig. 5.8 with the 2-path integrators in Fig. 4.8 is shown, for various opamp DC gain (Fig. 5.10a) and for various capacitor mismatches (Fig. 5.10b) when *OSR* is 32 and *CMRR*=60 dB. From these curves, the case of DC opamp gain of 70 dB and ±0.25% mismatches were observed to be acceptable to achieve 80 dB SNR.

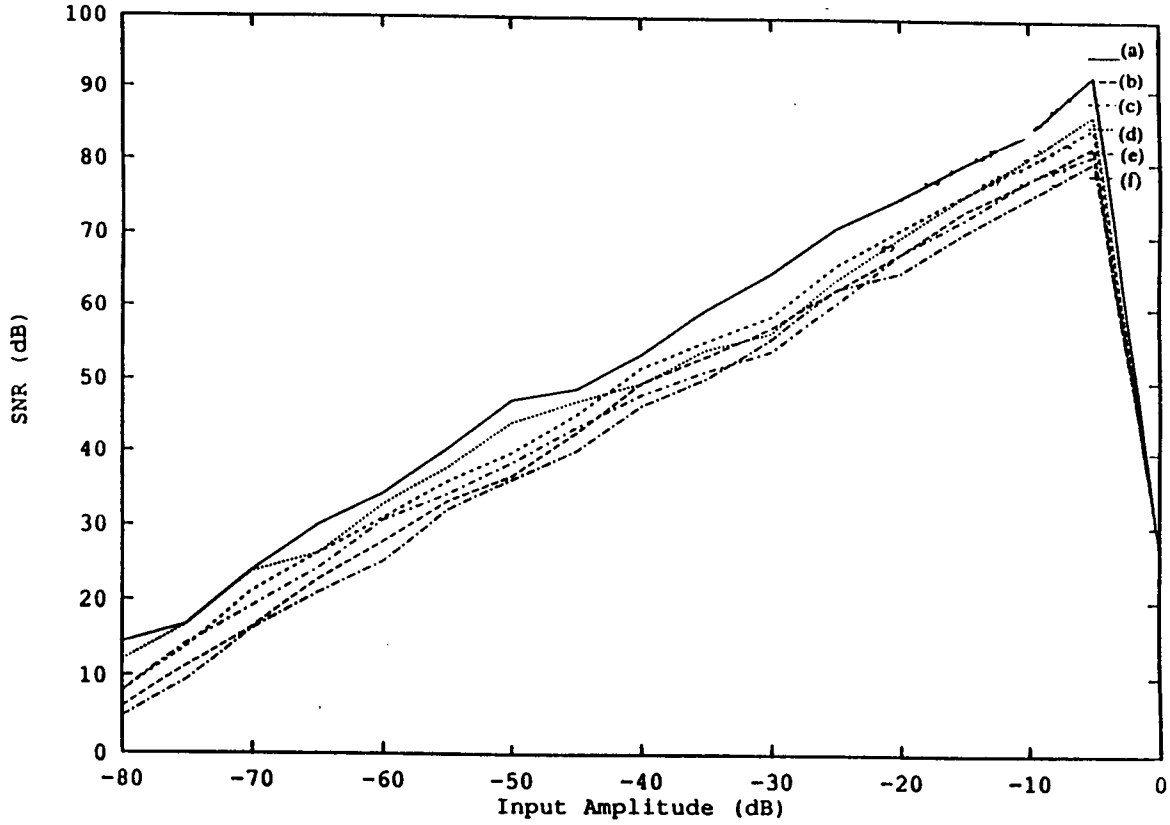
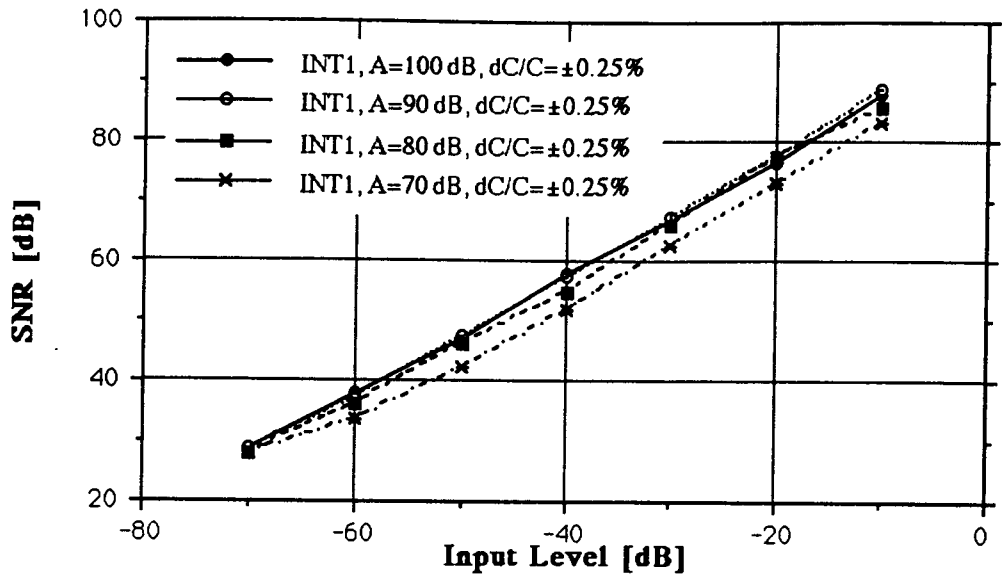
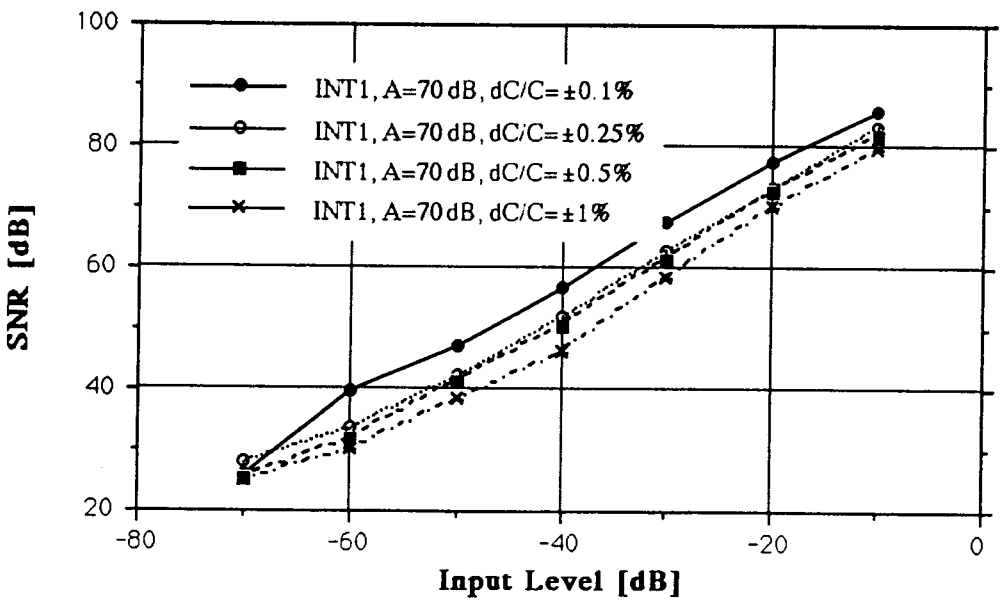


Fig. 5.9. SNR performances of the bandpass 2-stage multi-bit cascaded delta-sigma modulators (OSR = 32) with a perfect 3-bit DAC (a) $\alpha = 0.5$ and $\beta = 1$, (b) $\alpha = 0.25$ and $\beta = 1$, (c) $\alpha = 0.5$ and $\beta = 0$); and with a 5-bit linear DAC (d) $\alpha = 0.5$ and $\beta = 1$, (e) $\alpha = 0.25$ and $\beta = 1$, (f) $\alpha = 0.5$ and $\beta = 0$.



(a)



(b)

Fig. 5.10. SNR performances of the system with the 2-path integrator cell in Fig. 3.8. (OSR = 32 and with a 5-bit linear DAC).
(a) as opamp gain, A, varies (±0.25% capacitor mismatching)
(b) as capacitor mismatching varies (A=70 dB)

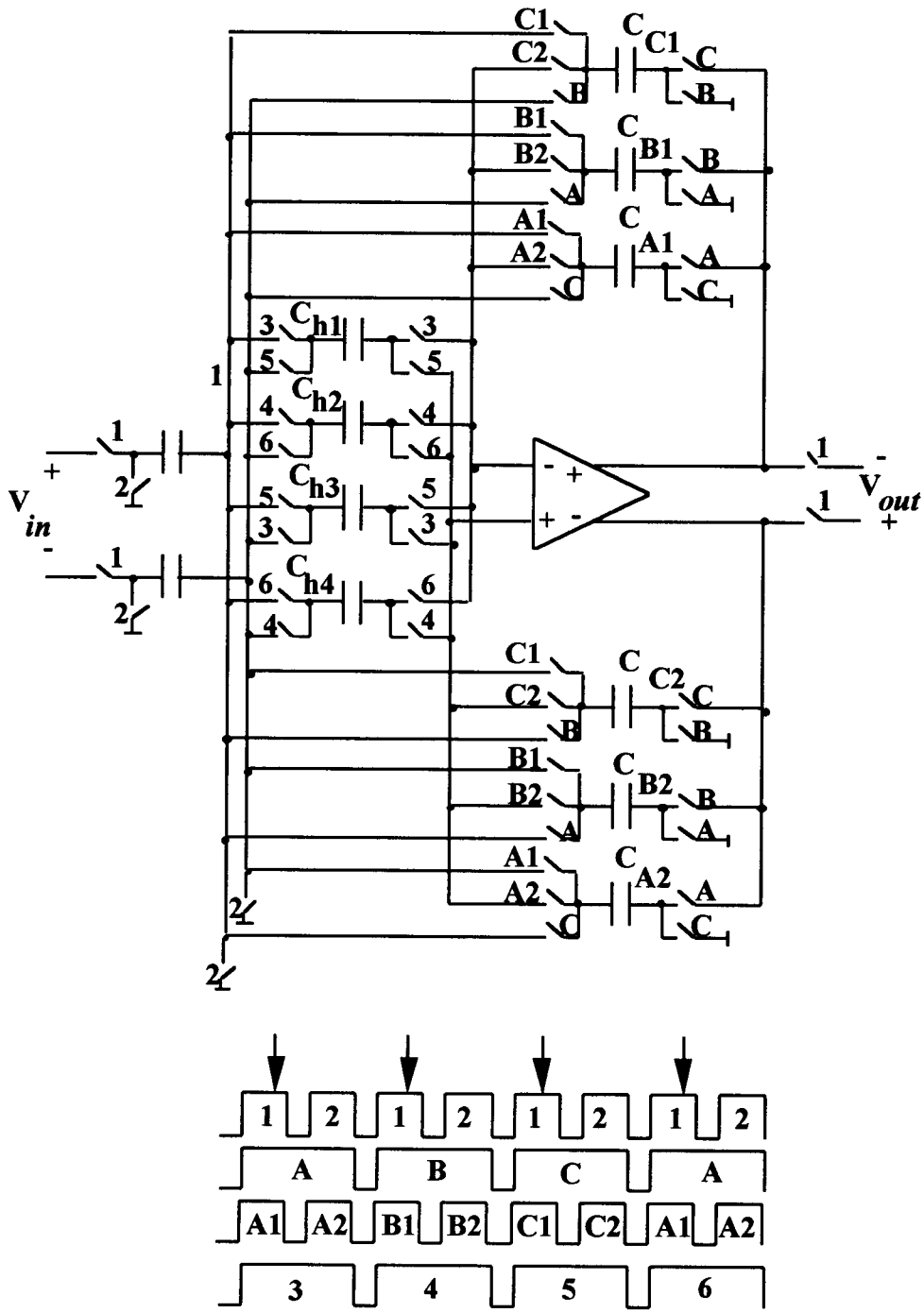


Fig. 5.11a. Finite-gain-compensated differential pseudo-2-path integrator (2pc1).

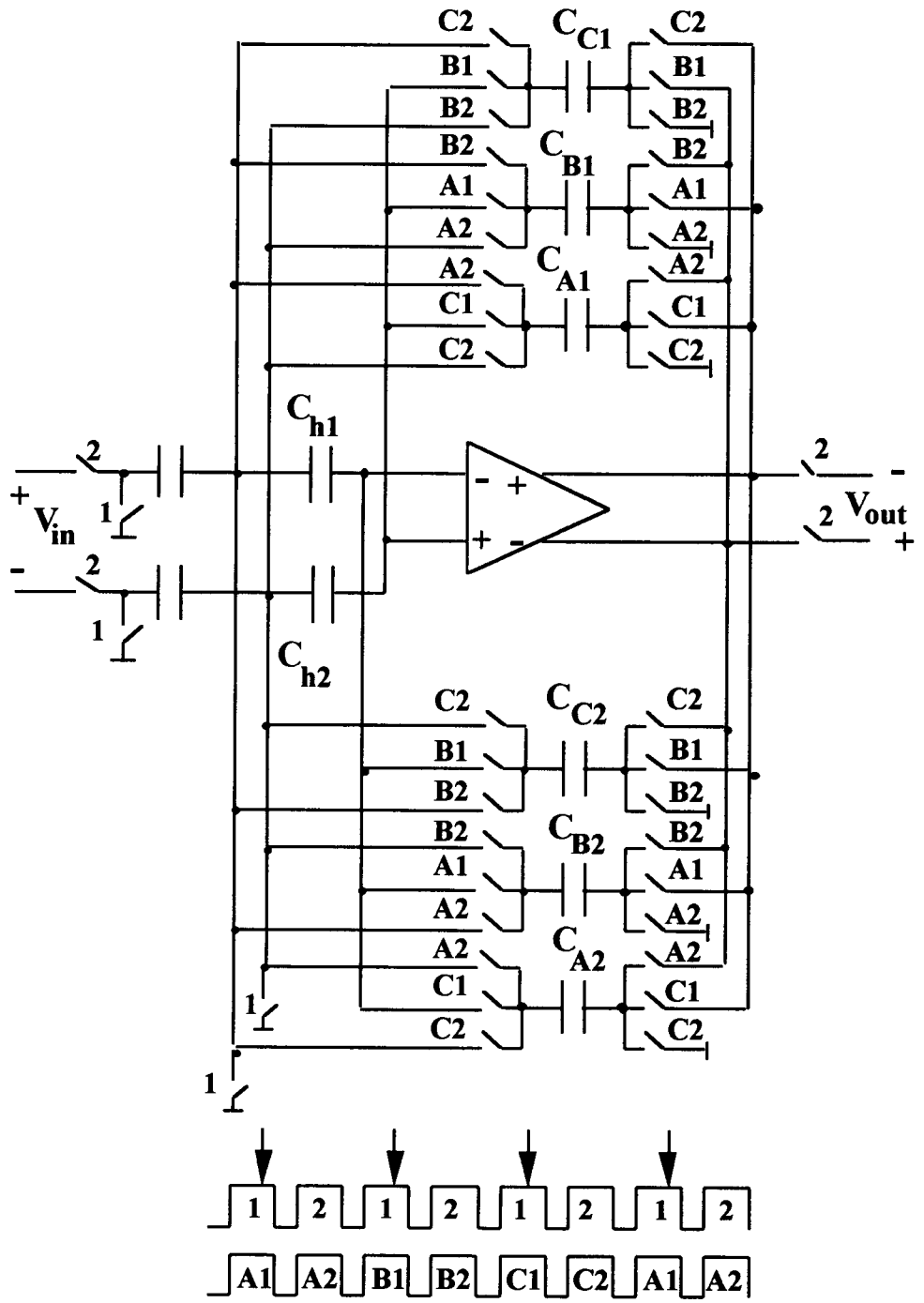
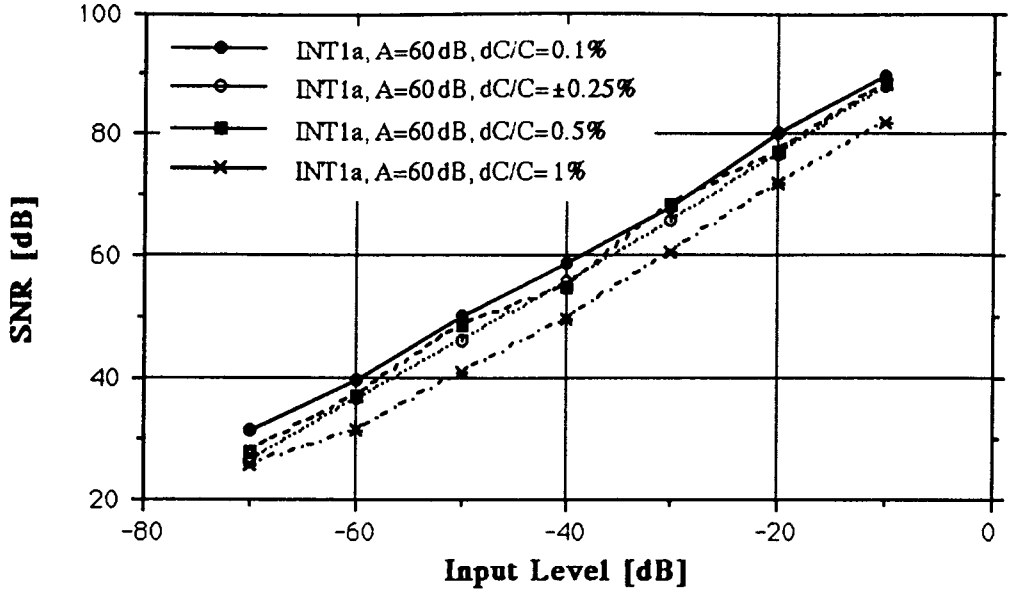


Fig. 5.11b. Finite-gain-compensated differential pseudo-2-path integrator (2pc2).



(a)

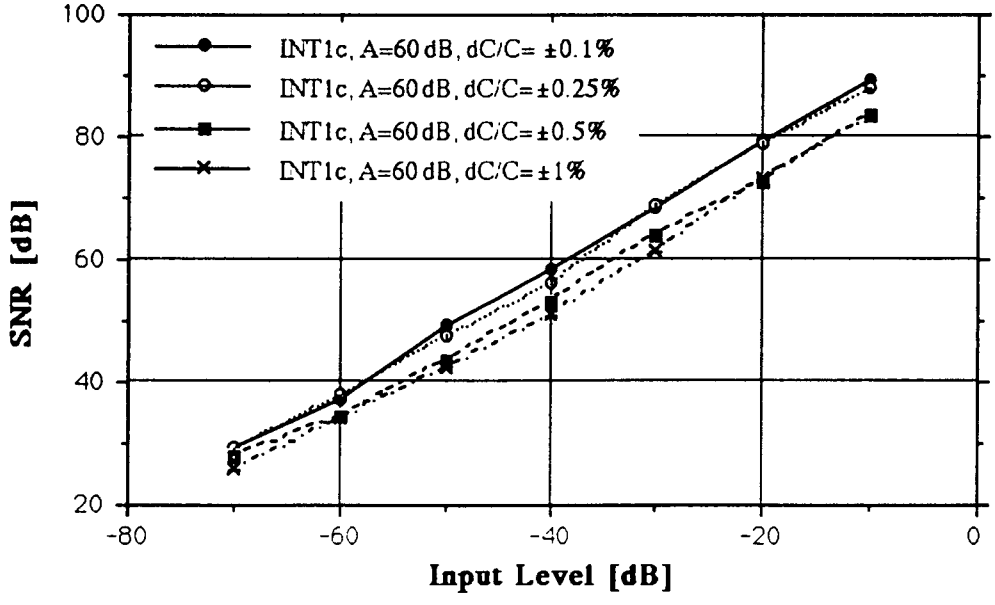


Fig. 5.12 (a) SNR performance of the system in Fig. 5. 8 with the gain compensated 2-path integrator in Fig. 5.11a (2pc1).
(b) SNR performance of the system in Fig. 5. 8 with the gain compensated 2-path integrator in Fig. 5.11b (2pc2).

5.4.4. Finite Gain Compensation

The relatively high opamp DC gain requirements prompted a further search for circuit techniques. The idea behind the offset- and finite-gain-compensated 2-path integrators shown in Fig. 5.11a and 5.11b is to store the offset voltage at the input of the opamp in one clock period by using an additional capacitor, e.g. ϕ_1 for circuit in Fig. 5.11b, then redefine the virtual ground of the opamp by putting this capacitor in series with the input in the next clock period [52]. The simulations revealed that the minimum opamp gain requirement is thus reduced to 60 dB in both cases (Fig. 5.12).

5.5. Conclusions

In this chapter, a new methodology to implement bandpass delta-sigma modulators was discussed. Transformed from a lowpass prototype delta-sigma modulator by using $z \rightarrow -z^N$ or $z \rightarrow z^N$ mapping, bandpass delta-sigma modulators preserve the desired stability and noise shaping properties of the prototype. To implement the $1/(1 + z^{-N})$ or $1/(1 - z^{-N})$ transfer functions, the novel PNP integrators that have been discussed in Chapter 4 are shown to be very promising. Two novel gain- and offset-compensated pseudo-2-path integrators solutions that can further address the relatively high opamp DC gain requirements for the implementation of 6^{th} order two-stage cascade bandpass delta-sigma modulator were introduced.

6. NOTCH LOOP

6.1. Introduction

In Fig. 6.1 the quantizer error in the delta-sigma loop is modeled as an additive white noise. The analyses that were given in the Section 2.4 rely on this basic assumption. A part of the delta-sigma loop operates in analog domain (loop filter), while the other part operates in digital domain (DAC). It can be theoretically observed that the entire loop were to be made of analog components, leaving out the ADC and the DAC. Let us assume a white noise is introduced through a summing node following the integrator. The power spectrum density of the loop output will show a notch around the center frequency of the loop filter. Just as the quantization error is shaped by the delta-sigma modulator, the spectrum of the injected noise is "notched" as well.

Applying this observation to practice, delta-sigma loops that were made entirely of analog components were fabricated and tested to confirm the theory of the proposed PNP differential integrators.

The clock rate for this project was selected as 1 MHz, within which the opamps and phase generation circuitry could operate safely.

6.2. System Simulations

The first example of the notch loop with a pseudo-2-path differential integrator (Fig. 6.2) was designed and simulated with SWITCAP2 with its AC analysis option. The capacitors were mismatched ±0.25 % from their nominal values. Switches were modeled to include their clock feedthrough effect as described in the SWITCAP2 manual.

Fig. 6.3 demonstrates the output spectrum of the notch loop with the pseudo-2-path integrators in Fig. 4.8. It can be observed that the notch is centered as expected at $f_s/4$,

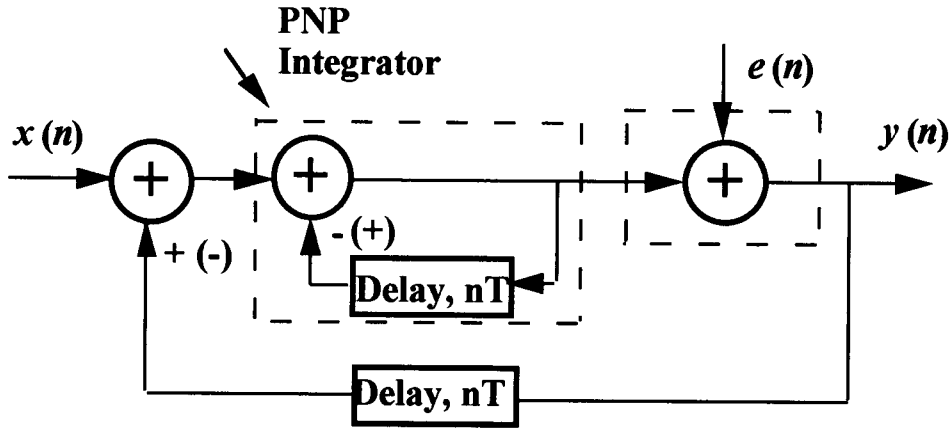


Fig. 6.1. Noise shaping loop.

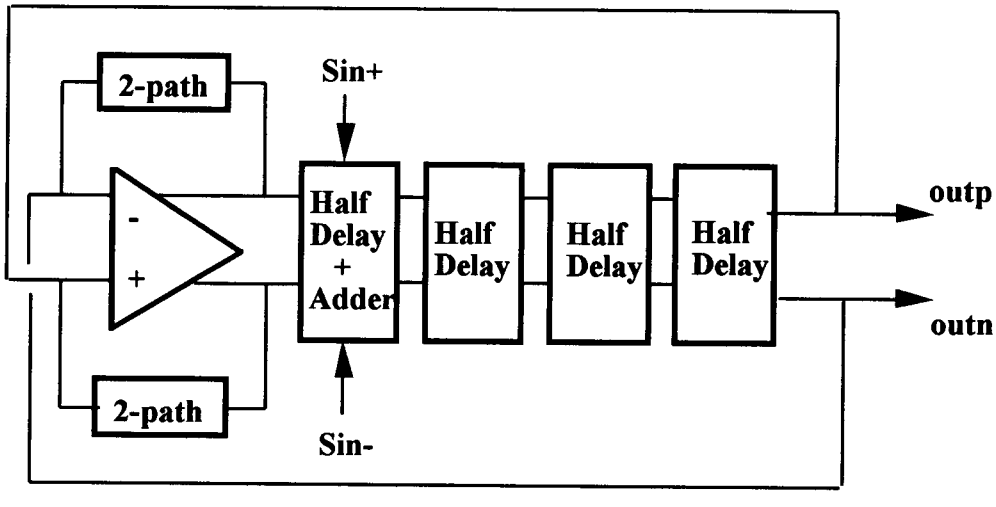


Fig. 6.2. Notch loop with the pseudo-2-path integrator.

250 kHz. As the theory suggests, the depth of the notch decreases as the DC gain of the opamp in the PNP integrator reduces, and is about -53 dB down for the case of 60 dB opamp gain. There are no observable peaks in the frequency spectrum due to clock feedthrough within the vicinity of the notch in the presence of ±0.25 % mismatching capacitors and imperfect switches.

6.3. Analog Half Delay Realization

Fig. 6.6a shows the single-ended version of the circuit that is used to implement the delays in the notch loop. It has a transfer function of $-z^{-1/2}$ if all the capacitors have equal values. Connecting a second set of switches and a capacitor similar to the input capacitor and switches, addition as well as delay functions can be accomplished (Fig. 6.6b). Addition function is needed to add the injected noise or tone into the loop.

6.4. Clock Generation

Fig. 6.7 depicts how the two non-overlapping phases are generated from the system clock. The inverters following the NOR gates add additional delay to the amount of non-overlapping. By gradually increasing the size of the inverters, the overload problem is avoided. The "*intd*" inverter is a delaying inverter containing transistors with larger lengths (3.6μm instead of 1.2μm minimum geometry). These are designed to generate delayed versions of the ϕ_1 and ϕ_2 to minimize the amount of charge injection on the switches.

The pseudo-2-path integrators with and without gain compensation need a variety of non-overlapping clocks with periods of $3T$. Three D flip-flops in Fig. 6.8 operate as a simple counter. The outputs of the each flip-flop are inputs to the latches to ensure non-overlapping. *Reset* pin allows all the phases to start simultaneously after power-up.

To generate the non-overlapping clocks with $4T$ periods of the gain-compensated pseudo-2-integrator, 2pc1, similar to the $3T$ case, four D flip-flops are used as a counter

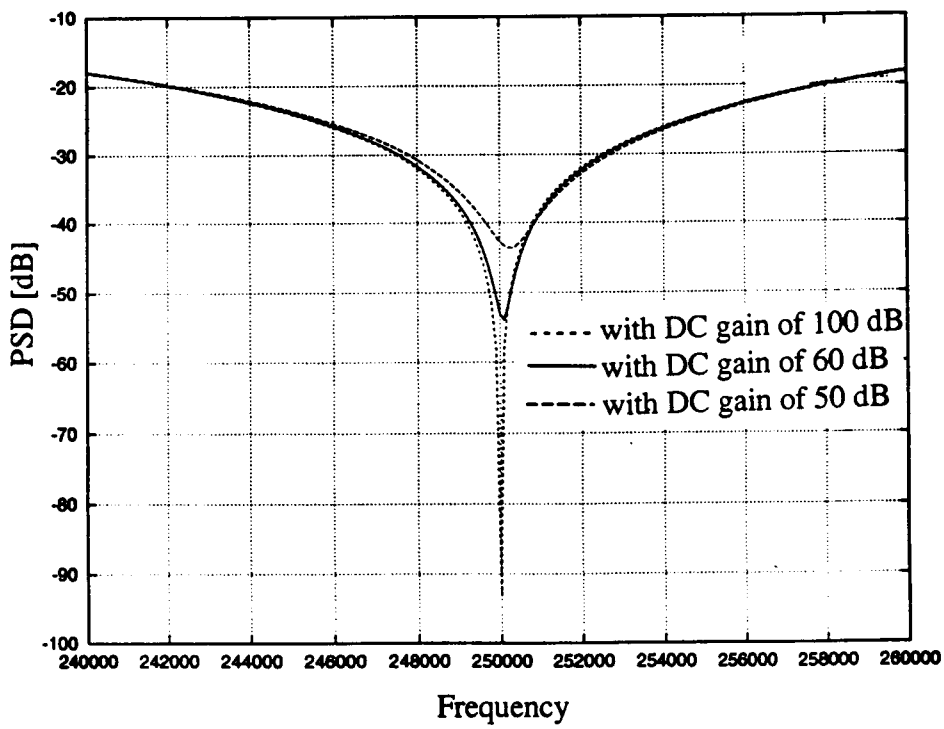


Fig. 6.3. Power spectral density of the notch loop with the 2-path integrator cell in Fig. 4.8.

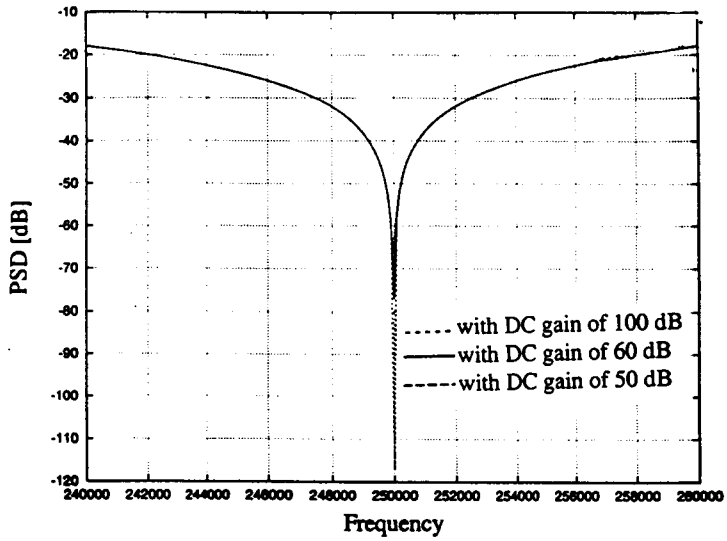


Fig. 6.4. Power spectral density of the notch loop with the gain-compensated 2-path integrator cell (2pc1) in Fig. 5.11a.

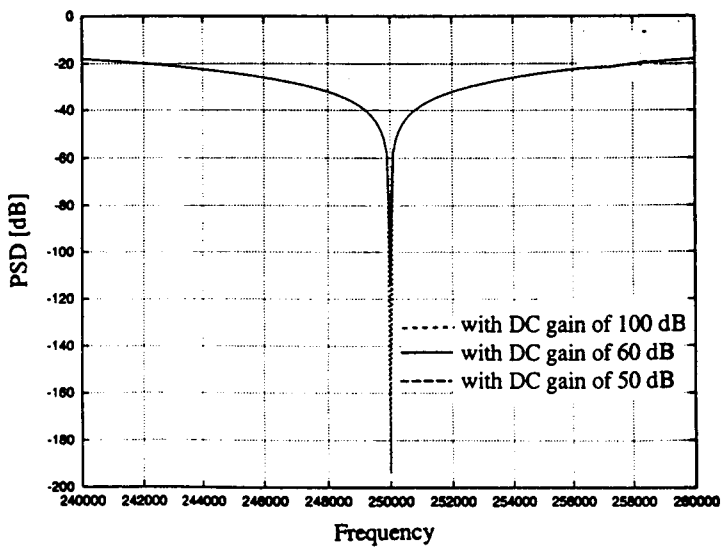


Fig. 6.5. Power spectral density of the notch loop with the gain-compensated 2-path integrator cell (2pc2) in Fig. 5.11b.

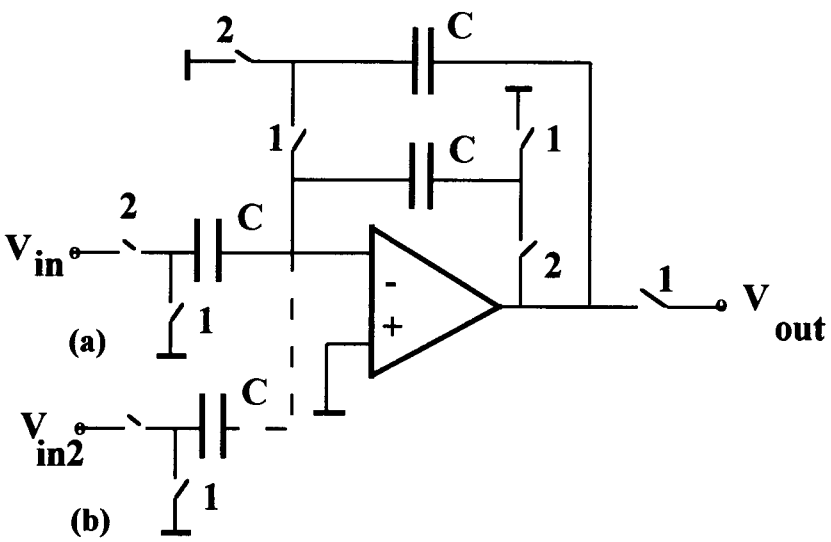


Fig. 6.6. (a) Analog half delay. (b) Analog half delay + adder.

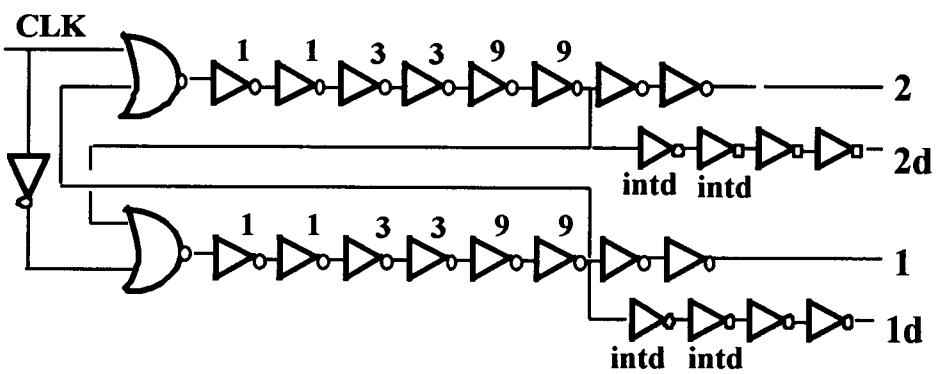


Fig. 6.7. 2-phase non-overlapping clock generation.

and their outputs are followed by latches. The gain-compensated psedo-2-integrator, 2pc2, requires a number of phases that can be generated from two and three non-overlapping clocks as shown in Fig. 6.9 simply by using NAND gates and inverters.

6.5. Operational Amplifiers

There are three main blocks in the notch loop that contain operational amplifiers (opamps): the PNP integrator, the half delay and the half delay + adder. To maximize the output range, a single-stage cascode differential opamp (Fig. 6.10) with a SC common-mode feedback is used for all the blocks except for the half delay unit before the system output. The last half delay block in the notch loop is designed with a differential two-stage opamp with a continuous resistive common-mode feedback to avoid any discontinuity in the system output prior to the spectrum or network analyzer (Fig. 6.11). In Fig. 6.12a and b, the frequency and phase responses of the single-stage and two-stage opamps for 4 pF loads are shown, respectively. The compensation capacitor of the two-stage opamp was 1.25 pF for this simulation.

Fig. 6.13 shows the photograph of the test chip that was designed to check the specs and functionality of the two opamps, a half delay block with the two-stage opamp, and a half delay + adder block with the single-stage opamp. Fig. 6.14a, b and c are the photographs of the notch loops designed with the pseudo-2-path (2p), pseudo-2-path with the first version of gain compensation (2pc1), and pseudo-2-path with the second version of gain compensation (2pc2), respectively.

6.6. Test Setup and Measurement Results

To test the system, a sine wave single tone is injected differentially to the notch loop. It was expected that this signal would be suppressed if it was located within the passband of the loop filter, which in this case the bandpass pseudo-2-path integrator with a center frequency at $f_s/4$.

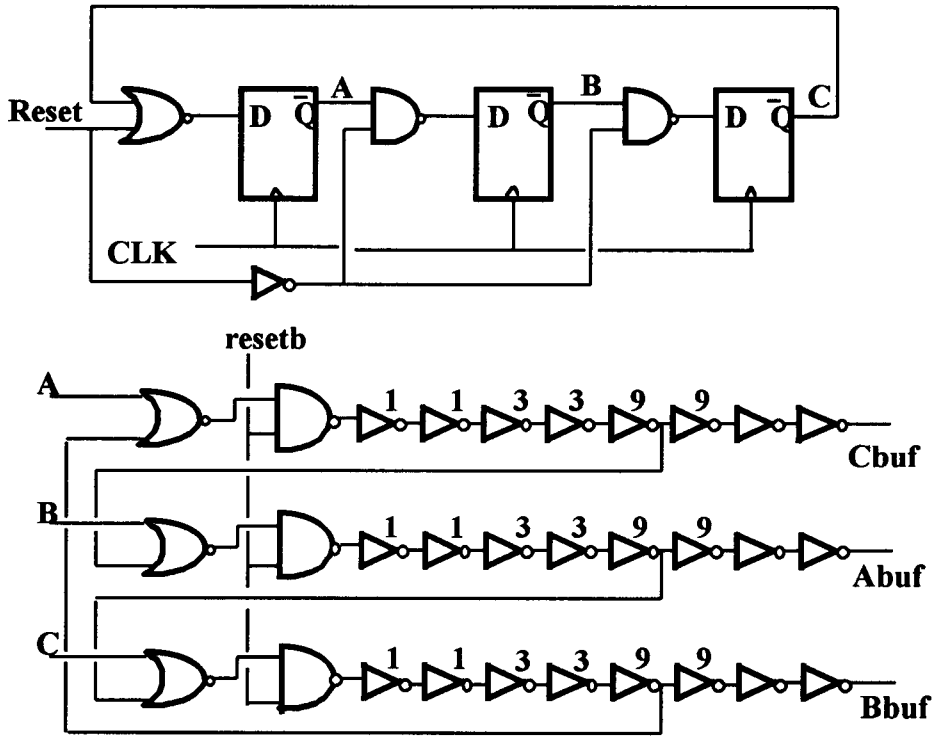


Fig. 6.8. 3-phase clock generation.

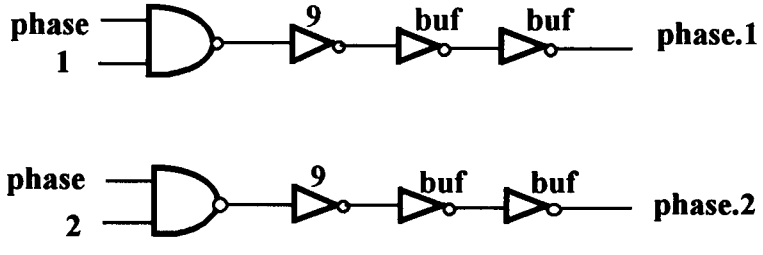


Fig. 6.9. 3-phase split clock generation. (phase, 1 and 2 are unbuffered signals.)

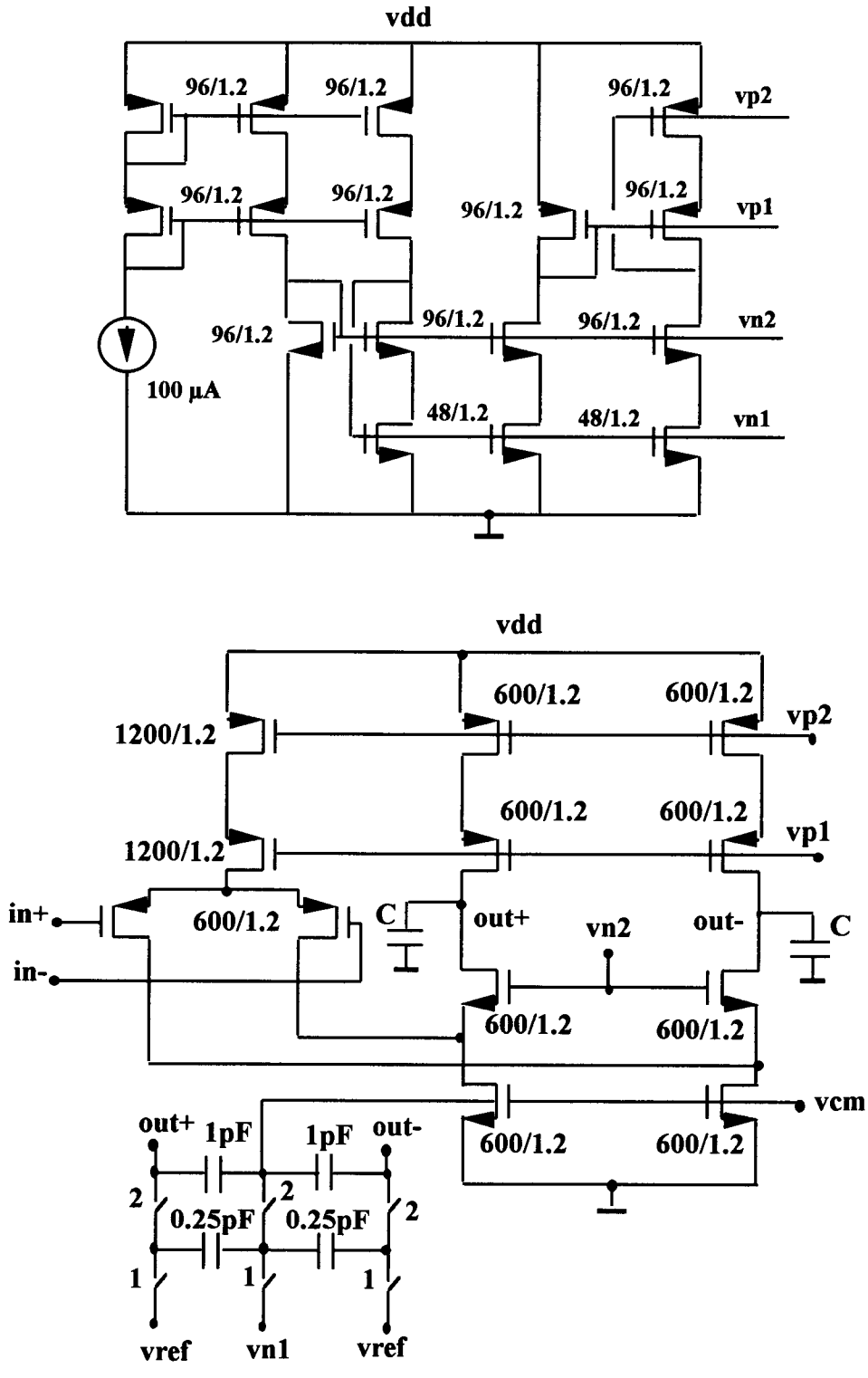


Fig. 6.10. Fully differential single-stage cascode opamp with its SC common-mode feedback and bias circuit.

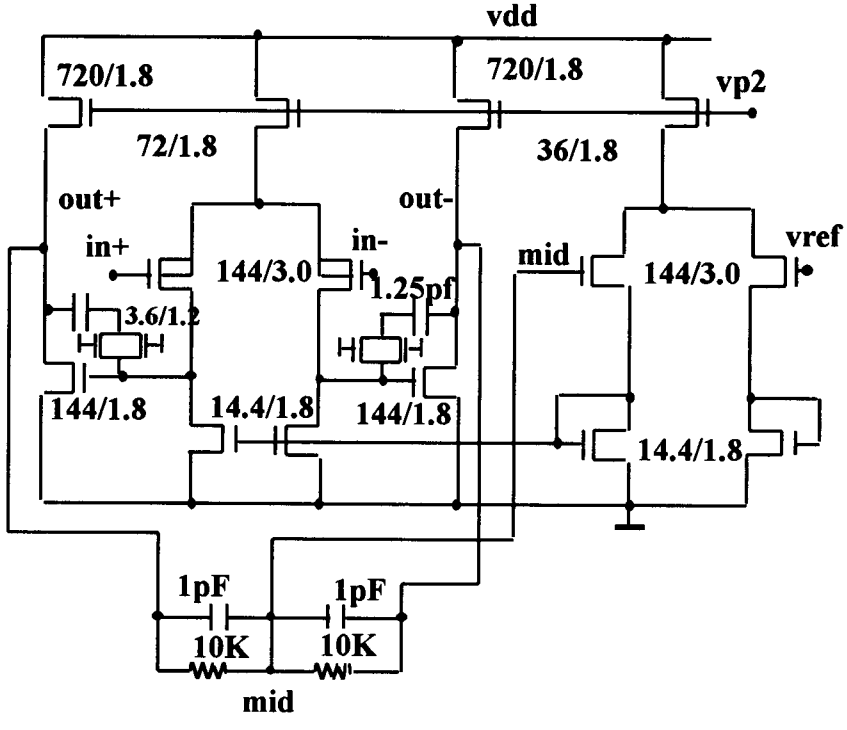


Fig. 6.11. Fully differential two-stage cascode opamp with its resistive continuous common-mode feedback.

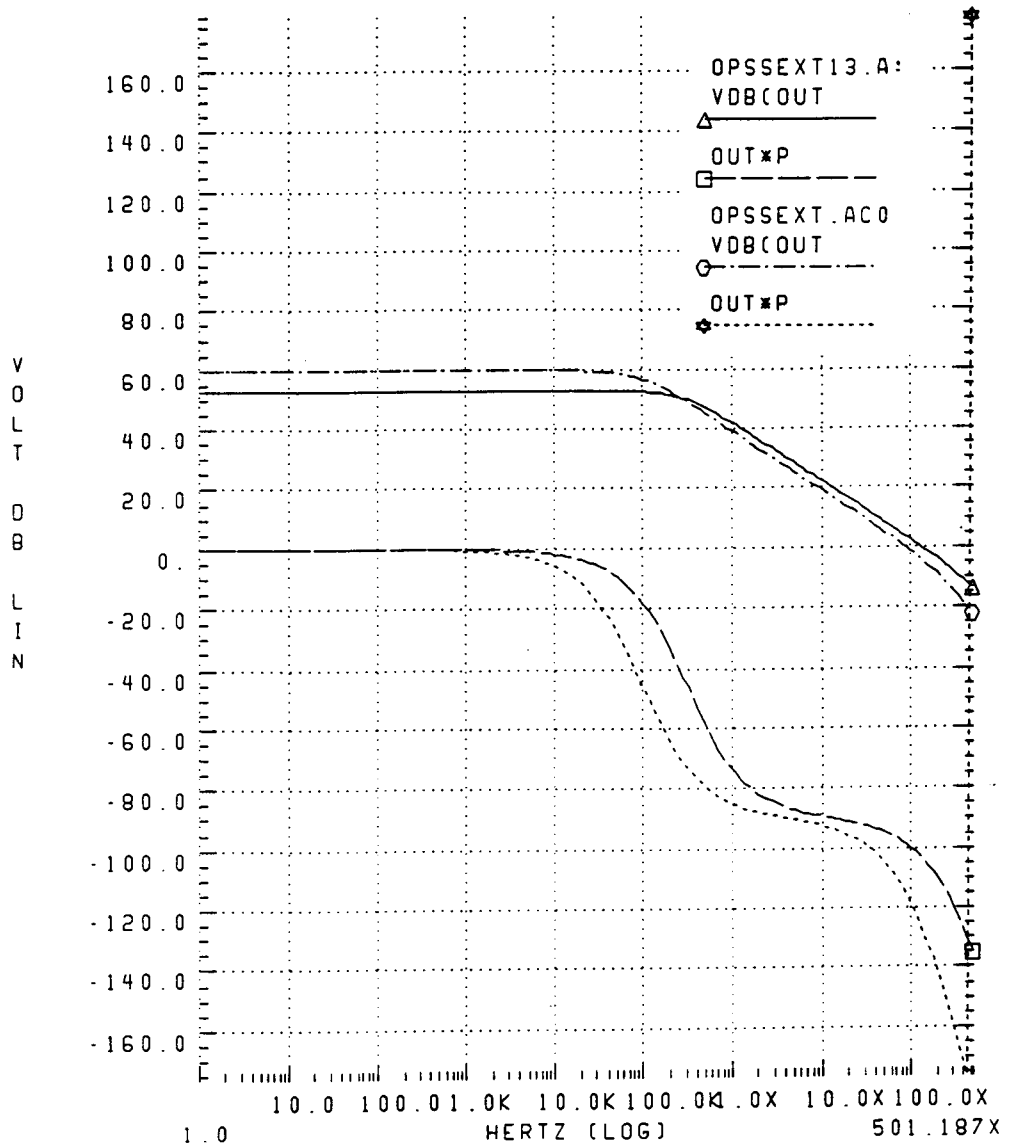


Fig. 6.12. (a) Phase and frequency responses of differential output of the single-stage cascode opamp in Fig. 6.11 with a 4 pF Load with LEVEL28 and LEVEL13 HSPICE models.

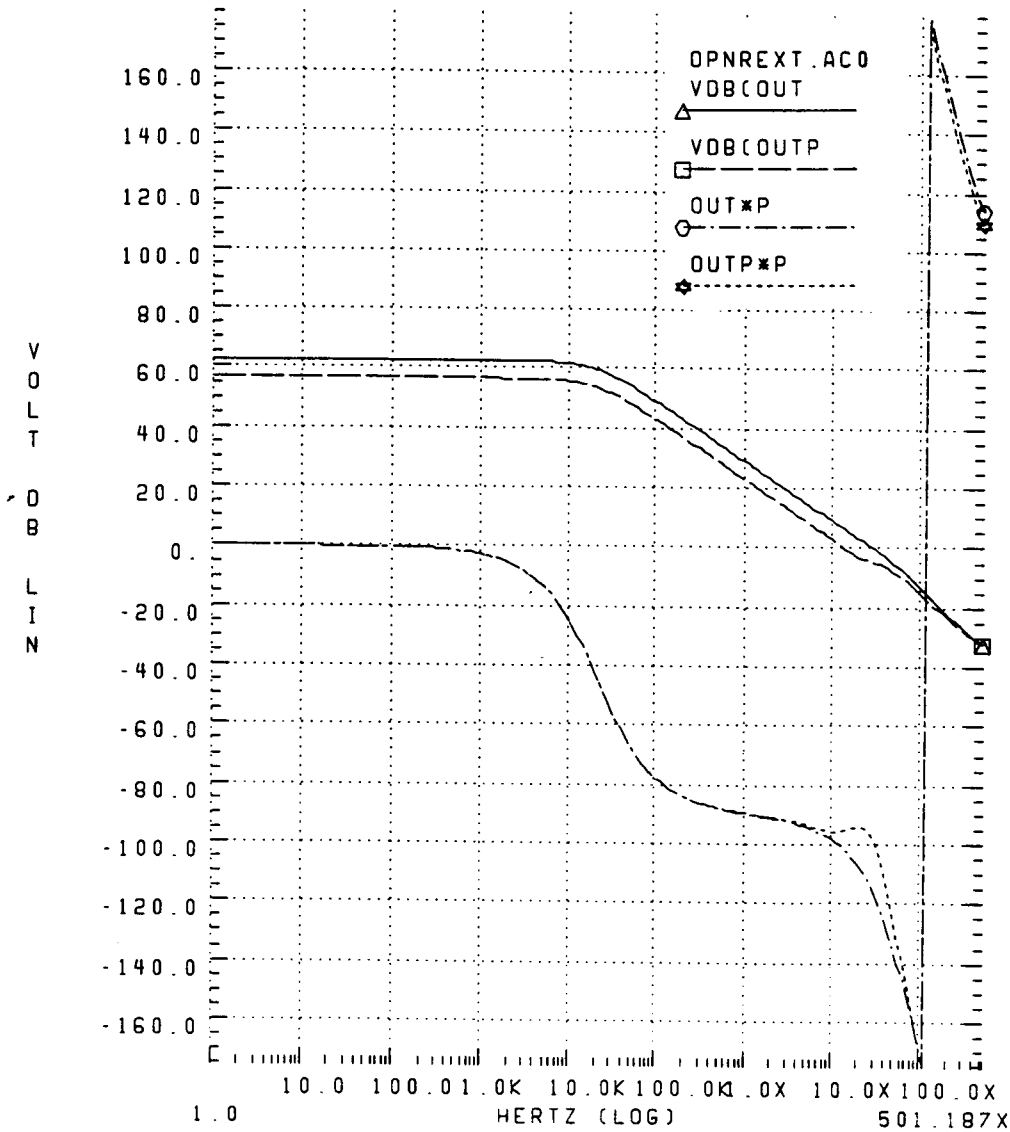


Fig. 6.12. (b) Phase and frequency responses of the two-stage opamp in Fig. 6.11 with a 4 pF Load for its differential output and the positive output.

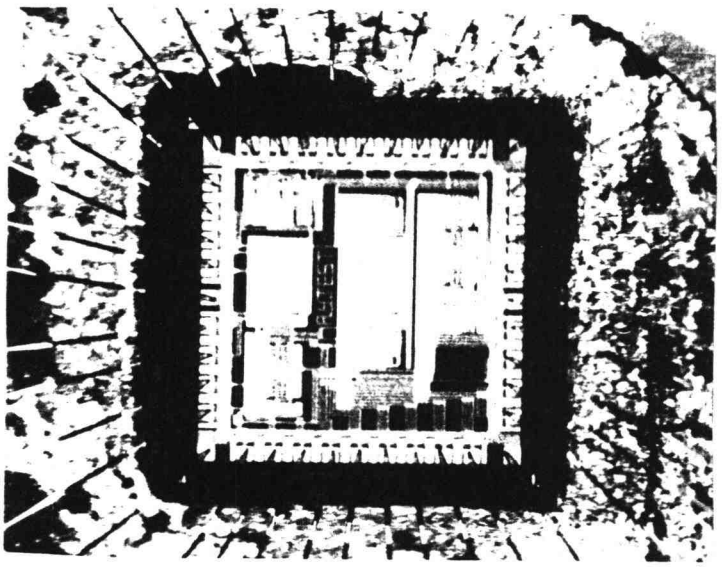


Fig. 6.13. The photo of the test chip that contains single-stage, two-stage opamps, half delay and half delay + adder circuits.

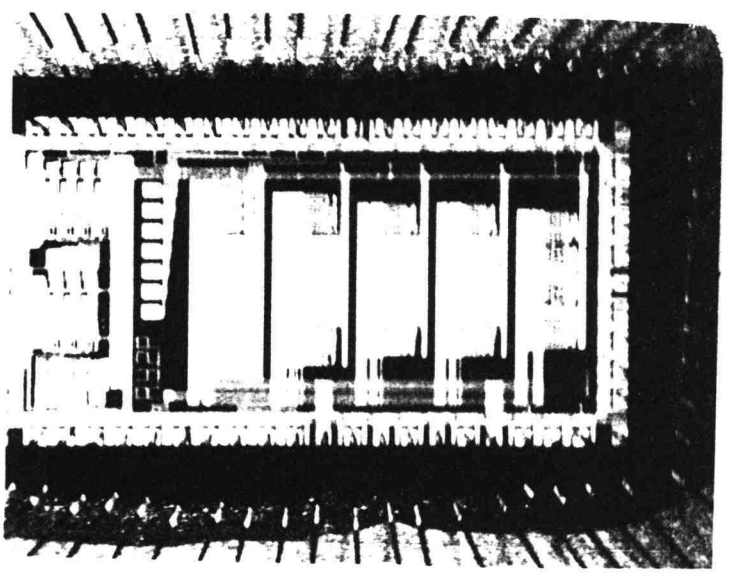
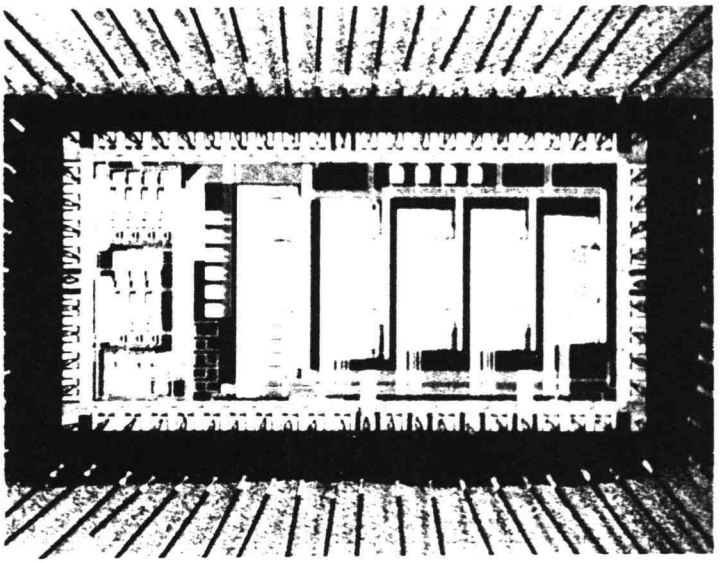
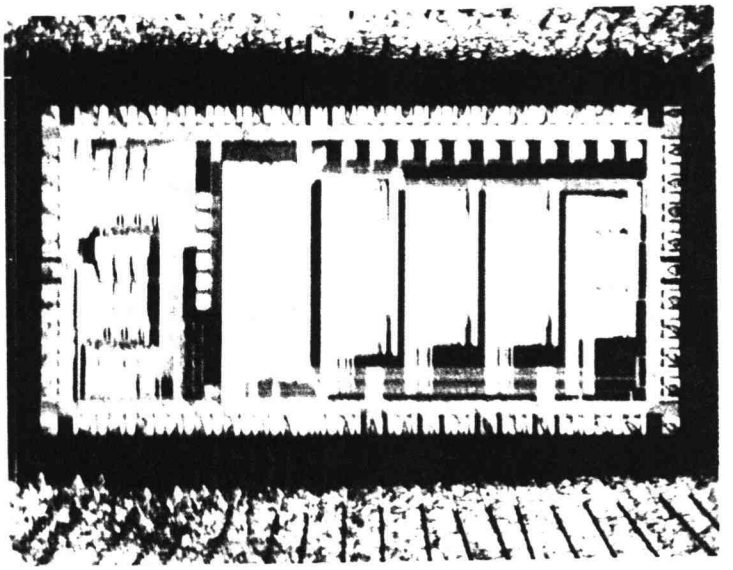


Fig. 6.14 (a) The photo of the notch loop with the pseudo-2-path integrator in Fig. 4.8.



(b)



(c)

Fig. 6.14 (b) The photo of the notch loop with the gain compensated pseudo-2-path integrator in Fig. 5.11a (2pc1).
(c) The photo of the notch loop with the gain compensated pseudo-2-path integrator in Fig. 5.11b (2pc2)

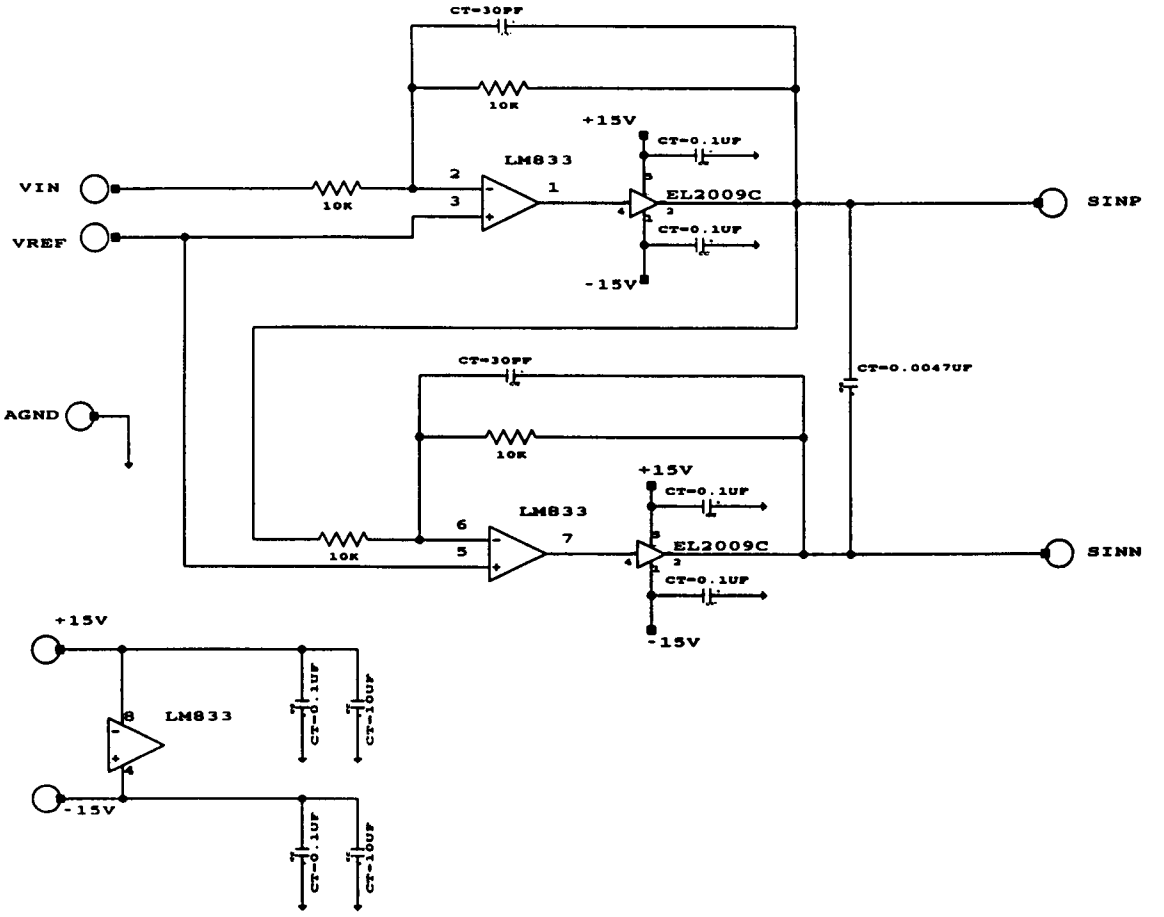


Fig. 6.15. Differential sine wave generator.

In order to generate a differential sine wave, a low-distortion single-ended sine wave from a network analyzer is connected to the block shown in Fig. 6.15. The output of the notch loop is attached to the network analyzer with a differential probe that performs differential to single-ended conversion on the output signal.

6.6.1. Clock Generation

Fig. 6.16 shows two of the outputs of the two-phase non-overlapping block, $\phi_1$and ϕ_{1d}. The delay between the rising edges of the two was measured to be about 20 ns. The system clock, and the two outputs of three non-overlapping phase generation block are depicted in Fig. 6.17. The waveform on the top is phase B, the middle one is phase A and the bottom one is the system clock. In Fig. 6.18 the system clock and one of the four non-overlapping phase outputs (phase 3) are displayed in the top and bottom, respectively.

6.6.2. Half Delay and Half Delay + Adder

Fig. 6.19 shows the positive output of the half delay circuit as well as its input, a single tone sine wave with 1V amplitude at 200 kHz. For easy comparison, the positive output is inverted by the oscilloscope selection. The clock was run at 1 MHz. It can be observed that the output was one clock period delayed and inverted as expected.

In Fig. 6.20 the positive output of the half delay + adder circuit and its input is shown. The clock was again running at 1 MHz and both of the inputs were connected to a differential sine wave generated. The output was, as expected, the summation of the two identical inputs and inverted.

6.6.3. Fully Differential Opamps

Using the test setup shown in Fig. 6.21, the DC gain and unity gain frequencies of the single- and two-stage opamps were measured. Fig. 6.22 (a) and (b) are the waveforms at

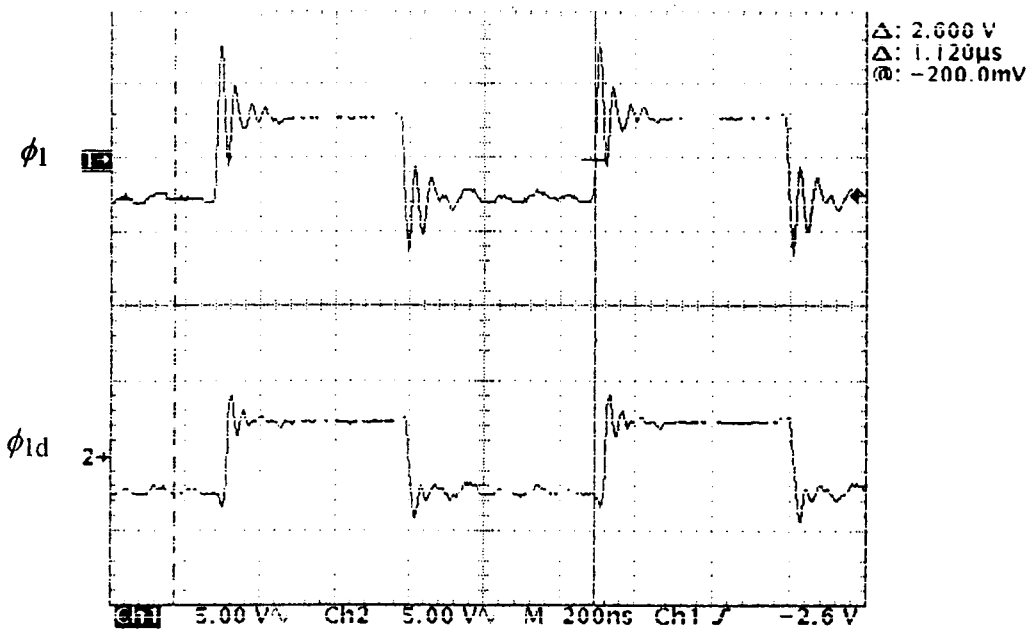


Fig. 6.16. Clock phases ϕ_1 and ϕ_{1d} generated by the two non-overlapping phase block.

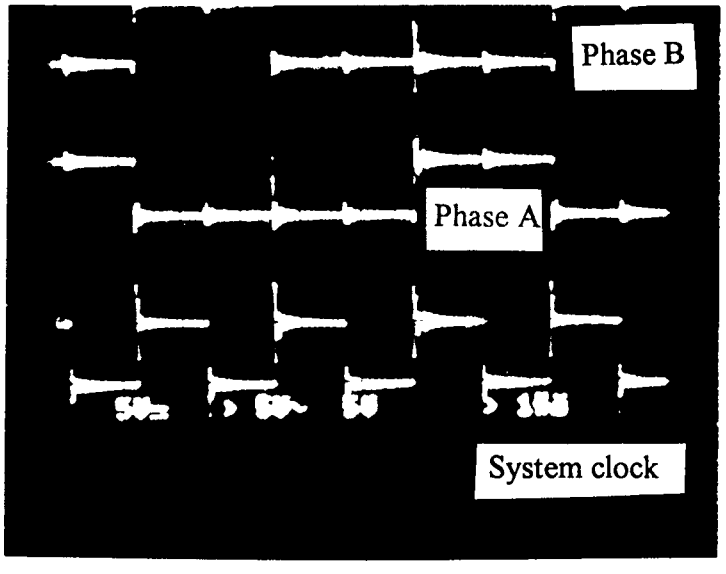


Fig. 6.17. Outputs from the three non-overlapping phase generator block.

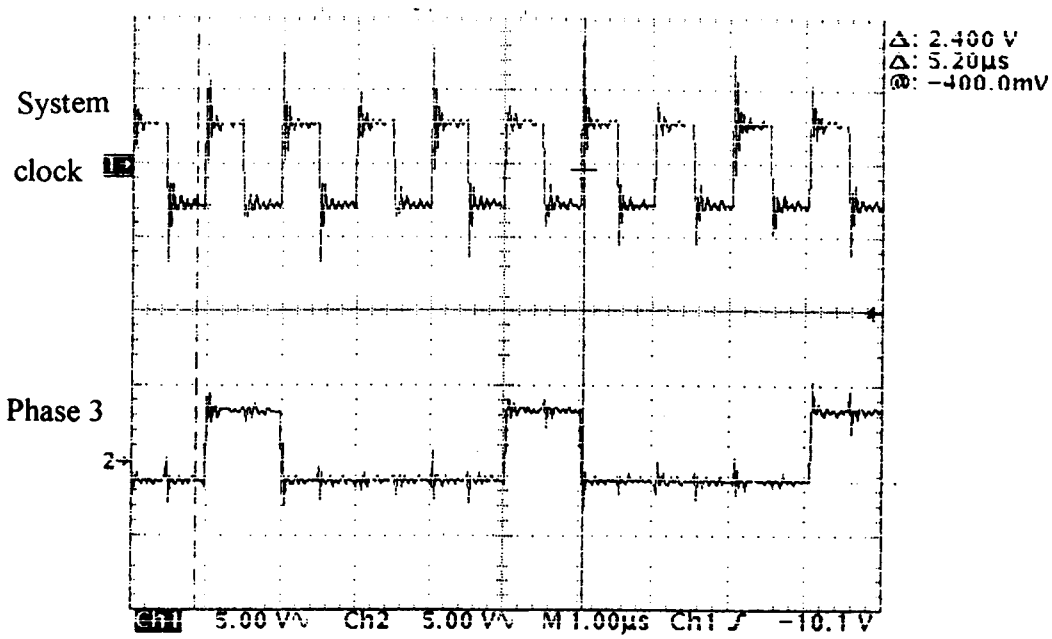


Fig. 6.18. Outputs from the four non-overlapping phase generator block

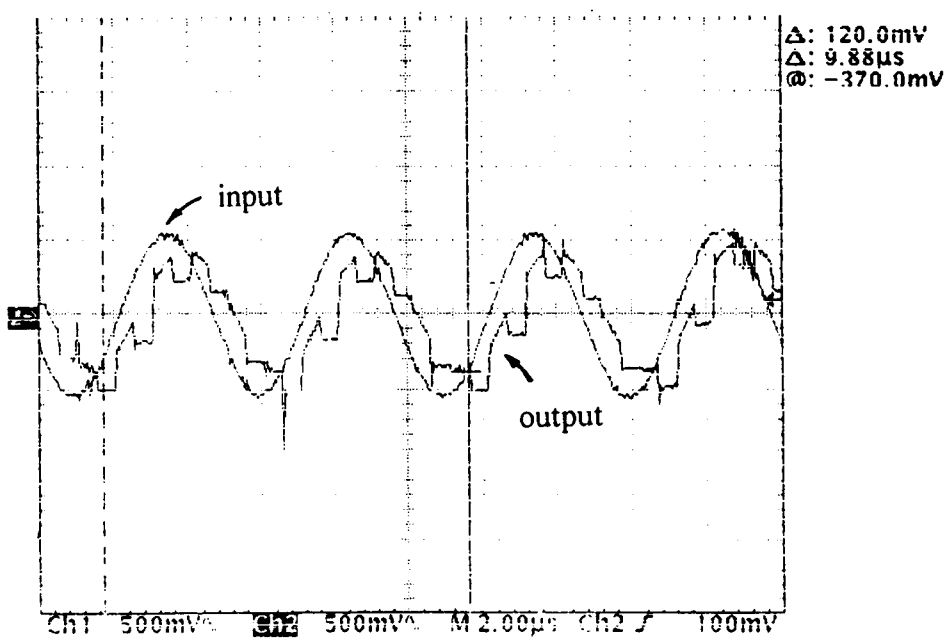


Fig. 6.19. Input and inverted output of the half delay block.

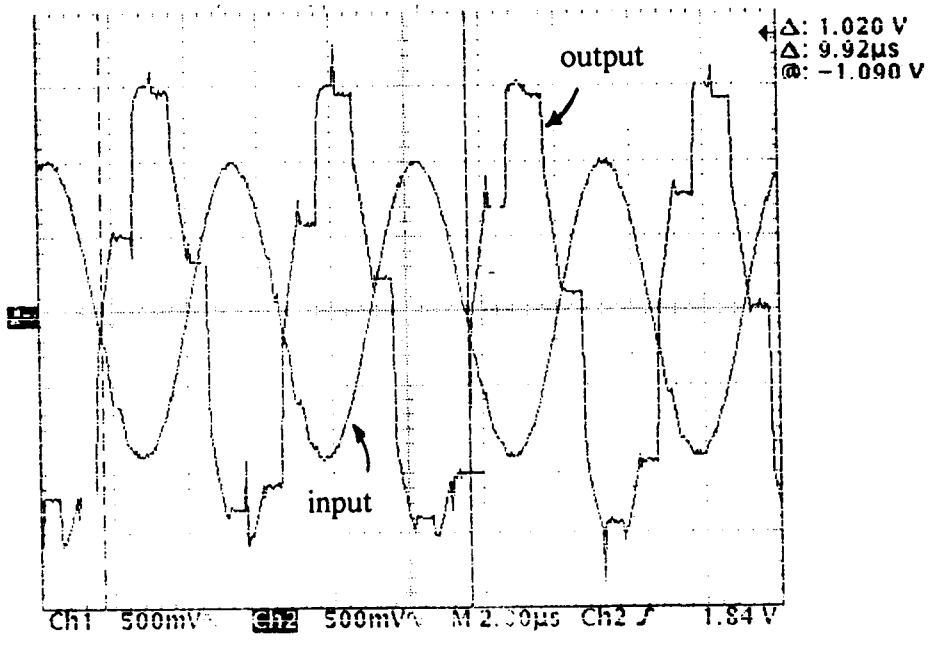


Fig. 6.20. Input and output of the half delay + adder block.

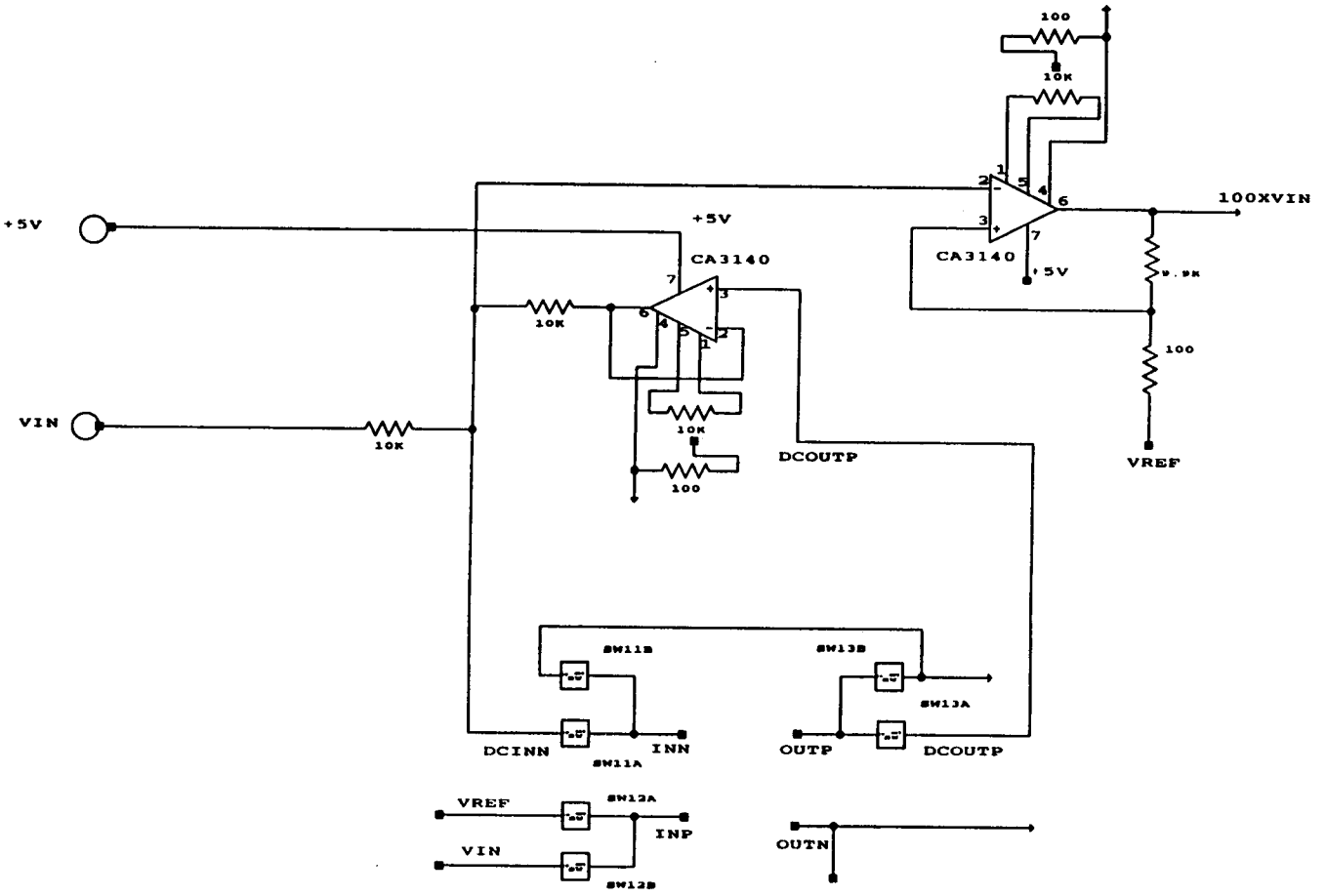


Fig. 6.21. Test board for measuring opamp DC gain and unity gain bandwidth.

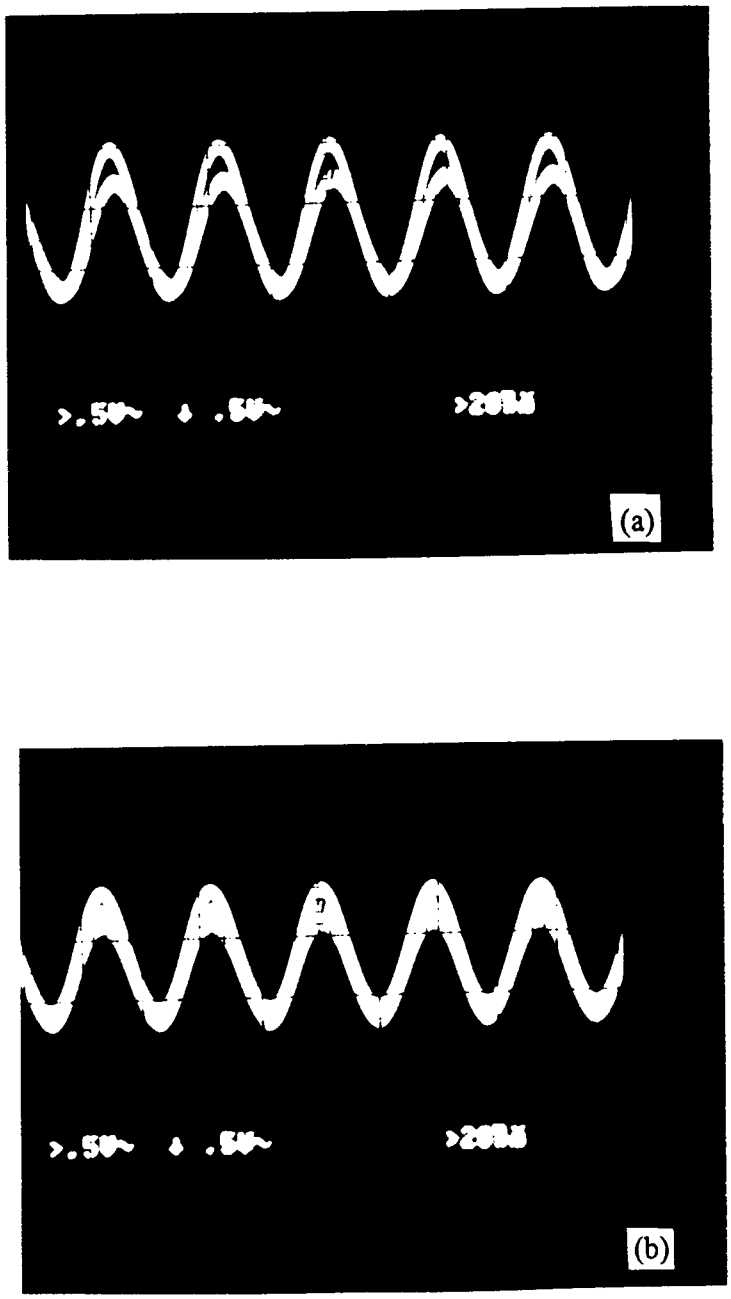


Fig. 6.22 (a) Positive output and input of the two-stage opamp in unity gain configuration with a sine input at 26 MHz.
(b) Positive output and input of the single-stage opamp in unity gain configuration with a sine input at 30 MHz.

the positive output and the positive input of the two-stage and single-stage opamps, respectively, in the unity gain configuration. The unity gain bandwidth of the opamps were measured based on the principle that the opamp output amplitude becomes half of the input amplitude at the unity gain frequency. For the single-stage opamp it was measured to be 30 MHz and for the two-stage opamp it was 26 MHz. The DC gain of the opamps were measured as 58 dB (single-stage) and 56 dB (two-stage). The smaller measured bandwidth of the single-stage opamp is mainly due to the higher load capacitor of the pin, estimated to be approximately 20 pF, which also serves as the compensation capacitor.

6.6.4. Notch Loop with the Pseudo-2-Path Integrator

For these measurements, the differential outputs of the notch loop were connected to the network analyzer with a differential probe. The low-distortion single-ended sine wave signal produced by the analyzer was used as an input to the differential sine wave board shown in Fig. 6.15. The differential sine wave was then injected into the notch loop as in Fig. 6.2. The spectrum of this signal was measured and used for normalization.

Fig. 6.23 (a), (b) and (c) are the plots of the output spectrum of the notch loop with the pseudo-2-path integrator at the clock frequencies 250 kHz, 500 kHz and 1 MHz, respectively. It can be observed that the relative shape of the spectrum is preserved as the clock frequency changes. However, the depth of the notch is much less than what was predicted by the simulations (about -20 dB, instead of less than -50 dB). The tests on the main blocks show that they are functional and operating close to their design specs. Noise

generated in the test board is the primary suspect of this degradation, and efforts to reduce it are continuing to obtain better readings.

6.7. Conclusions

In this chapter, an analog delta-sigma loop containing the proposed pseudo-2-path integrators is examined. The simulation results confirmed the relationship between the depth of the notch and the DC gain of the opamp in the integrator. Several prototypes containing the proposed pseudo-2-path integrators with and without gain compensation were fabricated in the ORBIT 1.2 μm double-poly double-metal n-well CMOS process. All of the main blocks that make up the notch loop are shown to function within their design specs, although the notch depth of the notch loop with the pseudo-2-path integrator is measured at values much less than expected.

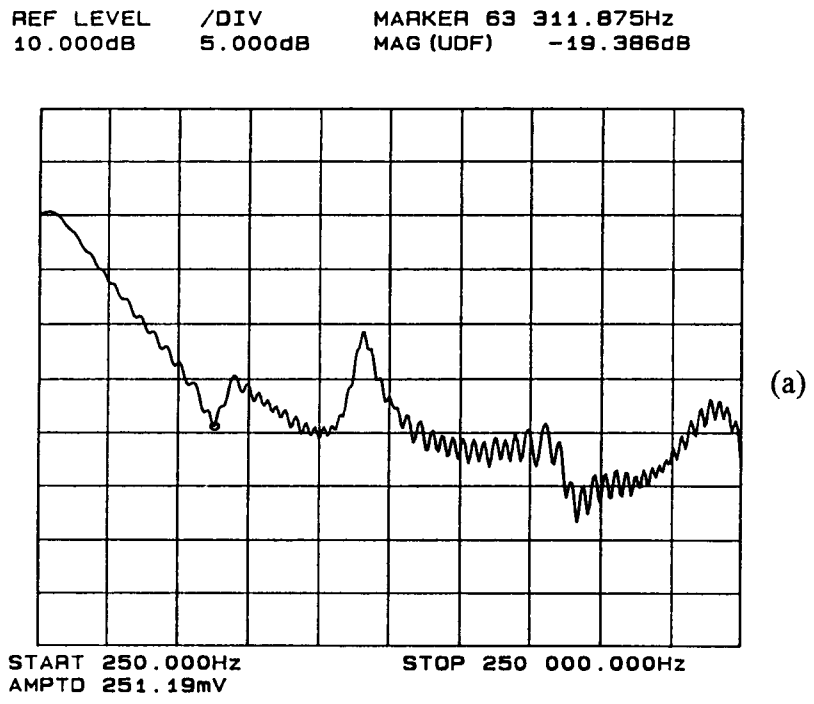


Fig. 6.23. Output spectrum of the notch loop with the pseudo-2-path integrator
(a) with 250 kHz clock frequency.
(b) with 500 kHz clock frequency.

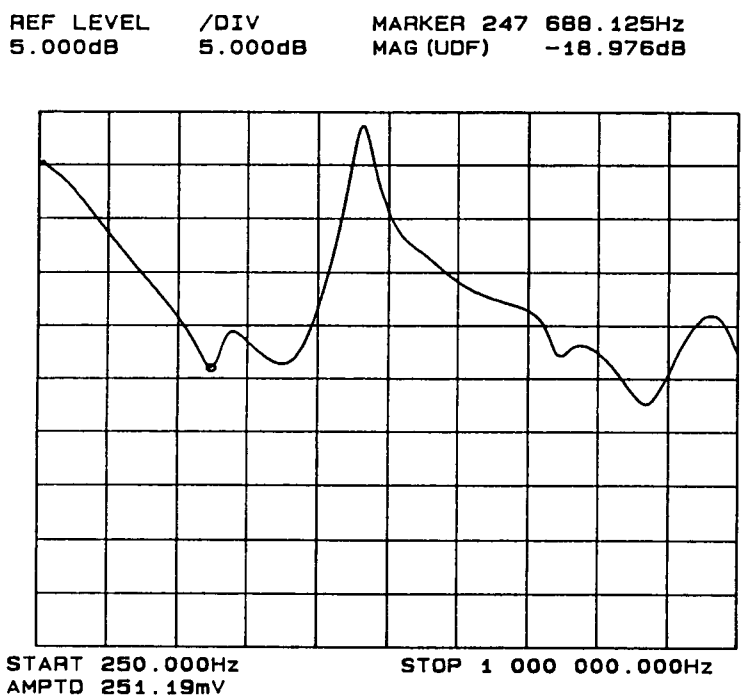


Fig. 6.23. Output spectrum of the notch loop with the pseudo-2-path integrator (c) with 1 MHz clock frequency.

7. CONCLUSIONS

In this study, novel lowpass multiplexed delta-sigma modulator architectures that exchange hardware complexity with a faster clock are proposed. Moreover, it is shown that with $z \rightarrow z^N$ or $z \rightarrow -z^N$ transformations, it is possible to obtain bandpass delta-sigma modulator architectures based on existing lowpass ones. Both the lowpass and the bandpass proposed architectures can be implemented with PNP integrators. The novel PNP integrators with out-of-passband noise peaks are very attractive for implementing the proposed modulators. The DC gain requirements of the opamps in the PNP integrators can be further reduced by gain-compensation techniques.

To confirm the theory, all-analog notch loops containing the proposed PNP integrators were fabricated in the ORBIT 1.2 μm double-poly double-metal n-well CMOS technology. The measurement results, although not as good as the ones estimated from the simulations, showed that the proposed PNP integrators can be used in realization of bandpass delta-sigma modulators.

Implementation of the 6^{th} order two-stage multi-bit single-bit bandpass delta-sigma modulator discussed in Section 5.4.2 with the proposed pseudo-2-path integrators with and without gain compensation is the next step for future work.

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APPENDIX

APPENDIX

The system-level simulations discussed in Chapter 5 revealed that the 6th order two-stage bandpass delta-sigma modulator with pseudo-2path integrators (Fig. 5.8) requires a fully differential opamp with a minimum gain of 70 dB if gain compensation is not used. If the sampling rate, f_s is chosen to be 10 MHz, the opamp at the first loop filter has to settle fairly quickly (half a period, or 50 ns) and very accurately (0.01%). This means that the opamp also needs to have a large bandwidth. The rule of thumb is to design opamps with unity gain bandwidths that are about 5-6 times larger than the clock frequency. For this study, a bandwidth of 70-80 MHz was chosen.

The output swing is intended to be the maximum available considering that the A/D converter will be operated with a single 5V power supply, therefore a SC-type common-mode feedback circuitry is used. For the slew rate, the rate of change at the outputs of the integrators were observed from simulations and a rate of 200 V/μs is determined as the goal.

In a conventional cascode single-stage opamp, DC gain and bandwidth of the opamp are coupled together. Increasing one decreases the other. The report [78] of a CMOS differential opamp with a DC gain of 90 dB and a unity-gain frequency of 116 MHz (16 pF load) was, therefore, significant. The proposed technique which practically decouples the two quantities is called *gain-boosting* (Fig. A.1) [79, 80]. It is based on increasing the cascoding effect of M2 by adding an additional gain stage. The output impedance is then increased by the gain of the additional stage, A_{add}, and it can be written as:

$$R_{out} = (g_{m2}\, r_{o2}\, (A_{add}+1)+1)r_{o1}+r_{o2} \qquad \text{(A.1)}$$

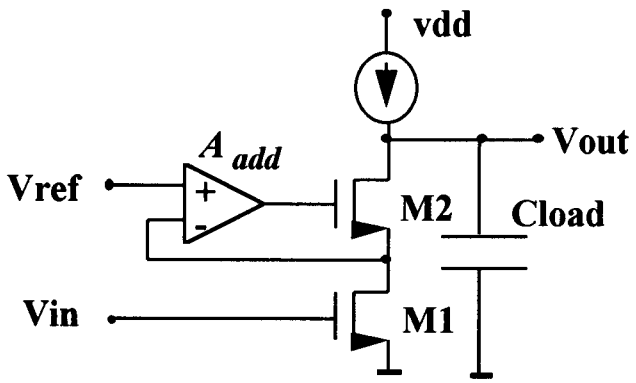


Fig. A.1. Cascoded gain stage with gain enhancement.

The DC gain of the overall opamp is:

$$A_{tot} = g_{m1} r_{o1} (g_{m2} r_{o2} (A_{add}+1)+1) \quad \text{(A.2)}$$

By implementing the additional stage with gain boosting the performance can be even further increased. However, repeating the same technique many times is not possible as a result of limiting factors such as leakage currents, weak avalanche, and thermal feedback.

In [78], for gainboosting of a fully differential opamp, four additional gain stages were used (Fig. A.2). In fact, it is possible to reduce the number of gain stages to two [81]. Observing that the additional gain stage is only necessary for differential signals, we can combine the two gain stages (Fig. A.3a). Fig. A.3b and Fig. A.3c show the additional gain stages for upper and lower cascode transistors of the main opamp, respectively. Since these additional gain stages are also fully differential they need their own common-mode feedback circuits. The SC-type common-mode feedback [82] is chosen for the main opamp to maximize its output range. It is preferable due to its larger

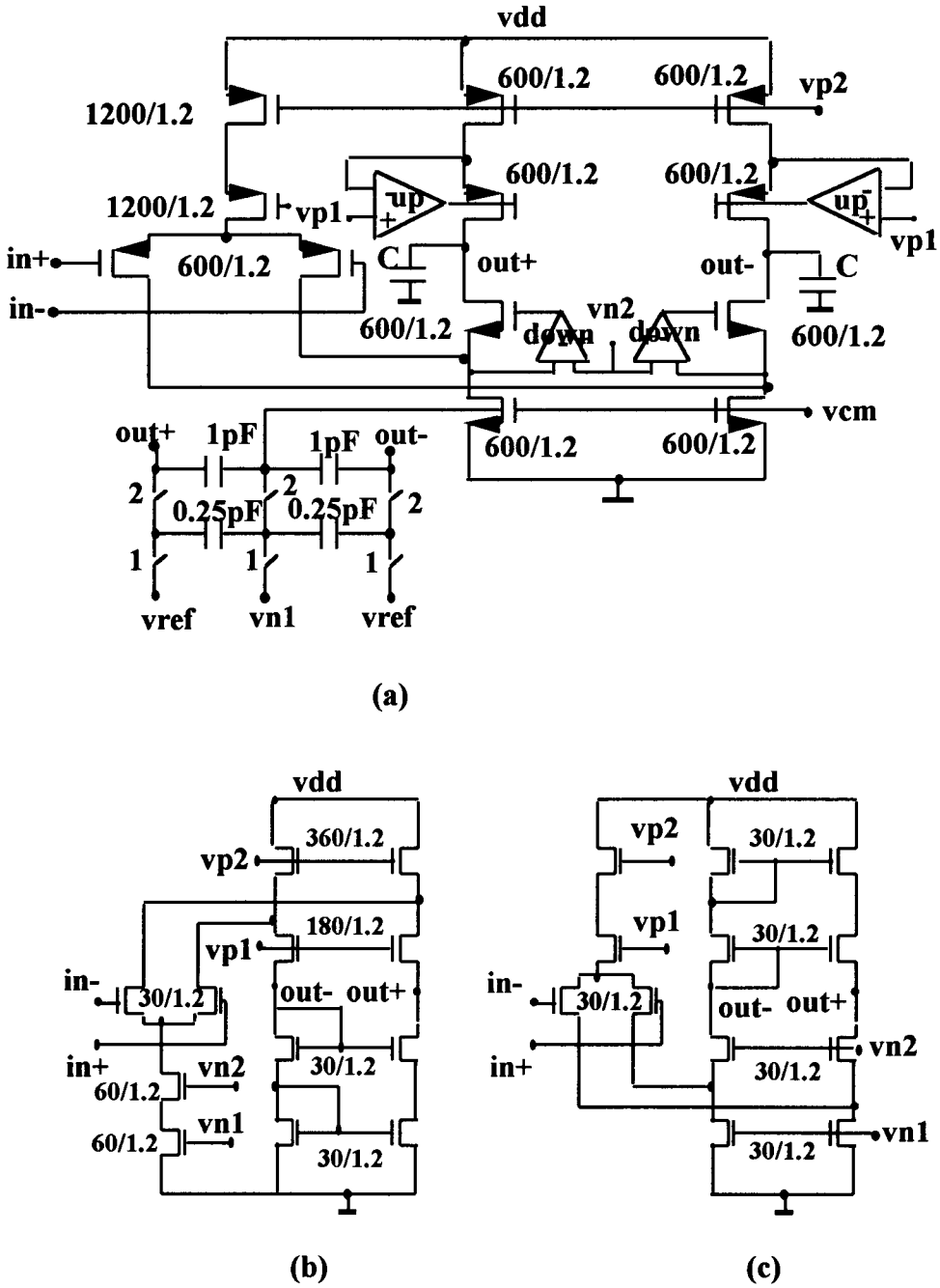


Fig. A.2. Conventional gain boosted opamp and its additional gain stages.

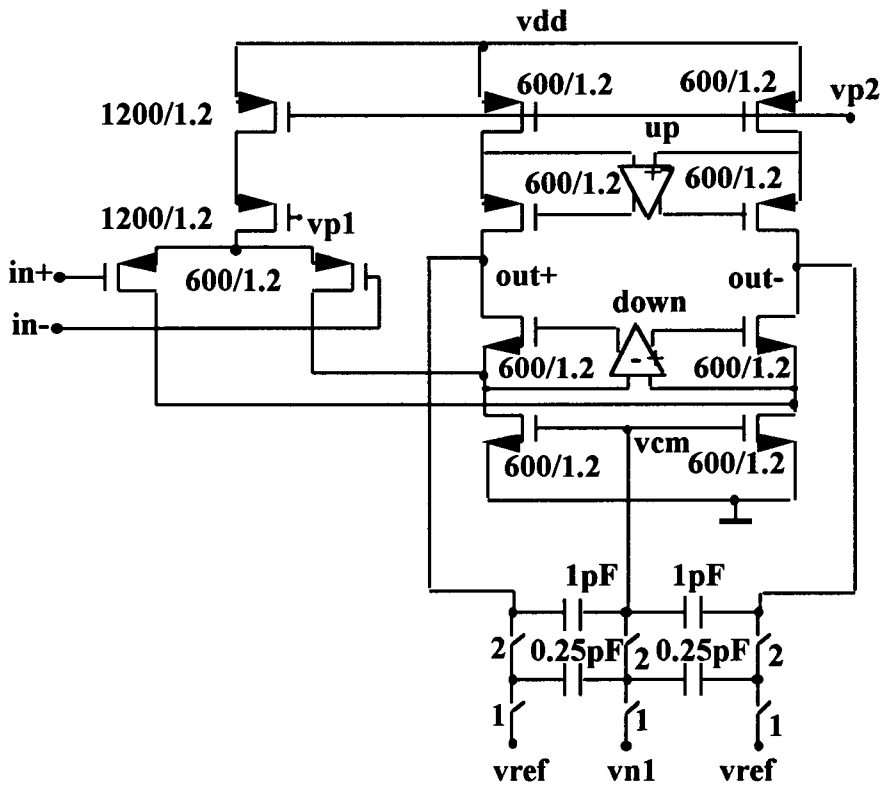


Fig. A.3a. Differentially gain boosted opamp and its SC common-mode feedback.

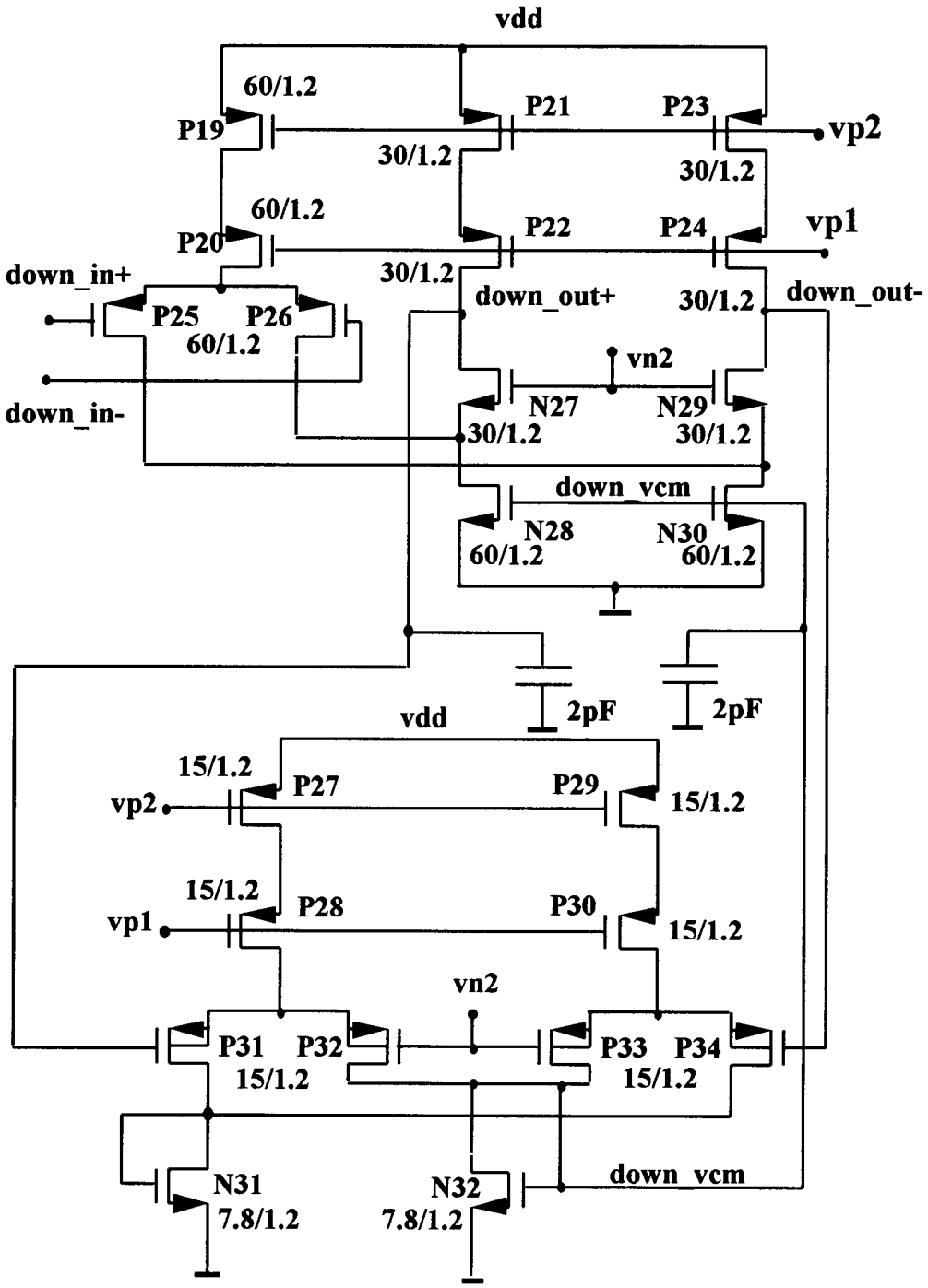


Fig. A.3b. Additional gain stage "down" and its continuous common-mode feedback.

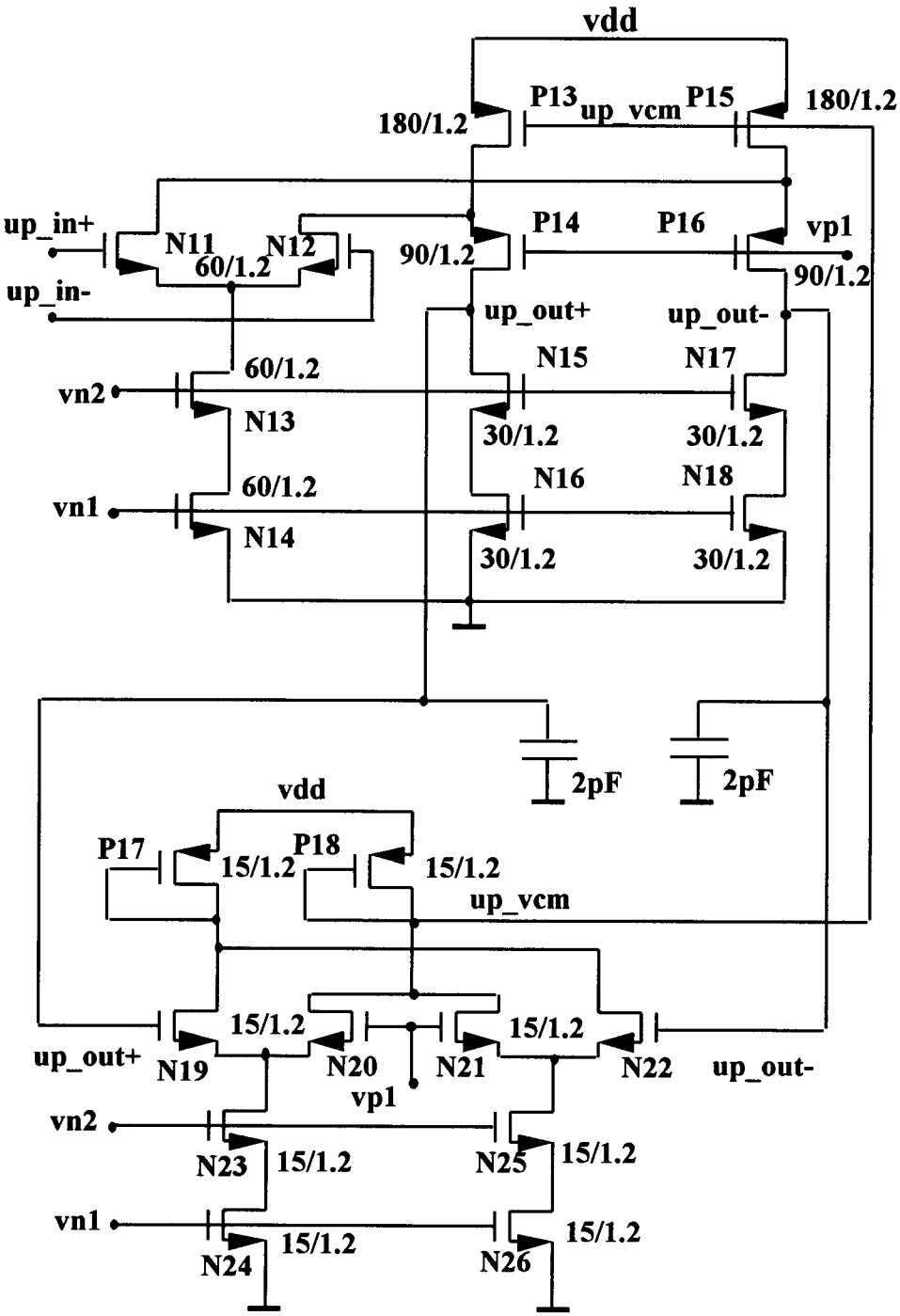


Fig. A.3c. Additional gain stage "up" and its continuous common-mode feedback.

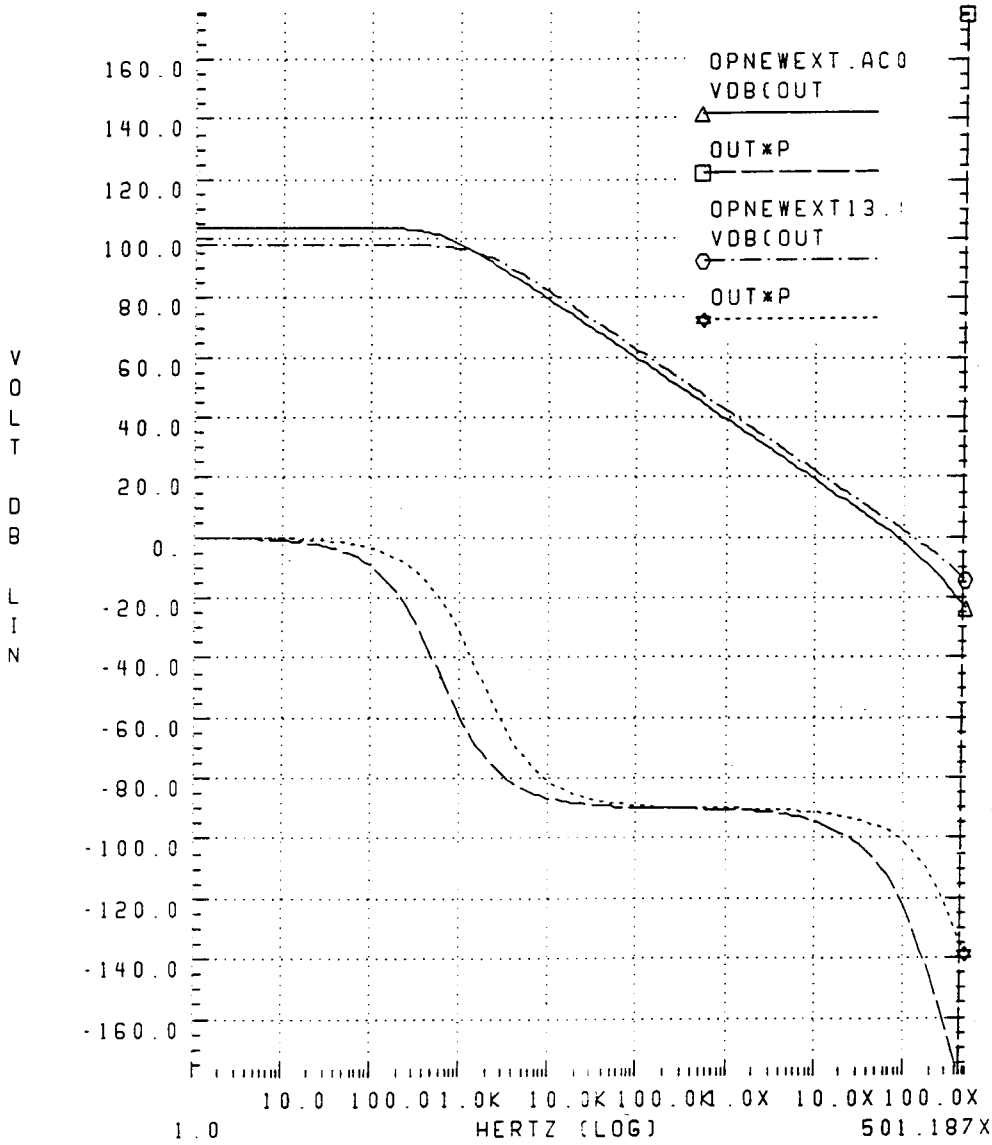


Fig. A.4. Frequency and phase response of the conventional gain boosted opamp.

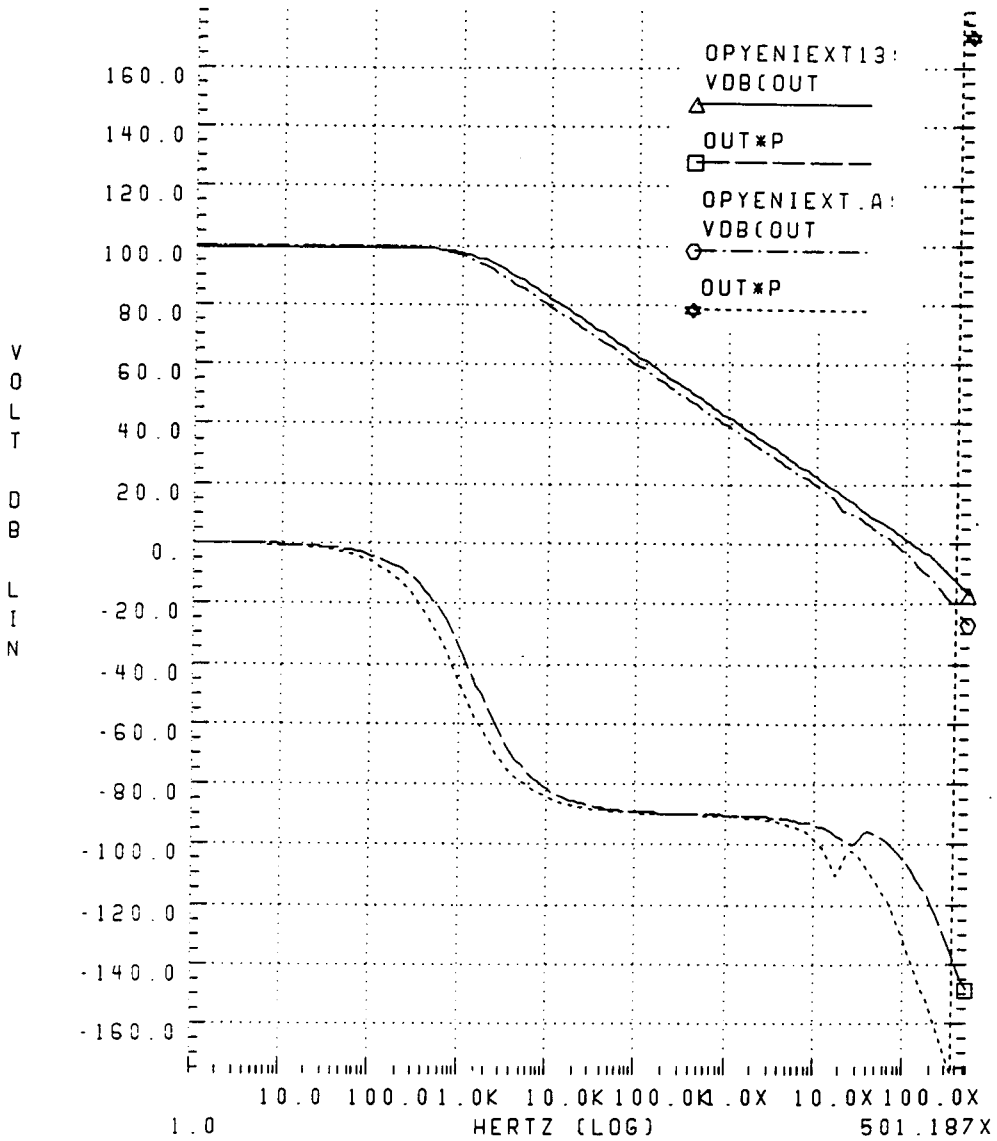
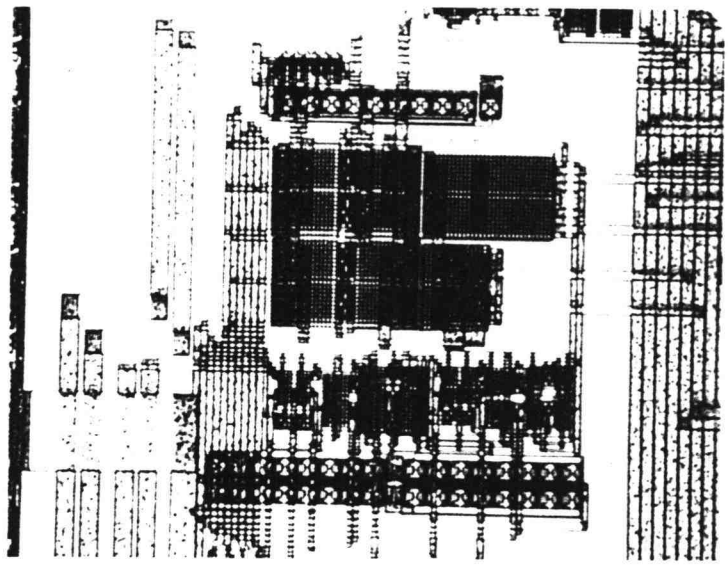


Fig. A.5. Frequency and phase response of the differentially gain boosted opamp with LEVEL 28 and LEVEL 13 models.

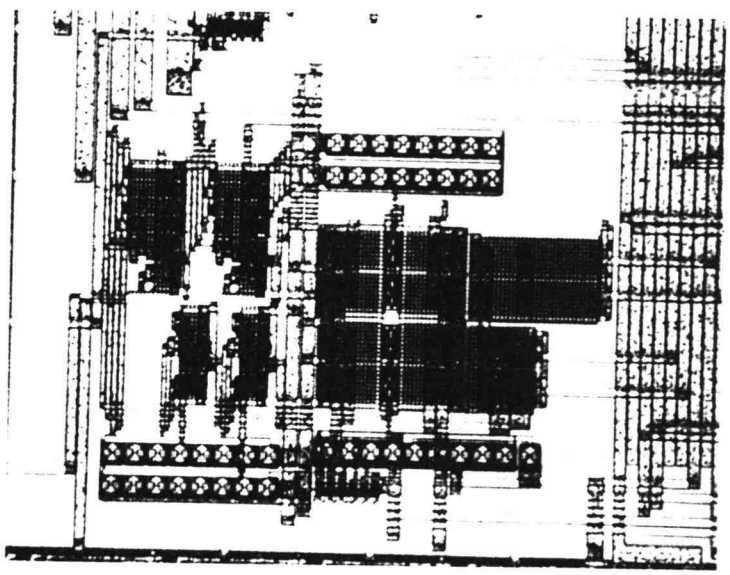
input range over continuous common-mode feedback circuits that are chosen for the additional gain opamps.

The frequency and phase response of the conventional gain boosted opamp(Fig. A.2) and the differential gain boosted opamp (Fig. 3 a, b, c) are plotted in Fig. A.4 and A.5, respectively. Notice that the core opamp of both of these opamps is the one given in Fig. 6.10. It is clear that the inclusion of the additional gain stages improves the DC gain considerably, from 58 dB, by the amount of DC gain of the additional gain stages.

These two types of gain boosted opamps were fabricated in the ORBIT 1.2 μm double-poly double-metal n-well process. The chip photographs of the differential and conventional gain boosted opamps are shown in Fig. A.6a, and b, respectively. To test the opamp DC gain and bandwidths, the test setup shown in Fig. 6.21 was used. For testing very high opamp DC gains, the test board did not allow very small voltage readings in the 3-4 mV range to be measured accurately. Cautions were taken such as shortening the length of the connector wires, using additional bypass capacitors on the power and bias lines, and using separate power supplies for digital and analog sections. However, voltage readings only confirmed DC opamp gains were above 80 dB. A printed board test setup could have allowed better readings. The unity gain bandwidths of the opamps were measured using the technique explained in Section 6.6.3. The conventional gain boosted opamp was measured to have 20 MHz and the differential gain boosted opamp had about 10 MHz bandwidth. The load capacitor at the outputs of the test opamps was estimated about 20 pF during testing. This explains the smaller than expected unity gain frequency measurements.



(a)



(b)

Fig. A.6 (a) Chip photograph of the differential gain boosted opamp.
(b) Chip photograph of the conventional gain boosted opamp.