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David J. Allstot

The ability to integrate designs from board level, multi-chip modules to single process solutions is highly attractive in today's PC multimedia industry. Saving board area and chip count will decrease the production cost of personal computing hardware and increase profitability. The ability to integrate analog circuit capability and it's reference circuitry with DSP cores and processors creates a highly profitable line of products. This possible line of products warrants research and development of the ability to produce high quality analog functionality in digital processes. Techniques for analog design in digital processes are valuable pieces of intellectual property.

Digital processes rarely include analog functionality and analog processes' feature sizes tend to be several generations behind those of the digital. Personal computing is a driving force behind today's integrated circuit market. The primary functionality of the PC utilizes mainly digital products. The most prevalent products are processors closely followed by Digital Signal Processing cores. In these cases analog functionality has been implemented at the board level in costly analog chip packages such as sound cards and reference systems. The ability to integrate all of the analog and digital functionality on a single die, even at a lower performance level is profitable and attractive option for today's PC multimedia industry.

Three amplifiers have been designed and tested in a digital CMOS process. The goal of this effort is to provide some insight into the feasibility of precision analog functionality in digital processes. Each amplifier has been tested with three types of resistors and

three types of capacitors readily available in digital processes. The results are tabulated and some insights into the design theory are presented. And finally some insight into amplifier topological choices when only specific passive components are available are shared.

Power Amplifier Design in Digital CMOS Processes

By

Brett E. Forejt

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APPROVED:

Redacted for privacy

Major Professor, representing Electrical and Computer Engineering

Redacted for privacy

Head of Department of Electrical and Computer Engineering

Redacted for privacy

Dean of Graduate School

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Power Amplifier Design in Digital CMOS Processes.

CHAPTER 1: Introduction

The ability to integrate designs from board level, multi-chip modules to single process solutions is highly attractive in today's PC multimedia industry. Saving board area and chip count will decrease the production cost of personal computing hardware and increase profitability. The ability to integrate analog circuit capability and its reference circuitry with DSP cores and processors creates a highly profitable line of products. This possible line of products warrants research and development of the ability to produce high quality analog functionality in digital processes. Techniques for analog design in digital processes are valuable pieces of intellectual property.

Digital processes rarely include analog functionality and analog processes' feature sizes tend to be several generations behind those of the digital. Personal computing is a driving force behind today's integrated circuit market. The primary functionality of the PC utilizes mainly digital products. The most prevalent products are processors closely followed by Digital Signal Processing cores. In these cases analog functionality has been implemented at the board level in costly analog chip packages such as sound cards and reference systems. The ability to integrate all of the analog and digital functionality on a single die, even at a lower performance level is profitable and attractive option for today's PC multimedia industry.

Digital processes lack several key components needed for analog functionality including resistors values that are accurately predicted and have very little dependence upon temperature and process variations. Consequently, capacitors that are dense and have high linearity are preferable as design components in analog design. Digital CMOS processes lack these components and in fact have few options as their replacements.

Digital designs rarely need any components other than the complementary N and P channel devices and therefore the modeling and processing of other types of components is given very little consideration compared to those in analog CMOS processes. With all of these limitations considered, high performance analog design using digital technology may be difficult at best.

The elements that are available in digital process are limited to simple, cost effective components. Exotic solutions which may decrease yield and/or increase cost of manufacture are avoided. There are three resistive elements available that are presented. First is the silicide blocked poly resistor. This is a highly linear resistor but the density is low. Second is the N-WELL resistor. The density is very good but, there are multiple problems. Both the voltage and temperature linearity are very low and the absolute value of the resistance varies greatly over process, voltage, and temperature variations. The third and final resistive element is a trioded MOSFET. While the density is somewhat higher than that of N-WELL, it is very non-linear. There are applications in amplifier design where the trioded MOSFET may be desired to match some other transistor element in the circuit.

There are also three capacitive elements that have been chosen for study; namely, metal sandwich capacitors, n-channel over N-WELL capacitors, and FET capacitors. The metal sandwich capacitors have good linearity but poor density. The n-channel over N-WELL capacitors are simply natural threshold voltage transistor gate capacitors. Their density is very but the linearity is poor. MOSFET gate capacitances have a much higher density than that of the sandwich capacitors. They also have a voltage linearity similar to that of the n-channel over N-WELL capacitor. These capacitor elements force a serious trade-off between linearity and die area.

Analog processes give the analog designer many advantages over digital processes. The passive components are specified rigorously and there are typically several extra active components such as bipolar transistors and variants of the MOS transistor. Bipolar transistors are used in bandgap references, and if they are of high enough quality they can be used in amplifier design.

Low threshold voltage MOSFET's are useful in today's technology due to the shrinking values of the power supplies and when headroom is an issue these devices can be a valuable asset. The difficulty of analog design greatly increases with the unavailability of each of these components.

Each analog block has its own set of sensitive parameters. Band-gap circuits are highly dependent upon low temperature co-efficient, high linearity, and highly accurate resistor matching. Band-gap circuits are difficult to create without bipolar technology. If the specifications or the modeling of the passive components are not available for the process, these reference systems may not function properly and adversely affect the entire analog block.

Power amplifier design uses both resistors and capacitors and relies heavily upon their quality to achieve high Total Harmonic Distortion (THD) performance. The die area of the power amplifier is heavily dependent upon the size of the compensation capacitors. If the density of the capacitors is low in the process the die area can soar which reduces the profitability of the product. Some of the applications for power amplifiers in audio multimedia include microphone, speaker, and line drivers. In these cases the loads are very large compared to any on-chip load and require large application specific amplifiers with large on chip resistor and capacitor components. The performance of these amplifiers is heavily dependent upon the quality of the on-chip passive elements.

Byrkett [1] presents a discussion of a single amplifier topology with three types of compensation capacitors, a parallel combination of a N and P channel devices, gate channel capacitances in parallel with gate-bulk capacitances, and a metal sandwich capacitor. Their merits are discussed and evaluated. However, non-linear resistors are not evaluated for on-chip applications. When an amplifier is implemented in a product situation, it includes a feedback network to set the gain. In continuous-time systems this network is comprised mostly of resistors. Their area and linearity can have a profound impact upon circuit performance. Also, only a single topology is presented. The design space for amplifiers is quite large and other topologies may react differently to these components.

All other references cited [2-45] here do not include any analysis of the effects that non-linear passive elements have on circuit performance. Allstot and Black's paper [47] discusses all different possible passive components available in CMOS processes and their relative merits. However, in today's digital processes some of these elements may no longer exist and most likely are not modeled. If the components are modeled, it is done on a one-time basis and is not kept current through the lifetime of the process. The suspect availability and/or the accuracy of the models makes the task of creating precession analog designs in digital CMOS processes quite challenging.

In this text the study of three different amplifier topologies in a specific system is reviewed. To make the study as broad as possible the three amplifiers are chosen to be as distinct as possible. Therefore we chose topologies from the literature which have strong performances in non overlapping specifications. Power efficiency, size, THD, power supply rejection ration, slew rate, and settling responses are all prime choices for testing. Each amplifier shall be evaluated based upon these parameters.

The first amplifier chosen from [48] is a classical two-stage amplifier. It is has a particularly good power efficiency and power supply rejection ratio but has a non-symmetrical output swing which hurts the distortion performance. The second amplifier [49] is a non classical topology. It is a 4 stage nested miller compensated amplifier designed to drive a large resistive and capacitive load. This amplifier has tremendous gain and harmonic distortion performance but its design is quite complicated. The third and final amplifier [50] is a hybrid two-stage design which combines a typical first stage design with class-AB biasing scheme into the first stage. It uses only two transistors as the output stage. The final amplifier has great power efficiency but it has problems with stability and DC biasing in low supply environments.

The system in which these amplifiers are implemented is a simple inverting fixed gain power amplifier. In the typical systems the pre-amplification is realized using either programmable gain amplifiers or audio band mixers as the pre-stages.

The gain in which the amplifier is fixed can be as high as 12 dB and nominally is 0 dB. For simplicity the gain is set to unity in these designs and all analyses are performed at this gain. Each amplifier will be designed and evaluated for this test case.

In Chapter 2, the theory and reasoning of the amplifier design, the effects of non-linear components on such a design, and a system analysis of the test circuit are each described. Key performance parameters for the design of an amplifier are discussed and a review of the design methodology presented. Also presented in the chapter are some methods for hand calculation of the THD of these amplifiers and the system as well as several compensation schemes. A description of the sensitivity of the designs to non-linear components is provided in combination with some calculations. A topological view of the application circuit and the performance impact of non-linear components on that circuit are provided. A conceptual view of the design process of three amplifiers in a single system along with its specifications is demonstrated in Chapter 2.

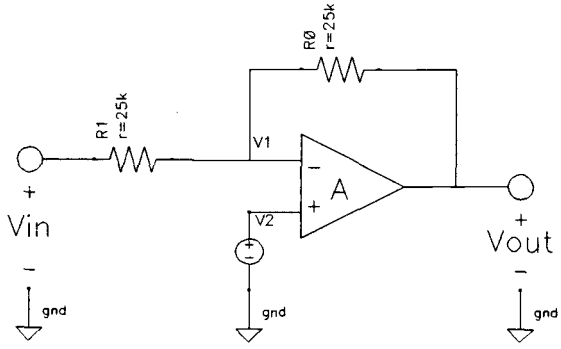
Chapter 3 includes detailed information of the design of the amplifiers on a transistor level. Performance characteristics are determined and presented and insights into the application of each amplifier are added. Chapter 4 include experimental simulation results. For the purposes of this text, only simulations are presented since the silicon will not return in a timely fashion. In order to replace the absence of silicon, statistical modeling is used to improve confidence in the performance and yield of these circuits. Five categories have been chosen to be statistically modeled. These categories are open-loop small-signal performance, power supply rejection ration, noise, THD, and the settling response to an input step. Chapter 5 outlines some conclusions, practical solutions for power amplifier design, and possible solutions for processing of passive components.

CHAPTER 2: Design Theory and Reasoning

In PC audio applications there is a need to drive low impedance loads such as speakers or headphones. In such applications the impedance can be as low as 32 Ω. With such a low load impedance, a system with a variable gain pre-amplifier and fixed gain power amplifier is chosen. In this chapter the system requirements for a the fixed gain power amplifier stage are presented and reviewed. Also, the impact of non-linear passive components in the system both inside the amplifier (compensation techniques) and the external feedback network (fixed gain) is analyzed and presented.

There are two basic fixed gain configurations: inverting and non-inverting. An inverting buffer was chosen as the drive stage over a non-inverting buffer to keep the voltage swings at the input nodes of the amplifier to a minimum. In a non-inverting stage the input is connected directly to the positive input terminal of the amplifier and the amplifier is connected with a unity-gain shunt from the output to the negative input terminal. When connected as such, the voltages at both input terminals swing with the same magnitude as that of the input signal. When the voltages at both input terminals of the amplifier move on this order, the operation point of the amplifier changes and directly effects the DC gain. It will be shown later that gain changes are some of the main sources of harmonic distortion. An inverting configuration is pictured in Figure 2.1.

Figure 2.1. **Inverting output buffer**



In the inverting case, the negative feedback caused a "virtual short" between the positive and negative input terminals. The term "virtual short" describes the fact that the positive input terminal is connected to a reference voltage and the voltage on the negative terminal moves by an amount that is proportional to that of the input and inversely proportional to that of the gain. Equation 2.1 shows this relation,

$$V_1 = \frac{V_{in}}{(A+2)} \qquad \text{(EQ 2.1)}$$

where A is the DC gain of the amplifier. Equation 2.1 shows that if A is large, the voltage swing on node V_1 is reduced by a factor of A. Now the amplifier is biased into a nearly constant condition that varies only slightly with the swing of the input. This eliminates any harmonic distortion that is caused by common mode swing on the inputs.

A drawback to the inverting configuration is the overall input impedance of the system. The input impedance is now solely determined by the input resistor. In the non-inverting configuration, the input impedance is that of the amplifier. In CMOS amplifiers the input impedance is very large because the input of most voltage amplifiers is the gate of a MOSFET. The gate terminal of a MOSFET is known to have nearly infinite DC input impedance. To create a large input impedance in the inverting configuration, the values of the resistors must be large. Large resistors (large input impedances) have problems with thermal noise performance and small resistors will force the preceding stage to have larger load handling capability. Increased load drive capability will increase the power dissipation of the stage, the area occupied by the stage, or both. Clearly there is a design trade-off between the noise of the input resistor and the drive capability of the preceding stage.

The circuitry shown in figure 2.1 is intended as an off-chip driver on integrated system chips where audio output capability is desired. Into 32 Ω, the specifications are an output swing of 2 V peak-to-peak, Total Harmonic Distortion (THD) of less than -70 dB @ 1 KHz, and an output step that has less than 6% overshoot to a 2 volt 10 V/μs input step. Also, the output must not ring when perturbed by the same input step. These performance

specifications are fairly stringent for power amplifier applications. In Chapter 3 the designs of three amplifiers that meet these specifications are discussed.

The only remaining components used in this system are the resistors that comprise the feedback network. In an on-chip application, we are limited to only a few choices of resistors. N-well resistors, silicide blocked poly resistors, and linear MOSFET's are all options for use and their relative merits were discussed in Chapter 1. Attention now turns towards the amplifier and its specifications. Without a properly designed amplifier the system will have little hope of meeting specifications.

For all of the following calculations Figure 2.2 is assumed to be the system. In this figure the classical two-stage amplifier is shown as a block diagram consisting of resistors, capacitors and transconductances. Each stage is modeled as a transconductance with an equivalent load resistance and capacitance. The DC gain of the amplifier is given by

$$A_{Vdc} = g_{m1}g_{m2}R_1R_2 \qquad \text{(EQ 2.2)}$$

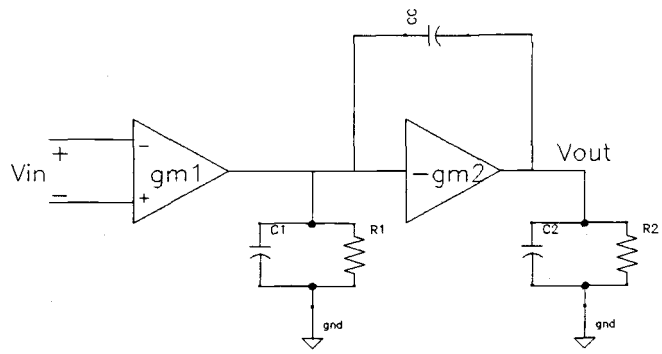
and the poles and zeros of the system are approximately

$$\omega_{p1} = -\frac{g_{m1}}{A_{Vdc}C_C},\ \omega_{p2} = -\frac{g_{m2}}{C_2},\ \omega_{z1} = \frac{g_{m2}}{C_C}\ . \qquad \text{(EQ 2.3)}$$

From equations 2.2 and 2.3 it is apparent that the first pole is inversely proportional to the compensation capacitor value. If the compensation capacitor has a non-linear voltage dependence then so will the pole frequency. This variation can cause harmonic distortion which will be discussed later. In order to maintain the stability of the amplifier, good phase margin and gain margin must be maintained. To maintain the phase margin, a good rule of thumb is to keep the second pole at least two octaves above the frequency of the first pole. The design must take into account the minimum C_C[1] value possible and adhere to the rule of thumb in order to keep good phase margin.

1. The variations of C_C due to its voltage dependent non-linearity.

Figure 2.2. **two-stage amplifier block diagram**

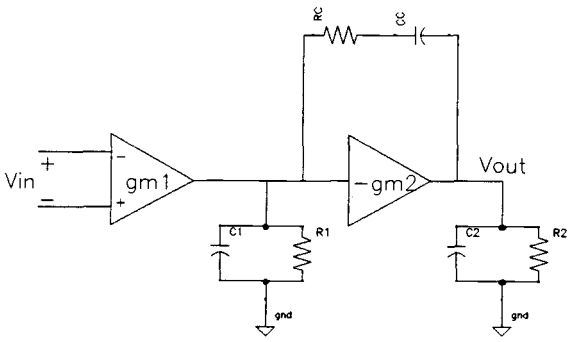


The gain margin is similar to the phase margin in this two pole system. The definition of the gain margin is the difference between unity-gain and the gain when the phase crosses 180^{o}. Obviously a positive value means an unstable system and a larger negative value means a more stable system. If the second pole is brought closer to the unity-gain frequency, the gain margin is increased but the phase margin decreases. There is a trade off between the "realistic" values of gain margin and phase margin. Compensation techniques are used to position the poles in the system to make this trade off. One technique is shown in figure 2.2. C_C is the compensation capacitor added to the system to "split" the poles.

Compensation is an integral part of amplifier design. There are many different techniques that are available; Miller compensation and shunt compensation are two examples. In all cases there is a need for high density, high linearity capacitors. In that lies the problems of designing analog circuits in a Digital CMOS process. The only available capacitors include metal sandwich capacitors, n-poly over N-WELL, and FET gate capacitances. Each of these capacitors has serious drawbacks. Metal sandwich capacitors occupy very large die areas per unit of capacitance but they have very good linearity. N-poly over N-WELL capacitors are quite non-linear but they are very dense. FET gate capacitances have possible back gate parasitics, non-linearity similar to that of the n-channel over N-WELL capacitors, but have high density. Some calculations to show the effects of both non-linear capacitors and resistors on performance of an amplifier follow.

Another system of compensation is shown in Figure 2.3. Here the compensation capacitor is replaced with the series combination of a resistor and a capacitor. Adding the

Figure 2.3. **two-stage with RC compensation.**



resistor to the system produces a third pole and provides the ability to move or eliminate the zero. The DC gain of the system remains unchanged and the new pole/zero locations are given by

$$\omega_{p1} = -\frac{g_{m1}}{A_{Vdc}C_C}, \omega_{p2} = -\frac{g_{m2}}{C_L}, \quad \omega_{p3} = \frac{-1}{R_C C_1}, \omega_{z1} = \frac{1}{C_1\left(\frac{1}{g_{m2}} - R_C\right)}. \quad \text{(EQ 2.4)}$$

There are several options for the positioning of the zero. One option is to cancel the zero exactly and therefore reduce the complexity of the system. The problem with this technique is that a resistor and a transistor transconductance do not track each other with process, voltage, or temperature variations. There are techniques where a transistor that is biased in linear is used as a resistor and the conductance of a linear FET will better track with a transconductance. This may be acceptable to use in high bandwidth applications, but there may still be an inexact cancellation of the pole zero pair. Using a linear FET as the compensation resistor has the major drawback that the impedance of the linear FET is non-linear with the voltage across its terminals. The FET may even turn off for certain

portions of the output swing and the amplifier will be uncompensated. A second possibility is to move the zero into the left half plane to cancel the second pole. This technique allows for an increased bandwidth but, again the positioning of the zero must track with the pole location over process, voltage, and temperature. If it does not, the a pole/zero doublet will be formed and the transient response may not be acceptable.[1] The third option is to move the zero into the left half plane just far enough beyond the bandwidth to render it harmless. It is important that the zero remain in the left half plane for all conditions or the stability will suffer. The design must take into account the variations of the transconductance and the resistance for this to be accomplished.

One of the most important specifications in audio/multimedia applications is Total Harmonic Distortion (THD). The compensation technique chosen has a direct bearing upon the THD of the amplifier. As discussed earlier, in RC compensation the location of the zero is very important to stability of the amplifier. In all designs used here, the zero is chosen to be placed just to the left of the bandwidth to render it harmless. In order to meet the step response requirement of the system, it is an important not to have any pole zero doublets and therefore the pole/zero cancellation technique is avoided. The linearity of the compensation resistor is immaterial as long as the zero remains in the left half plane.

The compensation capacitor has a great impact upon the THD of the amplifier. The bandwidth of the system is directly proportional to the value of the compensation capacitor,

$$BW = \frac{g_{m1}}{C_C} \qquad \text{(EQ 2.5)}$$

In order to analyze the effect of the capacitor variation at a specified frequency, the approach outlined in [51] is followed. Here, the amplifier is connected as a non-inverting buffer and the gain at 1 KHz is found over a range of DC input voltages. Using the maximum, minimum, and quiescent gains from this analysis the second-order and third-order

1. Pole/zero doublets create long settling times and large overshoots even when the phase and gain margins predict otherwise.

fractional harmonic distortion components can be estimated. Assuming that we have the relation,

$$V_O = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + \ldots . \quad \text{(EQ 2.6)}$$

the derivative is taken to get the small-signal gain for the input defined as

$$V_{in} = \hat{V}_{in} \cos \omega t . \quad \text{(EQ 2.7)}$$

The maximum, minimum, and quiescent gains are derived to be

$$A_{max} = a_1 \hat{V}_{in} + 2a_2 \hat{V}_{in} + 3a_3 \hat{V}_{in}^2 + \ldots \quad \text{(EQ 2.8)}$$

$$A_{min} = a_1 \hat{V}_{in} - 2a_2 \hat{V}_{in} + 3a_3 \hat{V}_{in}^2 - \ldots \quad \text{(EQ 2.9)}$$

$$A_Q = a_1 . \quad \text{(EQ 2.10)}$$

Equation 2.8 is arrived at when the cosine's value is +1, equation 2.9 when it is -1, and equation 2.10 when it is zero. Now define the differential gains as

$$E_p = \frac{A_{max} - A_Q}{A_Q}; \; E_n = \frac{A_{max} + A_Q}{A_Q} \quad \text{(EQ 2.11)}$$

$$E_p = \frac{2a_2 V_{in} + 3a_3 V_{in}^2}{a_1} \quad \text{(EQ 2.12)}$$

$$E_n = \frac{-2a_2 V_{in} + 3a_3 V_{in}^2}{a_1} . \quad \text{(EQ 2.13)}$$

With these definitions and making the observation that

$$E_p - E_n = 8HD_2 \quad \text{(EQ 2.14)}$$

$$E_p + E_n = 24HD_3 . \quad \text{(EQ 2.15)}$$

where HD_2 is the second harmonic distortion component and HD_3 is the third-order component as found in [52]. Finally the THD is defined as

$$THD = \sqrt{(HD_2)^2 + (HD_3)^2}. \quad \text{(EQ 2.16)}$$

The preceding calculation was chosen over other techniques because in many cases the capacitor voltage coefficients are not supplied in the models. Without these coefficients, calculations in other techniques would not be possible. In some cases a look-up table of the capacitance values over applied voltage or the absolute min/max/nom values are supplied. This calculation allows the THD to be estimated regardless of capacitor models supplied.

The slew rate is limited by the tail current source in the first stage (differential stage) of the amplifier and the value of the compensation capacitor. Again the variance in the compensation capacitor value must be taken into account. For the slew rate, only the maximum value of the compensation capacitor is the important parameter. The slew rate is defined as

$$SR = \frac{I_{tail}}{C_C}. \quad \text{(EQ 2.17)}$$

The larger the variance in the capacitance the larger the tail current must be to meet the minimum slew rate specification.

In some topologies, there is a series shunt capacitance between the output and the positive supply rail. This leads to decreased Power Supply Rejection Ratio (PSRR) at higher frequencies. If the capacitor varies with the output voltage, then the minimum PSRR will be defined when the capacitor is at its maximum. As long as the size of the compensation capacitor needed to produce the desired bandwidth/stability does not create a PSRR problem there is little concern. In the case where high PSRR applications are needed, other topologies should be investigated. In Chapter 3 an amplifier with superior PSRR is designed and discussed [Babanezhad].

Indirectly the capacitive load capability is determined by the compensation capacitor size. With the relation

$$\frac{g_{min}}{C_{comp}} < \frac{g_{mout}}{4C_L} \qquad \text{(EQ 2.18)}$$

(which was defined as a "rule of thumb" earlier), it can be seen that the phase margin will degrade with either increased load capacitance or decreased compensation capacitance. Therefore the value of the compensation capacitor must be designed for the maximum load capacitance. The value determined from this calculation is the minimum that the compensation capacitor can be over process, voltage, and temperature variations.

The compensation capacitor is a fundamental parameter in determining bandwidth, THD, slew rate, and stability of the amplifier. Its characterization is integral to the design and performance of the circuit. The dependence of these parameters upon the capacitor value and linearity have been outlined in the previous sections. Understanding the variations and non-linearities of the capacitors allows the designer to produce robust and manufacturable designs.

Now that the amplifier has been qualified and its specifications analyzed, the rest of the system shall be analyzed. The remaining portion of the system is the global feedback network pictured in Figure 2.1 with the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{-R_0}{R_1}\left(\frac{1}{1+\frac{R_0+R_1}{AR_1}}\right). \qquad \text{(EQ 2.19)}$$

Since A >> 1, the relation reduces to

$$\frac{V_{out}}{V_{in}} = \frac{-R_0}{R_1}. \qquad \text{(EQ 2.20)}$$

The resistors of system are non-linear with applied voltage and follow the relation

$$R = R_{ideal}(1 + a_1 V + a_2 V^2) \quad . \qquad \text{(EQ 2.21)}$$

Combining equations 2.20 and 2.21 yields

$$\frac{V_{out}}{V_{in}} = \frac{-R_{ideal0}(1 + a_1 V_{in} + a_2 V_{in}^2)}{R_{ideal1}(1 - a_1 V_{in} + a_2 V_{in}^2)} \quad . \qquad \text{(EQ 2.22)}$$

Since $R_{ideal0} = R_{ideal1}$, these values cancel. After some manipulation and neglecting the higher order terms it is concluded that

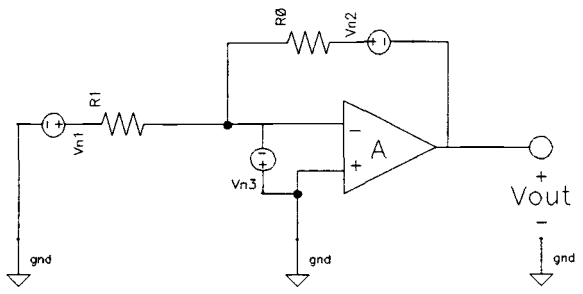
$$V_{out} = V_{in} + 2a_1 V_{in}^2 + 2a_1^2 V_{in}^3 . \qquad \text{(EQ 2.23)}$$

Now using the relations derived in [53] the fractional harmonic distortion components are defined as

$$HD_2 = a_1 , HD_3 = \frac{a_1^2}{2} \qquad \text{(EQ 2.24)}$$

and the Total Harmonic Distortion is defined in equation 2.16. It has been shown that in the case of a unity-gain buffer, the even order terms of the resistor non-linearity cancel. Only the odd order harmonics contribute to the distortion of the system. In some cases, the system THD performance will be dominated by the resistor non-linearity. In applications where very low THD must be attained, it is critical to use linear resistors in the feedback network.

Figure 2.4. **Buffer with noise sources V_{n1},V_{n2}, and V_{n3}.**



The final critical performance parameter left to analyze is the noise of the system. Each component of the system has a noise source associated with it. The amplifier noise is determined as an input referred quantity and is shown in figure 2.4 as V_{n3}. In Chapter 3, a detailed analysis of noise is described for the three amplifiers chosen as test cases; therefore, amplifier noise will not be discussed here. The resistor noise power is defined as

$$P_{rnoise} = 4KTR\Delta f. \qquad \text{(EQ 2.25)}$$

The total output noise of the system is the important parameter. Using superposition to find the total output noise voltage due to V_{n1},V_{n2}, and V_{n3},

$$\overline{V^2_{outnoise}} = \overline{V^2_{n3}}\left(1+\frac{R_0}{R_1}\right)^2 + 4KT\Delta f R_1\left(1+\frac{R_1}{R_0}\right). \qquad \text{(EQ 2.26)}$$

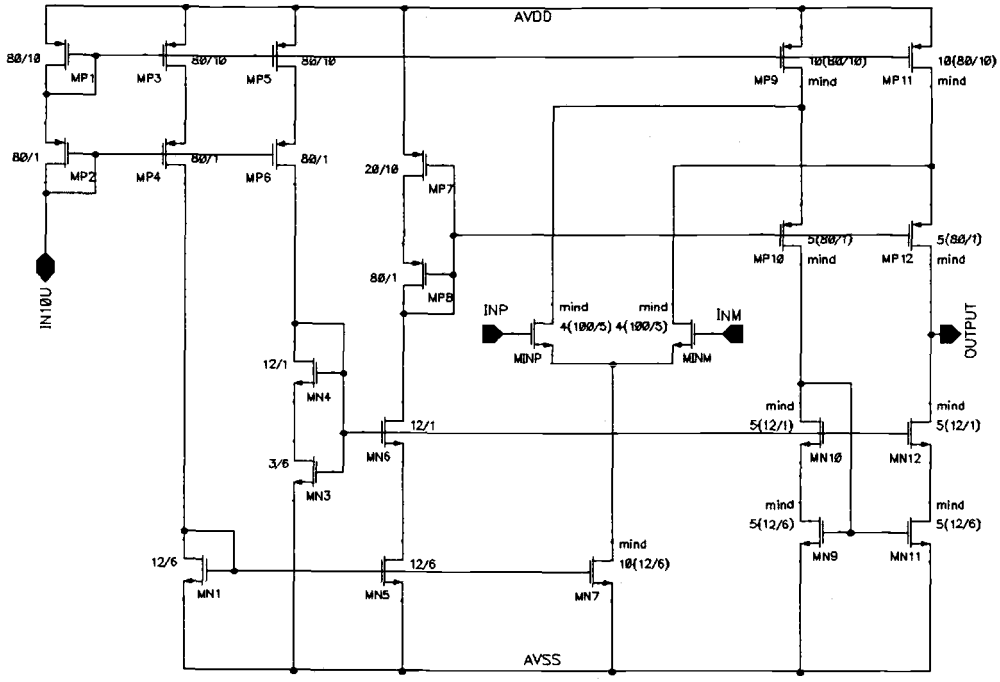
An inverting configuration fixed gain power amplifier has been presented and its performance goals have been defined. This amplifier is needed in PC audio/multimedia applications in order to drive speakers and headphones. Since this system is implemented in CMOS which lacks quality linear passive components, the effects of non-linear passive components on the amplifier performance have been presented.

In Chapter 3, various amplifier topologies are designed and reviewed. These topologies were chosen to be distinct from each other in order to span as large a range in the design space as possible. Chapter 4 presents the simulation results of these amplifiers in the system discussed in this chapter using the non-ideal passive components presented in Chapter 1.

CHAPTER 3: Circuit Design

Three amplifiers have been chosen from the literature to provide test cases for the theories stated in Chapter Two. Babanezhad[48], Castello[49], and Huijsing[50] each have distinctive topologies, advantages, and disadvantages. Babanezhad's amplifier is a two-stage amplifier, Castello's amplifier is a 4 stage amplifier with Nested Miller Compensation, and Huijsing is a hybrid two-stage amplifier. These topologies have been chosen for their separate and distinct capabilities. A description of the design of each amplifier follows as well as some observations of their potentials and limitations.

Figure 3.1. **FCC schematic**



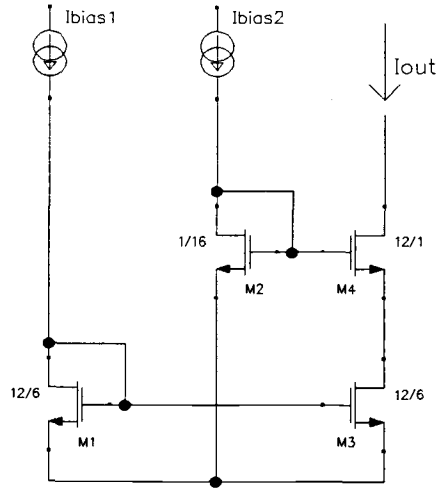
The first stage of the each of the amplifier topologies shown in Figure 3.1 is a folded cascode (FCC) amplifier. The FCC amplifier was chosen because of its excellent ability for driving capacitance and high impedance loads. The gain is the input device transconductance multiplied by the output impedance. This value is severely degraded by low

impedance loads. The large output impedance gives the FCC a very large single stage gain with an approximate single-pole response; the FCC has a large gain-bandwidth per power ratio. However, the stage has a limited swing range especially in high swing, low supply environments.

Low voltage applications of the FCC architecture require a few special biasing techniques. The FCC amplifier will swing within a $V_t + 2V_{dsat}$ of each rail if normal cascode mirroring is used. In this amplifier, the biasing is "high swing" and will allow the FCC to swing within $2V_{dsat}$ of the rails. Figure 3.1 depicts the stage as used in the designs.

A classical high swing biasing technique is shown in Figure 3.2. Here two legs with two diode connected devices M1 and M2 are used to create two bias voltages at a $V_t + V_{dsat}$ and $V_t + 2V_{dsat}$ respectively. However, this technique does not match well. First, the device M2 will not have any back gate biasing effect whereas the intended biased devices have back gate biasing. Secondly, M2 needs to have a large V_{ds} in order to compensate for the back gate biasing of the intended biased devices. If this is not the case, M3 will be driven into the linear region of operation.

Figure 3.2. **High swing biasing.**



In Figure 3.1, MN3 and MN4 replace M2 (Figure 3.2) and create a matching bias voltage. MN4 is guaranteed to be saturated and MN3 is designed to be in non-saturation. MN4's size matches that of the cascode devices in need of biasing and MN1 matches the biased rail device sizes. MN3 is sized such that its length is the same as that of MN1 and the width of MN3 sets the voltage at the source of MN4. The W/L ratio of MN3 is typically 1/8 of MN1. This technique lowers the V_{ds} across the diode device (M2/MN4) and gives MN4 a matching back gate bias to that of its biased counterparts.

Since the FCC has been chosen to be the first stage for all three topologies, a good design is critical. A good first stage design has low noise, high gain, high bandwidth, and low power and each of these requirements must be met in a low voltage environment. If designed properly, the FCC amplifier has low noise (although not as low as a simple differential pair), large gain, and high bandwidth, but area and power are traded for this performance. It is now useful to discuss the advantages and disadvantages of the FCC architecture.

As compared to a simple differential pair, the folded cascode has very high gain and exhibits excellent power supply rejection ratio (PSRR). This makes the FCC an excellent choice for a high gain first stage in any multi-stage architecture.

A disadvantage of the folded cascode architecture is its noise compared to that of a simple differential pair. In a simple differential pair with current mirror loads, the noise is determined by the input and current mirror load devices. In the folded cascode the noise is dependent upon the input devices, the current mirror, and the added load devices. Therefore there are 2 more noise contributing devices in the FCC compared with the simple differential pair.

Careful design for noise considers both, thermal and flicker (or 1/f) noise of a MOSFET [50].

$$\frac{\overline{v_{in}}^2}{\Delta f} = \frac{8}{3} \bullet \frac{kT}{g_m} + \frac{K_f}{WLC_{ox}f} \qquad \text{(EQ 3.1)}$$

where k is Boltzman's constant, T is the operating temperature, g_m is the transconductance of the device, K_f is the flicker noise constant, W is the width, L is the length, C_{ox} is the oxide capacitance and f is the frequency of interest. This equation interprets the noise power of a MOSFET as a root mean square input referred voltage. The first term is the thermal noise component and the second term is the flicker or 1/f noise.

Applying this knowledge to the folded cascode circuit yields equations for the overall noise of the amplifier[54]. These results can be taken further to find optimum lengths of the respective device pairs for a given g_m of the devices. This optimum sizing equation[53] is shown in equation 3.2. The device transconductance is set independently of this equation by the thermal noise requirements.

$$\frac{1}{L_{in}^2} = \frac{2\mu_{load}K_{fload}}{\mu_{in}K_{fin}} \bullet \frac{1}{L_{load}^2} + \frac{1}{L_{mirror}^2} \qquad \text{(EQ 3.2)}$$

The specification for noise in this design is an integrated, A-weighted quantity that is less than 4 μV. In order to meet this specification, a common low noise technique is adopted choosing a "corner" frequency where the dominance of the flicker component and the thermal component are approximately equal. Using this frequency as a design parameter the areas and the transconductances of each MOSFET can be calculated. The thermal noise component is dependent upon temperature and transconductance. Temperature cannot be controlled, but the g_m is a function of power dissipation and implies that higher noise performance demands higher power. Flicker noise is a function of device area, oxide capacitance (C_{ox}), frequency, and K_f. K_f or the flicker noise constant is solely a process determined parameter.

K_f parameters are of little interest in digital design due to the binary nature of the data and thus are not critical process parameters. This yields K_f values that can vary by several orders of magnitude. In drastic contrast with digital CMOS processes, analog CMOS processes maintain strict control of the flicker noise constant. Large K_f values have severe impacts upon device sizings (equations 3.1 and 3.2) and large devices have large parasitic

capacitances which can affect stability, bandwidth, and power consumption. Ideally, K_f should be tightly controlled at a minimum in the process for low noise designs.

Since we are designing in a digital CMOS process the overall area of the devices is the most critical parameter for a stable low noise design. The larger the area, the lower the flicker noise component. As stated previously, with increased size comes increased parasitic capacitances. These parasitics can introduce two poles and a RHP zero from the high swing mirrors in the FCC which may degrade the stability of the amplifier. By following careful design practices a good balance between the g_m (power) and area of the devices will yield low noise and high performance with minimal area.

The gain of the FCC is known to be g_{min}/g_{out}. In order to achieve moderate gain values, g_m must be large and g_{out} small. There are several other considerations for the g_m of the input pair that must be taken into consideration. Firstly, the bandwidth in multi-stage designs is typically g_{min}/C_{c1}, where C_{c1} is the compensation capacitor from the overall output of the amplifier to the output of the first stage. In order to keep C_{c1} small, g_{min} must also be small. Secondly, the thermal noise has a direct dependence upon g_{min}. Equation 3.1 shows that the larger g_m, the lower the thermal noise component. Third, since g_m is directly proportional to the current through a device with constant $(V_{gs} - V_t)$, low power demands low g_m values.

In this design, the input transconductance is determined by the noise specifications and is moderately large. It can be inferred that in low thermal noise designs the input g_m is naturally high and so the gain will also be moderately high given a moderately high output impedance. Again, assuming low noise design, the lengths of the devices are fairly long in order to keep the flicker noise contribution low. This produces very small values of g_{out} in a cascoded load or mirror. Therefore, moderate gain is a natural product of low noise FCC design.

The bandwidth of the first stage is determined by its transconductance and the load capacitance. The load capacitance is usually the sum of a gate capacitance (which is the input of the second stage) and a compensation capacitance (in this case, C_{c1}). In most

applications the compensation capacitance is much greater than the parasitic gate capacitance. Hence the load capacitance is approximately C_{c1}. Therefore the bandwidth is g_{min}/C_{c1}, and is a designable parameter with C_{c1} being the design variable.

It is very important to keep quiescent power dissipation to a minimum in most applications. The quiescent power of the FCC is determined by the tail current source, the two cascode legs, and the biasing network. Comparing these three sources, the tail current is nearly half the current as well as the two cascode legs. These minimum currents are determined by gain, bandwidth, and noise requirements. The biasing circuitry adds a small fraction to the overall power consumption of the FCC amplifier and is negligible in low noise designs. The power is determined by other specifications and is not a designable parameter.

The FCC stage has been designed to operate in a low voltage environment with low noise, moderate gain, and high bandwidth. The following table describes the performance parameters of this amplifier and Figure 3.3 shows plots of the AC and PSRR responses.

TABLE 3.1. FCC amplifier performance specifications.

Cload	DC Gain	Phase Margin	Band width	PSRR	quiescent POWER	Noise
65 pF	84.1 dB	86 deg.	1.96 MHz	-97db @20 KHz	77 μW	3.9 μV Integrated
10 pF	84.1 dB	71.5 deg.	11.9 MHz	-97db @20 KHz	77 μW	3.9 μV Integrated

Now that a robust first stage is available (the FCC), each of the three test case amplifiers is designed. Since the FCC has been designed for low noise and the input-referred noise of subsequent stages is divided by the multiplication of all gains up to that point, we can ignore noise considerations going forward. Noise considerations in subsequent stages

can be ignored since their contributions are divided by the sum of all gain up until the input of that stage. With that in mind, no effort is expended upon low noise design in the remaining design.

Babanezhad's amplifier is a classical two-stage power amplifier with non-symmetrical class-AB output. Asymmetry in an output stage can lead to clipping on one side of the wave form. This will yield a large third harmonic distortion component which is undesirable in audio band signals. class-AB stages cut the overall power consumption in power amplifiers by lowering the steady-state or quiescent power drain while having the ability to supply large currents needed for large voltage swings into large loads. Babanezhad's amplifier is shown in Figure 3.4.

The output stage of Babanezhad's amplifier consists of three parts: a source-follower amplifier M12, a common gate amplifier M13, and a current mirror M14,19. The source-follower provides a level shifting function and the common-gate amplifier provides some gain in the signal path. The current mirror provides the necessary phase inversion to the output as well as increasing the gain by the current mirror ratio, P. The output devices are a current source M19 and a common-source device M18. From [48] we get these sizing relations:

$$\left(\frac{W}{L}\right)_{12} = P\left(\frac{W}{L}\right)_{16} \quad \left(\frac{W}{L}\right)_{13} = P\left(\frac{W}{L}\right)_{17} \quad \left(\frac{W}{L}\right)_{18} = MP\left(\frac{W}{L}\right)_{15} \quad \left(\frac{W}{L}\right)_{19} = M\left(\frac{W}{L}\right)_{14} \tag{EQ 3.3}$$

and with these sizings the current relations are thus:

$$I_{M12} = PI_{M15} \quad \text{and} \quad I_{M(18,19)} = MPI_{M15} \tag{EQ 3.4}$$

The maximum output current in the pull-down direction is limited only by the K' and the size of the transistor;

$$Idown_{max} = \frac{K_n W}{2 L}(V_{DD} - V_{SS} - V_T)^2 \tag{EQ 3.5}$$

the maximum pull-up current depends upon the current source M20 and the absolute sizes of the transistors. This gives the ability to have very small quiescent currents with large drive current capability. This is an important feature of this amplifier and with careful design the power efficiency can attain a relatively large value.

$$Iup_{max} = \frac{MK_{12}K_{13}}{(\sqrt{K_{12}} + \sqrt{K_{13}})^2} \bullet \left(\sqrt{\frac{I_{M20}}{K_{15}}} + \sqrt{\frac{I_{M20}}{K_{16}}} + \sqrt{\frac{I_{M20}}{K_{17}}} + V_T \right)^2 \qquad \text{(EQ 3.6)}$$

The transconductance of the output stage is given by

$$g_{mout} = g_{m18} + M\left(\frac{g_{m12} \bullet g_{m13}}{g_{m13} + g_{m13}}\right) \qquad \text{(EQ 3.7)}$$

which shows that the output transconductance is limited to that of the final output mirror. Equation 3.7 also shows the dependence that g_{mout} has on g_{m13}. In order to keep an optimum transconductance for the output stage, the transconductances of M12 and M13 must be nearly equal. Otherwise, power efficiency will be lost along with drive capability.

In order to correctly DC bias the output stage, attention turns to the output of the first stage. It is observed that the output voltage needs to match the voltage at the drain of MN19 for minimal quiescent current offset in cascode legs of the FCC. Device M21 has been added for this purpose and its bias voltage is the same as the gates of MN18 and MN20. The voltage at the gate of M12 is determined by

$$V_{outFCC} = V_{gsM15} + V_{sgM16} + V_{gsM17} - V_{gsM13} - V_{sgM12}. \qquad \text{(EQ 3.8)}$$

Therefore the drains of MN18 and MN20 match to first-order in the quiescent condition and this minimizes any systematic offset due to current mismatch in the FCC amplifier.

Figure 3.3. **(A and B) Magnitude responses of the FCC amplifier.**

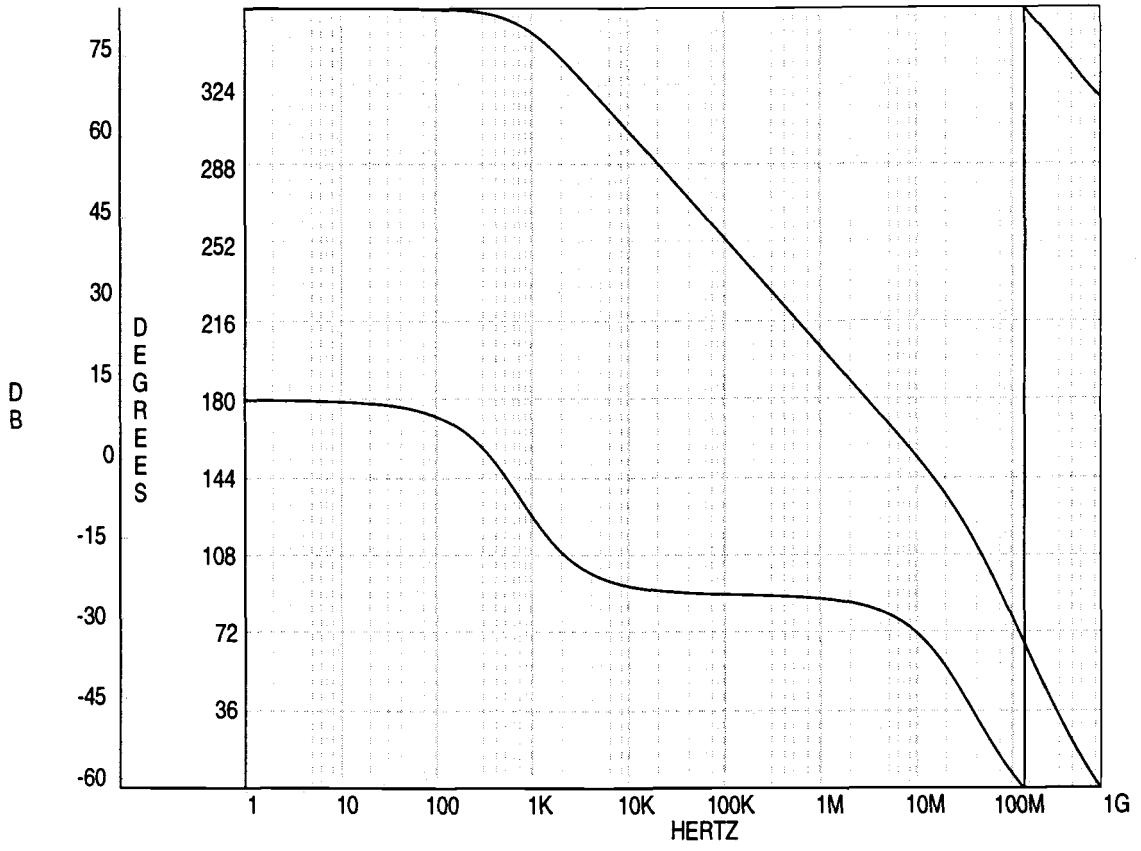
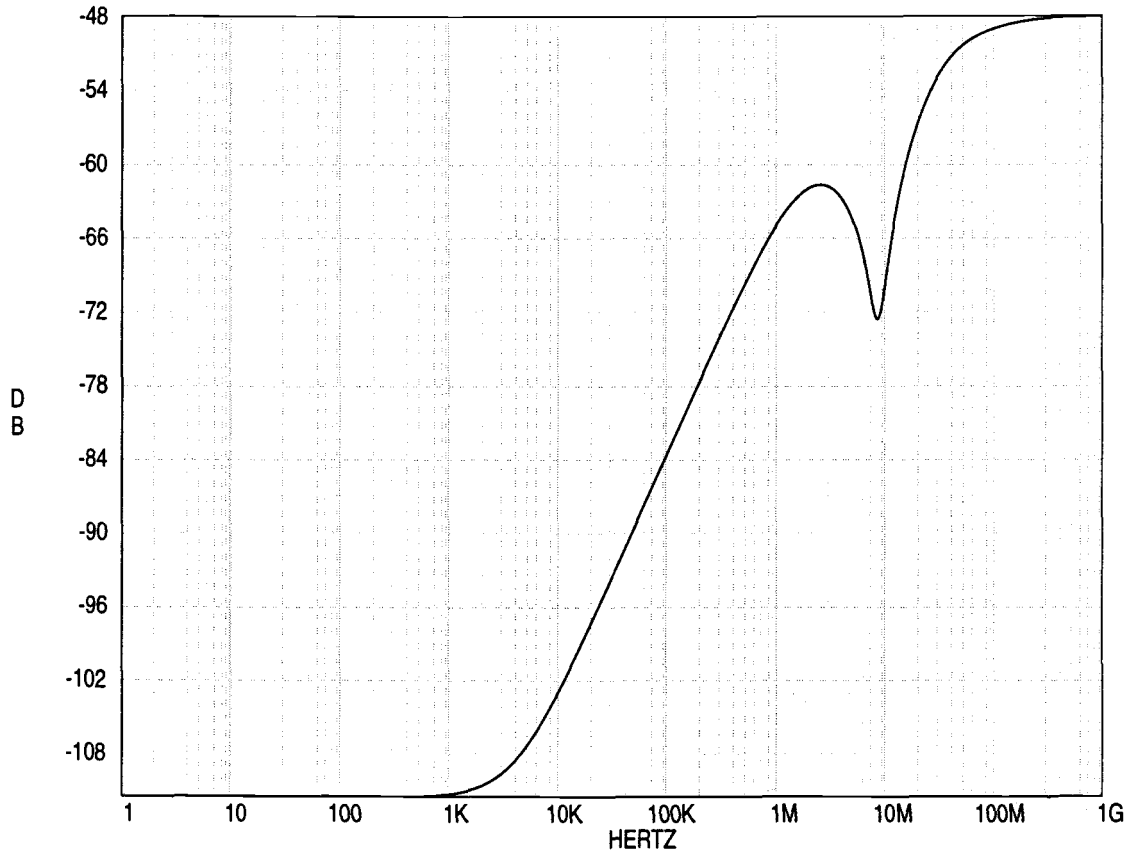
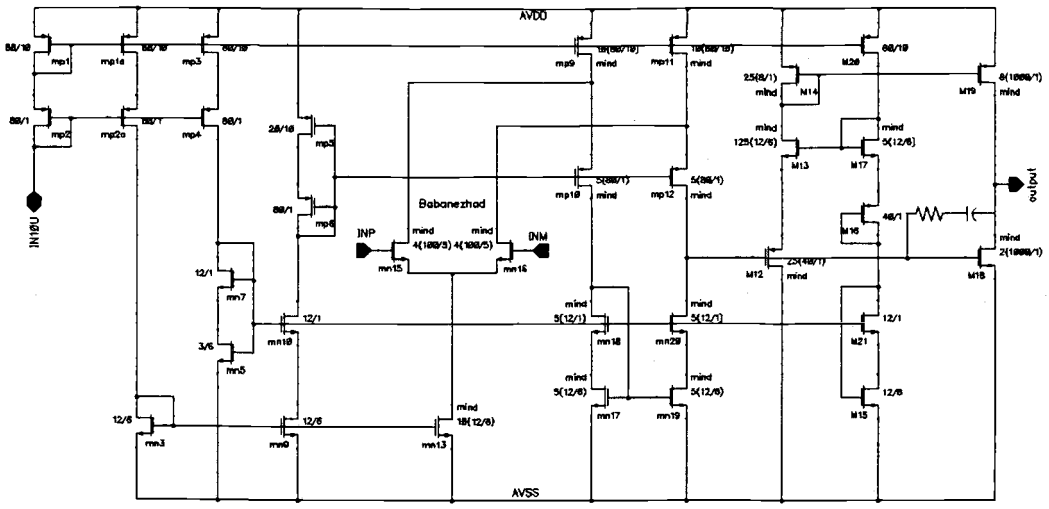


Figure 3.3. **(C)PSRR of the FCC amplifier.**



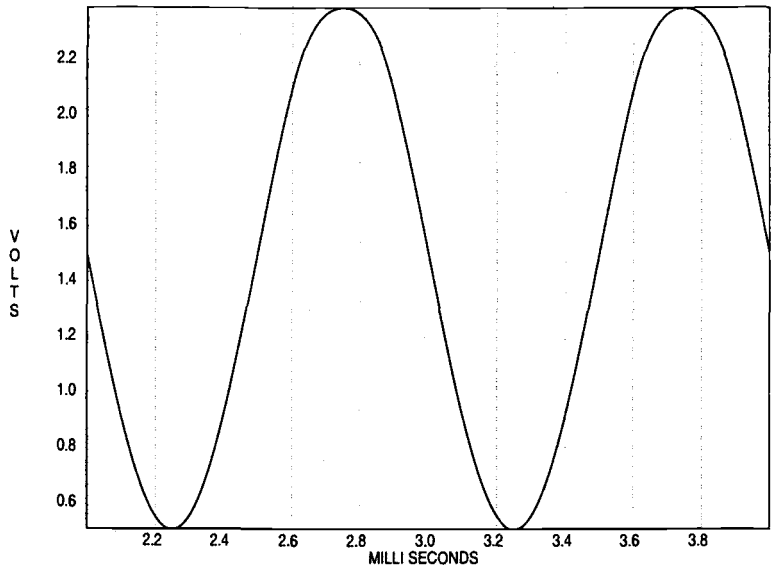
This output stage delivers low quiescent power and high bandwidth capabilities; however, the stage does not have a symmetrical drive response. This asymmetry introduces clipping further from AVDD than from AVSS when large output swings are demanded. Asymmetric clipping produces odd order harmonics and in particular the third-order harmonic is now the dominant term in the total harmonic distortion (THD). It is known that in high performance audio systems the third-order harmonics are less desirable than second-order harmonics in listening tests. An explanation of this is beyond the scope of this text and shall not be discussed. To maintain low third-order harmonics, it is imperative that the output does not clip within the specified swing range.

Figure 3.4. **Babanezhad's amplifier schematic**



During the design phase of Babanezhad's amplifier some observations have been made. First, the output stage transconductance must be much larger that the design equations predict. This is due to the inability of the p-channel current mirror to meet the swing requirements. Using the design equations to derive a g_{mout} that can drive 25 Ω in the worst case, the output swing is only +.83 V to -1 V (Figure 3.5). In this design, a swing of.7 V_{rms} is the specification and clearly the previous numbers fall short of the goal. The current source is designed to handle enough current to accommodate the load and the n-channel common-source amplifier in its quiescent condition. This assumes that g_{m18} remains unchanged throughout the signal swing and thus the current demand of M18 remains fixed for positive output swings. In reality g_{m18} changes with the drain bias. Positive output swings increases the current demand of M18. The current source M19 must be sized to accommodate the increased demand of M18 as well as the load current.

Figure 3.5. **Input is a 1 KHz sine wave with amplitude of 1V peak. Output is shown here and its maximum voltage falls short of the designed swing of 1V peak.**



A design that includes the increased demand of M18 with increased drain bias yields an output transconductance that is nearly 4 times the original designed value. This increase in g_m precipitates a power and/or area penalty. The power penalty will negatively effect the power efficiency of the amplifier and the area penalty not only increases cost of the part but adds extra parasitics to the circuit. These parasitics may cause stability problems especially in the final output mirror. The simulated performance results are summarized in Table 2.

Notice in Table 2 that Babanezhad's amplifier has excellent power supply rejection and the relatively slow settling times. The Power Efficiency factor is a little low, but it is believed that if careful optimization is applied the Efficiency factor could rise to approximately 10. The power efficiency factor is defined as follows

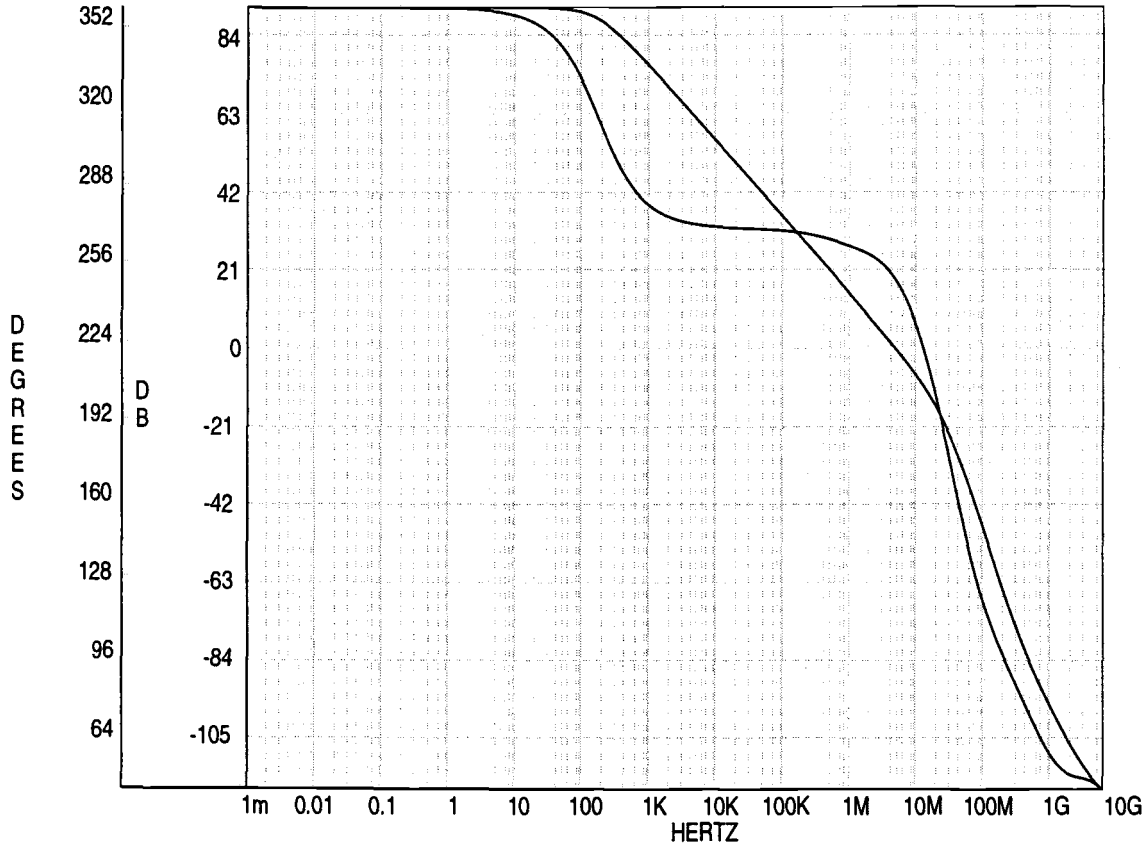
$$P_{eff} = \frac{I_{load}}{I_{quiescent}}. \qquad \text{(EQ 3.9)}$$

The gain, phase, and PSRR of Babanezhad's amplifier is displayed in Figure 3.6

TABLE 3.2. Performance data of the Babanezhad's amplifier.

DC Gain	91.7 dB	Overshoot of a 200 mV step	6.4%
unity-gain Bandwidth	7.13 MHz	Overshoot of a 2 V step	2.8%
Phase Margin	68.64 deg	small-signal Settling to 100 dB	1.2 μs
Gain Margin	21.75 dB	Large Signal Settling to 100 dB	1.6 μs
PSRR @ DC	97.3 dB	Power Dissipation	21.8 mW
1 KHz	93.0 dB	Power Efficiency Factor	5.8
10 KHz	75.0 dB	THD @ 1KHz	73.3 dB
1 MHz	36.7 dB	Systematic Offset	265 nV
Total Integrated Noise	3.83 μV	Load	26 Ω || 200 pF
Compensation capacitor	10 pF		

Figure 3.6. **(A and B) Gain/Phase of Babanezhad's amplifier.**



In recent publications new power amplifier architectures have been explored[49]. A new interesting compensation concept that allows more than two stages, Nested Miller Compensation (NMC), has been presented and reviewed. These concepts have been applied to the design of an amplifier which meets the specifications of this design. Figure 3.7 shows a schematic diagram of Castello's amplifier.

Figure 3.6. **(C) PSRR of Babanezhad's amplifier.**

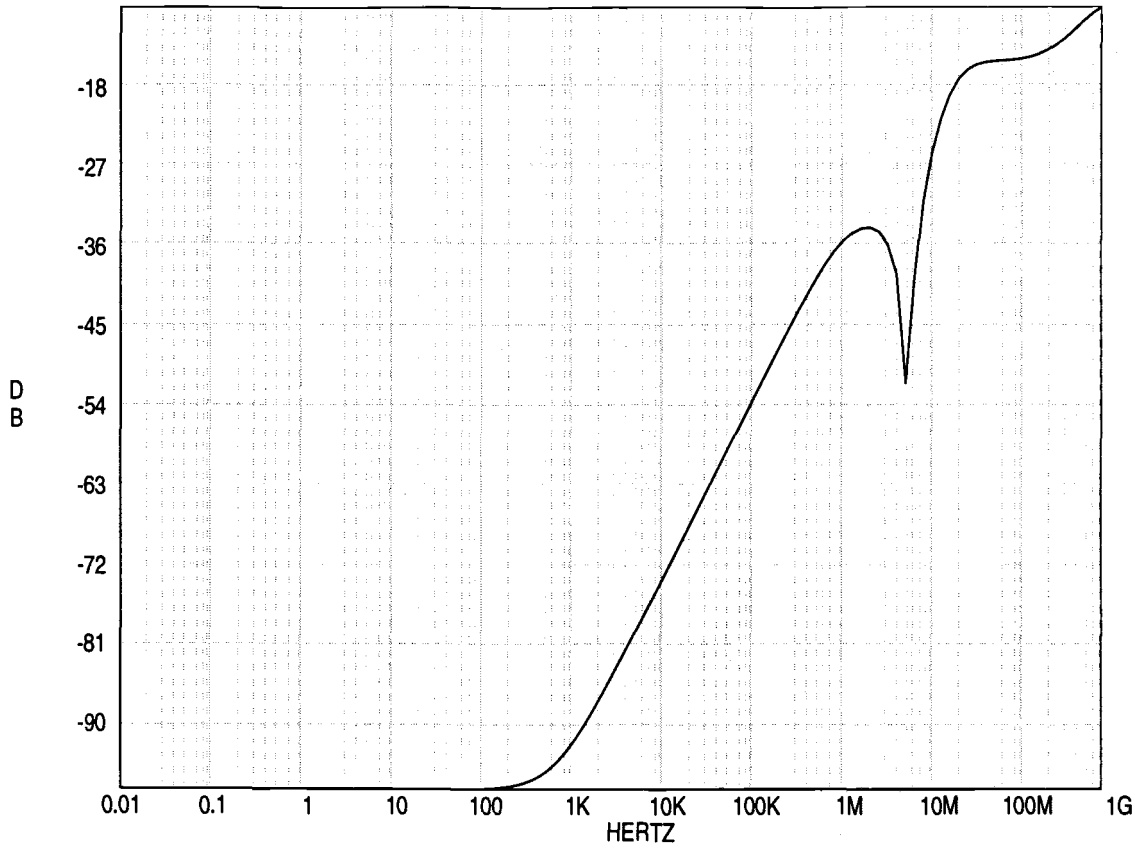
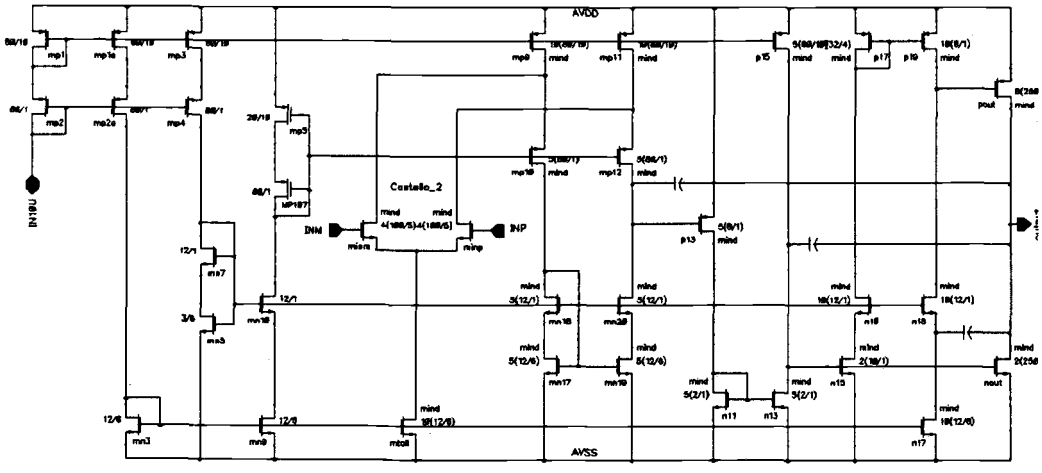


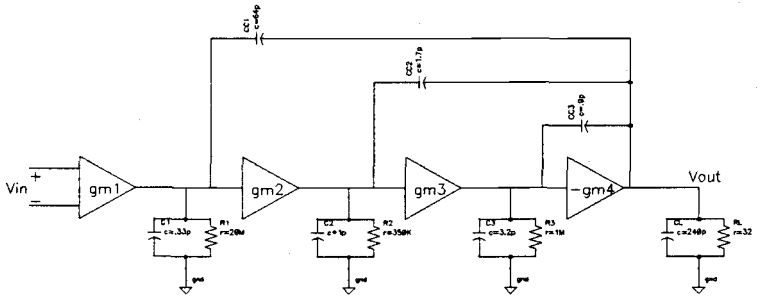
Figure 3.7. **Castello's amplifier schematic**



As in the previous design the FCC amplifier is the first stage and in accordance with the previous discussion, the noise of subsequent stages is negligible. A four-stage Nested Miller Compensated amplifier is chosen as the next amplifier. Its design and discussion follow.

Figure 3.8 shows a block diagram of a 4 stage amplifier. The first stage is a differential g_m (which can be either negative or positive for this analysis) followed by a parasitic resistance and capacitance. Each of the second and third stages have positive transconductances and also drive parasitics on their output nodes. The fourth and final stage has a negative transconductance value. Detailed analysis of the transfer function has been performed [55], and with the following assumptions the pole locations (EQ 10) are derived. It is important to note that for derivation purposes the poles are assumed to be well spaced in the final design. If this were not the case, stability would not be achieved.

Figure 3.8. **4-Stage block diagram**



Assuming that R_1 << all other R's and all $1/g_m$ values, C_1 >> all other C's, and C_{C1} >> C_1.

$$P_1 = \frac{g_{m1}}{C_{C1} \bullet A_{Vdc}} \qquad P_2 = \frac{g_{m2}}{C_{C2}} \qquad P_3 = \frac{g_{m3}}{C_{C3}} \left[\frac{g_{m4}\left(\frac{C_{C2}}{C_2 + C_{C2}}\right)}{g_{m4} + g_L\left(\frac{C_1 + C_{C1}}{C_{C1}} \cdot \frac{C_3 + C_{C3}}{C_{C3}}\right)} \right] \qquad P_4 = \frac{g_L}{C_L}$$

$$A_{Vdc} = \frac{g_{m1}}{g_1} \cdot \frac{g_{m2}}{g_2} \cdot \frac{g_{m3}}{g_3} \cdot \frac{g_{m4}}{g_4} \qquad \text{(EQ 3.10)}$$

and the zeros are defined as

$$Z_1 = -\frac{g_{m4}}{C_{C3}} \quad Z_2 = \frac{g_{m3}}{C_{C3}}\left(\frac{C_{C3}}{C_3 + C_{C3}}\right) \quad Z_3 = \frac{g_{m2}}{C_{C1}}\left(\frac{C_{C2}}{C_2 + C_{C2}}\right) \qquad \text{(EQ 3.11)}$$

Notice that when this topology has small resistive loads, the fourth pole moves to an even higher frequency than classical theory predicts and the third pole moves to a lower frequency. These equations show that with large loads classical design is not adequate. However for smaller loads (large R_L), the equations follow classical Miller compensated design.

Normally moving the fourth and dominant pole to a higher frequency would help the frequency response as long as no other poles were affected by the loading of the output stage. In this design the low load impedance splits the third and fourth pole in the frequency domain. The third pole is now the dominant pole of the system and this design departs from classical theory where the output pole is the next dominant-pole in the system.

Note that the gain-bandwidth and the dominant pole are independently designable parameters. Given this fact, high bandwidth with very good stability can be obtained by increasing the total power usage of the amplifier.

As with the dominant pole, the zeros of this circuit do not follow commonly accepted design practices. The zeros which are normally expected to be at or near infinity are close to the unity-gain frequency. The left half plane zeros increase the phase margin of this design, but degrade the gain margin to nearly unacceptable levels (see Figure 3.9). In Figure 3.9a it is observed that the magnitude peaks due to pole-zero pairs and that this peak is above unity-gain. The amp is now unstable and must be modified to be stable.

Originally the circuit was designed with a C_{C1} of 32 pF to position the unity-gain frequency at approximately 4 MHz. Figures 3.9a and 3.9b depict the gain/phase response of the original design. In Figure 3.9a the gain response flattens and even peaks due to the close proximity of several poles and zeros. Upon inspection of equations 3.10 and 3.11, it was observed that increasing the output stage transconductance and lowering the bandwidth of the overall amplifier should space the poles and zeros enough to reduce the peak-

ing and increase the gain margin to acceptable levels. The original bandwidth was designed to be 4 MHz but with the pole-zero crowding phenomena, the final bandwidth was halved.

In classical two-stage amplifier design, halving the bandwidth would lower the distortion numbers by approximately 6 dB. With a large output load the secondary internal feedback loop has very low loop gain and thus does not contribute the THD performance. Since the local feedback loop does not contribute to the performance there will be a decrease in THD with bandwidth due to the roll off of the gain. In the four stage design, there are three loops which all have relatively high feedback factors. The presence of these extra internal loops acts to increase the THD performance of this amplifier by providing feedback to increase the excess gain available at the frequency of interest. Table 3 shows the performance data of Castello's amplifier.

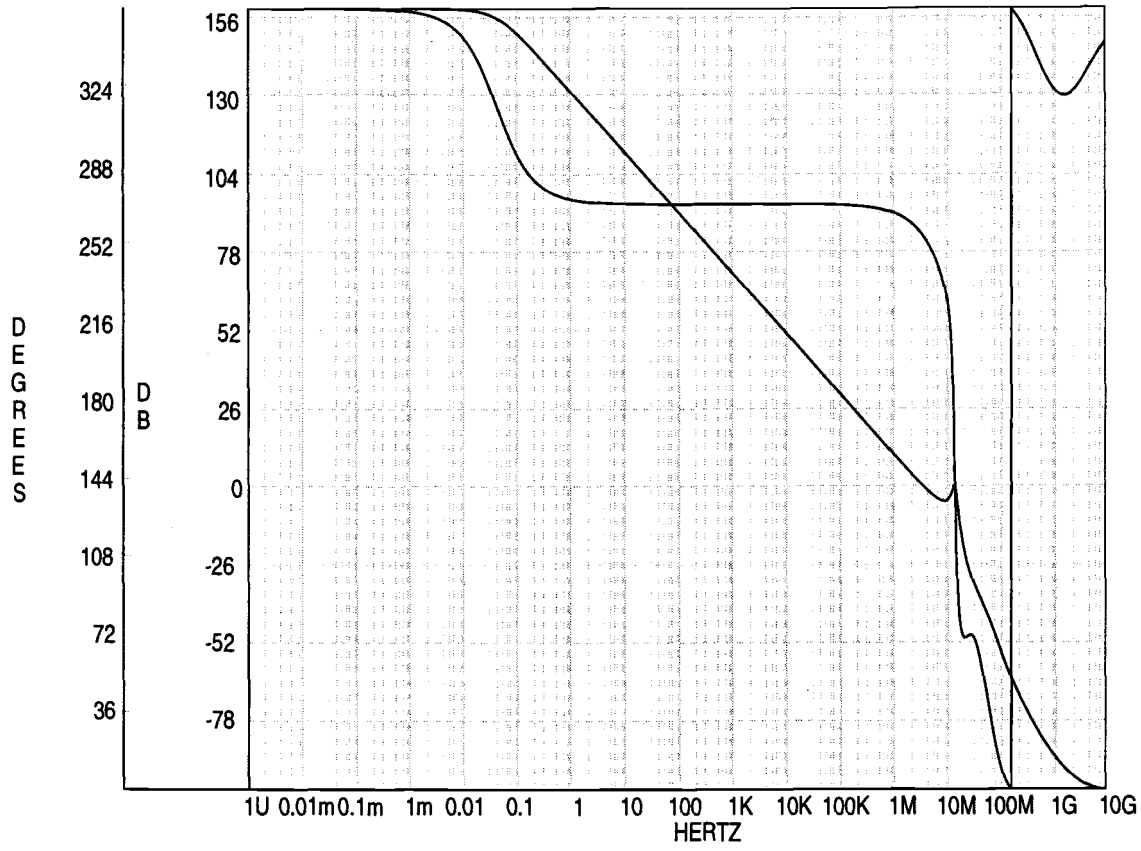
The final frequency response of Castello's amplifier is depicted in Figures 3.9c and 3.9d. The output transconductance was doubled and the bandwidth halved compared to that of the initial design in order to produce this response

In Castello's amplifier, the first stage is the FCC amplifier discussed earlier. The second and third stages are non-inverting and are "compliments" of each other. They consist of a common-source amplifier and a simple current mirror. This produces a net positive gain for the second and third stages. The fourth stage is a current source and a common-source amplifier which is a class-AB stage. The output stage is chosen be class-AB for high power efficiency. Performance data of Castello's amplifier.

TABLE 3.3. Performance data of Castello's amplifier.

DC Gain	164.3 dB	Overshoot of a 200 mV step	0.0%
unity-gain Bandwidth	2.03 MHz	Overshoot of a 2 V step	0.0%
Phase Margin	82.4 deg.	small-signal Settling to 100 dB	1.6 μs
Gain Margin	11.05 dB	Large Signal Settling to 100 dB	2.9 μs
PSRR @ DC	85.2 dB	Power Dissipation	15.5 mW
1 KHz	65.9 dB	Power Efficiency Factor	8.2
10 KHz	45.9 dB	THD @ 1KHz	108.7 dB
1 MHz	6.7 dB	Systematic Offset	99.6 μV
Total Integrated Noise	3.83 μV	Load	26 Ω || 200 pF
Compensation Capacitors	C1=64pF C2=1.7pF C3=0.9pF		

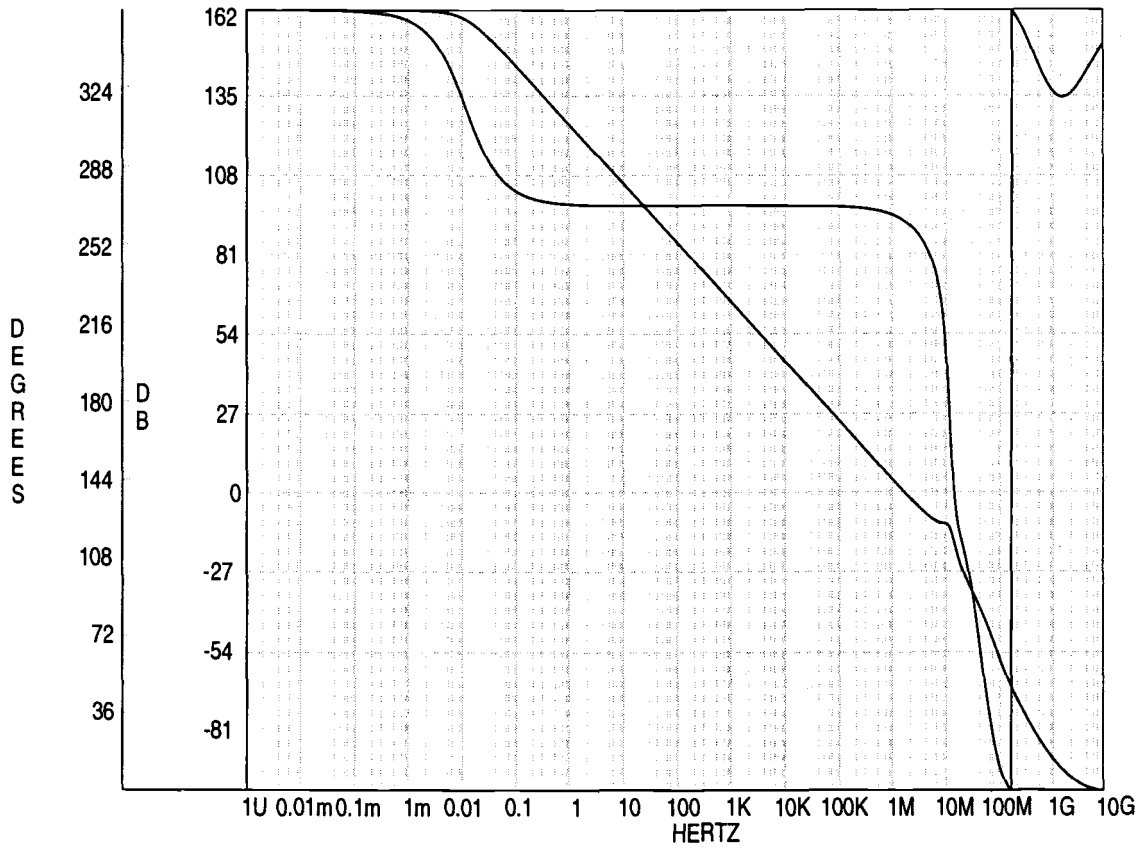
Figure 3.9. **Gain/Phase responses of Castello's amplifier in the original design.**



class-A action is controlled by the current source which in turn is controlled by the stage 3 gain. Class B action is dominated by the common-source amplifier driven directly from the second stage output.

There are only 3 stages through the n-channel output transistor while there are four through the p-channel current source. Simulations have confirmed that any feed-forward zeros created by this dual path are at or near infinity and thus have no effect on the practical design. The extra gain stage through the p-channel device can act to narrow the size differential caused by the difference in mobilities between n and p devices. This is beneficial to compact and symmetrical layouts.

Figure 3.9. **Gain/Phase responses of Castello's amplifier in the final design.**



Castello's amplifier has nearly a single-pole response except for the diminished gain margin. Notice that there is no overshoot and that the settling time is increased. The excellent gain and phase margin values contribute to the excellent THD and the power dissipation is lower than that of Babanezhad's amplifier. The simplicity (lack of cascoding) of the third and fourth stages allows a trade off between the power supply rejection ration and output swing. With decreased swing in intermediate stages, the Power Efficiency factor will also decrease. Cascoding as well as other techniques can be applied to increase the PSRR performance, if needed, and if the voltage supplies are of high enough value.

The third and final amplifier (Huijsing) is found in [50] and is pictured in Figure 3.10. This topology is a hybrid of the FCC architecture and a symmetrical class-AB output

stage. The symmetry is accomplished by creating a floating voltage source with transistors MP17 and MN25 and replacing the output node of the FCC amplifier with this source. A simple analysis shows that the node voltages cp and cn follows the relation,

$$V_{cp} = V_{cn}\frac{g_{mn25}}{g_{mp17}}. \qquad \text{(EQ 3.12)}$$

This now creates two identical signals separated enough to eliminate any crossover distortion that might be seen when the output stage changes from class-A to class-B operation. In this case the output transistors are both common-source amplifiers with matching transconductances. This matching provides the symmetry needed for high performance low THD designs.

Extra current legs are added to provide the DC bias voltages for the two transistors that create the floating voltage source. V_{cn} is defined by

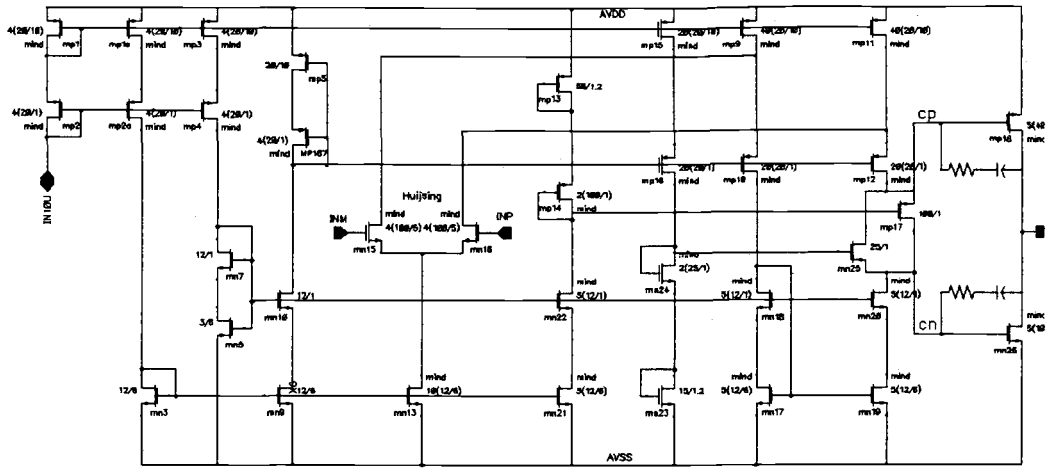
$$V_{cn} = V_{gsn23} + V_{gsn24} - V_{gsn25}. \qquad \text{(EQ 3.13)}$$

and V_{cp} is defined by

$$V_{cp} = AVDD - V_{sgp13} - V_{sgp14} + V_{sgp17}. \qquad \text{(EQ 3.14)}$$

Therefore, if the current densities in transistors MN24 and MN25 match, then the gate voltage of MN26 (or V_{cn}) is set by MN23. Careful effort must be provided to match MN23 and MN26. The output current is set by the ratio of the sizes between MN23 and MN26. The bias of the p-channel device MP18 is set similarly to that of MN26.

Figure 3.10. **Huijsing's schematic**



A disadvantage of this stage is the need for dual compensation paths. Each path compensates half of the output stage. It can be argued that only a single path is needed which connects around the longest signal path. In this case that would be around the n-channel drive transistor MN26.

For output voltages at or below mid-rail this performs fine; however, when the output voltage begins to approach the upper rail, the n-channel transistor begins to turn off and the compensation is lost. This will cause the output to perform very well below mid-rail and possibly oscillate near VDD.

Another problem with this architecture is that it is sensitive to the magnitude of the threshold voltages. Viewing the n-channel transistors MN19 and MN20, it is observed that the drain of the cascode device MN20 is at V_{cn}. This limits the drain to source voltages of both MN19 and MN20. If the threshold voltage is too low (~ 500 mV), these devices have problems remaining in saturation over process, voltage, and temperature variations. This severely limits the low voltage performance of this architecture to 2.7 V and above. However for supply voltages above 2.7 V this amplifier has an extremely symmetrical drive response which yields very low third-order harmonic distortion components. Therefore, if

the supply rails are large, this amplifier is an excellent topology for very low distortion performance.

Since the output quiescent current can be set independently of the signal path, the Huijsing amplifier has an excellent power efficiency factor (as shown in TABLE 3). Using very small currents in extra basing legs allows the designer to trade area for power. The smaller the bias leg currents, the lower the quiescent power and the larger the output devices for the same drive capability. This is a first-order approximation that is broken by the presence of large parasitic capacitances on the gates of the output transistors when this relation is taken to the extreme. At very large sizes the area grows exponentially to overcome the parasitic poles created by these parasitics. The best power efficiency factor reported by [53] is greater than 25 with a relaxed THD specification.

As with both Babanezhad's and Castello's amplifiers, Huijsing's amplifier uses the FCC as its first stage. Therefore, the noise is dominated by the FCC and little consideration is given to the noise of the added devices.

It is worth noting that the addition of the floating bias is not without its detrimental effects. This addition along with the dual compensation path creates a very intricate series of poles and zeros that can cause problems with designs that attempt to surpass a bandwidth of 10 MHz.

Figure 3.11 shows the PSRR response of Huijsing versus frequency while Figure 3.12 shows Huijsing's amplifier's frequency response. TABLE 4 summarizes the performance of this amplifier.

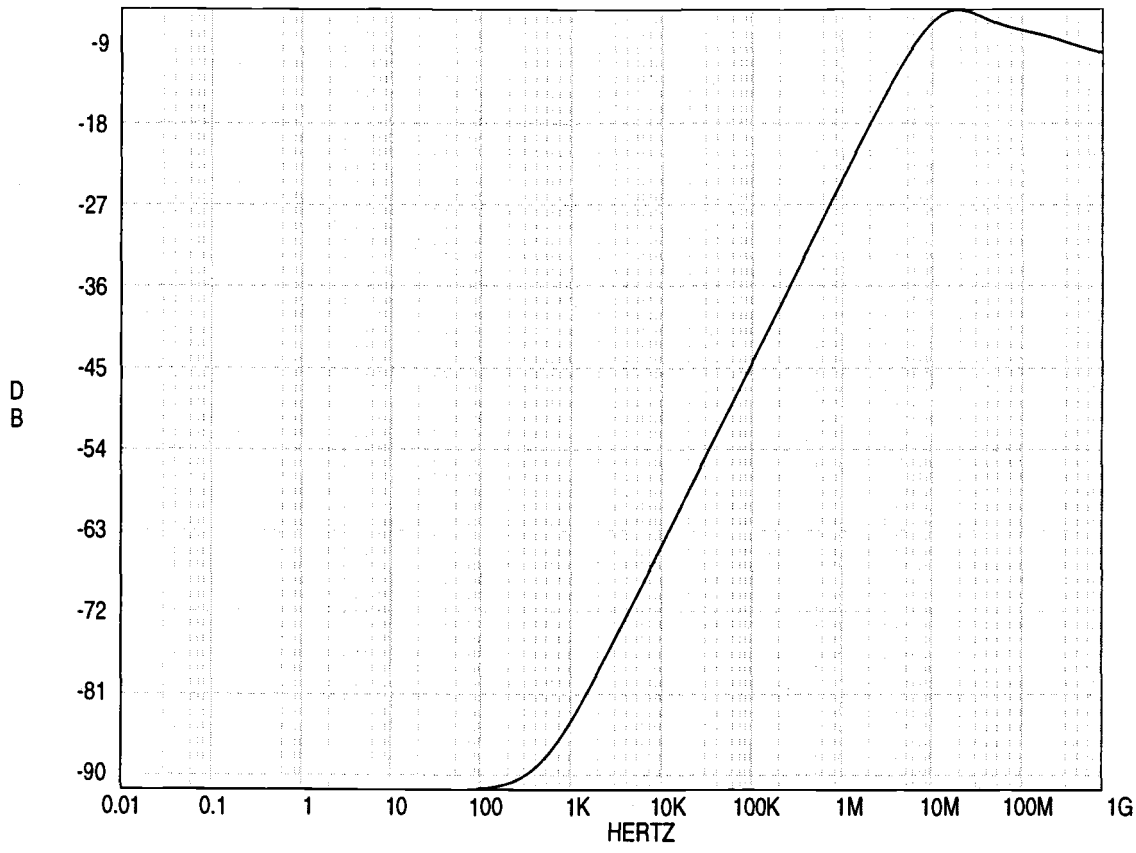
Even with low DC gain, the Huijsing amplifier shows very good THD performance because symmetrical drive capability maximizes the THD performance for a given gain. The Huijsing amplifier exhibits excellent phase margin. Normally a high phase margin would infer a single-pole response but here the high phase margin is a little misleading. First, the floating voltage source introduces several poles and zeros that tend to degrade the settling response. Secondly the high swing mirrors in the FCC amplifier introduce a

pole that degrades the phase response. This amplifier has very fast response to an input step with very little overshoot compared to the two previous designs due to these added poles and zeros. It should be noted that the compensation capacitors are larger than the typical design equation

$$\frac{g_{min}}{C_{comp}} < \frac{g_{mout}}{4C_L} \qquad \text{(EQ 3.15)}$$

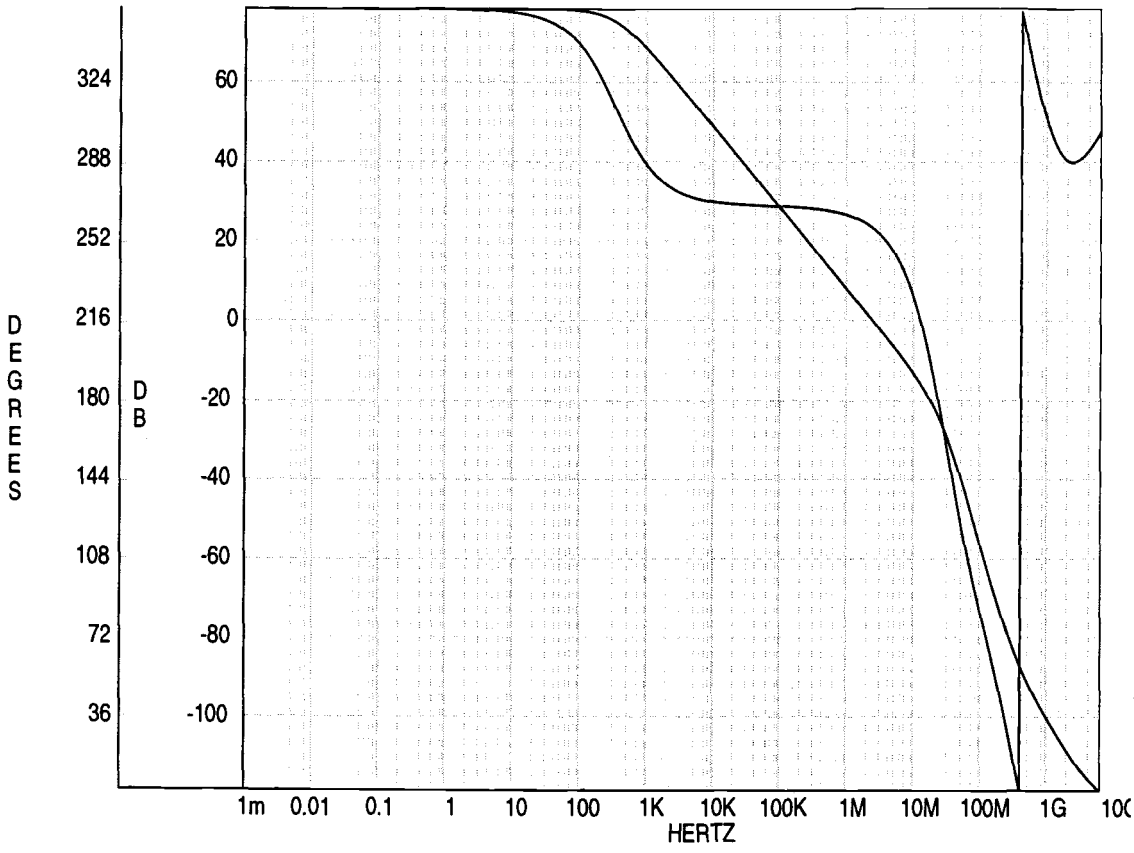
(where the first term is the bandwidth) predicts for good phase margin due to these additional poles and zeros. Analysis shows that the limiting factor in the other two topologies that is not present here is the presence of a mirror in the output stage. The current mirror has limited response to that of a common-source amplifier and hence has a slower step response.

Figure 3.11. **PSRR of Huijsing.**



Compared with the other topologies, the Huijsing amplifier has very low quiescent power dissipation. This is evident by the P_{eff} factor which is greater than two times that of the next greatest value. The power is minimized because drive capability and the quiescent output stage current are independent of each other as discussed earlier.

Figure 3.12. **Magnitude and Phase response of the Huijsing amplifier.**



Three amplifiers have been designed for experimentation: a tradition two-stage amplifier, with moderate power efficiency and good PSRR (Babanezhad's amplifier), a four stage amplifier with Nested Miller Compensation and excellent THD (Castello's amplifier), and a hybrid two-stage amplifier with high power efficiency and excellent step response performance (Huijsing). These topologies were chosen to represent as wide a range as possible in the design space. Each of these amplifiers have distinct and diverse applications. Castello's amplifier is the obvious choice for very high performance THD applications, Huijsing has a very clean step response with no overshoot, and Babanezhad's amplifier has very high PSRR.

TABLE 3.4. Performance data of the Huijsing amplifier.

DC Gain	78.4 dB	Overshoot of a 200 mV step	0.22%
unity-gain Bandwidth	3.5 MHz	Overshoot of a 2 V step	0.0%
Phase Margin	79.8 deg.	small-signal Settling to 100 dB	812 ns
Gain Margin	24.1 dB	Large Signal Settling to 100 dB	2.9 μs
PSRR @ DC	91.7 dB	Power Dissipation	6.58 mW
1 KHz	84.8 dB	Power Efficiency Factor	19.2
10 KHz	65.8 dB	THD @ 1KHz	77.6 dB
1 MHz	25.9 dB	Systematic Offset	47.5 μV
Total Integrated Noise	3.83 μV	Load	26 Ω || 200 pF
Compensation capacitor	6 pF each.		

In the next chapter the performance of each of these circuits with non-ideal passive elements will be evaluated and presented. Each topology will show distinct variations in the performance with each of the passive elements available in Digital CMOS process. These variations shall be explored and the specifications for the best applications will be defined.

CHAPTER 4: Experimental Results

A design experiment is constructed with the three amplifiers depicted in Chapter 3. Each of the amplifiers are placed in the inverting fixed gain configuration discussed in Chapter 2. The load in all cases is a parallel combination of 25 Ω and 200 pF. Simulations of the small-signal magnitude and phase responses, the response to a rising edge 2 V input step, the total harmonic distortion, and the noise have been simulated and their results are listed below. It is important to note that the noise of the system is fundamentally determined by the noise of the first stage of the amplifier[1]. Since all amplifiers in this experiment have the same first stage, the noise simulations offer little insight into the performance impacts that each of the components has on the individual architectures.

For each amplifier, all combinations of the passive compensation elements have been simulated. This means that for Babanezhad's, and Huijsing's amplifiers, 9 separate circuits that are evaluated and presented. Castello's architecture used only Miller multiplied capacitive compensation and therefore only has three versions. Each of the 21 amplifiers are discussed and their relative merits are examined. The examination is broken into 3 distinct categories: small-signal performance, THD, and settling response. Each amplifier in all of its versions has been simulated and some statistical data of those simulations is presented.

Beginning with small-signal performance, figure 4.1 shows the gain/phase diagram of each of the amplifiers in the nominal case.[2] The performances shown are used as metrics for the rest of the analysis. Since compensation has no effect on the DC solution of these circuits, the DC gain remains unchanged for each of the three amplifiers over the entire set of experiments. The phase margin is directly determined by several unchanging circuit parameters and the relative values of the compensation and load capacitances.

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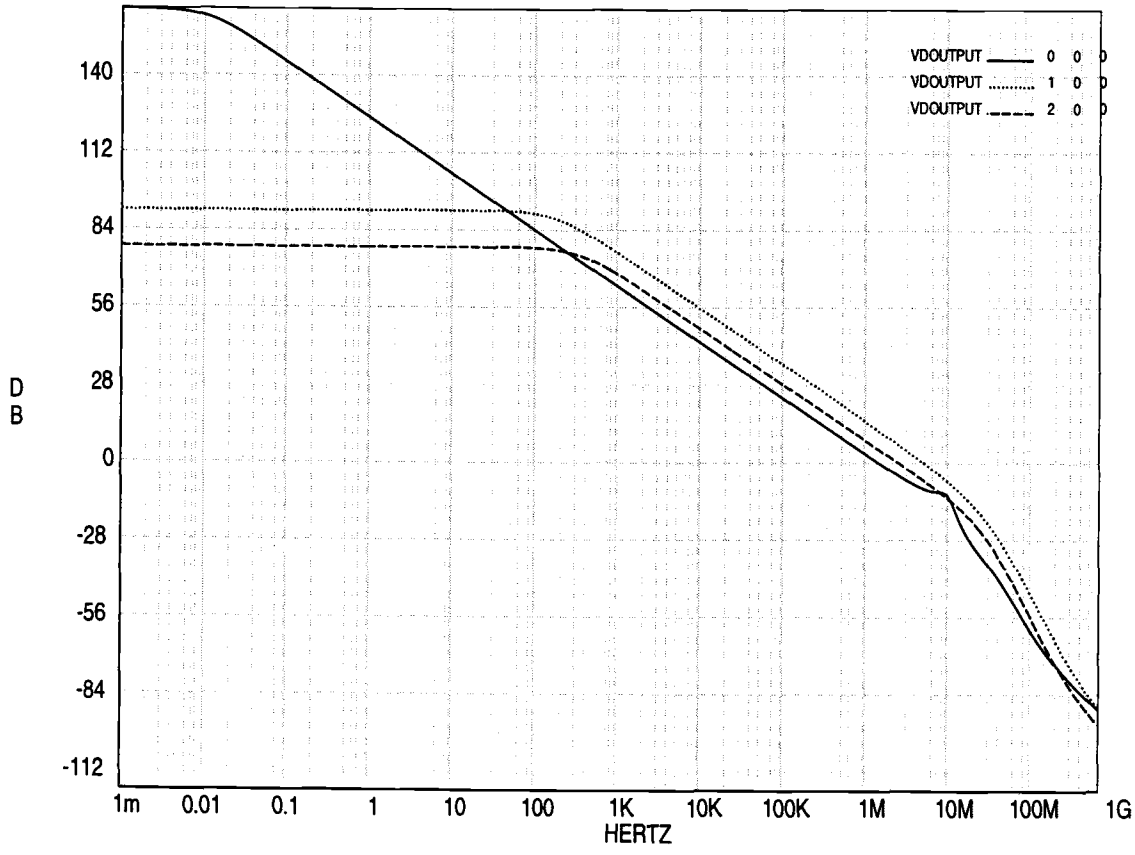
1. See Chapter 3.
2. For a complete list of performance parameters, see Chapter 3.

Likewise the gain margin is determined by the parasitic poles with respect to the "placed" compensation and load poles. The bandwidth is in direct relation to the value of the compensation capacitor.

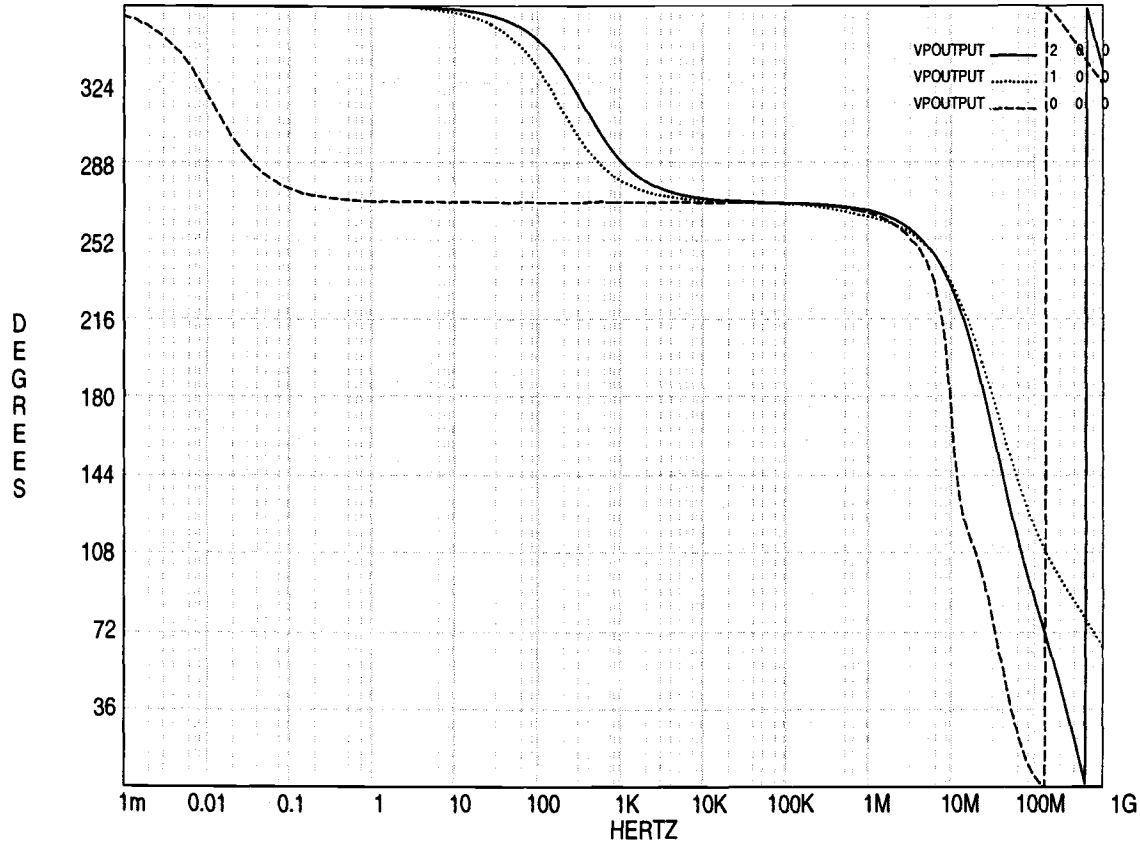
Figure 4.1. **(A) Magnitude responses of each amplifier in the nominal case.**



In Table 4.1, the statistical data for all configurations of each amplifier are listed. Relevant test cases have been grouped together. It is worth noting that Castello's amplifier has serious problems with stability when using the MOSFET capacitors. From table 4.1, the phase margin of the amplifier is large and negative. Upon inspection of the magnitude and phase responses of this amplifier, it is noted that new pole-zero pairs are introduced

by the application of the MOSFET capacitors. In this case, these pole-zero pairs create a peaking in the magnitude response just before the unity-gain frequency.

Figure 4.1. **(B) Phase responses of each amplifier in the nominal case.**



The phase rolls off sharply and the amplifier becomes unstable. It is believed that the extra back gate parasitics that are not present in the N-channel over N-WELL capacitor is the cause of this problem.

The phase and gain margin of the Huijsing amplifier is fairly robust to changes in compensation components. This is due to the dual compensation capacitance paths. When the output voltage swings, the multi-path capacitances exhibit more linear overall total

compensation capacitance than the other two amplifiers which have only single path compensation. Since the Babanezhad's amplifier is a more traditional two-stage design with single path compensation, it shows the greatest sensitivity to varying types of compensation capacitors.

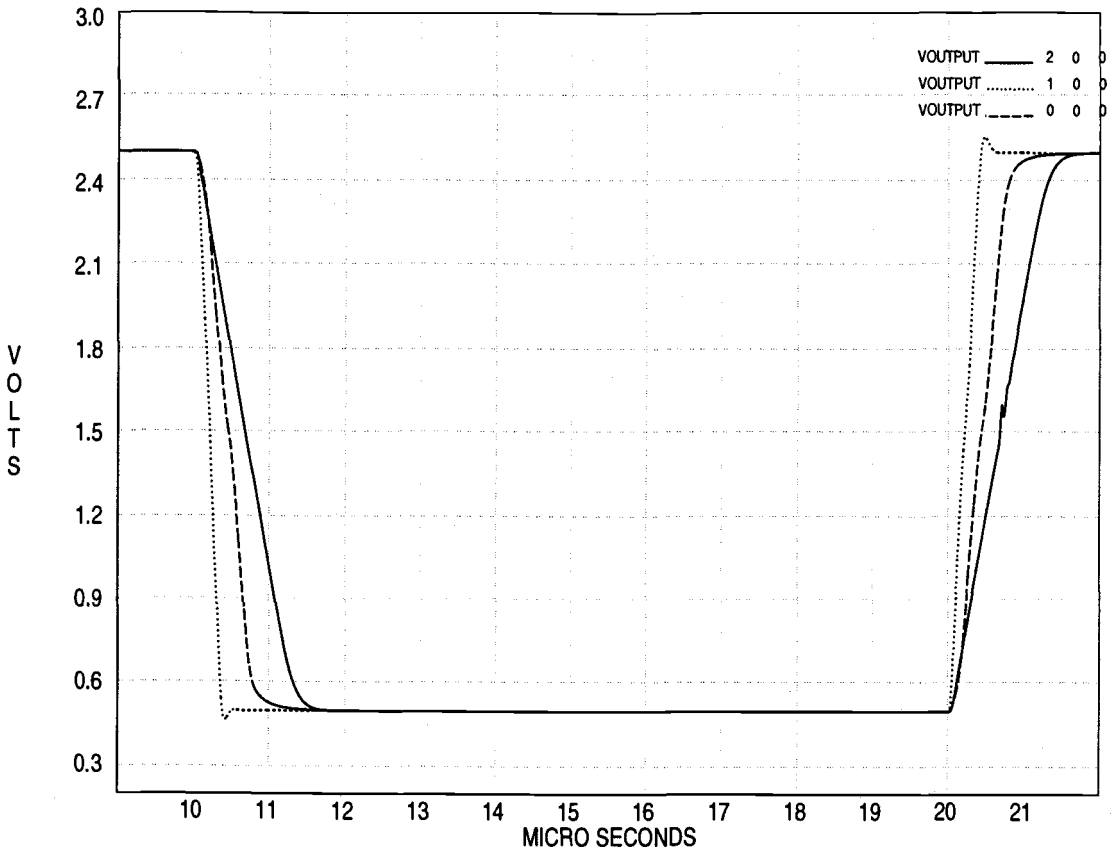
The compensation resistors position the zero created by the compensation network and therefore only have a second-order effect upon the magnitude/gain response of the amplifier. Of the two architectures that use this technique, the positioning of the zeros is most important in the Huijsing architecture. There are two zeros that are placed in this architecture and as the compensation resistor varies, the effect on the system is two times as significant.

The bandwidth of each of the amplifiers does not fall below the minimum required value because the designs are implemented by using the minimum possible value of the capacitors across the linearity curves. Castello's amplifier bandwidth has the greatest dependence upon the compensation capacitance. Both Huijsing's and Babanezhad's amplifier topologies have a fairly broad variance with bandwidth, but since their phase margins remain within acceptable limits, this variance is of little consequence.

TABLE 4.1. B-> small-signal performance. B, C, and H denote Babanezhad's, Castello's, and Huijsing's amplifiers respectively.

Amplifier	Phase Margin (deg.)		Gain Margin (db)		Bandwidth (Mhz)	
	Mean	Std. Dev.	Mean	Std. Dev.	Mean	Std. Dev.
Each Amplifier with sandwich capacitors and polysilicon resistors						
B 1	70.3	.0546	23.6	.0122	5.8	.0359
C 1	82.4	.0036	10.9	.1181	2.0	.0056
H 1	80.2	.1878	24.7	.1797	3.4	.0387
Each Amplifier with N-channel over N-WELL capacitors and polysilicon resistors						
B 2	56.7	.7700	17.8	.0650	10.0	.1840
C 2	84.2	.0008	8.7	.1180	2.1	.0068
H 2	78.9	.2810	21.4	.2400	4.3	.0744
Each Amplifier with MOSFET capacitors and polysilicon resistors						
B 3	41.3	.2120	13.4	.0020	13.7	.1362
C 3	-48.2	16.52	8.7	.9960	13.8	.1306
H 3	69.2	.8770	17.5	.1684	7.2	.1575
Babanezhad and Huijsing with sandwich capacitors and N-WELL resistors						
B 4	71.1	.0690	25.1	.0490	5.8	.0375
H 4	80.4	.1896	25.1	.2020	3.4	.0387
Babanezhad and Huijsing with N-channel over N-WELL capacitors and N-WELL resistors						
B 5	57.2	.8310	18.3	.1010	10.0	.1841
H 5	79.0	.2820	21.6	.2610	4.3	.0744
Babanezhad and Huijsing with MOSFET capacitors and N-WELL resistors						
B 6	41.7	.2220	13.7	.0027	13.8	.1362
H 6	69.3	.8750	17.6	.1725	7.2	.1575
Babanezhad and Huijsing with sandwich capacitors and MOSFET resistors						
B 7	70.8	.1020	24.5	.0992	5.8	.0351
H 7	78.9	.0990	25.2	.1307	4.7	.0510
Babanezhad and Huijsing with N-channel over N-WELL capacitors and MOSFET resistors						
B 8	57.2	.8750	18.7	.1156	9.9	.1762
H 8	72.3	.1800	19.9	.2818	6.7	.1151
Babanezhad and Huijsing with MOSFET capacitors and MOSFET resistors						
B 9	42.1	.2520	13.8	.0037	13.4	.1318
H 9	63.9	.4680	16.5	.1492	8.7	.1610

Figure 4.2. **Step Response of each amplifier topology in the nominal case.**



For a topology that is totally MOSFET with no passive components, the best solution is the Huijsing amplifier. Table 4.1 shows that in the case where only active elements are used, Castello's amplifier fails to function with stability. Babanezhad's amplifier will still function, but it will do so at a greatly reduced stability. The Huijsing topology shows remarkable immunity to the passive elements chosen.

The step response of each of the amplifiers to an input step of 2V is shown for the nominal case in Figure 4.2. In this figure, it is observed that Babanezhad's amplifier has the best slew rate and settling time, but it also has the highest overshoot. Both Castello's and Huijsing's amplifiers follow a nearly single-pole step response with Huijsing being the faster of the two. However, Castello's amplifier has a slight non-linearity about mid-

rail. Investigation into this phenomena reveals a topological error in the amplifier itself. A discussion of this is beyond the scope of this text.

The settling response of Babanezhad's amplifier varies little with each of the compensation capacitor components. It has the fastest response with the MOSFET capacitor because the capacitance value decreases as the voltage swings. This allows the loop to become less stable and increase the speed of transition. Likewise, the Huijsing amplifier is faster with MOSFET capacitors. However, the Huijsing amplifier varies greatly with process, voltage, and temperature which makes it very unpredictable. The settling time of Castello's amplifier is unstable for the MOSFET capacitor case as discussed earlier, but varies little with the other two choices of capacitors.

Castello's amplifier has zero overshoot for stable systems. This is due to the nature of the compensation scheme. The significant poles are all placed using compensation capacitors and since all capacitors vary in a like manner with process, voltage, and temperature, the poles move together. The Huijsing amplifier has a very small overshoot with a tightly packed distribution across all the individual component sets. This is due to the symmetrical nature of the output stage. All the poles and zeros track each other in this system. Babanezhad's amplifier has the greatest overshoot, but still falls well within specifications.

For cases where the amplifier is stable, Castello's amplifier is clearly the best choice for Total Harmonic Distortion performance. The distribution is tightly packed and the numbers are well above specifications. Babanezhad's amplifier topology shows superior performance on average, but it has a very broad distribution. The Huijsing amplifier has a tighter distribution but questionable performance.

TABLE 3.2. Step and THD performance. B, C, and H denote Babanezhad's, Castello's, and Huijsing's amplifiers respectively.

Amplifier	Settling (ns)		Overshoot (%)		THD (dB)	
	Mean	Std. Dev.	Mean	Std. Dev.	Mean	Std. Dev.
Each Amplifier with sandwich capacitors and polysilicon resistors						
B 1	682.8	53.59	.173	.00096	67.5	34.82
C 1	2381.3	489.40	0	0	103.42	.5458
H 1	1642.5	209.90	.006	.0000006	57.655	32.89
Each Amplifier with N-channel over N-WELL capacitors and polysilicon resistors						
B 2	655.5	320.75	.201	.00130	64.4	28.71
C 2	2306.3	1211.28	0	0	82.12	.5880
H 2	1522.2	249.20	.005	.0000007	56.8	31.15
Each Amplifier with MOSFET capacitors and polysilicon resistors						
B 3	603.128	0.35	1.949	.05852	66.92	33.71
C 3	Unstable		.191	.00093	81.14	.0024
H 3	927.8	719.54	.116	.00030	58.99	35.70
Babanezhad and Huijsing with sandwich capacitors and N-WELL resistors						
B 4	681.28	80.54	.159	.00082	67.45	34.82
H 4	1642.75	2485.36	0	0	57.66	32.89
Babanezhad and Huijsing with N-channel over N-WELL capacitors and N-WELL resistors						
B 5	655.83	224.15	.185	.00111	64.38	28.71
H 5	1522.58	248.56	.005	.0000007	56.80	31.15
Babanezhad and Huijsing with MOSFET capacitors and N-WELL resistors						
B 6	600.63	.67	1.938	.05929	66.92	33.71
H 6	927.86	719.4	.115	.00029	58.99	35.70
Babanezhad and Huijsing with sandwich capacitors and MOSFET resistors						
B 7	679.43	125.18	.158	.00080	67.43	34.78
H 7	3064.71	1193.83	0	0	50.90	20.16
Babanezhad and Huijsing with N-channel over N-WELL capacitors and MOSFET resistors						
B 8	653.82	22.60	.183	.00109	64.73	28.71
H 8	2976.47	3171.64	0	0	50.67	19.79
Babanezhad and Huijsing with MOSFET capacitors and MOSFET resistors						
B 9	599.93	1.69	1.948	.06189	66.91	33.70
H 9	2086.75	446.99	.107	.00030	55.50	28.25

CHAPTER 5: Conclusions

In conclusion, a set of power amplifiers for embedded audio band applications have been designed and tested. These amplifiers are compatible with digital CMOS process and have the ability to drive loads of 25 Ω and 200pf with low distortion and moderate power efficiency from a single 3 V power supply. The ability to use purely active components for all aspects of the circuit has been demonstrated. A design system has been outlined that shows the ability to design various architectures in digital processes which yields marked improvements over [1].

To determine the best topology and passive components for each application, the results from chapter 4 are reviewed. The Huijsing amplifier is robust and its small-signal performance varies little with the choice of components. In fact, the stability of the amplifier actually increased with the introduction of the non-linear N-channel over N-WELL capacitor. This remarkable insensitivity makes this topology a good choice as a digital CMOS output driver. However, the topology is limited to approximately a 2.7 - 3.0 V single supply. The future of digital is moving towards sub 2 V supplies, and therefore this architecture will become outdated. In this architecture, the introduction of the non-linear resistors has only a second-order effect on performance. The only performance parameter that is notably affected by the resistor choice is the bandwidth and since its value increases only, this is not a problem as long as good phase margin is maintained.

Castello's amplifier uses only capacitive compensation and therefore it has a smaller set of data. The topology was not stable with the MOSFET capacitors, but has exceptional performance with the other types of capacitors tested. With the availability of a well modeled N-channel over N-WELL capacitor, this amplifier is the clear choice of the three.

Classical two-stage designs have first-order dependencies upon the compensation elements linearities. Babanezhad's amplifier is a classical two-stage design and shows the greatest variation over the passive element choices. It is concluded that this amplifier is the least desirable of the three chosen for the given application. However, the topology has the ability to operate in lower supply environments than that of the Huijsing topology.

In a situation where only active components are available and a low supply is present, the Babanezhad's amplifier topology may be the prudent choice.

In audio applications the response to an input step is an important performance specification. In the case where speed is the important parameter and some overshoot can be tolerated Babanezhad's amplifier topology is the best choice. Its maximum mean overshoot is 1.95% and it has nearly a two times faster settling time than its counterparts. Castello's amplifier is the slowest of the three and also demonstrates some non-linearity about the mid-rail voltage. This topology is the least desirable in applications where fast linear step responses are required. Huijsing's amplifier shows a linear single-pole step response. It is faster than Castello's amplifier, but is much slower than Babanezhad's amplifier. In applications where no overshoot can be tolerated[1] and there is a limited bandwidth of signals[2], Huijsing's amplifier is the optimal choice.

One of the defining specifications for high precession audio circuits is the Total Harmonic Distortion. Castello's amplifier shows tremendous performance in this area. However, it is unstable for MOSFET compensation capacitors. If N-channel over N-WELL capacitors are available, this topology is the clear choice in ultra high performance audio output applications. Babanezhad's amplifier has the greatest variance over process, voltage, and temperature, but it has the better average performance by a great margin over the Huijsing amplifier. The Huijsing amplifier has the poorest mean THD performance. Compared to Castello's amplifier, the other topologies have high sensitivities which makes them suspect in high performance applications.

Metal sandwich capacitors have enormous die area impacts, but they have very good voltage linearity. These capacitors also have small variances in absolute value over process. If area is not an issue these are the capacitive choice. N-channel over N-WELL capacitors have good density, but they have poor linearity over voltage. In situations where known voltages are applied across the terminals, these capacitors are best used.

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1. This would be in precision audio band outputs. When speakers, headphones, or lines are driven by these amplifiers.
2. 20 Hz - 20 KHz in the audio band.

However, they are suspect in any transient signal application. The MOSFET capacitors also have good density but have the worst linearity of the three. These capacitors are used in DC situations and in "last resort" cases where the other types are not available.

Silicided poly resistors are highly linear in comparison to the other types chosen but they have relatively low densities. They are the clear choice for linear applications. N-WELL resistors not only have large non-linearities with voltage and temperature, but they also vary greatly over process. However, one advantage that N-WELL resistors have is a very high density. These resistors are used in applications where very large resistors with little accuracy are needed. MOSFET resistors have linearity problems due to V_{ds} changes. The density is not as high as the N-WELL resistors, but is higher than that of the poly resistors. Applications are similar to those of N-WELL resistors but also include the application in a compensation network to match to a drive transistor.[1]

There are other solutions to these problems but they require additional process steps and cost. There are of course the passive elements available in analog CMOS process such as high permittivity oxide capacitors and poly-poly capacitors. There are pinched resistors which behave similarly to diffusion resistors but with much greater density. The addition of any "new" components to the digital process adds complexity and cost.

Three amplifiers have been presented and reviewed for applications in digital CMOS processes. It has been shown through simulation that the possibility of integration of current stand-alone analog functionality with digital products is now possible. Integrating processors and DSP cores with analog functionality at very high performances brings rise to an entirely new set of products. This is the future of low cost, low power, and high performance integrated circuits.

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1. There are applications where a MOSFET resistor is chosen in the compensation network where there is a zero placed to cancel a pole. The resistor value must track with a transconductance of a MOSFET and therefore this application. See chapters 2 and 3.

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