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Yunteng Huang for the degree of Doctor of Philosophy in Electrical & Computer Engineering presented on March 6, 1997.

Title: Design Techniques of High-Performance Switched-Capacitor Circuits in the Presence of Component Imperfections.

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Gabor C. Temes

This thesis describes design techniques for high-performance switched-capacitor (SC) circuits, primarily for high-linearity low-noise SC circuits in the presence of component imperfections, such as nonlinear op-amp voltage transfer characteristics, capacitor nonlinearities as well as the finite op-amp dc gain and op-amp offset and noise. Various correlated-double-sampling (CDS) schemes are discussed, and some novel predictive CDS schemes are proposed. Analysis, simulation and experimental results show that these schemes are very effective for reducing the effects of op-amp imperfections, resulting in lower signal distortion and reduced low-frequency noise and dc offset. The effect of capacitor nonlinearity in an SC circuits is analyzed in detail, and techniques for linearization are discussed. Applying these techniques, MOSFET capacitors can be used in high-performance digital-process-compatible SC circuit designs.

To verify the effectiveness of the proposed techniques, three prototype chips containing a 3-V all-MOSFET delta-sigma modulator, predictive gain- and offset-compensated track-and-hold stages, and SC amplifiers with various CDS techniques, were designed and fabricated in 1.2 μm CMOS technology. The measured results show that these circuit techniques are highly effective in high-performance SC circuit designs.

Design Techniques of High-Performance Switched-Capacitor Circuits in the Presence of Component Imperfections

by

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Design Techniques of High-Performance Switched-Capacitor Circuits in the Presence of Component Imperfections

Chapter 1. Introduction

This thesis describes design techniques for high-performance switched-capacitor (SC) circuits, primarily for high-linearity low-noise SC circuits in the presence of component imperfections, such as nonlinear op-amp voltage transfer characteristics, capacitor nonlinearities as well as the finite op-amp dc gain and input-referred op-amp offset and noise. Various correlated-double-sampling (CDS) schemes are discussed, and some novel predictive CDS schemes are proposed. Analysis, simulation and experimental results show that these schemes are very effective in reducing the effects of op-amp imperfections, resulting in lower signal distortion and reduced low-frequency noise and dc offset. The effect of capacitor nonlinearity in SC circuits is analyzed in detail, and techniques for linearization are discussed. Applying these techniques, MOSFET capacitors can be used in high-performance digital-process-compatible SC circuit designs. As an example, a 3-V all-MOSFET delta-sigma modulator prototype was developed using the series capacitor nonlinearity compensation technique. The measured results show that these circuit techniques are highly effective in high-performance SC circuit designs.

1.1 Motivation

There are a number of component imperfections that degrade the performance of an SC circuit. The most important ones can be divided into three categories. One is associated with noise effects, which corrupt the signal. These include the thermal noise, op-amp $1/f$ noise, op-amp offset and charge injection noise. The second category is associated with linear variations of the transfer function of the circuits, which cause gain error and misplaced pole/zero locations. These effects include the finite op-amp gain, parasitic capacitances and capacitor mismatch. The third one is associated with components'

nonlinear behavior, which causes signal distortion. These effects include the op-amps' nonlinear voltage transfer characteristics and the capacitors' voltage dependence. This research work concentrates on techniques for reducing the circuit's nonlinear distortion effect, with the other two categories only briefly discussed.

1.1.1 Sources of Harmonic Distortion in SC Circuits

Switched-capacitor circuits are widely used in the area of analog signal processing, such as analog-to-digital and digital-to-analog data converters, filters, precision gain stages, track-and-hold/sample-and-hold stages, etc. High performance is usually desired for these important building blocks. They feature a large dynamic range (DR), a high signal-to-noise ratio (SNR), high signal to total harmonic distortion (S/THD), and sometimes low power consumption as well. While the limiting factors for the DR and SNR are mainly electronic noise and quantization noise, the mechanism causing circuit nonlinearity is far more complex. It is well known that the sources of circuit nonlinear distortion are mainly analog component imperfections, namely, nonlinear MOS switch on-resistances, charge injection from MOS switches, nonlinear op-amp voltage transfer characteristics and capacitor nonlinearity. Techniques are available to cope with the first two sources [1],[2], but effective techniques to suppress the nonlinear distortion resulting from the latter two are not well developed.

1.1.2 Enhancing Op-amp Linearity Using CDS Techniques

With today's ICs moving towards the direction of low power and low cost, low supply voltages are commonly used in a mixed-signal device, and the use of basic CMOS technology for fabrication has become more and more desirable. Although low supply voltage does not necessarily lead to a low-power solution for analog circuitry, due to the large percentage of digital circuitry in today's mixed-signal ICs, it usually drastically reduces the overall chip power dissipation. Low-voltage operation, however, creates a

number of challenges for analog circuit designers who want to achieve high performance in SC circuits. One of these challenges is the trade-off between dynamic range and power consumption. In a low-voltage environment, the electronic noise becomes more significant relative to the reduced signal power. To achieve large dynamic range, large devices are normally used and more current is drawn. In addition, when the supply voltage is scaled down, the device threshold voltages do not get scaled down as much. This makes the signal voltage swing range even more important. Having larger signal voltage swing relative to the rails will decrease the power dissipation; but, on the other hand, due to the nonlinear op-amp voltage transfer characteristics, an increase of the op-amp output voltage swing increases the harmonic distortion as well. This scenario can be much improved by incorporating a CDS scheme in the circuit, especially by using the predictive CDS techniques proposed in this research work. It will be shown later that some types of CDS schemes can suppress nonlinear harmonic distortion in a narrow frequency range, while some can provide suppression over a wide frequency range.

1.1.3 Design of High-linearity SC Circuits Without High Linearity Capacitors

The use of basic digital CMOS technology for mixed-signal ICs results in lower manufacturing costs and shorter fabrication cycle, but at the same time it causes poorer linearity as well. This is because of the lack of high-linearity capacitors. In an analog CMOS process, high-linearity capacitors can be realized in a poly-to-poly or metal-to-poly structure with a few more mask layers than that for a standard CMOS process, while in a basic CMOS process, such capacitors are not available. It was proposed by earlier researchers [3][4] that the gate-to-channel capacitances of a MOSFET can be used as capacitors. When operating in their strong-inversion region or accumulation region, such capacitors can have higher unit-area capacitance and better matching accuracy than the other types of capacitors such as poly-poly, poly-metal or metal-metal capacitors. And, most importantly, they are available in any basic CMOS technology. However, their

capacitance shows a strong voltage dependence that is usually 10 to 100 times higher than that of the poly-to-poly or poly-to-metal implementations [7][8][9]. This degree of nonlinearity imposes a significant limitation on the practical use of the MOSFET capacitors in high-performance applications. To the author's best knowledge, none of the reported SC circuits implemented using MOSFET capacitors had signal to total harmonic distortion ratio (S/THD) better than 80 dB [3][4] when signal swing is close to 1 V.

We next discuss how capacitor nonlinearity causes distortion. In a SC circuit, an analog signal is processed by charge scaling and by transferring charge between capacitors. Complete charge transfer from one capacitor to another is made possible by the virtual ground of the op-amp. As will be shown in detail in Chapter 4, under certain conditions, the capacitor nonlinearity need not cause any signal processing imperfections if all the signal processing is done in the charge domain. Nonetheless, the input and output signals of a SC circuit are usually voltages, and the charge delivery from one stage to the next stage is achieved by sampling the output voltage of the previous stage and converting the voltage into charge via the input capacitors. If we can have linear charge delivery between stages and linear conversion between voltage and charge at the input and output of a SC circuit, we can perform linear signal processing with the overall circuit.

Based on the above observation, a high-linearity SC circuit can be designed using a high-linearity voltage-to-charge (V–Q) converter at the input, then processing the signal in the charge domain before it is sent to a high-linearity charge-to-voltage (Q–V) converter at the output. The high-linearity V–Q and Q–V converters can be realized by using linearized SC branches [4][5][6]. Having capacitors connected in series, the signal voltage swing across each capacitors is smaller, thus the linearity is much improved. In addition, having two capacitors with similar nonlinearity connected in opposite direction (back-to-back) also cancels the nonlinearity to a first-order approximation. A delta-sigma modulator

prototype utilizing this technique is described in this thesis and experimental results are shown.

1.2 Thesis Structure

Chapter 2 serves as an overview of correlated double sampling techniques. Some basic CDS schemes are discussed for comparators, T/H stages, voltage amplifiers and integrators. Then the principle of using CDS to suppress the op-amp harmonic distortion is introduced.

In Chapter 3, the concept of predictive CDS is introduced, and some novel predictive track-and-hold (T/H) stages are proposed. Some predictive CDS SC amplifiers and integrators are also discussed.

Chapter 4 deals with the capacitor nonlinearity problem. Analysis is performed on how capacitor nonlinearity affects the SC circuit linearity, then design techniques are described for high-linearity SC circuits using nonlinear capacitors.

In Chapter 5, kT/C noise analysis is performed for SC circuits, and a comparison is made between circuits employing correlated-double-sampling schemes.

Chapter 6 presents the design of a 3-V 96-dB dynamic range all-MOSFET delta-sigma modulator, and measurement results obtained from the prototype chip are also shown.

In Chapter 7, after a brief description of the predictive gain- and offset-compensated track-and-hold prototype chip, experimental results are shown and comparison is made with the other S/H stages implemented on the same chip.

Chapter 8 presents the experimental results on reduced harmonic distortion in circuits with gain-compensating CDS schemes. The measured results are obtained from a chip with various SC amplifiers.

Finally, Chapter 9 contains a summary of the work and plans for future work.

Chapter 2. Correlated Double Sampling: Background

Correlated double sampling techniques are often used to compensate for nonideal effects in op-amps, such as narrow-band ($1/f$) input-referred noise, input-referred offset and finite dc gain.

In this chapter, the basic principles of CDS operation are reviewed. Then the mechanism of signal distortion resulting from op-amp gain nonlinearity is investigated, and a solution based on CDS is proposed.

2.1 Introduction

The accurate operation of switched-capacitor circuits relies on accurate charge transfer between capacitors, so that the signal can be processed in the charge domain. This is achieved by the active elements used in the circuit. Operational amplifiers (op-amps) are often used as such elements, whose main function is to create a virtual ground. A virtual ground is a node that is forced to a constant potential and the current required to force it is steered in an error free manner to another part of a circuit. Using op-amps with MOS input transistors, the op-amp input current, which is the same as the virtual ground error current, at low frequencies can be made very small; however, the input voltage of a practical op-amp is usually significantly affected by several nonideal effects. These include input referred noise (most importantly, $1/f$ and thermal noise), input-referred dc offset voltage, as well as the signal voltage needed to generate the desired output voltage of the op-amp. In a low-supply-voltage design, such nonidealities will be more significant, because of the relatively larger noise compared to the limited signal swing, and high-gain op-amps might not be available. Typically, the thermal noise has a wide frequency band, while the $1/f$ noise and offset are narrow-band signals. The input signal can be either narrow-band or wide-band, depending on the application. The narrow-band noise (dc offset and $1/f$ noise),

because of the strong correlation between adjacent signal samples, can be greatly reduced using correlated double sampling techniques. These techniques are applicable to such important building blocks as comparators, voltage amplifiers, sample-and-hold (S/H) stages, ADC and DAC stages, integrators, etc.

2.2 The Basic Principle of CDS

The basic idea behind CDS is to sample the unwanted quantity (noise, offset as well as the induced signal at the op-amp input node), and then to subtract it from the instantaneous value of the contaminated signal either at the op-amp input node or the output node [10].

Figure 2.1 shows a simple offset-compensated comparator. The op-amp input referred noise is denoted as v_n, and is modeled as a voltage source at the op-amp input node. When ϕ_1 goes high, capacitor C is charged to the input-referred noise voltage v_n of the op-amp, and this value is subtracted from the input voltage v_{in} when $\phi_2 = 1$. A simple analysis shows that the transfer relation from v_n to v_{out} is

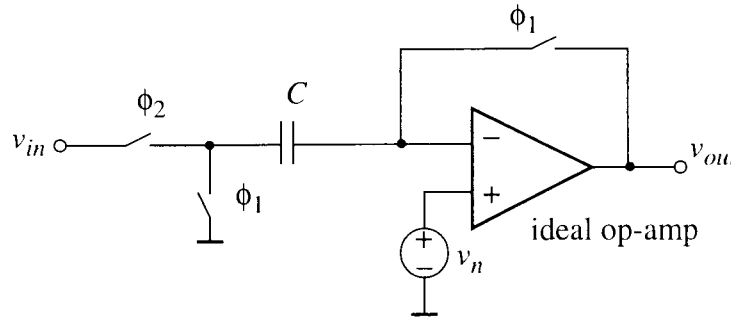


Figure 2.1: A simple offset-compensated comparator

$$V_{out}(z) = H_n(z) \cdot V_n(z) = (1 - z^{-1}) \cdot V_n(z). \tag{2.1}$$

The transfer function in the frequency domain is given by

$$|H_n| = 2 \cdot \left| \sin\left(\frac{\omega T}{2}\right) \right|, \tag{2.2}$$

where $V_{out}(z)$ and $V_n(z)$ are the z-domain output signal and the op-amp input referred noise, respectively. Figure 2.2 shows the magnitude response of the noise transfer function H_n. Since H_n is a highpass function, the low-frequency components of v_n are suppressed by this operation. Thus, the dc offset voltage and much of the input-referred $1/f$ noise will be suppressed. Note, however, that the voltage acquired by C during the $\phi_1 = 1$ interval does not contain the input signal v_{in}, and hence the effect of finite op-amp gain is not reduced by this circuit.

Unlike the dc offset voltage and $1/f$ noise, the thermal noise (generated by the switches and the op-amp) is a wide-band random process, and its adjacent samples are uncorrelated. Thus, the noise powers present at these samples do not cancel, but increase in the baseband due to aliasing.

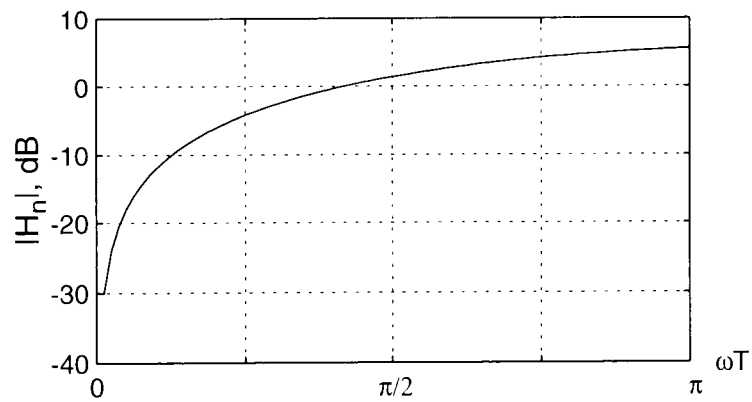


Figure 2.2: The magnitude response of H_n.

The basic operation described above is called auto-zeroing or offset cancellation. Also, since it cancels low-frequency noise by sampling it twice and generating the difference of these correlated samples, it is often called correlated double sampling, or CDS. (The term CDS is usually reserved for sampled-data circuits, while the others are applied for continuous-time circuits as well.)

2.3 Offset-Compensated SC Circuits

Shown in Figure 2.3 is a conventional SC voltage amplifier [11]. The ideal output is $v_{out} = -(C_1/C_2)\, v_{in}$, but the finite op-amp gain A and the input-referred dc offset V_{os} change it to

$$v_{out} = G_{id} \cdot (1 + E) \cdot v_{in} + (1 + G_{id}) \cdot V_{os}, \tag{2.3}$$

where

$$E = \frac{-(1 + C_1/C_2)/A}{1 + (1 + C_1/C_2)/A} \tag{2.4}$$

is the relative gain error and G_{id} is the ideal voltage gain $-C_1/C_2$. Thus, for typical values

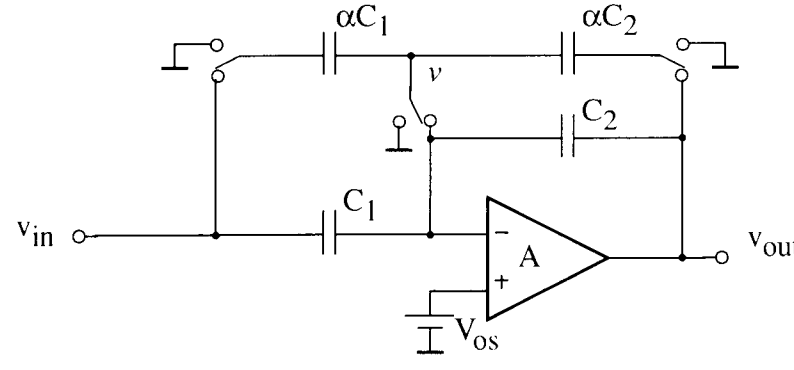


Figure 2.3: Uncompensated SC voltage amplifier

of A, G_{id} and V_{os}, namely (A = 60 dB, G_{id} = 10, and V_{os} =10 mV), a gain error of 1% and an output dc offset of 100 mV may occur. In some high-precision applications, e.g. if the amplifier is part of a DAC or ADC, this may be unacceptable. Also, the large output dc offset may become a significant limitation on the permissible signal swing, especially in low-supply-voltage designs.

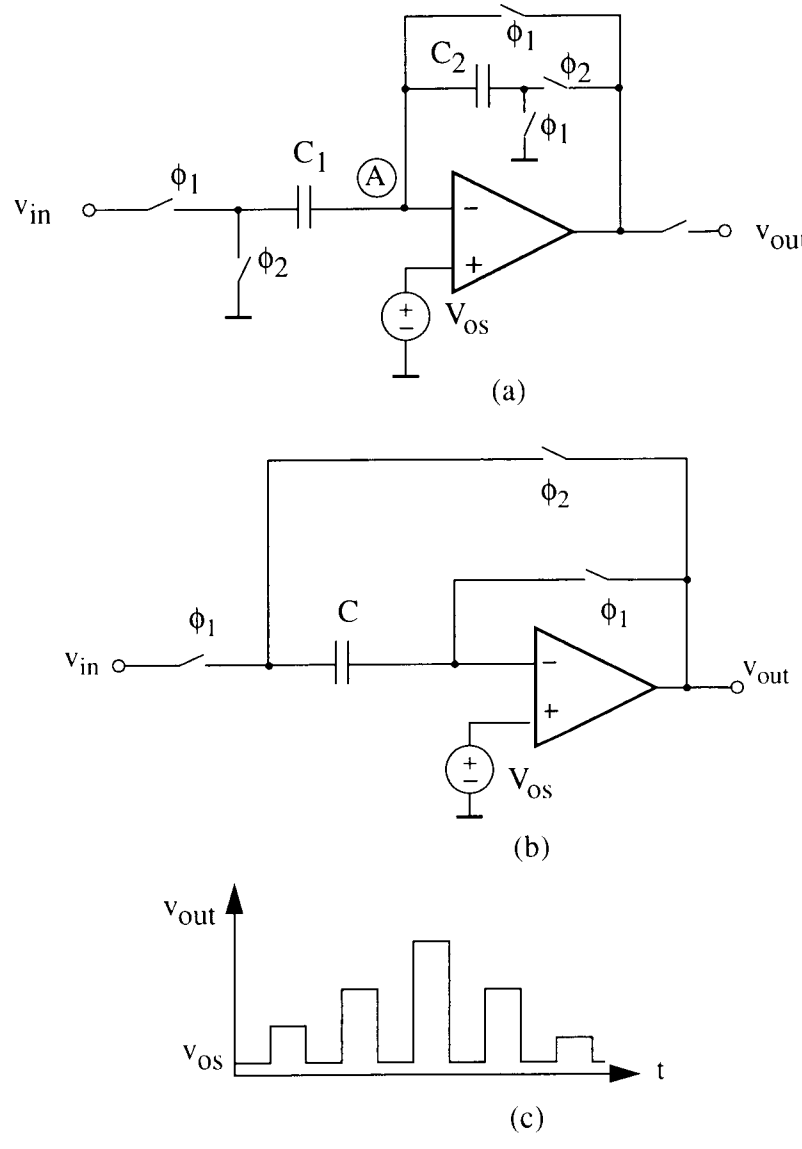


Figure 2.4: a. Offset-compensated SC amplifier; b. offset-compensated S/H; c: output waveform the two circuits.

Figure 2.4a shows a simple offset-compensated amplifier [13]. The output of this stage at the end of ϕ_2 is

$$v_{out} = \frac{-C_1/C_2}{1+(1+C_1/C_2)/A} \cdot v_{in} + \frac{V_{os}}{A}. \tag{2.5}$$

The effect of the op-amp dc offset as well as the input referred $1/f$ noise is now reduced by the op-amp open-loop gain A, and becomes negligible in most applications. The same auto-zeroing operation can be applied to a S/H stage and an offset-compensated S/H circuit (Figure 2.4b) is resulted . However, these circuits have some drawbacks. As Figure 2.4c illustrates, during the $\phi_1 = 1$ intervals the output is pulled to V_{os}, thus the op-amp must have a high slew rate to enable v_{out} to slew back and forth at each clock transition. Also, the stage gain is still affected by the finite dc gain of the op-amp in a same way as in the circuit of Figure 2.3.

2.4 Gain- and Offset-Compensated SC Circuits

An improved SC amplifier which does not require resetting of the output in each clock period, and hence allows more relaxed op-amp specifications for low- frequency inputs, is shown in Figure 2.5a [14]. In this circuit, the feedback reset switch is replaced by the elementary S/H branch consisting of C_3 and its two associated switches. Assume that the circuit is used as a noninverting amplifier, and hence the clock phases shown outside of the parentheses in Figure 2.5a are valid. Then, when $\phi_2 \rightarrow 1$, C_1 discharges into C_2, and the valid output voltage is generated. This voltage is stored in C_3. When next $\phi_1 \rightarrow 1$, C_3 becomes the feedback capacitor, C_1 samples the input, and C_2 discharges. If the signal bandwidth is much smaller than $f_s/2$, i.e. the signal is significantly oversampled, then v_{out} does not vary much from one clock phase to the next clock phase. Thus, for a finite dc op-amp gain A, the signal voltage $-v_{out}/A$ at the virtual ground is a slowly varying signal which is therefore nearly cancelled by the CDS switching of C_1 and C_2. This reduces the effect of the op-amp finite gain A on the voltage gain of the stage.

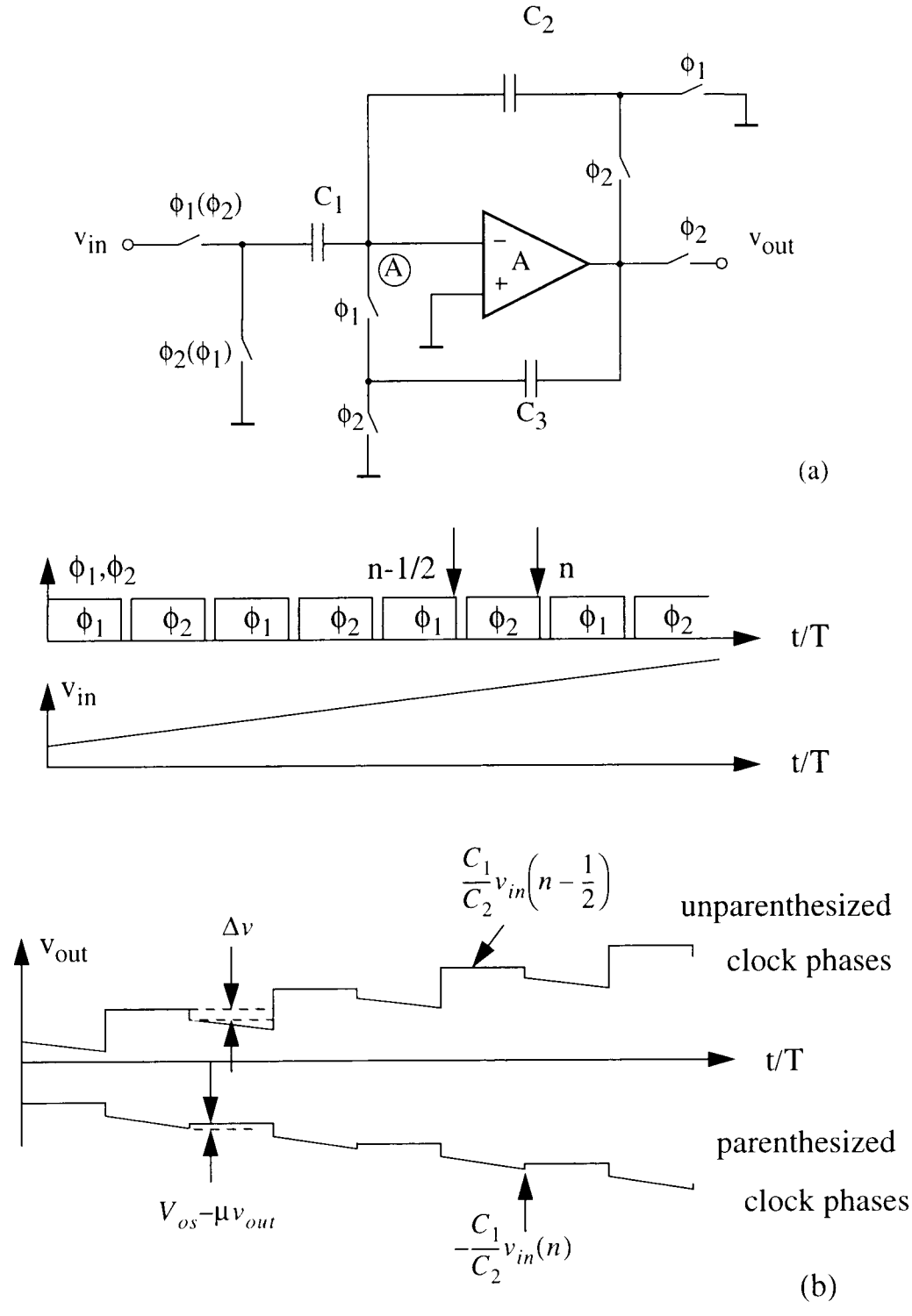


Figure 2.5: a. An offset- and finite-gain-compensated SC amplifier; b. clock and signal waveforms.

Figure 2.5b illustrates the clock phases and waveforms of the amplifier. When $\phi_1 \rightarrow 1$ and the reset phase begins, there is a small step $\Delta v = V_{os} - \mu v_{out} - (C_1/C_3)\Delta v_{in}$ in the output voltage, where Δv_{in} is the change in v_{in} during the $\phi_2 = 1$ interval. (The Δv_{in} term enters only for noninverting operation.) This occurs because, as $\phi_1 \rightarrow 1$, C_3 is disconnected from ground and reconnected to the virtual ground. Here $\mu \equiv 1/A$. As Δv is of the order of a few mVs, this step change does not require a fast settling time or a high slew rate from the op-amp. The dc output offset voltage is $\mu\ (1+C_1/C_2)\ V_{os}$.

Detailed analysis [14] shows that the gain is now weakly frequency dependent due to the highpass CDS effect on the virtual ground voltage, with the dc gain given by

$$H(z)_{z=1} = \frac{-C_1/C_2}{1 + (1 + C_1/C_2)\mu^2} \tag{2.6}$$

As Eq. (2.6) demonstrates, the error term in the denominator of the transfer function is now proportional to μ^2, rather than μ, Thus, the effective value of the op-amp gain as far

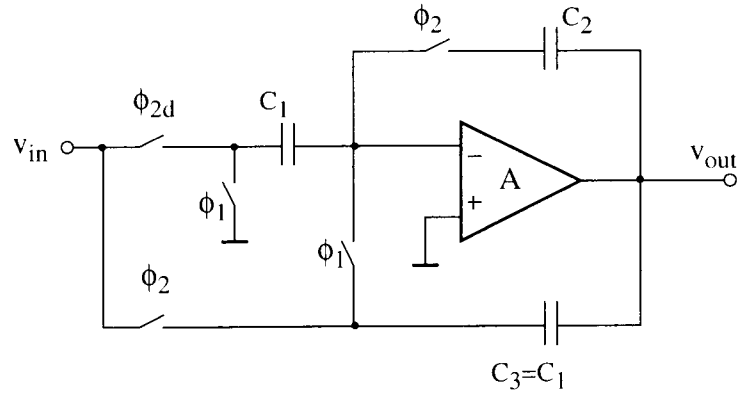


Figure 2.6: Gain- and offset-compensated SC integrator.

as the dc gain is concerned is the square of the true value. Circuits with this property are called gain-enhanced or gain-squaring stages.

With some modifications, the compensation schemes described above can also be applied to SC integrators. Figure 2.6 shows a gain- and offset-compensated SC integrator. Unlike in a SC amplifier where the feedback capacitor C_2 is completely discharged during every clock phase ϕ_1, and its charge cancels the charge from C_1, here, in order to balance the charge flow from C_1 when ϕ_1 goes high, C_3 needs to be precharged between input and output during ϕ_2. To reduce the signal-dependent charge injection, the switch that disconnects C_2 from the feedback path should be moved from the side of the op-amp output to the op-amp input. Simple analysis shows the input referred offset is reduced to $\mu\ (1+C_1/C_2)\ V_{os}$, and the pole error is now $(C_1 / C_2)\mu^2$ [18].

2.5 Reducing Harmonic Distortion Using CDS Schemes

Aside from the input-referred noise and finite gain, one other major limitation of the monolithic op-amp in an SC circuit is its nonlinearity. In a continuous-time application (or during instantaneous operation within one clock phase in an SC circuit) as shown in

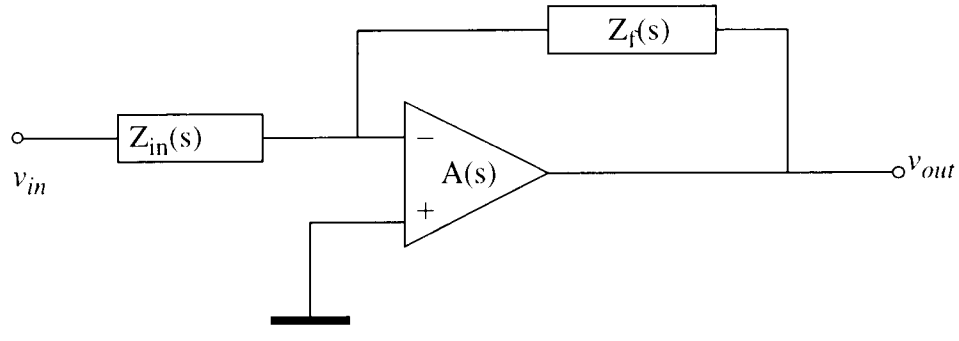


Figure 2.7: A closed-loop op-amp.

Figure 2.7, it is known that the open-loop harmonic distortion is suppressed by the loop gain under close-loop operation.

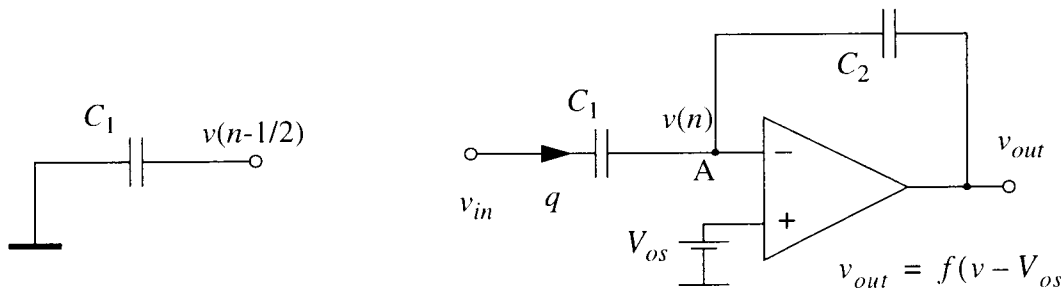
$$HD_{closed-loop} \approx \frac{HD_{open-loop}}{A(s) \cdot \dfrac{Z_{in}(s)}{Z_{in}(s)+Z_f(s)}}. \tag{2.7}$$

Eq. (2.7) shows that the higher the loop gain is, the lower the harmonic distortion will be. In a sampled-data system, the harmonic distortion can be further suppressed by using a gain-compensation scheme. Depending on the actual scheme, CDS can provide harmonic suppression over a narrow band or a wide band in the discrete frequency domain.

Consider the simple charge-transfer operation shown in Figure 2.8, where the op-amp open-loop voltage transfer function is denoted as $v_{out} = f(v_i - V_{os})$. Here, v_i and v_{out} are the voltages of the op-amp input node and output node, respectively, and V_{os} is the input-referred offset. At the nth clock transition, the charge entering into node A can be found as

$$q = C_1[v_{in} - v(n) + v(n-1/2)] = C_1[v_{in} - v_e], \tag{2.8}$$

where the error term is



during discharging phase

during charging phase

Figure 2.8: Charge transfer in SC circuit.

$$v_e = v(n) - v(n-1/2) = f^{-1}[v_{out}(n)] - f^{-1}[v_{out}(n-1/2)]. \quad (2.9)$$

Clearly, the closer $v_{out}(n)$ is to $v_{out}(n - 1/2)$, the smaller the charge transfer error will be.

In many correlated double sampling schemes, the right side of C_1 in Figure 2.8 is never disconnected from the op-amp input node (CDS circuits with error storage capacitors are exceptions), so that $v(n - 1/2) = V_{os} + f^{-1}[v_{out}(n - 1/2)]$. Assume the op-amp is fully differential and the input/output relationship can be written in the form

$$v = V_{os} + f^{-1}(v_{out}) \cong V_{os} + \mu \cdot v_{out} + \alpha \cdot v_{out}^3. \quad (2.10)$$

Where α is a constant coefficient from the Taylor expansion of f^{-1}. Then we have

$$v_e \cong \zeta \cdot [v_{out}(n) - v_{out}(n-1/2)], \quad (2.11)$$

where

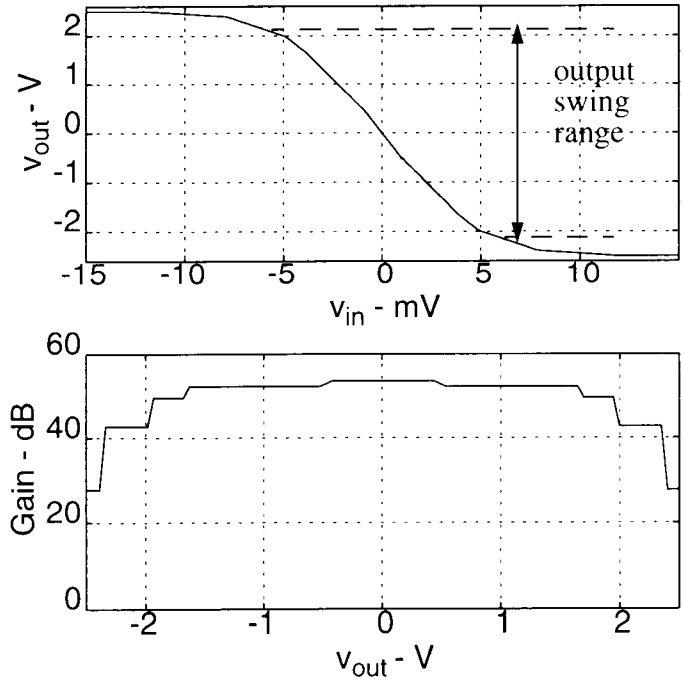


Figure 2.9: a: op-amp nonlinear transfer characteristics; b: op-amp gain vs. op-amp output.

$$\zeta = \mu + \alpha \cdot [v_{out}^2(n) - v_{out}(n) \cdot v_{out}(n-1/2) + v_{out}^2(n-1/2)]. \qquad (2.12)$$

From Eq. (2.11), we can conclude that the closer $v_{out}(n)$ is to $v_{out}(n\text{-}1/2)$, the smaller the charge transfer error and the nonlinear term will be. It should be pointed out that the reduced charge transfer error also leads to the reduced gain error in SC amplifiers and reduced pole error in SC integrators with CDS.

To verify the effectiveness of harmonic distortion reduction in gain-compensated SC circuits, simulations were performed for the SC amplifier shown in Figure 2.5a, and the

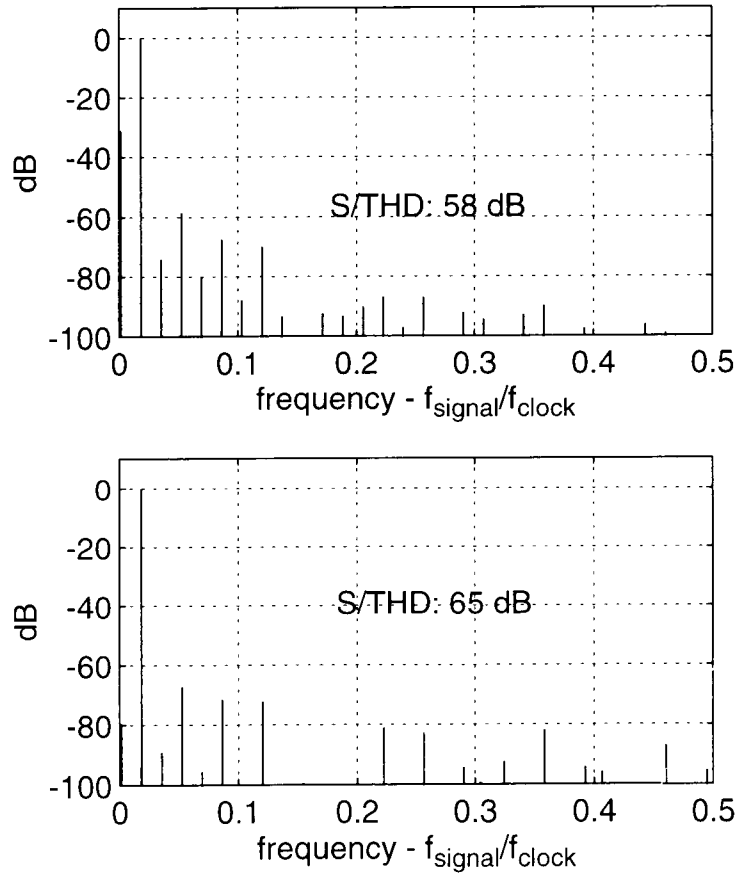


Figure 2.10: FFT spectrum of a: the uncompensated SC amplifier of Figure 2.3; b: gain- and offset-compensated SC amplifier of Figure 2.5.

uncompensated SC amplifier in Figure 2.3 for comparison. An op-amp is assumed with the piece-wise linear voltage transfer characteristics shown in Figure 2.9, and with an input referred offset voltage of 5 mV. The op-amp unity-gain frequency is assumed to be infinite for complete settling during each clock phase. The output voltage swing is 2.2 $V_{p\text{-}p}$ and the closed-loop voltage gain is -2. Figure 2.10 shows the resulting output spectra for the two SC amplifiers. The gain- and offset-compensated amplifier shows about 15 dB reduction on the second-order harmonic, and 8 dB reduction on the third-order harmonic. However, for higher-order harmonics at higher frequencies, the suppression decreases rapidly, and even amplification occurs for harmonics whose frequencies are higher than one-tenth of the clock frequency. This is due to fact that in the circuit of Figure 2.5, $v_{out}(n-1/2) \cong v_{out}(n-1)$, and the error voltage in Eq. (2.11) has a high-pass filtered spectrum. More detailed analysis and discussion will be given in the next chapter.

2.6 Conclusions

The error voltage at the op-amp input node contains the input-referred noise, the dc offset and the induced signal due to the finite op-amp gain. The goal of correlated double sampling is to reduce this error. Since the $1/f$ noise and dc offset are narrow-band signals, and the correlation between adjacent samples is strong, they can be greatly reduced by an operation similar to differentiation, i.e., subtraction of the unwanted quantity from the next sample. For the finite op-amp gain induced signal, the same argument can be applied for over-sampled systems, where the input signal frequency is much lower than the clock frequency. However, for applications in which Nyquist sampling must be used, this kind of technique is no longer effective. This leads to the discussion of predictive correlated double sampling, where the correlated sampling action is made when the op-amp has a predicted value of the output for the next clock phase.

Chapter 3. Predictive Correlated Double Sampling

In the last chapter, basic correlated double sampling techniques were introduced. They are very effective in reducing the input-referred narrow-band noise, as well as compensating the finite op-amp dc gain in a narrow signal frequency range. However, in some SC circuits such as track-and-hold or sample-and-hold stages, Nyquist-rate data converters, post filters of $\Delta\Sigma$ ADCs, etc., the input signal frequencies are close to (or even higher than) half the sampling frequency. This makes the CDS techniques introduced in chapter 2 ineffective when it comes to gain compensation and harmonic distortion suppression. To achieve gain-compensation over the entire frequency band, predictive CDS techniques ought to be used. A predictive CDS scheme is a circuit in which the op-amp predicts its output for the next clock period during the present clock period, so that the adjacent two samples are nearly the same. The predictive operation results in a maximum correlation between the unwanted signal and the signal that is subtracted during the double sampling intervals. Since predictive CDS schemes can compensate for the op-amp input-referred offset and reduce the finite op-amp gain effect over a wide signal frequency range, they are also called wideband *gain- and offset-compensated* (GOC) circuits. In this chapter, some novel predictive gain- and offset-compensated T/H stages are proposed, and then some existing and some newly proposed predictive CDS schemes for SC gain stages and integrators are described and compared.

3.1 Gain- and Offset-Compensated Track-and-Hold Stages

High-accuracy and high-speed CMOS track-and-hold stages are widely used in data acquisition systems, pipeline ADCs, time-interleaving ADCs and other applications. The design challenges often come from the op-amp's dc offse, finite gain and finite slew rate. Here, some novel fully-differential track-and-hold stages are proposed. The gain of the stages does not depend on capacitor matching, and they use a predictive CDS scheme to

reduce the effects of op-amp offset and finite dc gain. By incorporating an improved switching scheme, the slew rate requirement for the op-amp can be relaxed as well. Due to these properties, they are well suited, e.g., for the construction of the front stage in a parallel (time-interleaving) system. Simulations indicate that these circuits are capable of high-speed and high-accuracy operation without requiring high-quality components.

3.1.1. A Non-Predictive Track-and-Hold Stage

To improve the track-and-hold stage in Figure 2.4b, a gain- and offset-compensated S/H (Figure 3.1a) was proposed in 1987 by Wang and Temes [19]. It does not require

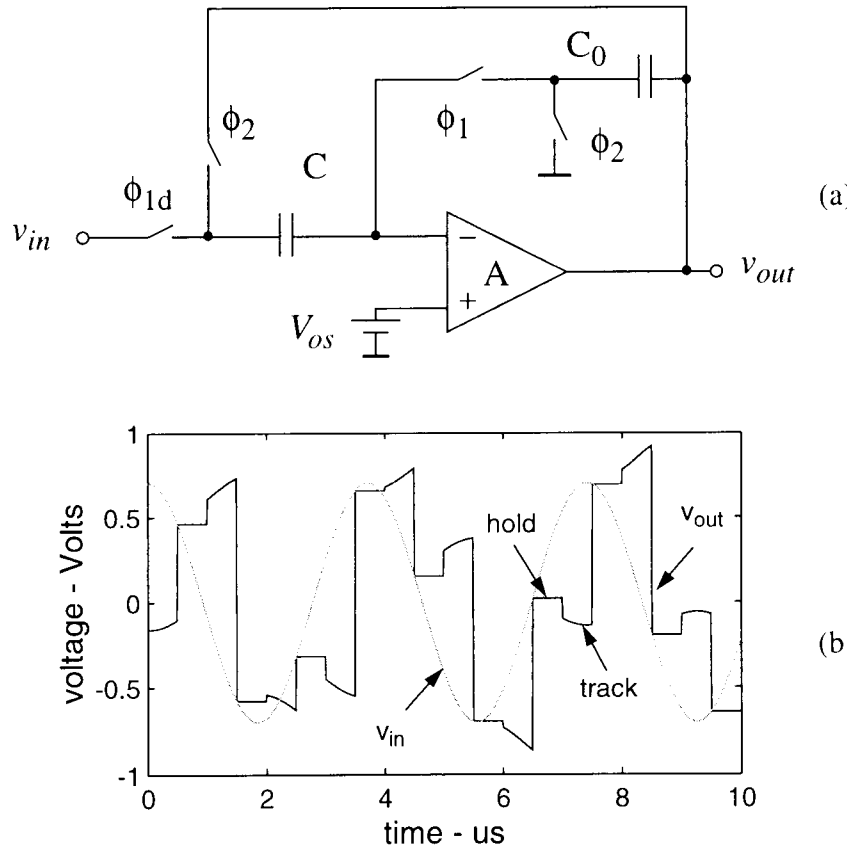


Figure 3.1: Gain- and offset-compensated track-and-hold stage.
a: circuit diagram; b: input and output waveforms. ($C_0 / C = 4$)

resetting the output voltage in every clock phase, so that the op-amp does not have to slew drastically during each clock transition. The circuit compensates the op-amp offset voltage V_{os} and provides reduced sensitivity to the finite dc gain A of the op-amp when the input signal frequency is much lower than the clock frequency. Analysis reveals that the output during the holding phase is

$$v_{out}(z) \approx \frac{1-\mu \cdot C/C_o}{1+\mu \cdot (1-z^{-1}-z^{-1} \cdot C/C_o)} \cdot v_{in}(z) + \mu \cdot V_{os}(z). \qquad (3.1)$$

where $\mu = 1/A$. At low frequencies ($z \approx 1$), if μ, $C/C_0 \ll 1$, v_{out} follows v_{in} closely. However, if the input signal frequency is high, close to $f_s/2$ ($z \approx -1$), Eq. (3.1) indicates a gain error that is even greater than for an uncompensated circuit. This drawback stems from the absence of accurate tracking. As Figure 3.1b shows, the output voltage does not actually track the input during the tracking time interval when ϕ_1 is high. In fact, the output voltage changes in a direction opposite to that of the actual input signal with a gain C/C_0. It undertakes a voltage jump $C/C_0 \cdot [v_{in}(n) - v_{in}(n-1/2)]$ during the nth transition from HOLD to TRACK, and a voltage jump $(1 + C/C_0)[v_{in}(n) - v_{in}(n-1)]$ during the nth transition from TRACK to HOLD. This reduces both the speed and the available swing during the operation. Increasing C_0/C will slightly ease this problem at the cost of larger silicon area and slower slewing and settling when the circuit enters the HOLD mode.

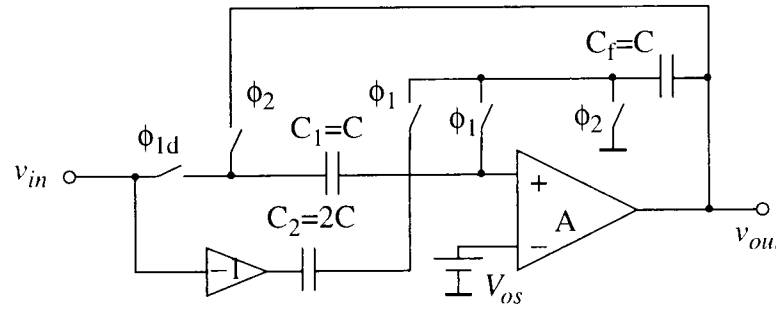
3.1.2. Predictive CDS Track-and-Hold Stage

Having identified the problem of the gain- and offset-compensated T/H in Figure 3.1, a straightforward improved circuit is shown in Figure 3.2. The input signal is sampled using a delayed-cutoff clock signal ϕ_{1d} to reduce the signal-dependent clock feedthrough noise. The operation of the stage is as follows. When ϕ_1 goes high, the circuit enters the TRACK mode: v_{out} changes from the earlier held value of v_{in} to the present input voltage and tracks it. During the interval when ϕ_1 remains high, $v_{out} = v_{in}$ is valid under

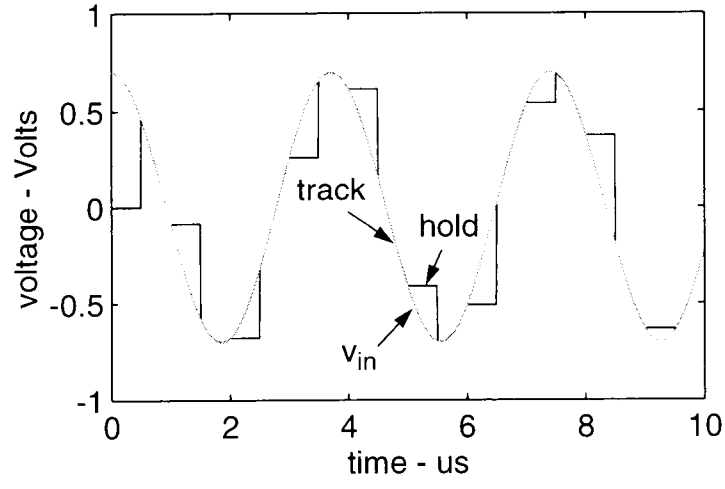
ideal conditions. As ϕ_2 goes high and the HOLD interval begins, the input capacitor C_1 is therefore precharged to a voltage

$$v_{c_1} = v_{in} - V_{os} + v_{in}/A. \tag{3.2}$$

As Eq. (3.2) shows, when ϕ_2 goes high and the left-side terminal of C_1 is switched to the output node, the output voltage becomes



(a)



(b)

Figure 3.2: Predictive gain- and offset-compensated T/H. a: the circuit configuration; b: the input and output signal waveforms.

$$v_{out} = V_{os} - v_{out}/A + v_{c1} = v_{in}(1 + 1/A) - v_{out}/A . \qquad (3.3)$$

This gives $v_{out} = v_{in}$. Thus, even in the presence of finite gain and nonzero offset of the op-amp, the held value of the output voltage is identical to the input signal sampled at the time instant when ϕ_{1d} went low.

The operation described above does not depend on having a high oversampling ratio, and hence the circuit is inherently suitable for high-frequency applications. However, the derivation assumed that $v_{out} = v_{in}$ holds exactly during tracking. In fact, V_{os} and A do affect the tracking output slightly, as a more exact analysis reveals. Assuming $C_1 = C_f = C_2 / 2 = C$, the z-transform of the T/H output when $\phi_2 = 1$ is then found to be

$$V_{out}^{(2)}(z) = \frac{1}{1 + (4 + z^{-1})/(A(A + 5))} V_{in}(z) + \frac{V_{os}(z)}{A + 5 + (4 + z^{-1})/A} . \qquad (3.4)$$

If $A \gg 5$, $v_{out}^{(2)}$ can be approximated by

$$V_{out}^{(2)}(z) \approx \frac{V_{in}(z)}{1 + (4 + z^{-1})/A^2} + V_{os}(z)/A . \qquad (3.5)$$

Thus, the error terms due to the finite gain and the nonzero offset are both reduced by a factor $1/A$, thanks to the predictive correlated double sampling (CDS) used in the circuit. (The error in $v_{out}^{(1)}$ is only the op-amp input-referred error of $v_{out}^{(2)}$!) The mismatch between the capacitors which are nominally equal to C and $2C$ also affects the compensation. However, this effect is usually negligible, since it only appears during the tracking mode, and hence the error which it causes in the held signal is second-order small. Unlike in earlier T/Hs, the error in the output given in Eq. (3.5) changes only slightly with frequency, so the speed limitation of the stage is mainly due to the unavoidable settling time of the op-amp.

The circuit of Figure 3.2 is easily converted to a more practical fully-differential operation, which also makes the voltage inversion used in the single-ended circuit unnecessary (Figure 3.3). In Figure 3.3, V_{com} is the desired common-mode input voltage of the op-amp. In the circuit, we also included two "deglitching" capacitors C_{dg1} and C_{dg2}, which provide feedback for the op-amp during the time interval when the non-overlapping clock phases ϕ_1 and ϕ_2 are both low [20], and hence reduce the sharp voltage spikes ("glitches") which would otherwise be generated during this interval. Since the switches at the input are opened by ϕ_{1d} somewhat earlier later the other switches operated by ϕ_1, the clock-feedthrough noise becomes nearly signal-independent and is thus suppressed by the op-amp common-mode rejection.

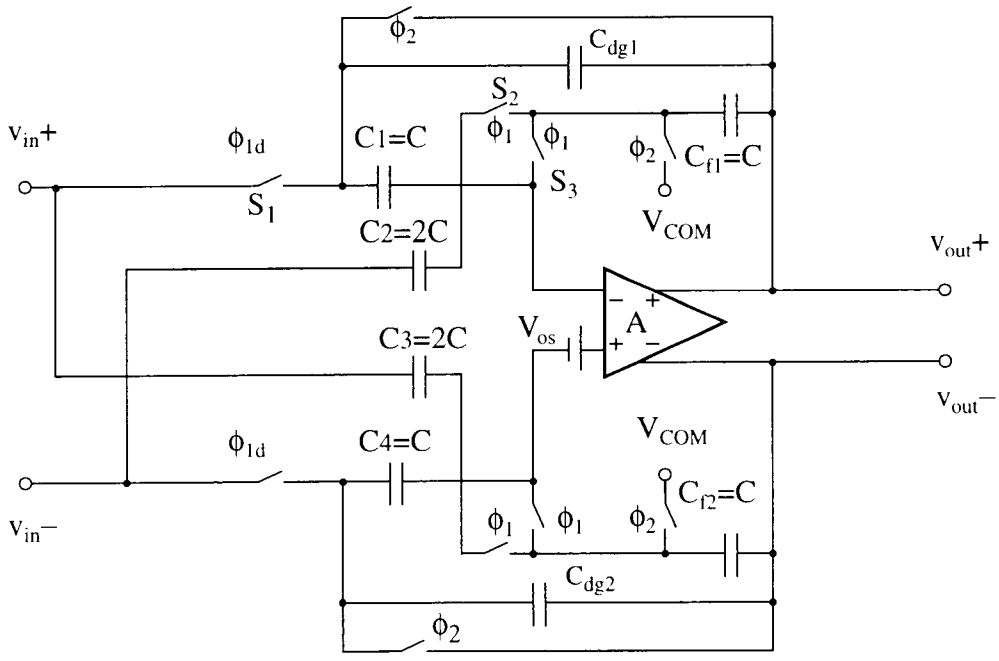


Figure 3.3: Fully-differential track-and-hold circuit.

The proposed T/H stages can also be converted into the more commonly used S/H stage by cascading a master and a slave T/H, or by using the "ping-pong" architecture shown in Figure 3.4. Here, the two T/H stages operate in tandem, and the output voltage

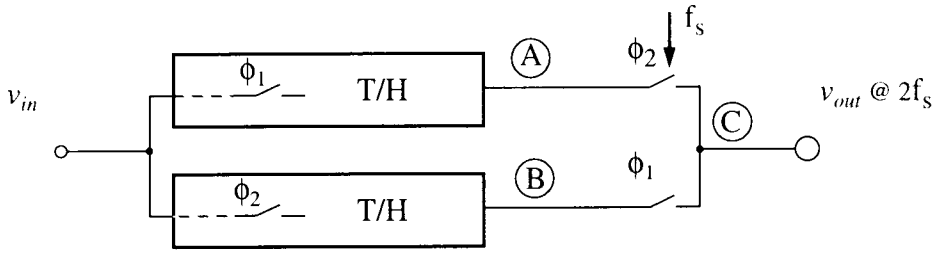


Figure 3.4: S/H stage using two T/H blocks.

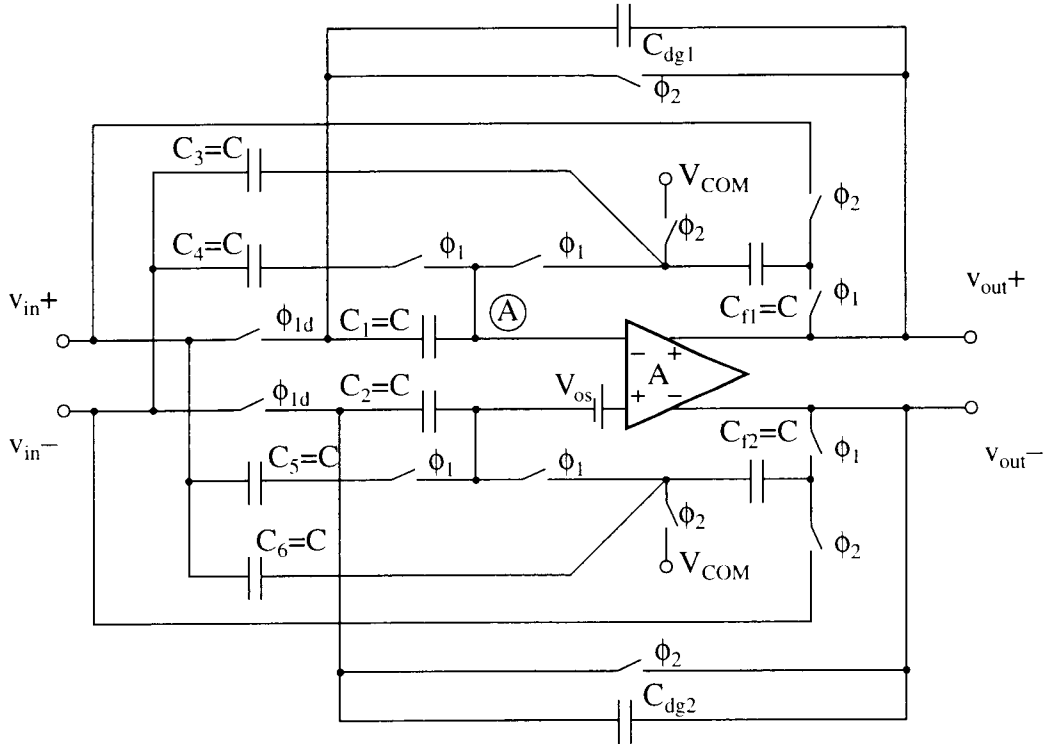


Figure 3.5: Fully-differential track-and-hold circuit with improved switching scheme.

v_{out} contains only the held outputs. This operation requires two T/H circuits, but it doubles the effective sampling rate. Since both stages have very accurately controlled voltage gains $A_v = 1$, and both have very little offset and finite-gain errors, the mismatch error usually present in ping-pong structures is likely to be negligible in most applications. However, the MOS switch clock-injection mismatch between the channels may introduce a fixed tone at f_s, as will be shown later in Sec. 3.1.3.

Figure 3.5 shows an improved switching scheme for the proposed T/H stage. An improvement in speed and accuracy is achieved by precharging all capacitors appropriately during the HOLD mode. This is achieved by splitting each of the input tracking capacitors C_2 and C_3 of Figure 3.3 into two equal-value capacitors ($C_3 - C_6$ in Figure 3.5) and using them differently. Consider the transition into the tracking mode, which is the critical part of the operation. When ϕ_1 goes high, C_1 sends a charge $q_1 = C_1 [v_{in}(n) - v_{in}(n-1)]$ into node A. This is now balanced by an equal but opposite charge through C_4. Since C_{f1} was precharged to $v_{in}(n)$ during the hold interval when $\phi_2 = 1$, and since C_3 (which is precharged to $-v_{in}(n)$) does not contribute charge to node A when $\phi_1 -> 1$, the capacitors need not be charged by the op-amp to achieve $v_{out}(n) = v_{in}(n)$, when ϕ_1 goes high. This reduces the slewing as well as the settling time of the op-amp when tracking is resumed.

Next, we consider the speed requirements for the op-amp. Figure 3.6 shows the circuit configurations of the T/H of Figure 3.5 during both clock phases. They will be used to calculate the op-amp's settling time constants during the track and hold operations. For simplicity, only half of the fully-differential circuit is shown. The parasitic capacitances at the OTA input are denoted as C_{pi}, and the capacitive loads at the op-amp output during tracking and holding are denoted as C_{LT} and C_{LH}, respectively. Without loss of generality, a single-stage OTA is assumed, with its dominant pole residing at the output node. Let the

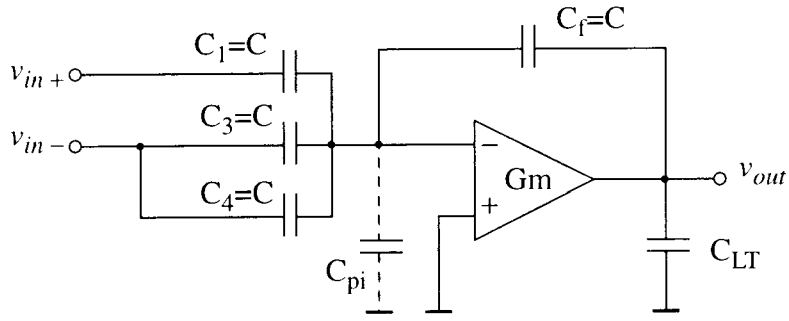
transconductance of the OTA be *Gm*, then the settling time constant during tracking phase can be obtained as

$$\tau_{track} = \frac{(3C + C_{pi}) + C_{LT}/\beta_{track}}{Gm}, \tag{3.6}$$

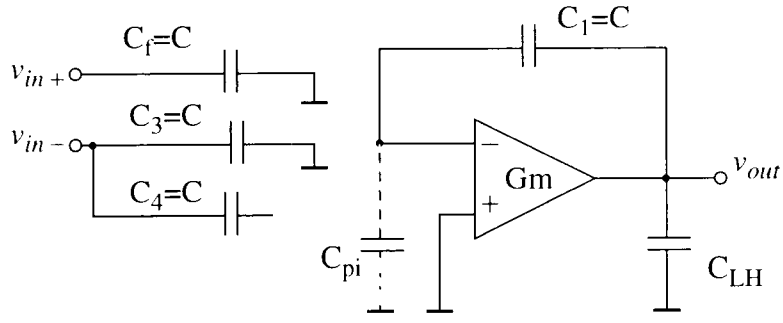
where β_{track} is the op-amp feedback factor during the track phase, defined as

$$\beta_{track} = \frac{C_f}{C_f + C_1 + C_3 + C_4 + C_{pi}} \approx \frac{1}{4}. \tag{3.7}$$

Similar analysis for the holding phase yields



(a)



(b)

Figure 3.6: Op-amp capacitive load for the circuit in Figure 3.5.
a: during tracking; b: during holding.

$$\tau_{hold} = \frac{C_{pi} + C_{LH} \cdot (1 + C_{pi}/C)}{Gm} \tag{3.8}$$

It should be noted that in most T/H applications (such as a front stage in a flash ADC), the op-amp's capacitive load during the track phase (C_{LT}) is usually much smaller than that during the hold phase (C_{LH}). Equalizing τ_{tack} and τ_{hold} can be easily achieved by optimizing the values of C, C_{LT} and C_{LH}. The speed of tracking, nonetheless, is greatly affected by the small feedback factor during tracking as Eq. (3.7) shows. Also, because the input signal is sampled on C_1 between input v_{in} and the op-amp virtual ground, slow op-amp settling during tracking directly affects the accuracy of the signal being sampled.

To alleviate these problems, the T/H stage can be further modified as shown in Figure 3.7. Delayed cut-off clock signals ϕ_{1d} and ϕ_{2d} are used to reduce the signal-dependent charge-injection noise. The circuit uses a capacitor C_{store} to store the error voltage ($V_{os} + V_{out}/A$) at the op-amp input terminal during the tracking. Also during the tracking phase (Figure 3.7b), C_1 and C_2 together with the op-amp forms an inverting unity-gain stage. (Assuming $C_1 = C_2$ and neglecting the small amount of charge entering C_{store}.) Interchanging the two terminals of the differential input signal, the op-amp output v_{out} is actually equal to v_{in} without being inverted. Meanwhile, C_{samp} samples the input signal referred to the analog ground, rather than the op-amp virtual ground as in the circuit of Figure 3.5. Next, when ϕ_2 goes high and the circuit enters its hold phase, C_{samp} is switched in series with C_{store} and acts as the feedback capacitor in the unity-feedback configuration. At the same time, C_1 and C_2 are precharged to $-v_{in}$ and $+v_{in}$, respectively, so that the op-amp does not have to provide the slewing current for them when tracking resumes in the next clock phase. Notice that the feedback factor during tracking is now increased to approximately 1/3, which means that the settling is faster than that of the circuit in Figure 3.5.

The kT / C noise in the held output now contains the noise from the two switched capacitors C_{samp} and C_{store}. However, since C_1 and C_2 now can be smaller than C_{samp}, to

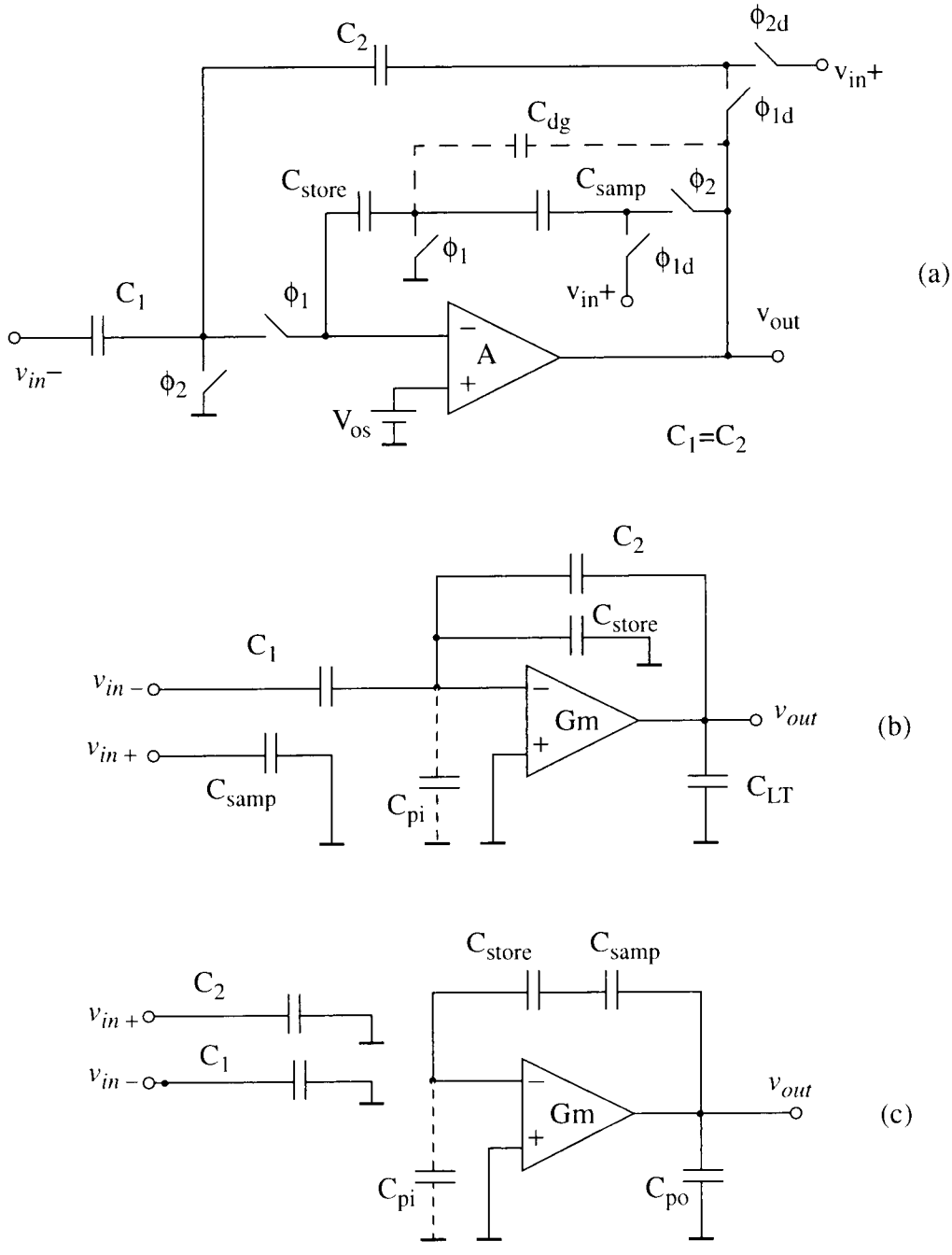


Figure 3.7: A predictive gain- and offset-compensated T/H using an error storage capacitor. a: the basic circuit; b: circuit configuration during tracking; c: circuit configuration during holding.

achieve the same dynamic range, the penalty from increased capacitor area and op-amp capacitive load should not be significant. Detailed analysis of the kT / C noise in this circuit is given in Appendix A.

The circuit of Figure 3.7a has a capacitive load about $3C$ at the input nodes during the track mode. This may impose some added driving requirements on the signal source. To alleviate this problem, an alternative circuit may be used (Figure 3.8). In Figure 3.8, C_1 and C_2, instead of being precharged to v_{in} during the hold phase (ϕ_2), remain at the voltage of the previous sample $v_{in}(n\text{-}1)$. When next ϕ_1 goes high, a charge $C_1[v_{in}(n) - v_{in}(n\text{-}1)]$ enters C_2, so that the output tracks the input as in the circuit of Figure 3.7a. The disadvantage of this circuit is the slewing requirement for the op-amp at the beginning of each tracking phase.

The finite-gain compensation of the correlated-double-sampling circuits described is achieved by sampling the error voltage (v_{out}/A, or $f^{-1}[v_{out}]$ in general) at the op-amp

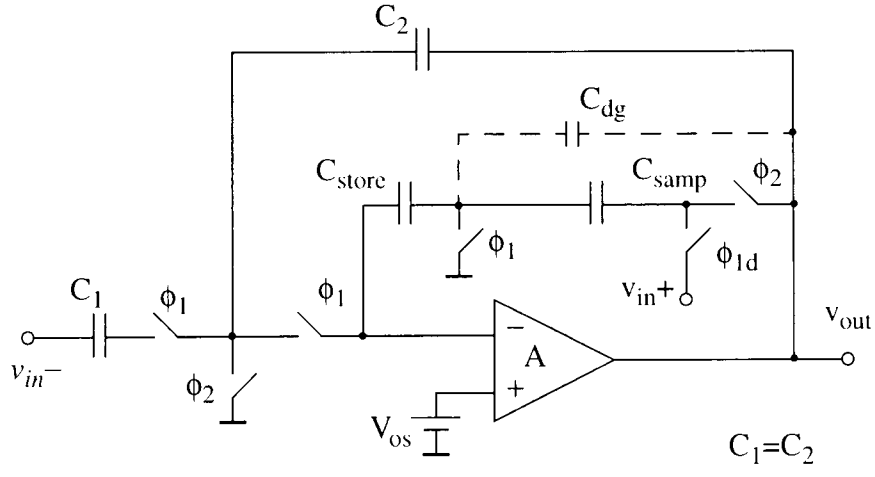
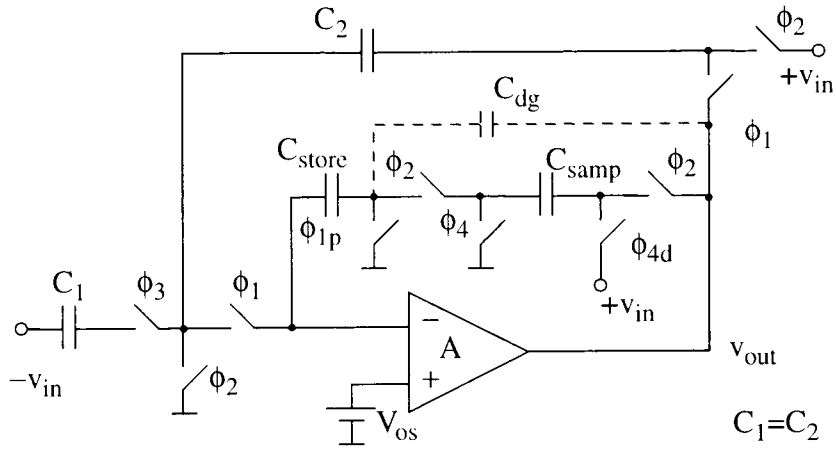
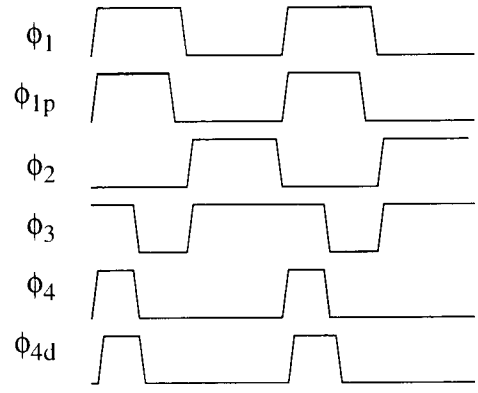


Figure 3.8: An alternative predictive GOC T/H.

input node during one clock phase, and then subtracting this error voltage from the output during the next clock phase. In particular, predictive CDS circuits sample the error voltage



(a)



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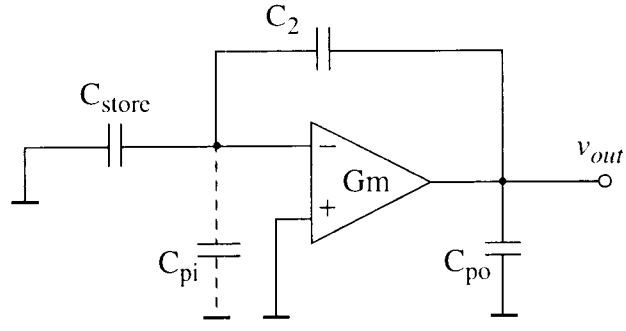


(c)

Figure 3.9: High-speed T/H with a self-settling phase. a: the circuit; b: the clock signals; c: circuit configuration during self-settling interval (ϕ_3 is low).

when the op-amp output reaches the predicted value in the next clock phase, so that the error voltages resulting from the op-amp are almost the same in the two adjacent clock phases. Hence the errors in the adjacent samples are maximally correlated. As a result, the error due to the op-amp offset and finite gain is cancelled. However, this cancellation is based on the assumption that the op-amp behaves the same way during the two double sampling clock periods. This is true in most switched capacitor circuits, where the operation is based on the steady-state settling in each clock phase. In a S/H circuit, however, the op-amp operates with a time-varying input signal during tracking, and operates with a dc input during holding. Depending on the actual op-amp frequency response and the operating frequency range of the circuit, the op-amp gain A or the op-amp voltage transfer function $v_{out} = f(v_{in})$ may be quite different during the track and hold

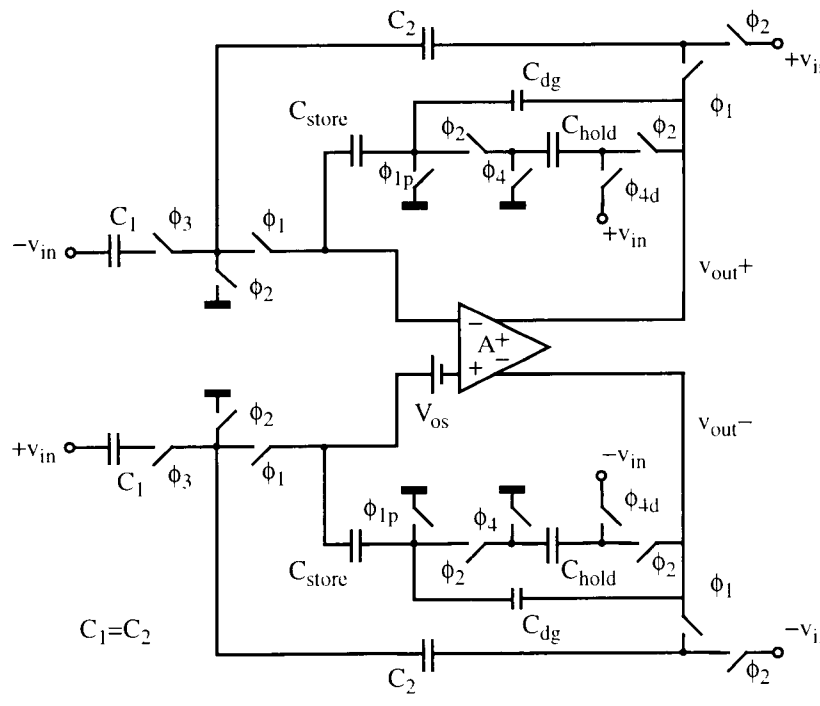


Figure 3.10:Fully differential realization of the improved gain- and offset-compensated THA.

operations. This different op-amp behavior during the two double-sampling clock periods will result in inaccurate gain-compensation.

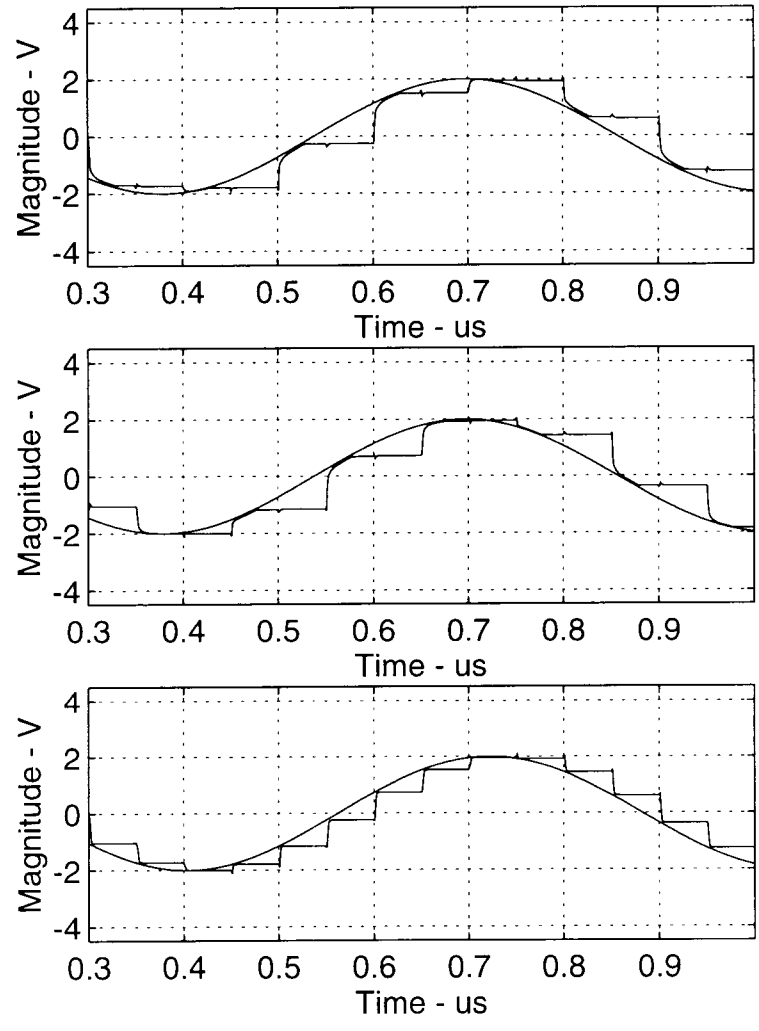


Figure 3.11:HSPICE simulation of the "ping-pong" structure. (a) T/H *A* output and the input signal; (b) T/H *B* output and the input signal; (c) the "ping-pong" output and the input signal.

To solve this problem, a self-settling interval can be introduced. The modified T/H circuit of Figure 3.7 is shown in Figure 3.9. In this circuit, the interval during which ϕ_1 is high has been split into two sub-intervals: the tracking interval (when ϕ_4 is high) and the self-settling interval (when ϕ_3 is low). The circuit configurations during tracking and

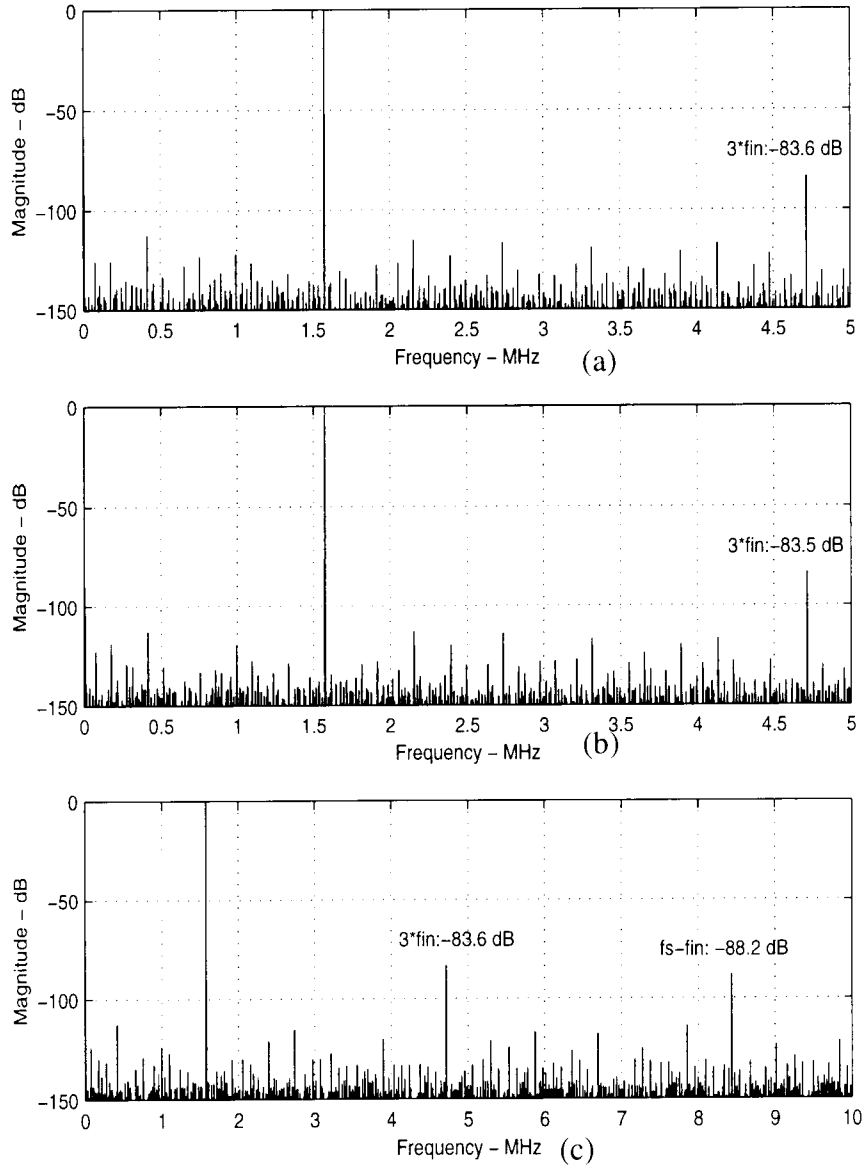


Figure 3.12:Signal spectra: (a) T/H A output; (b) T/H B output; (c) "ping-pong" output.

holding are identical to the circuit of Figure 3.7, and the circuit configuration during the self-settling clock phase is shown in Figure 3.9c. By disconnecting the circuit from continuously changing input signal, the op-amp settles at dc, and thus the input-referred error at the op-amp input node is now sampled on C_{store} when the op-amp operates with a constant input.

The circuit of Figure 3.9 can also be readily converted into a fully-differential structure as shown in Figure 3.10. HSPICE simulations of a ping-pong S/H stage (Figure 3.4) using the circuit of Figure 3.10 were performed using an OTA behavioral macro model and MOS switches modeled for the MOSIS 1.0 μm process. The computed time-domain responses with a signal frequency of 1.57 MHz and an effective sampling rate of 20 Msample / s are shown in Figure 3.11 and the spectra of the output signals are shown in Figure 3.12. The parameters assumed were asymmetric for the two paths of the ping-pong structure: an OTA dc gain = 60 dB, V_{os} = 5 mV, Gm = 1 mA/V for path A and an OTA dc gain = 58 dB, V_{os} = -5 mV, Gm = 1.5 mA/V for path B. Notice that the inter-modulation product at $f_s / 2 - f_{in}$ caused by channel mismatches is negligible even though the assumed parameters for the op-amps of the two channels were badly matched. This verifies that the new track-and-hold circuits are suitable for the realization of practical time-interleaving systems.

3.1.3. Other Error Sources in T/H Circuits

It should be pointed out that in addition to the nonidealities of the op-amp and the capacitor nonlinearity, there are also some other important error sources affecting the accuracy of a T/H stage, such as sampling clock-jitter and switch charge injection.

The sampling clock jitter is also sometimes called aperture jitter. Consider a sinusoidal wave $v_{in} = A \sin(2 \pi f_{in} t)$ sampled at $t = k T_s + \varepsilon$, where ε is the aperture jitter,

the error in each sample is approximately $\varepsilon \cdot dv_{in}/dt = \varepsilon \cdot 2\pi \cdot f_{in} \cdot A\cos(2\pi f_{in}t)$. Assuming that ε is a random jitter noise with its mean squared value of ε_{rms}^2, the maximum signal to noise ratio (SNR) limited by aperture jitter can be found as

$$SNR = -20\log(2\pi f_{in}\varepsilon_{rms})\,\text{dB}. \tag{3.9}$$

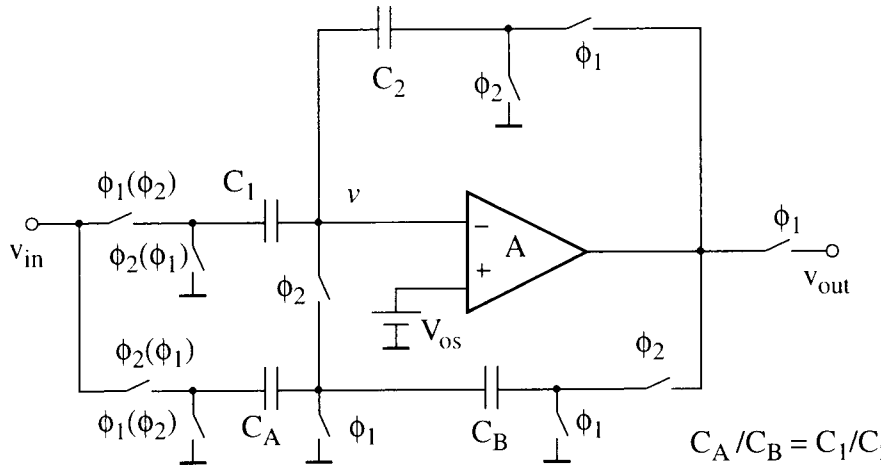
For f_{in} = 10 MHz, ε_{rms} needs to be kept smaller than 160 picoseconds in order to achieve better than 80 dB SNR.

If the sampling clock jitter is a constant, it causes an aperture delay. A constant aperture delay is usually harmless for a S/H stage. However, in a parallel system, such as the ping-pong structure of Figure 3.4, the mismatch of the aperture delays between channels will result in signal intermodulation. Consider the "ping-pong" structure of Figure 3.4 with an aperture delay mismatch of δ. The resulting signal can be viewed as the sum of an undistorted signal $[v_{in}(t) + v_{in}(t+\delta)]/2$ and a signal $[v_{in}(t) - v_{in}(t+\delta)]/2$ modulated by f_s, or multiplied by $(-1)^n$. The resulting output spectrum then consists of a fundamental tone $A\cos(\pi f_{in}\delta) \cdot \cos[2\pi f_{in}(t + \delta/2)]$ and two intermodulation tones at $f_s \pm f_{in}$ with amplitudes of $\sin(\pi f_{in}\delta)$.

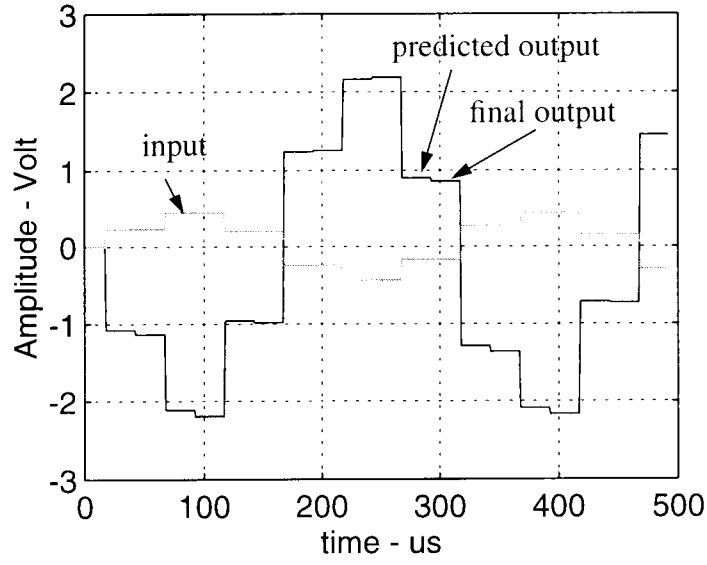
Clock injection noise is another major limiting factor in high-speed high accuracy switched-capacitor circuits. In a given technology, the trade-off between the charge-injection noise and the speed of the circuit results in switch sizes optimized for a certain range of clock and signal frequencies. While techniques like using a fully-differential structure and delayed cut-off clock-phases greatly reduce the signal-dependent charge injection, the signal-independent charge injection does appear in the output as a constant offset. The mismatch of such constant offsets (together with the op-amps' residual offsets) will cause a fixed tone at f_s in the output of the "ping-pong" structure, and sometimes digital calibration is needed to remove this tone.

3.2 Predictive Gain- and Offset-Compensated SC Amplifiers

The gain- and offset-compensated SC amplifier in Figure 2.5a reduces the finite op-amp gain effect at low frequencies only. To extend the compensation to higher frequencies,



(a)



(b)

Figure 3.13:The Larson-Temes wideband GOC SC amplifier. a: the circuit; b: the input and output signal waveforms.

predictive correlated-double-sampling techniques can be incorporated in the circuits. Figure 3.13 shows [21] a wide-band gain- and offset-compensated SC amplifier using two signal paths, one is the prediction path which consists of C_A and C_B, and the other one is the main path for compensated signal amplification, which consists of C_1 and C_2. When ϕ_2 is high, v_{in} gets amplified through the prediction path and the op-amp output becomes

$$v_{out}\left(n-\frac{1}{2}\right) \approx \frac{-C_1/C_2}{1+(1+C_1/C_2)/A} \cdot v_{in}(n) + V_{os} \cdot (1+C_1/C_2)\,. \tag{3.10}$$

Meanwhile, C_1 samples the error voltage $V_{os} - v_{out}(n-1/2)/A$ at the op-amp input node. Next, when ϕ_1 goes high, v_{in} is amplified through the main signal path and the input error voltage of the op-amp is subtracted. Because $v_{out}(n-1/2) \approx v_{out}(n)$, the op-amp offset and finite gain effect is then compensated. More exact analysis show that the amplifier response at dc is

$$v_{out} \approx \frac{-C_1/C_2}{1+(1+C_1/C_2)^2/A^2} \cdot v_{in}(n) + V_{os} \cdot \frac{(1+C_1/C_2)}{A}\,. \tag{3.11}$$

Compared with Eq. (2.6), the error term in the denominator is now larger by a factor of

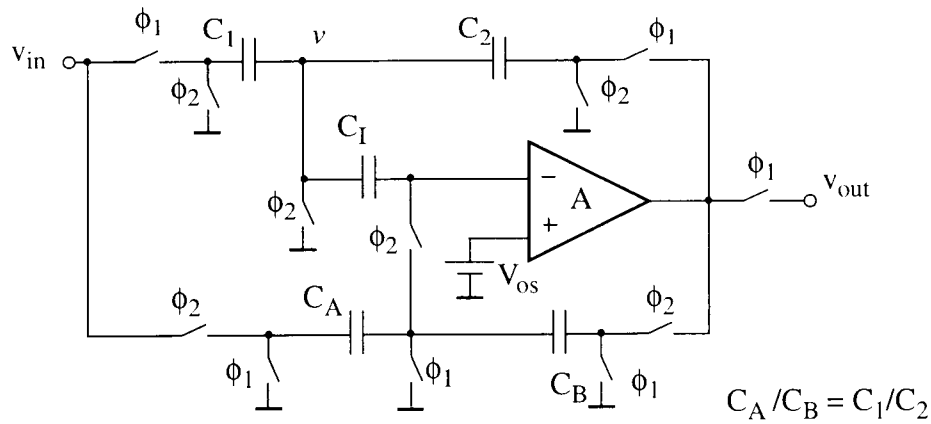
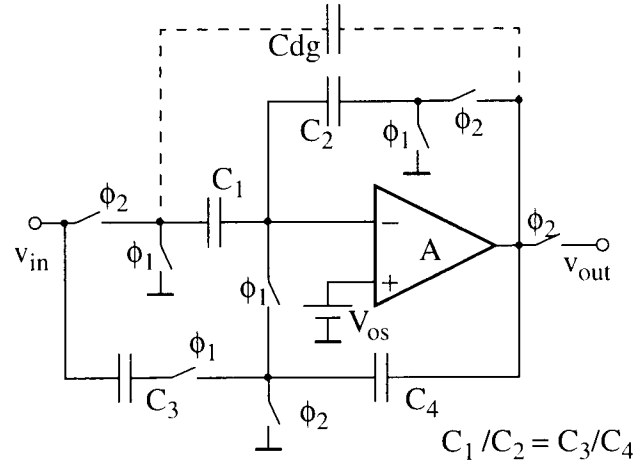


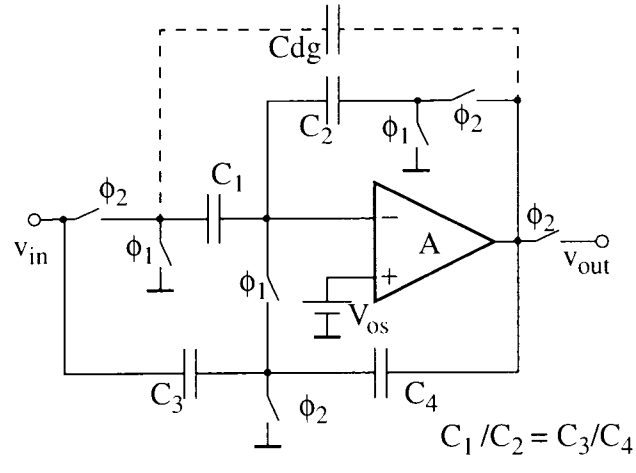
Figure 3.14:Nagaraj wideband OGC SC amplifier.

$1 + C_1 / C_2$. The comparison of gain-error versus signal frequency for various SC amplifiers is given in Figure 3.16.

Applying the principle of the T/H circuit in Figure 3.7, an error storage capacitor can be used in yet another predictive gain- and offset-compensated amplifier as shown in



(a)



(b)

Figure 3.15:a: Improved predictive SC amplifiers. b: simplified circuit without the disconnecting switch.

Figure 3.14. This circuit is the same as the one proposed by Nagaraj in [22]. The corresponding gain-error vs. signal frequency is also shown in Figure 3.16.

Figure 3.15a shows another proposed novel predictive OGC SC amplifier. It is somewhat similar to the circuit in Figure 3.13; however, three of the switches have been eliminated, and (as will be shown) the performance much improved. It is assumed that $C_1/C_2 = C_3/C_4$, and that v_{in} is a sampled-and-held signal which changes only when ϕ_1 goes high. The output is valid when $\phi_2 = 1$. When $\phi_1 = 1$, C_4 acts as feedback capacitor, and C_3 adds a charge proportional to the change in v_{in} to the charge stored in C_4, thus updating v_{out} to its next predicted value. The resulting new virtual-ground voltage of the op-amp is stored in the signal-processing capacitors C_1 and C_2. When the next clock phase ϕ_2 goes high, C_1 and C_2 form the signal path around the op-amp, and the new v_{out} is generated.

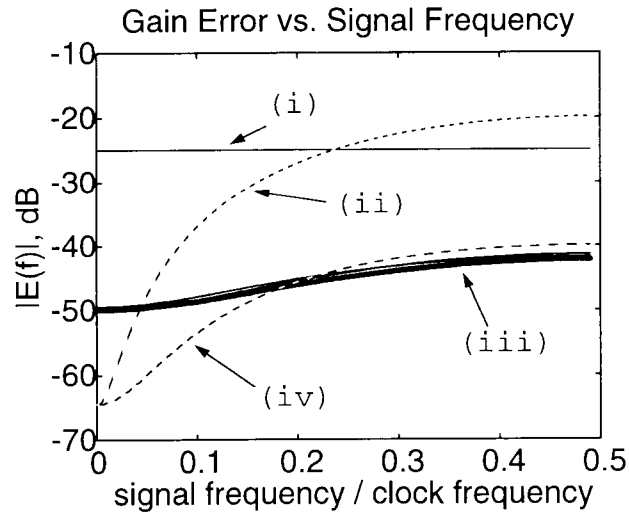


Figure 3.16:Gain error of SC amplifiers with $A_{closed\text{-}loop} = 5$, $A_{opamp} = 40$ dB;(i): uncompensated; (ii) narrowband compensated Figure 2.5; (iii) wideband compensated (Figure 3.13, Figure 3.14 and Figure 3.15b; (iv) circuit of Figure 3.15a.

The sole function of the small capacitor C_{dg} is to maintain a closed loop around the op-amp [20] during the non-overlapping interval between ϕ_1 and ϕ_2.

The circuit of Figure 3.15a can be further simplified by leaving out the switch in series with C_3 (Figure 3.15b) [33]. Now C_3 is recharged during both clock phases, but otherwise the operation of the circuit remains unchanged. The performance is slightly degraded; it becomes comparable to that of the circuit introduced in Figure 3.13 and Figure 3.14.

One of the advantages of circuits using CDS is that they become less sensitive to op-amp imperfections such as the finite dc gain A_{dc}, which results in smaller finite-gain error. For SC amplifiers, the stage gain under ideal conditions is $H = -C_1/C_2$, independent of frequency and op-amp gain. For practical circuits, H can be written in the form

$$H \cong -(C_1/C_2)(1-e) \tag{3.12}$$

Here, e is the relative gain error. For the basic stage of Figure 2.3, $e \cong (1 + C_1/C_2)/A_{dc}$, where A_{dc} is the dc gain of the op-amp. For the narrow-band CDS stage of Figure 2.5, e is very small at dc: $e_{dc} \cong (1 + C_1/C_2)/A_{dc}^2$. This is much smaller than for the basic stage since $A_{dc} \gg 1$. However, e rises rapidly with frequency. For the wide-band predictive circuits in Figure 3.13 and Figure 3.14, e is nearly independent of frequency, and its value is $e_{dc} \cong (1 + C_1/C_2)^2/A_{dc}^2$. Thus, the dc gain error is somewhat larger than for the narrow-band stage, but it remains low at all frequencies.

For the circuit of Figure 3.15a, the gain error at dc is as low as for the narrow-band CDS stage, and it rises much more slowly, while for the circuit of Figure 3.15, e behaves the same way as for the wide-band CDS circuits of Figure 3.13 and Figure 3.14. A comparison of the gain error vs. frequency responses for various CDS amplifiers is shown in Figure 3.16, and a comparison of harmonic distortion suppression is given in Sec. 3.4.

3.3 Predictive Gain- and Offset-Compensated Integrators

Applying the concepts of the T/H circuit in Figure 3.7 and of the SC amplifier circuit in Figure 3.14, a predictive gain- and offset-compensated integrator can also be constructed using an error storage capacitor [23] as shown in Figure 3.17. It also has a predictive path and a main signal path. When the clock phases outside the parenthesis are used, the circuit functions as an inverting integrator. The input signal is assumed to be sampled and held, and changes only when ϕ_2 goes high. When the clock phases inside the parenthesis are used, the circuit becomes a noninverting integrator with one clock period delay. Now the input is assumed to be sampled and held which changes only when ϕ_1 goes high. The circuit functions in a similar way to the SC amplifier in Figure 3.14. During the prediction phase, the anticipated output is obtained and the input referred error voltage is sampled on capacitor C_h, and an improved virtual ground is created at node A. Next, when the main signal path is restored, a charge $\pm(v_{in} \cdot C_1)$ enters the integration capacitor C_2 via the improved virtual ground. Thus, the inaccuracy of the integration operation comes only

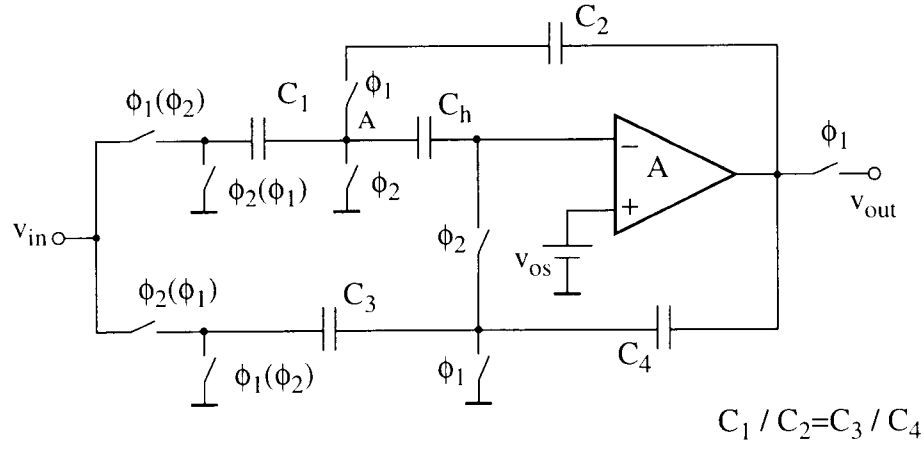


Figure 3.17:Predictive gain- and offset-compensated integrator

from the slight voltage difference between the improved virtual ground and the real analog ground, which is equal to the difference between the predictive output and the integration output being referred back to the op-amp input. Hence, this error is second-order small, as a result of the gain-compensation.

The requirement of a sample-and-held input for the predictive GOC integrator may impose some constraints on its applications; nevertheless, in oversampling data converters (one of the most important applications of GOC integrators), such a requirement may be inherently met. For a delta-sigma DAC, the unfiltered analog output is sampled-and-held by structure, and it is the input of the integrator in the following post filter. For a delta-sigma ADC, the DAC feedback is a sampled-and-held signal and the signal input can be viewed as a good approximation of a sampled-and-held signal for a large oversampling ratio.

3.4 Reduced Nonlinear Harmonic Distortion in Predictive CDS Circuits

Besides reducing the op-amp's input-referred low-frequency noise and the gain error (and/or pole error) caused by the finite op-amp gain, gain-compensating CDS circuits also provide suppression of the harmonic distortion resulting from the op-amp nonlinear gain characteristics. This principle was briefly discussed in Sec. 2.5. In this Section, various predictive CDS circuits are compared along with some non-predictive ones in terms of harmonic distortion reduction.

Recalling the analysis of the nonlinear op-amp distortion in Sec. 2.5, the reduction of harmonic distortion is achieved by minimizing the error term $v_e = v(n) - v(n\text{-}1/2)$ in Eq. (2.8). We next consider the magnitude of this error term and the resulting harmonic distortion in SC amplifiers using various CDS schemes. (The results for SC amplifiers can be extended to SC integrators, as will be shown later.)

We again assume that the nonlinear op-amp input/output relation can be written as $v_o = f(v_i - V_{os})$, and that the circuits are considered only under their static conditions. Hence, the voltage at the op-amp input terminal is

$$v = V_{os} + f^{-1}[v_{out}]. \tag{3.13}$$

For the uncompensated SC amplifier of Figure 2.3, $v(n-1/2) = 0$, and the error term is given by

$$v_e(n) = v(n) - v\left(n - \frac{1}{2}\right) = V_{os} + f^{-1}[v_{out}(n)]. \tag{3.14}$$

Since $f(v)$ is a nonlinear function of v, Eq. (3.14) represents a large nonlinear output error, resulting a total harmonic distortion which may only be 40 ~ 60 dB below the signal level, depending on the close-loop gain C_1/C_2 and the open-loop gain characteristic $f(v)$.

For circuits incorporating correlated double sampling (Figures 2.4, 2.5, and 3.13 – 3.15), the error term can be written as

$$v_e(n) = f^{-1}[v_{out}(n)] - f^{-1}[v_{out}(n - 1/2)]. \tag{3.15}$$

Note that in circuits using an error storage capacitor such as Figure 3.14, $v(n-1/2) = 0$, while $v(n) = f^{-1}[v_{out}(n)] - f^{-1}[v_{out}(n - 1/2)]$. Hence, Eq. (3.15) gives the error term for such circuits as well.

The main difference between these CDS gain stages lies in the value of the preset voltage $v(n - 1/2)$ which they generate. By Eq. (2.11) in Sec. 2.5, the closer $v_{out}(n)$ is to $v_{out}(n - 1/2)$, the smaller the charge transfer error and the nonlinear term will be. For the simplest offset-compensated SC amplifier shown in Figure 2.3, the error term is given by

$$v_e(n) = f^{-1}[v_{out}(n)] - f^{-1}(V_{os}) \tag{3.16}$$

Here, $f^{-1}(V_{os})$ is very small (typically, less than 100 μv) and has a constant value.

However, the first term of $v_e(n)$ in Eq. (3.16) indicate a typically large nonlinear output error of the same order of magnitude as that of the uncompensated circuit.

In the GOC stage of Figure 2.5 [14], $v_{out}(n-1/2) \approx v_{out}(n-1)$ holds. Hence, for low-frequency signals where $v_{out}(n) \approx v_{out}(n-1)$ is valid, $v_e(n)$ will be small, and the effect of op-amp nonidealities is reduced. Unfortunately, the harmonics generated by the nonlinear $f[v_i]$ characteristic represent a wide-band noise, and the high-frequency noise components are actually amplified by the high-pass noise transfer function as shown by the relation valid for this stage:

$$v_e = (1 + C_1/C_2)\{f^{-1}[v_{out}(n)] - f^{-1}[v_{out}(n-1)]\} \tag{3.17}$$

Thus, this circuit (which is generally very useful for reducing finite op-amp gain effects) does not represent a good choice for linearizing the operation of SC circuits.

The circuits shown in Figure 3.13 – 3.15 anticipate the value of $v_{out}(n)$ by performing similar switching operations at the $\phi_2 \rightarrow 1$ and $\phi_1 \rightarrow 1$ time instants to achieve $v_{out}(n-1/2) \approx v_{out}(n)$. To make this possible, $v_{in}(n)$ must be sampled-and-held signal which changes only when $\phi_2 \rightarrow 1$.

A simple but lengthy derivation, which assumes that the differential open-loop op-amp gain $|A_{dc}| = |df[v_i]/dv_i|$ is much larger than the closed-loop stage gain C_1/C_2, shows that the output error is given by

$$v_e(n) \cong -\frac{(1 + C_1/C_2)^2}{A_{dc}} f^{-1}[v_{out}(n)] \tag{3.18}$$

This error is frequency-independent and (for usual values of C_1/C_2 and A_{dc}) much smaller than v_{out}. Hence, the wideband predictive GOC circuits of Figure 3.13 – 3.15 can provide good suppression of harmonic distortion at all frequencies.

To verify the theoretical and heuristic results given above, various SC amplifiers were simulated using HSPICE. The nonlinear op-amp gain characteristic assumed is the same as in Figure 2.9. It is a piece-wise-linear curve; its slope, the differential gain A_d, varies between 30 dB and 54 dB for $|v_i| < 12$ mV. In the simulations, a stage gain $C_1/C_2 = 2$ and an input offset voltage $V_{os} = 5$ mV were assumed. The circuits were realized in fully differential configurations and were analyzed in the time domain with sine-wave input signals of different amplitudes and frequencies. A typical set of spectra of the output voltages, giving also the computed S/THD ratios, is shown in Figure 3.18 and Figure 3.19. Table 3.1 illustrates the magnitude of the THD as well as the second and third signal

Table 3.1: Harmonic distortion comparison for various SC amplifiers

Circuit configuration	THD (dB)	HD2 (dB)	HD3 (dB)
uncompensated (Figure 2.3)	-63.1	-85.9	-64
offset-compensated (Figure 2.4)	-63.1	-102	-64
narrow-band GOC (Figure 2.5)	-70.6	-95.2	-73.2
wide-band GOC (Figure 3.13)	-81.7	-86.2	-85.8
wide-band GOC (Figure 3.14)	-81.7	-86.2	-85.9
wide-band GOC (Figure 3.15b)	-81.4	-86.0	-85.6
wide-band GOC (Figure 3.15a)	-89.8	-95.3	-93.7

harmonics for the SC gain stages obtained from the simulation. The conclusions which can be draw from the simulation results are the following:

1. The output spectrum of the uncompensated stage of Figure 2.3 exhibits large odd- and even-order harmonics, the latter due to the shift of the output bias caused by the $(1+C_1/C_2)V_{os}$ = 15 mV offset term in v_{out}.

2. The output signal of the offset-compensated circuit of Figure 2.4 contains large odd-order harmonics spurs, as could be predicted from the previous discussions. However, even-order harmonics are suppressed along with the dc offset.

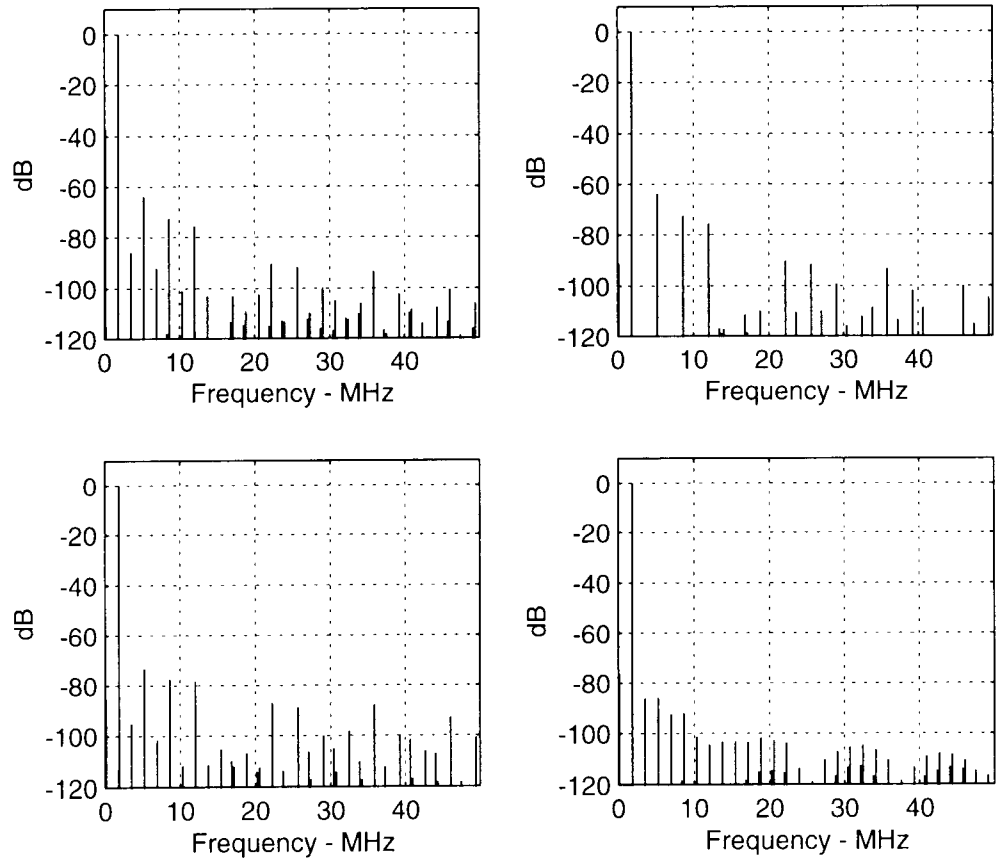


Figure 3.18:Simulated SC amplifier output spectra. a: uncompensated (Figure 2.3); b: offset-compensated (Figure 2.4); c: narrow-band compensated (Figure 2.5); d: wideband compensated (Figure 3.13).

3. The harmonic distortion in the output signal of the narrow-band compensated stage of Figure 2.5 is slightly reduced at low frequencies but enhanced at higher ones, again as predicted by the theoretical analysis given in the preceding section.

4. The distortion spectra of the output signals of the two wideband compensated circuits of Figure 3.13 , 3.14 and Figure 3.15b are nearly identical, as the theory predicts, and the harmonic components are reduced over the complete frequency range $0 - f_S/2$ compared to the other stages. The S/THD ratio is more than 10 dB higher than for the

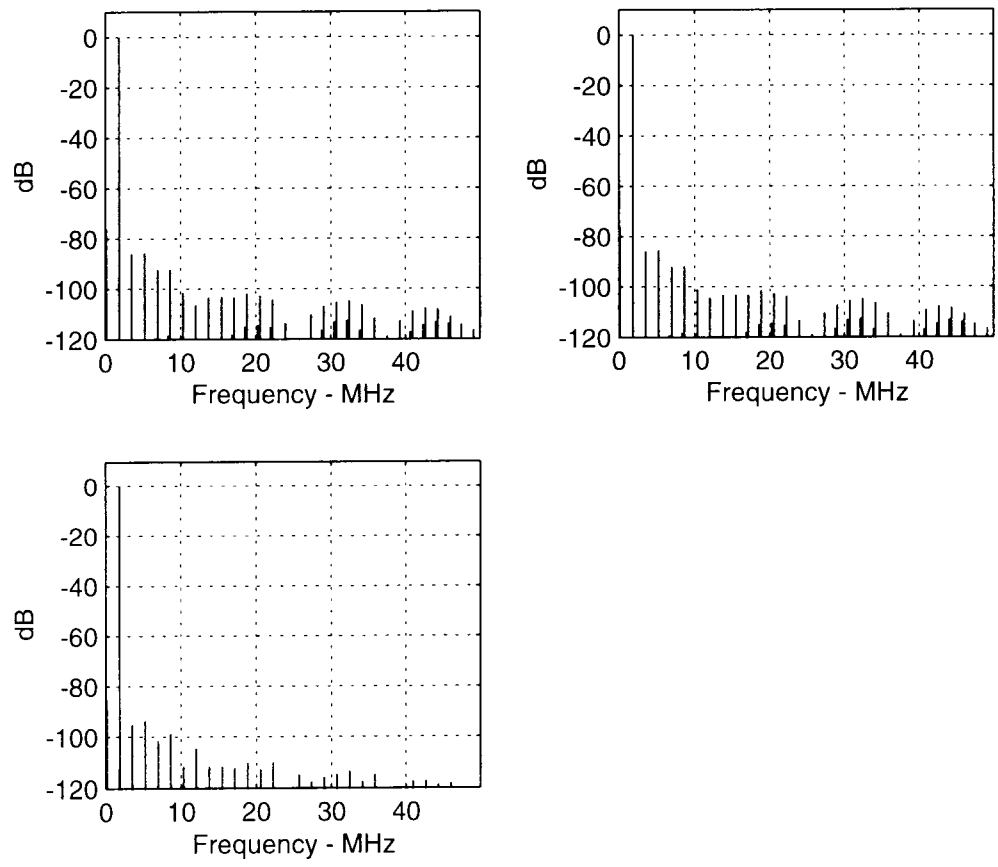


Figure 3.19:Simulated SC amplifier output spectrum. a: wideband compensated circuit using an offset storage capacitor (Figure 3.14); b: proposed novel SC amplifier (Figure 3.15b); c: proposed novel SC amplifier (Figure 3.15a).

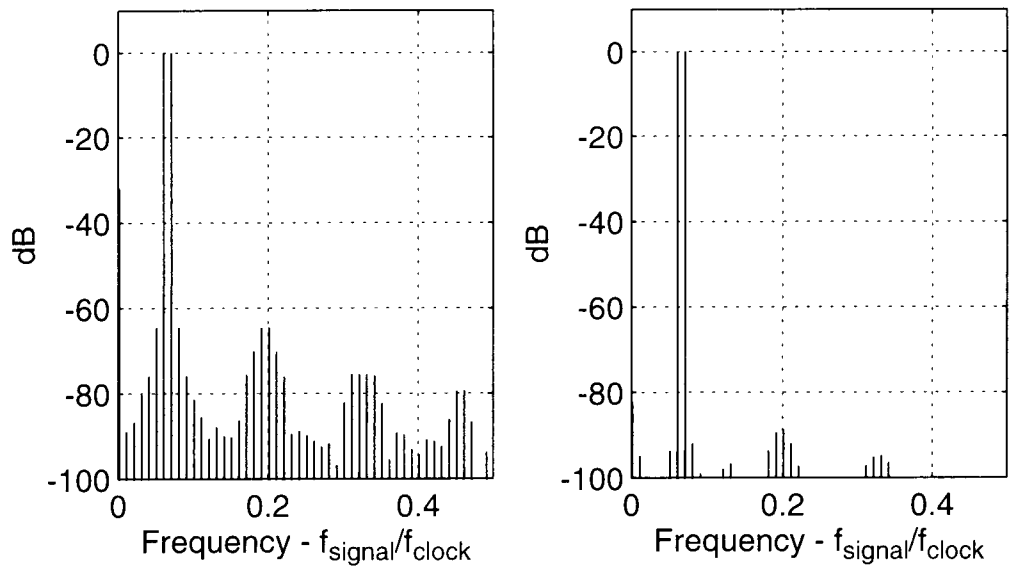


Figure 3.20:Output spectra with a two-tone input. a: the uncompensated SC amplifier; b: wideband GOC SC amplifier in Figure 3.15a.

narrow-band compensated circuit of Figure 2.5 and nearly 20 dB higher than for the stages of Figure 2.3 and Figure 2.4. The proposed circuit of Figure 3.15a has yet 10 dB higher S/THD than any of the existing circuits.

Offset-compensated SC stages reduce the effects of the input-referred op-amp dc offset voltage V_{os} by making the signal charge transfer nearly independent of V_{os}. Gain- and offset-compensated (GOC) SC circuits reduce also the effect of the finite op-amp gain on the signal transmission, by reducing the effect of the nonzero op-amp input voltage v_i on the charge transfer. The cancellation of the v_i effect is highly frequency-dependent in narrow-band GOC stages, such as the one shown in Figure 2.5; it is nearly frequency independent in wide-band GOC circuits such as those illustrated in Figure 3.13 – 3.15.

It should also be pointed out, that the intermodulation distortion for a two-tone input caused by the op-amp gain nonlinearity is reduced in the same manner as for single-tone signal harmonic distortion. Figure 3.20 shows the simulated output spectra with two-tone sine-wave inputs.

So far, we have looked at the harmonic distortion reduction achieved by employing predictive CDS schemes in SC amplifiers. However, from the mechanism of such operation, it can be anticipated that such harmonic suppression can also be achieved in predictive gain- and offset-compensated T/H stages, SC integrators and other precision SC circuits.

3.5 Conclusions

By anticipating the output of the next clock phase, predictive CDS circuits provide reduced sensitivity to finite op-amp gain over a wide signal frequency range. As a result, the gain error and pole error can be reduced. Also, the nonlinear harmonic distortion can be greatly suppressed. The difference in the harmonic distortion reduction performance of the CDS circuits is due to the difference in the residual error voltage v_e. The smaller the v_e is, the smaller the nonlinear distortion will be. The same argument is true for the gain error in SC amplifiers and the pole error in SC integrators. Thus, one should not be surprised to find the gain error vs. frequency response is somewhat similar to the harmonic distortion response.

Chapter 4. Design of High-Linearity SC Circuits without Using High-Linearity Capacitors

In the last two chapters, one major source of harmonic distortion in SC circuits, the op-amp nonlinear voltage transfer characteristics, was discussed, and techniques for reducing its effect were proposed. Another major source of harmonic distortion in SC circuits is the capacitor nonlinearity, especially in a basic digital CMOS process, where the capacitors are implemented using MOSFETs. In this chapter, the effect of capacitor nonlinearity in SC circuits is analyzed and techniques for reducing those effects are presented.

4.1 The Effect of Capacitor Nonlinearity in SC Circuits

In SC circuits, the signal is processed as charges being converted from and to voltages. The accurate conversion between voltages and charges is achieved by the capacitors used in the circuits. However, the capacitance of a practically implemented capacitor often exhibits some degree of voltage dependence [7][9], due to the space-charge capacitance generated in the electrodes. This problem is especially severe for MOSFET capacitor realizations, whose capacitance typically has a voltage dependence as large as 40 kppm/V [24][25] even when they are biased in their strong inversion or accumulation region. Next, we shall discuss how this nonlinearity affects the overall SC circuit performance.

Consider the SC biquad in Fig. 4.1. The circuit elements can be partitioned into three functional groups: voltage-to-charge ($V-Q$) converters, charge adders, and charge-to-voltage ($Q-V$) converters. The $V-Q$ converter group, whose function in the circuit is to convert signal voltages into charge flows with appropriate scaling factors, includes the capacitive branches containing C_1, C_2, C_3 and C_4. The charge adder, whose function is to

sum all the converted charges, includes integration capacitors C_A, C_B and op-amps op1 and op2. The $Q-V$ converter, whose function is to convert the signal processed in the charge domain back into voltages, includes C_A and C_B. It can be seen that the accuracy of the charge summation is affected only by the op-amp nonidealities, while the accuracy of $V-Q$ and $Q-V$ conversions is directly affected by the capacitors' voltage dependence, i.e., capacitor nonlinearity.

Let's first study the capacitor nonlinearity effect on $V-Q$ conversion. Let the small-signal capacitance $C = dq/dv$, be a function of the voltage v between the two terminals, denoted as $C = c_0 \cdot f(v) = C(v)$. By definition, when v changes from 0 to v_{in}, the amount of charge q delivered into the capacitor is

$$q = \int_0^{v_{in}} C(v)dv. \tag{4.1}$$

Assume

$$C(v) = c_0(1 + \alpha_1 v + \alpha_2 v^2), \tag{4.2}$$

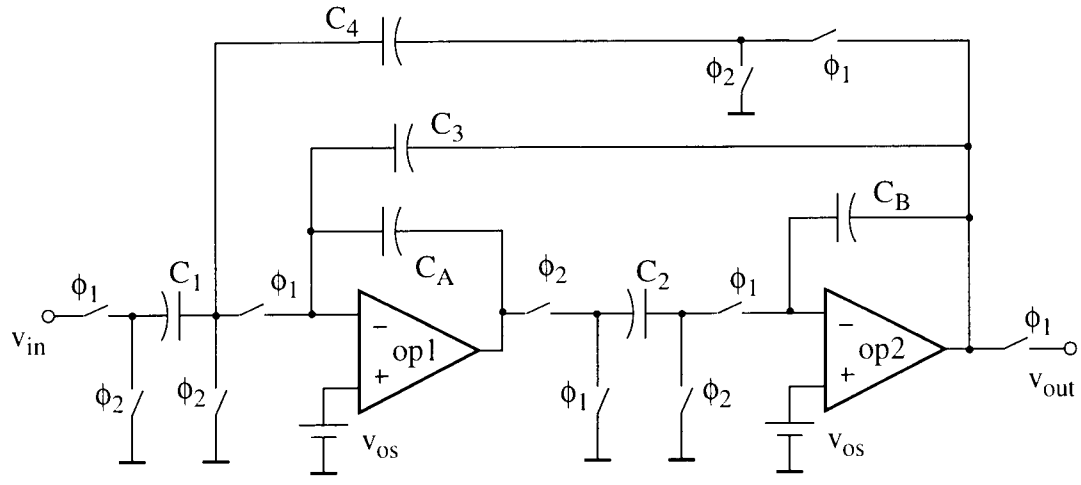


Figure 4.1: An SC biquad.

then we have

$$q = c_0\left(v_{in} + \frac{1}{2}\alpha_1 v_{in}^2 + \frac{1}{3}\alpha_2 v_{in}^3\right). \tag{4.3}$$

For a sinusoidal input signal $v_{in} = V_m\sin(\omega t)$, the magnitude of the second-order harmonic distortion introduced by this nonlinearity is given by

$$HD_2 \cong \frac{V_m^2 \cdot \alpha_1}{4}, \tag{4.4}$$

and the third-order harmonic distortion is given by

$$HD_3 \cong \frac{V_m^3 \cdot \alpha_2}{12}. \tag{4.5}$$

Eqs. (4.4) and (4.5) indicate that the second-order harmonic distortion is proportional to $V_m{}^2$ while the third-order is proportional to $V_m{}^3$. In a fully-differential structure, the dominant harmonic is usually the third-order harmonic; hence, the S/THD is inversely proportional to $V_m{}^2$.

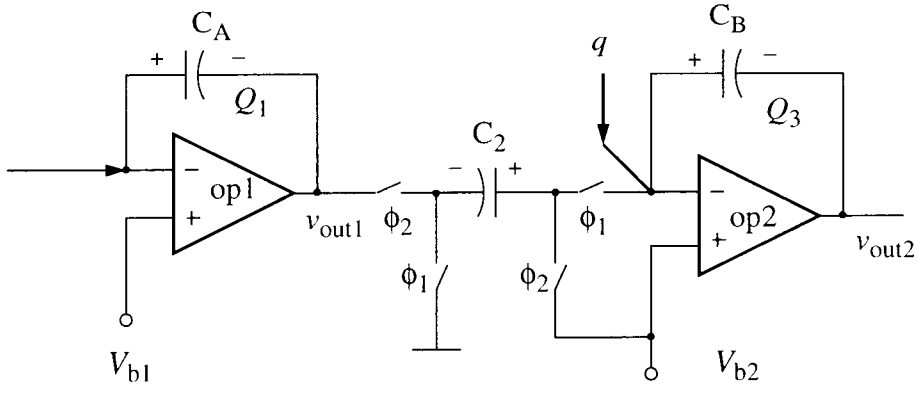


Figure 4.2: Switched-capacitor inter-stage signal coupling.

Next, we shall study the capacitor nonlinearity effect on the inter-stage signal coupling (Figure 4.2). In order to transfer the charge stored in C_A into C_B with a scaling factor, C_2 is used to sample the output voltage of the first stage op-amp during ϕ_2, and discharges into C_B during ϕ_1. Assume the op-amps and switches are ideal, and the capacitances are $C_i = c_i f_i(v)$, $i = A, 2, B$. The charges stored on C_A and C_2 are then given by

$$Q_A = \int_{v_{out1}}^{V_{b1}} c_A \cdot f_A(v)dv, \text{ and } Q_2 = \int_{v_{out1}}^{V_{b2}} c_2 \cdot f_2(v)dv. \tag{4.6}$$

If capacitors C_A and C_2 have the same nonlinearity, i.e., $f_A(v) = f_2(v)$, and $V_{b1} = V_{b2}$, the relationship between Q_A and Q_2 becomes

$$Q_A / Q_2 = c_A / c_2. \tag{4.7}$$

This shows that the inter-stage charge transfer linearity is not affected by the capacitor nonlinearity, as long as C_A and C_2 have the same voltage dependence and the same bias voltages.

For the capacitor nonlinearity effects on the $Q - V$ conversion, it is difficult to derive an analytical expression, and simulations are often used to address this issue. However, in most SC circuits, only the linearity of the very last stage's $Q - V$ conversion is crucial; hence, special care needs to be taken only for the integration capacitor of that stage. This point will be further illustrated in the MOSFET filter example in Sec. 4.6.3. Note that in a single-bit delta-sigma modulator, such nonlinearity in the last stage integrator does not affect the overall linearity as long as the $Q(v)$ characteristic of the last capacitor is monotonic.

4.2 Reducing the Capacitor Nonlinearity Using the Series Capacitor Branch

From Eqs. (4.4) and (4.5), the harmonic distortion increases with the voltage swing across the nonlinear capacitors. For the same signal magnitude, having several capacitors connected in series reduces the voltage swing on each capacitor, and thus improves the

linearity drastically. Due to practical aspects, such as the nonlinear stray capacitances at the series connection node, usually not more than two capacitors can be used in a series branch. It was also proposed [4][5] that by having two capacitors with similar nonlinearity connected back-to-back (Figure 4.3) will not only decrease the voltage swing on each capacitor, but also will cancel the odd-order nonlinear terms. For the SC branch in Figure 4.3, let C_1 and C_2 be the same type of capacitor with the same size. During ϕ_1, the two capacitors C_1 and C_2 are discharged to their initial operating points where the voltages across them are V_{b1} and $V_{b1} - V_{b2}$, respectively. During ϕ_2, a signal voltage v_{in} is applied at node A, and the charge delivered to this branch is

$$q = -\int_{V_{b1}}^{(v_B - v_{in})} C_1(v)dv, \tag{4.8}$$

where V_B is the voltage at node B during ϕ_2. Since charge is conserved at node B, we also have

$$q = \int_{(V_{b1} - V_{b2})}^{(v_B - V_{b2})} C_2(v)dv \tag{4.9}$$

Adding Eq. (4.8) and Eq. (4.9) and using $C_1(v) = C_2(v) = C(v)$ yields

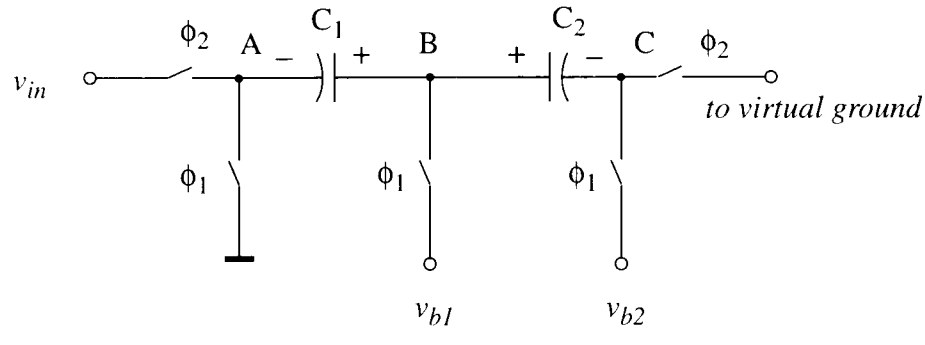


Figure 4.3: A series SC branch.

$$q = \frac{1}{2} \cdot \left[\int_{(V_{b1} - V_{b2})}^{(v_B - V_{b2})} C(v)dv - \int_{V_{b1}}^{(v_B - v_{in})} C(v)dv \right]. \tag{4.10}$$

Substituting $C(v)$ using Eq. (4.2), we get

$$q = \frac{1}{2} c_0 \left[v_{in} + \frac{1}{2}\alpha_1 \cdot \psi_1 + \frac{1}{3}\alpha_2 \cdot \psi_2 \right], \tag{4.11}$$

where

$$\psi_1 = 2v_B \cdot v_{in} - 2v_B \cdot V_{b2} - v_{in}^2 + 2V_{b1} \cdot V_{b2} , \tag{4.12}$$

$$\psi_2 = v_{in}^3 + 3v_B^2(v_{in} - V_{b2}) - 3v_B(v_{in}^2 - V_{b2}^2) + 3V_{b1}V_{b2}(V_{b1} - V_{b2}) . \tag{4.13}$$

Since $v_B \approx V_{b1} + v_{in}/2$, these two coefficients can be simplified to

$$\psi_1 \approx v_{in}(V_{b1} - V_{b2}) , \tag{4.14}$$

$$\psi_2 \approx \frac{1}{4}v_{in}^3 - \frac{3}{4}V_{b2}v_{in}^2 + \left(3V_{b1}^2 - 3V_{b1}V_{b2} + \frac{3}{2}V_{b2}^2\right). \tag{4.15}$$

Compared with Eq. (4.3), the effect of the first-order capacitor nonlinearity term $\alpha_1 {v_{in}}^2$ (responsible for the second-order signal harmonic distortion) is cancelled (when $V_{b2} = 0$), and the second-order nonlinear term $\alpha_2 {v_{in}}^3$ (responsible for the third-order signal harmonic distortion) is now reduced by approximately a factor of 4. Similar conclusion can be drawn for higher-order nonlinearities.

In Figure 4.3, the choice of different dc voltages at each node is often determined by the actual implementation, as will be further illustrated in the MOSFET implementations of Sec. 4.5 and in the 3-V all-MOSFET delta-sigma modulator design described in Chapter 5. Notice that when $V_{b2} = 0$, i.e., the two capacitors have the same initial bias voltages, the induced nonlinear term $\alpha_2 V_{b2} {v_{in}}^2$ disappears. In any case, in a fully-differential implementation, the even-order nonlinear terms containing ${v_{in}}^n$ (where $n = 2, 4, 6...$) are cancelled inherently by the differential structure, as will be shown in Sec. 4.4.

4.3 Reducing Capacitor Nonlinearity Using Parallel Compensation

In addition to the series-compensation branch, a parallel branch (Figure 4.4) can also be used reduce the capacitor nonlinearity effects [5][28]. Using the same notation as before, we find the charge stored in this composite branch

$$q = \int_{v_A}^{v_B} (C(v) + C(-v))dv. \tag{4.16}$$

Clearly, $C(v) + C(-v)$ is an even function of v, so the odd-order nonlinearities of $C(v)$ are cancelled. Thus, if V_A and V_B have the same dc potential, and an ac signal (i.e. sinusoidal signal) is applied between the two nodes of this branch, the sum of the induced charges on the two capacitors shall contain no even-order harmonics. This technique can be readily applied in very high-linearity poly-poly or poly-metal capacitor implementations and be incorporated in layout[26]. However, in a MOSFET capacitor implementation, where a dc bias is needed to keep the capacitors in their accumulation or strong inversion region [28], a more elaborate circuit is needed when using this technique, as will be shown in Sec. 4.6.

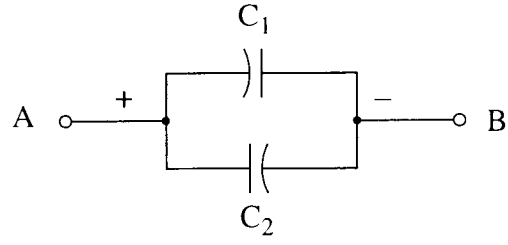


Figure 4.4: A parallel capacitor branch.

Compared with the series-compensation branch, the parallel-compensation branch needs only about one quarter of the total capacitor area to achieve the same level of kT/C noise. However, because it does not reduce the odd-order harmonic distortion, the effectiveness of parallel compensation is not as good as the series one. Also, as will be shown next, the compensation achieved by parallel connection is inherent in a fully-differential structure. These factors make the parallel technique suitable mainly for single-ended, area-limited applications.

4.4 Reduced Capacitor Nonlinearity Effect in Fully-Differential Structures

Shown in Figure 4.5 is a fully-differential SC integrator. Using the same notations for the capacitor nonlinearity as before, the differential charge entering the integration capacitor during ϕ_2 can be found to be

$$q = q_1 - q_2 = \int_{v_{in}}^{v_a} C(v)dv - \int_{-v_{in}}^{v_a} C(v)dv = \int_{v_{in}}^{-v_{in}} C(v)dv . \tag{4.17}$$

Here v_a is the voltage at the input node of the op-amp changed from the dc bias V_b during

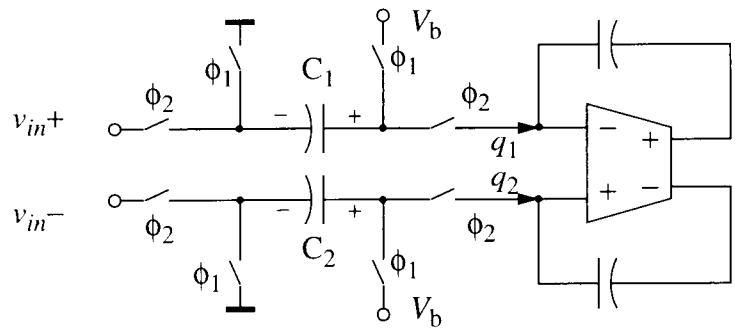


Figure 4.5: A fully-differential SC integrator.

ϕ_2. Assuming Eq. (4.2) holds for the capacitor voltage dependency yields

$$q = 2C_0\left(v_{in} + \frac{1}{3}\alpha_2 v_{in}^3\right). \tag{4.18}$$

It can be seen that the above expression does not contain any even-order powers of the input signal v_{in}. Compared with the compensation achieved in a single series SC branch with back-to-back connections, the fully differential structure does not reduce the odd-order nonlinear harmonic distortion, while the series branch suppresses it by cancellation and by reducing the signal swing on each capacitor. In actual design practice, these two techniques can be combined to further linearize the capacitors [34].

4.5 MOSFET Capacitors

In state-of-the-art devices, more and more signal processing functions are implemented after the signal has been digitized, and more and more digital functions are integrated on the same chip. Hence, most of the recent mixed-signal ICs contain a very small percentage of analog circuitry. Those analog blocks (mostly switched-capacitor circuits), nonetheless, oftentimes require linear capacitors as circuit components. In a CMOS technology, typically double-poly capacitors or metal-poly capacitors are used for realizing high-linearity capacitors, at the added cost of some extra fabrication layers. The other types of capacitor realizations (such as metal-metal) suffer from drawbacks, such as large parasitic capacitances, small unit area capacitance. So, it is very desirable to derive techniques whereby the analog circuits can be implemented in a basic digital CMOS technology.

It has been suggested by many researchers that the gate-to-channel capacitances of a MOS transistor can be used as capacitors if they are properly biased in their accumulation region or strong inversion region [3][4][5][27]. Accumulation-region operation is often preferred because the capacitance is less frequency dependent and has relatively small

voltage coefficients. Neglecting the space-charge-capacitance of the poly silicon layer, the total small-signal gate capacitance is given by

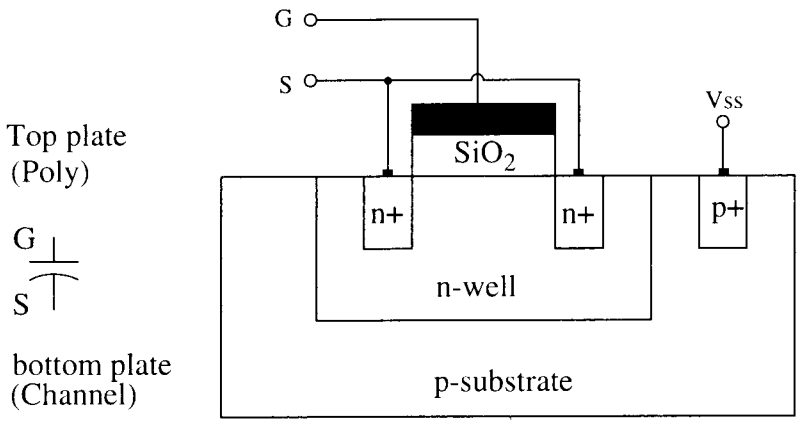
$$C_g = C_{ox} \cdot \left(1 - \frac{2\Phi_t}{|V_{gs} - V_0| + 2\Phi_t}\right) \tag{4.19}$$

where C_{ox} is the gate-oxide capacitance, Φ_t is the thermal voltage, V_{gs} is the gate-to-source voltage and V_0 is the flat-band voltage (V_{FB}) for accumulation operation or the threshold voltage (V_{TH}) for strong inversion operation [28].

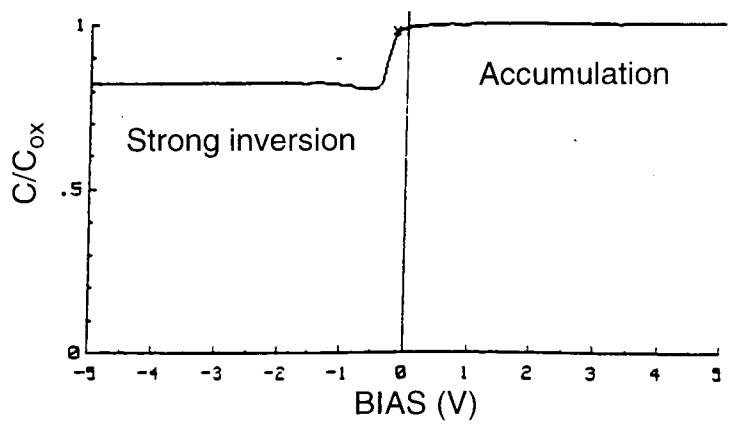
In a basic n-well CMOS process, there are four types of MOSFET capacitors available [3][28]: electron-accumulated, hole-accumulated, strong-inversion n-channel and strong inversion p-channel capacitors. Shown in Figure 4.6a is a cross section of the physical structure of a MOSFET capacitor implemented in a n-well process employing the electron-accumulated structure. This structure is favored against the other types of MOSFET capacitors because its capacitance is less frequency dependent and less voltage dependent [4][5][28] when biased properly, and it allows variable potential for both terminals. From Eq. (4.19), it can be seen that large V_{gs} is needed to bias the capacitors deeply so that their capacitances show minimal voltage dependency. Measured results (Figure 4.6b) show a first-order voltage dependence coefficient of 850-1000 ppm/V for an operating dc bias voltage between 0.5 V and 5 V when a 1 MHz 10 mV peak sinusoidal test signal was applied [28]. By Eq. (4.4), this capacitor nonlinearity corresponds to a second-order harmonic distortion of -66 dB for a 2 V_p sinusoidal signal. The HSPICE simulated small-signal low-frequency $C(v)$ curve is shown in Figure 4.6c. Note that the abrupt transition between the strong inversion region and the accumulation region is due to the imperfect MOSFET capacitor model (HSPICE level 3 model) used in the simulation.

Besides the large voltage coefficient, the MOSFET capacitor of Figure 4.6a also has a parasitic pn junction diode between the n-well and the p-substrate along with an

associated parasitic bottom-plate capacitor. Calculation shows that the parasitic capacitance is only about 10% of the total gate capacitance [28]. However, because this



(a)



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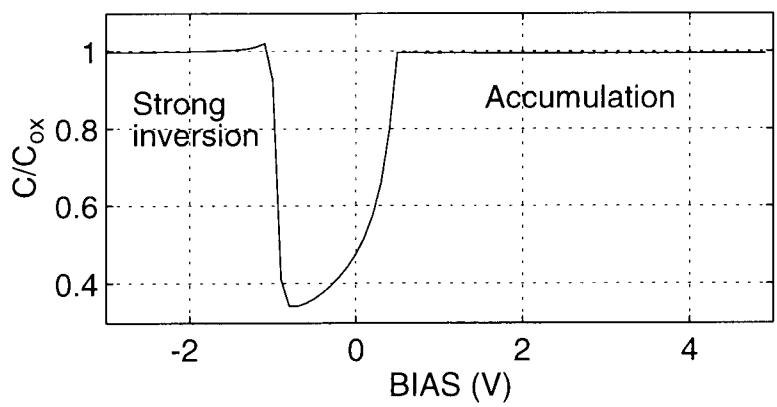


(c)

Figure 4.6: A MOSFET capacitor in n-well process. a: cross-section of the physical structure; b: measured high-frequency *c-v* curve. c: simulated low-frequency *c-v* curve.

capacitor is highly nonlinear, care should be taken in the design to avoid signal charge leaking to such parasitic capacitors.

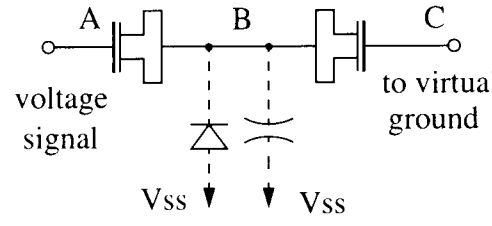
4.6 SC Circuits Using MOSFET Capacitors

As described in Sec. 4.1, in practical SC circuits only the linearity of the input capacitor of the first stage and the feedback capacitor of the very last stage affects the overall linearity, and compensation techniques need to be applied only for those capacitive branches.

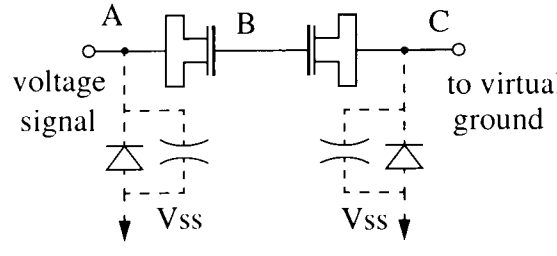
Despite disadvantages such as larger chip area and relatively high sensitivity to substrate noise, the series compensation scheme is still favored in constructing high-linearity SC circuits, because it provides the most effective compensation of the capacitor nonlinearity for a large voltage swing. Also, compared with the parallel compensation scheme, the biasing for the MOSFET capacitors in a series branch is more straightforward. Hence, in this thesis, only the series compensation technique is considered in the design of various SC circuits.

There are two possible connections for a series branch, as shown in Figure 4.7. In the bottom-to-bottom connection (Figure 4.7a), the voltage swing at nodes A, B and C needs to be arranged using proper dc biasing, so that V_{AB} , $V_{CB} > V_{accum}$ where V_{accum} is the gate-to-source voltage needed for operation in the accumulation region. A typical value of V_{accum} is around 0.5 V, and sometimes $V_{accum} = 1.2$ V is used to ensure deep accumulation operation for better linearity. In a similar way, for the top-to-top connection (Figure 4.7b), the voltages at nodes A, B and C need to be arranged so that V_{BA} , $V_{BC} > V_{accum}$. As discussed earlier, each MOSFET capacitor has a parasitic capacitor and a diode resulting from the pn junction between the n-well and the p-substrate. In Figure 4.7a, the nonlinear parasitic capacitor resides at the center node of the series connection, and thus

may cause unacceptable signal harmonic distortion resulting from the stray charge stored at this node. On the other hand, for the top-to-top connection, one of the parasitic capacitors is located at the signal input node, and it does not cause signal distortion. The other parasitic capacitor is at the op-amp input node, and it should not cause harmonic distortion either, because the signal voltage swing at that node is nearly zero. Having the bottom plate connected to the op-amp input terminal, however, makes the circuit more susceptible to substrate noise coupling, hence fully-differential structures should be used, and care should be taken in the layout to provide shielding to prevent direct noise coupling.



(a)



(b)

Figure 4.7: Series MOSFET capacitor branch. a. bottom-to-bottom connection; b. top-to-top connection.

4.6.1. SC Sample-and-Hold Stage

The S/H stage in Figure 3.1 uses the same capacitor for sampling the input voltage during tracking and providing the output voltage during holding, and thus the capacitor nonlinearity does not affect the T/H accuracy significantly. This can also be viewed as the conversions from voltage to charge and from charge to voltage happening on the same capacitor, so the capacitor nonlinearity does not change the accuracy of operation. Hence, MOSFET capacitors can be used for such T/H stage without compensation. However, the MOSFET capacitors still need to be properly biased to ensure their accumulation operation.

Figure 4.8 shows the resulting T/H circuit using MOSFET capacitors. For simplicity, only half of the fully-differential circuit is shown here. Assume that the potential of the analog ground (agd) is 0 V, and that all the other voltage potentials are referred to the analog ground. In order to ensure that capacitor C operates in its accumulation region,

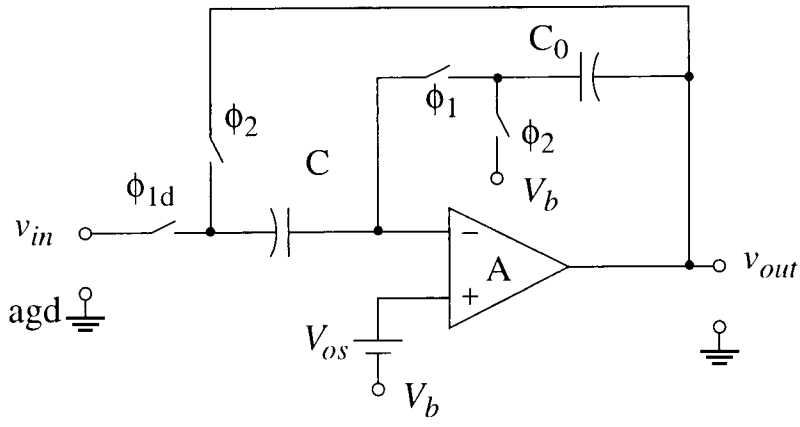


Figure 4.8: A gain- and offset-compensated T/H using MOSFET capacitors.

the dc bias voltage V_b for the op-amp input terminal needs to be greater than $V_{max} + V_{accum}$, where V_{max} is the maximum input signal magnitude, and V_{accum} is the gate-to source voltage needed for accumulation operation of the MOSFETs. This requires the op-amp to be able to operate at a high input common-mode level close to the positive rail, which can be achieved by using NMOS devices in the input pair for the op-amp.

The predictive gain- and offset-compensated T/H in Figure 3.7 can also be modified in a similar way using MOSFET capacitors. The resulting circuit is shown in Figure 4.9. To ensure accumulation operation for all capacitors, the bias conditions for the MOSFET capacitors are $V_{bp} > V_{max} + V_{accum}$ and $V_{bn} < -(V_{max} + V_{accum})$. In this circuit, although C_{store} and C_{samp} are in series with their bottom plates connected, the nonlinear

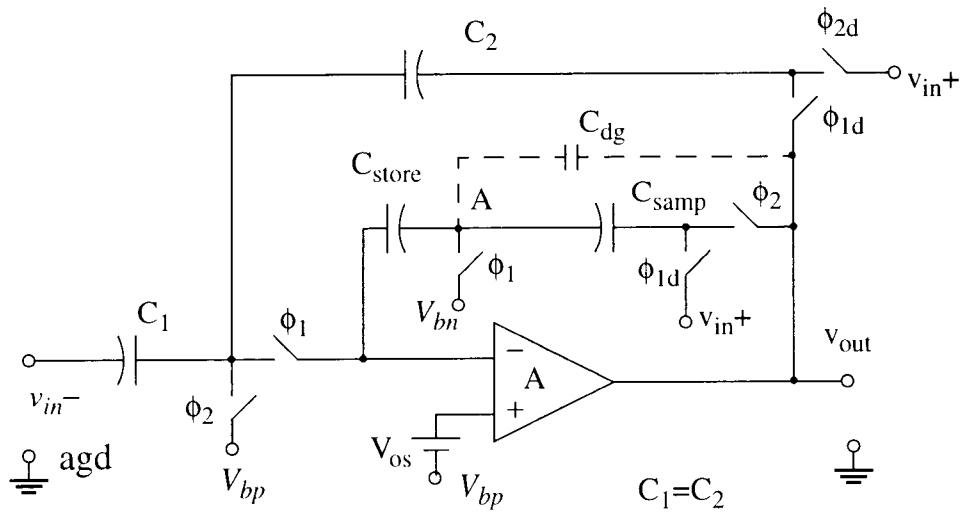


Figure 4.9: Predictive gain- and offset-compensated T/H stage using MOSFET capacitors.

parasitic capacitance at the center node *A* should not introduce much signal distortion since the voltage swing at that node is very small. The effect of common-mode voltage jump due to charge injection will be analyzed later in Chapter 7.

4.6.2. SC Gain Stages

Switched-capacitor gain stages are widely used as precision voltage amplifiers, programmable gain or AGC stages, etc. Unlike in a unity-gain sample-and-hold circuit, at least two differently scaled capacitors are used to realize the signal gain/loss from input to output. Hence, compensation techniques need to be incorporated to linearize the *V-Q* and *Q-V* conversions.

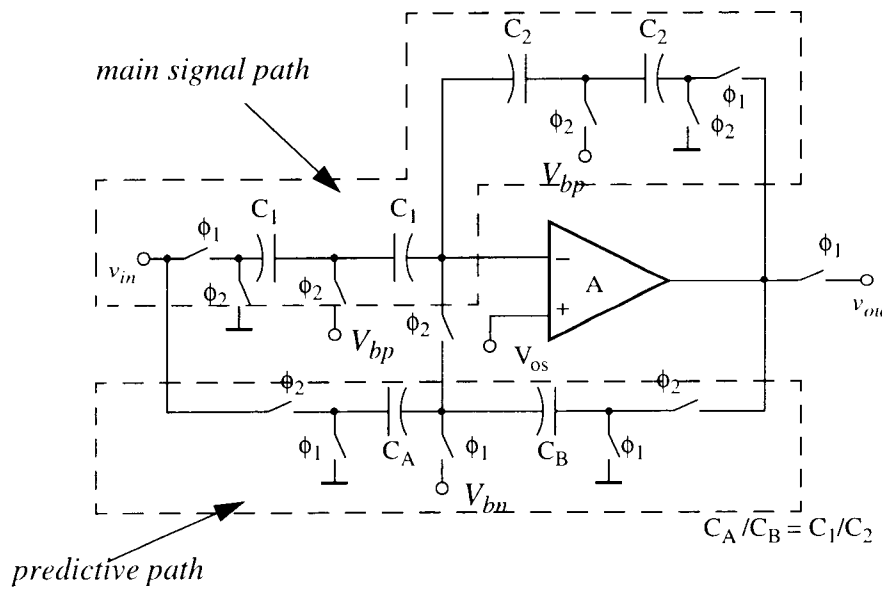


Figure 4.10:Predictive gain- and offset-compensated SC amplifier using MOSFET capacitors with series compensation.

Figure 4.10 shows an gain- and offset-compensated SC amplifier obtained from the circuit in Figure 3.13 by using series compensation technique. In order to have large signal swing at the input and the output, both the input capacitor C_1 and the feedback capacitor C_2 are implemented as series-compensated branches. It can be seen that if the stage gain is greater than unity, the feedback capacitor nonlinearity dominates, and when the stage is used as an attenuator, the input capacitor nonlinearity dominates. The dc bias condition is the same as that for the S/H circuit in Figure 4.9. Note that only simply biased MOSFET capacitors are used in the predictive signal path. This is because that any error in the output (due to op-amp error and capacitor nonlinearity) during the prediction phase will become input-referred error during the amplification phase, and is hence second-order small.

As described in Sec. 4.3, parallel capacitor branches can also be used to compensated the odd-order capacitor nonlinearity. Due to the requirement of dc bias voltages for the MOSFET capacitors, the parallel branch actually contains another two

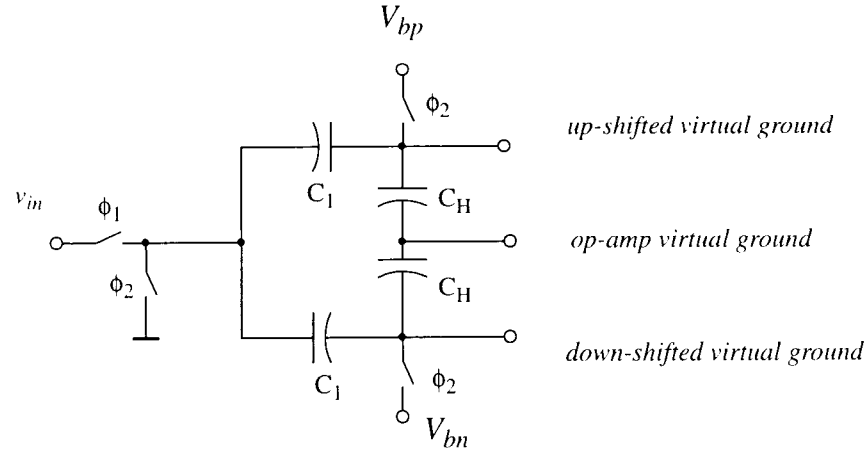


Figure 4.11:The basic MOSFET parallel compensation branch.

capacitors C_H acting as level shifters. Shown in Figure 4.11 is a basic MOSFET capacitor branch using parallel compensation. Because of its complex circuit configuration and reduced effectiveness compared with series compensation, the parallel compensation scheme in MOSFET realization will not be discussed any further in this thesis. An experimental chip with 66 dB S/THD has been reported in [28] for a predictive SC amplifier using parallel compensation.

4.6.3. SC Integrators and Filters

The SC integrator is the critical building block in many switched-capacitor circuits. Due to its high gain at low frequencies, it is always used in a circuit with some form of feedback. Depending whether the integrator is used in the first stage, in an intermediate stage or in the last stage, the linearization of the MOSFET capacitors may or may not be necessary.

Since the integration capacitor needs to able to keep the previous charges and can not be reset, it is difficult to provide a dc bias for that capacitor when it is implemented as a series-compensated branch, although it is possible for a lossy integrator. To overcome this problem, an uncompensated MOSFET capacitor is usually used for the integrator capacitor. Since the integration capacitor accumulates charges regardless its linearity, the transfer function of the integrator is not affected by the MOSFET integration in the charge domain. As will be illustrated in the following SC filter example (Figure 4.12), when such an integrator is followed by another SC block (integrator, gain stage, etc.), the capacitor nonlinearity may be completely cancelled by matching the capacitor nonlinearity of the integration capacitor and the input capacitor of the next stage; however when such an integrator is used as the last stage, a Q-V block is needed to cancel the integration capacitor's nonlinearity. This Q-V block can be part of a lossy integrator, or can be implemented as a unity-gain buffer with its feedback capacitor linearized and its input

capacitor having a nonlinearity matched to the feedback capacitor of the previous stage. When such an integrator is used in the last stage of a single-bit delta-sigma modulator, as will be shown in detail in Chapter 5, the integration capacitor nonlinearity need not be compensated.

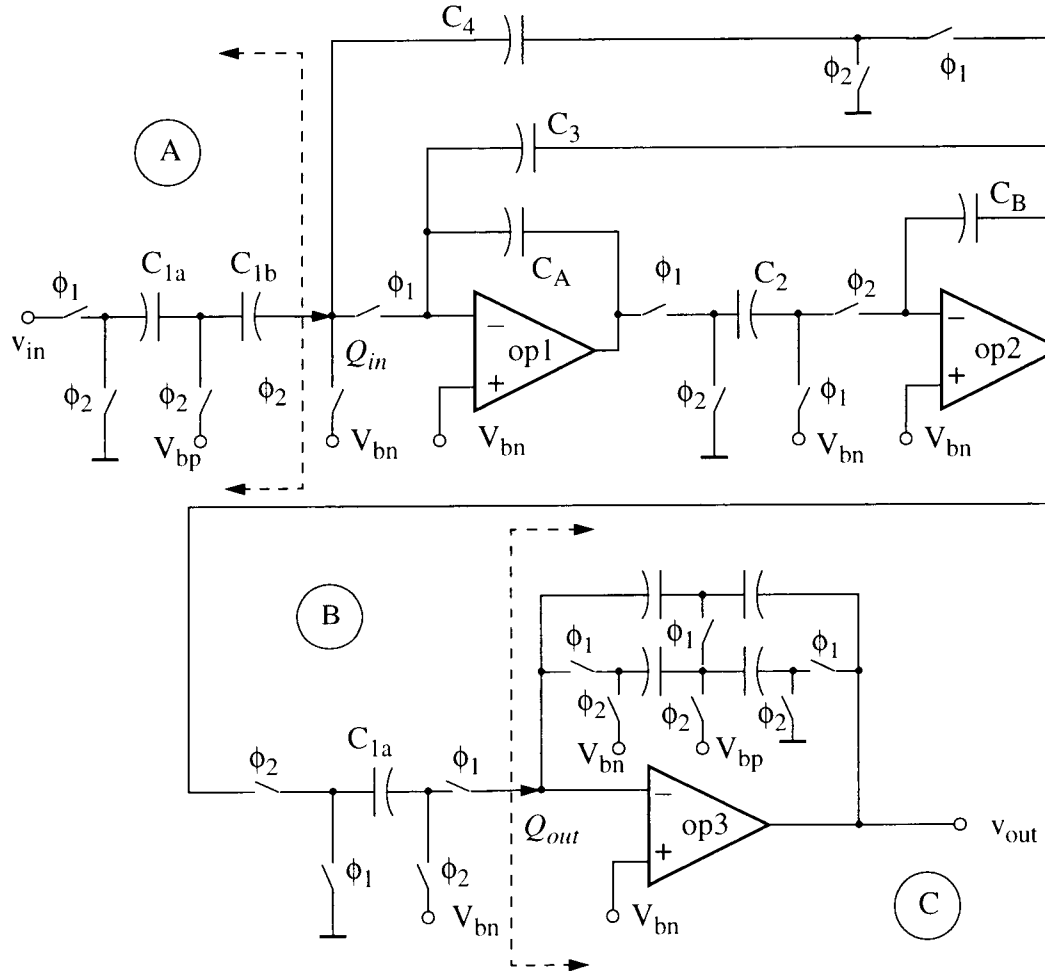


Figure 4.12:A third-order low-pass filter using MOSFET capacitors.

Figure 4.12 shows a third-order SC lowpass filter using MOSFET capacitors only. It consists of a lowpass biquad and a linear low-pass section. As described earlier in Sec. 4.1, the circuit can be partitioned in three functional blocks: the linearized $V-Q$ conversion block, the signal processing block and the linearized $Q-V$ conversion block. In Figure 4.12, the $V-Q$ conversion block is labelled as block A. It is a series-compensated SC branch for high linearity and high signal swing. Block B does the second-order low-pass signal processing in the charge domain, and it uses only simply biased MOSFET capacitors. As shown by Eq. (4.7), the capacitor nonlinearity does not affect the signal processing in the charge domain. Assume an undistorted signal charge Q_{in} flowing into B from A. The charge flowing out of B (Q_{out}) then represents the second-order filtered signal of Q_{in} with no distortion. Block C realizes the linearized $Q-V$ conversion incorporating

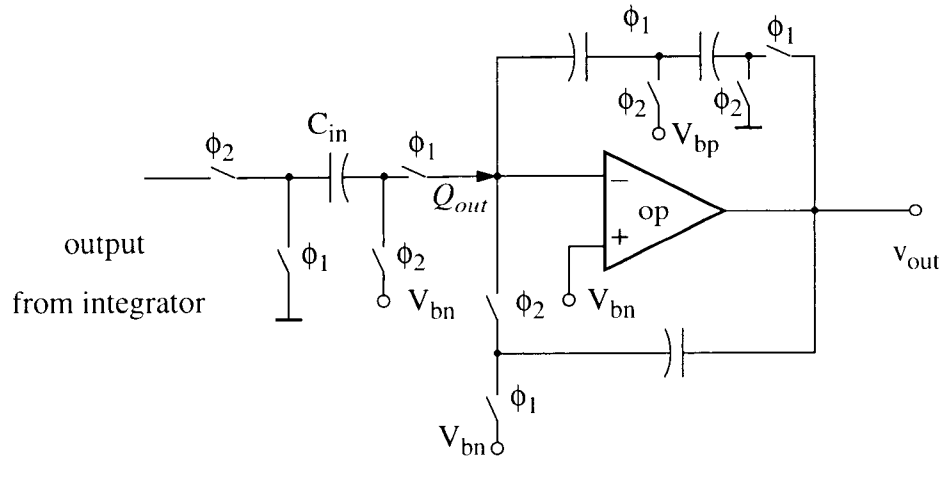


Figure 4.13:An extra gain- and offset-compensated gain stage for linearizing the integrator output voltage.

also the first-order lowpass function. Since the third integrator is a lossy integrator, linearization and dc biasing for the integration capacitor can both be achieved using a series branch.

If the last stage of a SC filter is a lossless integrator, the series branch cannot be used to provide dc biasing and linearization for the integration capacitor. However, an extra gain stage may be used to realize the linearized Q-V conversion. Shown in Figure 4.13 is an offset- and gain- compensated gain stage based on the circuit in Figure 2.5. In Figure 4.13, the input capacitor is not compensated; it is used to generate the undistorted Q_{out}. This requires that the nonlinearity of C_{in} match the nonlinearity of the integration capacitor in the previous stage.

In special cases such as a single-bit SC delta-sigma modulator, where the output of the integrator is the input to a 1-bit quantizer, the integrator capacitor need not be compensated, provided its $Q(v)$ characteristic is monotonic within the region of operation. This is because only the polarity of $v_{out} - V_{ref}$ is sensed by the quantizer. This subject will be further discussed in Chapter 6.

4.7 Conclusions

Depending on where the capacitor is used in the SC circuit, its nonlinearity may or may not directly contribute harmonic distortion to the overall signal processing. Series-compensated and parallel-compensated capacitor branches can be used where the capacitor nonlinearity directly affects the signal processing integrity. This is usually at the input branch and at the last stage of the signal processing block. Despite the larger capacitor area needed for kT/C noise reduction, the series-compensation technique is favored over the parallel one, due to its simpler biasing scheme, larger permissible signal swing and better capacitor nonlinearity compensation. Using the series-compensation technique, various SC

circuits can be constructed using only MOSFET capacitors without sacrificing much linearity, as will be shown in the design example described in Chapter 6.

Chapter 5. Thermal Noise Calculation in Switched-Capacitor Circuits

Thermal noise is perhaps the most fundamental error source in many switched-capacitor circuits. In this Chapter, thermal noise analysis is performed for the CDS circuits described in Chapter 2 and Chapter 3, and also for the circuits using MOSFET capacitors described in Chapter 4.

5.1 kT/C Noise in CDS Circuits

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium [38]. In switched-capacitor circuits, the thermal noise from both the op-amp and the switches needs to be taken into account when calculating the overall circuit noise. Thermal noise is limited usually only by the time constants of the switched capacitors or the bandwidth of the op-amps. Due to aliasing, when such wide-band noise is sampled in a switched capacitor circuit, the calculations of thermal noise is often complicated. As will be revealed next, the noise energy resulting from the switches is a function of the value of the sampling capacitor, the temperature and the Boltzmann constant, and is hence often referred as kT/C noise.

5.1.1. kT/C Noise in a Single Capacitor

Consider a capacitor and a resistor in series with a switch which periodically opens, sampling a noise voltage onto the capacitor (Figure 5.1). If the pole associated with the RC time constant is at a frequency much higher than the sampling frequency f_s (usually a requirement for switched-capacitor circuits), then all the thermal noise power can be considered as being aliased into a band from 0 to $f_s/2$.

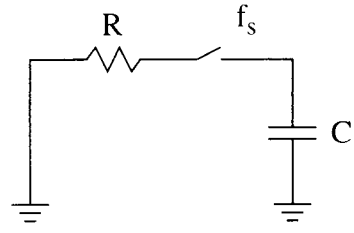


Figure 5.1: Periodically sampled capacitor

To calculate the total noise power, one can model the resistor as having a noise source in series, with a power equal to the Johnson noise $4kTR\Delta f$. The total noise power can be found by evaluating the integral

$$e_T^2 = \int_0^\infty \frac{4kTR}{1+(2\pi fRC)^2} df = \frac{kT}{C}. \tag{5.1}$$

It is interesting to note that while the thermal noise is generated in the resistor, the total noise power depends only on the capacitor. Since the noise is aliased down to the band from 0 to $f_s/2$, the final spectrum is white with a spectral density

$$S(f) = \frac{2kT}{f_s C}. \tag{5.2}$$

In most switched-capacitor circuits, there are two samplings of the thermal noise per clock period, resulting in a spectral density

$$S(f) = \frac{4kT}{f_s C}. \tag{5.3}$$

It should be noted that the noise spectral density of a switched capacitor is the same as that of its equivalent resistor, $R_{eq} = 1/(f_s C)$, in the band from 0 to $f_s/2$, i.e.

$$S_T(f) = 4kTR_{eq} = \frac{4kT}{f_s C} \tag{5.4}$$

5.1.2. kT/C Noise in Composite Capacitor Branch

In some cases, there are several capacitors and switches in a sampling branch. The kT/C noise calculation is then more complicated. Shown in Figure 5.2 is the kT/C noise calculation model for a series switched-capacitor branch with a switch at the center node. Simple nodal analysis of the circuit gives

$$V_A = \frac{(sC_1R_2)v_{n1} + (1 + sC_1R_1)v_{n2}}{1 + s(C_1R_1 + C_2R_2 + C_1R_2) + s^2C_2R_2C_1R_1}, \tag{5.5}$$

and

$$V_{AB} = \frac{-(1 + sC_2R_2)v_{n1} + v_{n2}}{1 + s(C_1R_1 + C_2R_2 + C_1R_2) + s^2C_2R_2C_1R_1}. \tag{5.6}$$

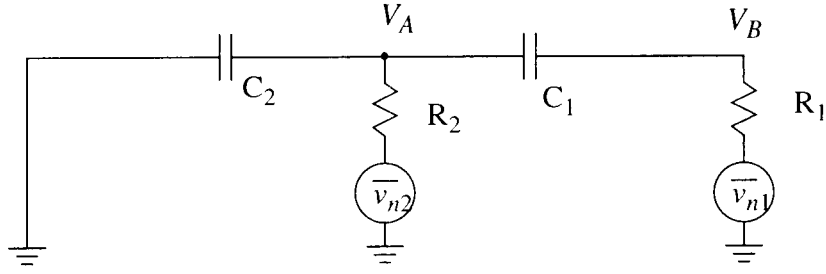


Figure 5.2: Thermal noise calculation model for a series capacitor branch with a switch at the center node.

It is convenient for the following analysis to define $D(s)$ to be the denominator polynomial:

$$D(s) = 1 + s(C_1R_1 + C_2R_2 + C_1R_2) + s^2C_2R_2C_1R_1 . \tag{5.7}$$

To calculate the signal power of V_A, the following well-known relation is used relating the input and output power spectral densities in the s-domain of a linear network having transfer function $H(s)$:

$$S_o(s) = H(s) \cdot H(-s) \cdot S_i(s), \tag{5.8}$$

where $S_o(s)$ and $S_i(s)$ are the bilateral Laplace transforms of the autocorrelation functions at the input and output respectively. Since the two thermal noise sources v_{n1} and v_{n2} are uncorrelated, their contribution may be analyzed separately and the resulting power spectral densities added, i.e.,

$$S_{VA}(s) = \frac{-s^2C_1^2R_2^2}{D(s)D(-s)}S_1(s) + \frac{1 - s^2C_1^2R_1^2}{D(s)D(-s)}S_2(s), \tag{5.9}$$

where $S_1(s)$ and $S_2(s)$ are the 2-sided power spectral densities of v_{n1} and v_{n2}:

$$S_{n1}(s) = 2kTR_1 \tag{5.10}$$

$$S_{n2}(s) = 2kTR_2 . \tag{5.11}$$

Following the approach in [35], Eq. (5.9) can be decomposed into partial fractions as

$$S_{VA}(s) = \frac{(A + Bs)}{D(s)} + \frac{(A - Bs)}{D(-s)} = S^+(s) + S^-(s), \tag{5.12}$$

where $S^+(s) + S^-(s)$ are the transforms of the causal and anti-causal components respectively of the autocorrelation function of V_A.

Equating the coefficients of s and s^2 in Eq. (5.9) and Eq. (5.12) yields

$$A = kTR_2 \tag{5.13}$$

$$B = kTC_1R_1R_2 . \tag{5.14}$$

Substituting Eq. (5.13) and Eq. (5.14) into Eq. (5.12) yields

$$S^{\dagger} = \frac{kTC_1R_1R_2}{C_1R_1C_2R_2}\left(\frac{s+\frac{A}{B}}{D'(s)}\right) = \frac{kT}{C_1}\left(\frac{s+\frac{A}{B}}{D'(s)}\right), \tag{5.15}$$

where $D'(s) = D(s)/(C_1R_1C_2R_2)$ with coefficient of 1 on the s^2 term. Recalling a well-known result from Laplace transform theory, the inverse transform of

$$\frac{s+\frac{A}{B}}{D'(s)}$$

has the form

$$e^{-\alpha\tau}(\cos\beta\tau + \Upsilon\sin\beta\tau),$$

and it has a value of 1 at $\tau = 0$. Thus, the variance of V_A, which is the value of its autocorrelation function $R(\tau)$ at $\tau = 0$, is given by

$$\sigma_{VA} = R(0) = \frac{kT}{C_2} \tag{5.16}$$

Note this is the same amount of kT/C noise as on a single capacitor.

Using the same approach to calculate the variance of V_{AB} yields

$$\sigma_{VAB} = \frac{kT}{C_1}\ . \tag{5.17}$$

Both Eq. (5.16) and Eq. (5.17) reveal that the kT/C noise sampled on individual capacitors is the same as if they were single capacitors. Calculation for the the circuit in Figure 5.2 with an additional switch at the left side of C_2 gives the same result. This conclusion can be extented to more complex SC branches, as predivted by the Equipartition Theorem [64].

5.1.3. kT/C Noise in Switched-Capacitor Circuits

Next, we calculate the kT/C noise in the offset-compensated SC amplifier shown in Figure 2.4a. Assuming that the op-amp is ideal, the overall input-referred kT/C noise is given by

$$\overline{v_T^2} = \frac{2kT}{C_1} + \frac{2kT}{C_2} \cdot \frac{C_2^2}{C_1^2} = \frac{2kT}{C_1} \cdot \left(1 + \frac{C_2}{C_1}\right). \tag{5.18}$$

Next, we shall study how an additive CDS signal path affects the circuit's input-referred kT/C noise. Consider the wide-band gain- and offset-compensated SC amplifier shown in Figure 3.13. The model for the kT/C noise calculation of the signal path during the predictive phase is shown in Figure 5.3. Assuming that the op-amp is ideal, the virtual ground is then ideal, and the kT/C noise resulting from the predictive path does not enter

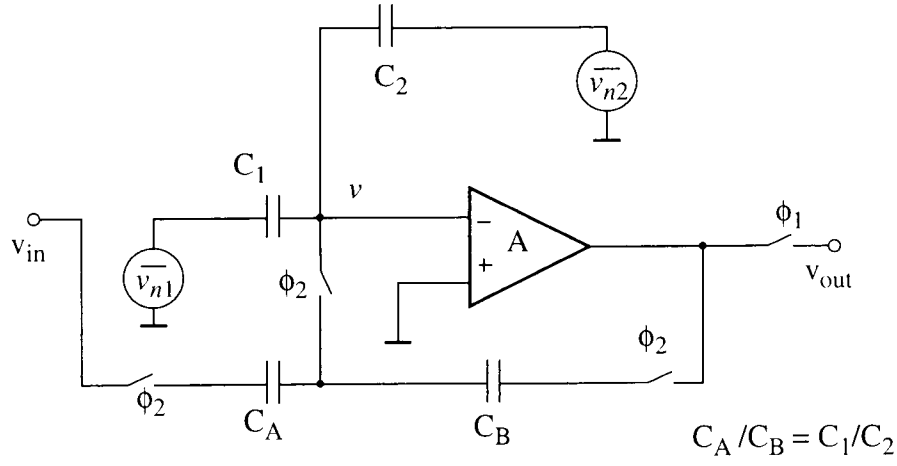


Figure 5.3: kT/C noise calculation model for the wide-band compensated SC amplifier of Figure 3.13.

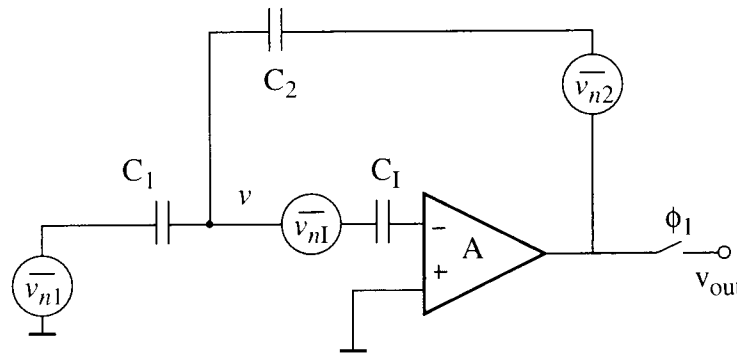


Figure 5.4: kT/C noise calculation for circuits with a storage capacitor.

the main signal path. Thus, the overall input-referred kT/C noise should be the same as that of the offset-compensated one with it magnitude shown in Eq. (5.18).

The kT/C noise calculation for circuits with a storage capacitor is a little more complicated. Consider Nagaraj's wide-band compensated SC amplifier [22] shown in Figure 3.14, which uses an error storage capacitor C_I. Again, assume that the op-amp is ideal, so that the kT/C noise of the predictive path does not affect the main signal path. During the predictive phase, according to the calculation performed in the previous section, capacitors C_1, C_2 and C_I pick up their share of kT/C noise. During the amplification phase, C_1 and C_2 pick up their kT/C noise one more time, so the resulting noise sources are as shown in Figure 5.4, with their values as follows:

$$\overline{v_{n1}^2} = \frac{2kT}{C_1} \tag{5.19}$$

$$\overline{v_{n2}^2} = \frac{2kT}{C_2} \tag{5.20}$$

$$\overline{v_{nI}^2} = \frac{2kT}{C_I}. \tag{5.21}$$

Simple calculation leads to the overall input-referred kT/C noise

$$\overline{v_n^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2}\left(\frac{C_2}{C_1}\right)^2 + \overline{v_{nI}^2}\left(1+\frac{C_2}{C_1}\right)^2 = 2kT\left(\frac{1}{C_1}+\frac{C_2}{C_1^2}+\frac{1}{C_I}\left(1+\frac{C_2}{C_1}\right)^2\right). \quad (5.22)$$

For the predictive gain- and offset-compensated T/H stage introduced in Figure 3.9, where a series branch is used in the main signal path, the kT/C noise calculation is rather straightforward when the result of Sec.5.1.2. is applied. The resulting single-ended kT/C noise is then given by

$$\overline{v_n^2} = 2kT\left(\frac{1}{C_{store}}+\frac{1}{C_{samp}}\right). \quad (5.23)$$

For SC integrators, a similar approach can be taken for the kT/C noise calculation. In a regular integrator, since the integration capacitor is unswitched, the kT/C noise contribution is only from the input capacitor. However, in SC integrators with correlated-double-sampling schemes, the integration capacitors are often switched, and thus extra kT/C noise is introduced.

The above calculations all assumed an ideal op-amp. When the op-amp has a bandwidth lower than the pole associated with the switches and the capacitors, the resulting thermal noise sampled on the capacitor is actually lower when the op-amp is involved in the sampling (if the op-amp noise is ignored). This is because that the thermal noise now gets low-pass filtered with a lower cutoff frequency. The op-amp noise will be discussed in the next Section.

It should be pointed out that the above kT/C noise analysis results for SC amplifiers conform very well with the measured results from experiments, as will be shown in Chapter 8.

5.2 Op-amp Noise in SC Circuits

Op-amp thermal noise can be calculated by inserting a current noise source from its generator as shown in [12], then performing the noise power integration including the transfer function. The magnitude of the current for such a noise source in a MOSFET in saturation is given by

$$\overline{i_n^2} = 4kT \cdot \left(\frac{2}{3}gm\right) \cdot \Delta f \,. \tag{5.24}$$

This approach, however, often lead to complicated analysis. For a single pole case, the noise voltage can be easily found by using the equivalent noise bandwidth concept [12] without going through complicated mathematics.

Due to the sampling operation in switched-capacitor circuits, the wide-band op-amp thermal noise is aliased down to the base band. Although the correlated-double-sampling technique greatly reduces the op-amp dc offset and the narrow-band $1/f$ noise, it cannot provide suppression for the op-amp thermal noise. Thus, care should be taken to ensure that the overall op-amp thermal noise is kept to a sufficiently low level in high-performance SC circuits.

5.3 Other Noise Sources

Flicker noise is also called $1/f$ noise because it has a spectral density that varies approximately inversely with frequency. In a MOSFET, the $1/f$ noise can be modeled as a voltage source in series with the gate. The spectral power density of the source is given by

$$S_{1/f}(f) = \frac{K}{WL}\frac{1}{f}, \tag{5.25}$$

where K is an empirically determined constant, and is dependent on the process and the type of the device.

Since $1/f$ noise is caused by a fluctuation in the number of carriers flowing in the channel, a device with no current flowing through it has no $1/f$ current noise. Thus, a MOSFET capacitor does not contribute any $1/f$ noise when the circuit is settled to its steady state. However, since the bottom plate of the MOSFET capacitor is the n-well (Figure 4.6a), it is more susceptible to substrate noise coupling, and care should be taken in layout to provide good shielding/isolation for the sensitive capacitors.

Chapter 6. A 3-V All-MOSFET Delta-Sigma Modulator

In Chapter 4, the effects of capacitor nonlinearity were analyzed and techniques were discussed which compensate for such nonlinearity. In this Chapter, a practical design example is described for a 1-bit second-order delta-sigma modulator. It uses MOSFETs in their accumulation region as capacitors, with the input branches linearized using series compensation. It utilizes only basic digital CMOS technology and was fabricated in the Orbit 1.2 μm process. The chip area of the modulator is about 1 mm^2. Measured results show that the modulator has a 96 dB peak S/N and an 86 dB peak S/THD+N for a 6 kHz bandwidth with 5.4 mW power dissipation using a 3 V power supply and a 3.6 V capacitor bias voltage.

6.1 Design Motivation and Design Goals

In many telecommunication applications, the voice-band CODEC is one of the key functional blocks, and it is usually integrated together with a large portion of digital circuitry in a single chip solution. So, it is very desirable to design such voice-band CODECs in a basic CMOS process using a low supply voltage. In particular, an all-MOSFET delta-sigma ADC is of great interest to industry. Also, because of its relatively simple structure and its sensitivity to the analog components' imperfections (primarily to capacitor nonlinearity), a delta-sigma ADC is a good test vehicle for measuring the effectiveness of capacitor nonlinearity compensation techniques, and to verify the analytic results on the capacitor nonlinearity effect described in Chapter 4.

In discussion with some CDADIC (NSF Center for the Design of Analog/Digital ICs) industrial members, typical specifications for the delta-sigma A/D converter were obtained and are shown in Table 6.1. The delta-sigma modulator described in this research

Table 6.1: Modulator design specifications

Parameters	Specifications
power supply (Vdd)	3 V
dynamic range	94 dB
peak S/THD + N	84 dB
input signal swing range (single ended)	0.3 V – 2.7 V
signal bandwidth	50 Hz – 6 kHz
oversampling ratio (OSR)	256
technology	1.2 μm digital CMOS
clock frequency	3.072 MHz

work was designed based on these specifications. It meets the requirements for most voice CODECs [41][42].

6.2 Delta-Sigma Modulation: Background

Oversampling delta-sigma modulation has become popular in recent years because it avoids many of the difficulties encountered with conventional methods for analog-to-digital and digital-to-analog conversion (ADC and DAC), especially for those applications that call for high-resolution representation of relatively low-frequency signals. Here, only the basic principle and basic delta-sigma modulator structures are discussed to serve as a background for the design described in this chapter. More description and analysis on the theory and design of delta-sigma data converters can be found in [38][39].

6.2.1. The First-Order Delta-Sigma Modulator

A first-order delta-sigma ($\Delta\Sigma$) analog-to-digital converter (MOD1) [39], containing an analog integrator, a single-bit quantizer (comparator), a single-bit DAC and a digital decimation filter, is shown in Figure 6.1. One may view the "delta" and "sigma" as referring to the analog operations in the system loop: subtraction of the signal fed back from the input signal and accumulation (integration) of the difference. Intuitively, the operation of the modulator is as follows: To keep the output of the integrator bounded, the DC component (or the low-frequency components) of the feedback must be very close to that of the input signal, thanks to the extremely high gain of the integrator at low frequencies. Thus the 1-bit output is a good digital representation of the analog input signal at low frequencies. The digital lowpass decimation filter removes the out-of-band noise and produces a high-resolution digital representation of the input. A simple derivation gives the output of MOD1 in the z domain

$$V(z) = z^{-1}U(z) + (1 - z^{-1})E(z) , \tag{6.1}$$

where V is a discrete-time binary-valued signal, U is a discrete-time continuous-amplitude signal and E is the quantization error [44]. According to Eq. (6.1), the quantization error is

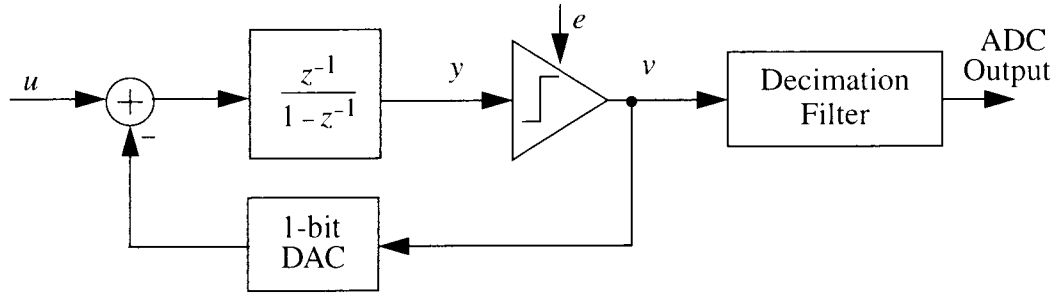


Figure 6.1: MOD1: A first-order delta-sigma ADC.

frequency-shaped by the function $H(z) = 1 - z^{-1}$. This *noise transfer function* (NTF) has a zero at DC and thus suppresses the quantization noise in the vicinity of DC.

Assuming that e is white noise with power σ_e^2, the in-band noise power for MOD1 is given by

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^2 d\omega = \frac{\sigma_e^2 \pi^2}{3R^3}, \tag{6.2}$$

where $\sigma_e^2 = \frac{\Delta^2}{12} = \frac{1}{3}$, if e is uniformly distributed in $[-1, 1]$.

Eq. (6.2) indicates that an octave increase in R will increase the SNR by 9 dB. In principle, the in-band noise can be made as small as desired, simply by making R large enough. Although the requirements for the analog components are much more relaxed that those in the conventional data converters, however, the misplacement of zero(s) in the noise transfer function caused by the finite op-amp gain does limit the amount of quantization noise attenuation in the signal band [40]. In practice, the achievable dynamic range is usually limited by the sum of the quantization noise, kT/C noise, op-amp noise and reference noise powers. The achievable linearity is usually limited by the analog components' imperfection such as op-amp nonlinearity, capacitor nonlinearity and clock feedthrough noise.

A switched-capacitor implementation of MOD1 is shown in Figure 6.2. The integrator is realized by 1 op-amp, 2 capacitors and 4 switches; the DAC by 2 reference voltages and 2 switches; and the quantizer by a simple comparator and a D flip flop [46]. The analog circuitry appears to be quite trivial.

An important property of single-bit modulators is what is often referred to as "inherent linearity" [45]. This property comes from the fact that the input-output transfer

curve of any static two-level DAC can be modeled exactly by a straight line between the two level points. A binary DAC is therefore ideal and does not introduce errors other than simple offset and gain errors. These errors do not introduce distortion, thus the conversion is inherently linear, although other effects (signal-related modulation of the reference, etc.) may introduce nonlinear distortion [38].

One disadvantage of MOD1 is the presence of idle tones in the modulator output caused by limit cycles [47]-[49]. To ease this problem, several methods may be used, such as using multi-bit DAC feedback [50], chaotic modulation [51]-[53], or adding a dither signal [54][55].

Another big disadvantage of MOD1 is that a high oversampling ratio is needed to achieve high resolution. For example, to achieve 16-bit resolution, the oversampling ratio must be about 1500. The high oversampling ratio usually leads to a very high sampling frequency and thus causes difficulties in implementation. As the next section will show,

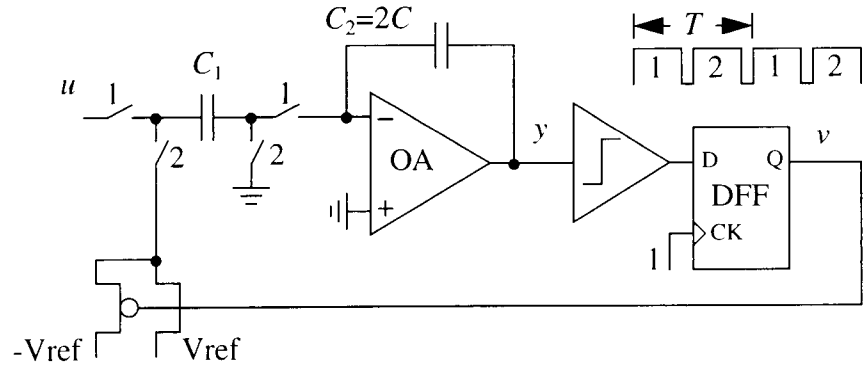


Figure 6.2: A switched-capacitor implementation of MOD1.

both of the above mentioned disadvantages are overcome with a higher-order delta-sigma modulator.

6.2.2. High-Order Delta-Sigma Modulators

A general model of a single-quantizer delta-sigma modulator is shown in Figure 6.3 [46]. This figure shows that such a system consists of three basic parts: a loop filter, a quantizer and a feedback DAC. Modeling the quantizer with $V = Y + E$, the output of the modulator is

$$V(z) = G(z)U(z) + H(z)E(z), \tag{6.3}$$

where $G(z)$ and $H(z)$ are the signal transfer function (STF) and noise transfer function (NTF) of the modulator, respectively. To achieve spectral separation between signal and noise, the magnitude of STF must be close to 1 in the band of interest whereas the NTF must be close to 0.

The simplest high-order delta-sigma modulator is the double-loop, or second-order, delta-sigma modulator [56], shown in Figure 6.4 [57]. The signal transfer function $G(z)$ and the noise transfer function $H(z)$ of this modulator are

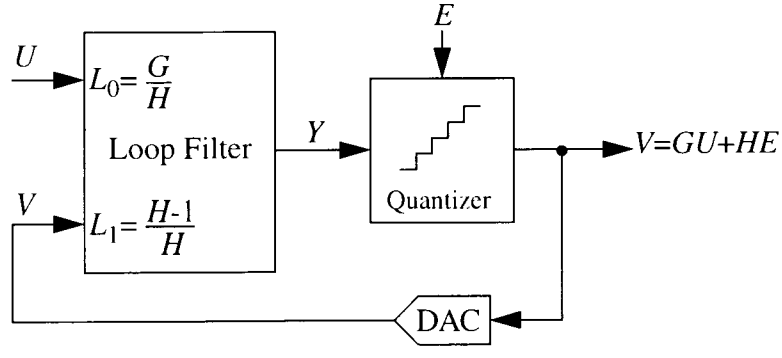


Figure 6.3: A general model of a discrete-time single-quantizer delta-sigma modulator.

$$G(z) = \frac{z}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)} \quad \text{and} \tag{6.4}$$

$$H(z) = \frac{z^2 + (-2 + \alpha + \beta)z + (1 - \beta)}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)} . \tag{6.5}$$

In the most common case where $(\alpha, \beta, \gamma) = (0, 0, 1)$, $H(z) = (1 - z^{-1})^2$. This modulator will be referred to as MOD2. Again assuming that E is a white noise with power σ_e^2, the noise power in the band of interest is

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^4 d\omega = \frac{\sigma_e^2 \pi^4}{5R^5} , \tag{6.6}$$

and thus MOD2 achieves a 15 dB (2.5 bit) increase in the SNR for each octave increase in R— 6 dB (1 bit) per octave better than that for the first-order modulator.

In the above derivation for the signal and noise transfer functions, the quantizer was modeled by $v = y + e$. This is often known as the linear model. The linear model allowed the quantizer, a nonlinear system, to be treated as a linear system with independent inputs y and e. Note that e and u are in reality causally related and therefore not completely

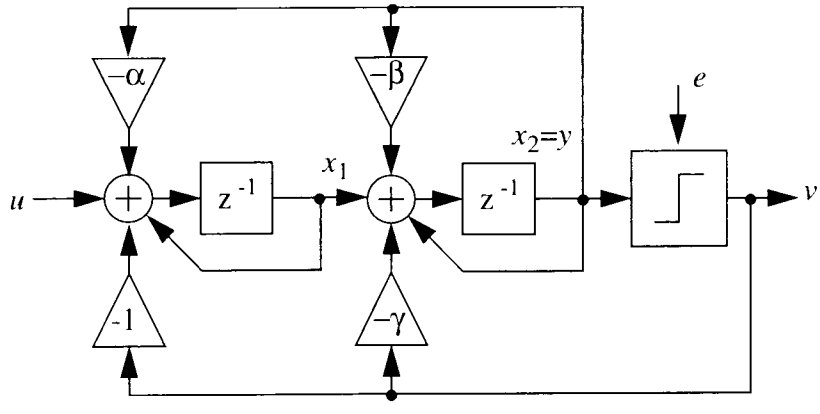


Figure 6.4: A general second-order delta-sigma modulator.

independent. For linear systems with stable transfer functions, the output and the internal states are bounded if the input is bounded. However, the same cannot be said for delta-sigma modulators with stable signal and noise transfer functions, because e is not a real input— e is derived from y, in a nonlinear way. Hence it is possible for $G(z)$ and $H(z)$ to be stable and yet result in a modulator with unbounded internal states.

6.3 Modulator Architecture

Simple calculation using Eq. (6.2) reveals that a second-order system will meet the SNR specification listed in Table 6.1, with a 1-bit quantizer and an OSR of 256. Although the MOSFET capacitor nonlinearity associated with α and β may be cancelled by matching capacitor nonlinearities (Section 4.1, "The Effect of Capacitor Nonlinearity in SC Circuits," on page 52), for simplicity, the standard MOD2 structure is used with $\alpha = 0$ and $\beta = 0$ as shown in Figure 6.5.

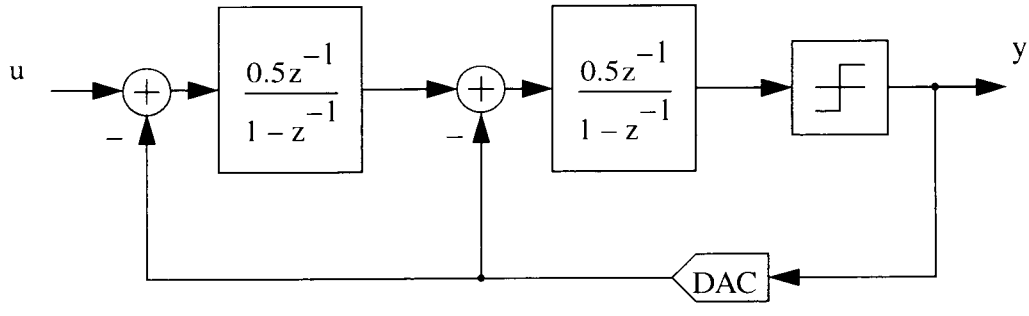


Figure 6.5: The architecture of the 2nd-order modulator.

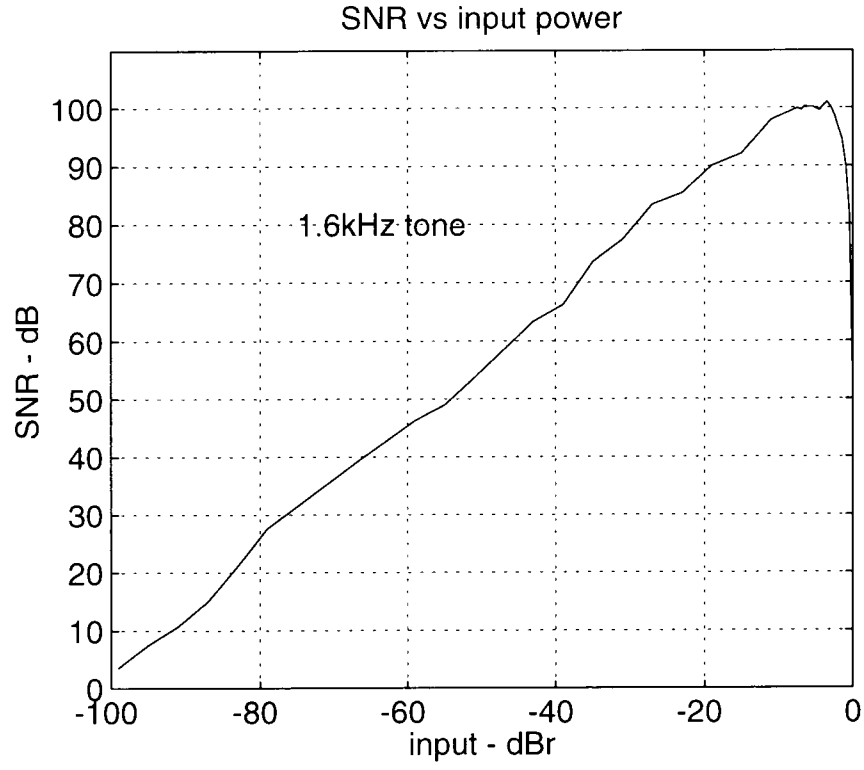


Figure 6.6: Simulated SNR vs. input signal amplitude

Figure 6.6 shows the SNR vs. input power obtained from behavioral simulation using MATLAB. The simulated peak SNR is around 100 dB.

6.4 Circuit Implementation

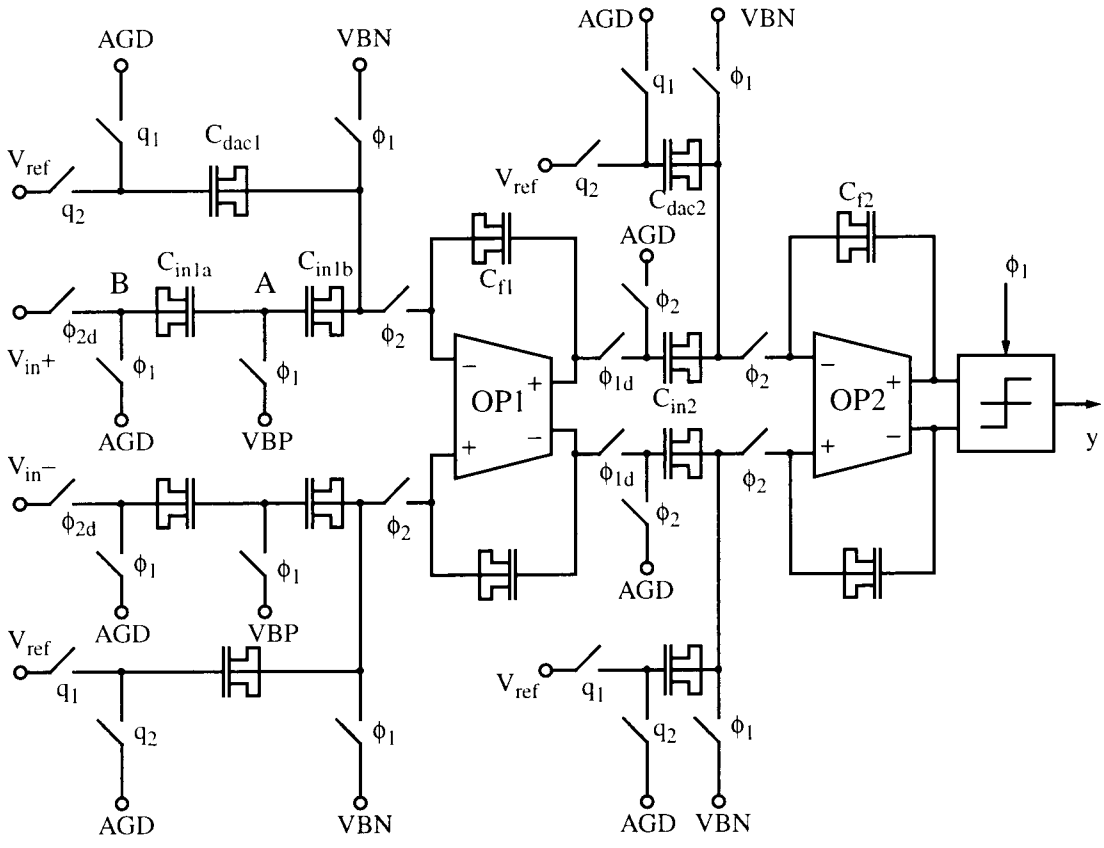
6.4.1. The Modulator Structure

Based on the analysis in Chapter 4 for the capacitor nonlinearity effects, and the methods shown to reduce such effects, the switched-capacitor implementation for the second-order modulator is designed as shown in Fig. 6.7 [40][42]. In the circuit, all capacitors are implemented as simply-biased MOSFET capacitors, except the input capacitors of the first stage, where the series-compensation technique is used. Each input

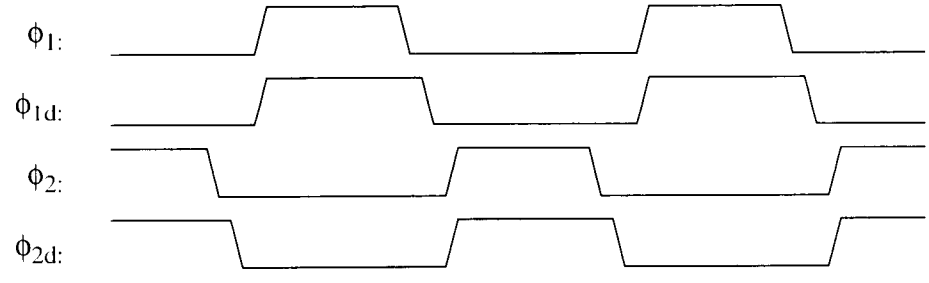
branch of the first integrator contains of two MOSFETs operating in their accumulation region, with their gate-to-channel capacitances C_{in1a} and C_{in1b} connected back to back (Fig. 6.8). The center node of the branch is connected to a bias voltage VBP during ϕ_1 to keep the MOSFET capacitors in their accumulation region. The back-to-back connection reduces the voltage swing across the capacitors and also compensates for their voltage dependence, thus linearizing the charge transfer to the integration capacitors [4][5]. Fig. 6.8b shows the physical realization of the MOSFET capacitor for such a branch [4][5][27].

It can be seen that the signal is processed in the charge domain after the input signal is converted from voltage to charge through the series-compensated SC branch. Since the quantizer has only one-bit resolution, any nonlinearity contained in the signal at the quantizer input (introduced by the $Q - V$ conversion nonlinearity due to the integration capacitor C_{f2} of the second stage) does not introduce signal distortion as long as the $Q - V$ curve is monotonic. For the DAC feedback capacitors C_{dac1} and C_{dac2} in Figure 6.7, since the DAC has only two levels, the capacitor nonlinearity does not introduce signal distortion either. Hence, the only place that the capacitor nonlinearity can directly introduce signal harmonic distortion is at the input capacitors in the first stage, and they are linearized using the series-compensation scheme.

The dc biasing in the circuit of Figure 6.7 is arranged in such a way that all capacitors are kept in their accumulation region during operation, and the capacitor nonlinearities are matched for C_{f1} and C_{in2}. In this particular process, the MOSFET capacitors need to be biased with a voltage greater than 0.5 V for accumulation operation, and greater than 1.2 V for good linearity [28]. In Figure 6.8, the voltage swing at the input node B is from 0.3 V to 2.7 V as called for by the design specifications. Assuming that C_{in1a} and C_{in1b} are equal, node A swings half the magnitude as node B. Let the dc bias voltages VBN and VBP be 0 V and 3.0 V, respectively, and let the analog ground voltage



(a)



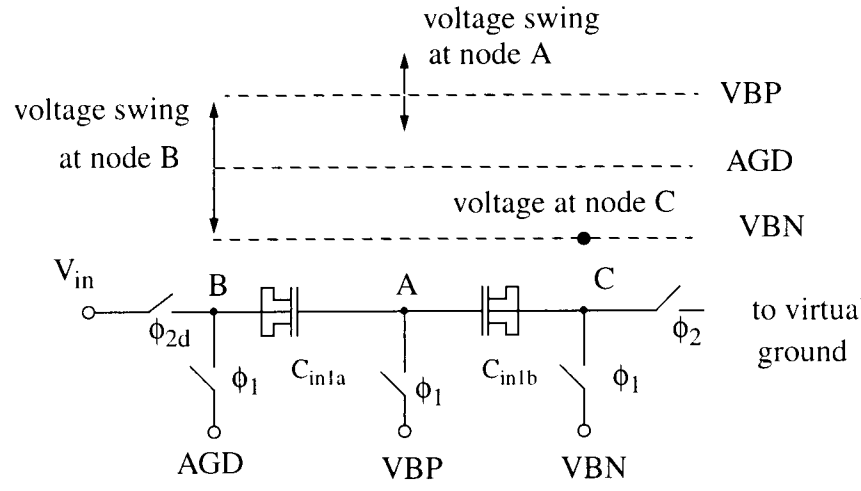
$$q_1 = \phi_{1d} \cdot \bar{y} + \phi_{2d} \cdot y$$

$$q_2 = \phi_{2d} \cdot \bar{y} + \phi_{1d} \cdot y$$

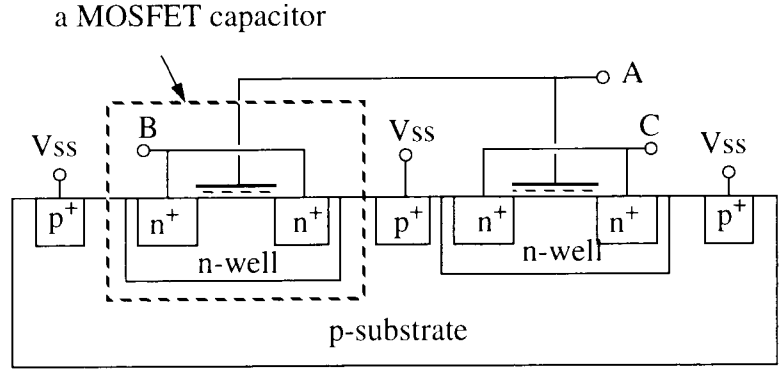
(b)

Figure 6.7: The second-order delta-sigma modulator: (a) circuit diagram; (b) clock signals.

AGD be 1.5 V, the minimum voltage across C_{in1a} is then $1.5 - 1.2 / 2 = 0.9$ V. This happens when the input signal voltage reaches 2.7 V. Then the minimum voltage across C_{in1b} is $3 - 1.2 / 2 = 2.4$ V. So, the input capacitors are guaranteed to operate in their accumulation region. For capacitors C_{f1}, C_{f2} and C_{in2}, the minimum voltage across them is determined by the voltage swing range at the integrator output. To ensure accumulation



(a)



(b)

Figure 6.8: The linearized branch: (a) voltage swing at each node; (b) physical realization.

region operation, scaling needs to be performed so that the voltage swing range of each integrator does not go below 0.8 V. The reference voltage V_{ref} used in this design is 3 V.

6.4.2. Capacitor Sizing

The scaling of the capacitors is primarily based on the desired kT/C noise level. To leave enough headroom for the other noise sources, the kT/C noise is designed to be 100 dB lower than the signal level. The main contribution to the kT/C noise is the input capacitor C_{in1a} and C_{in1b} and the DAC feedback capacitor C_{f1} in the first stage. Since the circuit is implemented in a fully-differential structure, the input signal power is

$$P_{signal} = 20 \cdot \log 10(2.4) - 3 = 4.6 \text{ dBV}. \tag{6.7}$$

The kT/C noise then needs to be lower then -95 dBV. The total in-band kT/C noise can be found as

$$P_{thermal} = 10 \cdot \log 10\left(\frac{k \cdot T}{OSR} \cdot \frac{4}{C_{in1}} \cdot \left(1 + \frac{C_{dac1}}{C_{in1}^2}\right)\right) \text{ dBV}, \tag{6.8}$$

where C_{in1} is the series combined capacitance of C_{in1a} and C_{in1b}. For $C_{in1} = C_{dac1} = 0.8$ pF (corresponding to $C_{in1a} = C_{in1b} = 1.6$ pF), and OSR of 256, Eq. (6.8) gives a kT/C noise level of -97 dBV. So, a capacitance size of 0.8 pF is used for both the input capacitors and the DAC feedback capacitors.

Once the size of the input capacitor is determined, internal scaling is then performed for optimal voltage swing at each node. The resulting values and sizes of the capacitors are listed in Table 6.2.

Figure 6.9 shows the historgram of the integrator output voltages for a -5 dBr, 1.2 kHz input signal corresponds to 3.4 V_{pp} (0 dBr is defined as full swing to the reference voltage, which is a differential input of 6 V_{pp} in this design). Figure 6.10 shows the upper

bound and lower bound of the integrator output voltages (single-ended) vs. input signal power.

6.4.3. Operational Amplifier Design

As described earlier, in a low-voltage mixed-signal IC, where a large amount of digital circuitry is placed on the same chip, a fully-differential structure is highly desirable. Thus, the op-amps discussed here are all fully-differential op-amps.

There are basically two types of operational amplifiers, single-stage (such as folded-cascode, telescopic) and multi-stage (such as two stage) op-amps. Single-stage op-amps usually do not need internal frequency compensation, and are therefore digital-process-compatible when a continuous-time common-mode feedback (CMFB) circuit is used. However, in a single-stage op-amp, since continuous-time CMFB usually reduces the

Table 6.2: MOSFET capacitor sizes

capacitor	nominal value (pF)	Geometry
C_{in1a}	1.6	8 x 12 μm x 12 μm
C_{in1b}	1.6	8 x 12 μm x 12 μm
C_{dac1}	0.8	4 x 12 μm x 12 μm
C_{f1}	3.5	4 x 25 μm x 25 μm
C_{in2}	0.87	1 x 25 μm x 25 μm
C_{dac2}	0.4	2 x 12 μm x 12 μm
C_{f2}	1.6	8 x 12 μm x 12 μm

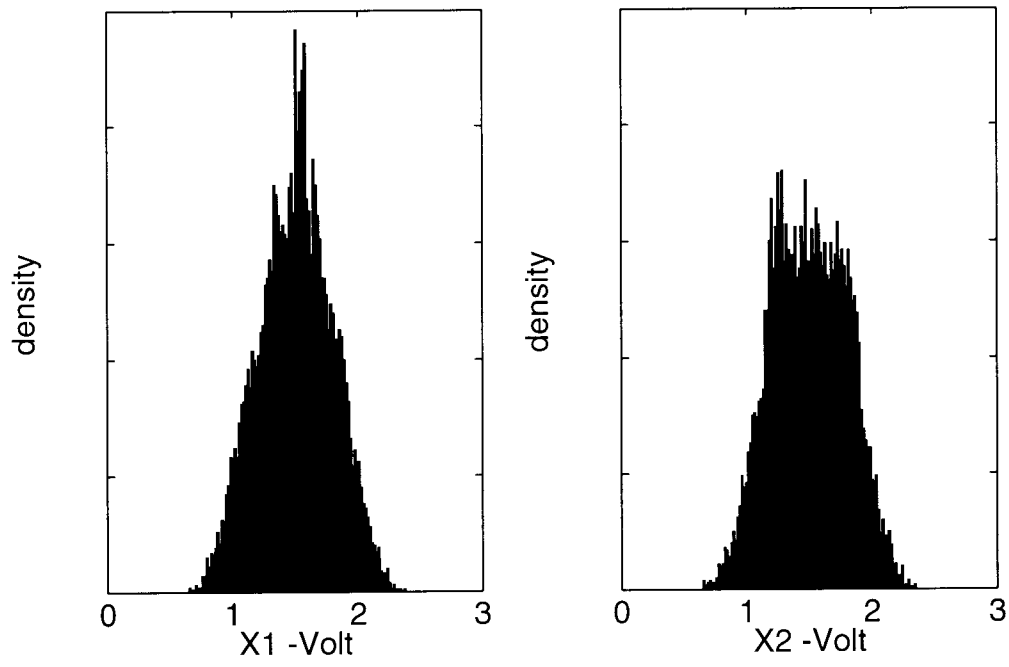


Figure 6.9: Histogram of integrator output. (a) first integrator; (b) second integrator.

achievable dc gain and creates an undesired pole and zero for the frequency response [60], switched-capacitor CMFB is more suitable. Multi-stage op-amps can drive smaller resistors, thus continuous CMFB can be used without sacrificing too much dc gain. Nonetheless, a multi-stage op-amp usually needs frequency compensation, where capacitors are required.

In a basic CMOS process, the op-amp also has to be implemented without the second poly layer, thus MOSFET capacitors ought to be used in place of the poly-poly (or poly-metal) capacitors used in a conventional analog technology. Even though the MOSFET capacitors act just as regular capacitors, the requirement for a dc bias voltage by

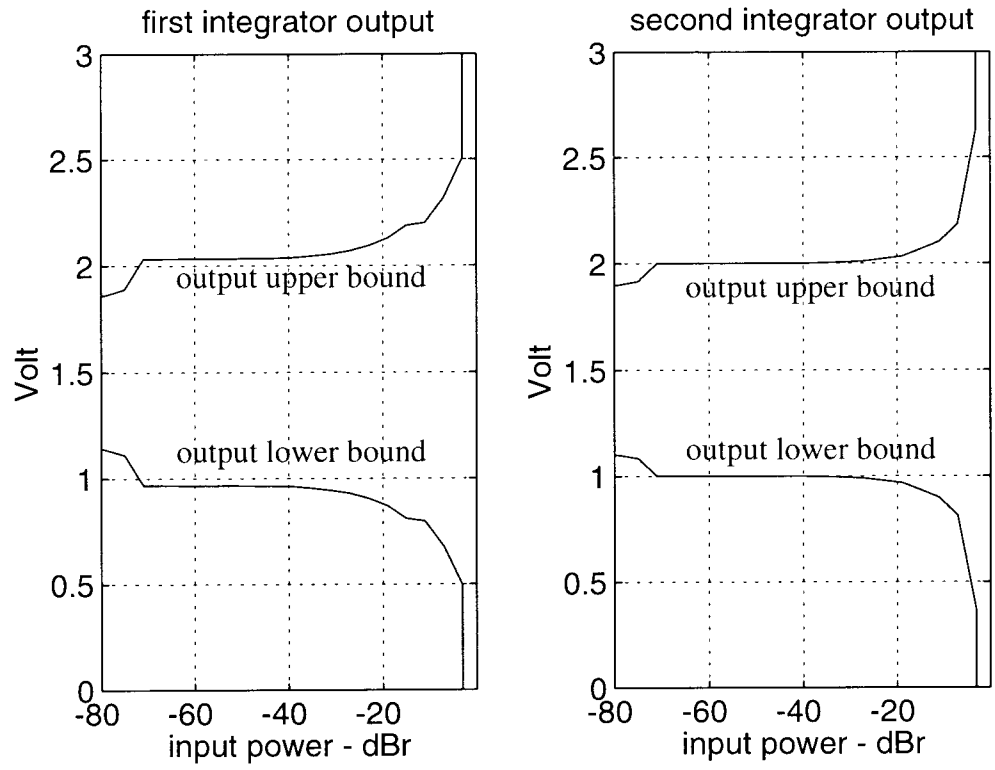


Figure 6.10:Maximum integrator output swing range vs. input power.

the MOSFET capacitors imposes several design challenges for the frequency compensation and CMFB, especially with high output swing range.

Figure 6.11 shows a two-stage op-amp using MOSFET capacitors and source followers for frequency compensation. The purpose of the source followers is to shift the voltage across the compensation capacitors so that they are biased in their accumulation region. One main drawback of this circuit is that the op-amp output swing is now reduced by the source followers. It can be seen that the single-ended output swing range is from Vss + V_{dsat} to Vdd – V_{th} – V_{dsat} as opposed to Vdd – V_{dsat} when such source followers are not used. The CMFB circuit consists of a resistive voltage-divider and an inverting

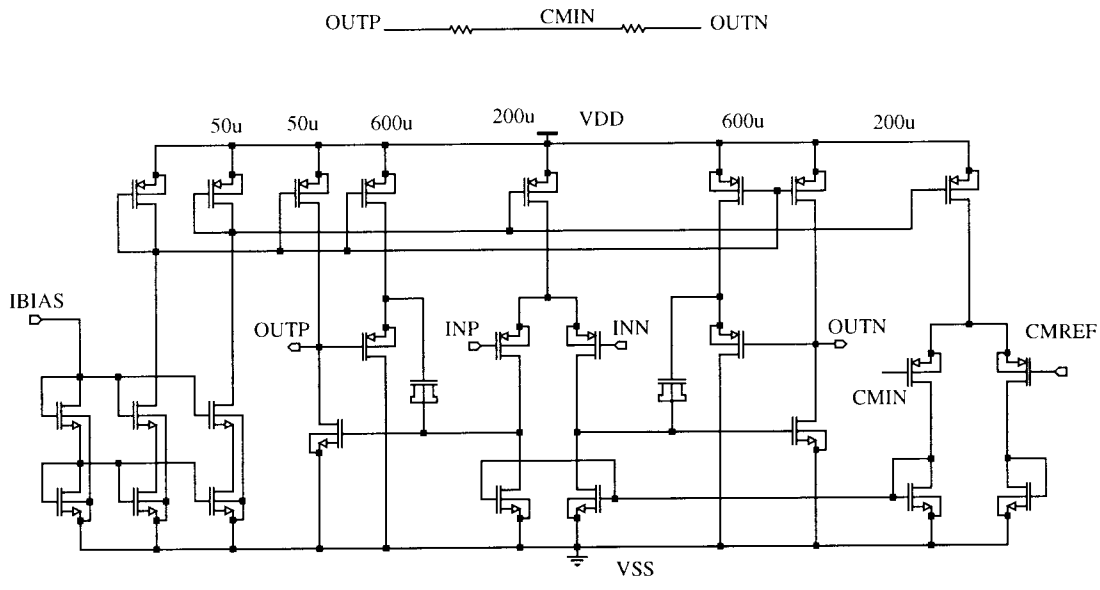


Figure 6.11:Two stage op-amp using a source follower for frequency compensation.

buffer. To improve the op-amp gain, the resistors can be applied between the outputs of the two source followers instead of the op-amp output nodes.

An alternative way of frequency compensation using MOSFET capacitors without sacrificing output swing range is to use composite switched-capacitor branches as shown in Fig. 6.12. This op-amp is used in the actual modulator described in this thesis. Since VBN = 0, and the common-mode voltage at the op-amp input nodes is set by VBN (Figure 6.7), PMOS devices are used in the input differential pair in order to allow such a low input common-mode voltage level. The Miller compensation capacitors are implemented using MOSFETs in two composite branches. Each of them consists of a series branch C_{cla} and C_{clb} (C_{cra} and C_{crb}), and a switched capacitor C_{clc} (C_{crc}) to provide a dc bias for the MOSFETs. During ϕ_2, C_{cla} and C_{clb} are in series and act as a regular compensation capacitor (Figure 6.13a). During ϕ_1, C_{cla} and C_{clb} (C_{cra} and C_{crb}) together

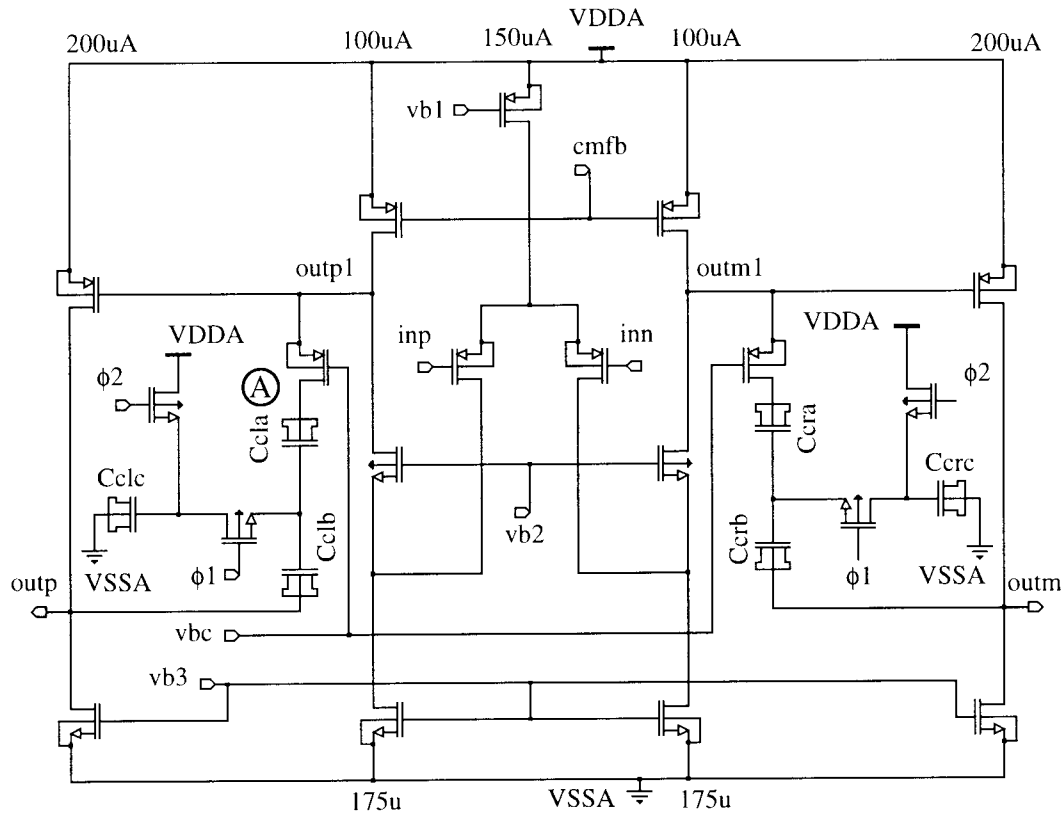


Figure 6.12:Two-stage op-amp using MOSFETs as Miller compensation capacitors.

with C_{clc} (C_{crc}) are connected in a "T" configuration (Figure 6.13b). The capacitance values in its "Π" equivalent circuit (Figure 6.13c) are given by

$$C_m = \frac{C_a \cdot C_b}{C_a + C_b + C_c}, \tag{6.9}$$

$$C_1 = \frac{C_a \cdot C_c}{C_a + C_b + C_c} \text{ and} \tag{6.10}$$

$$C_2 = \frac{C_b \cdot C_c}{C_a + C_b + C_c}. \tag{6.11}$$

When $C_c \ll C_{a,b}$, $C_m \cong (C_a \cdot C_b)/(C_a + C_b)$ results. So, by making $C_{clc,crc} << C_{cla,cra}$, $C_{clb,crb}$, the capacitance between nodes outp1 and outp (outm1 and outm) changes only

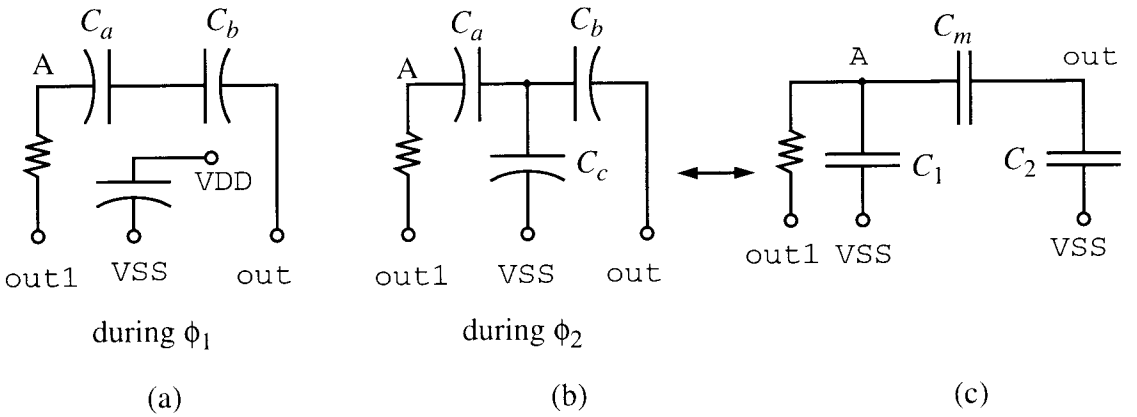


Figure 6.13:Frequency compensation branch. (a) during ϕ_1; (b) during ϕ_2 ; (c) equivalent circuit during ϕ_2 .

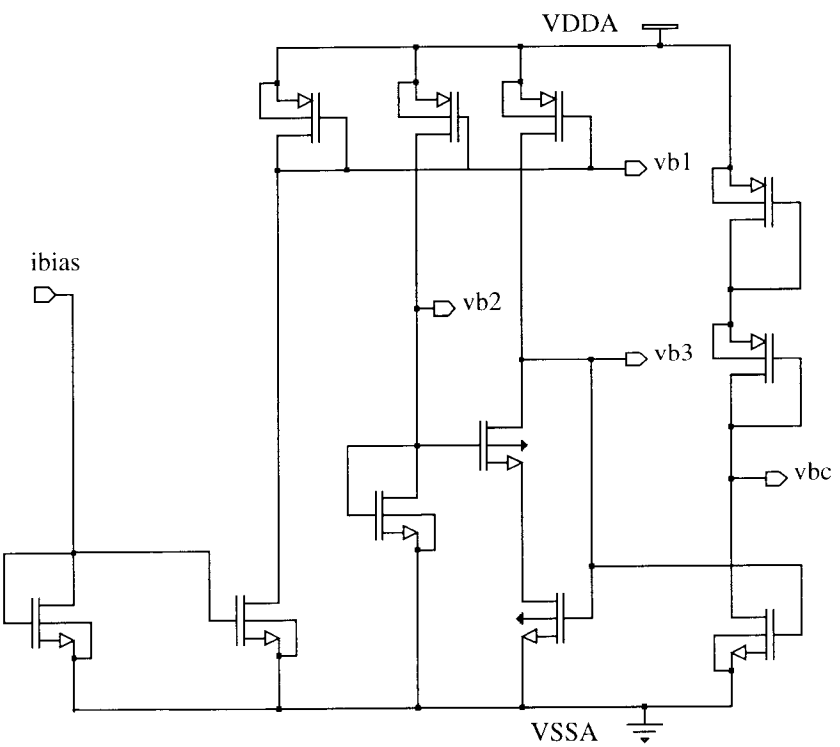


Figure 6.14:Bias circuit for the op-amp.

slightly from ϕ_1 to ϕ_2. This arrangement ensures that the MOSFET capacitors are kept in their accumulation region even when the op-amp outputs swing close to rail. A PMOS transistor in its triode region is used in series with the Miller compensation capacitors to remove the RHP zero and also to cancel the first non-dominant pole of the op-amp [59]. The insensitivity of the cancellation to temperature and process variations is achieved by a bias circuit (Figure 6.14) that provides bias voltages for these two PMOS devices. Simulations showed a 14-bit settling accuracy in 150 ns even in the presence of the pole-zero doublet mismatch tolerance. The switched-capacitor frequency compensation branches introduce some kT/C noise, however, since they are placed between the first gain stage and the second gain stage, the input-referred noise remains negligible.

Fig. 6.15 shows the switched-capacitor common-mode feedback circuit. In order to allow large op-amp output swing, series MOSFET capacitor branches were again used in place of the single capacitors, which would be used in a conventional design.

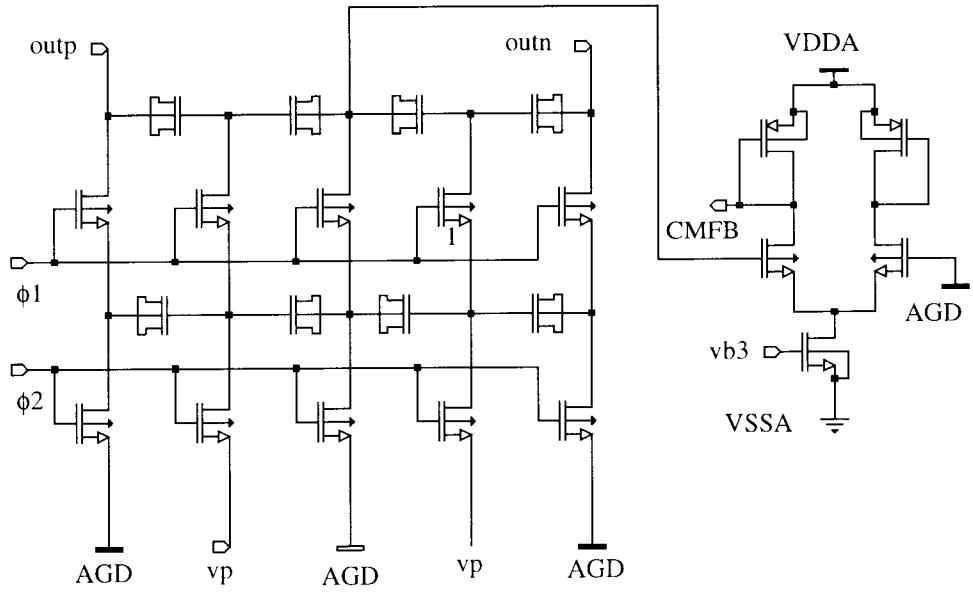


Figure 6.15:Common-mode feedback circuit.

6.4.4. Clock Generator, Clock Bootstrapping Stage and Comparator

In the series capacitor branches (used in the modulator input branches, the op-amp frequency compensation branches and the CMFB circuits), special care needs to be taken in designing the switches and clock drivers. Since the mid-point voltages of the series capacitor branches can go beyond VDD during the operation, clock signals higher than VDD are required. Note that using PMOS switches or CMOS switches does not solve this problem, because PMOS switches can not be completely turned off if the highest clock voltage is VDD. So, bootstrapping stages (Figure 6.16) are needed for the clock signals. Another reason for using bootstrapping stages is that the threshold voltages in this process can be as high as 1.2 V for the NMOS devices, and −1.1 V for the PMOS ones, which may result in insufficient gate over-drive voltages for the switches. The bootstrapping stages allow the use of NMOS devices for all switches. The output of the bootstrapping stage swings from 0 to close to 2Vdd (6 V), depending on the size of the capacitor used in the bootstrapping stage and the capacitive load it drives.

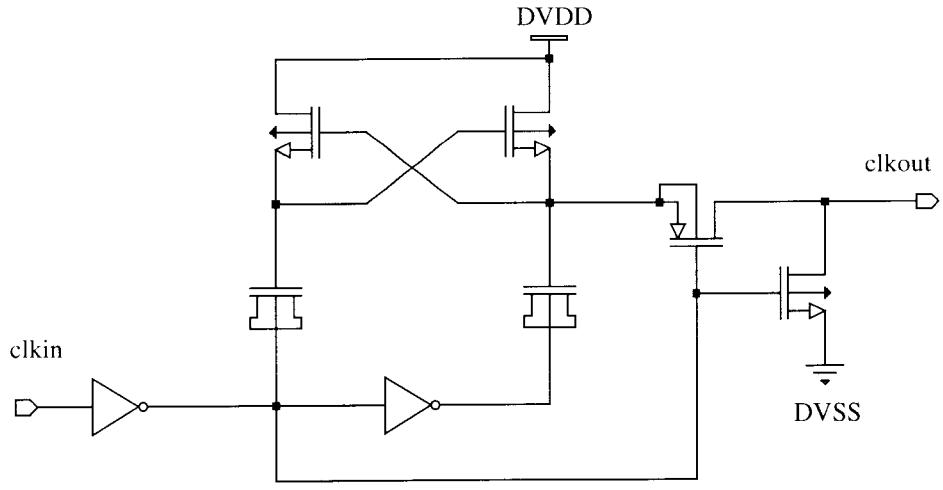


Figure 6.16:Clock bootstrapping circuit.

Figure 6.17 show the schematic of the comparator [61][38]. Since the comparator in a ΔΣ modulator appears after the loop gain block and before the output terminal, nonidealities associated with it are shaped by the loop in the same way that quantization noise is shaped. Nonetheless, there are still some circuit design issues to watch out for [38], such as metastability and hysteresis.

The clock generation circuitry is shown in Figure 6.18 and the overall clock generation circuit including control logic and bootstrapping stages is shown in Figure 6.19. Tunable delay stages were incorporated in the clock generator so that the intervals between the delayed-cutoff clock signals can be varied according the bias current applied at node *id*.

Shown in Figure 6.20 is the circuit diagram of the complete modulator.

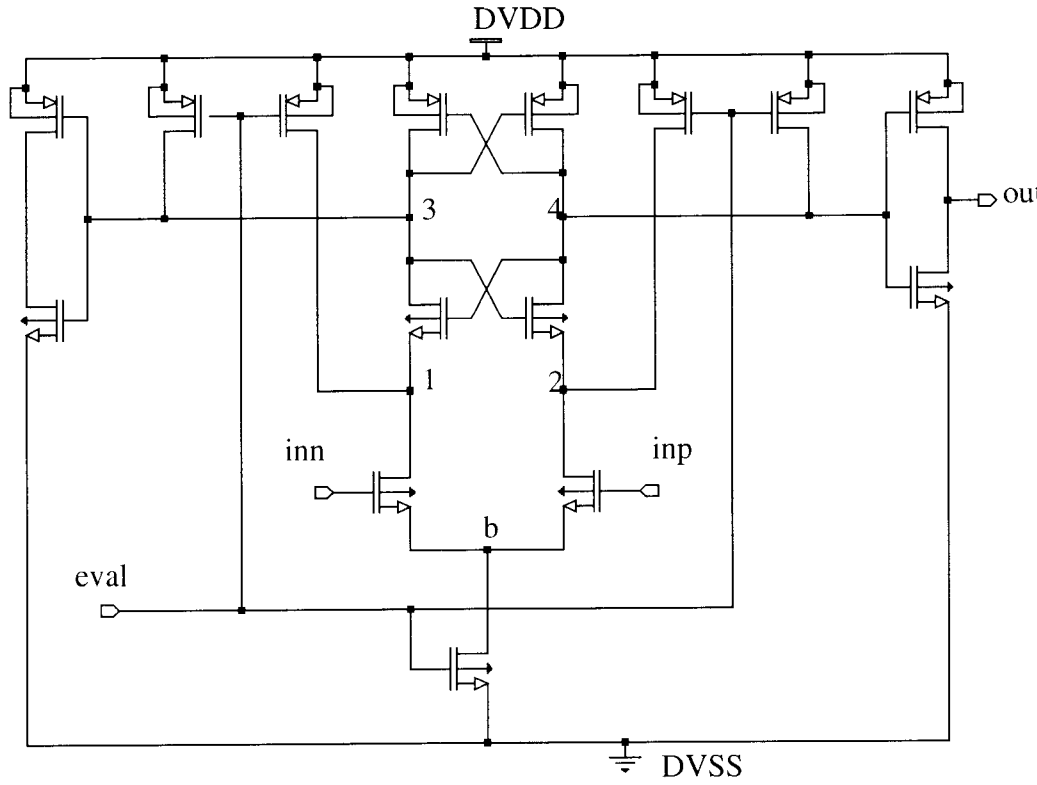


Figure 6.17:The comparator.

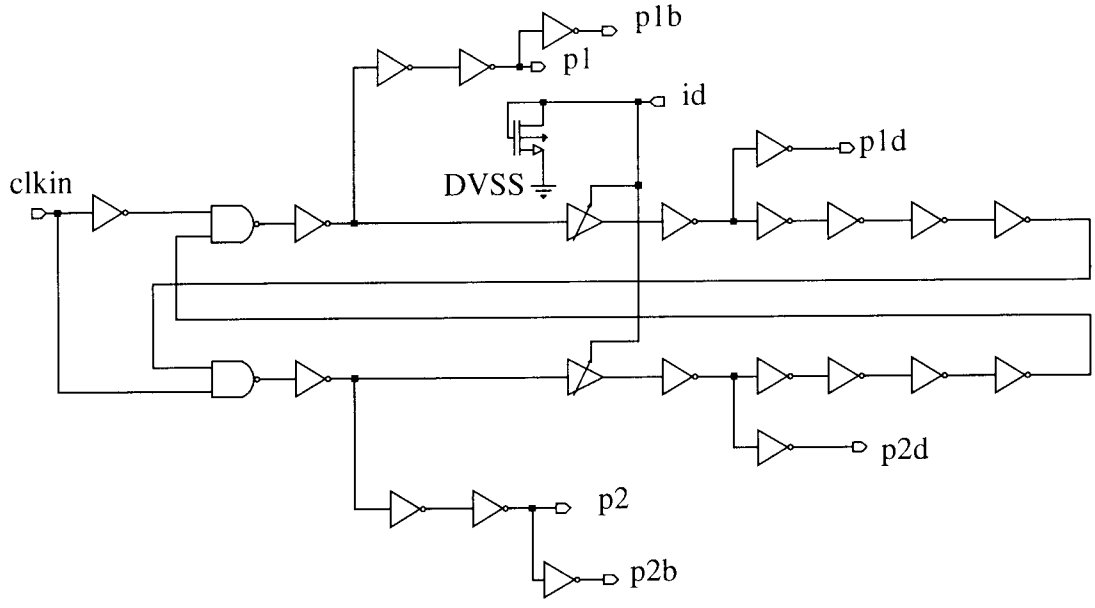


Figure 6.18:Clock generator

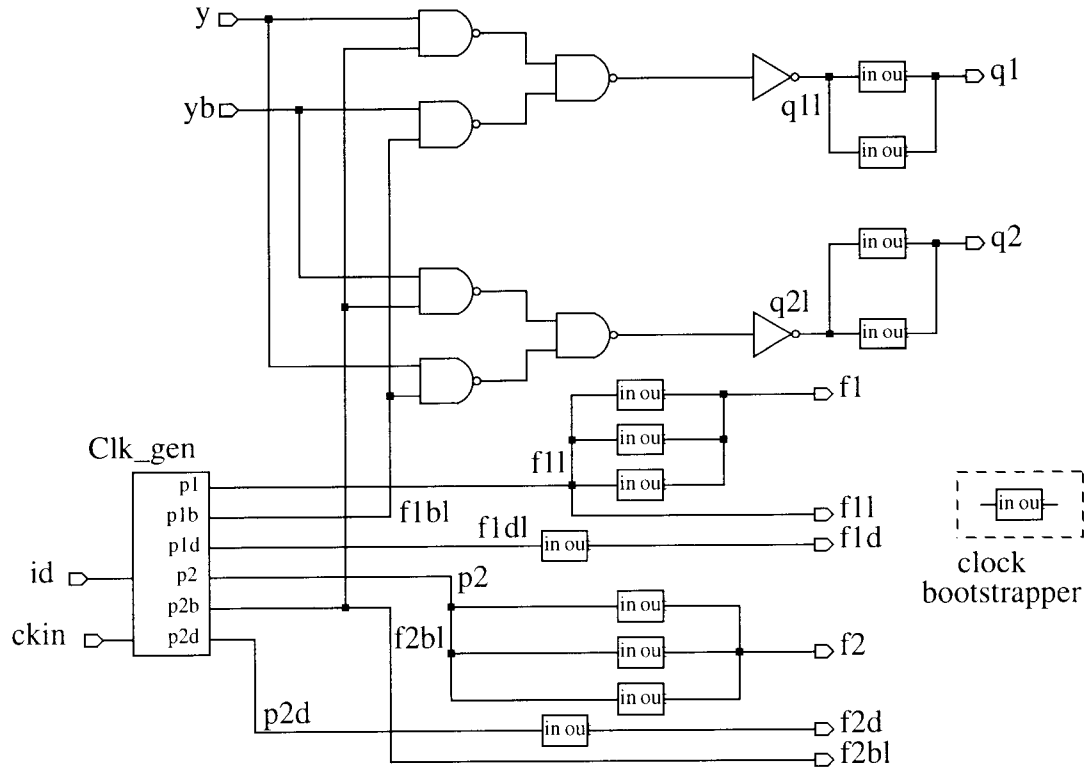


Figure 6.19:Clock generator with control logic and bootstrapping stages.

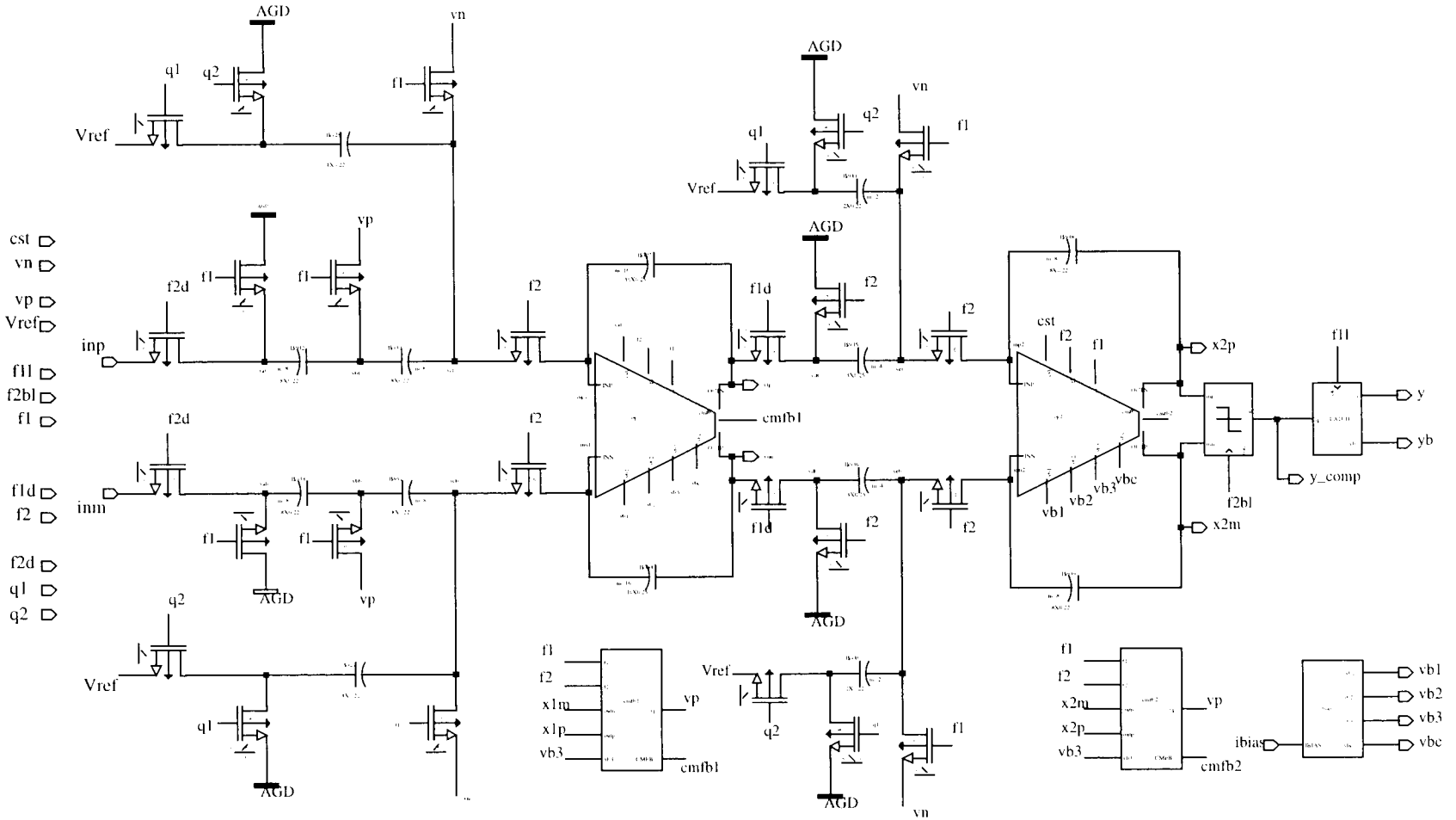


Figure 6.20:Complete modulator with comparator and latch.

6.5 Experimental Results

The resulting design was fabricated in Orbit 1.2 μm process. Figure 6.21 shows the microphotograph of the prototype chip. It consists of two modulators: Modulator A with clock bootstrapping stage, and Modulator B without clock bootstrapping stage.

Fig. 6.22 shows the test setup for this chip. A differential input signal was provided by a Tektronix FG5010 function generator, and a 3-MHz clock was obtained from a pulse

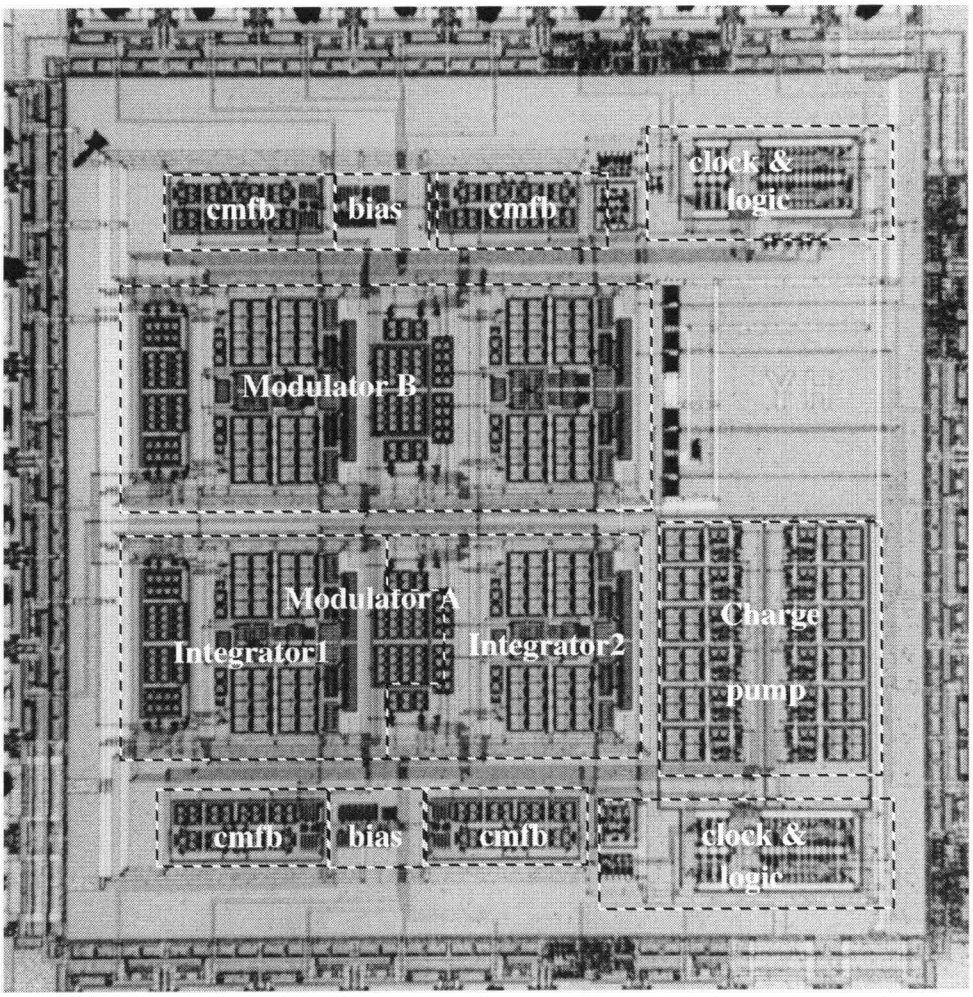


Figure 6.21:Chip photo

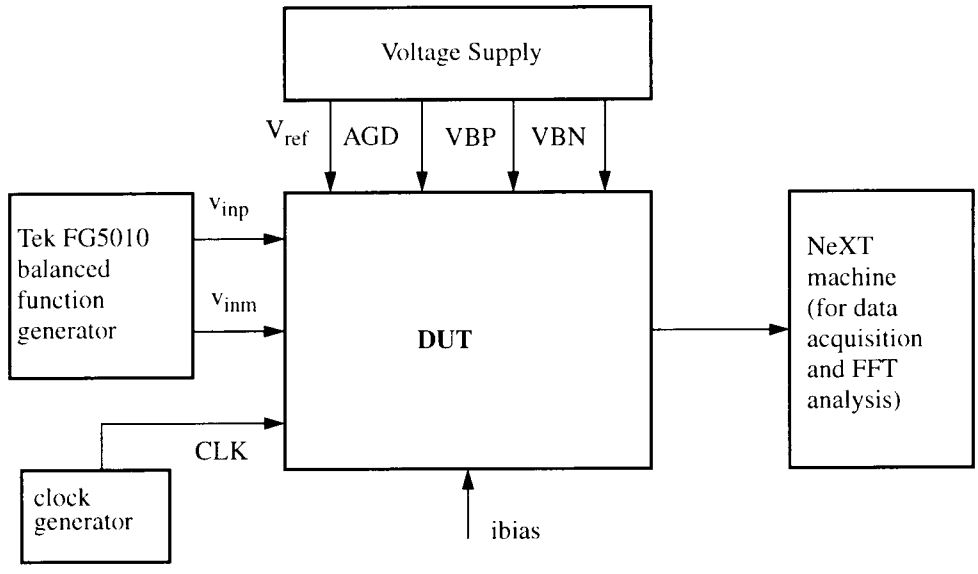


Figure 6.22:Test setup for the modulator.

generator. The bias voltages V_{ref}, AGD, VBP and VBN were provided externally by voltage supplies. A NeXT work station was used to collect the single-bit data stream for FFT analysis.

Figure 6.23 shows the measured responses of SNR, S/THD and S/THD+N vs. input power in a 50-Hz to 6-kHz brick-wall signal band (corresponding to an over-sampling ratio OSR = 256) for a 1.28 kHz sinusoidal test signal. The lowest level of the test signal applied was –80 dBr, which was limited by the signal source. Extrapolating the SNR curve to 0 dB SNR, it can be anticipated that the dynamic range is around 97 dB. For comparison, Figure 6.24 shows the simulated SNR and the measured SNR vs. input signal power. The difference between them is about 6 dB. This is due to the fact that the behavioral simulation did not include any circuit noise. This is further illustrated in Figure 6.25, where the measured SNR curve starts to deviate from the ideal curve when OSR is greater than 128.

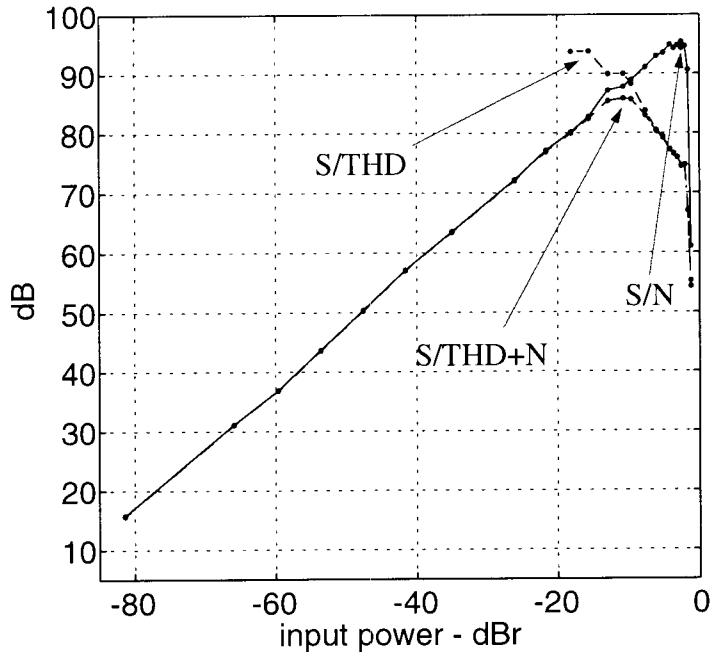


Figure 6.23:S/THD, S/THD+N and S/N vs. input power for a 1.28 kHz sine-wave input. Clock frequency was 3.072 MHz, signal band was 40 Hz - 6 kHz. (OSR=256).

The source of the circuit noise is identified to be the combination of substrate noise, kT/C noise, op-amp thermal noise and $1/f$ noise. Because of the big decoupling capacitor (15 μF) used for the reference sources, noise contributed by the reference sources should be negligible.

A 128 k-point FFT spectrum is shown in Figure 6.26 for a -10 dBr sine-wave input. It was found during the test that, in order to improve linearity at high input magnitude, the voltages across the MOSFET capacitor of the input branch need to be greater than 1.2 V to keep them biased deeply in the accumulation region. So, instead of using the nominal bias VBP = 3.0 V, a 3.6 V was used to obtain the test results in Fig. 6.23 and Figure 6.26. This bias provides a voltage across the MOSFETs greater than 1.35 V for all input levels.

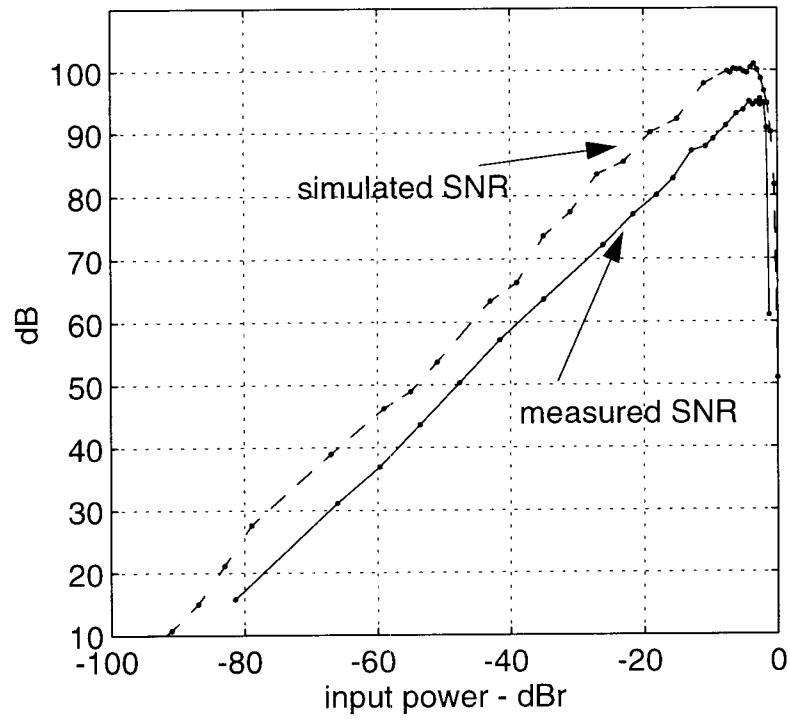


Figure 6.24:Comparison between simulated SNR and measured SNR.

A frequency sweep was also performed for a -5 dBr input signal with frequencies from 720 Hz to 5.6 kHz. The resulting S/N response is shown in Figure 6.27.

As expected, when the input magnitude was very large, the S/THD ratio deteriorated. However, for the same input magnitude, the linearity of the input branch can be improved by using higher VBP bias voltage. This is shown in Figure 6.28, where the S/THD, S/N and S/THD+N responses are plotted against VBP for a 1.28 kHz, -5 dBr sine-wave input.

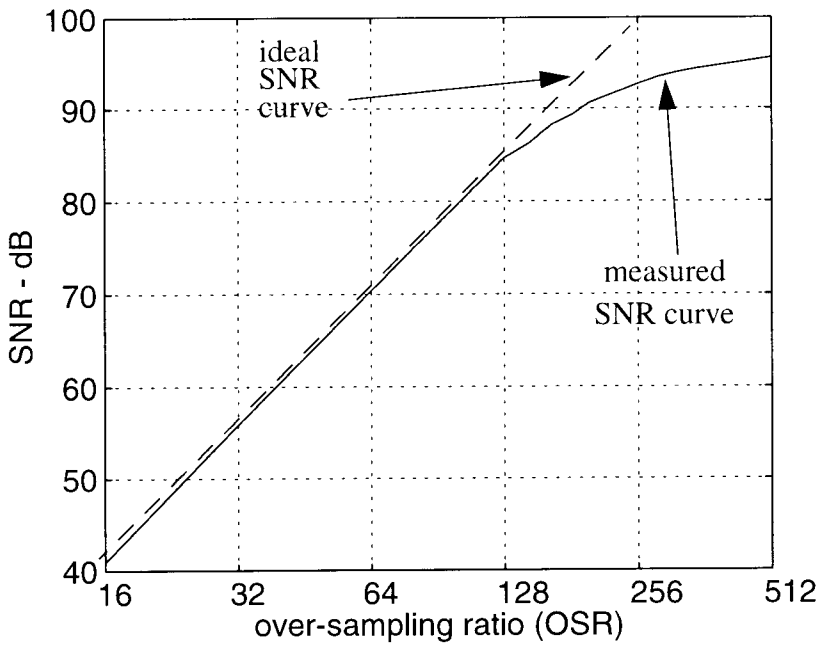


Figure 6.25:SNR vs. OSR for a -6 dBr input signal.

6.6 Conclusions

A 16-bit, 3-V delta-sigma modulator realized in basic digital CMOS technology using only MOS transistors as components was described, and the test results were shown. The measured performance shows that it is possible to build high-linearity SC circuits without using highly linear poly-poly capacitors, and that using a series-compensated capacitor branch is an effective technique to compensate for capacitor nonlinearity.

Due to the large input signal magnitude called for by the design specifications, the S/THD decreased well before the modulator was overloaded. Thus, the S/THD can be further improved by using larger input capacitors and thus decreasing the voltage swing of the input signal.

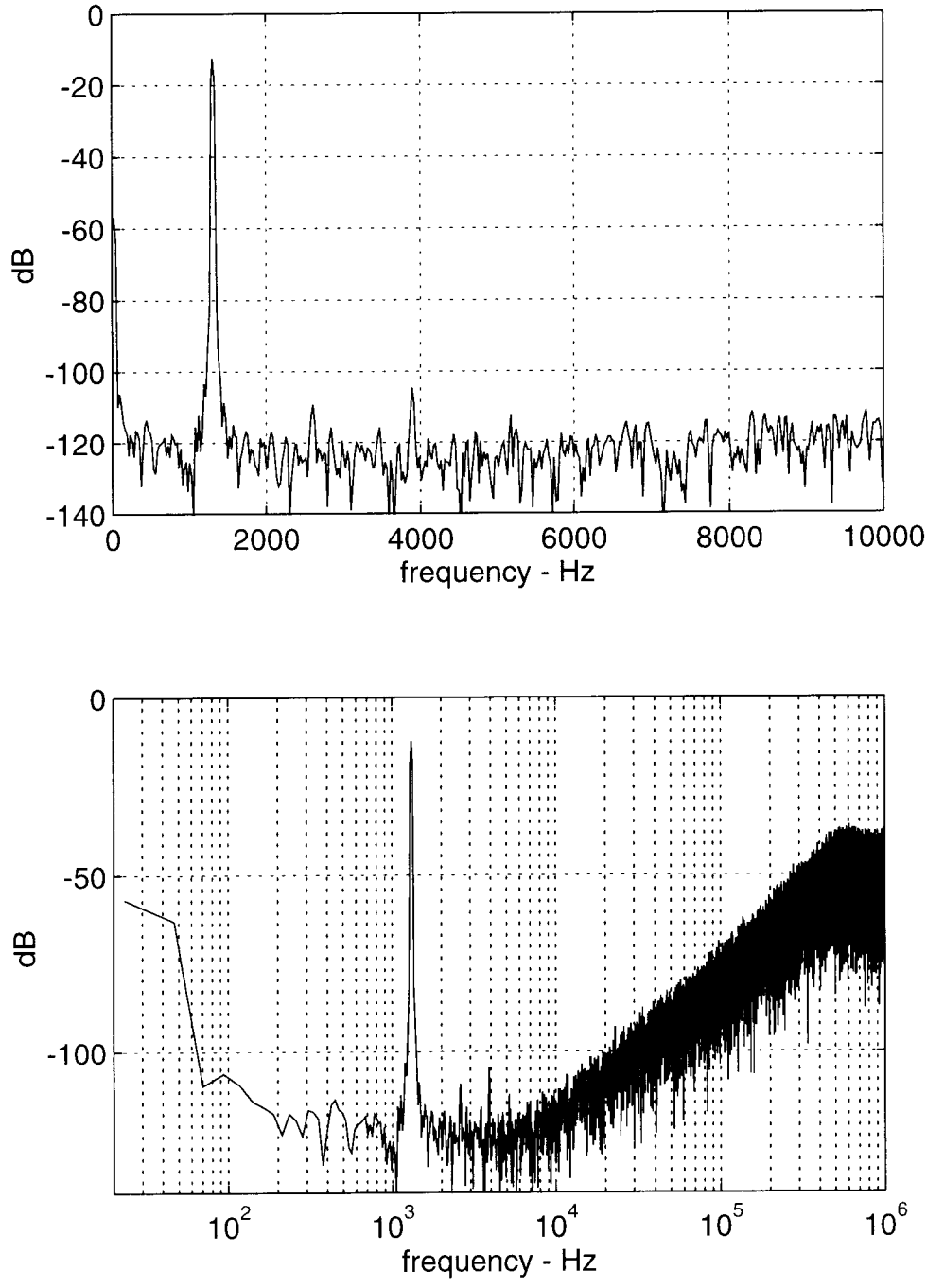


Figure 6.26:128 k-point FFT spectrum of the modulator output for a -10 dBr, 1.28 kHz sine-wave input.

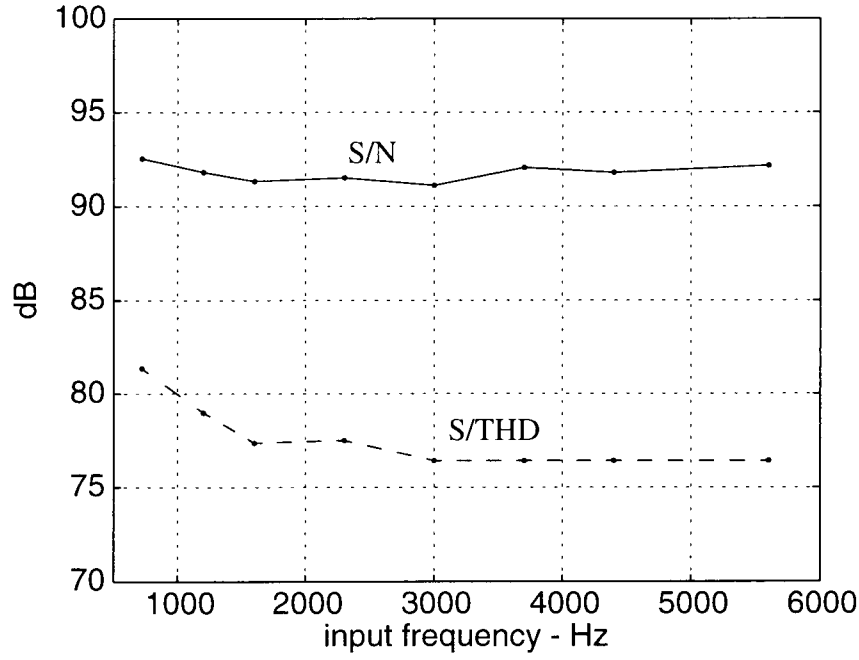


Figure 6.27:SNR and S/THD vs. input signal frequency for a -5 dBr sine-wave input. THD includes harmonics from the 2nd to the fifth order.

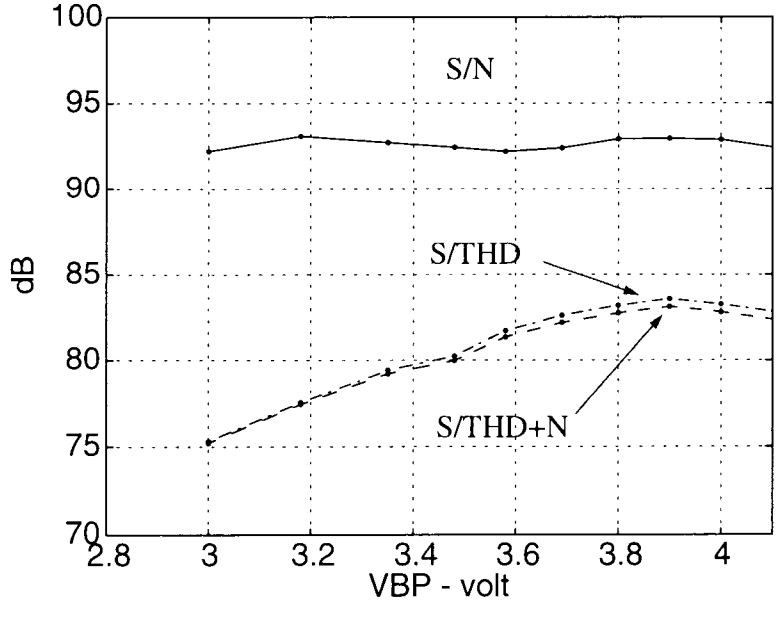


Figure 6.28:SNR, S/THD and S/THD+N vs. VBP bias voltage for a -5 dBr, 1.28 kHz sine-wave input.

Chapter 7. Experimental Results on the Predictive Gain- and Offset-Compensated Track-and-Hold Stage Prototype Chip

In this Chapter, a prototype chip containing the predictive gain- and offset-compensated T/H stage based on the circuit proposed in Chapter 3 is described. The chip was fabricated in the Orbit 1.2 μm double-poly double-metal process. Experimental results show that the S/H stage can achieve a Nyquist sampling rate of 3 MHz using a 5 V power supply. Performance comparison with the other two S/H stages implemented on the same chip indicates that the proposed T/H is superior in both speed and accuracy.

7.1 Motivation and Design Goal

A T/H stage is often used at the front end of an A/D converter to relax its timing requirements, and at the back end of a D/A converter to suppress its glitch impulses [37]. As such, they appear at the interface between the analog world and digital signal processing systems and must therefore achieve a precision and speed commensurate with the overall system performance.

The purpose of developing this prototype was to verify the idea of the proposed predictive gain- and offset-compensated T/H, and to compare its performance with other existing T/H (S/H) circuits. When a T/H stage is used at the front end of an A/D converter, its capacitive load is determined by the next stage, and is usually not very large in a high-speed application. However, as a stand-alone T/H stage, it usually has to drive a large capacitive load (typically 15 - 50 pF) when delivering signal off chip due to the capacitance of the pad and the off-chip wiring and off-chip buffer (or probe). Thus, the speed of the prototype is not expected to be as high as it could be when it is used at the front end of a A/D converter. The target specifications for the T/H stage were 10-11 bit accuracy, and a 2 MHz Nyquist sampling rate.

7.2 Prototype Chip Structure

The two identical predictive T/H stages shown in Figure 3.10 were implemented. They can be switched to operate in a "ping-pong" structure as shown in Figure 3.4. To compare with other existing T/H (S/H) circuits, the S/H proposed in [30] and the offset-compensated S/H shown in Figure 2.4b were also implemented on the same chip. The same op-amp design was used for all four T/H circuits, so that comparison can be made among the circuits without being influenced by the op-amps used.

7.3 Circuit Implementation

7.3.1. The Predictive Gain- and Offset-Compensated T/H

Figure 7.1 shows the schematic of the T/H stage based on the circuit diagram of Figure 3.10, including the switched-capacitor common-mode feedback circuit. All the capacitors used were 1 pF except for the CMFB capacitors whose value was 0.3 pF. According to Eq. (5.23), this corresponds to an input-referred differential kT/C noise of −75 dBV. Since the peak differential input signal power is greater than 3 dBV (corresponding to 4 V_{pp}), the kT/C noise level leaves enough margin for the other noise sources in this 10 - 11 bit design.

Figure 7.2a shows the fully differential folded-cascode op-amp used, and its bias circuit is shown in Figure 7.2b. The simulated bandwidth of the op-amp was around 100 MHz with 2 pF capacitive load and around 18 MHz with 15 pF load.

Figure 7.3 shows the clock generation circuit used to operate the two T/H stages in a "ping-pong" structure. The time intervals between the non-overlapping clock signals and the delay intervals between the delayed cut-off clock signals can be varied by changing the

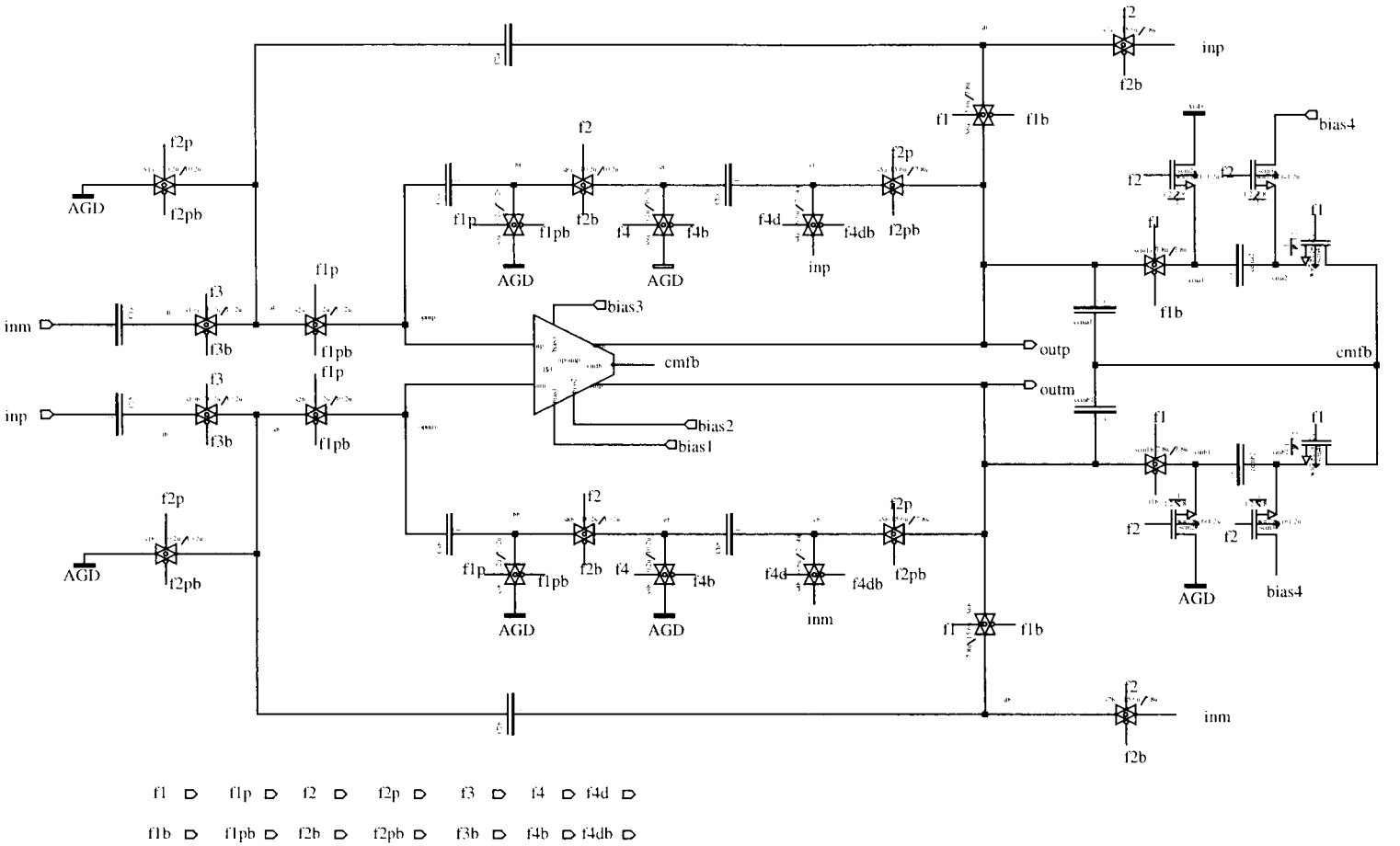
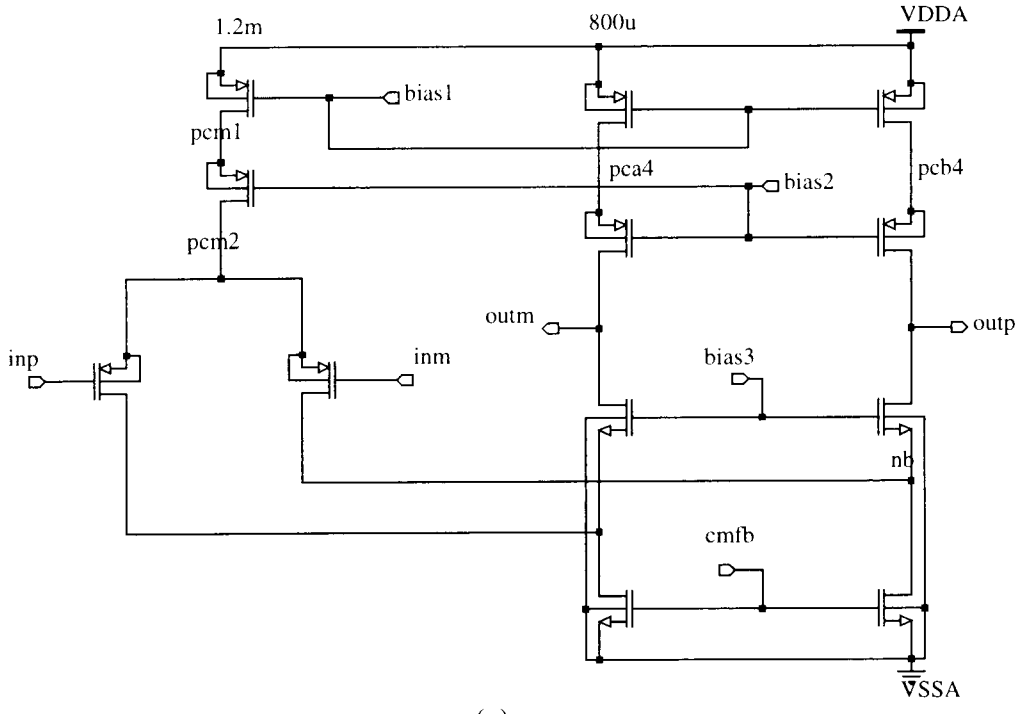
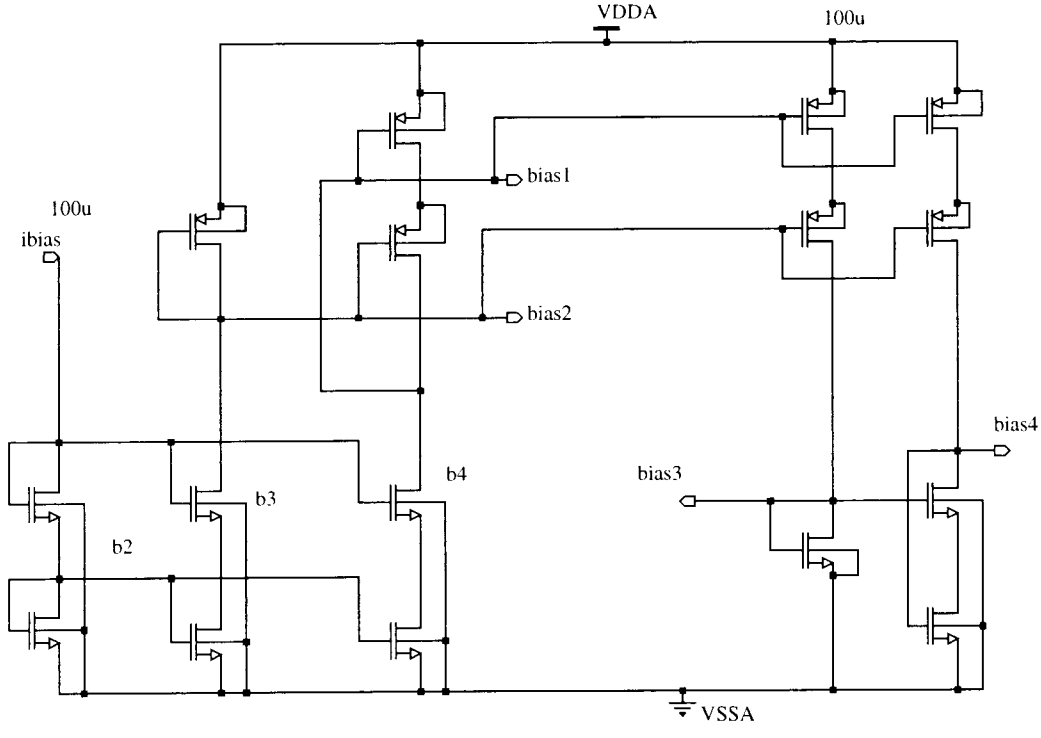


Figure 7.1: Schematic of the predictive T/H stage.



(a)



(b)

Figure 7.2: folded-cascode op-amp: (a) the op-amp circuit; (b) bias circuit.

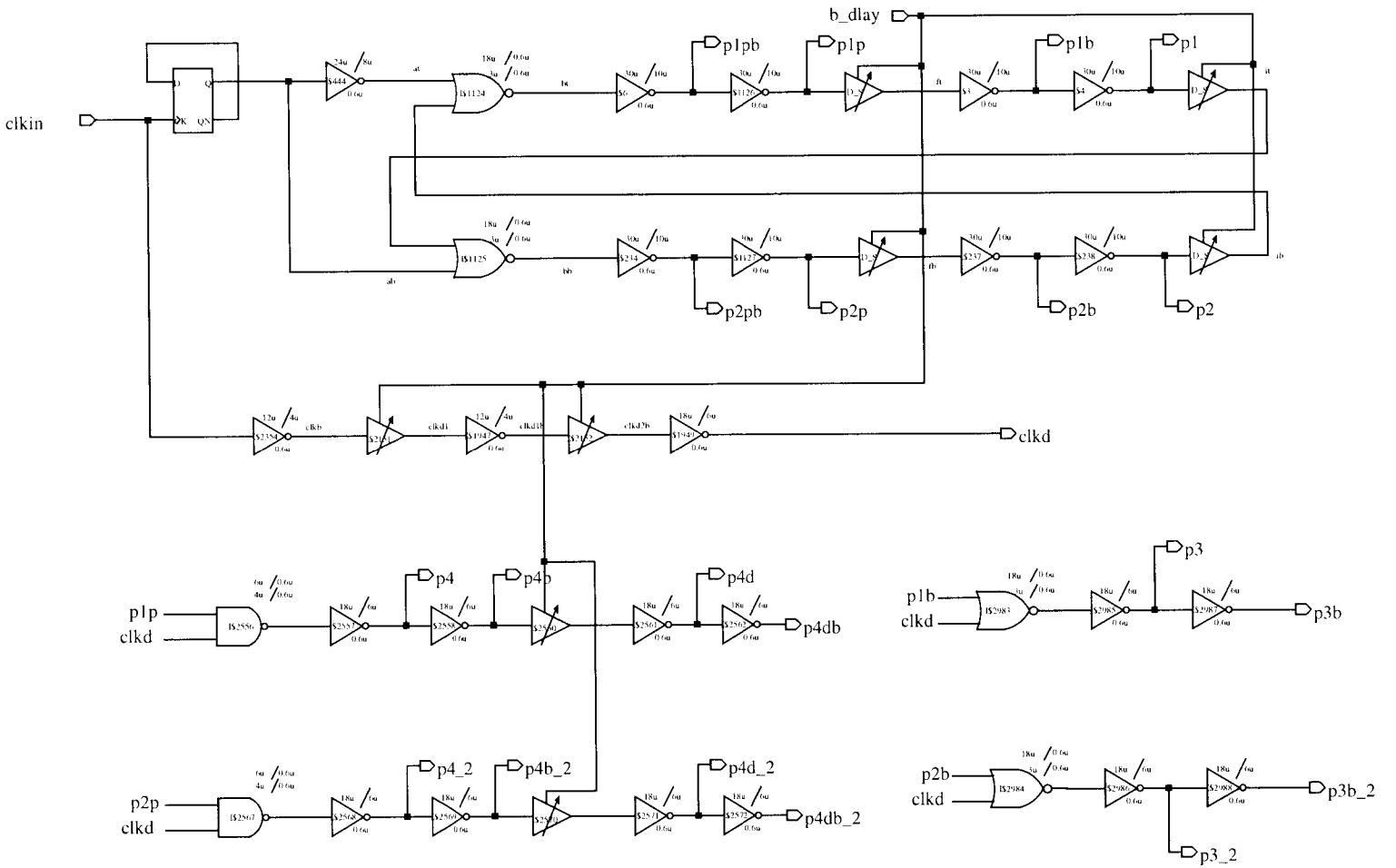


Figure 7.3: Clock generation circuit for the two T/H stages in a "ping-pong" structure.

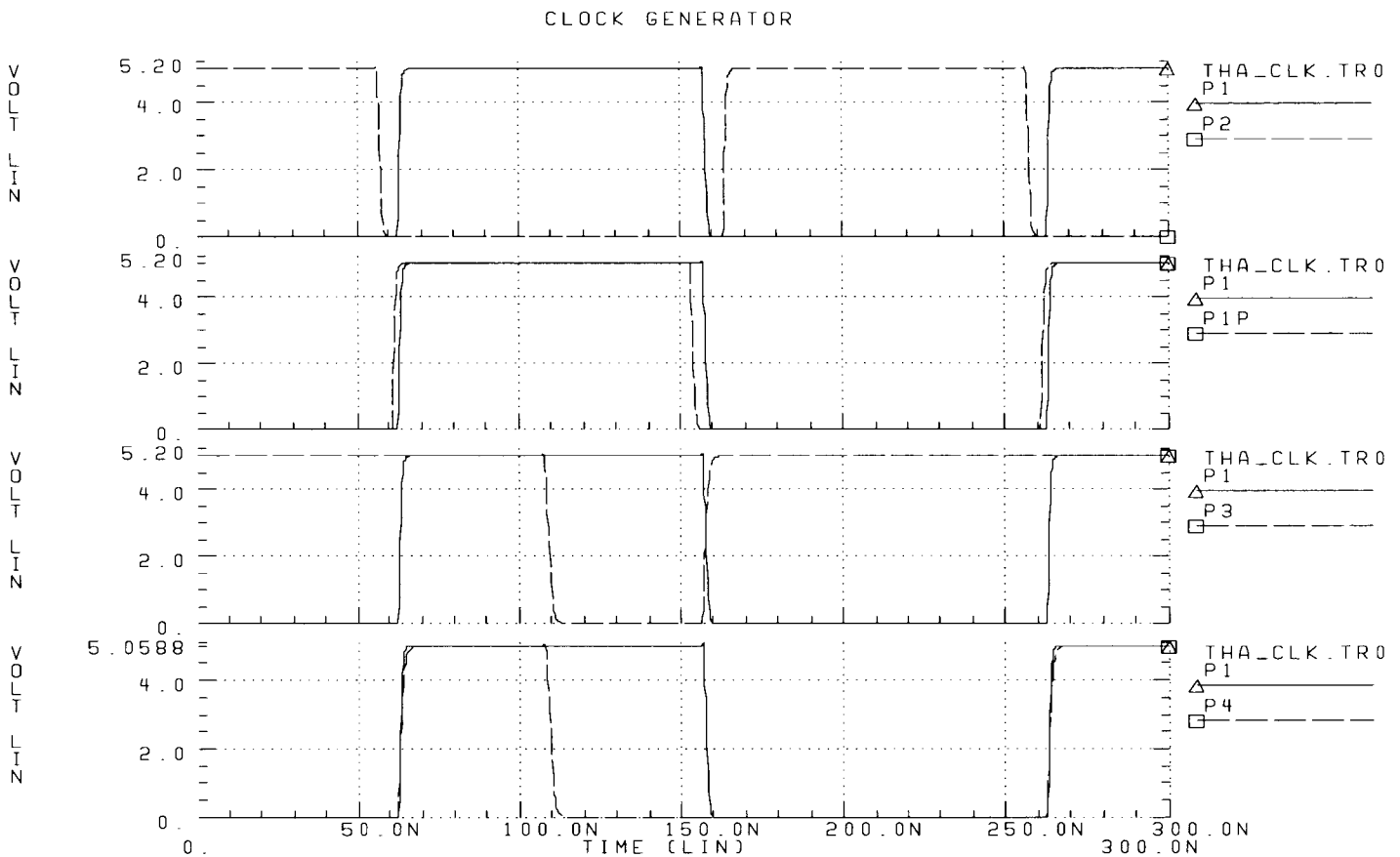


Figure 7.4: Clock signal waveforms.

bias current (node *b_dlay*) of the tunable delay cells. A typical clock waveform obtained from HSPICE simulation is shown in Figure 7.4.

7.3.2. Nicollini's S/H Stage

The fully-differential S/H circuit proposed in [30] by Nicollini, Confalonieri and Senderowicz was also implemented using the same op-amp as shown in Figure 7.2. For convenience, this circuit is referred to as Nicollini's S/H stage throughout this thesis. Figure 7.5 shows the circuit schematic. The capacitor size used was also 1 pF for all the capacitors except for the capacitors in the common-mode feedback circuit, whose value was 0.3 pF. Four-phase non-overlapping clock signals were used to reduce the signal-dependent charge-injection from the MOS switches.

7.3.3. Offset-Compensated S/H Stage

Figure 7.6 shows the schematic of a fully differential offset-compensated S/H stage based on the circuit in Figure 2.4b [13]. Four-phase non-overlapping clock signals were also used in this circuit.

7.4 Experimental Results

The S/H chip was fabricated in the Orbit 1.2 μm double-poly double-metal process. Figure 7.7 shows the die photo of the prototype chip.

Since both the input and output signals for the S/H circuits are analog ones, testing the accuracy of these circuits is very difficult [37]. A good way to measure the accuracy of the S/H circuits is to digitize the analog output, then evaluate it in the digital domain. However, due to the lack of a high-performance A/D converter, this test approach was not used. Instead, the analog output waveforms were observed using an oscilloscope and the

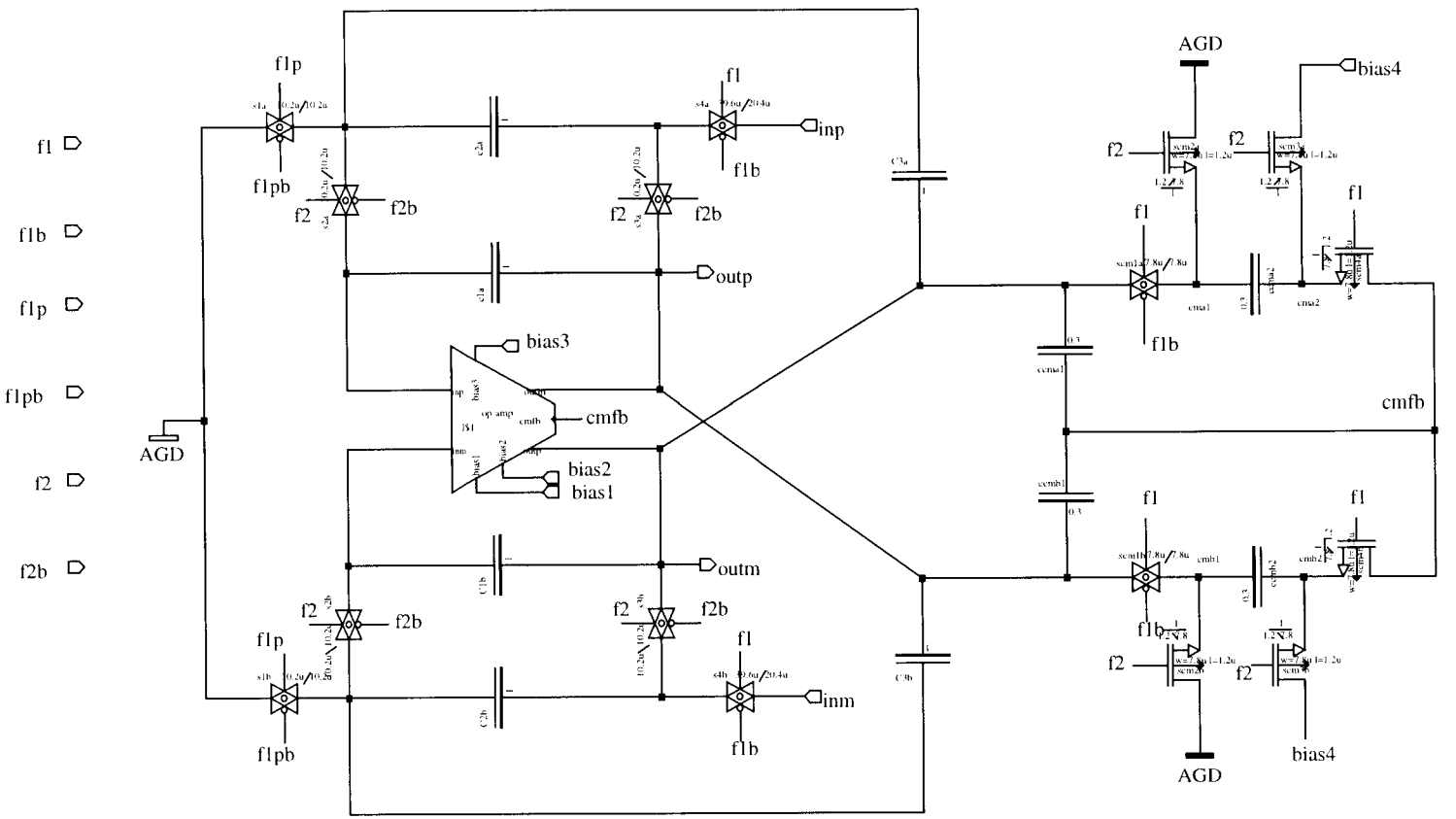


Figure 7.5: Nicollini's S/H stage.

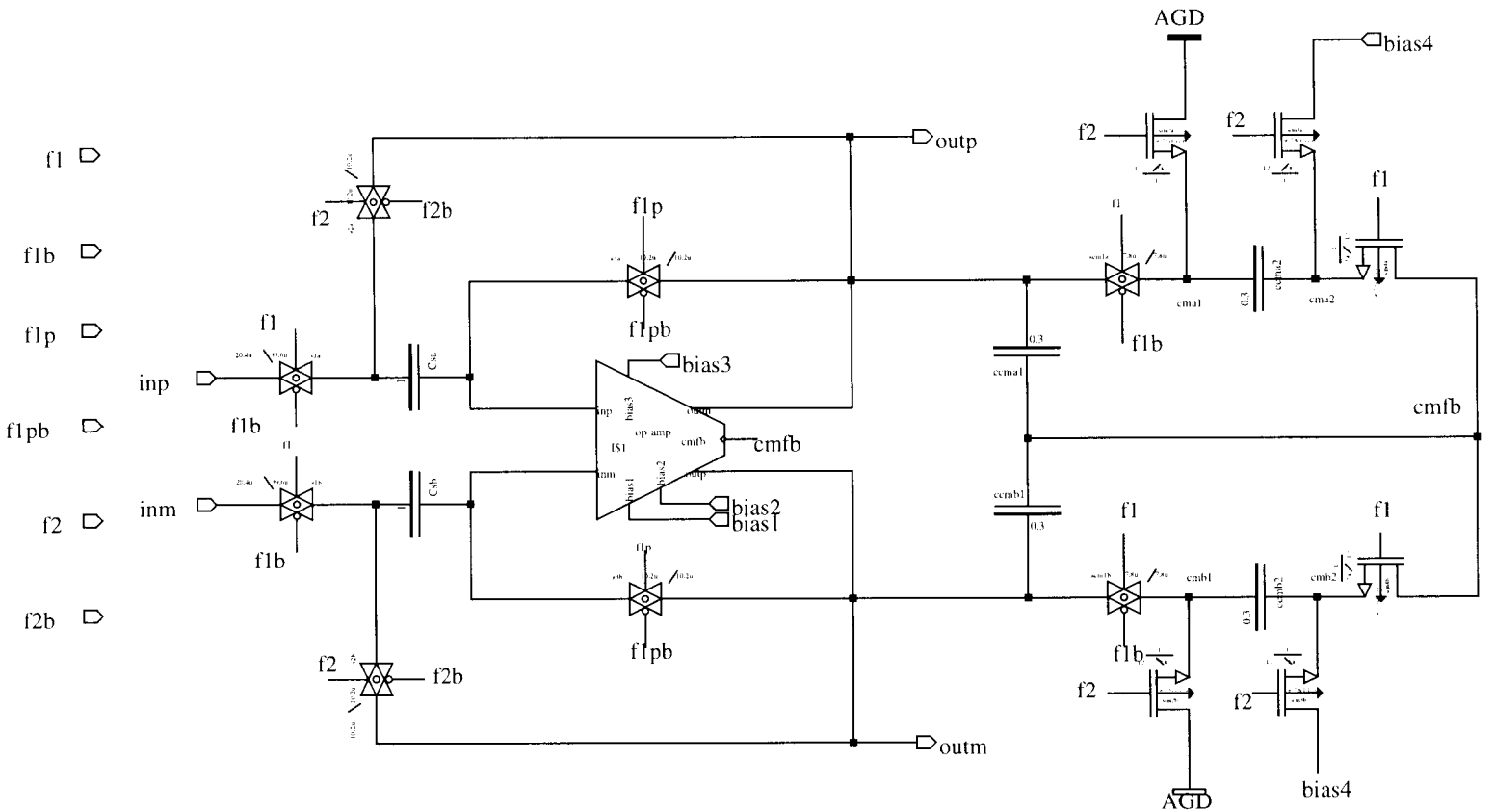


Figure 7.6: Offset-compensated S/H stage.

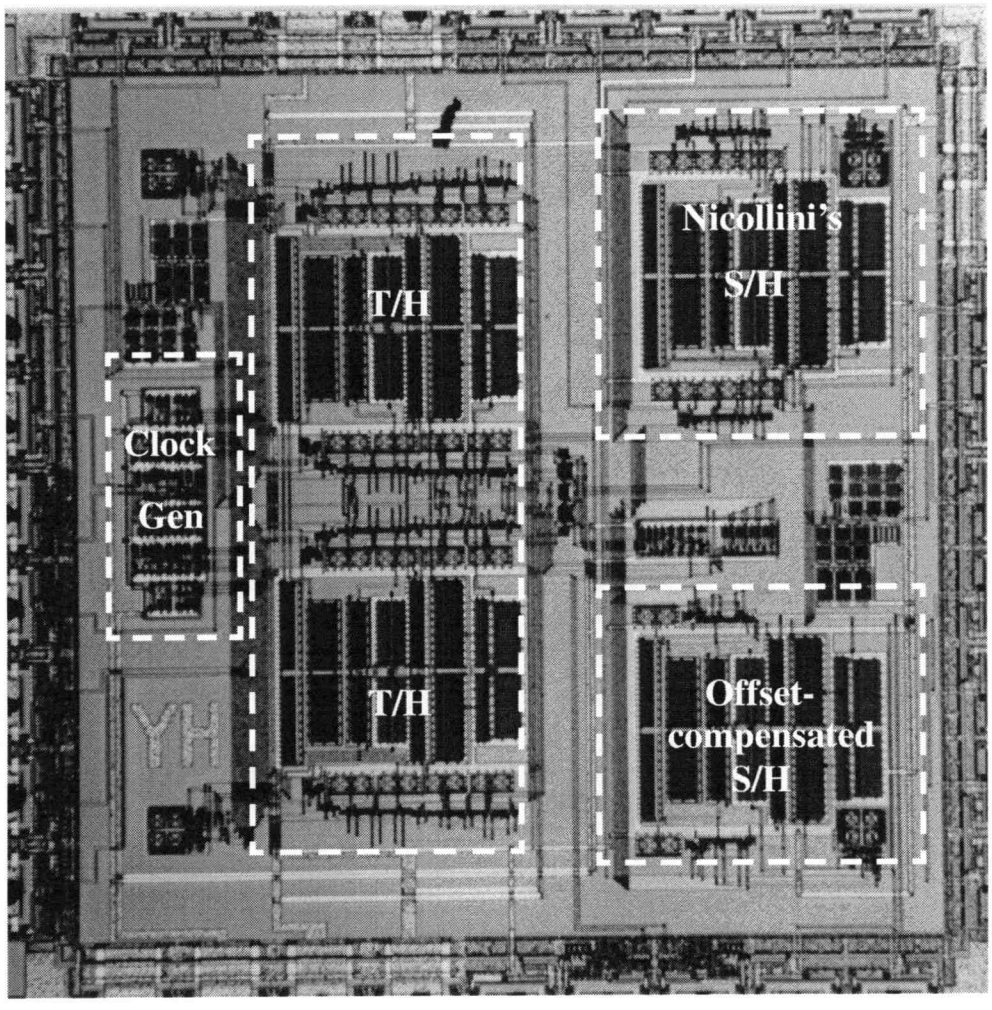


Figure 7.7: Die microphotograph of the S/H chip.

output spectra were measured using a spectrum analyzer. Figure 7.8 shows the test setup for this chip. Since the spectrum analyzer evaluates the entire waveform, the slewing and settling part of each output period and the output during the invalid clock phase were all taken into account, and thus gives a pessimistic estimation of the accuracy of the analog sampled-data output.

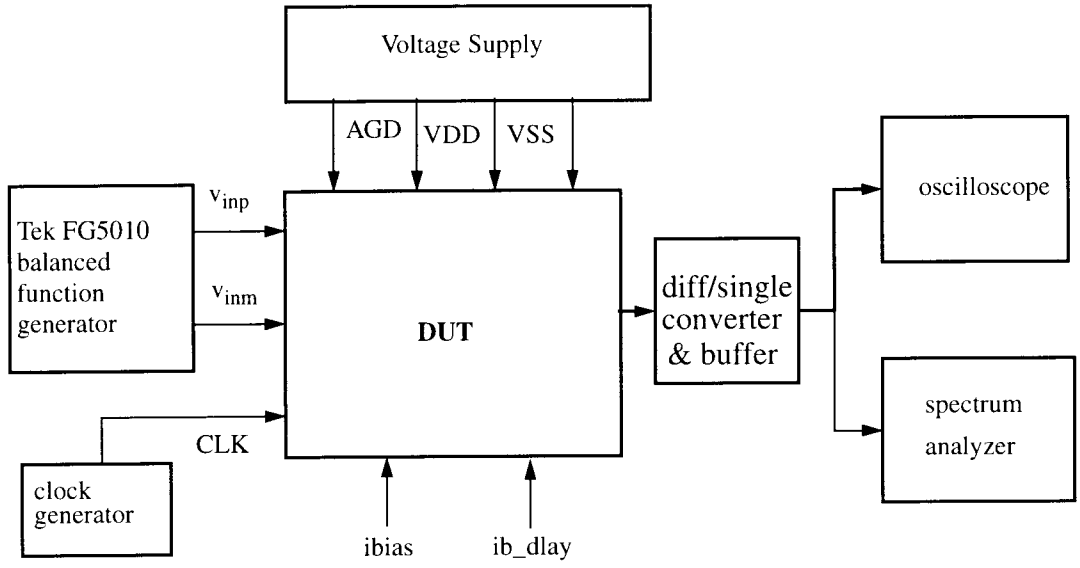


Figure 7.8: Test setup for the S/H chip.

Various input signal frequencies and sampling rates were applied to the three S/H stages implemented on the chip. Based on the observed output waveform from the oscilloscope, when an oversampling ratio of 2 was kept during the frequency sweep, the highest sampling rate achieved by the predictive S/H stage was 4 MHz, and 3 MHz for Nicollini's S/H, and 2 MHz for the offset-compensated S/H. However, due to the difficulties of capturing the time-domain waveforms and buffering the output signal without introducing too much extra distortion, only the operation at lower frequencies was documented. The time-domain waveforms of the three S/H stages were captured from the oscilloscope and are shown in Figs 7.9 - 7.13. The output spectrum of the predictive S/H in "pingpong" structure is shown in Figure 7.14. The input signal was a 1 kHz sine-wave, and the sampling rate was 10 kHz. The spectrum shows that the highest (third-order) harmonic is about 75 dB below the fundamental. Figure 7.15 shows the output spectrum for Nicollini's S/H with the same input signal and the same sampling rate. The measured

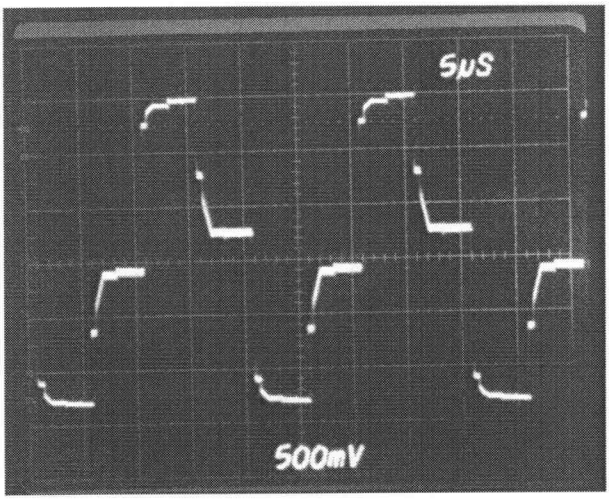


Figure 7.9: Track-and-hold stage output with a 50-kHz sine-wave input and a 200-kHz sampling rate.

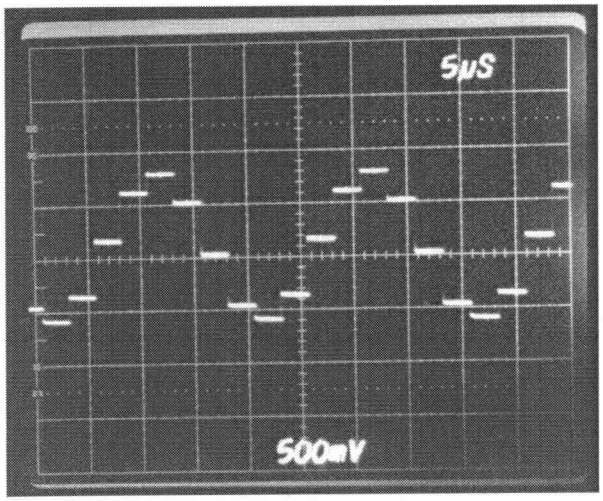


Figure 7.10: Output waveform of the "ping-pong" S/H output with a 50 kHz input and an effective sampling rate of 400 kHz.

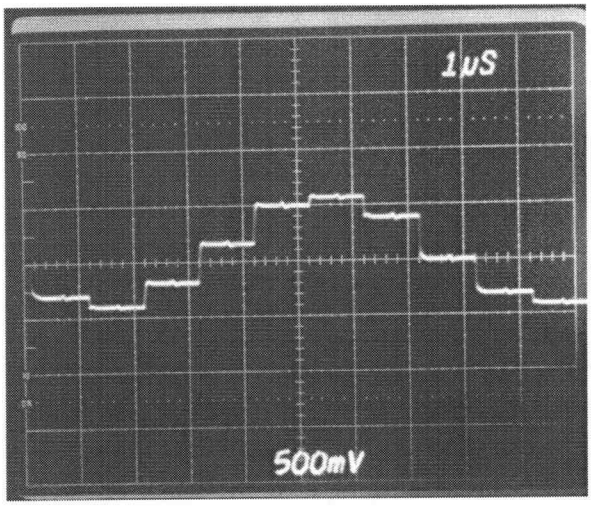


Figure 7.11:Output waveform of the "ping-pong" S/H output with a 125 kHz input and an effective sampling rate of 1 MHz.

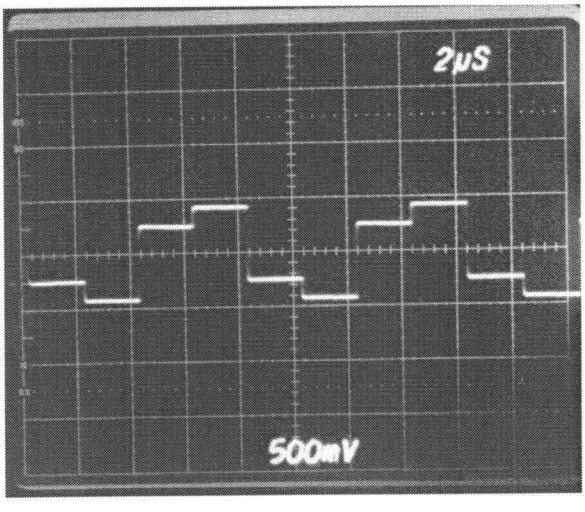


Figure 7.12:Output wave-form of Nicollini's S/H stage with a 125 kHz input and a 500 kHz sampling rate.

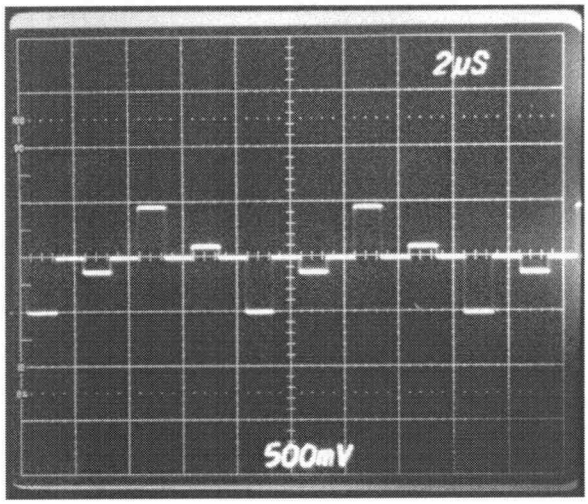


Figure 7.13:Output wave-form of the offset-compensated S/H stage with a 125 kHz input signal and a 500 kHz sampling rate.

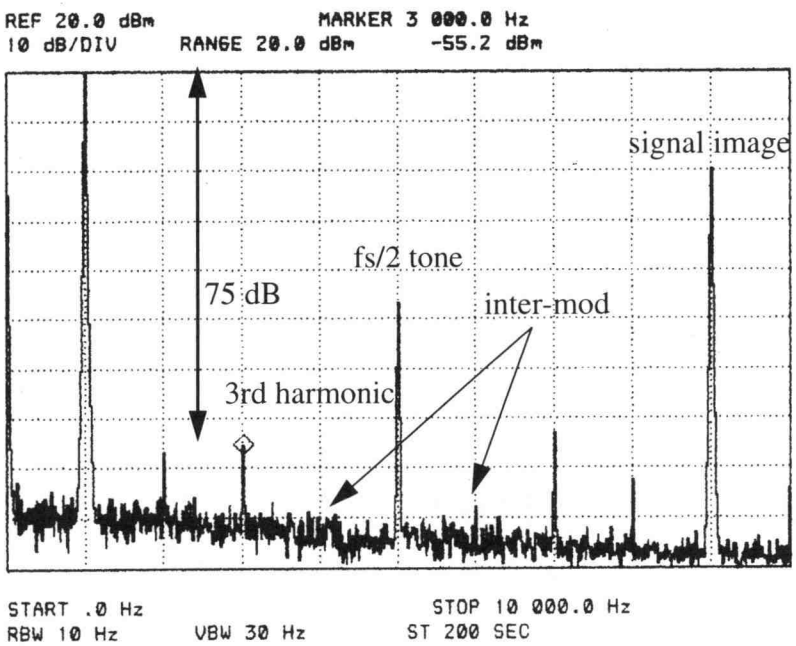


Figure 7.14:The output of the two predictive T/H stages operating in a "ping-pong" structure. The input signal frequency was 1 kHz and the sampling frequency was 10 kHz.

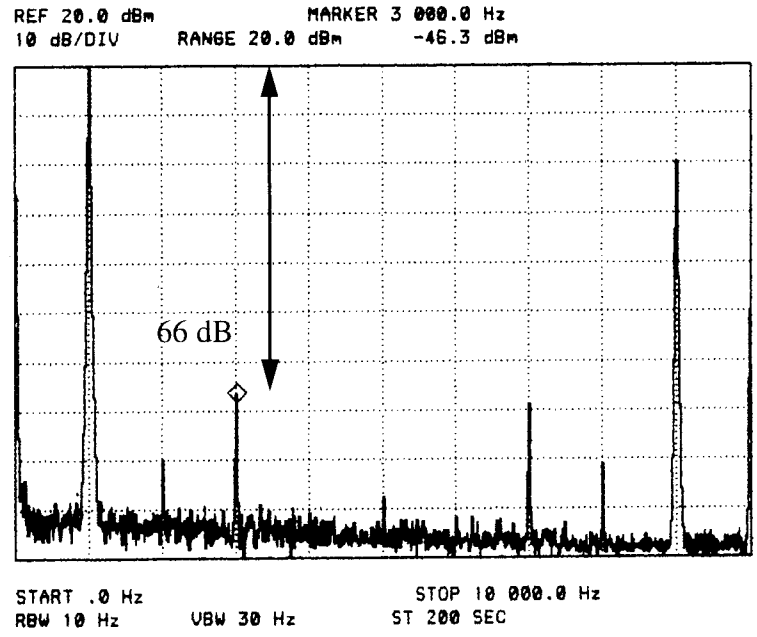


Figure 7.15:Output spectrum of Nicollini's S/H stage with a 1 kHz sine-wave input and a 10 kHz sampling rate.

9 dB improvement has been achieved by using the predictive CDS technique. Notice also, in Figure 7.14, the intermodulation terms are nearly 90 dB below the signal. This indicates that the two T/H stages in the "ping-pong" structure are very well matched when the CDS compensation technique is applied.

The $f_s/2$ tone shown in Figure 7.14 is introduced by the dc mismatch between the two T/H stages operating in "ping-pong" structure. (See "Other Error Sources in T/H Circuits" on page 36.) The mismatch of the signal-independent charge-injection between the two differential signal paths in each T/H stage results in a dc offset at each of the T/H outputs. The mismatch of this dc offset, together with the mismatch of the residual op-amp dc offset, is responsible for the $f_s/2$ tone. This is verified in the test that the magnitude of this $f_s/2$ tone remained unchanged when signal magnitude was varied, and the magnitude

of the $f_s/2$ tone changed when the clock supply voltage was changed. This fixed $f_s/2$ tone is usually not very important in many applications.

7.5 Conclusions

Two predictive gain- and offset-compensated track-and-hold stages were implemented in Orbit 1.2 μm process. They can be switched to operate individually or in a "ping-pong" structure. To compare the circuit performance with other existing S/H circuits, two other S/H stages were also implemented on the prototype chip using the same op-amp and tested under the same condition. The measured results show that the proposed T/H stage is superior in both speed and accuracy.

Due to the large capacitive loads seen by a stand-alone S/H stage, it is anticipated that the proposed circuits can operate at a much higher speed when used as part of an A/D on the same chip.

Chapter 8. Experimental Results On Reduced Harmonic Distortion in Circuits with Correlated Double Sampling

To verify the analytical and simulation results for reduced harmonic distortion in gain-compensated SC circuits, three SC amplifier stages were chosen for the experiments. In this Chapter, the experimental results obtained from a prototype chip are shown. The chip contains three SC amplifier stages and was fabricated in the Orbit 1.2 μm double-poly double-metal process. Measured results show an improvement of more than 10 dB in S/THD for the circuits with gain-compensated CDS scheme compared to the circuit without gain-compensation.

8.1 Prototype Chip Description

The chip contains three fully-differential SC amplifiers: an offset-compensated SC amplifier based on the circuit in Figure 2.4a, a narrow-band gain- and offset-compensated SC amplifier based on the circuit in Figure 2.5 and a wide-band gain- and offset-compensated SC amplifier based on the circuit in Figure 3.13 [21]. All three SC amplifiers were implemented using the same op-amp shown in Figure 7.2, and with a selectable voltage gain of 2 or 4. The schematics of the implemented circuits together with their common-mode feedback circuits are shown in Figs. 8.1 - 8.3. The input capacitors used for all three gain stages were 2 pF. According to Eq. (5.18), this corresponds to a differential kT/C noise level of -79 dBV when a voltage gain of 2 is selected.

Figure 8.4 shows the four-phase non-overlapping clock generation circuit. By enabling or disabling the clock control signal *clk_ctl*, it generates clock signals for delaying or non-delaying operation for the narrow-band GOC SC amplifier and the wide-band GOC amplifier.

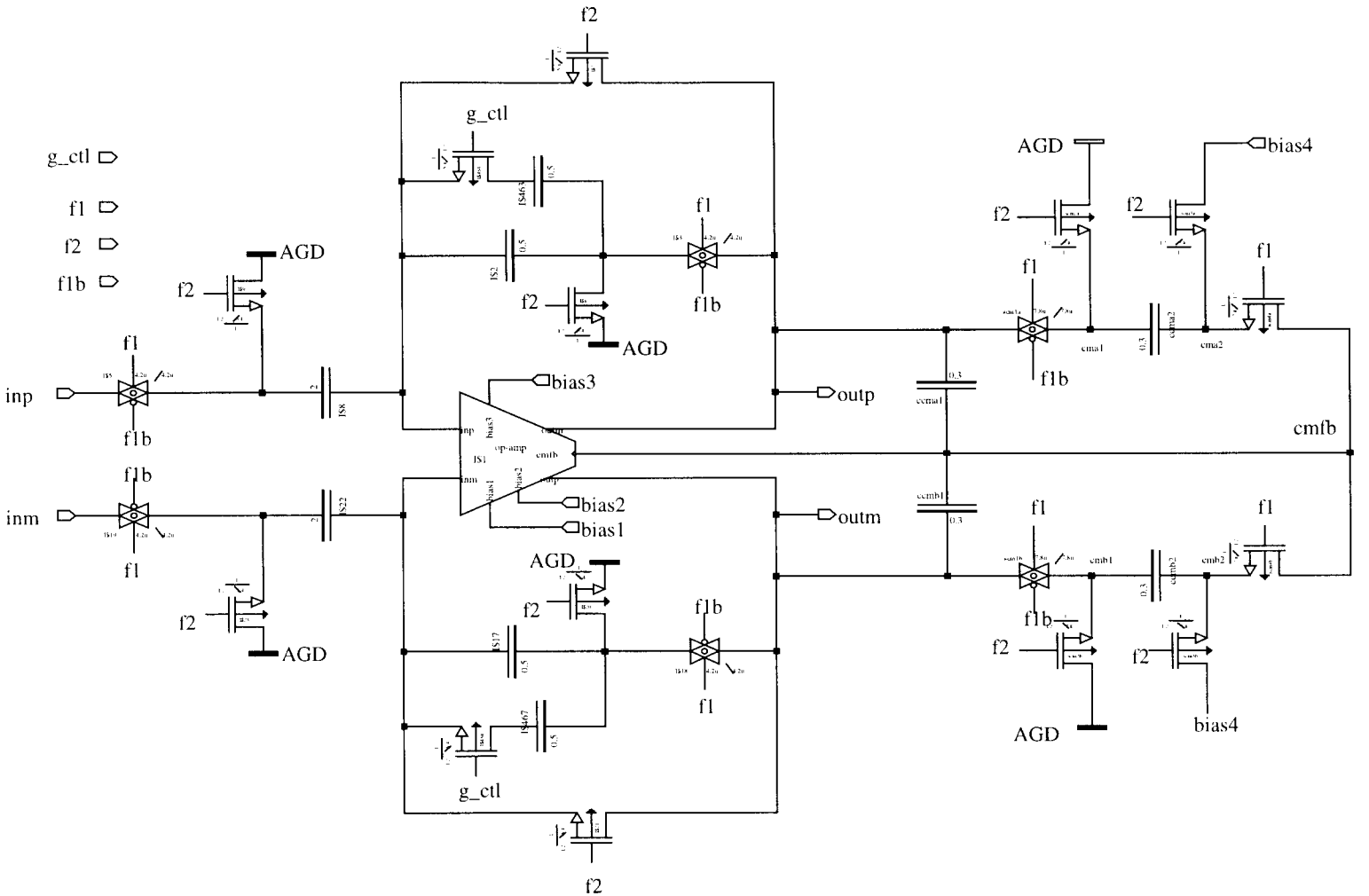


Figure 8.1: Offset-compensated SC amplifier.

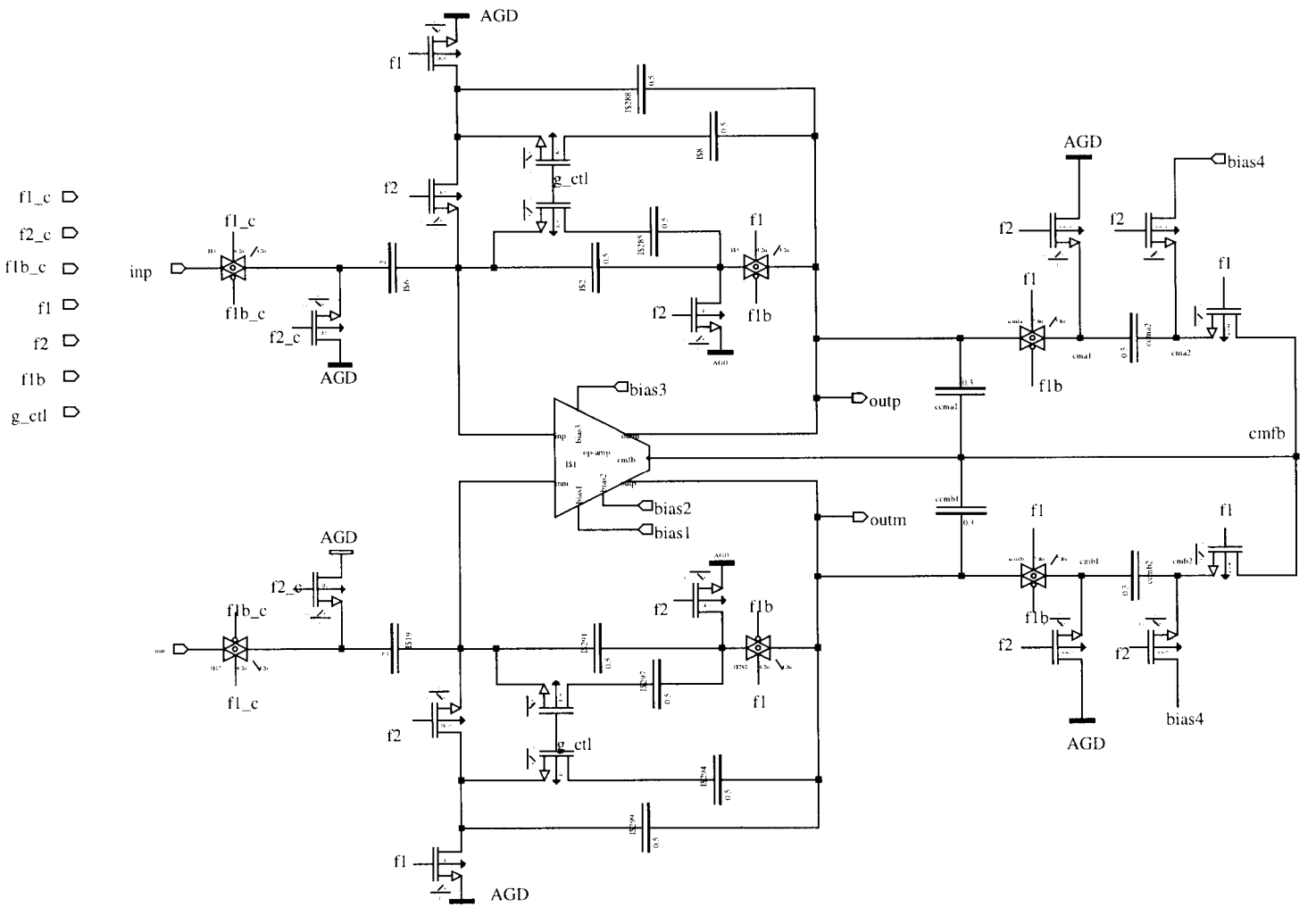


Figure 8.2: Narrow-band gain- and offset-compensated SC amplifier.

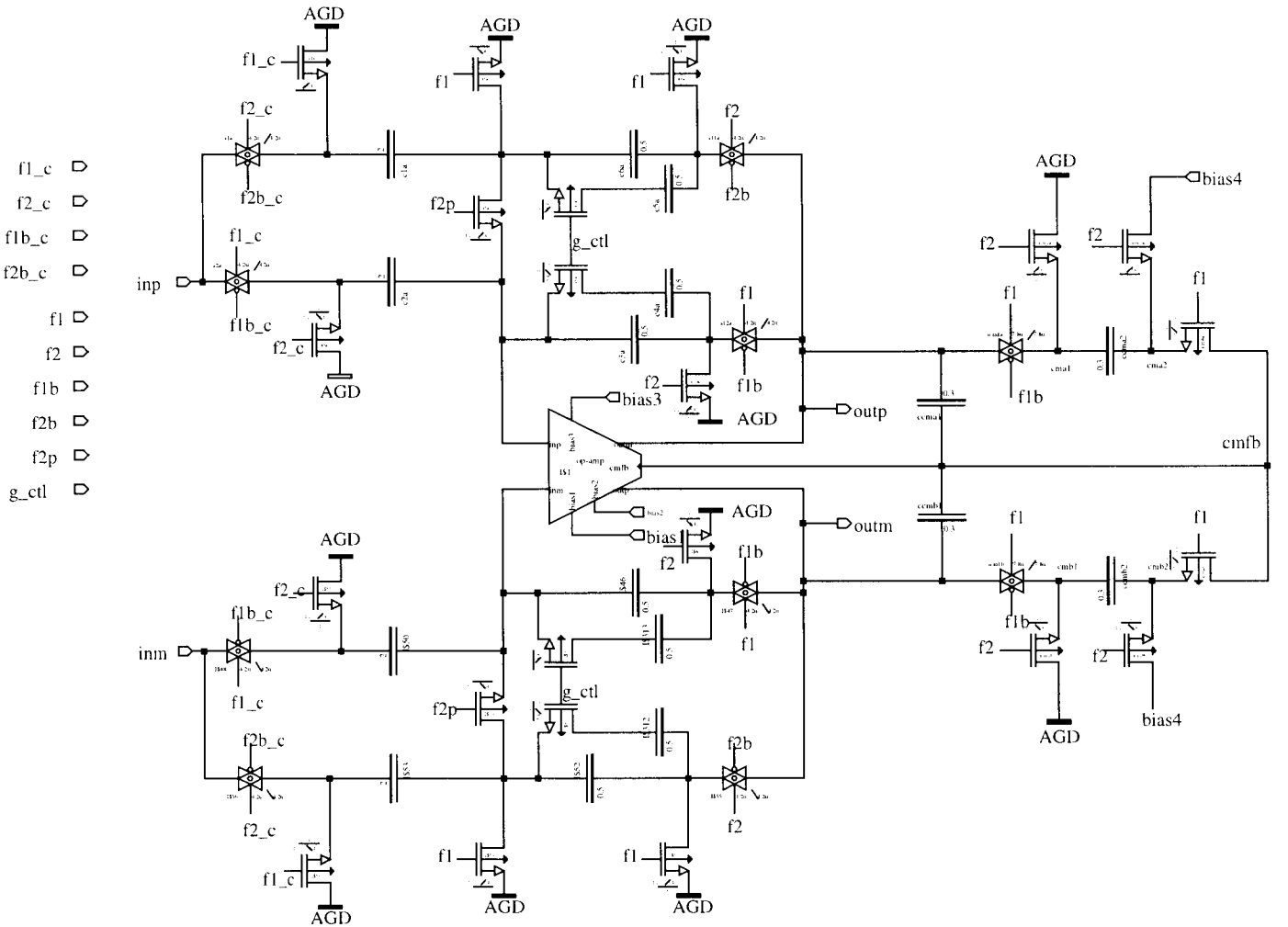


Figure 8.3: Wide-band gain- and offset-compensated SC amplifier.

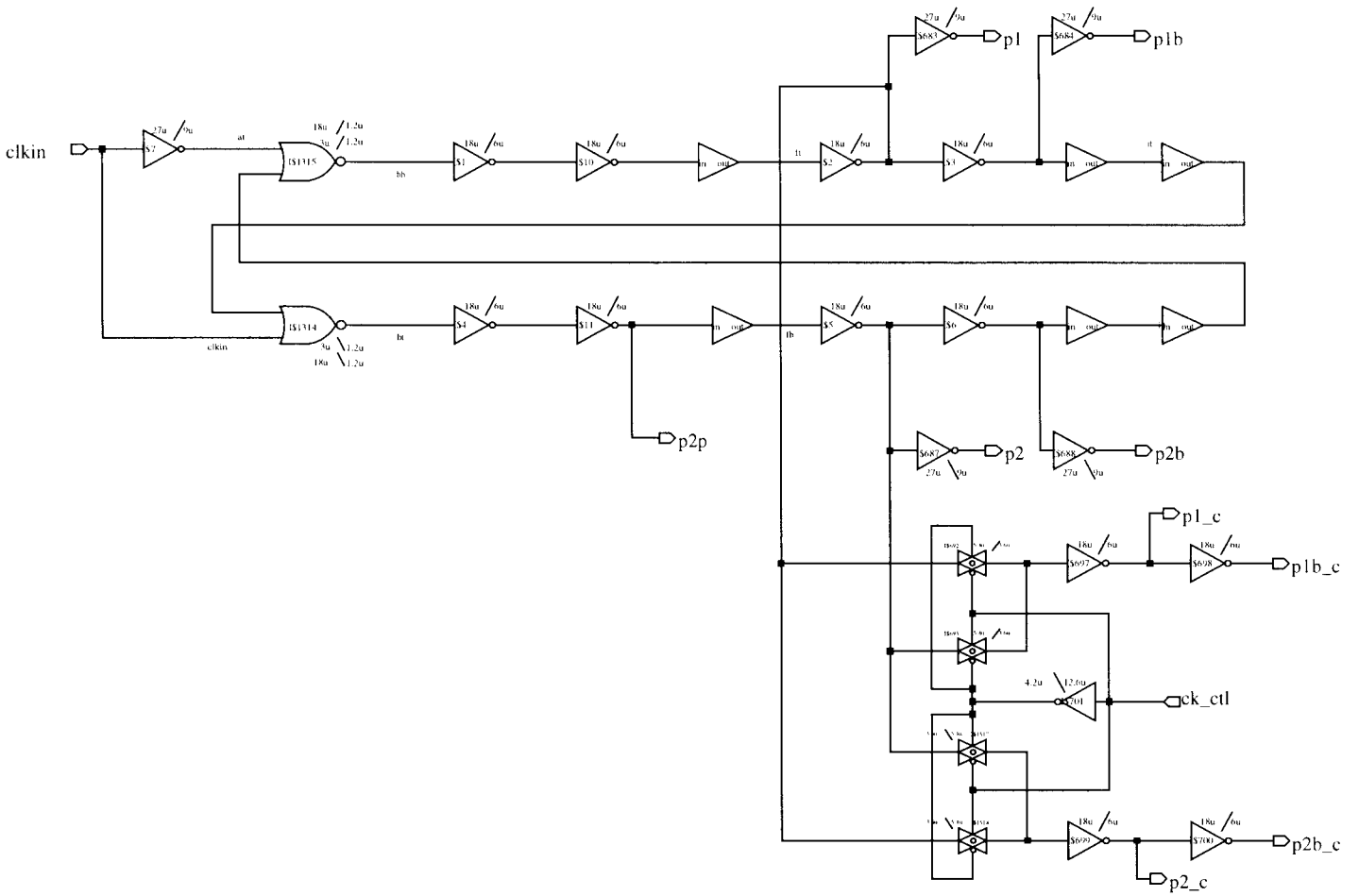


Figure 8.4: Clock generator.

8.2 Experimental Results

The prototype chip was fabricated in Orbit 1.2 μm process. The chip photo is shown in Figure 8.5.

The test setup for this chip is the same as that for the S/H chip shown in Figure 7.8. As shown in Figure 2.5, the narrow-band SC amplifier operates as a non-delaying gain

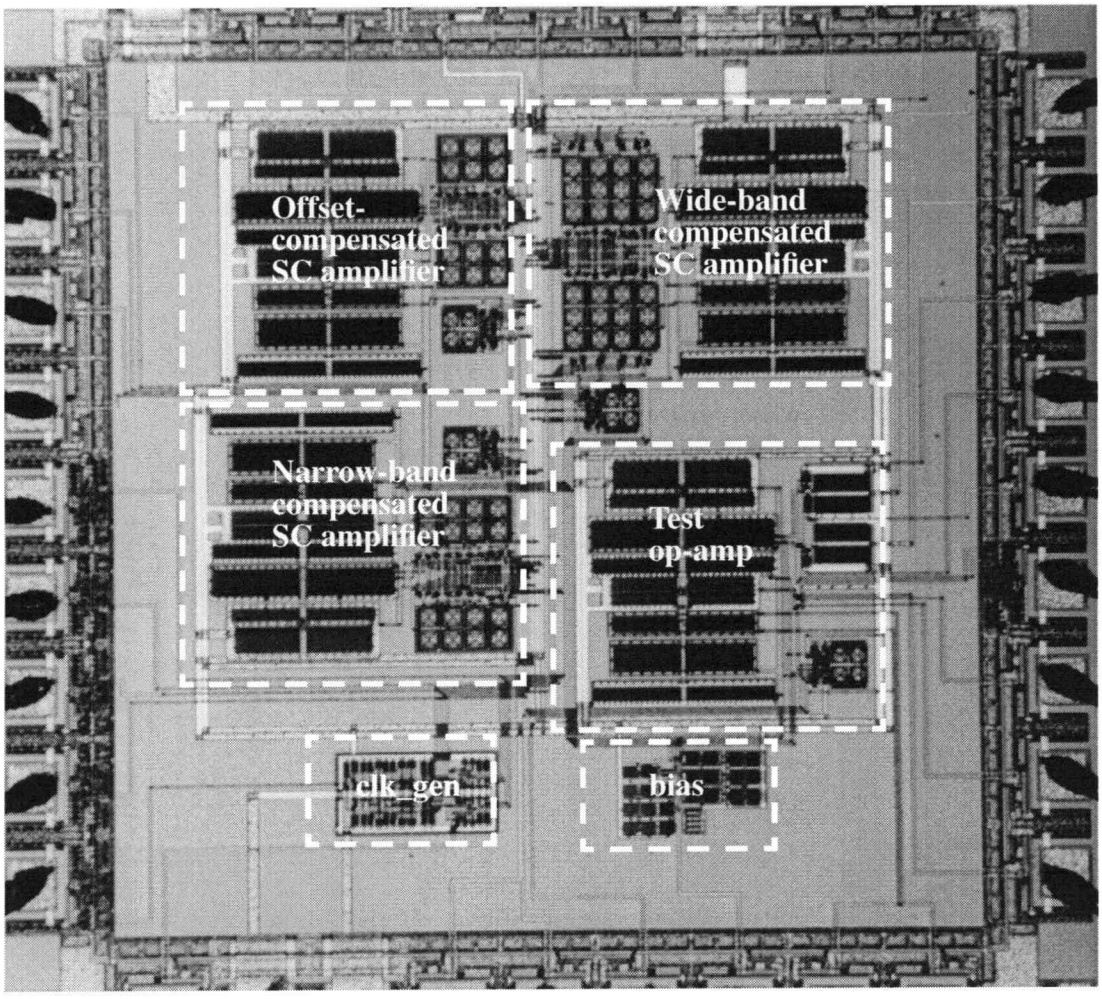


Figure 8.5: Microphotograph of the SC amplifier chip.

stage when the parenthesized clock phases are used, and operates as a delaying gain stage when the unparenthesized clock phases are used. The wide-band compensated SC amplifier can also be selected to operate in its delaying mode or non-delaying mode as shown in Figure 3.13, with the parenthesized or unparenthesized clock phases. A typical set of time-domain responses is shown in Figs. 8.6 - 8.10.

To compare the circuits' performance in S/THD, the three SC amplifiers were all tested using an input signal frequency of 6 kHz, and a voltage gain of 4. Their output spectra were then measured using the spectrum analyzer. While keeping the same input signal, two clock rates, (50 kHz and 500 kHz) were applied to obtain the measurements for when the oversampling ratio is low and high. A typical set of the output spectra is show in Figs. 8.11 - 8.19. Table 8.1 shows a summary of the measured S/THD for the circuits under various operation conditions.

Table 8.1: Measured S/THD for the SC amplifiers

S/THD	offset-compensated	narrow-band compensated	wide-band compensated
non-delaying, f_s = 50 kHz	63 dB	55 dB	60 dB
non-delaying, f_s = 500 kHz	45 dB	68 dB	63 dB
delaying, f_s = 50 kHz	N/A	34 dB	48 dB
delaying, f_s = 500 kHz	N/A	63 dB	63 dB

From the measured data, the following conclusions can be drawn:

1. Comparing the non-delaying narrow-band SC amplifier with the offset-compensated SC amplifier when $f_{in}/f_s = 6 / 500$, an improvement of 23 dB was achieved in S/THD, and the third-order harmonic distortion was about 11 dB lower. This shows that the gain-compensated CDS scheme greatly reduces the signal distortion.

2. When $f_{in}/f_s = 6 / 50$ (Figure 8.13), the non-delaying narrow-band SC amplifier gives 13 dB lower S/THD than when $f_{in}/f_s = 6 / 500$ (Figure 8.14). This shows that the narrow-band compensated SC amplifier does not compensate for the finite op-amp gain effect when the signal frequency is high compared to the clock frequency, and thus verifies the analytical and simulation results presented in Chapter 2 and Chapter 3.

3. The minor difference of 3 dB in S/THD for the wide-band compensated SC amplifier when $f_{in}/f_s = 6 / 50$ (Figure 8.17) and when $f_{in}/f_s = 6 / 500$ (Figure 8.19) indicates that the circuit compensates for the finite op-amp gain effect in a wide frequency range. However, its gain compensation at lower frequency is not as effective as that of the narrow-band compensated one. This conclusion again agrees with the simulation results shown in Figure 3.16.

4. Large second-order harmonic distortion is shown in the output of the offset-compensated SC amplifier when clock frequency is high. This is resulted from the fact that the circuit resets in every other clock period, and the slewing of the differential-to-single-ended conversion amplifier introduces a large distortion when the entire waveform is analyzed.

The differences in the measured S/THD among the SC amplifiers are not as large as those shown in the simulation results of Table 3.1. This is because the spectrum analyzer uses the entire waveform for spectrum analysis rather than doing impulse sampling as was done in simulation. Also for both two gain-compensated SC amplifiers, the outputs are gain-compensated only during one clock period, and are not gain-compensated in every other clock period. Thus, the resulting spectra contained "corrupted information", including the nonlinear slewing and settling as well.

8.3 Conclusions

Experiments were performed to investigate the reduced harmonic distortion in circuits with gain-compensated correlated-double-sampling. The measurement results confirm that gain-compensated schemes greatly suppress the signal harmonic distortion. Narrow-band compensated circuits reduce the finite op-amp gain effect (and thus reduce harmonic distortion) only at lower frequency, and the wide-band (predictive) compensated ones provide gain compensation over the entire frequency range.

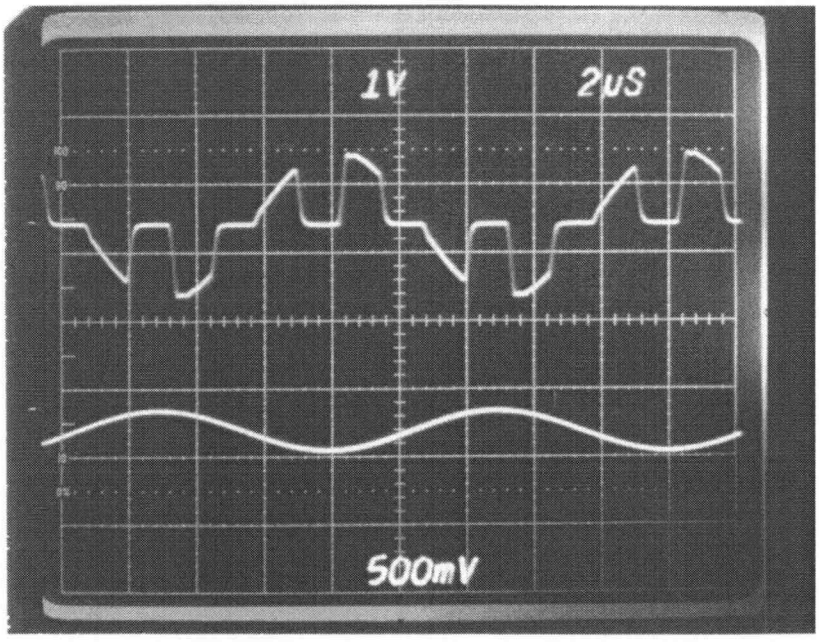


Figure 8.6: Signal waveforms of the offset-compensated SC amplifier. The upper curve is the output signal and the lower curve is the input signal.

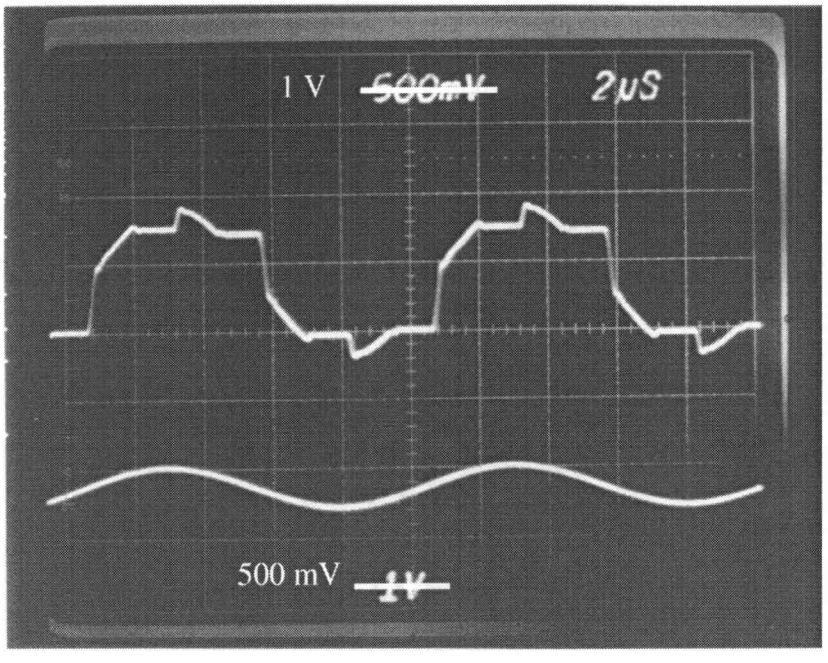


Figure 8.7: Output and input waveforms of the narrow-band compensated SC amplifier, when non-delaying operation was selected.

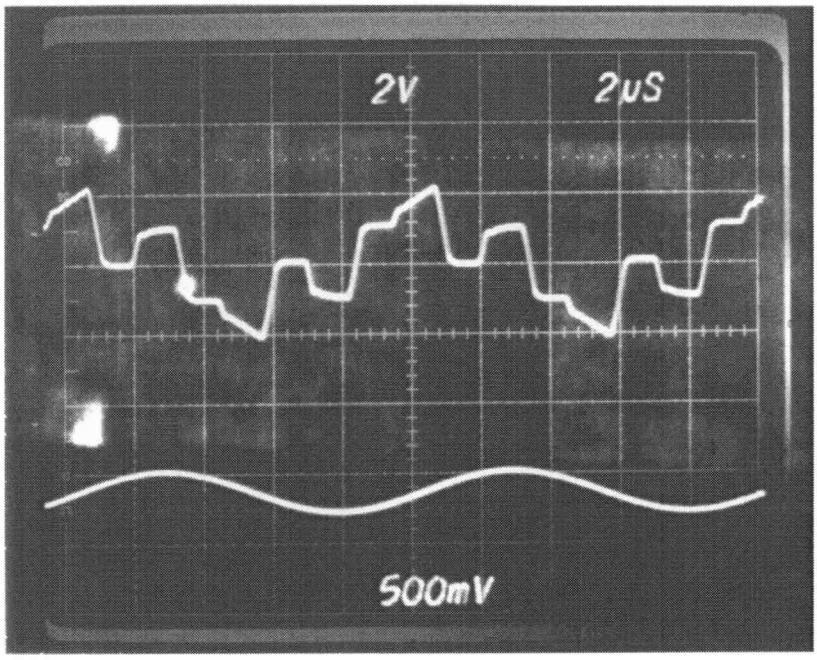


Figure 8.8: Output and input signal waveforms of the narrow-band compensated SC amplifier when delaying operation was selected.

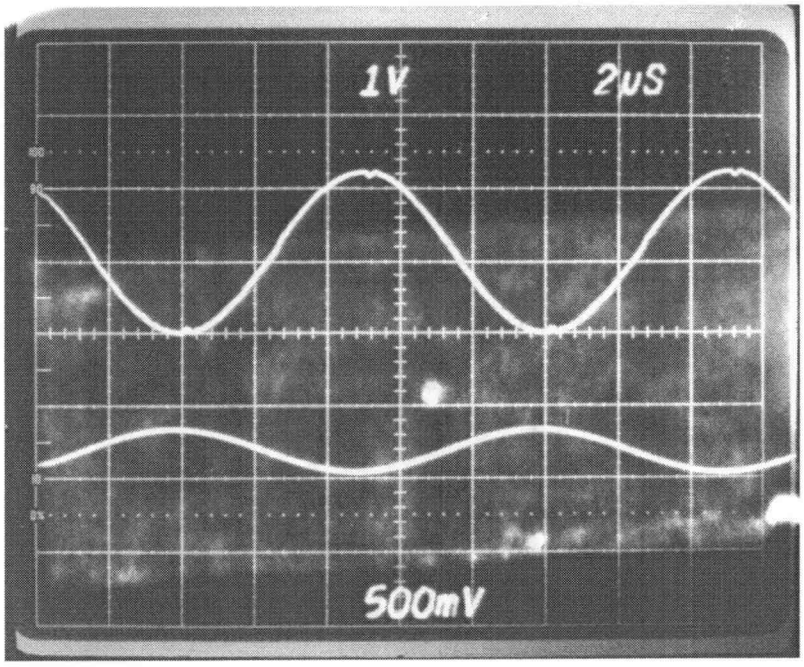


Figure 8.9: Output and input signal waveforms of the wide-band compensated SC amplifier when non-delaying operation was selected.

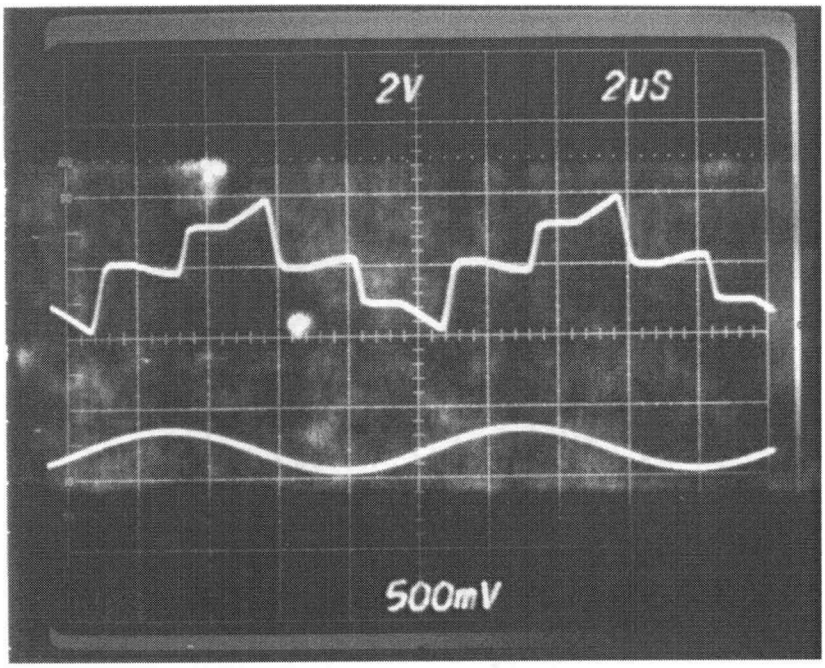


Figure 8.10:Output waveform for the wide-band compensated SC amplifier when delaying operation was selected.

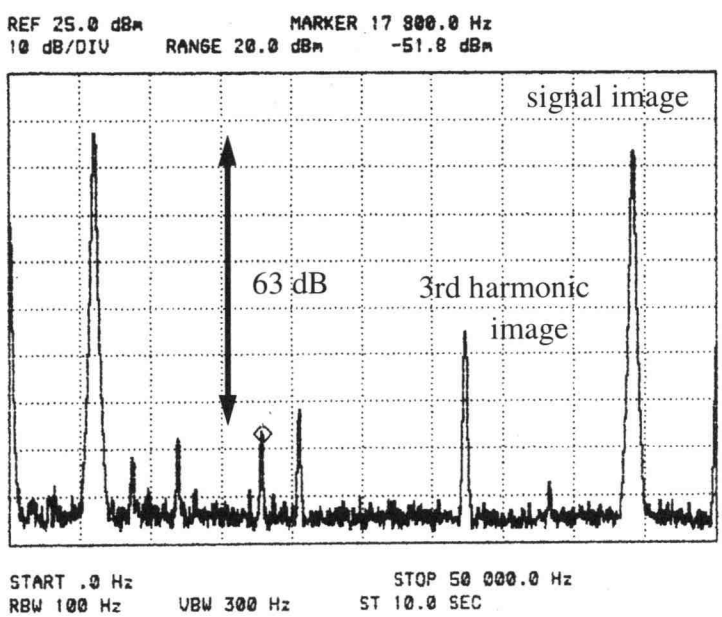


Figure 8.11:Output spectrum of the offset-compensated SC amplifier with a clock frequency of 50 kHz (non-delaying).

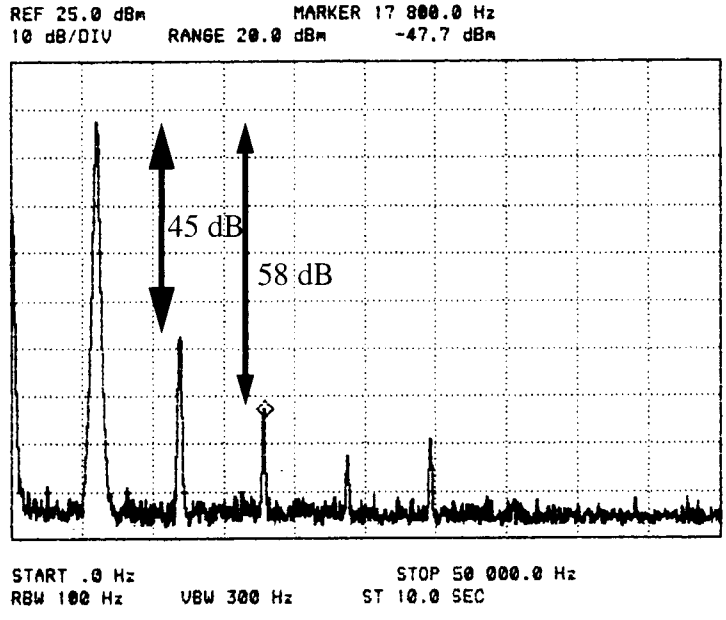


Figure 8.12:Output spectrum of the offset-compensated SC amplifier with a clock frequency of 500 kHz (non-delaying).

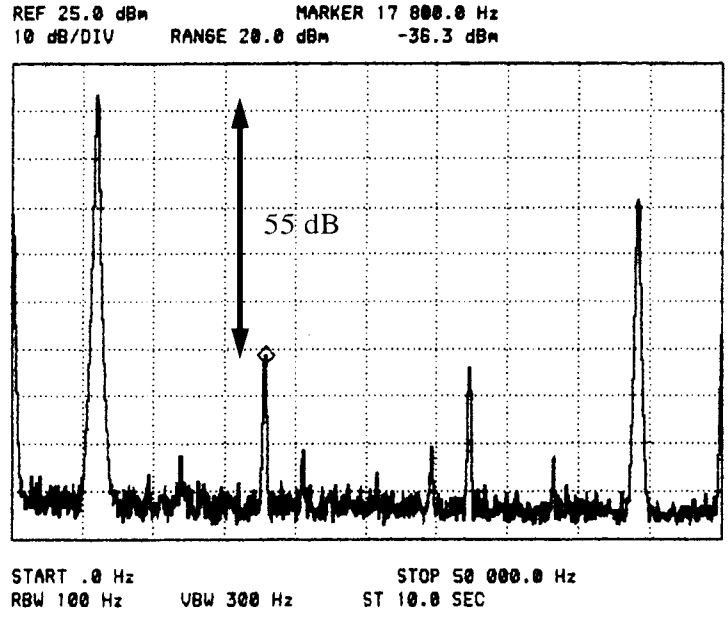


Figure 8.13:Output spectrum of the narrow-band compensated SC amplifier in non-delaying operation with a clock frequency of 50 kHz.

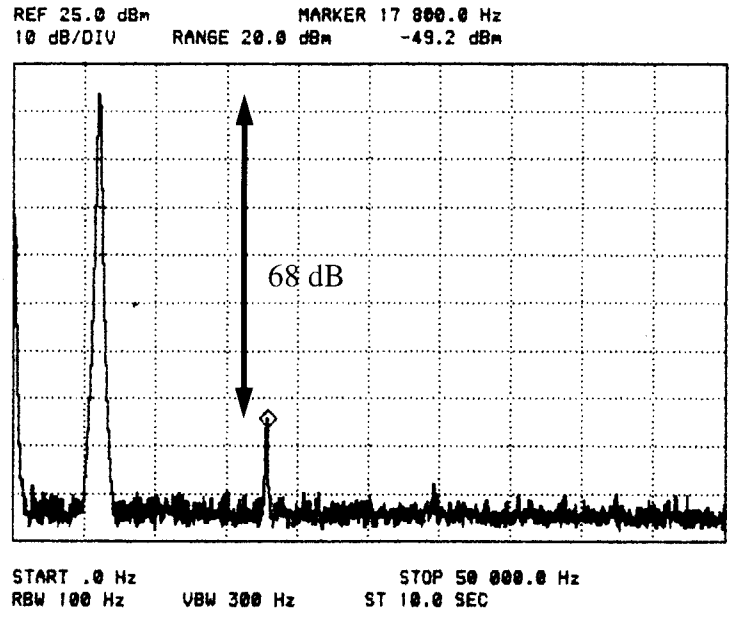


Figure 8.14:Output spectrum of the narrow-band compensated SC amplifier in non-delaying operation with a clock frequency of 500 kHz.

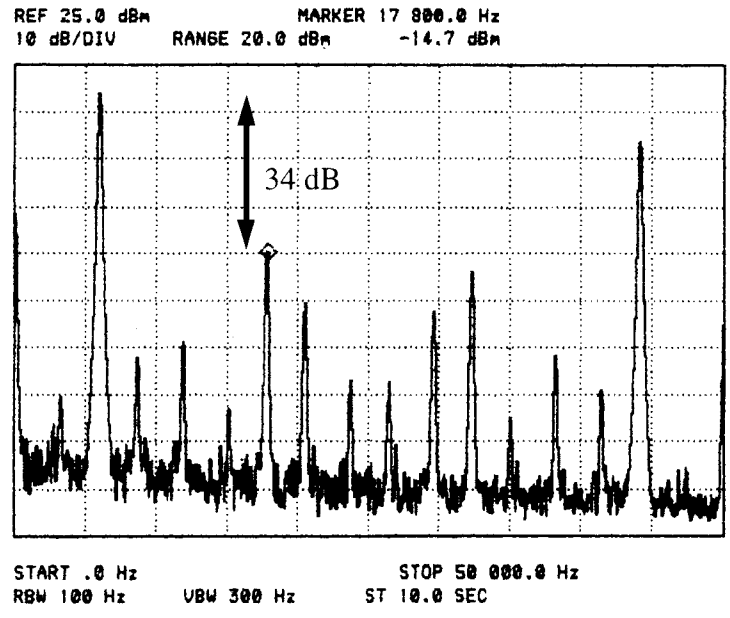


Figure 8.15:Output spectrum of the narrow-band compensated SC amplifier in delaying operation with a clock frequency of 50 kHz.

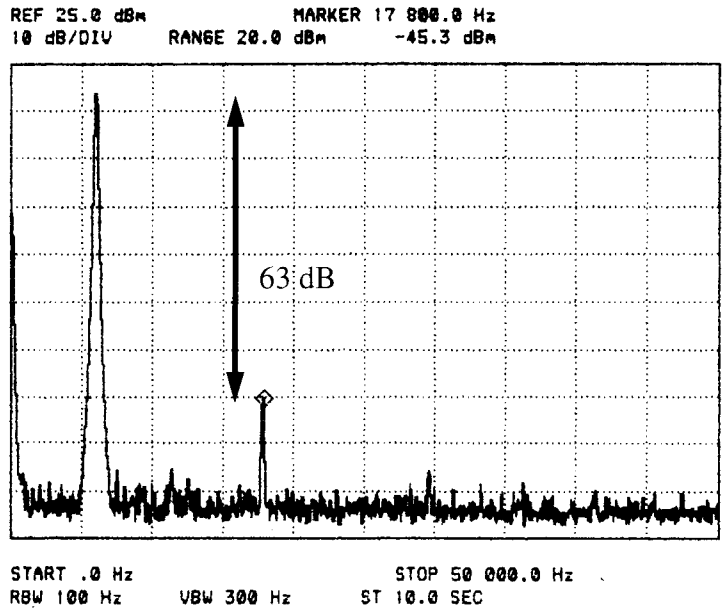


Figure 8.16:Output spectrum of the narrow-band compensated SC amplifier in delaying operation with a clock frequency of 500 kHz.

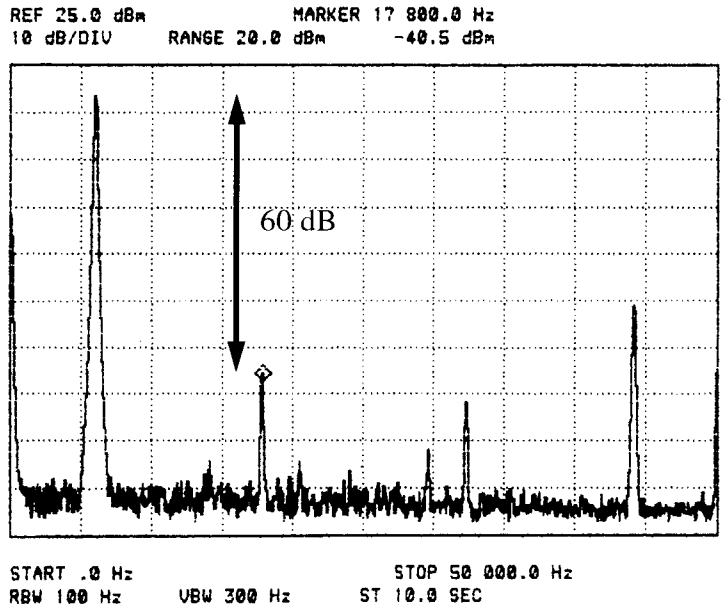


Figure 8.17:Output spectrum of the wide-band compensated SC amplifier in non-delaying operation with a clock frequency of 50 kHz.

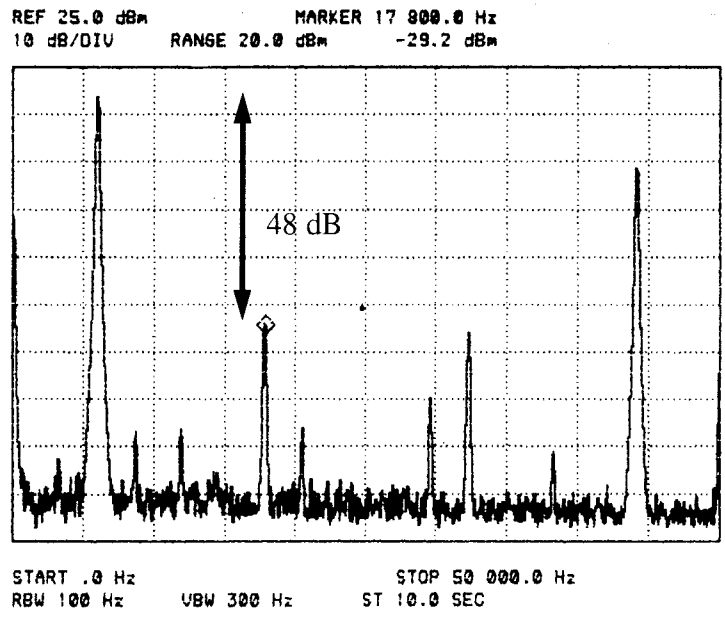


Figure 8.18:Output spectrum of the wide-band compensated SC amplifier in delaying operation with a clock frequency of 50 kHz.

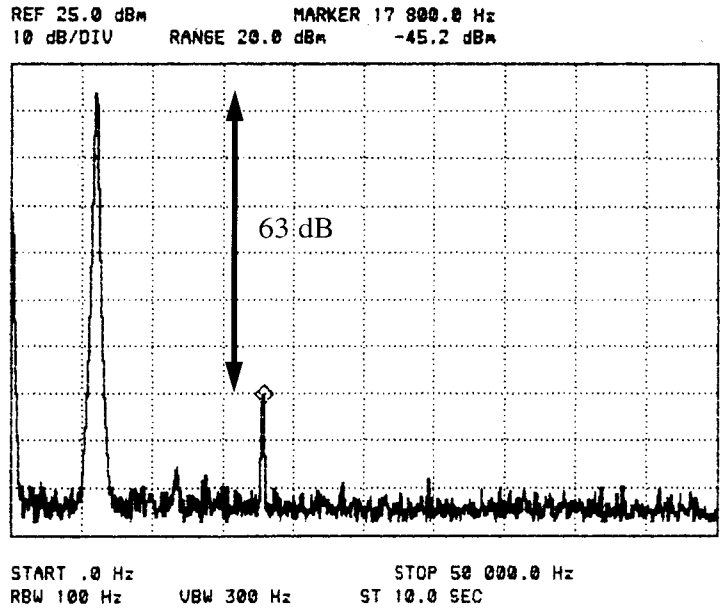


Figure 8.19:Output spectrum of the wide-band compensated SC amplifier in non-delaying operation with a clock frequency of 500 kHz. The resulting spectrum for delaying operation is almost the same in this measurement.

Chapter 9. Summary and Future Work

9.1 Summary

In this dissertation, techniques are proposed to compensated for two major error sources in high-performance SC circuit design: the op-amp gain nonlinearity and capacitor nonlinearity. Many associated topics have also been examined in detail. These include the following:

1. The principle of correlated-double-sampling technique, and the concept of predictive correlated-double-sampling.

2. Analysis of the effects of op-amp gain nonlinearity in SC circuits and comparison of S/THD performance among various SC circuits. Then superior performance of predictive CDS was demonstrated.

3. Analysis of the effects of capacitor nonlinearity in SC circuits, and techniques which reduce such effects.

4. Design issues for digital-process-compatible fully-differential op-amp.

5. kT/C noise analysis for SC circuits with correlated double sampling.

The prototype chip of an all-MOSFET delta-sigma ADC described in this dissertation has the largest dynamic range and the lowest signal distortion reported to date for switched-capacitor implementation in basic CMOS process. Also the prototype chip of the proposed T/H stage can operate at a higher speed with higher accuracy compared to existing S/H stages when they are implemented using the same elements and operate under

the same condition. Finally, the experimental results obtained from the SC amplifiers chip show that using gain-compensated CDS schemes is an effective technique to reduce harmonic distortion. The measured results agree with the analytical and simulation results well.

9.2 Future Work

The all-MOSFET delta-sigma chip can be improved for better SNDR (signal to noise + distortion) by increasing the size of the input capacitors, so that the voltage swing at the input node can be reduced. Also, it would be interesting to place two modulators on the same chip, one using poly-poly capacitors and the other only MOSFET capacitors, and then compare their performances in terms of dynamic range and signal distortion.

The proposed techniques can be combined in a low-voltage (1.8 V) all-MOSFET design, where CDS is used to compensate for the finite op-amp gain effect and to reduce the harmonic distortion resulting from the op-amp.

The described design techniques for digital-process-compatible delta-sigma ADC can be further applied for SC filters, so that a complete voice-band CODEC can be implemented in basic digital CMOS process.

To overcome the testing problem encountered, an on-chip ADC can be implemented using the high-speed track-and-hold stage as the front stage. Also, MOSFET capacitors can be used in this circuit.

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APPENDIX

APPENDIX

Digital Data Acquisition

A digital signal acquisition facility is needed to feed the digital output of the modulator into the computer for the performance evaluation. The SSI (Synchronous Serial Interface) port of NeXT workstation [62] that controls the transmission of the serial data to or from the outside port is an interface that is suitable for this purpose [50]. It uses the Motorola DSP56000 Digital Signal Processing chip to control the operation of the interface [63]. To measure the delta-sigma ADC prototype chip, the asynchronous mode (SYN=0) is selected, with the external clock signal (connected to the SC0 pin) provided by a pulse generator. The two SSI control register A (CRA) and B (CRB) are set to 6030hex and 2410hex, respectively [50]. The SSI samples the data at the falling edge of the external clock.