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Title: Improved Design Techniques For Low-Voltage Low-Power Switched-Capacitor Delta-Sigma Modulators.

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This dissertation investigates the constraints which arise when switched-capacitor (SC) delta-sigma modulators are designed for low-voltage operation, targeting also low power dissipation, and proposes methods of improving the performance and optimizing for low power dissipation. This is accomplished by identifying critical elements whose performance can lead to increased power dissipation, as well as the fundamental limitations of available analog circuit techniques. A prototype was designed and fabricated, which reflected these findings, and therefore exhibited good performance and nearly optimum power dissipation.

One of the key performance parameters is the dc gain of the amplifier in the first stage; it should be high. This is necessary for high linearity and low quantization noise leakage. In low-voltage operation, it may become impractical to use conventional topologies employing cascoding techniques (e.g., folded-cascode) which provide high gain in one single stage. Rather, cascaded structures have to be used. The disadvantage of the latter is the necessity for frequency compensation which results in increased power dissipation. Hence, another objective of this work is to exploit techniques which compensate for the open-loop gain characteristic of the amplifier (dc gain and nonlinearity), thus permitting the utilization of single-stage low-gain topologies. Predictive correlated double sampling is one of such techniques and is analyzed in detail.

Improved Design Techniques For Low-Voltage Low-Power Switched-Capacitor Delta-Sigma Modulators

by

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Jorge Grilo, Author

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To my parents.

Aos meus pais.

Improved Design Techniques for Low-Voltage Low-Power Switched-Capacitor Delta-Sigma Modulators

1. INTRODUCTION

The rapidly decreasing minimum feature device size in CMOS technologies permits the integration of a larger number of devices, and hence more signal processing functions. Due to their low sensitivity to noise and process variations, digital signal processing (DSP) techniques have become a favorite in the implementation of such functions. Moreover, digital processors have achieved a state of significant sophistication and efficiency, which strongly supports the drive towards digital solutions. However, a fully digital implementation is usually not possible, since most signals occur in analog form. This places considerable emphasis on the implementation of the interfaces between the two worlds. The devices which implement these interfaces are called analog-to-digital (A/D), and digital-to-analog (D/A) converters (ADC's and DAC's, respectively). There are many requirements on these interfaces:

- They must be compatible with high-density integrated solutions, if possible in digital technologies.

- Many digital solutions require high-performance A/D converters, and possibly high-speed operation.

- The interfaces must dissipate low power, a particularly important aspect in portable communication devices.

- The utilization of submicron technologies forces the utilization of lower power supply voltages, which complicates all aspects of the design.

Various techniques have been proposed to implement A/D and D/A interfaces [1]. The choice of one over another depends on the application and the performance requirements for that application. Dynamic range (DR), linearity and speed are perhaps the most common parameters in the design of such systems. Delta-sigma modulation is a widely adopted technique in moderate-speed, high-performance applications. It permits relaxed component performance requirements, and can provide very high dynamic range for moderate-speed applications. The purpose of this work is not to study or analyze in detail the various methods of signal conversion, or even the structures employing the delta-sigma technique (the literature on this topic is vast [2][3]). Rather, we concentrate on two important aspects of the integration of these A/D and D/A interfaces: low-voltage (LV) operation and low power (LP) dissipation, with the focus on delta-sigma modulators.

The topic of LV/LP mixed-signal design has recently received much attention, driven by technological and economical factors. Two key aspects are: 1) modern sub-micron CMOS processes cannot handle large power supply voltages, and 2) lower production and testing costs can be achieved when analog and digital blocks are integrated on the same die. Unfortunately, such integration raises problems associated with the performance of the analog blocks (substrate noise coupling), and also the lower power supply voltage makes the task of achieving a high dynamic range quite difficult. Since the maximum amplitude of the input signal is limited by the value of the power supply voltage, the only approach to increasing the DR is to reduce the noise floor. This solution has severe repercussions in terms of power dissipation. These topics, and others, will be further expanded in the following chapters.

1.1 OBJECTIVE

The objective of this dissertation is to investigate the constraints which arise when switched-capacitor (SC) delta-sigma modulators are designed for low-voltage operation, targeting also low power dissipation, and to propose methods of improving the

performance and optimizing for low power dissipation. This is accomplished by identifying critical elements whose performance can lead to increased power dissipation, as well as the fundamental limitations of available analog circuit techniques (Chapter 3). A prototype was designed and fabricated, which reflected these findings, and therefore exhibited good performance and nearly optimum power dissipation (Chapter 4).

One of the key performance parameters is the dc gain of the amplifier in the first stage; it should be high. This is necessary for high linearity and low quantization noise leakage (Chapters 2 and 3). In low-voltage operation, it may become impractical to use conventional topologies employing cascoding techniques (folded-cascode, telescopic cascode) which provide high gain in one single stage. Rather, cascaded structures have to be used. The disadvantage of the latter is the necessity for frequency compensation which results in increased power dissipation. Hence, another objective of this work is to exploit techniques, in the context of delta-sigma modulators, which compensate for the open-loop gain characteristic of the amplifier (dc value and nonlinearity), thus permitting the utilization of single-stage low-gain topologies. Predictive correlated double sampling is one of such techniques. It will be analyzed in Chapter 5.

1.2 THESIS ORGANIZATION

This dissertation is organized in six chapters, the first of which is this introduction. In it, the objectives of this dissertation, its organization and contributions are presented.

Chapter 2 extends the background and motivation touched upon in Chapter 1. The power dissipation in digital and analog circuits is addressed, and the implications of lowering the power supply voltage are discussed. Delta-sigma modulation is introduced and its performance metrics presented. Fundamental limits to power dissipation are derived, and a figure-of-merit for delta-sigma modulators proposed. This figure-of-merit is

used to compare the performance of recently proposed devices in the area of LV/LP delta-sigma modulators.

Chapter 3 analyzes in detail the power and voltage constraints in a second-order delta-sigma modulator. Design criteria will be derived to minimize the power dissipation. The contribution of the amplifiers, in the context of performance requisites, towards the total power dissipation will be analyzed in detail.

Chapter 4 presents the design of a second-order switched-capacitor delta-sigma modulator intended for voice applications, based on the results of Chapter 3. This device was fabricated, and it provided low power dissipation and high performance even though operating from a low (1.8 V) power supply. Issues related to designing switched-capacitor circuits in a low-voltage environment are addressed as well.

Chapter 5 explores predictive correlated double sampling as a means of achieving good linearity and low power dissipation in low-voltage moderate-performance delta-sigma modulators. The technique reduces the effect of the open-loop nonlinearity characteristic of the amplifier, thereby allowing the utilization of single-stage low-gain structures. Single-stage amplifiers require no compensation other than their load, with significant reduction in the power dissipation. Their noise performance is also analyzed. Chapter 5 presents also design criteria for delta-sigma modulators employing predictive correlated double sampling, and identifies areas of potential application. Simulations illustrate the functionality of the technique.

Chapter 6 presents the conclusions of this dissertation and proposes new directions for future work.

1.3 ORIGINAL CONTRIBUTIONS OF THE THESIS

The research described in this dissertation includes the following original results:

- A systematic analysis of voltage and power constraints in a switched-capacitor second-order delta-sigma modulator, and optimization criteria for the design of such structures. Based on this theory a prototype was designed and fabricated. It provided an unequaled combination of high performance and low power dissipation [31].

- A novel and useful figure-of-merit for delta-sigma modulators, which permits the evaluation of the power efficiency for a given performance.

- An analysis of predictive correlated double sampling in SC integrators, and of the design criteria and noise performance of structures employing such techniques.

2. GENERAL DESIGN CONSIDERATIONS FOR LV/LP ΔΣ MODULATORS

This chapter provides the motivation for designing integrated systems with low supply voltages and reduced power dissipation. This motivation is driven by technological factors, in particular the necessity of integrating a large number of devices and functional blocks. The delta-sigma technique is also introduced, and discussed briefly in a qualitative context, so as to provide a first insight into its characteristics. Performance metrics for delta-sigma modulators are discussed to introduce the terminology used in the remainder of the text. A more detailed and formal analysis of a generalized delta-sigma structure is presented later in order to consolidate the material introduced earlier, and provide a better understanding of the performance requirements in such structures. This section lays the foundations for a more rigorous analysis of power and voltage constraints in a delta-sigma modulator, to be given in Chapter 3. The (lower) fundamental limits to power dissipation are also derived, under the assumption of a dominant thermal noise. Based on these results, a figure-of-merit for delta-sigma modulators is proposed, which can be utilized to estimate the power efficiency of different structures. Using this figure-of-merit, a comparison of representative implementations is presented.

2.1 MOTIVATION FOR LV/LP DESIGN

Why is it necessary to design for low-voltage operation, and how does this relate to power dissipation? The motivation lies in factors of technological nature, as well as application-related and market-demand factors.

As technology evolves towards submicron and deep-submicron feature sizes, the oxide thickness of the MOS devices decreases as well. To avoid punchthrough and p-n junction breakdown, the intensity of the electric field has to be reduced. For example, a standard 0.8 μm CMOS process can withstand a maximum *sustained* power supply

voltage of about 5.5 V, but devices made using a 0.5 μm CMOS process can only tolerate about 3.5 V. (They can, however, withstand larger voltage *transients*.) It is possible to develop a 0.5 μm or smaller feature size process which will still withstand a 5 V supply. This can be done by increasing the doping of the substrate which results in thinner depletion regions around the drain and source diffusions, hence mitigating the risk of punchthrough. Although a higher doping concentration reduces the p-n junction breakdown voltage V_{BD}, it increases the punchthrough voltage V_P. The rate at which V_{BD} decreases is, however, lower than the rate at which V_P increases, and hence some trade-off can be achieved. Eventually, as the feature size is further reduced junction breakdown becomes dominant and the power supply voltage must be reduced. This aspect clearly points towards the need to design systems capable of operating from power supply voltages lower than the typical 5 V.

In fact, this reduction of the power supply voltage is not only necessary but also desirable. In digital circuits with a high level of switching activity, the power dissipated is essentially dynamic, that is, associated with charging and discharging various capacitors. The expression for the dynamic power dissipation assumes the general form

$$P = p \cdot C \cdot V^2 \cdot f_s \tag{2.1}$$

where p is the activity factor (dependent on the statistics of the signal), and f_s is the switching frequency. In most digital circuits, the voltages representing the "high" and "low" states coincide with the power supply rails, i.e., V_{DD} and ground, and hence V equals V_{DD}. Since the power is proportional to the square of the voltage step V, decreasing that step from, say, 5 V to 3 V, results in a reduction of the power dissipation by a factor of about 2.8. This result is important not only in terms of lower overall power dissipation but also in terms of power dissipation *density*, as submicron processes allow the integration of a larger number of functions. For reliability, the thermal density should be kept low. A side

benefit of using smaller feature sizes is that the parasitic switched capacitances contributing to C are also smaller, and hence so is the power dissipation.

It would seem that the power dissipation could be reduced to tolerable values simply by reducing the power supply voltage. In practice, various factors prevent this from happening, or at least complicate the trade-off. For instance, a lower value of the power supply voltage impacts the delay of the cells and hence reduces the speed of operation. The loss in speed can be compensated if the threshold voltages are also reduced, or if parallel or pipelined architectures are utilized [4][5]. Equation (2.1) suggests, however, that the total power can be minimized in other ways, such as by minimizing the activity and the parasitic switched capacitance. The activity can be reduced by devising algorithms which require fewer computation cycles, and by using event-driven blocks which are de-activated when not in use [6][7]. The capacitance can be reduced by making the digital processing elements (architecture, logic cells, layout) as simple and small as possible [4], and by using branch-based logic [8][9]. Nevertheless, lowering the value of the power supply voltage is still the most efficient way of reducing the power dissipation in digital circuits.

The subject of power optimization in digital circuits is beyond the scope of this work. It serves, however, to provide insight into one of the most important driving forces for designing for LV/LP conditions. The question at this point is "What about the power dissipation of analog circuits?" The answer, and this is the subject of the remainder of this work, is that lowering the power supply voltage usually does not yield a lower power dissipation. Although moving to submicron processes (small feature sizes, thin oxide) inherently provides the capability for lower power dissipation due to smaller parasitic capacitances and larger transconductances, the performance of analog circuits is often measured also in terms of dynamic range, that is, the ratio of the maximum signal power to the noise floor. Decreasing V_{DD} limits the maximum amplitude of the input signal which can be accommodated by the circuit, but it does not reduce the noise floor. To attain a lower noise floor, larger capacitances, hence larger transconductances, have to be

realized, which dramatically increase the power dissipation. We will return to this topic later in this chapter. So, why design analog circuits for low-voltage operation? The answer is cost. The present trend is to integrate analog and digital functionality on the same die, to reduce the cost of processing and packaging with single-chip solutions. However, if analog and digital circuits are to coexist on the same substrate the former has to be able to operate from the same low power supply voltage as the latter.

The proliferation of portable communication devices (laptop computers, cellular phones, etc.) constitutes another incentive for designing for LV/LP. Low voltage translates into smaller, lighter and cheaper batteries. Low power means longer battery lifetime, hence a reduced cost of operation and increased dependability. Although these are essentially market-related issues, they often constitute the major driving force for pursuing new design directions.

At this point, it should be clear why designing for low-voltage operation and for low power dissipation is a topic of great importance. The main issues are cost and dependability. This is what the industry and the consumer sees and wants. In this work we convert this simple requirement into more specific ones, involving low-power dissipation and low-voltage operation, dynamic range, reference voltage and noise floor, dynamic power and static power, power supply voltage and CMOS switches, power supply voltage and bandwidth, among others.

2.2 THE DELTA-SIGMA TECHNIQUE

Delta-sigma ($\Delta\Sigma$) modulation is a data conversion technique which has gained significant popularity recently in the implementation of A/D and D/A interfaces [2][3]. By trading resolution in amplitude for resolution in time, the requirements on the analog components are much relaxed. It is intuitively obvious that the fewer samples one takes from a given signal, the more accurate those samples and the processing elements have to

be. If instead the signal is sampled at a very high rate, significant redundancy is introduced. Hence, even if the samples are corrupted by noise, or processed with less accuracy, it is clear that if properly averaged, the effect of those errors can be made negligible. This requires a knowledge of the statistics of the input signal and of the noise.

In delta-sigma modulation, this redundancy is exploited in two ways. One is by sampling the input signal at a rate f_s much higher than the Nyquist rate (this is called oversampling); the power of signals with spectral content extending beyond $f_s/2$ (such as white noise) will therefore be distributed between dc and f_s [2][10]. This means that in the band of interest (input signal band), the spectral floor due to the noise will be lower. If the energy falling outside the signal band is removed by filtering, the signal-to-noise ratio (*SNR*) improves. (This filtering in fact implements the averaging process mentioned above.) The other way is by making use of feedback. It is known that feedback techniques can radically change properties of open-loop systems which might otherwise be of little use due to nonlinearity and other imperfections. In a delta-sigma modulator, a filter (called the loop filter) with high gain in the band of interest and a quantizer constitute the forward path of a feedback system (Figure 2.1). Due to the feedback loop, the spectral components of any signal injected or applied at nodes in the forward branch following the output of the loop filter will be attenuated by the gain of the filter at those frequencies. For the system shown in Figure 2.1, if we assume for simplicity that the quantizer linearly adds a noise component E_Q to the signal at the output of the loop filter, one can easily arrive at the following expression for the output of the system in the frequency (Laplace- or z-transform) domain:

$$Y = \frac{H}{1+H} \cdot X + \frac{1}{1+H} \cdot E_Q \tag{2.2}$$

If the loop filter has a very high gain ($|H| \gg 1$) in a range of frequencies, then the signal transfer function is approximately unity in that band, whereas the noise components in the same range are greatly attenuated, resulting in increased *SNR*. This is commonly

called in the context of delta-sigma modulation, of *noise shaping*, and is illustrated in Figure 2.2, where E_Q is assumed to have a flat power spectral density (*PSD*). Hence, the effect of the feedback loop can be significantly more beneficial than that of oversampling alone, since it effectively reduces the noise power in the band of interest. The out-of-band noise, however, is not attenuated and has to be removed by subsequent filtering.

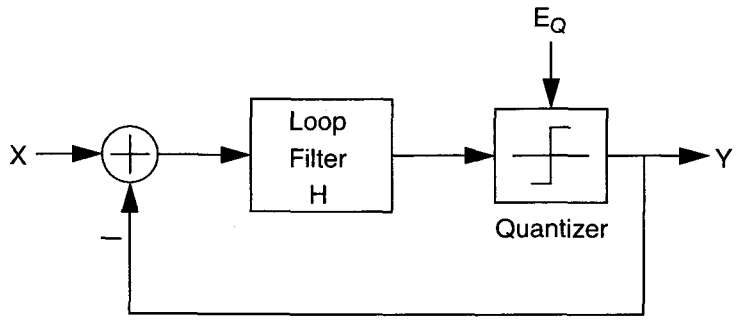

Figure 2.1: Simplified block diagram of a delta-sigma modulator.

At this point, the potential of the delta-sigma technique should be clear. The most important feature is that the combined utilization of oversampling and feedback relaxes the requirements on blocks following the loop filter. Actual implementation of the loop filter may be by low-order sections with feedback, and possibly feedforward branches, for improved stability. In such cases, all noise appearing at any internal nodes following the *first stage* of the loop filter, when referred back to the input, will undergo some degree of filtering and becomes less important. In other words, one can tolerate noise of larger magnitude, and errors due to non-idealities of the active devices, without compromising the performance. This includes performing a coarse quantization of the signal, ultimately to one bit. Later in this chapter we will introduce performance metrics, and quantify the benefits originating from noise shaping and oversampling.

As shown in Figure 2.2, the spectral components of the noise falling inside the signal band are attenuated, compared to the original *PSD* of the noise. The same does not happen to those falling outside of the signal band. Indeed, those are amplified and need to be removed by a digital filter.

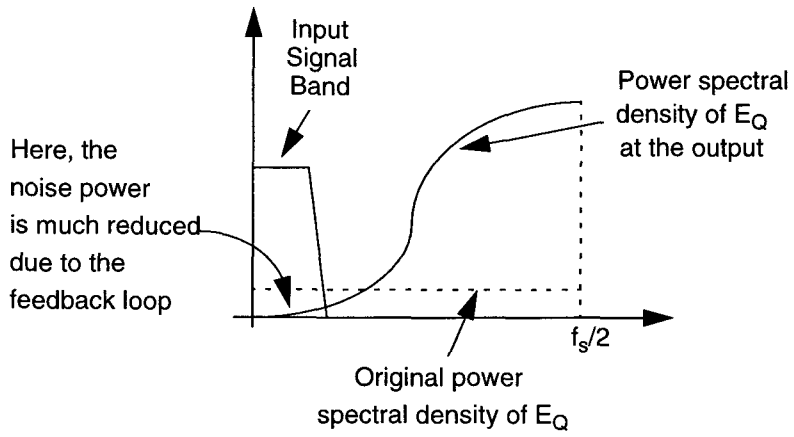

Figure 2.2: The concept of noise shaping.

The rate f_s of the output digital bit stream Y (Figure 2.1) is usually too high for complex digital post-processing, which would consequently require very complex circuitry and dissipate excessive power. Hence, the digital filter which follows the modulator implements the function of down-sampling as well. The combined filter and down-sampler is commonly (and somewhat loosely) known as *decimator* or *decimation filter*. The reduction of the sampling rate is usually accomplished in several stages, depending on the rejection characteristics of unwanted components of each block, and is accompanied by an increase in the wordlength. This is plausible since that was the original trade-off. Once the out-of-band noise has been removed, the oversampling ratio can be reduced and the wordlength has to be increased to represent the input signal accurately. The complexity of the decimator can be significant due to the large out-of-band noise energy that has to be removed. This is where one of the trade-offs takes place; the

requirements for the analog blocks are relaxed, but a penalty has to be paid on the digital post-processing. Note, however, that this penalty is only in the complexity of the digital filter, which can be implemented with any desired accuracy, while the same cannot be said about analog blocks. The combination of a delta-sigma *modulator* and a *decimation filter* constitutes a delta-sigma data *converter* or ADC.

Since this technique exploits oversampling, it is not suited for very high-frequency and high-resolution applications. Some work targeting high-speed and low- to moderate-resolution applications has been reported [12][13], but the delta-sigma technique finds its main niche in low- to moderate-speed, high-resolution applications, such as instrumentation [14], unconventional signal processing [15][16], and at voice [17] and audio range frequencies [18]. The latter are of particular importance in communications where high-performance, moderate-speed A/D and D/A interfaces are required. Due to its robustness, the delta-sigma technique is then typically the preferred choice.

2.3 PERFORMANCE METRICS

Before we proceed, it is necessary to introduce appropriate performance metrics for delta-sigma *modulators*. Contrary to other conversion methods, the performance of a $\Delta\Sigma$ *modulator* is better understood in terms of signal and noise spectra, signal-to-noise ratio and dynamic range, rather than the number of output bits. The reason lies in that the typical wordlength of the digital output of a delta-sigma modulator is *one*. (Moreover, there is not a one-to-one relation between the input and the output samples.) However, the *SNR* in the signal bandwidth can be very large, due to the noise shaping effect of the loop. For example, a flash ADC will take a sample of the input signal, quantize that sample and assign a digital code with wordlength N to the quantized value. The ADC is called an N-bit ADC. If the conversion is performed at the Nyquist rate, it can be shown that the *SNR* resulting from such quantization (for a sinusoidal input signal) can be approximated by

$$SNR_{dB} = 6.02 \cdot N + 1.76 \tag{2.3}$$

Hence, a 10-bit ADC ideally displays a signal-to-noise ratio of about 62 dB, and a 16 bit ADC displays an *SNR* of about 98 dB. This concept is also used in delta-sigma modulators, where the signal-to-noise ratio is determined and "converted" to the equivalent bit accuracy or resolution. For instance, if the peak *SNR* is 98 dB, the modulator is called a 16-bit modulator, even if the output signal wordlength is unity. Note that this simply means that if the out-of-band noise would be completely eliminated, and the output rate reduced to the Nyquist rate, the maximum meaningful wordlength that could be used to represent the input signal is 16. The removal of the out-of-band noise and the reduction of the output rate constitute the function of the decimator. The wordlength of the digital output of a delta-sigma *converter* is not one, but the equivalent of the *SNR* in the signal band, or more.

We are now in a position to introduce and understand the metrics utilized in the evaluation of the performance of such systems. These metrics are illustrated graphically in Figure 2.3. Note that some of the following definitions have a scope which extends beyond delta-sigma modulation.

- *Overload point*, P_{MAX}, is the value of the input signal power which overloads (saturates) the modulator. At this point, the slope of the *SNR* curve reduces, and eventually becomes negative with further increase of the input signal level.

- *Total dynamic range*, or simply dynamic range, *DR*, is the ratio between the maximum input signal power P_{MAX}, and the lowest input signal power P_{MIN} that can be discriminated from the noise floor (P_{MIN} is also referred to as *resolution).*

- *Instantaneous dynamic range*, *IDR*, defined as $IDR = SNR_X - P_X$ (all quantities in decibel), where P_X is the input signal power (with appropriate reference), sufficiently small that there are no distortion or overloading effects (for instance, $P_X = -60\,\text{dB}$), and SNR_X the signal-to-noise ratio for that input signal level. The following relation holds: $IDR \geq DR$.

- *Peak signal-to-noise ratio*, SNR_{Peak}, is the maximum signal-to-noise ratio that can be obtained. Strictly speaking, this maximum may occur for values of the input signal level larger than P_{MAX}. The following relation holds: $SNR_{Peak} \leq -P_{MIN}$.

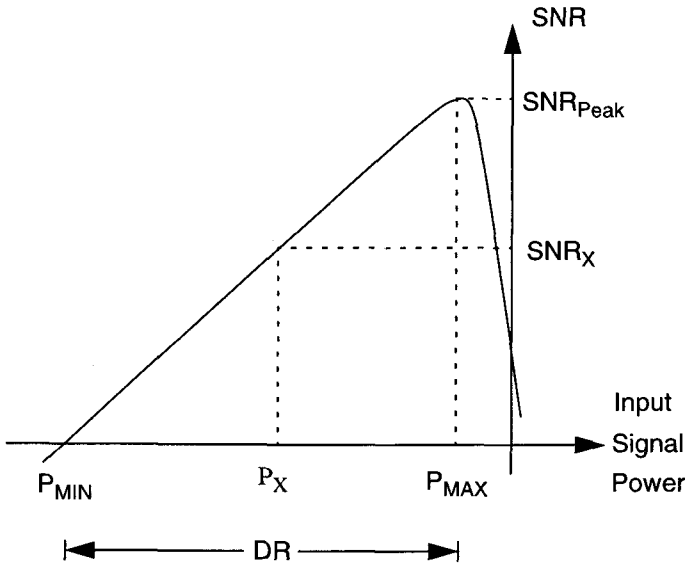

Figure 2.3: Performance metrics used in connection with delta-sigma modulators.

Both the peak signal-to-noise ratio and the dynamic range are used to express the performance of a delta-sigma modulator, and are quantified in decibels or bits, as

discussed above. Also, it is common to normalize the curve in Figure 2.3 to the value of the reference voltage V_{REF}, in which case the scale is in dBr (0 dB corresponds to the power of a sinewave with amplitude V_{REF}). We can now proceed with a more detailed analysis of the performance requirements of a delta-sigma modulator.

2.4 GENERAL PERFORMANCE REQUIREMENTS IN A ΔΣ MODULATOR

In section 2.2 we introduced the delta-sigma technique, and discussed how feedback techniques, in conjunction with oversampling, could be used to selectively reduce the noise power in a band of interest. In this section we quantify the benefits of such techniques, and infer the implications in terms of performance requirements. This analysis will be refined for a second-order structure in chapter 3.

Consider Figure 2.4. It illustrates an idealization of a single-loop delta-sigma modulator with arbitrary order. Note that the loop filter transfer function is expressed in terms of z-transform, because in this work we do not contemplate continuous-time implementations of such structures. Even continuous-time implementations cannot be asynchronous, hence most of the discussion that follows still applies. Another aspect that is new relative to Figure 2.1, but which was mentioned at the time, is the implementation of the loop filter. The loop filter consists of a cascade of accumulators (integrators in the continuous-time domain), with multiple feedback loops. An accumulator displays a low-pass type of transfer function, and for that reason the structure is said to be a low-pass delta-sigma modulator. Analogously, band-pass transfer functions can be implemented to process band-pass signals [19]. The feedback loops are required for stability purposes, and in most systems with order equal or larger than three, feedforward branches are required as well to realize stabilizing zeros in the transfer function. (The feedforward branches have also been used to realize a Chebyshev transfer function [11].) This is an aspect linked to the implementation of such systems, and does not greatly influence the following analysis which concentrates on the spectral properties of the signals.

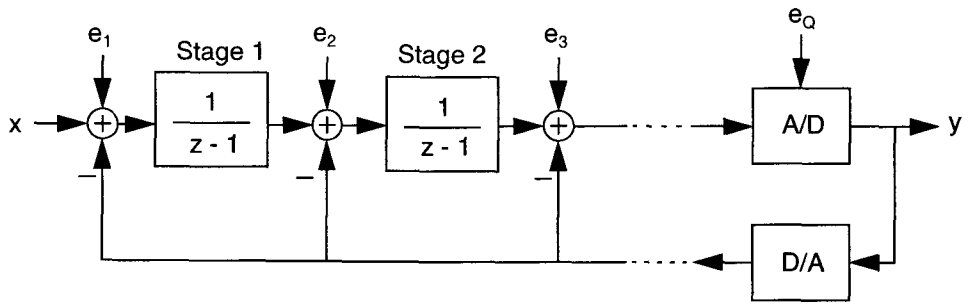

Figure 2.4: Simplified block diagram of an idealized ΔΣ modulator of arbitrary order.

Also new to Figure 2.1 is the presence of an A/D and a D/A converter. The A/D converter performs the function of the quantizer, and converts the result into a digital word. Typically, 1-bit quantization is utilized in delta-sigma, and the A/D converter consists of a comparator (quantizer) followed by a latch (A/D conversion). The D/A converter changes the output digital word into an analog representation of that signal. In the case of single-bit quantization, the D/A converter consists of a switch which selects $+V_{REF}$ or $-V_{REF}$ (or the equivalent, if only a single reference voltage is available).

Following the approach used in connection with Figure 2.1, it is assumed that the A/D converter introduces a component of quantization noise e_Q which adds to the output signal of the previous stage. Note that this is correct, as no assumption was made regarding the properties of the noise signal. For simplicity of analysis, e_Q is commonly considered to be white, uncorrelated with the input signal (linear analysis). For structures of first and second order, this is markedly untrue [20][21][22], and caution has to be exercised when estimating the noise performance. Nevertheless, the model provides a good insight on the functionality of these structures. The sources e_i denote *any* addition of noise or error to the signal path. They represent the input-referred noise and nonidealities of stage i, nonidealities in the feedback path from the D/A converter, and other sources of noise such as thermal noise, clock charge injection and substrate noise; anything that is

applied or injected at node i. At the output end, e_i coincides with the quantization noise e_Q. The analysis of the linearized model yields

$$Y(z) = z^{-N} \cdot X(z) + \left(1 - z^{-1}\right)^N \cdot E_Q(z) + \sum_{i=1}^{N} \left(1 - z^{-1}\right)^{i-1} \cdot z^{-(N+1-i)} \cdot E_i(z) \tag{2.4}$$

The first line in (2.4) contains the term in the input signal X and the term in the quantization noise E_Q. The second line aggregates all the remaining sources of noise e_i. The transfer function from noise source e_i to the output Y is

$$H_i(z) = \left(1 - z^{-1}\right)^{i-1} \tag{2.5}$$

a power of the difference between successive samples of noise. The exponent varies from 1 for the leftmost source (same as the input signal), to $N-1$ for the rightmost one. If the signal being sampled (noise in this case) is rapidly varying in time, the difference between two consecutive samples can yield a large value, because the samples can differ by a large amount. If the signal is slowly varying, the two consecutive samples will look alike and the difference will be small (particularly if oversampling is being used). This means that taking the difference between two consecutive samples is equivalent to performing a high-pass filtering function. Taking a power of the difference corresponds to a more elaborate filtering, with more coefficients. Notice that due to the delays in the system, it has memory, and higher-order systems make use of that memory by developing inherently more rigorous estimates of the signal, through proper averaging of noise samples. This is the essence of delta-sigma modulation.

To better understand all implications, it is useful to analyze in more detail equation (2.5). Let us assume that the oversampling ratio *OSR* (defined as the ratio between the sampling frequency and the Nyquist sampling rate) is very high (two orders of magnitude is a typical value). The absolute value of the transfer function in (2.5) can then be approximated according to

$$\left|H_i(\omega)\right| = \left|1 - \exp\left(-j \cdot \omega T_S\right)\right|^{i-1} \cong \left(\omega T_S\right)^{i-1} \tag{2.6}$$

where T_S is the inverse of the sampling frequency, and ω is the variable angular frequency. The noise power in the signal band $[-bw, bw]$ (bw is a normalized frequency, therefore comprised between 0 and π) can be calculated by integrating the output power spectral density due to the noise sources [23]:

$$P_i = \frac{1}{2 \cdot \pi}\int_{bw}^{bw}\left(S_{ei}(\omega) \cdot \left|H_i(\omega)\right|^2\right)d\omega \tag{2.7}$$

where S_{ei} represents the *PSD* of the noise originated by source e_i. We indicated above that the sources e_i can represent any type of noise. This generality poses difficulty in evaluating the integral in (2.7). However, assuming that the e_i refer to sources of white noise, with constant power, the task of evaluating the integral is greatly simplified, and the insight gained quite significant. The auto-correlation function of white noise is a delta function [23]. Hence its *PSD* is constant with frequency, and uniformly distributed between 0 hertz and the sampling frequency (positive frequency representation). Since the power is constant, the level of the *PSD* is inversely proportional to the sampling frequency: $S_{ei} \propto 1/f_s$. (This result does not apply if the noise signal is *oversampled.*) In other words, if the sampling frequency doubles, the *PSD* of the noise decreases by a factor of two, or 3.01 dB. Since the band of interest is only a fraction of the whole spectrum, the noise power in that fraction is smaller by a factor of two as well. Inserting the dependency above with f_s in (2.7) one easily arrives at

$$P_i \propto \left(\frac{\pi}{OSR}\right)^{2i-1} \tag{2.8}$$

This result is of paramount importance as it combines the effects of oversampling and noise shaping. The former is accounted for through *OSR* and the latter through the exponent. For instance, for noise appearing at the input of the first and second stages (i=1, 2) one obtains

$$P_1 \propto \frac{\pi}{OSR} \text{ and } P_2 \propto \left(\frac{\pi}{OSR}\right)^3 \tag{2.9}$$

This result states that noise at the input stage benefits only from oversampling, whereas noise at the input of the second stage benefits from both oversampling and from noise shaping. More generally, it can be said that the noise power (at the output) with origin in source e_i (input of i^{th} stage) is reduced by $3.01 \cdot (2 \cdot i - 1)$ dB for each octave of increase in *OSR*, opposed to only 3.01 dB due to oversampling. From one stage to the following, the power is reduced by a factor proportional to $(OSR/\pi)^2$. Figure 2.5 plots the output power as given by (2.9), for three common values of the oversampling ratio. For the values of *OSR* indicated, the in-band noise power originating at the input stage, and superimposed to the input signal, is attenuated by 13 dB to 19 dB, as a result of oversampling. The in-band noise power originating at the input of the i^{th} stage is attenuated by 26 dB to 38 dB, relative to the *previous* stage.

This discussion assumes that all noise sources are identical. If the same noise signal appears at the output with a power which depends on the location of the source in the loop, this is an indication that we can tolerate larger levels of noise at certain nodes without seriously compromising the performance (*SNR*). Namely, it becomes clear that the input stage determines to a large extent the overall performance of the system; here, noise and errors arising from element nonideal behavior can benefit, at most, from the oversampling. They are, otherwise, regarded as part of the input signal, with unity transfer

function to the output, and have to be minimized. The following stages, however, see their performance requirements much relaxed due to the noise shaping effect, especially if that noise is *not* broadband. Offset dc signals and flicker noise are virtually cancelled (the noise transfer function has at least one zero at dc). For this reason, a large fraction of the total power (typically more than 50%) is often dissipated in the first stage, since it requires larger capacitances to reduce the noise floor, hence larger transconductances and larger biasing currents. (A different approach to implementing delta-sigma modulators was recently proposed. It utilizes a passive loop filter, thereby placing the performance requirements -- speed, gain -- on the quantizer rather than the first stage [32].)

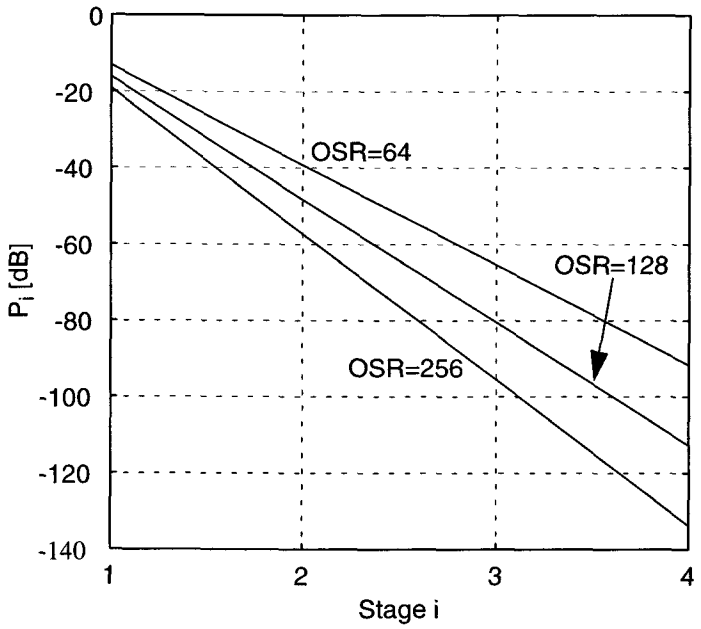

Figure 2.5: Attenuation of the noise power generated at the input of stage *i*.

Chapter 3 addresses in detail the power and voltage constraints in a second-order delta-sigma modulator, including the power dissipation of the amplifiers. Before we investigate this subject, it is pertinent to ask "What is the minimum power that can be dissipated?" The answer to this question varies according to the specifications of the

system, and with what limits the performance. Nevertheless, the best performance that can be obtained is determined by the purity of the input signal itself and the quality of the sampling process. If the sampling process does not introduce any error, then the ubiquitous thermal noise will be the limiting factor. The next section analyzes this issue.

2.5 FUNDAMENTAL LIMITS TO POWER DISSIPATION

Figure 2.6 illustrates the sampling process that takes place at what could be the input stage of a delta-sigma modulator. The input signal V_{in} is sampled into a capacitor C_{in}. Due to the resistance of the switches, a noise voltage V_n is also stored in C_{in}. This noise is of thermal origin, and band-limited by the RC constant formed by the resistance of the switch and the sampling capacitor C_{in}. It can be shown [10] that the power of the resulting signal depends only on the size of the sampling capacitor, and on the absolute temperature T according to

$$N_{th} = \frac{kT}{C_{in}} \tag{2.10}$$

where k is the Boltzmann constant. Since the noise signal has a broad bandwidth (Lorentzian spectra display typical time constants in the order of 10^{-14} s, the relaxation time in electron-electron scattering), it is undersampled, and only a fraction of the total power is contained in the signal band. That fraction is equal to the inverse of the oversampling ratio. Moreover, since the stored charge has to be transferred to the output through a second switch, another sample of noise is added to the stored value. Because the noise samples are uncorrelated, the powers of the corresponding signals add. Expression (2.11) gives therefore the in-band noise power:

$$N_{th,b} = \frac{2kT}{C_{in} \cdot OSR} \tag{2.11}$$

It is intuitive that the minimum power that is dissipated is associated with the process of sampling the input signal: the charging and discharging of the input capacitor. This transfer of charge over a fixed period of time ($1/f_s$) corresponds to having an average current flowing through a resistor [10], current which is drawn from the power supply. Hence the minimum dissipated power is given by

$$\begin{aligned} P_{MIN} &= V_{DD} \cdot \langle I \rangle \\ &= V_{DD} \cdot f_s \cdot \langle Q \rangle \\ &= \alpha \cdot C_{in} \cdot V_{REF} \cdot V_{DD} \cdot f_s \end{aligned} \tag{2.12}$$

where $\alpha \cdot V_{REF}$ represents the maximum value of the input signal V_{in}, and $\langle x \rangle$ denotes the average value of x. In this representation, α is smaller than one and is an indication of a saturation mechanism. Frequently, the maximum value of the input signal which can be accommodated by a system is slightly lower than the reference voltage V_{REF}. In the case of a delta-sigma modulator, this situation is referred to as overloading, Section 2.3, and results from increased quantization noise in the signal band due to instability. Its value varies with the order and topology of the modulator.

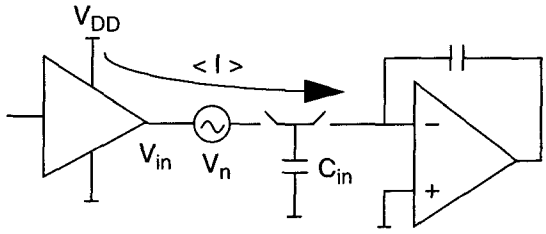

Figure 2.6: Sampling the input signal.

Expression (2.12) gives the power which is dissipated in the process of sampling the input signal, but it does not provide any information about the purity of that sample. Except for the input capacitor C_{in}, all the variables in (2.12) are well known. As we saw earlier, C_{in} determines the noise signal which is superimposed to the input signal, and its value and the *OSR* define the *noise floor*, or the minimum input signal power which can be represented with an *SNR* larger than one (i.e., the resolution). Since the power is maximum when the signal reaches its maximum, we can relate the powers of both signal and noise through the parameter *dynamic range* (Section 2.3). For a sinusoidal signal,

$$DR = \frac{\text{Maximum Input Signal Power}}{\text{Integrated In-Band Noise Power}} = \frac{\frac{(\alpha \cdot V_{REF})^2}{2}}{\frac{2kT}{C_{in} \cdot OSR}} \tag{2.13}$$

This result can be used in (2.12), yielding

$$P_{MIN} = \frac{8 \cdot kT \cdot DR \cdot BW}{\alpha} \cdot \left(\frac{V_{DD}}{V_{REF}} \right) \tag{2.14}$$

where BW is the signal bandwidth, and we made use of $F_S = 2 \cdot OSR \cdot BW$. An optimum, or absolute minimum, is obtained when α=1 and V_{REF}=V_{DD} that is, when the system does not overload for signals weaker than the reference voltage, and the latter can be made as large as the power supply voltage. This absolute minimum is given by

$$P_{MIN} = 8 \cdot kT \cdot DR \cdot BW \tag{2.15}$$

A few remarks are in order:

- P_{MIN} does not depend on the absolute value of the power supply voltage, but rather on how large the input signal can be made relative to that voltage.

- P_{MIN} is constant for a constant dynamic range. This statement holds as long as the input capacitor size and the magnitude of the reference voltage can be exchanged to obtain the same *DR*, according to (2.13).

- P_{MIN} increases by a factor of four for each added bit of dynamic range.

Figure 2.7 plots the minimum energy consumption as a function of the dynamic range in bits. In practice, the power dissipation is larger than the minimum given by (2.15) by three to five orders of magnitude. The reason for such large discrepancy is that expression (2.15) is representative only of the power dissipated in sampling the input signal, assuming that thermal noise is the only limitation. Other sources of noise, parasitic components and, most importantly, amplifier biasing currents, also contribute to the power dissipation. Static power dissipation from biasing currents will actually increase with decreasing power supply voltage. Assume, for instance, that a class A amplifier is used as the active element in the first stage of a delta-sigma modulator (Figure 2.6). The capacitive load of the amplifier will be in the order of magnitude of the sampling capacitor C_{in} the size of which, as we saw, is determined by the desired dynamic range. Hence, for a given gain-bandwidth product,

$$P_{STATIC} = V_{DD} \cdot I_{BIAS} \propto V_{DD} \cdot gm \propto V_{DD} \cdot C_{in} \tag{2.16}$$

Moreover, by (2.13), for a constant dynamic range, $C_{in} \sim 1/V_{DD}^2$. Introducing this result in (2.16) one concludes that $P_{STATIC} \propto 1/V_{DD}$. Therefore, in general, if the

performance (*DR*) in analog circuits is limited by thermal noise, the power dissipation *increases* with *decreasing* power supply voltage. This result is somewhat unsettling since integration of digital and analog blocks in the same fine-line IC die requires that the latter operate from lower power supply voltages. However, as we have just shown, the increase in power dissipation is inherent to the circuit techniques currently in use. There is, of course, space for numerous improvements, and in this work we will analyze a viable path in that direction.

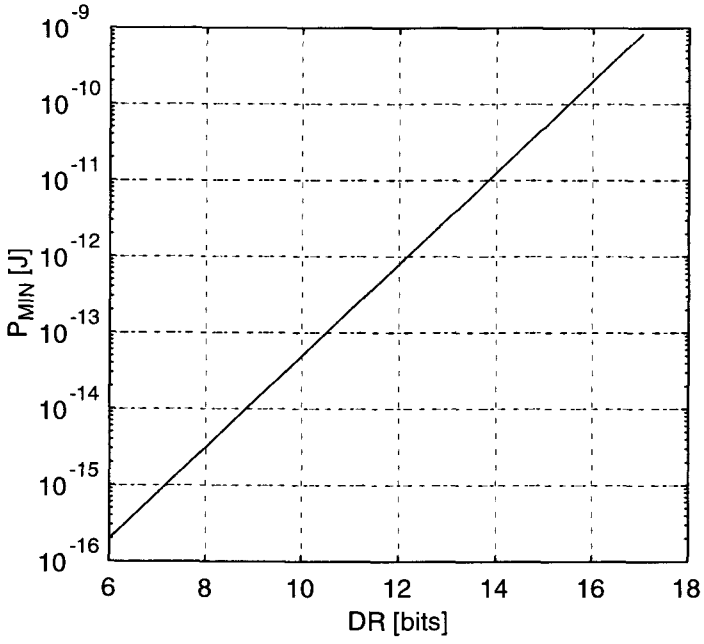

Figure 2.7: Minimum energy consumption (power per bandwidth) as a function of the dynamic range.

To provide insight on how far current implementations are from reaching the minimum power dissipation value expressed by (2.14) or (2.15), we propose a figure-of-merit *FOM* for delta-sigma modulators [24]. This figure-of-merit allows a coarse estimation of the performance and overall *efficiency* of a particular implementation. The

underlying assumption is that about half of the total power dissipated can be allocated to the first stage. We then define *FOM* as

$$FOM = \left(\frac{PWR}{8kT \cdot DR \cdot BW}\right)\left(\frac{V_{REF}}{V_{DD}}\right)\left(\frac{\alpha}{2}\right) \tag{2.17}$$

where *PWR* is the total power dissipation. Ideally, *FOM* should be close to one. Note that the parameters involved relate exclusively to performance, not to technology. Hence it provides a measure of the efficiency of utilization of the energy, to achieve such performance. The larger *FOM* is, the more inefficient the system.

It should be pointed out that the proposed figure-of-merit is only applicable to structures in which the performance is determined thermal noise. If, say, quantization noise were the limiting factor, then the calculation of the dynamic range would have to take into account not only the oversampling ratio, but also the topology (order) of the modulator, and the distribution of the quantization noise.

Table 2.1 collects several references on recent works related to LV/LP delta-sigma modulators, with indication of technology utilized, topology of the modulator, switched-capacitor (SC) or continuous-time (CT) technique, as well as the parameters relevant to the calculation of *FOM*. The rightmost column shows the calculated *FOM* for each implementation (due to insufficiency of data α was made equal to one). Noticeably, a low value for the power dissipation does not necessarily result in a low *FOM*. Moreover, the lowest *FOM* is still about three orders of magnitude above the minimum as given by (2.15). Our work described in [31] displays the lowest figure-of-merit, hence the highest efficiency, and will be described in detail in Chapter 4. Figure 2.8 provides a graphical view of these results.

Ref	Realization	Topology	Process	VDD [V]	VREF [V]	BW [kHz]	DR [dB]	PWR [mW]	FOM (α=1)
[25]	SC	4th order, cascaded	1.2 µm BiCMOS	3	1.5	25	93	55	8323
[26]	CT	2nd order	0.5 µm CMOS Low-VT	1	0.25	192	58	1.56	48600
[27]	SC	4th order, bandpass	2 µm CMOS	3.3	0.5	30	69	2	19200
[28]	SC	3rd order	1.5 µm CMOS	2.4	0.5	8	80	1	3931
[29]	SC	1st order	0.5 µm CMOS Low-VT	1	0.25	4	54	0.1	751260
[30]	SC	3rd order, cascaded	1.2 µm CMOS	1.8	0.9	25	92	6.3	1200
[31]	SC	2nd order	0.6 µm CMOS	1.8	0.6	3.5	94	2	1144
[32]	SC	2nd order	1.2 µm CMOS	3.3	1	20	87	0.23	1680
[33]	SC	3rd order	1.2 µm CMOS	1.95	0.375	8	73	0.34	6184

Table 2.1: Comparison of the performance of reported work on LV/LP delta-sigma modulators.

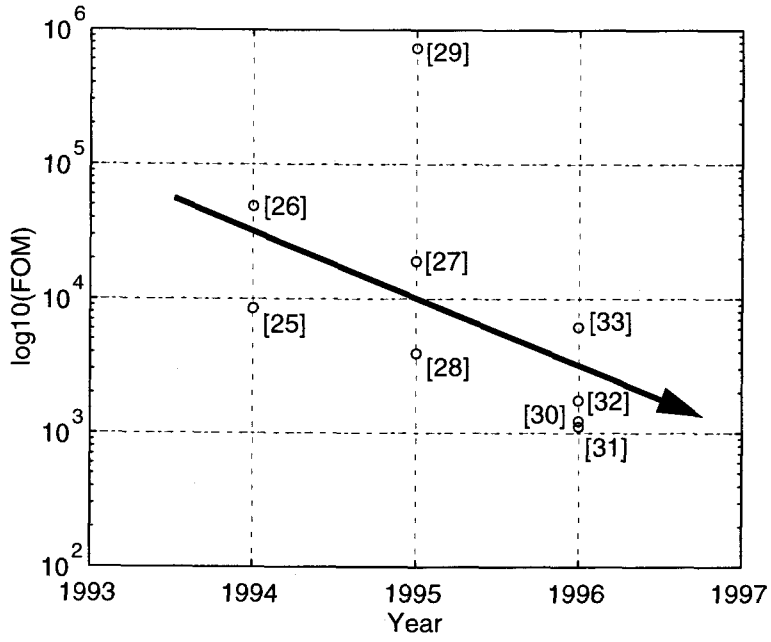

Figure 2.8: Trend for efficiency of utilization of energy. A large *FOM* means less efficiency.

2.6 SUMMARY

This chapter provided the motivation for designing for LV/LP operation, particularly in the context of A/D and D/A interfaces. Delta-sigma conversion was introduced as an efficient technique frequently utilized in the implementation of such interfaces. The performance requirements for each of the blocks in a delta-sigma modulator, and implications in terms of power dissipation, were briefly discussed. The fundamental limits to power dissipation in the presence of thermal noise were derived, and a figure-of-merit for delta-sigma modulators proposed. This figure-of-merit is an expression of the efficiency in the utilization of energy to achieve a given performance.

3. CRITICAL ANALYSIS OF VOLTAGE AND POWER CONSTRAINTS IN A 2ND-ORDER ΔΣ MODULATOR

An important aspect of analog IC design preluded by Chapter 2 is that reducing the power supply voltage does not necessarily result in lower power dissipation. The opposite is usually true. Therefore, it is of interest to investigate the limitations of current design techniques and topologies when utilized in a low-voltage environment.

This chapter addresses in detail the impact of utilizing a low supply voltage in the design of a low-power switched-capacitor, 2nd-order, single-bit delta-sigma modulator. We chose a 2nd-order topology for its popularity and simplicity, but the conclusions can be extended to other, more complex, structures. Switched-capacitor techniques were given preference due to their excellence in high-performance applications. It is our belief that at this time switched-current (SI) techniques do not offer any advantages compared to SC when designing for low-voltage operation. The justification lies in that they suffer from the same problems as SC, with the aggravation of a lower dynamic range (assuming a quadratic model for the devices, the signal-to-noise ratio of a stored current is 6 dB lower than that of the corresponding stored gate voltage). Continuous-time solutions are not competitive in high-resolution (especially high-speed) applications either, since the performance becomes dominated by clock timing uncertainties.

3.1 THE 2ND-ORDER SINGLE-LOOP DELTA-SIGMA MODULATOR

Figure 3.1 shows the block diagram of a linearized 2nd-order single-loop ΔΣ modulator. In analogy with the analysis presented in Chapter 2, various inputs representing error sources are shown. They are e'_1 and e'_2, the *input referred* noise originating in the operational amplifiers of the first and second integrators, respectively; e_{D1} and e_{D2}, the errors originating in the feedback paths -- e.g., noise and distortion from

the DAC(s); and e_Q, the quantization noise. The quantizer and A/D converter are represented by a branch gain k and the additive noise source e_Q. Since the nonidealities of the DAC(s) are lumped into e_{D1} and e_{D2}, this block was replaced by a unity gain element. Each (forward Euler) integrator is described by a transfer function in the z-domain

$$H(z) = \frac{1-\alpha}{z-(1-\beta)} \tag{3.1}$$

where the parameters α and β are the gain and pole errors, respectively. They result from mismatches and op-amp finite dc gain. Both are ideally equal to zero. For frequencies much below the Nyquist frequency, the output signal is given by

$$\begin{aligned} Y(z) \cong\ & (1-\alpha_1)\cdot(1-\alpha_2)\cdot[X(z)+E'_1(z)-E_{D1}(z)]+ \\ & \frac{1-\alpha_2}{k_1}\cdot(z-1+\beta_1)\cdot[E'_2(z)-E_{D2}(z)]+ \\ & \frac{k}{k_1\cdot k_2}(z-1+\beta_1)\cdot(z-1+\beta_2)\cdot E_Q(z) \end{aligned} \tag{3.2}$$

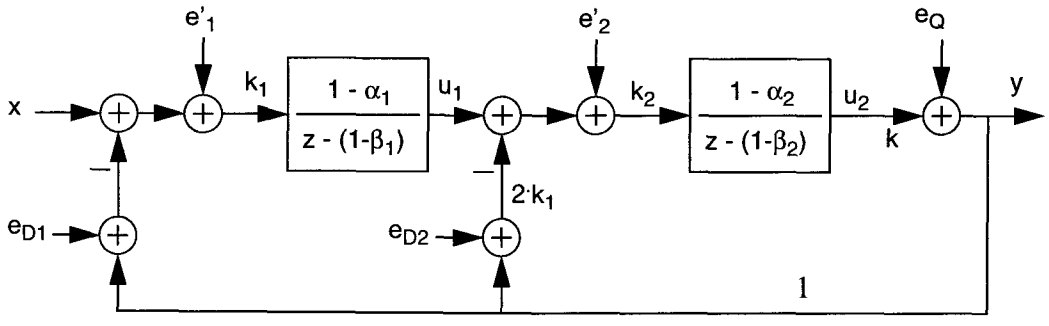

Figure 3.1: Block diagram of a 2nd-order delta-sigma modulator with indication of various noise sources.

The quantization noise transfer function $Y(z)/E_Q(z)$ (NTF) of the ideal modulator displays two zeros at $z = 1$ (since β is zero). The finite dc gain of the amplifiers, however, shifts those zeros to $z = 1-\beta_1$ and $z = 1-\beta_2$, as shown by (3.2). This results in a flattening of the transfer function near dc ($z = 1$), and hence in increased integrated noise power, known as noise leakage (Figure 3.2 illustrates this concept). The excess noise can easily be calculated and is approximately given by

$$\frac{N^2_{Q,\text{ Finite Gain}}}{N^2_{Q,\text{ Infinite Gain}}} \cong 1 + \frac{5}{3}\cdot\left(\beta_1^2+\beta_2^2\right)\cdot\left(\frac{OSR}{\pi}\right)^2 + 5\cdot\beta_1^2\cdot\beta_2^2\cdot\left(\frac{OSR}{\pi}\right)^4 \tag{3.3}$$

Since the pole error β is inversely proportional to the dc gain of the amplifier [10] this noise can be made very small if

$$A^i_{DC} \gg \frac{OSR}{\pi} \tag{3.4}$$

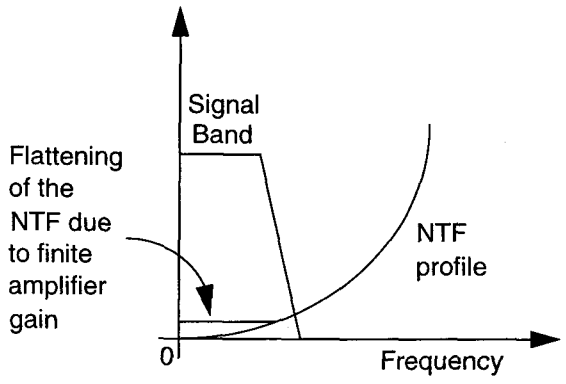

Figure 3.2: Effect of the amplifier finite dc gain on the noise transfer function.

Making one of the gains very large (say, that of the input op-amp) and the other small is not enough to provide reduced noise leakage. This is apparent from the second term in (3.3). Moreover, higher oversampling ratios require larger gains, which is not surprising since the in-band quantization noise power decreases with *OSR*. This is an interesting aspect as it says that we cannot relax the gain requirement for an amplifier, even if it is part of the second stage. This is not in contradiction with the previous result of tolerating larger errors as we progress down the loop towards the quantizer. The analysis assumed perfect transfer functions. The results still apply, but the gain of the amplifier has to be sufficiently large so as to not become a dominant source of error. For example, if both amplifiers have a dc gain of 40 dB, and the oversampling ratio is 256, the in-band noise power increases by about 6 dB due to the pole errors. If the performance is limited by quantization noise, this loss (*SNR*) may be unacceptable, depending on the initial tolerance. This result was derived using a linear model, therefore the numbers are not exact. Figure 3.3 shows the simulated output power spectral densities of a 2nd-order modulator when the amplifiers have a dc gain of 40 dB and 100 dB. The effect of the dc gain of the amplifiers on the noise floor is obvious.

The requisites for the amplifier gain become even more stringent in cascaded topologies [34][35]. The performance of such structures relies on the matching between analog and digital transfer functions. Although matching between digital transfer functions can be implemented with any desired accuracy, matching between analog and digital transfer functions cannot, and the result is again noise leakage, and consequent degradation of the *SNR*. Implementing accurate analog transfer functions requires the utilization of operational amplifiers with very large dc gain, in order to reduce the pole error β. (The gain error is not so important as it results in a linearly filtered error component.). Some authors have proposed digital calibration techniques utilizing adaptive algorithms [36], but no successful implementation has yet been reported. Moreover, the substantial added complexity makes these solutions somewhat unattractive.

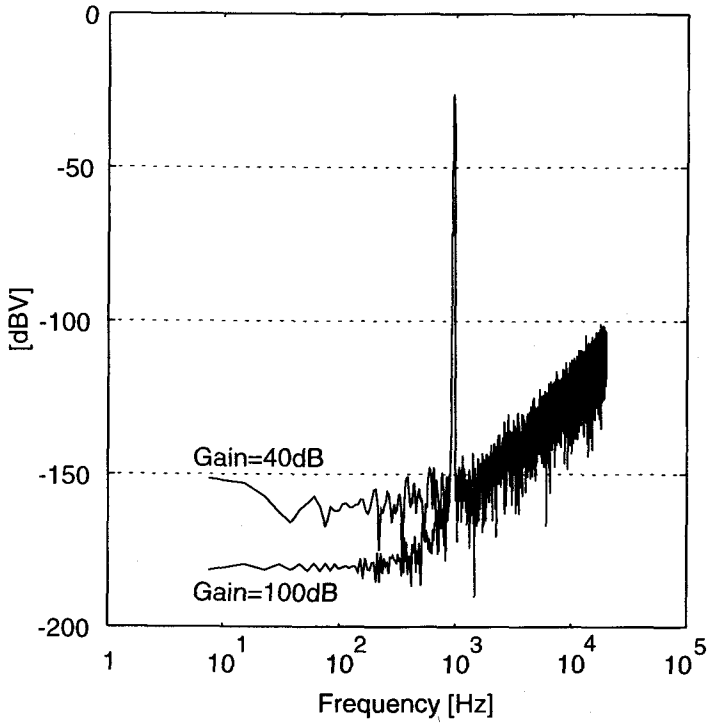

Figure 3.3: Quantization noise leakage due to op-amp finite dc gain. The input signal was a -22.4 dBV (-15 dBr), $3/\pi$ kHz sinewave, and the sampling frequency 2 MHz.

Another aspect related to the dc gain of the amplifier is distortion. The gain characteristic of an amplifier varies with the magnitude of the output signal, in a nonlinear manner. Since distortion is a result of the variation of a parameter relative to its nominal value, it is always desirable that the nominal value be very high compared to the absolute variation. Hence, for very low distortion, the dc gain required for the amplifier might exceed that suggested by (3.3) and (3.4). Figure 3.4 shows the simulated effect of using a nonlinear open-loop characteristic for the amplifier. A quadratic characteristic was used to introduce an absolute gain variation of about 2 dB over ± 0.4V. The second harmonic disappears and the third harmonic is reduced by about 10 dB when the gain is increased from 40 dB to 100 dB.

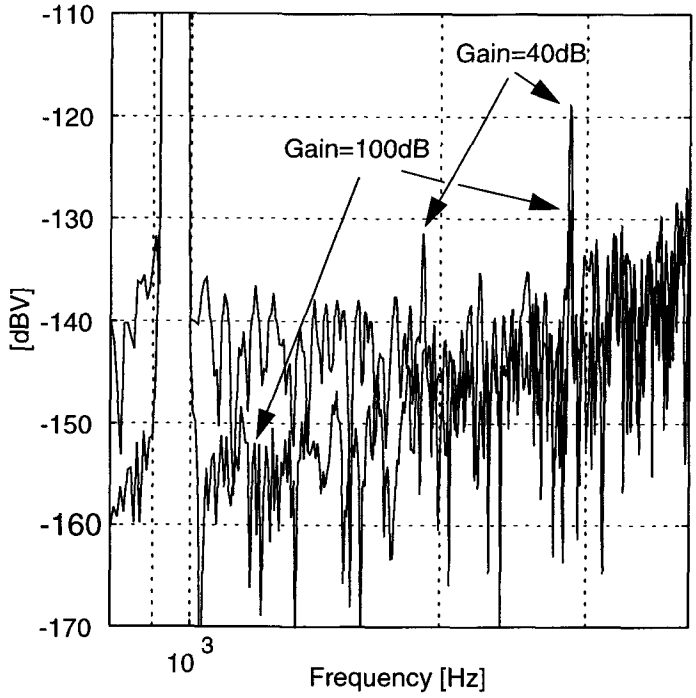

Figure 3.4: Effect of the nominal dc gain on distortion. The input signal was a -17.4 dBV (-10 dBr), $3/\pi$ kHz sinewave, and the sampling frequency 2 MHz.

The problem of harmonic distortion is especially critical when designing for low-voltage operation, as the devices require a minimum applied voltage to attain the gain and bandwidth specifications. Hence, to remain in the high-gain region of the amplifiers, signals have to be scaled down considerably, which reduces the *SNR*. This topic and others will be discussed in detail in the sections to follow.

3.2 THE FIRST INTEGRATOR

The most common sources of noise which can impair the performance of the modulator are the white noise sampled at the input, component noise (flicker noise and white noise), clock jitter (important in high-performance, high-frequency applications), finite amplifier gain and bandwidth, nonlinearity of components (capacitors and switches), clock injection, and amplifier offset and open-loop nonlinearity. If these errors occur in the first integrator, their transfer function to the output is nearly unity. Hence, a successful design necessarily reflects an awareness of these problems, and ways of coping with them.

In general, these nonideal effects cannot be handled in isolation; improvement in certain areas will lead to degradation in others. In the following sections, we analyze these trade-offs in detail.

3.2.1 The choice of the reference voltage and the sizing of the sampling capacitor

The internal A/D converter and D/A converter (Figure 2.4) establish an interface between the analog front-end of the modulator and its digital output. Since the digital output is a representation of the analog input signal, a basis for conversion is required. This basis, or measure, is the reference voltage V_{REF}. The reference voltage is the upper bound for the maximum value of the amplitude of the input signal, and is related to the Most Significant Bit (MSB) in the A/D and D/A converters. In a multibit representation, with $\pm V_{REF}$ used, the range $\pm V_{REF}$ is divided into a number of subranges (equal to one Least Significant Bit -- LSB), each being assigned a digital code. In a single-bit representation, the signal is encoded into a sequence of ones and zeros, corresponding to a sequence of two levels $\pm V_{REF}$ (sign detector).

A single-bit delta-sigma modulator requires only a comparator and a latch to realize the quantizer and the A/D converter, and a switch to realize the D/A converter in its simplest implementation. This switch toggles between $+V_{REF}$ and, $-V_{REF}$ as a function of the output signal y, and the sequence thus generated is compared to the input signal x. The running average of that sequence of positive and negative pulses is the analog representation of x.

Since the algorithm is based on a comparison between the input signal x and the reference voltage (from the internal DAC), Figure 2.4, the efficiency of the technique is affected by the noise present at those two nodes, in other words, by the signal-to-noise ratio. Hence, an improvement can be obtained either by increasing the input signal power, that is V_{REF}, or by decreasing the noise floor, or both. How large can the reference be? Ignoring the gain and phase errors α and β (they are irrelevant in this analysis, as will become apparent), the output voltage of the first integrator can be shown to be (Figure 3.1)

$$U_1 = k_1 \cdot \left[z^{-1}X - z^{-1}\left(1 - z^{-1}\right)E_Q\right] \tag{3.5}$$

where E_Q, the quantization noise introduced by Q, is uniformly distributed between $-V_{REF}$ and V_{REF}. Hence, at the onset of overloading, say $|x| = \alpha \cdot V_{REF}$ (Chapter 2), the maximum value that U_1 can assume is

$$\left|U_1\right|_{max} \cong (2 + \alpha) \cdot k_1 \cdot V_{REF} \tag{3.6}$$

The scaling factor k_1 and the reference voltage must be chosen so as to prevent the amplifier from leaving its high-gain region (say, $\pm V_{MAX}$), to avoid distortion. (From this perspective, the high-gain region of an amplifier depends on the nominal gain and permissible deviation from that value.) For a 2nd-order modulator, $\alpha \cong 0.7$. If

V_{REF} = 0.6 V and V_{MAX} = 0.4 V, then we must have $k_1 \leq 0.25$. Although such a large output occurs very seldom, with greater incidence in highly oversampled systems (Figure 3.5), it should not be exceeded to prevent early overloading of the modulator. Furthermore, a very large number of samples with values close to the maximum given by (3.6) does occur, reinforcing the need for such care.

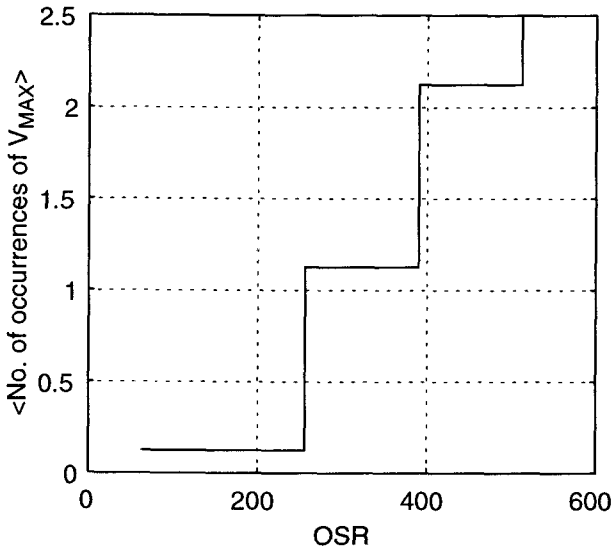

Figure 3.5: Average number (simulated) of occurrences of V_{MAX}, per period of the (sinusoidal) input signal, as a function of the oversampling ratio.

Although expression (3.6) suggests that we have two degrees of freedom, this is not necessarily true. Indeed, in Chapter 2 we concluded that achieving minimum power dissipation requires making the reference voltage as large as possible relative to the power supply voltage. For this reason, the choice of the reference voltage should not be based on (3.6), rather it should be determined by constraints imposed by the implementation. For example, for maximum signal swing (and dynamic range), the input and output signals should be centered at the output common-mode voltage, usually half of the power supply voltage V_{DD}. Hence, the maximum value that the reference can assume is also $V_{DD}/2$,

which would correspond to utilizing the power supply rails (0 and V_{DD}) as the reference voltages. This, however, can impact significantly the performance of the system, as noise (mostly from switching digital circuitry) may corrupt the power supply. Therefore, V_{REF} should be chosen such that it can easily be generated on-chip. Generating a reference voltage on-chip implies that a buffer stage has to be implemented to supply current to the load. This function is most efficiently realized if the devices of the output stage of the buffer operate in the region of highest gain. Hence, the voltages generated cannot be too close to the power supply rails, as the devices must operate in their saturation region. System requirements (interface compatibility, etc.) may impose additional restrictions on the value that the reference can assume.

Once the maximum value for V_{REF} has been identified, equation (3.6) can then be used to calculate the maximum value of the scaling coefficient k_1, based on the knowledge of the region of high gain of the amplifiers. If the latter is not known precisely at this point, a somewhat conservative approach should be followed. It is worth noting that the scaling coefficients should also be made as large as possible, since this results in larger signal-to-noise ratio.

Interestingly, equation (3.6) corroborates the otherwise empirically found results proposed by other authors as the "optimum" scaling coefficient for the first stage, $1/2$ in [37] and $1/3$ in [38]. Clearly, the maximum value that k_1 should assume is

$$k_{1max} = \frac{1}{2+\alpha} \tag{3.7}$$

which will happen when $|U_1|_{max} = V_{REF}$. Note that the objective is to maximize the reference voltage to improve the dynamic range, which should then be as close as possible to V_{DD}. If $V_{REF} = V_{DD} - \Delta V_1$ and $|U_1|_{max} = V_{DD} - \Delta V_2$, attaining low-power in a low-

voltage environment invariably requires $\Delta V_1 \leq \Delta V_2$. This is an entirely new design philosophy, when compared to a 5 V (or more) design.

Since α is close to one, (3.7) indicates an optimum value close to $1/3$. (In [38] the authors utilized a 2+1 cascaded topology, where the overload point is determined by a first order section; hence $\alpha \cong 1$.) Note that this says that the scaling coefficients should be such that the maximum value of signals internal to the system should equal the value of the reference voltage. In principle, if there are no constraints regarding the minimum value of V_{REF}, it should be always possible to attain such condition; as the power supply voltage is reduced, however, this implies that the choice of the value of the reference voltage will be rigidly determined by the linear output swing of the amplifier.

To summarize this discussion, for maximum dynamic range and minimum power dissipation, the reference voltage should be made as large as possible, and equal the width of the high-gain region of the amplifier. This maximizes the scaling coefficients (higher *SNR*), and makes them independent of the power supply voltage. A larger value results in early overloading due to saturation of the amplifier, or requires a smaller scaling coefficient, with some degradation of the *SNR* (a conservative approach). A smaller value under-utilizes the linear swing of the amplifier resulting in increased power dissipation. (The amplifier noise was not considered in the foregoing discussion. Its effect will be analyzed later in this chapter.)

The other approach to improving the dynamic range of the modulator is to reduce the noise floor. The lower the noise floor, the higher the resolution. As in Chapter 2, we will assume for the moment that the (*kT/C*) thermal noise is the fundamental limiting factor; hence the size of the sampling capacitor is closely related to the noise floor.

To determine how the sampling capacitor should be sized, one requires knowledge on the implementation of the input stage. As it is shown in Figure 3.1, the integrator takes

two signals, the input signal and the feedback (reference) signal. (As discussed, both branches are critical in determining the performance of the modulator.) The reference voltage can be utilized (or fed back) in one of two forms: double- or single-valued reference. The former implies the generation of two voltages centered around the mid-rail voltage, $V_{DD}/2 \pm V_{REF}$, which are subtracted from the input signal. The latter requires only one internal voltage, $V_{DD}/2 + V_{REF}$, which is passed through a switched-capacitor branch, configured either in a positive- or negative-charge transfer mode. The selection of V_{REF} or $-V_{REF}$, or a particular configuration of the feedback SC branch, is a function of the output signal y (Figure 3.1). Figure 3.6 illustrates four possible, single-ended, implementations of these solutions, and the timing diagram.

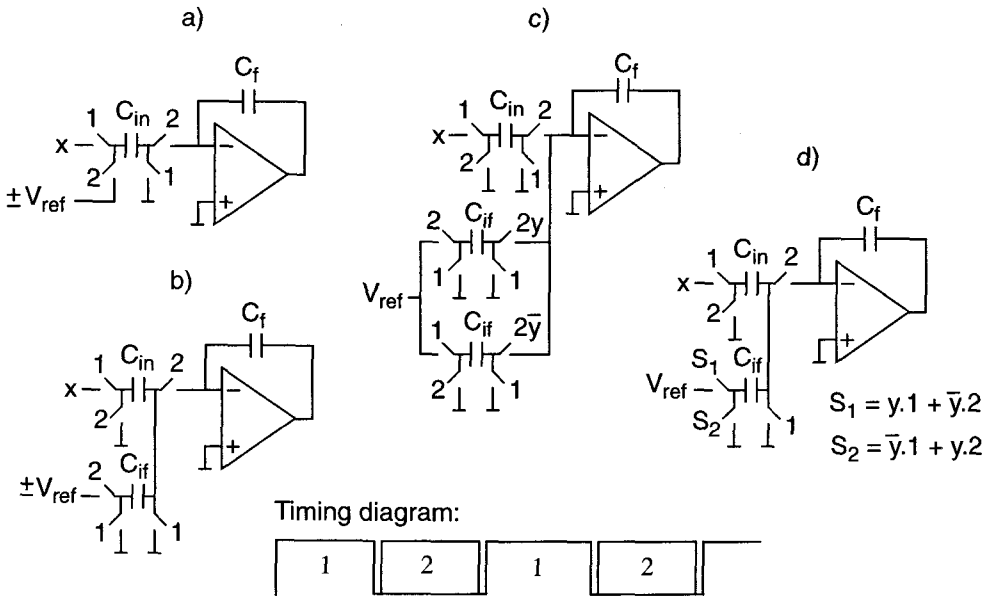

Figure 3.6: Switched-capacitor, single-ended implementation of the first integrator with a) double reference voltage -- single input branch, b) double reference voltage -- two input branches, c) single reference voltage -- three input branches, and d) single reference voltage -- two input branches.

These solutions present both advantages and disadvantages. The one depicted in Figure 3.6a takes the least area, and since the input signal and reference paths share the input capacitor, it also contributes the least noise power (*kT/C* noise as well as charge injection). A disadvantage of this solution is that incomplete settling of the reference voltage buffers results in a residual term which is a function of the input signal, thus causing distortion. A way to circumvent this difficulty is shown in Figure 3.6b, where an additional SC branch is utilized for the feedback signal. Now, the residual term resulting from the incomplete settling of the reference buffers is not a function of the input signal, resulting only in a gain error. (Later in this chapter we will analyze in greater detail the effects of non-idealities associated with the feedback path.) An important drawback is that two contributions of *kT/C* noise are present, one from C_{in} and another from C_{if}.

To evaluate the effects of both capacitors on the noise performance, one must refer the total noise power to the input, since this is where the input signal is applied. Referring the feedback signal to the output of the integrator, and then to the input, one concludes that the noise power at the input node e_T^2 is

$$\begin{aligned} e_T^{\,2} &= e_{C_{in}}^{\,2} + e_{C_{if}}^{\,2} \\ &= \frac{2 \cdot kT}{OSR \cdot C_{in}} + \frac{2 \cdot kT}{OSR \cdot C_{if}} \cdot \left(\frac{C_{if}}{C_f}\right)^2 \cdot \left(\frac{C_f}{C_{in}}\right)^2 \\ &= \frac{2 \cdot kT}{OSR \cdot C_{in}} \cdot \left(1 + \frac{C_{if}}{C_{in}}\right) \end{aligned} \tag{3.8}$$

If C_{if} is much smaller than C_{in}, the contribution of the feedback path is negligible. But this requires that the input signal amplitude be much reduced to prevent overloading. (The technique is useful, however, in the implementation of a low-amplitude dither signal.) In practice, $C_{if} \geq C_{in}$ and the total input referred noise power is at least doubled. Hence, to maintain the signal-to-noise ratio C_{in} also has to be, at least, doubled for the same reference voltage. A larger capacitance results in increased power dissipation.

The structure in Figure 3.6c has the advantages and drawbacks of the one in Figure 3.6b, but requires only one internal voltage, with the benefit of lower power dissipation and perhaps smaller area. Note that although the structure in Figure 3.6c requires three input SC branches, the differential implementation requires only one additional input branch, as the ones implementing the feedback path would be shared (they are not used simultaneously). It is also possible to use a single SC branch to implement the feedback path when a single-valued reference is used, as shown in Figure 3.6d. This approach is not very popular, however, as the comparator has to be able to settle in the beginning of the comparison phase since it does not benefit anymore from a half of a clock cycle delay. Additional logic control circuitry is also required to provide the proper charge transfer mode.

We can now extend the results derived in Section 2.5 to determine the minimum power dissipation when we know how the input stage is implemented. Expression (2.13), here repeated as (3.9), still applies requiring only a few changes to accommodate the details of the implementation illustrated in Figure 3.6. The dynamic range at the input is given by

$$DR = \frac{\left[\sigma_x^2\right]_{MAX}}{\frac{2kT}{C_{in} \cdot OSR}} \tag{3.9}$$

where $\left[\sigma_x^2\right]_{MAX}$ is the maximum input signal power. Note that we did not assume that the maximum signal power was given by $(\alpha \cdot V_{REF})^2/2$, for reasons which will shortly become clear.

The utilization of separate SC branches for the input and feedback paths requires, as shown above, that we multiply the denominator of (3.9) by $1 + C_{if}/C_{in}$. In a fully

differential implementation, there are twice as many sources of noise, hence the denominator should be multiplied by two. However, since the signal is differential, it amounts to using a reference voltage with twice the value and the numerator should be multiplied by four. These facts can be combined to yield the following general expression for the dynamic range

$$DR = \frac{\left[\sigma_x^2\right]_{MAX} \cdot OSR \cdot C_{in}}{\left(1 + \frac{C_{if}}{C_{in}}\right) \cdot kT} \tag{3.10}$$

where C_{if} should be made equal to zero when the input and feedback paths share one single SC branch. Given the maximum value of the input signal power and oversampling ratio, one can use (3.10) to find the minimum value for C_{in} required to attain a specified dynamic range DR.

In analogy with Chapter 2, we can determine the minimum power dissipation resulting from using one or two SC branches at the input. In the more general case of two SC branches (input and feedback), the power dissipated per cycle (energy delivered) in charging and discharging C_{in} and C_{if} is

$$P_{2SC} = C_{in} \cdot V^2_{xmax} + C_{if} \cdot V^2_{REF} \tag{3.11}$$

where V_{xmax} is the maximum amplitude of the input signal (previously $\alpha \cdot V_{REF}$). In general we have

$$C_{in} \cdot V_{xmax} = \alpha \cdot C_{if} \cdot V_{REF} \qquad (\alpha \leq 1) \tag{3.12}$$

Expression (3.12) states that the charge stored in capacitor C_{in} cannot exceed that stored in the feedback capacitor C_{if}. (If $C_{if} = C_{in}$, the input signal amplitude cannot be larger than the reference voltage.) Substituting (3.12) in (3.11) yields

$$P_{2SC} = C_{in} \cdot \left(\frac{C_{if}}{C_{in}} \right) \cdot \left[1 + \alpha^2 \left(\frac{C_{if}}{C_{in}} \right) \right] \cdot V^2_{REF} \tag{3.13}$$

Using (3.10) and (3.12) (the maximum input signal power is $\left[\sigma_x^{\,2}\right]_{MAX} = V^2_{xmax}/2$) we arrive at

$$P_{2SC} = \frac{2 \cdot kT \cdot DR}{OSR} \frac{(1 + C_{if}/C_{in}) \cdot \left[1 + \alpha^2 (C_{if}/C_{in}) \right]}{\alpha^2 (C_{if}/C_{in})} \tag{3.14}$$

The power, as given by (3.14), displays a minimum at $C_{if}/C_{in} = 1/\alpha$. Attaining this minimum requires scaling the input and feedback signals differently, in such a way that the input signal can be made as large as the reference voltage (see (3.12)). For this reason, making $C_{if} = C_{in}$ does not yield a minimum power solution, except (as mentioned in Chapter 2) in topologies in which overloading is determined by a first-order section ($\alpha \cong 1$). When $C_{if}/C_{in} = 1/\alpha$, (3.14) can be simplified to give

$$P_{2SC,\,MIN} = \frac{2 \cdot kT \cdot DR}{OSR} \left(\frac{1 + \alpha}{\alpha} \right)^2 \tag{3.15}$$

When the input stage uses only one SC branch, as in Figure 3.6a, the power dissipated per cycle in charging and discharging C_{in} is given by

$$P_{1SC} = C_{in} \cdot (\alpha \cdot V_{REF})^2 + C_{in} \cdot V^2_{REF} \qquad (3.16)$$
$$= \frac{2 \cdot kT \cdot DR}{OSR}\left(\frac{1+\alpha^2}{\alpha^2}\right)$$

Note that (3.16) does not result from minimizing a more general expression for the power, as with (3.15). Figure 3.7a shows the ratio between $P_{2SC,MIN}$ and P_{1SC} as a function of α, and Figure 3.7b shows $P_{2SC,MIN}$ and P_{1SC} normalized by $2 \cdot kT \cdot DR/OSR$. The minimum value of the power dissipation occurs for $\alpha = 1$, in both cases; or when the modulator does not overload for inputs weaker than the reference voltage. Moreover, configurations utilizing two SC branches always dissipate power than those using only one.

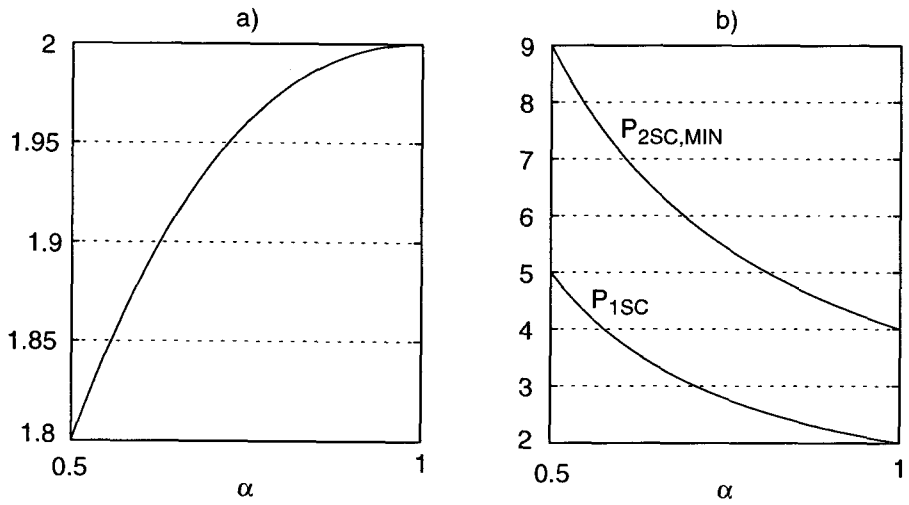

Figure 3.7: a) Ratio between $P_{2SC,MIN}$ and P_{1SC}. b) $P_{2SC,MIN}$ and P_{1SC} normalized to $2 \cdot kT \cdot DR/OSR$.

Figure 3.8 plots the minimum size of the input capacitor and associated power dissipation as a function of the power supply voltage, when one and two SC branches are

utilized in the input stage. These plots were obtained for $DR = 16$ bit, and $OSR = 256$. It was assumed that the reference voltage could not exceed $V_{DD}/2 - 0.3$, and that the minimum allowed size for C_{in} was 0.2 pF (due to matching requirements, charge injection, etc.). The power supply voltage varied between 1.5 V and 5 V.

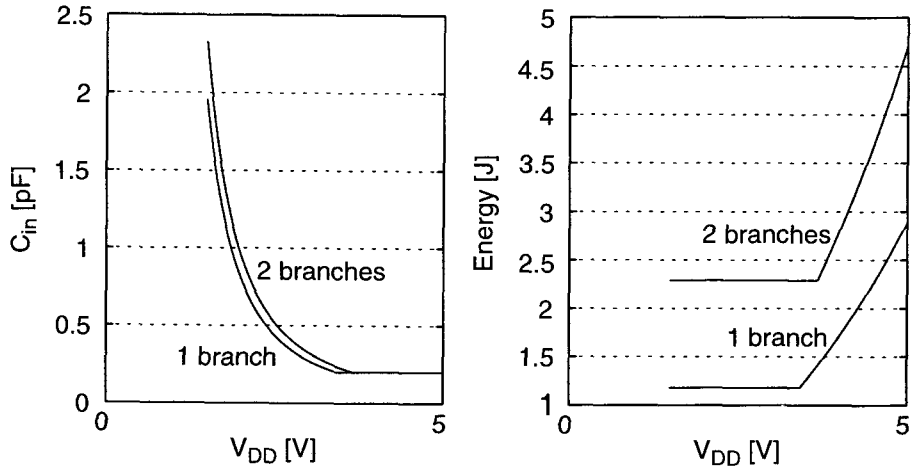

Figure 3.8: a) Minimum size of the input capacitor when one and two SC branches are utilized in the input stage, as a function of V_{DD}, and b) Power dissipation per cycle (energy) when one and two SC branches are utilized in the input stage, as a function of V_{DD}.

A few remarks are in order regarding this Figure. First, as the power supply voltage is reduced, larger values of the input capacitor are required to maintain the same dynamic range constant. This, however, does not result in increased power dissipation! Equations (2.12) and (3.10) indicate that $DR, P_{MIN} \propto C_{in} \cdot V^2_{REF}$. Since DR is kept constant through an appropriate exchange of the value of the reference voltage and the value of the input capacitor, P_{MIN} remains constant as well. The curves show a breakpoint around $V_{DD} = 3.4\,\text{V}$ and $V_{DD} = 3.6\,\text{V}$, for one and two input branches, respectively. (These values depend on the choice of parameters utilized in the generation

of the plots.) Above the breakpoint, the capacitance required to maintain the specified dynamic range is smaller than the designated minimum of 0.2 pF, and the power dissipation increases simply because V_{REF} is increasing which, for constant C_{in}, implies an increase of the dynamic range. When two branches are utilized, the noise floor is higher, thus requiring larger capacitors. Note that the optimization of the input and feedback capacitor ratio for minimum power dissipation results in a total input and feedback capacitance smaller than that obtained, had the relationship $C_{if} = C_{in}$ been used. (The ratio of the two total input capacitances equals $(1+\alpha)^2/4$, which is always less than one. This results from the necessity to increase the size of the input capacitor C_{in} when $C_{if} = C_{in}$, to maintain the dynamic range constant, due to the lower maximum value that the input signal can assume.)

The foregoing analysis assumed that the noise floor was determined by *kT/C* noise. In practice, a number of noise sources and non-idealities have to be taken into account as well. To the total *kT/C* noise power, one should add the noise from the amplifier (intrinsic noise). The amplifier contributes mostly two types of noise: thermal and flicker noise (also known as 1/*f* noise). The former can be treated analogously to *kT/C* noise, as it possesses identical properties (white, wideband). Lowering this component will require typically larger biasing currents in the amplifier, since it is inversely proportional to a transconductance (the gate-referred thermal noise spectral density of a MOSFET in saturation is $S(f) = 8kT/(3g_m)$). Flicker noise may or may not play an important role, depending on the bandwidth of interest and on the implementation. This type of noise is usually attributed to trapping and releasing of carriers between the oxide and inversion layer (McWhorter's number fluctuation model [39][40]), with a distribution of time constants (superposition of Lorentzian, or generation-recombination, spectra). Since it displays a spectral density which varies approximately inversely with frequency, the energy is concentrated at low frequencies and is hardly affected by oversampling [41]. To reduce the flicker noise power, the area of the critical devices should be increased. Circuit techniques such as correlated double sampling (Chapter 5) and chopper stabilization

[41][61], can be used as well. However, if the signal band does not extend to values near dc, it may not be of concern.

Capacitor matching may also be a relevant factor. In a delta-sigma modulator, unlike in other SC filter applications, the matching between the sampling and integration capacitors is not very important, as it results in a linear gain error only. However, in a fully-differential structure it is important that both sides of the topology match well, otherwise even-order distortion arises. This requires careful layout techniques and typically imposes a limitation on the minimum value of the capacitors. For instance, if capacitors C_1 and C_2 are to match well, and due to process variations they see a small deviation from their nominal values of ΔC_1 and ΔC_2, respectively, then their ratio can be approximated by

$$\frac{C_1 + \Delta C_1}{C_2 + \Delta C_2} \cong \frac{C_1}{C_2} \cdot \left(1 + \frac{\Delta C_1}{C_1} - \frac{\Delta C_2}{C_2} \right) \tag{3.17}$$

The error term $\Delta C/C$ can assume values as large as 20%, being larger for smaller geometries of C (inaccuracy of the lithographic process). However, if capacitors C_1 and C_2 are closely spaced and of identical size, ΔC_1 and ΔC_2 will track and the two error terms in (3.17) tend to cancel. The minimum size for a given accuracy is dependent on the process and has to be determined experimentally [42][43].

Another aspect which may restrict the minimum size of the sampling capacitor is clock charge injection (Appendix B). The latter occurs during the falling edge of the clock signal, to which typically corresponds the sampling of the input signal. Charge injection is due to the overlap capacitances and the channel charge of the switches. It results in an error term ΔQ in the charge Q representative of the input signal, stored in the sampling capacitor. (This error term usually contains dc as well as signal dependent components.) To minimize $\Delta Q/Q$, one can minimize ΔQ, maximize Q or both. To minimize ΔQ, small

geometry switches must be used; and to maximize Q we must use a larger input sampling capacitor. It should be noted, however, that these procedures are not decoupled: a larger capacitor may require wider switches for settling accuracy. A compromise has to be reached.

These issues, *kT/C* noise, amplifier noise, matching and charge injection, must be taken into consideration when sizing the input capacitor, if minimum power dissipation is to be attained. (If a particular phenomenon is not well understood, the system has to be overdesigned to assure sufficient robustness, and hence more power is dissipated.) If these contributions are made negligible compared to *kT/C* noise, then the previous analysis prevails.

Substrate noise is an increasingly important problem, as larger mixed-mode systems are integrated on the same die. Noise due to the switching activity of digital blocks propagates through the substrate corrupting sensitive analog nodes. This noise is not reduced by the choice of the input capacitor, and if the *kT/C* noise floor is very low, it may render the previous analysis useless. The best defense against substrate noise is the utilization of fully differential topologies, careful layout techniques which do not destroy symmetry, and physical isolation of analog and digital blocks.

3.2.2 The operational amplifier

The main function of an operational amplifier in linear active circuits is that of creating a virtual ground -- a node with constant voltage that sinks no current. Seemingly trivial, this feature is essential to analog processing. A requisite for zero current sinking is the utilization of high-input-impedance devices, hence MOS technologies are preferred. Constancy of the input node voltage requires a linear, low-noise, high-gain amplifier. Moreover, the amplifier time constant has to be low enough to permit settling within the specified accuracy.

For proper operation, the devices inside the amplifier require adequate biasing conditions. These conditions translate into the requirement of a minimum gate overdrive voltage and drain current (MOS devices). Performance and power supply, therefore, determine the power dissipation of an amplifier. The following sections analyze these issues in the light of the material of the previous Section.

3.2.2.1 Power dissipation

Operational amplifiers are composed of several (often many) transistors with various functions. Each device can be modeled by a set of parameters which include a number of nonideal elements. Among these we count capacitive and resistive parasitic elements. Each node in the signal path can be characterized by an equivalent impedance, with a resistive and a capacitive component, and hence a time constant. For this reason, an operational amplifier can display numerous poles in its transfer function. However, only a few have a sufficiently low frequency to be of concern. These, so-called dominant poles, are associated with high-resistance, high-capacitance nodes, typically output stage nodes. Hence, a single-stage amplifier, if properly designed, has one dominant pole; a 2-stage amplifier has two dominant poles, and so forth. In practice, a 2-pole description might be more rigorous, even for a single-stage amplifier. However, if the phase margin is large (say, greater than 70^{o}), then a single-pole description is appropriate and preferable. In the remaining of this section we concentrate on amplifiers which can be described by a first order transfer function. Chapter 4 analyzes 2-stage amplifiers with Miller frequency compensation.

A single-stage amplifier can be simplistically modeled as shown in Figure 3.9a. The stage is characterized by an input transconductance, and an output conductance and capacitance. Figure 3.9b shows the same amplifier in a feedback configuration, as in the transfer mode in a switched-capacitor integrator.

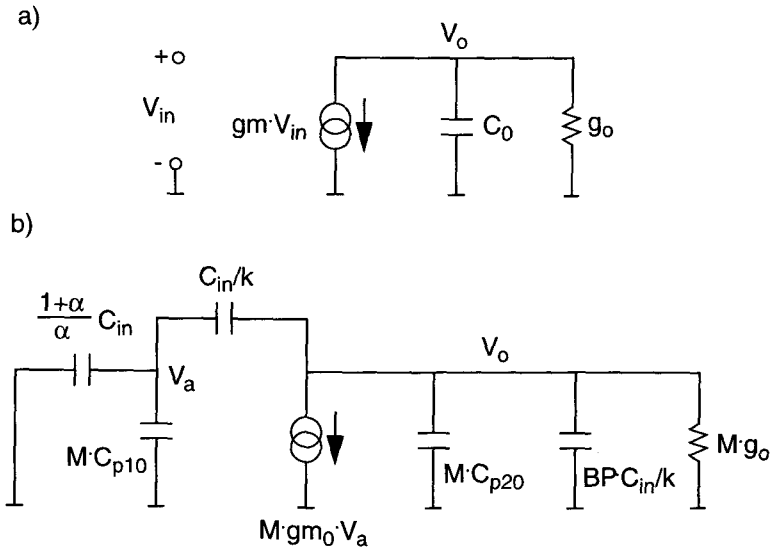

Figure 3.9: Small-signal model of a single-pole amplifier in a) stand-alone configuration. b) feedback configuration.

The amplifier was modeled as consisting of a number M of elementary amplifiers in parallel, each characterized by input and output elementary parasitic capacitances C_{p10} and C_{p20}, an elementary output conductance g_o, and a current density. The current density determines the current I_0 flowing through the elementary stage, such that the total current equals $M \cdot I_0$. The performance of the circuit can thus be controlled by varying M, and by varying the current density (through the gate overdrive voltage $V_{GST} = V_{GS} - V_T$). In the analysis to follow, it is assumed that the input and output devices are designed to have the same, small perhaps, gate overdrive voltage. A small V_{GST} is recommendable in devices contributing to the gain of the stage (high g_m/I ratio), but not for elements in current sources. One of the issues which arises from using small V_{GST} in the devices composing current sources, is a poor control of the current flowing in that branch (matching to the reference current), resulting in significant variations in the operating point (hence performance) with process variation. This means, of course, that the power

dissipation is poorly controlled as well. Another issue relates to current modulation from power supply noise. Noise in the power supply line introduces variations in the gate overdrive voltage; to minimize this effect, or improve the power supply rejection, the ratio $\Delta V_{GST}/V_{GST}$ should be kept small. The only variable within strict control of the designer is V_{GST}, which should consequently be made as large as reasonably possible. In low-voltage operation, however, the V_{GST} of all the devices in the output stage should be small for large swing, current sources included. This condition will require a compromise and a careful evaluation of the matching and noise requirements.

Matching considerations were partly the motivation for modeling the amplifier as a parallel combination of several (M) elementary amplifiers. The total current in the stage is obtained by adding replicas of a reference (bias) current several times. Since the devices have the same dimensions and the same terminal voltages, the drain currents have superior matching. Another reason is that it greatly simplifies the analysis, as most parameters can be expressed as the product of an elementary parameter and the (common) multiplicity M of the device.

In Figure 3.9b, the value of the input capacitor combines the loading effect of both input and feedback capacitors, C_{in} and C_{if}, such that minimum power dissipation is achieved (cf. Section 3.2.1). The integration gain k is defined as the ratio between the input capacitor C_{in} and the integration capacitor C_f. Also included in the model is the effect of the bottom-plate ($BP < 1$) capacitance of the integration capacitor. Since we expect the power dissipation of the amplifier to increase with the capacitive load, the condition which corresponds to minimum power dissipation in the process of sampling the input signal, $C_{if}/C_{in} = 1/\alpha$, also corresponds to minimum static power dissipation for the amplifier, as the total input capacitance is then minimized.

Using a quadratic model for the MOS devices [44], the input transconductance can be expressed as

$$gm = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}\left(M \cdot \frac{B}{2} \cdot V^2_{GST}\right) = M \cdot B \cdot V_{GST} \tag{3.18}$$

where $B = k' \cdot (W/L)_0 \cdot (1 + \lambda \cdot V_{DS})$ contains information about the transconductance of the unit devices and the channel modulation effect. Applying the KCL to the network in Figure 3.9b, one can determine its natural frequency, which is the *closed-loop* bandwidth BW (pole) of the amplifier. It can be shown (Appendix A) that the following relationship holds:

$$M^2 + \frac{a \cdot BW + gm_0 + b \cdot g_o}{c \cdot BW + d \cdot g_o} \cdot C_{in} \cdot M + \frac{e \cdot BW}{c \cdot BW + d \cdot g_o} \cdot C^2_{in} = 0 \tag{3.19}$$

Expression (3.19) relates four important parameters in the design of an amplifier: the bandwidth (hence the settling time), the gate overdrive voltage (through gm_0 and g_o), the size of the devices (through the multiplicity M of the elementary stage), and the dynamic range (through the size of the input capacitor C_{in}). The coefficients a through e depend on the parasitics of the elementary stage and on parameters which will typically remain constant (with possible exception of the integration gain k). However, (3.19) appears in a rather convoluted form, and some simplification would be desirable. For that purpose we will investigate the effect of discarding the terms containing the output conductance g_o. Solving (3.19) for the closed-loop bandwidth BW when g_o is present and when it is not, and taking the ratio of the two results, one arrives at

$$\frac{BW_{\text{with } g_o}}{BW_{\text{without } g_o}} = 1 + \frac{g_o}{gm_0} \cdot \left[1 + k \cdot \left(1 + \frac{1}{\alpha} + M \cdot \frac{C_{p10}}{C_{in}}\right)\right] \tag{3.20}$$

For typical values of the parameters involved, $g_o/gm_0 \approx 10^{-2}$, $C_{p10}/C_{in} \approx 10^{-2}$, $k, \alpha \approx 10^{-1}$, this ratio is very close to one, even for very large values of the multiplicity M (where this simplified model is not valid anymore). We will therefore ignore the output conductance, bearing in mind the limitations of the model. Using a positive frequency notation for the bandwidth BW (equation (3.19) reflects the fact that the pole is in the left-half complex plane), (3.19) can be simplified to yield

$$M^2 + \left(a - b \cdot \frac{V_{GST}}{BW}\right) \cdot C_{in} \cdot M + c \cdot C^2{}_{in} = 0 \tag{3.21}$$

where the coefficients a, b and c are given by

$$a = \frac{1}{C_{p10}} \cdot \left(1 + \frac{1}{k} + \frac{1}{\alpha}\right) + \frac{1}{C_{p20}} \cdot \left(\frac{1 + BP}{k}\right) \tag{3.22}$$

$$b = \frac{B}{k \cdot C_{p10} \cdot C_{p20}}$$

$$c = \frac{1 + \frac{1}{\alpha} + BP \cdot \left(1 + \frac{1}{k} + \frac{1}{\alpha}\right)}{k \cdot C_{p10} \cdot C_{p20}}$$

Expression (3.21) assumes a considerably simpler form than (3.19), and explores the trade-offs among various important parameters. It can be used, for instance, to determine the maximum bandwidth attainable by varying the multiplicity M (with other parameters constant). This value can be shown to be

$$BW_{MAX} = \frac{b}{2 \cdot \sqrt{c} + a} \cdot V_{GST} \tag{3.23}$$

for which $M = \sqrt{c} \cdot C_{in}$ is required. Note that BW_{MAX} is not a function of the input capacitor C_{in} (or a very weak one if the output conductance is taken into consideration). This result is comparable to that obtained for the cut-off frequency (f_T) of an MOS device, in the sense that the maximum attainable bandwidth is determined by the *intrinsic* parameters of the device, here the unit device, and not by the surrounding circuitry. However, the value of M required to attain this maximum bandwidth is a function of the input capacitor, and hence of the power supply voltage and dynamic range. The reason for the existence of such maximum is that for moderate values of M, the feedback coefficient

$$\beta = [1 + (1/\alpha + 1) \cdot k + M \cdot (k \cdot C_{p10}/C_{in})]^{-1} \tag{3.24}$$

remains essentially constant, and since the transconductance increases with M, so does the bandwidth. As M assumes very large values, however, β decreases, virtually forcing the amplifier into open-loop operation, with a larger time constant.

At this point it is pertinent to analyze the coefficients in (3.22) for magnitude. The exact quantification of these parameters requires knowledge of the topology of the amplifier, as well as the process parameters and dimensions of the devices used in the elementary amplifier. Two architectures which can be described in a fairly accurate manner by the model in Figure 3.9 are the cascode amplifier (also called telescopic cascode) and the folded cascode amplifier, shown in Figure 3.10. These structures were chosen for their popularity, although some other topologies would also be good candidates. The objective is to identify the origin of the parasitic capacitances C_{p10} and C_{p20}. (The utilization of cascoding justifies even further neglecting of the output conductance in our model.) The input parasitic capacitance C_{p10} contains three terms: one from the gate-to-channel capacitance, and two others due to the thin-oxide overlap of the gate and the drain and source diffusions of device M1. The first term assumes values in the order of 40 fF for n-type devices with an elementary area of about 20 μm^2 (0.6 - 0.8

μm processes). For the same area, the other two terms assume values in the order of 5 fF. If we opt to use p-type input devices, these values increase by a factor of two to three, due to the lower hole mobility (thus requiring wider devices to attain the same current density). Hence, $(C_{p10})_N \approx 5 \cdot 10^{-14}$ F and $(C_{p10})_P \approx 10^{-13}$ F. Note that the gate-drain overlap capacitance was simply added to C_{p10}, as the cascode device greatly reduces the Miller multiplication effect.

The output parasitic capacitance C_{p20}, which is the same for both implementations, contains four terms: two drain-to-bulk junction capacitances and two thin-oxide overlap capacitances (gate-to-drain), from the n- and p-type devices. The first two assume values in the order of 20 - 30 fF, and the last two in the order of 5 fF. Hence C_{p20} has the same order of magnitude as C_{p10} for n-type input: $C_{p20} \approx 5 \cdot 10^{-14}$ F.

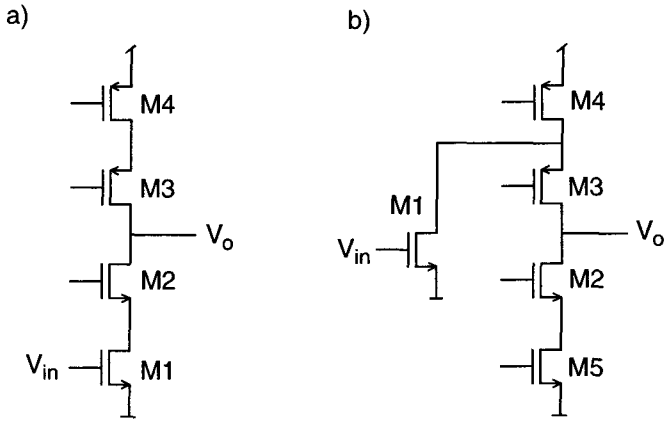

Figure 3.10: Simplified single-ended implementation of a a) telescopic cascode amplifier. b) folded-cascode amplifier.

The parameter $B = k' \cdot (W/L)_0 \cdot (1 + \lambda \cdot V_{DS})$ assumes values in the order of 300 μA/V^2, hence $B \approx 3 \cdot 10^{-4}$ A/V^2. The capacitance associated with the bottom plate of

a capacitor is about 15% to 30% of its nominal value, therefore $BP \approx 2 \cdot 10^{-1}$. As discussed in the previous section, α, $k \approx 5 \cdot 10^{-1}$. Introducing these orders of magnitude in (3.22) one obtains $a \approx 10^{14}\,\mathrm{F}^{-1}$, $b \approx 10^{23}\,\mathrm{AV}^{-2}\mathrm{F}^{-2}$ and $c \approx 10^{27}\,\mathrm{F}^{-2}$.

Figure 3.11a plots the static power dissipation P_A of a single-stage amplifier as a function of the power supply voltage V_{DD}. Figure 3.11b plots the ratio between the amplifier static power dissipation and the minimum power dissipated at the input sampling network, as derived in Section 3.2.1. These plots were obtained using the following parameters: $DR = 16$ bits, $OSR = 256$, and $V_{GST} = 0.3$ V. The reference voltage was set at $V_{DD}/2 - 0.3$ V and the integration gain was chosen to be $k = 1/(2+\alpha)$ (hence the swing of the amplifier equals the value of the reference voltage). The minimum size of the input capacitor was set at 0.2 pF. The bandwidth BW was derived as the minimum bandwidth required to achieve DR (bits) linear settling accuracy within $(3/8)\,T_S$ (this is a typical value, but we will return to this issue shortly), where T_S is the sampling period (here assumed to be 500 ns). Using this criterion, one can derive the following condition for the minimum value of the closed-loop bandwidth:

$$BW \geq 1.85 \cdot f_s \cdot DR\,[\text{bits}] \quad [\text{rad/s}] \tag{3.25}$$

The power dissipation was calculated as a result of the minimum multiplicity M required to satisfy (3.21).

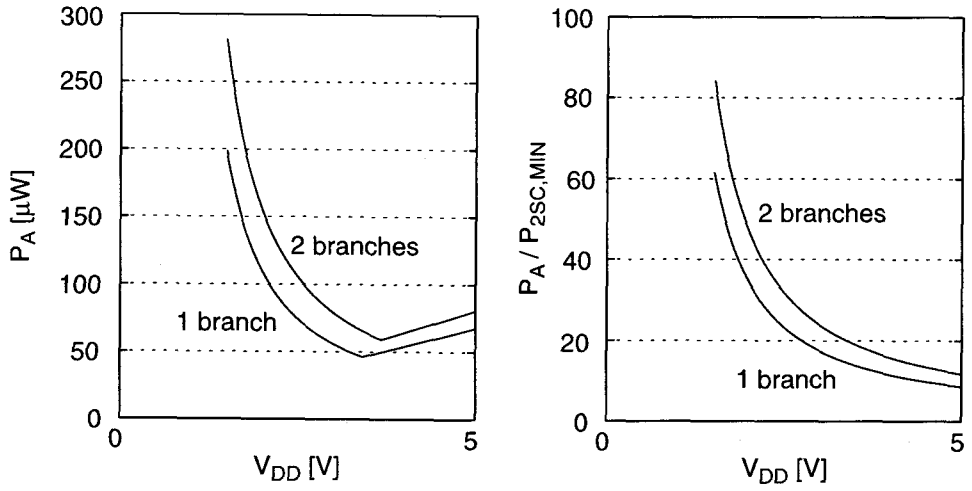

Figure 3.11: a) Amplifier (fully-differential folded-cascode) static power dissipation. b) Ratio between the amplifier static power dissipation and the minimum dynamic power dissipation in the sampling network.

As mentioned briefly in Chapter 2, the power dissipation of the amplifier increases with decreasing power supply voltage, as long as the noise floor is determined by thermal noise. Indeed, from Figure 3.11a, one can conclude that a minimum is reached when the performance starts being dominated by such type of noise (see the breakpoints at $V_{DD} = 3.4\,\text{V}$ and $V_{DD} = 3.6\,\text{V}$). When the power supply voltage is sufficiently high, the size of the input capacitor is likely to be determined by considerations related to other practical limitations or even other sources of noise. This is an interesting point, as we made no mention, for instance, of quantization noise in this analysis. The choice of a 2nd-order (or any order) structure implied that for a given *OSR*, quantization noise would not be a limiting factor. This is essentially different from the traditional approach, where topologies were chosen or optimized for low quantization noise power, because that was indeed the limiting factor. When designing for low-voltage operation, we choose a structure which is known to exceed the requirements, and then size the sampling network

to meet the specification while minimizing the power dissipation. Clearly, that minimum is reached when the input capacitance is minimized.

Figure 3.11b shows that the static power dissipation of the amplifier can exceed significantly the power dissipated in the sampling network. In Chapter 2 we mentioned that their ratio assumed typically three or more orders of magnitude. These results are not contradictory as different sources of noise, design tolerance and bias circuitry were not taken into account.

An aspect which may seem to have been overlooked is the static power dissipation due to slewing requirements. The minimum current required to prevent slewing can be easily derived. According to the criterion used to obtain (3.25), the maximum time allowed for slewing is $T_S/8$. The maximum signal step that can occur at the output of the amplifier is $k \cdot V_{REF}$, where k is the integrator gain factor, as the input signal is oversampled. It can be shown (Appendix A) that the minimum current I_{SR} required for slewing (according to this criterion) is

$$I_{SR} = 8 \cdot k \cdot \beta \cdot V_{REF} \cdot f_s \cdot C_L \tag{3.26}$$

where β is the amplifier feedback factor and C_L is the capacitive load which, in conjunction with the transconductance of the input stage, determines the time constant of the amplifier in closed-loop operation (BW). This current is to be compared with the current I_{BW} required to obtain the bandwidth BW, according to (3.21) -- from M -- and (3.25):

$$I_{BW} = \frac{1.85 \cdot f_s \cdot V_{GST} \cdot DR\,[\text{bits}]}{2} \cdot C_L \tag{3.27}$$

Taking the ratio of the two currents one obtains

$$\frac{I_{BW}}{I_{SR}} = \frac{1}{8.65} \cdot \left(\frac{1}{k \cdot \beta}\right) \cdot \left(\frac{V_{GST}}{V_{REF}}\right) \cdot DR\,[\text{bits}] \tag{3.28}$$

Figure 3.12 plots this ratio as a function of the power supply voltage when the dynamic range is 12 bits and 16 bits (the remaining parameters assume the values used previously).

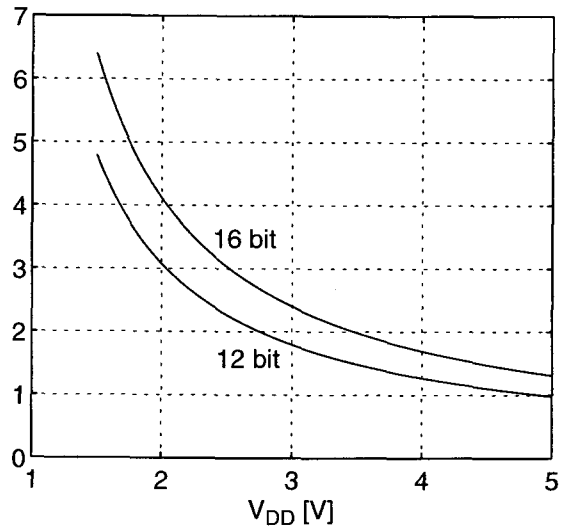

Figure 3.12: Ratio between the minimum current to obtain the required closed-loop bandwidth, and the minimum current required for slewing, for $DR = 12\,\text{bits}$ and $DR = 16\,\text{bits}$.

In general, the current required to achieve the desired settling accuracy exceeds that required for slewing, although a different combination of parameters may yield different results. The nearly $1/x$ dependence with the power supply voltage is due to the linear variation of the reference voltage with V_{DD}. The feedback factor is also a weak function of V_{DD}. In practice, we may be forced to reduce slightly the gate overdrive

voltage as V_{DD} is much reduced. The effect will, however, only moderate the steepness of the curve. The situation is aggravated for a larger dynamic range, as the load is increased to reduce the noise power. It should be pointed-out that the capacitive load seen during slewing is always smaller than the capacitive load seen during linear settling; in Appendix A it is shown that $(C_L)_{Slewing} = \beta \cdot (C_L)_{Settling}$.

Analysis reveals, however, that the previous criterion can result in increased power dissipation. Indeed, it is obvious that the current required for either settling or slewing is a strong function of the time allocated for that mode of operation. Consider a more general scenario where the time allocated for slewing is $m \cdot T_S$, and the time allocated for settling is $(0.5 - m) \cdot T_S$, with $m \in [0,1/2]$. (In practice this interval is somewhat smaller, for various reasons.) Appendix A shows that in such case the current required for settling is

$$I_{BW} = \left(\frac{\ln 2}{1-m}\right) \cdot f_s \cdot V_{GST} \cdot DR\,[\text{bits}] \cdot C_{Lac} \tag{3.29}$$

and that needed for slewing is

$$I_{SR} = \left(\frac{2}{m}\right) \cdot k \cdot \beta \cdot V_{REF} \cdot f_s \cdot C_{Lac} \tag{3.30}$$

Figure 3.13 shows pictorially the dependence of these currents on m. It is clear that the choice for m should be that where both curves meet, since it is the large value of I_{SR} and I_{BW} which determines the minimum current that will satisfy both requirements. So, m_{opt} yields minimum power dissipation. Note that this criterion may not result in a global power minimization. For instance, in a two-stage amplifier both stages can be slew-limited. The slewing in the first stage is limited by the current in the input device and the compensation capacitor, and so is the unity-gain bandwidth. Hence, m_{opt} can be determined from the first stage requirements, and its power minimized. In the second

stage, however, the level of current required to achieve a proper phase margin usually exceeds that required for slewing, and the above analysis is irrelevant. Nevertheless, some local optimization is possible. From (3.29) and (3.30) one easily arrives at

$$m_{opt} = \frac{1}{1 + \frac{\ln 2}{2} \cdot \left(\frac{DR[\text{bits}]}{k \cdot \beta} \right) \cdot \left(\frac{V_{GST}}{V_{REF}} \right)} \tag{3.31}$$

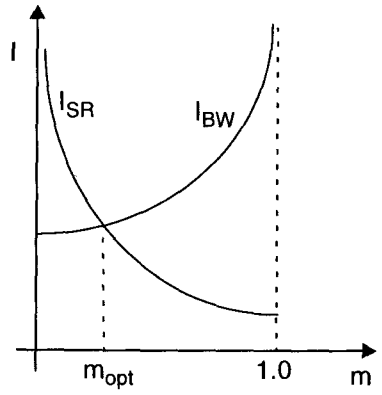

Figure 3.13: Qualitative behavior of the minimum current required for settling I_{BW} and of the minimum current required for slewing I_{SR}, as functions of the fraction m of the sampling period.

As an example, let us compare the previous situation where $m = 1/4$ with the one where we use the optimum value of m according to (3.31). The parameters are $V_{GST} = 0.3\,\text{V}$, $V_{REF} = 0.6\,\text{V}$, $DR = 16\,\text{bits}$, $k = 1/4$, and $\beta = 4/5$. Equation (3.31) yields $m_{opt} = 1/15$! This is a very small fraction of the clock cycle. From (3.29), or (3.30), we conclude that the required current is therefore, $I = 3.6 \cdot f_s \cdot C_L$. If we use $m = 1/4$, then the minimum current value is given by (3.29), as can be appreciated from Figure (3.13), yielding $I = 4.44 \cdot f_s \cdot C_L$, a value about 23% higher. Despite the huge

difference between the values of m (almost four times), the increase in the current is not proportionally larger. This is owed to the weak sensitivity of I_{BW} to variations in m for small m (see Appendix A, also Figure 3.13). Had we used a smaller value for m (smaller than m_{opt}), the increase in current would have been larger, as it would be dominated by the slewing current.

The component noise originating in the amplifier itself must be also taken into account. In the analysis to follow we will consider the contribution of thermal noise only due to its wideband characteristics.

The input-referred noise power for the topologies in Figure 3.10 is given by

$$\left(e^2_{in}\right)_{Cascode} = 2 \cdot \left[e^2_{M1} + \left(\frac{g_{mM4}}{g_{mM1}}\right)^2 \cdot e^2_{M4}\right] \tag{3.32a}$$

$$\left(e^2_{in}\right)_{Folded-cascode} = 2 \cdot \left[e^2_{M1} + \left(\frac{g_{mM4}}{g_{mM1}}\right)^2 \cdot e^2_{M4} + \left(\frac{g_{mM5}}{g_{mM1}}\right)^2 \cdot e^2_{M5}\right] \tag{3.32b}$$

where the factor 2 arises from considering a fully differential structure. A worst-case scenario occurs when all the devices are sized to have identical transconductances (the input device is typically designed to have the highest transconductance). In this situation the devices M4 and M5 possess the same noise gain as the input device M1. Hence, we need only to calculate the integrated noise power for the input device and multiply the result by the appropriate factor. To avoid tedious repetition, we will focus on the folded-cascode structure only. The results can be easily re-derived for a regular cascode structure. The input-referred power spectral density of the thermal noise for an MOS device in saturation is, as mentioned earlier, $S(f) = 8kT/(3g_m)$, and the total input-referred noise power spectral density is $S(f) = \gamma \cdot 8kT/(3g_m)$, where γ is a noise excess factor. (γ accounts for the presence of all devices, and represents their noise normalized to that of

the input transistor. Under the worst-case assumption that all devices possess the same transconductance, $\gamma = 6$.)

To calculate the total input-referred noise power, one must take into account the transfer function of the amplifier and the feedback configuration. The equivalent noise bandwidth is $B_{eq} = (\pi \cdot BW)/2$, where BW is the closed-loop bandwidth (in Hz), as defined earlier. Hence, the total baseband output noise power is given by

$$e^2_o \approx B_{eq} \cdot S(0) \cdot |H(0)|^2 \tag{3.33}$$

where $S(f)$ is the amplifier input-referred noise power spectral density, and $H(f)$ is the closed-loop transfer function of the amplifier:

$$H(f) = \frac{\frac{A_0}{1+\beta \cdot A_0}}{1+\frac{f}{BW}} \tag{3.34}$$

Substituting (3.34) in (3.33) one easily arrives at

$$e^2_o = \left(\frac{\gamma}{\beta}\right) \cdot \frac{2 \cdot kT}{3 \cdot (C_L)_{Slewing}} \tag{3.35}$$

This value has to be referred to the input of the switched-capacitor integrator, and the oversampling ratio taken into account. Moreover, by using the relationship between the capacitive loads seen during settling and slewing, further simplification is allowed. One then obtains for the total in-band input-referred integrated amplifier white noise power:

$$e^2_w = \left(\frac{\gamma}{OSR \cdot k^2}\right) \cdot \frac{2 \cdot kT}{3 \cdot (C_L)_{Settling}} \tag{3.36}$$

Expression (3.36) indicates that, to first order, the thermal noise power of the amplifier is a function of the load capacitance only (actually of the compensation capacitor), and not of the transconductance of the devices. This is particularly valid if the dominant contributor is the input device.

The total in-band noise power, as given by (3.36), will now be compared with the *kT/C* noise originating in the sampling network. Combining (3.8) and (3.36), one arrives at the following result for the total input-referred thermal noise for a differential structure (with two input SC branches sized to minimize the power dissipation):

$$e^2_{in} = \frac{4 \cdot kT}{OSR \cdot C_{in}} \cdot \left(\frac{1+\alpha}{\alpha}\right) \cdot \left(1 + \frac{\frac{\gamma}{6 \cdot k^2} \cdot \frac{\alpha}{1+\alpha}}{(C_L)_{Settling}/C_{in}}\right) \tag{3.37}$$

The right-most factor in parenthesis is the noise power excess factor due to the amplifier thermal noise:

$$\gamma_w = 1 + \frac{\frac{\gamma}{6 \cdot k^2} \cdot \frac{\alpha}{1+\alpha}}{(C_L)_{Settling}/C_{in}} \tag{3.38}$$

The expression for the capacitive load seen during settling is derived in Appendix A, and is a function of the parasitic elements, gain factor, and stage multiplicity. Using this result one obtains

$$\frac{(C_L)_{Settling}}{C_{in}} = \frac{C_{p10} \cdot C_{p20}}{C^2_{in}} \cdot k \cdot M^2 + \left\{ \left[1 + \left(1 + \frac{1}{\alpha} \right) \cdot k \right] \cdot \frac{C_{p20}}{C_{in}} + (1 + BP) \cdot \frac{C_{p10}}{C_{in}} \right\} \cdot M + \left(1 + \frac{1}{k} + \frac{1}{\alpha} \right) \cdot BP + 1 + \frac{1}{\alpha} \tag{3.39}$$

Note that for moderate values of the stage multiplicity M, the ratio in (3.39) can be approximated by the term independent of M. This weak dependence on the stage multiplicity is clearly demonstrated in Figure 3.14, which plots the noise excess factor in (3.38) as a function of the power supply voltage. For the purpose of comparison, the cases corresponding to $\gamma = 2$ and $\gamma = 6$, best and worst cases, respectively, are shown. It is clear that the total thermal noise can be significantly degraded (about a factor of two, for the set of parameters utilized) due to the contribution of the amplifier. This implies that the size of the input capacitor has to be made larger (γ_w times larger) to accommodate this excess without degrading the performance. For instance, for $\gamma_w = 3\,\text{dB}$, the size of the input capacitor doubles.

Interestingly, due to its extremely weak dependence on the size of the amplifier (M), γ_w can be estimated based solely on knowledge of the architecture (α), and the relative dimensions of the bottom-plate capacitances in the process (BP) (assuming that the optimum value of k in (3.7) is utilized). Under these circumstances, the larger the value of α, the higher the excess noise factor γ_w. This is not surprising as it corresponds to using a smaller gain factor k; once referred to the input, the amplifier noise power is divided by k^2, and it is desirable that this quantity be as large as possible. More importantly, a small α results in a larger total input capacitance, hence in a narrower equivalent noise bandwidth (less noise). Similarly, γ_w is a decreasing function of an increasing BP. Recall that the bottom-plate capacitance loads the amplifier directly (Figure 3.9b), and larger values of BP result in a higher capacitive load of the amplifier. One can therefore conclude that the steps which should be taken to minimize the power

dissipation (leading to small capacitances) are in conflict with those which should be taken to minimize the thermal noise power (leading to large capacitances).

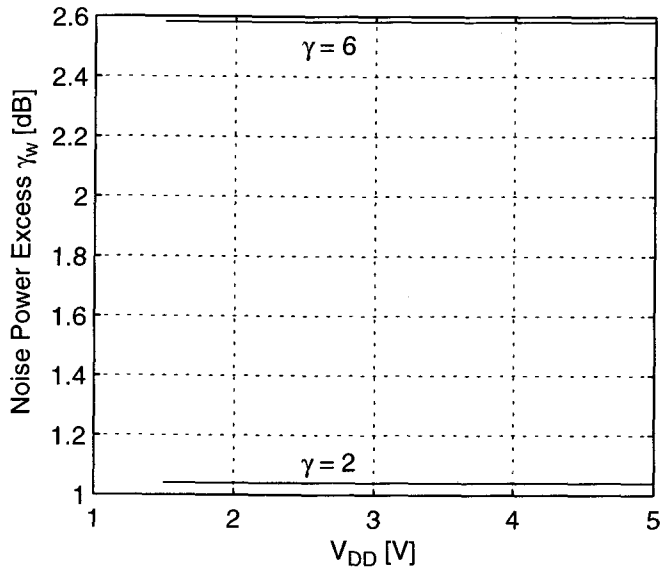

Figure 3.14: Thermal noise excess factor at the input, due to amplifier noise.

It is possible to exchange the input and output capacitance to achieve the same dynamic range while maintaining approximately constant the power dissipation of the amplifier. This exchange results neither in less total capacitor area nor lower power dissipation, and consequently might not be of obvious advantage. However, it results in smaller input capacitor sizes, which relaxes the performance requirements on the CMOS switches, and provides a heavier capacitive load during the sampling mode, therefore improving settling. (The former is particularly important in low-voltage and moderate- to high-frequency operation, and will be discussed in greater detail in Chapter 4.) The value of the input capacitor required to attain a given dynamic range in the presence of amplifier noise is, as discussed above, $\gamma_w \cdot C_{in}$, where C_{in} is determined by the *kT/C* noise in the sampling network only. It can be shown that if a capacitor with value C_o is connected to

the output of the amplifier, the noise excess factor $\gamma_w = 1 + \gamma_{w0}$ becomes (again neglecting the terms affected by the stage multiplicity)

$$\gamma_w = 1 + \frac{\gamma_{w0}}{1 + \eta \cdot \left(\frac{C_o}{C_{in}}\right)} \tag{3.40}$$

where γ_{w0} and η are given by

$$\gamma_{w0} = \frac{\gamma}{6} \cdot \frac{\frac{\alpha \cdot (2+\alpha)^2}{1+\alpha}}{\left(3 + \alpha + \frac{1}{\alpha}\right) \cdot BP + 1 + \frac{1}{\alpha}} \tag{3.41a}$$

$$\eta = \frac{1 + 3 \cdot \alpha + \alpha^2}{(2+\alpha) \cdot (1 + \alpha + BP \cdot [1 + \alpha \cdot (3+\alpha)])} \tag{3.41b}$$

The load capacitance, to which the amplifier static power dissipation is proportional, is given by

$$C_{L,\ Without\ C_o} = (1 + \gamma_{w0}) \cdot \theta \cdot C_{in}$$

$$C_{L,\ With\ C_o} = \left[1 + \frac{\gamma_{w0}}{1 + \eta \cdot \left(\frac{C_o}{C_{in}}\right)}\right] \cdot \left[\nu \cdot \left(\frac{C_o}{C_{in}}\right) + \theta\right] \cdot C_{in} \tag{3.42}$$

with ν and θ given by

$$\theta = \left(3 + \alpha + \frac{1}{\alpha}\right) \cdot BP + 1 + \frac{1}{\alpha}$$

$$\nu = 1 + \frac{1+\alpha}{\alpha \cdot (2+\alpha)} \tag{3.43}$$

Figure 3.15 plots the ratio of the load capacitance with C_o included to that without C_o, as a function of the ratio C_o/C_{in}, curve (a), and the size of the input capacitor with C_o normalized to that without C_o, also a a function of C_o/C_{in}, curve (b). The input capacitance was chosen such that the noise excess in (3.40) was unity (in order to meet the noise floor specification), and the ratio C_o/C_{in} varied. Adding capacitance to the output does indeed increase the total capacitive load C_L, but since it permits some reduction in the size of the input capacitor, this load increases more slowly than if the input capacitor had been kept constant. For the case shown, using $C_o/C_{in} = 1$ results in a load increase of about 32% and a decrease in the size of the input capacitor of 18%, while maintaining the same thermal noise performance. The load increase may not necessarily require a corresponding increase in the current of the amplifier, if the resulting error is linear and the quantization noise leakage negligible, as discussed in Section 3.1. The smaller size of the input capacitor, however, leads to smaller switches (the ON-resistance can be larger by 18%), and less associated parasitics (which improves power supply rejection and substrate noise immunity).

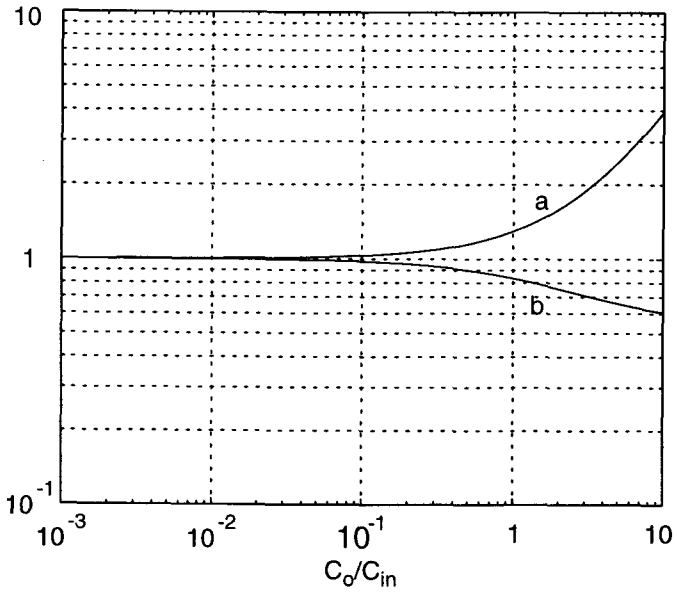

Figure 3.15: Amplifier load capacitance with C_o, normalized to that without C_o, (a), and input capacitor size with C_o, normalized to that without C_o, (b), as a function of the ratio C_o/C_{in}.

In the foregoing analysis the first stage gain factor k_1 was always given by (3.7). In connection with this expression, we discussed the effects of choosing different values for k_1 and V_{REF}. In particular, it was mentioned that using a value for the reference voltage larger than the value corresponding to the high-gain region of the amplifier, and consequently a smaller value for k_1, would result in some degradation of the *SNR* due to increased input-referred noise.

To analyze the trade-off we will make use of expressions (3.37), (3.38) and of the discussion thereof. The dynamic range clearly displays the following proportionality:

$$DR \propto \frac{V_{REF}^2}{\gamma_w} \tag{3.44}$$

where γ_w is a function of V_{REF} through (3.6). As can be appreciated from (3.38) and (3.6), γ_w is an increasing function of V_{REF} since a larger reference implies the use of a smaller gain factor k. However, this increase is weaker than the square of the reference voltage, and hence the dynamic range actually increases slightly. This means than the input capacitance can be made smaller, therefore reducing the power dissipation. Let us give a numerical example. Consider $\alpha = 0.7$, $U_{1max} = 0.4\,\mathrm{V}$, $BP = 0.2$, and $\gamma = 6$ (worst case). In principle, one would choose $V_{REF} = 0.4\,\mathrm{V}$ yielding a maximum $k = 1/(2+\alpha) = 0.37$, which is independent of the power supply voltage. Figure 3.16 plots the dynamic range, expression (3.44), as a function of the reference voltage, normalized to the value obtained when $k = 1/(2+\alpha)$. The figure plots also the gain factor k and the noise excess factor γ_w. Clearly, using a reference voltage larger than 0.4 V results in increased dynamic range. For instance, using $V_{REF} = 0.6\,\mathrm{V}$ (and $k = 0.25$) yields an improvement of about 1.7 dB in DR, relative to $V_{REF} = 0.4\,\mathrm{V}$. However, this does not take into account the increased input-referred noise power due to subsequent stages of the modulator. Noise injected at the input of the second stage, once referred to the input, will have a power about 3.4 dB larger if $V_{REF} = 0.6\,\mathrm{V}$ is used ($3.4 = 20 \cdot \log 10\,(0.37/0.25)$). This may not be of much consequence since it is first-order noise shaped, but the trade-off should be exercised carefully, or overall degradation of the dynamic range might result.

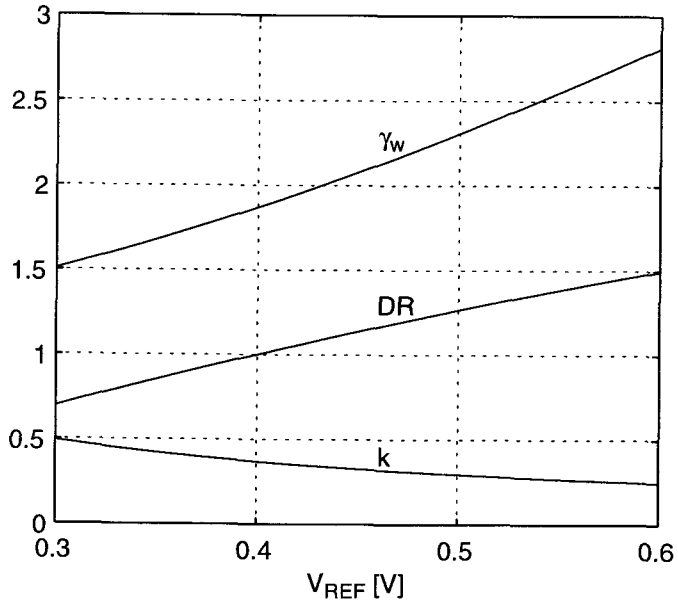

Figure 3.16: Dynamic range as a function of the reference voltage, normalized to the value obtained when V_{REF} = 0.4 V. Also shown are the excess noise and gain factors.

3.2.2.2 Biasing the operational amplifier

An important aspect of the design of operational amplifiers for low voltage operation is the bias point of the input and output stages. Large dynamic ranges can better be achieved if the signal swing is also large, therefore the operating point should be placed so as to maximize both positive and negative excursions of the signal. Moreover, they should be symmetrical, unless the requirement is explicitly different.

We will now analyze four popular amplifier structures for their biasing requirements and minimum power supply voltage. Figure 3.17 shows a basic differential pair (a), a telescopic cascode amplifier (b), a folded-cascode amplifier (c), and a 2-stage amplifier with Miller frequency compensation (d) (with only one side of the output stage

shown). (Only fully differential implementations will be considered here, since they outperform their single-ended counterparts.)

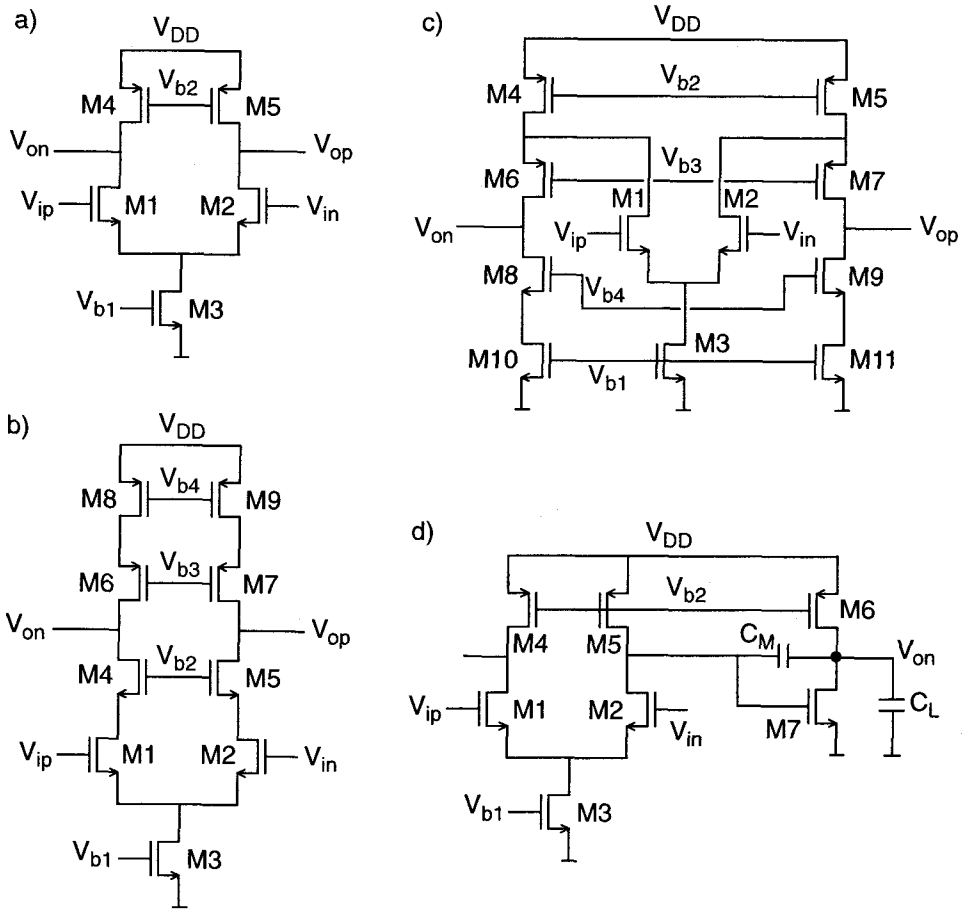

Figure 3.17: Four popular amplifier topologies: a) differential pair, b) telescopic cascode amplifier, c) folded-cascode amplifier, and d) two-stage Miller amplifier.

The traditional approach to biasing these structures is simply that of making the input and output common-mode voltages equal to half the power supply voltage, $V_{DD}/2$. However, as V_{DD} is reduced, the optimum bias point for the input stage has to be made

larger, or smaller (depending on the type of devices used in the input stage), than $V_{DD}/2$ to accommodate the asymmetry of this stage. In general, the optimum bias point for the output stage will remain equal or close to $V_{DD}/2$, since this maximizes the output signal swing. (As mentioned above, this may change if the output stage is asymmetric or if the following stage requires a low or high input common-mode voltage, for instance, a continuous-time buffer stage).

Hence, two scenarios can be pictured. One occurs when the input and output common-mode voltages are equal to $V_{DD}/2$, and the other when they can be set independently. The structures shown in Figure 3.17 utilize the same input stage (n-type input differential pair), and hence have the same requirements regarding the input common-mode voltage. For proper operation of the input devices (for the purpose of this analysis we define "proper" as operation in strong inversion and saturation), the minimum input dc voltage is $V_{Tn1} + 2 \cdot \Delta V$, where ΔV is the magnitude of the drain-source saturation voltage (here assumed to be equal for p- and n-type devices), and V_{Tn1} the threshold voltage of the input transistors. If this dc voltage is equal to $V_{DD}/2$, the minimum power supply voltage is clearly given by

$$(V_{DD})_{min} = 2 \cdot V_{Tn} + 4 \cdot \Delta V \tag{3.45}$$

In order to use a value lower than that given by (3.45), one must bias the input and output stages independently. The absolute minimum power supply voltage that can be used corresponds, according to the definition of proper operation given above, to having all the devices operate at the onset of saturation that is, when $|V_{DS}| = \Delta V$. Therefore, it is predictable that structures employing cascoding may be in disadvantage in a low-voltage operation environment. Moreover, one must assure that all the bias voltages can be generated, that is all the V_{bi}'s must belong to the interval $[0, V_{DD}]$. A quick inspection of

the structures shown in Figure 3.17 allows us to arrive at the results summarized in Table 3.1.

Structure	Minimum V_{DD} (Input device bias)	Minimum V_{DD} (Output stage bias)	Minimum V_{DD} (Bias voltages)
Differential pair	$V_{Tn1} + 2 \cdot \Delta V$	$3 \cdot \Delta V$	$\lvert V_{Tp4} \rvert + \Delta V$
Telescopic cascode amplifier	$V_{Tn1} + 2 \cdot \Delta V$	$5 \cdot \Delta V$	$V_{Tn4} + 3 \cdot \Delta V$
Folded-cascode amplifier	$V_{Tn1} + 2 \cdot \Delta V$	$4 \cdot \Delta V$	$\lvert V_{Tp4} \rvert + 2 \cdot \Delta V$
2-stage Miller amplifier	$V_{Tn1} + 2 \cdot \Delta V$	$2 \cdot \Delta V$	$\lvert V_{Tp4} \rvert + \Delta V$

Table 3.1: Minimum Power supply voltage for the amplifier structures shown in Figure 3.17.

The minimum value of the power supply voltage equals the largest of the three minima. In general, $\lvert V_{Tp} \rvert > V_{Tn}$, and the minimum power supply voltage for a folded-cascode circuit is dictated by the threshold voltage of the p-type transistors. As expected, the telescopic cascode structure requires the largest value of the power supply for proper operation, followed by the folded-cascode amplifier. Moreover, due to the body effect, $V_{Tn4} > V_{Tn1}$. When the largest term is $V_{Tn1} + 2 \cdot \Delta V$, the input common-mode voltage is set equal to V_{DD} and both input and load devices operate in saturation, therefore with high gain.

The 2-stage Miller amplifier has the same biasing requirements as the basic differential pair. However, due to the frequency compensation capacitor C_M, the output impedance of the first stage is low and the signal swing is much reduced. The output stage can swing to within ΔV of the power supply rails, giving the largest attainable range.

A numerical example is appropriate to provide insight on the order of magnitude of the minima in Table 3.1. If $|V_{Tp4}| = 0.9\,\text{V}$, $V_{Tn1} = 0.7\,\text{V}$, $V_{Tn4} = 0.8\,\text{V}$ and $\Delta V = 0.2\,\text{V}$, one obtains

$$V_{Tn1} + 2 \cdot \Delta V = 1.1\,\text{V}, \qquad 3 \cdot \Delta V = 0.6\,\text{V}, \qquad |V_{Tp4}| + \Delta V = 1.1\,\text{V}$$
$$5 \cdot \Delta V = 1.0\,\text{V}, \qquad V_{Tn4} + 3 \cdot \Delta V = 1.4\,\text{V}$$
$$4 \cdot \Delta V = 0.8\,\text{V}, \qquad |V_{Tp4}| + 2 \cdot \Delta V = 1.3\,\text{V}$$

It should be noted that the input common mode range is relatively unimportant in fully-differential SC circuits. In such structures the input stage is biased by a dc voltage (input common-mode voltage), and the input signals swing in opposite directions, therefore the common-mode voltage remains constant.

3.3 THE SECOND INTEGRATOR

Section 2.4 clearly indicated that as one progresses along the forward path towards the output node, the performance requirements become more relaxed due to the property of noise shaping. The focus of this chapter has been on determining how the various sources of noise affect the performance of the modulator and how they should be handled to minimize power dissipation. These sources of noise, namely *kT/C* noise from the sampling network and thermal noise from the amplifier, are also present at the input of the second integrator. However, due to the noise shaping property, their integrated power (over the signal band) is attenuated by a factor proportional to the square of the oversampling ratio. An oversampling ratio of 256 results in an output (integrated) noise power reduction of about 38 dB, compared to the first stage (cf. Section 2.4). Since the limiting source of noise is that with origin in the sampling network, *i.e.*, the *kT/C* noise, this means that the sampling capacitor in the second stage can be made smaller than the sampling capacitor in the first stage by the same factor.

This reduction in size is, however, limited mostly by matching requirements. To achieve good power supply rejection, it is desirable to use fully differential topologies which require good matching. Therefore, one cannot make the sampling capacitors arbitrarily small, as then they become poorly matched due to the inaccuracy of the photolithographic process. But even the matching requirements are somewhat relaxed due to noise shaping, and it is common to use capacitances in the order of 100 fF or less. From the analysis developed in this chapter, if the first stage required an input capacitor of, say 2 pF, to meet the noise specifications, the amplifier in the second stage would dissipate about 20 times less power with a 100 fF input capacitor, while maintaining the same gain-bandwidth product. Typically, the amplifier in the second stage is a down-scaled version of the amplifier in the input stage. Moreover, the amplifier in the second stage can have lower gain-bandwidth product if thermal noise is largely dominant, since this would result only in some, likely tolerable, quantization noise leakage.

In a low voltage design, the first amplifier may require a 2-stage structure in order to achieve high gain (for low harmonic distortion), and high signal swing. This requirement is somewhat relaxed in the second integrator, and a single-stage amplifier may suffice. This leads to additional savings in power dissipation. Since the signal swing is smaller in a single-stage amplifier, careful scaling is required. (Recall, however, that the gain reduction may result in excessive quantization noise leakage -- cf. Section 3.1.)

In analogy with Section 3.2.1, one can obtain the expression for the output voltage of the second integrator (Figure 3.1):

$$U_2 = k_1 \cdot k_2 \cdot \{z^{-2} \cdot X - [z^{-2} + 2 \cdot z^{-1} \cdot (1 - z^{-1})] \cdot E_Q\} \tag{3.46}$$

At the onset of overloading, the maximum value that U_2 can assume is, therefore,

$$|U_2|_{max} \cong (3+\alpha) \cdot k_1 \cdot k_2 \cdot V_{REF} \tag{3.47}$$

where α is related to the overload point of the modulator (cf. Section 3.2.1). Formerly, the scaling coefficients were typically chosen to be unity, which resulted in large swing requirements for the second-stage amplifier (about four times the reference voltage). Later, it was proposed to use $k_1 = k_2 = 0.5$ [37], which required a voltage swing equal to one reference voltage only. Expression (3.47) indicates that we have enough flexibility to set these coefficients independently if we wish, in order to accommodate differences in the amplifier topology. Solving (3.6) for k_1 and substituting in (3.47) one obtains

$$k_2 = \frac{2+\alpha}{3+\alpha} \cdot \frac{|U_2|_{max}}{|U_1|_{max}} \tag{3.48}$$

Note that (3.48) *requires* that k_1 be given by (3.6); if that is not the case, then one must use (3.47). Using a value larger than that given by (3.47) or (3.48) will result in early overloading of the modulator. Using a smaller value increases the input-referred noise, but without much consequence since it is noise shaped.

Note that the considerations above do not necessarily hold for a cascaded structure. In such case, the output signal of the second integrator is used to extract the quantization noise introduced in that section, to be cancelled at a later stage. For that reason, the amplifier still has to settle within reasonable accuracy [45].

3.4 THE COMPARATOR

The comparator is a component with less stringent performance requirements. The reason is that the non-idealities occurring in this block are shaped by a 2nd-order transfer function, therefore treated just like quantization noise. Although relaxed, its design should not be neglected, as some of the non-idealities can compromise the performance of the modulator. Let us briefly analyze this component in light of a few of its most important characteristics: dc offset, hysteresis, and gain.

Ideally, the dc offset would be completely eliminated by the loop since an ideal integrator possesses infinite gain at dc. However, the finite dc gain of the amplifiers prevents this from happening by shifting the pole frequency from $z = 1$ to $z = 1 - \beta$ (cf. Section 3.1). Therefore, a dc component in the quantization noise sequence or a dc offset in the comparator is only attenuated by $1/(\beta_1 \cdot \beta_2)$, where the β_i's are inversely proportional to the dc gain of the amplifier in stage *i*. This is the phenomenon most responsible for quantization noise leakage at low frequencies.

Hysteresis in the comparator amounts to memory in the system. If the signal is not strong enough to overcome the width of the hysteresis characteristic, the comparator will not switch states. This phenomenon modifies the loop dynamics by introducing additional poles in the system, which then create errors in the transfer functions and may compromise the stability of the loop. It is desirable to use structures with a reset phase to eliminate hysteresis, and Chapter 4 describes in more detail a structure using such technique.

The gain of the comparator determines its capability to produce a correct output in a given period of time. If the gain is very high, the comparator will respond almost immediately even to very small inputs. The inaccuracy of producing either a zero or a one for a very small input due to noise, for instance, will be averaged by the decimation filter,

and hence is of very little consequence. If the gain is relatively small, the comparator may enter a region of metastability in the presence of small input signals. When this occurs, the output of the comparator will eventually drift towards a correct decision, but it may not reach that decision at the end of the clock phase. This results in severe distortion (and constitutes another reason for not recommending the utilization of a single switched-capacitor branch when a single-reference voltage is being used, as discussed earlier in Section 3.2.1).

3.5 THE D/A CONVERTER

The D/A converter is as critical to the overall performance of the modulator as the first integrator; any errors introduced during the sampling of the reference voltage (thermal noise, flicker noise, distortion) are transferred to the output with unity transfer function. In Section 3.2 we analyzed the contribution of *kT/C* noise by the feedback branch. Such analysis did not include errors with source in the reference generator buffers, or errors resulting from different loading conditions of those buffers. We will now look into these issues.

Many applications utilizing delta-sigma modulation target an overall linearity and dynamic range of 14 bits to 16 bits. This requires from the D/A converter the same level, or better, of performance. It is very difficult, however, to realize multi-bit DACs with such a high linearity. Some work on delta-sigma structures employing multi-bit internal A/D and D/A conversion, and digital correction techniques to linearize the D/A, has been reported [46][47][48]. Although reasonable results were attained, the added circuit complexity is rather unappealing. Moreover, the techniques are likely to be impaired by parasitic elements when very high performance is approached. Recently, several authors have also employed noise shaping techniques to modulate the nonlinearity characteristic of the D/A converter, in a manner similar to the high-pass filtering of the quantization noise in delta-sigma modulation [49][50][51]. Indeed, the errors in the D/A converter are

modulated by a delta-sigma loop which provides a noise-shaping characteristic. First- and second-order noise shaping have been reported.

The most obvious advantages of using multi-bit conversion are lower quantization noise power, improved stability, and reduced in-band tone power. All of these can lead to a low-power design, since lower-order topologies can be used. It should be noted, however, that at very low power supply voltage (the assumption in this thesis), the performance is still limited by thermal noise, and hence all the considerations at which we arrived in this chapter regarding the performance of the first integrator still apply.

To better understand the requirements on the linearity of the D/A converter, let us briefly contemplate the following situation. Consider a 2nd-order delta-sigma modulator in which a 4-bit quantizer is utilized. Such structure requires a 4-bit DAC in the feedback path, from which a 16-bit linearity is required. Using a switched-capacitor DAC with 0.5% capacitor mismatch to implement the main DAC, and using an auxiliary capacitor array to fine tune the main array [48] to within half LSB at 16 bits, one obtains the (simulated) results shown in Figure 3.18. The potential improvement through calibration is dramatic, but it also shows how critical this block is. For this reason, 1-bit DACs are preferred, since they only have two levels, and hence are inherently linear (there is a straight line that can join two points).

There are, however, other nonideal mechanisms which can compromise the overall performance of the modulator. These are related to insufficient filtering of the reference generators and to nonlinear or signal dependent operation of the reference buffers.

Wideband noise superimposed on the reference (dc) signal can be significant. The sampling of the superimposed noise by the input stage results in aliasing into the baseband, which increases the noise floor, and hence reduces the resolution of the modulator. Moreover, since the reference signal is multiplied by the output signal of the

system, the quantization noise appearing at frequencies near half the sampling rate is also aliased back onto the baseband (through the convolution of both noise signals). The high-frequency quantization noise is not attenuated by the loop; indeed, it is amplified, which can amount to a significant degradation of the performance. For this reason, it is very important to filter adequately the reference generators.

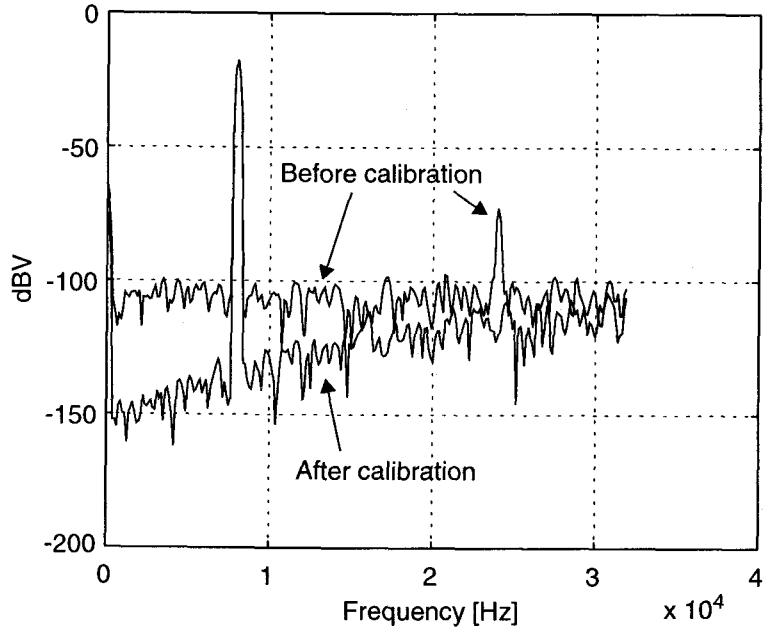

Figure 3.18: Simulated spectrum of the output of a 2nd-order delta-sigma modulator employing 4-bit quantization, with and without calibration of the D/A converter. The sampling frequency was 2.048 MHz, the capacitor mismatch in the uncalibrated DAC was 0.5%, and the number of samples 16,384. The uncalibrated DAC had a differential nonlinearity of 85 16-bit LSBs, and the calibrated DAC 0.52 16-bit LSBs.

As discussed in connection with Figure 3.6, repeated here for convenience as Figure 3.19 on the following page, an input SC branch samples the reference voltage provided by the reference buffers. Since this action results in a change of the load impedance seen by those buffers, a transient will occur. In Figure 3.19a, the reference

voltage is sampled onto capacitor C_{in} and the information transferred to the integrating capacitor, simultaneously. In the previous phase C_{in} was used to sample the input signal, and hence the charge delivered to it from the reference voltage buffer is a function of x. Moreover, since the sampling of the reference voltage and the charge transfer to the integration capacitor take place in the same clock phase, the process will be affected by the settling of both the reference buffer and of the amplifier. This may result in a signal dependent charge delivery, and consequently harmonic distortion. This problem is overcome by using either structure in Figure 3.19b or Figure 3.19c. Here, the sampling of the reference voltage and charge transfer occur in different clock phases, thus allowing for independent settling of the buffers and of the amplifier. Furthermore, different capacitors are used to sample the input and the reference, therefore eliminating signal dependent charge delivery.

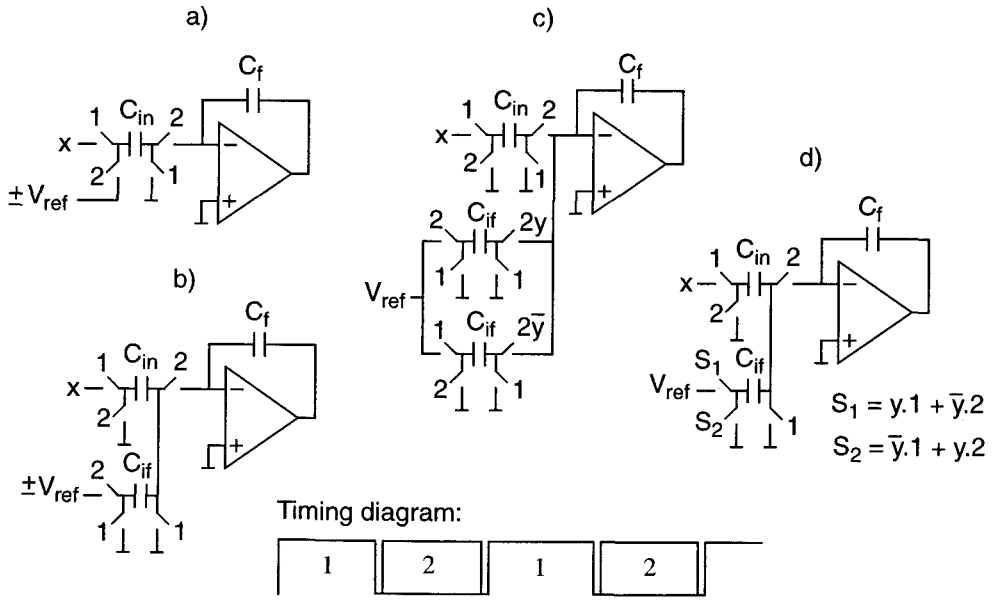

Figure 3.19: Switched-capacitor, single-ended implementation of the first integrator with a) double reference voltage -- single input branch, b) double reference voltage -- two input branches, c) single reference voltage -- three input branches, and d) single reference voltage -- two input branches.

Another potential problem associated with the structure in Figure 3.19a is related to the density of "ones" and "zeros" in the bitstream. Since "ones" and "zeros" result in different amounts of charge being drawn from the buffers, the average value of the reference voltage will be slightly different from the nominal, and a signal-dependent gain error is introduced. This problem is also eliminated through the use of the structure in Figure 3.19c, and also Figure 3.19b if it is differential. Note that in Figure 3.19c, the reference sees always the same capacitive load in every clock cycle, independent of the transition density. For this to happen in Figure 3.19b, a differential structure must be used, otherwise the positive and negative references will display different levels of activity.

Inherent to the double-reference voltage solutions is the mismatch between $+V_{REF}$ and $-V_{REF}$, which will always occur to some degree. In the presence of such mismatch, one of the signal excursions (positive or negative), if sufficiently high, will drive the modulator into early overloading, effectively reducing its usable dynamic range. This mechanism, however, does not introduce nonlinearity; only offset. However, the reduction in dynamic range may impact severely the performance, and some margin should be left when sizing the input capacitor. Naturally, this will result in a larger value of the power dissipation.

It is clear that the design of the feedback DAC can be very critical. The reference buffers should be designed to have sufficient speed and driving capability to settle fully. The reference should never be sampled when the comparator is still making a decision, as this would result in charge delivery dependent on the comparator's input signal (and hence distortion). Preferably, the settling of the reference buffers and of the amplifier should be decoupled. Moreover, low-noise DAC performance is imperative and, as mentioned earlier, the loading of V_{REF} must be signal independent.

3.6 SUMMARY

In this chapter we analyzed the performance requirements for each block in a SC 2nd-order delta-sigma modulator. The trade-offs were presented and a detailed analysis of the power dissipation of the amplifier was provided. The issues related to biasing the amplifiers were discussed as well. The first integrator is the block responsible for most of the power dissipation due to the stringent requirements on its performance. The second most important block is the feedback D/A converter. The remaining blocks possess relatively relaxed performance requirements as they benefit from noise shaping.

The condition to achieve low power dissipation when limited by thermal noise is the utilization of minimum-size capacitances. Hence, the signal swing should be maximized.

4. A 1.8 V 94 dB DYNAMIC RANGE ΔΣ MODULATOR FOR VOICE APPLICATIONS

This chapter describes the design and the implementation, based on the principles discussed earlier, of a single-bit second order switched-capacitor delta-sigma modulator intended for voice applications [31]. It should provide a dynamic range of 92 dB (15 bit) or more over the signal bandwidth 300 Hz - 3.5 kHz. The modulator is to operate from a 1.8 V power supply.

4.1 CIRCUIT DESIGN

A second-order delta-sigma modulator based on the architecture depicted in Figure 3.1 was designed for fabrication in a 0.6 μm 5 V CMOS process, with the goal of verifying experimentally the results derived in Chapter 3. The objective was to achieve 92 dB of dynamic range and a peak signal-to-noise ratio of 85 dB over the voice band. This performance was to be attained while operating from a 1.8 V power supply (the low-end voltage of two series connected batteries), and utilizing conventional SC techniques. Additionally, the sampling frequency was set to 2 MHz for system compatibility.

Figure 4.1a shows a fully-differential implementation of the modulator, consisting of two parasitic insensitive SC forward-Euler integrators, a latched comparator that serves as the 1-bit A/D converter, and a distributed 1-bit D/A converter. The utilization of a fully-differential configuration provides superior noise immunity and adds 3 dB to the dynamic range (cf. Section 3.2.1). The modulator operates on a four-phase, nonoverlapping clock (Figure 4.1b), to reduce signal dependent clock injection [52]. The upper and lower paths of the clock generator were designed to have equal delays. To obtain coincident clock rising edges, the delay of inverter INV1 was made equal to the delay of the cascade of NAND1 and BUFF1.

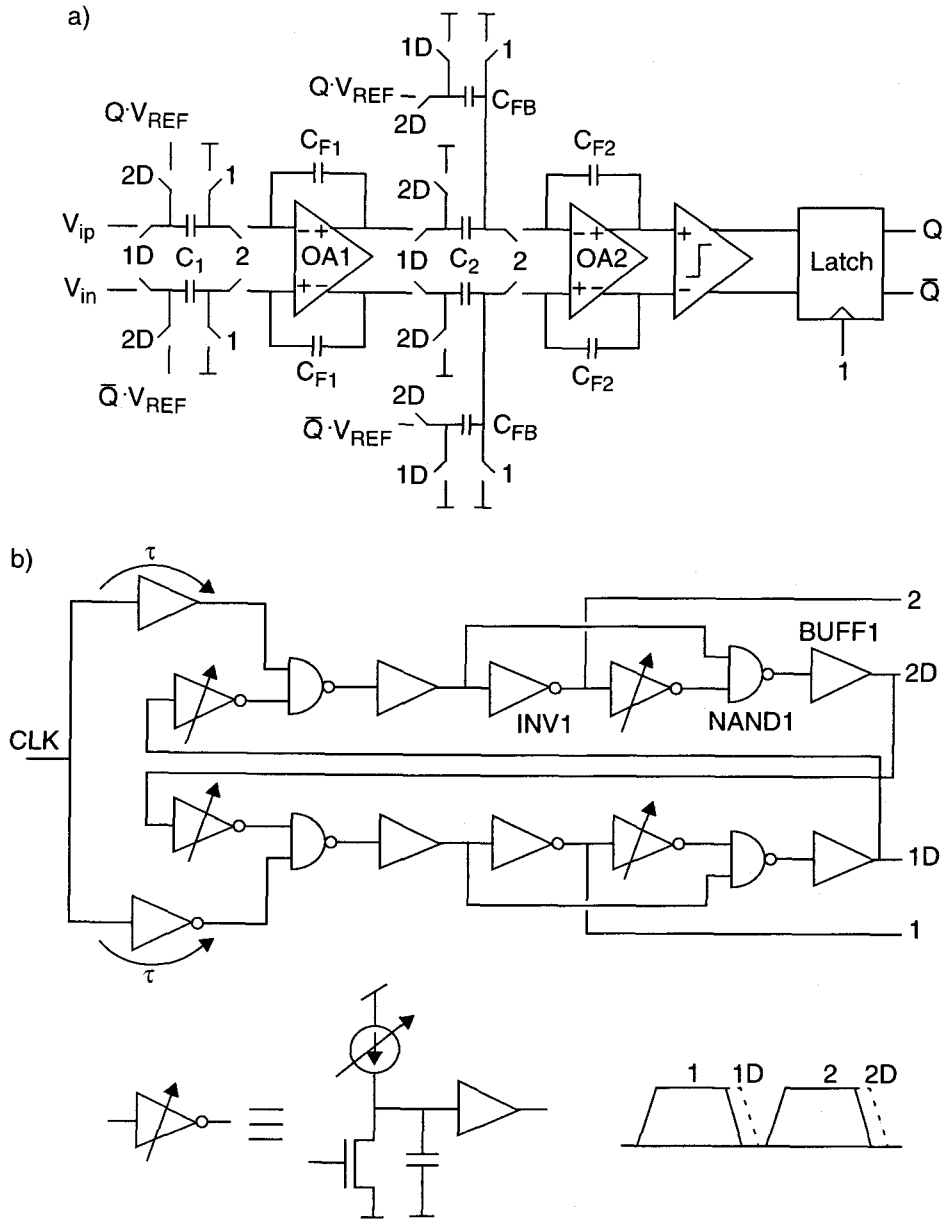

Figure 4.1: a) Fully differential switched-capacitor implementation of the 2nd-order delta-sigma modulator. b) Four-phase clock generator and timing diagram.

For test purposes, variable delay elements were included which permit the fine adjustment of the nonoverlapping and delay time frames. This feature permits the

observation of the effect of incomplete settling of the amplifiers on the signal-to-noise ratio. The performance of the comparator, described later in this section, is also dependent on the duration of the nonoverlapping time periods.

Given the signal bandwidth and the sampling frequency, the oversampling ratio is well defined, 286 in this case. For such a high value of the *OSR*, a second-order modulator possesses a quantization noise floor sufficiently low to provide a dynamic range and peak *SNR* better than 100 dB, and hence the performance will not be limited by this type of noise, but rather by thermal noise. To reduce the *kT/C* noise power, a single input switched-capacitor branch was used in the input stage, which is shared between the input and feedback paths (Figure 4.1a). This has several implications. The most important is that the *kT/C* noise power is reduced by a factor of two, therefore requiring capacitors with half the size to achieve the same performance. Another implication is that the input and feedback signals may not be scaled independently. This may or may not be an important limitation, depending on the system requirements. A third consequence is that we are forced to use a double reference voltage, as discussed in Section 3.2.1.

A potential limitation of this structure is that incomplete settling of the reference buffers results in a signal dependent component, hence harmonic distortion (cf. Section 3.3.3). For this reason we chose for the reference voltages a conservative value of $V_{DD}/2 \pm 0.6\,\mathrm{V}$ that is, 0.3 V and 1.5 V, a comfortable 300 mV from the power supply rails. This makes the on-chip reference voltage generation straightforward, as the output devices of the buffers can operate in the saturation (high gain) region. It also provides better power supply noise rejection and results in lower power dissipation. An alternative is to use the power supply rails as the references, which would amount to having a 0.9 V reference voltage. However, to reduce the risk of noise coupling into the circuit from the power supply lines, separate pads would be required. The feasibility of this solution in a large system is likely to be impaired by the unavailability of extra pins, hence it was not contemplated. The consequence is a reduction of the maximum input signal power of

about 3.5 dB, which will require capacitors with more than twice the size (and hence higher power dissipation).

The stage gain factors C_i/C_{Fi} were chosen so as to guarantee that the amplifier output signals do not assume values beyond the high-gain region. For the present design, the amplifier open-loop dc gain starts dropping for output signal levels exceeding 0.4 V. Since $V_{REF} = 0.6\,\text{V}$, according to (3.6) this requires $(C_1/C_{F1})_{max} = 0.247$. A more conservative solution was adopted by making $C_1/C_{F1} = 0.24$. The second-stage gain factor was chosen according to (3.47). The output swing of the second-stage amplifier is smaller than that of the first-stage amplifier, as it drives directly the input stage of the comparator, which cannot be biased at half of the power supply voltage (to be discussed later in this chapter). The output common-mode voltage is then set at a higher value, therefore reducing the signal swing. The dc gain of this amplifier starts dropping for signal levels exceeding 0.25 V. According to (3.47) this requires $(C_2/C_{F2})_{max} = 0.47$. A more conservative approach was taken and $C_2/C_{F2} = 0.42$ was chosen. The inner feedback loop gain factor C_{FB}/C_{F2} was set at 1.7 times the gain factor of the first stage, therefore assuring stability [53]. Note that the reference voltage is larger than the amplifier's region of high gain. As discussed in Chapter 3, this yields a slightly larger dynamic range which can be used to reduce the size of the input capacitor C_1. This was sized to reflect a compromise between noise performance, including kT/C noise as well as noise from the amplifier, and power dissipation resulting from proper compensation. Simple calculations suggested a value of 2 pF, which also provides headroom for process and temperature variations. Capacitors C_2 and C_{FB} had a value equal to 1.25 pF and 0.5 pF, respectively. Behavioral simulations, including finite dc op-amp gain, thermal and flicker noise, *kT/C* noise and clock injection (Appendix B), showed that with these scaling factors it is still possible to achieve a peak *SNR* of 94 dB and a *DR* of about 98 dB *i.e.*, a better than 15 bit performance. The simulated *SNR* as a function of the input signal power level is shown in Figure 4.2.

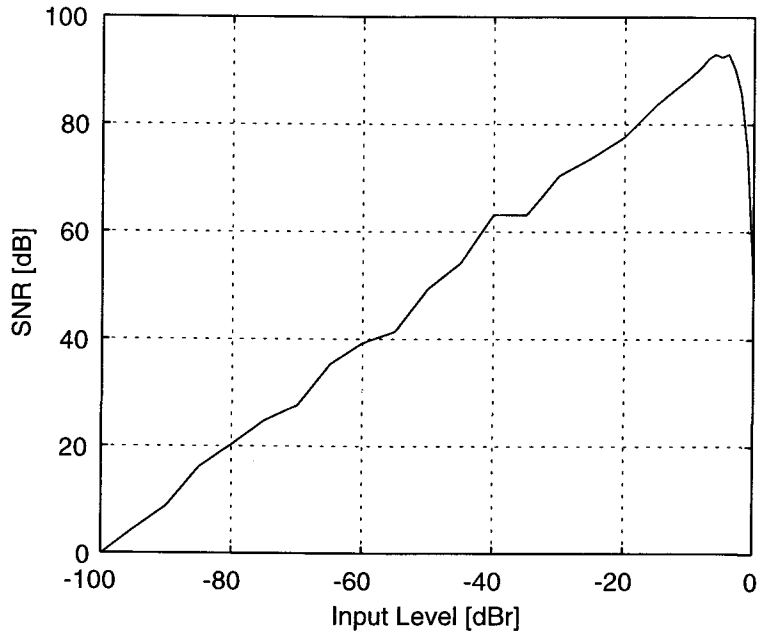

Figure 4.2: Simulated *SNR* as a function of the input signal level power, for a 1 kHz frequency input sinewave.

A critical aspect of low-voltage design with SC techniques is to insure that all switches can turn ON under all conditions (the time constant of the sampling network has to be much lower than that of the amplifier). A 1.8 V supply is insufficient for this, hence it was decided to use bootstrapping. Figure 4.3 shows the circuit used for that purpose [54]. The bootstrapping stage consists of two coupled, back-to-back voltage doublers. Since this configuration results in the gate voltage of devices M1 and M2 exceeding V_{DD}, the output voltage V_{OUT} can reach $2 \cdot V_{DD}$ rather than $2 \cdot V_{DD} - V_T$, where V_T is the threshold voltage of transistor M2. In practice, the efficiency of this circuit is reduced by the presence of the load capacitance C_p (which can include some parasitic capacitance, for instance due to routing) and of the parasitic capacitance C_{p1} according to (Appendix C)

$$V_{out} = \frac{2 \cdot C_{pump} + C_{p1}}{C_{pump} + C_p + C_{p1}} \cdot V_{DD} \tag{4.1}$$

V_{out} needs to be reset periodically, which is done by the inverter stage M3-M4.

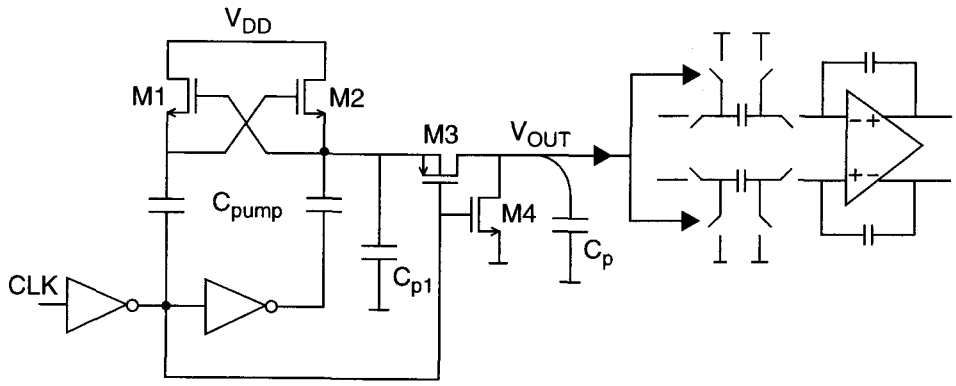

Figure 4.3: Clock bootstrapping stage.

It was decided to use local bootstrapping rather than global, to reduce the risk of cross-talk between sensitive nodes. Moreover, the design of a global clock charge pump is more difficult to optimize since it is hard to predict the total load capacitance. If the load capacitance is very large, that solution may also require an external capacitor, and hence two additional pins. Each bootstrapping stage was designed to drive two transistor gates simultaneously, symmetrically positioned (in both schematic and layout), to reduce the effect of unwanted common-mode mechanisms. The resulting clock output voltage went from 1.8 V to 3.4 V. This voltage assures a maximum channel on-resistance of approximately 1.4 kΩ, which exceeds the linear settling requirements for the present application. Linear settling to within half LSB of N bits of accuracy requires the value of the ON resistance of the switches R_{ON} to satisfy

$$e^{-\frac{T_S/2}{R_{ON} \cdot C}} < 2^{-(N+1)} \tag{4.2}$$

where C is capacitance in the RC sampling network (say, the input capacitor).

The most complex component in the modulator is the operational amplifier, as discussed in Chapter 3. The topology of this component and the general design criteria have to be judiciously defined.

Typically, for higher values of the power supply voltage, a common folded-cascode topology is preferred (Figure 3.10b), since it provides high gain and bandwidth. However, at 1.8 V power supply, the output swing is much reduced, resulting in deteriorating distortion and *SNR* performance. An alternative is to eliminate one of the cascode devices and follow this stage by a class-A stage with Miller frequency compensation (Figure 4.4a). The second stage provides the largest signal swing and compensates for the gain loss in the first stage, therefore reducing distortion. This topology was previously analyzed in the context of improved power supply rejection ratio (PSRR) [55], with cascode Miller compensation. The disadvantage of this structure is that the second pole is determined by the output stage, not by the cascode node of the first stage. This makes compensation somewhat more complicated. (The cascode device M3 has to be designed such that the frequency of the pole associated with its source is larger than the frequency of the pole associated with the output node; accordingly, the bulk of M3 can be connected to the power supply rather than to its source.) Nevertheless, this structure has better high-frequency properties than the typical differential pair with active load, since the Miller multiplication effect of the gate-to-drain capacitance of the input transistors is greatly reduced.

Another issue is the choice between a class-A and class-AB output stage. Normally, a class-AB stage would be used with a resistive load or where slewing could otherwise be a problem. The stage would then be biased at a relatively low quiescent

current (for class-A operation), and this current would be boosted during transitions (class-B operation). However, for the present design, meeting the targeted settling accuracy required a quiescent current exceeding that required for slewing, hence class-B operation was unnecessary (this was expected as discussed in Section 3.2.2.1). It is sometimes assumed that incomplete settling is equivalent only to a gain error, and therefore it is permissible to use a lower quiescent current; but usually the settling error will in fact be a function of the input signal, since the transition from class-B operation to class-A operation may be degraded by the reduction in the phase margin due to a lower quiescent current.

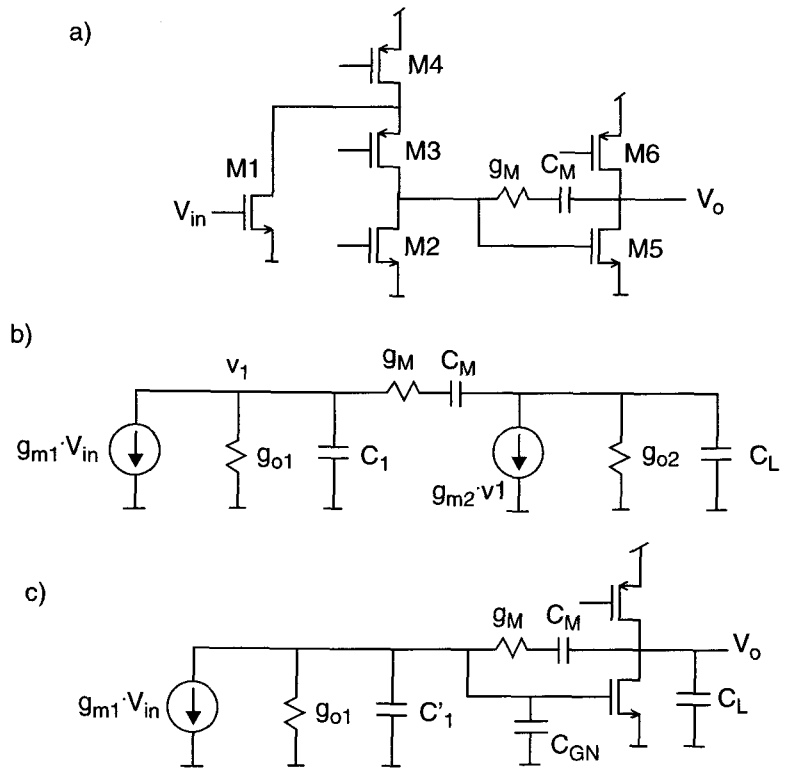

Figure 4.4: Two-stage amplifier with Miller frequency compensation. a) Simplified single-ended circuit. b) Simplified linear model. c) Detail of output stage.

For these reasons, it was decided to adopt the structure shown in Figure 4.4a for the first stage amplifier. Cascode Miller compensation was not used, because the ringing introduced by it slowed the settling of the amplifier. A possible solution would be to make the transconductance of the cascode devices large compared with those of the output devices, or increase the input capacitance of the output stage. The first option is hardly feasible since the output devices must have a very high transconductance (for adequate phase margin), and the second would further reduce the efficiency of the Miller feedback loop at higher frequencies, bringing the second pole closer to the unity gain bandwidth. For the second amplifier, the structure chosen is that of Figure 4.4a without the second stage. Although the gain is now relatively low, about 46 dB, behavioral simulations showed that the performance of the modulator is not affected. This is because it only increases the quantization noise leakage, a non-dominant contribution to the baseband noise power.

Figure 4.4b shows a simplified model of the amplifier in Figure 4.4a, and Figure 4.4c the model including the details of the output stage. The transfer function can be easily obtained:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} \cdot g_{m2}}{g_{o1} \cdot g_{o2}} \cdot \frac{1 - s/s_z}{1 + a_1 \cdot s + a_2 \cdot s^2 + a_3 \cdot s^3} \tag{4.3}$$

where

$$s_z = \frac{g_{m2} \cdot g_M}{(g_M - g_{m2}) \cdot C_M}$$

$$a_1 = \frac{[(g_{o1} + g_{o2} + g_{m2}) \cdot C_M + C_L \cdot g_{o1} + C_1 \cdot g_{o2}] \cdot g_M + g_{o1} \cdot g_{o2} \cdot C_M}{g_{o1} \cdot g_{o2} \cdot g_M}$$

$$a_2 = \frac{[(g_{o2} + g_M) \cdot C_M + C_L \cdot g_M] \cdot C_1 + (g_{o1} + g_M) \cdot C_L \cdot C_M}{g_{o1} \cdot g_{o2} \cdot g_M}$$

$$a_3 = \frac{C_1 \cdot C_M \cdot C_L}{g_{o1} \cdot g_{o2} \cdot g_M} \tag{4.4}$$

As in Chapter 3, the amplifier was modelled as consisting of a parallel combination of elementary stages, characterized by a set of elementary parameters. (An elementary device carries a current of 10 μA, and has the dimensions of $(9.6\mu m)/(2.4\mu m)$ for an n-channel transistor and $(23.1\mu m)/(2.4\mu m)$ for a p-channel transistor.) Equation (4.3) can now be used to obtain the unity-gain bandwidth f_u, and the phase margin ϕ_{PM}.

It is not possible to develop here a general analysis like the one presented for single-pole amplifiers, as there are more degrees of freedom in an amplifier with two or more poles. Nevertheless, the same principles leading to low power dissipation still apply: maximize signal swing, minimize capacitances and noise excess factor. These principles are independent of the amplifier topology. The remainder of this section concentrates on determining the point corresponding to minimum power dissipation, based on the trade-off between two important design variables: the stage multiplicity M and the gate overdrive voltage V_{GST}.

Figures 4.5a and 4.5b show f_u as a function of the multiplicity M and gate overdrive voltage V_{GST}, respectively. In Figure 4.5a, the parameter is V_{GST} and in Figure 4.5b the multiplicity. For a constant V_{GST} (Figure 4.5a), f_u is an increasing function of M, saturating at approximately 9.5 MHz. (The input transconductance and Miller capacitance were designed to provide a unity-gain bandwidth of about 10 MHz.) For values of M greater than 20, f_u flattens which means that the Miller loop has shifted the second pole to a frequency sufficiently high such that the amplifier behaves as a single-pole system. For low multiplicities, higher gate overdrive voltages yield higher unity-gain bandwidths. For very high values of the multiplicity, f_u starts dropping as the parasitics become dominant.

Similar plots can be obtained for the phase margin *PM*, which is approximately given by

$$\phi_{PM} = -\text{atan}\left(\frac{\zeta - 1}{\zeta} \cdot \frac{f_u \cdot C_M}{g_{m2}}\right) - \text{atan}\left(\frac{a_1 \cdot f_u - a_3 \cdot f_u^3}{1 - a_2 \cdot f_u^2}\right) \tag{4.5}$$

where $\zeta = g_M / g_{m2}$. The ϕ_{PM} plots are shown in Figure 4.6 for $\zeta = 0.875$, when the zero frequency is about seven times higher than the frequency of the non-dominant pole: $z \approx p_2 \cdot \zeta / (1 - \zeta) = 7$. Again, for values of M greater than 20, the phase margin is essentially constant and higher than 70°. For each 100 mV increase in V_{GST}, the phase margin increases approximately by 5°.

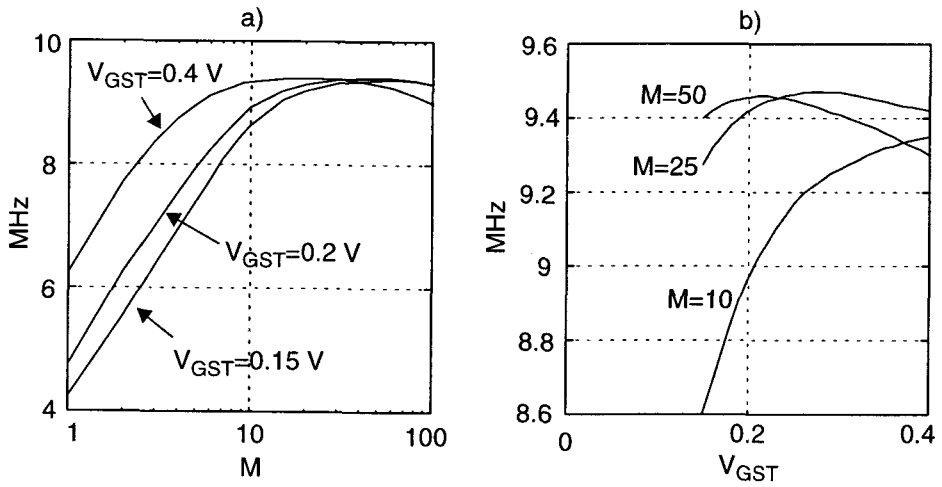

Figure 4.5: Unity-gain bandwidth as a function of a) multiplicity M, parameter is gate overdrive voltage, and b) gate overdrive voltage V_{GST}, parameter is multiplicity.

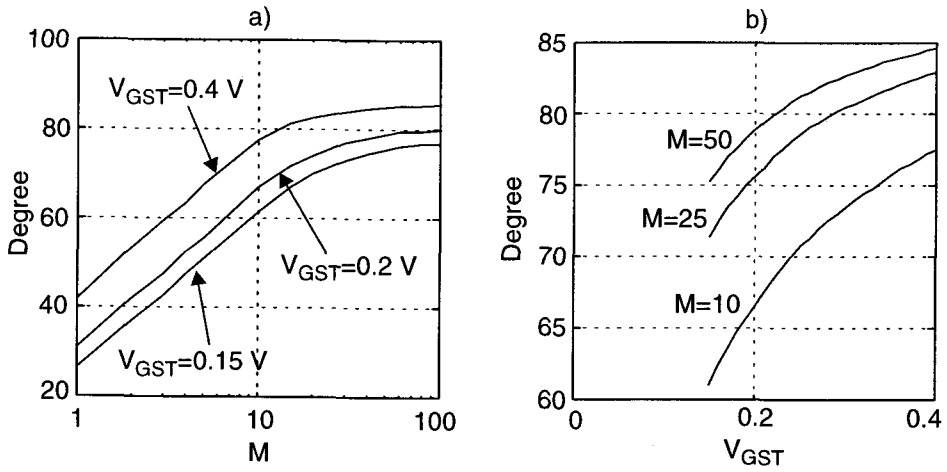

Figure 4.6: Phase margin as a function of a) multiplicity M, parameter is gate overdrive voltage, and b) gate overdrive voltage V_{GST}, parameter is multiplicity.

The dc gain of the amplifier was made high, approximately 90 dB, to reduce the effects of loop and amplifier nonlinearities.

The other parameter of interest is the power dissipation of the output stage (most of the power will be dissipated in the output stage to achieve proper frequency compensation. Figures 4.7a and 4.7b show the static power dissipation of the output stage, normalized to the values corresponding to this design, as a function of the phase margin for constant V_{GST} (Figure 4.7a), and as a function of the multiplicity for constant V_{GST} (Figure 4.7b). They show that the phase margin is more efficiently improved by increasing the current density (V_{GST}), rather than the aspect ratio of the devices (M). However, larger current densities imply loss in output swing, and a value sufficiently low for high swing, but not too low to avoid the gray area of moderate inversion, was chosen: V_{GST} = 200 mV. With V_{GST} fixed, the only degree of freedom left is that of varying the multiplicity. The action of increasing M yields good results only up to a certain value, at which point the parasitic capacitances of the output stage become relevant. Further

increase in the transconductance of the output device (from increasing M), results in an even larger increase in the output equivalent capacitive load (the feedback coefficient of the Miller loop decreases), and the second pole starts approaching the unity-gain frequency with loss of phase margin. In this design a value $M = 25$ (*i.e.*, $I_D = 250$ μA) was used. The point corresponding to the design described here is also shown in these Figures, indicating that it is nearly optimum since an incremental improvement in performance would require excessive power dissipation.

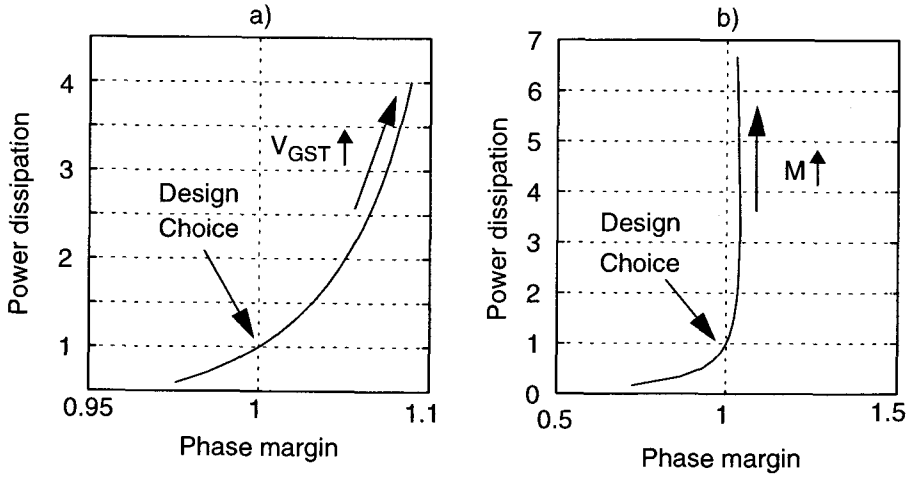

Figure 4.7: Normalized power dissipation ($V_{DD} = 1.8$ V) as a function of the normalized phase margin: a) for $V_{GST} = 0.15 \ldots 0.4$ V. b) for $M = 1$ to 200.

Figure 4.8a shows the complete circuit schematic of the amplifier and its bias circuit, and Table 4.1 the aspect ratios used in this design. To reduce the channel modulation effect, non-minimum length devices were used throughout the design (except for the switches). The differential pair tail current is 40 μA. For better dynamic response, the cascode transistor Mb3 in the biasing circuit was biased with a gate voltage which closely follows the input common-mode voltage of the main amplifier. This way, V_{b1} adjusts itself more rapidly to changes in the input common mode voltage of the amplifier.

The input common-mode voltage was set at 1.2 V, and the output common-mode voltage at 0.9 V ($V_{DD}/2$).

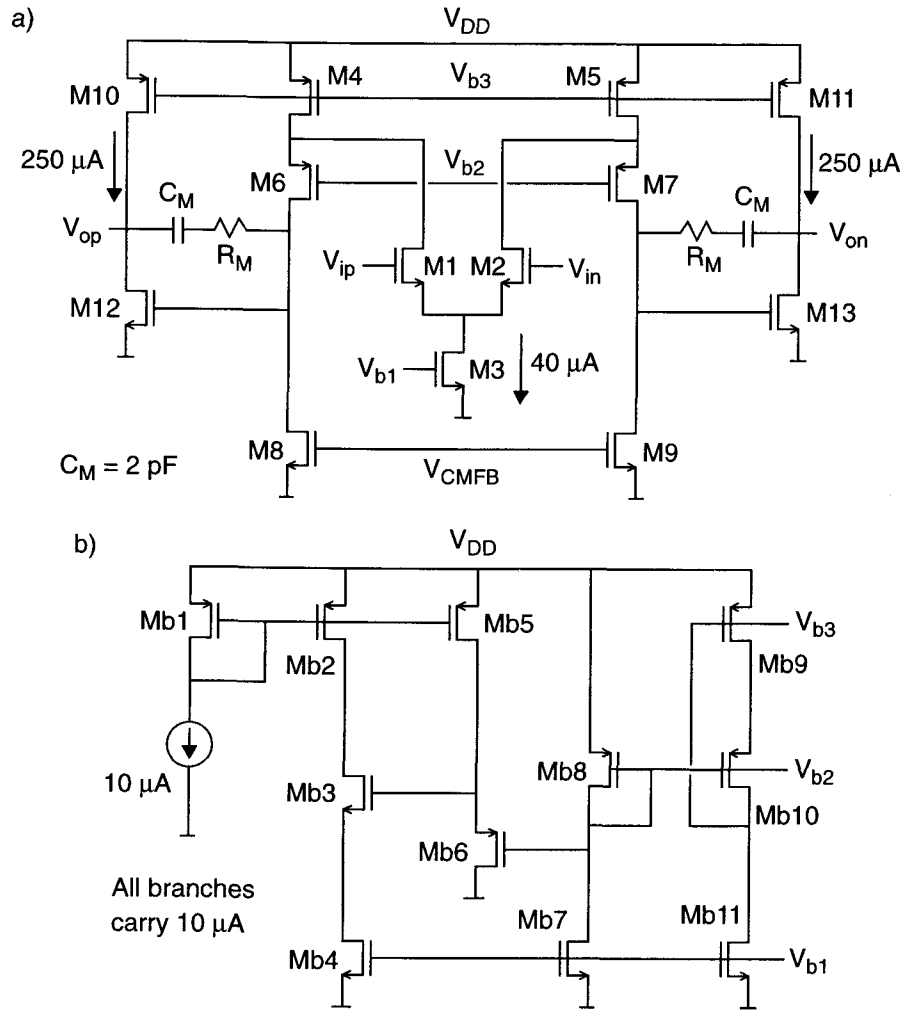

Figure 4.8: a) Complete circuit diagram of the first stage amplifier. b) Bias circuit.

The common-mode feedback (CMFB) circuit for the first op-amp (OA1, Figure 4.1a) is shown in Figure 4.9. It uses a switched-capacitor sensing circuit, with an inverting amplifier stage to provide negative feedback. Note that the input (M2) of the amplifier is

connected to the input common-mode voltage (analog ground) rather than the desired output common-mode voltage. This is required to bias properly the differential pair which, otherwise, would not turn ON. To accomplish this, the switched capacitors in Figure 4.9 implement a level translator which raises the average gate voltage of M1 from the output common-mode voltage to the input common-mode voltage.

The common-mode circuit for OA2 does not have the amplifier since OA2 lacks a second stage, so no phase inversion is needed in the CMFB stage.

Devices	W/L	Multiplicity
M1, M2	9.6/2.4	2
M3	9.6/2.4	4
M4, M5	23.1/2.4	4
M6, M7	15/1.5	2
M8, M9	9.6/2.4	2
M10, M11	23.1/2.4	25
M12, M13	9.6/2.4	25
Mb1, Mb2, Mb5	15/1.5	1
Mb3, Mb4	6/1.5	1
Mb6	15/1.5	1
Mb7, Mb11	6/1.5	1
Mb8	16/6.9	1
Mb9, Mb10	15/1.5	1

Table 4.1: First stage amplifier and bias circuit device aspect ratios.

The critical issues in the design of the CMFB circuit of OA1 are its bandwidth (which will affect the transient response of the overall amplifier) and its noise. The latter significantly affects the former, since the common-mode circuit drives the gates of two devices (M8 and M9) which have noise gains as high as the input transistors (the amplifier noise excess factor is $\gamma = 6$). Hence, for low noise, the areas of both the input differential pair devices and current sources M4, M5, M8 and M9 (Figure 4.8a) must be made large. The increased area contributes additional capacitive load, and hence care should be exercised to make the 3 dB bandwidth of the common-mode circuit larger than the unity-gain frequency of the amplifier. As a rule of thumb, the bandwidth of the common-mode circuit should be at least twice as large as the unity-gain bandwidth of the main amplifier.

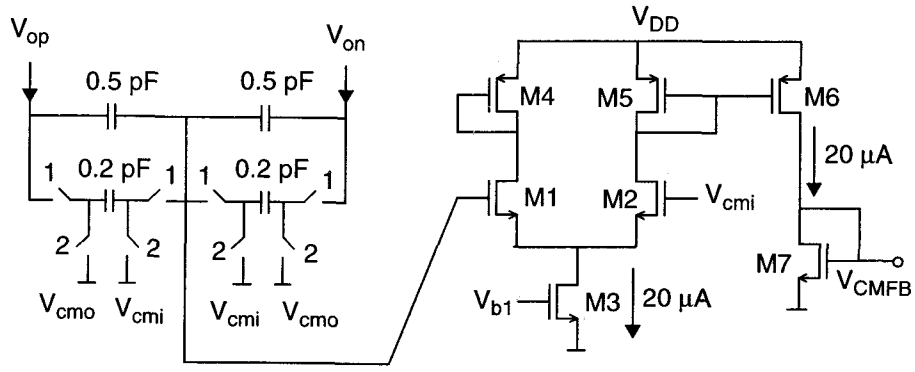

Figure 4.9: Common-mode circuit.

Figure 4.10 shows the comparator used in this design [56]. It is clocked by two nonoverlapping, complementary clock phases, CLK1 and CLK2. During clock phase CLK1 (reset phase), the comparator senses the input signal across the ON resistance of switch S1 and pre-charges the nodes of the second latch to V_{DD} by closing switches S4 and S5 (this destroys system memory, which would otherwise result in hysteresis). Switches S2 and S3 are open, isolating the input and output stages. In clock phase CLK2 (compare phase), switches S2 and S3 close and switches S1, S4 and S5 open, allowing the

amplification of the voltage difference developed across S1. Note that since S1 is controlled by CLK1 rather than CLK2, it actually opens before S2 and S3 close or S4 and S5 open. This is very important since allows for signal amplification by the input stage during the nonoverlap period. Appropriate nonoverlapping periods have to be provided to allow sufficient amplification in order to overcome the offset of the second stage, which can be large (in the order of 50 mV to 100 mV). To achieve this, the clock generator was designed with variable delay elements, as described earlier.

For fast operation, switches S2 and S3 were also driven by clock bootstrapping circuits.

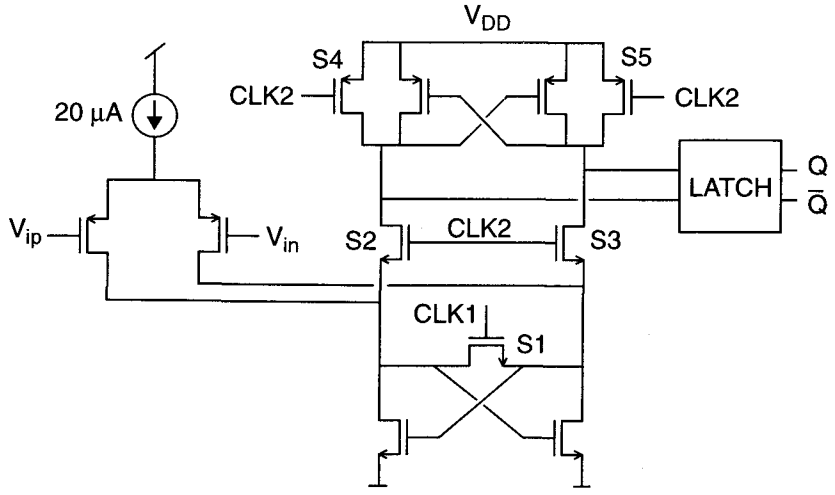

Figure 4.10: Comparator circuit.

4.2 LAYOUT CONSIDERATIONS

Figure 4.11 shows a microphotograph of the chip. Each amplifier was laid out using a stacked, inter-digitated layout technique to improve matching. This technique can be regarded as a one-dimensional common-centroid layout. To reduce cross-talk, each amplifier uses a separate bias circuit. A MOS capacitor was connected to each bias line to reduce noise levels. The input and integrating capacitors were placed between the core of the respective amplifier and the switches of that stage, hence providing better isolation. The clock bootstrapping circuits were placed next to the respective switches, to improve efficiency, as given by (4.1). Notice that despite the large number of clock bootstrapping circuits, a total of 24, the area penalty is negligible. This is due to the close proximity between these circuits and the switches which they drive (thus requiring small "pump" capacitances), and to the use of MOS capacitors operating in the accumulation region to implement the charge pump capacitors (Figure 4.3). (MOS capacitors have a larger per unit area capacitance.) The nonlinearity of these capacitors is irrelevant as a constant voltage (V_{DD}) is always applied. More importantly, they are not in the signal path.

The clock generator was placed about 100 μm away from the modulator core to reduce coupling. This circuit also possesses it own bias circuit, used to generate the bias voltages for the variable delay elements.

The area of the smallest rectangle which embraces all the blocks shown in Figure 4.11 is 0.44 mm^2, and hence the area actually occupied by the circuit is substantially smaller.

The circuit was fabricated in the facilities of Rockwell Semiconductor Systems, in Newport Beach, California.

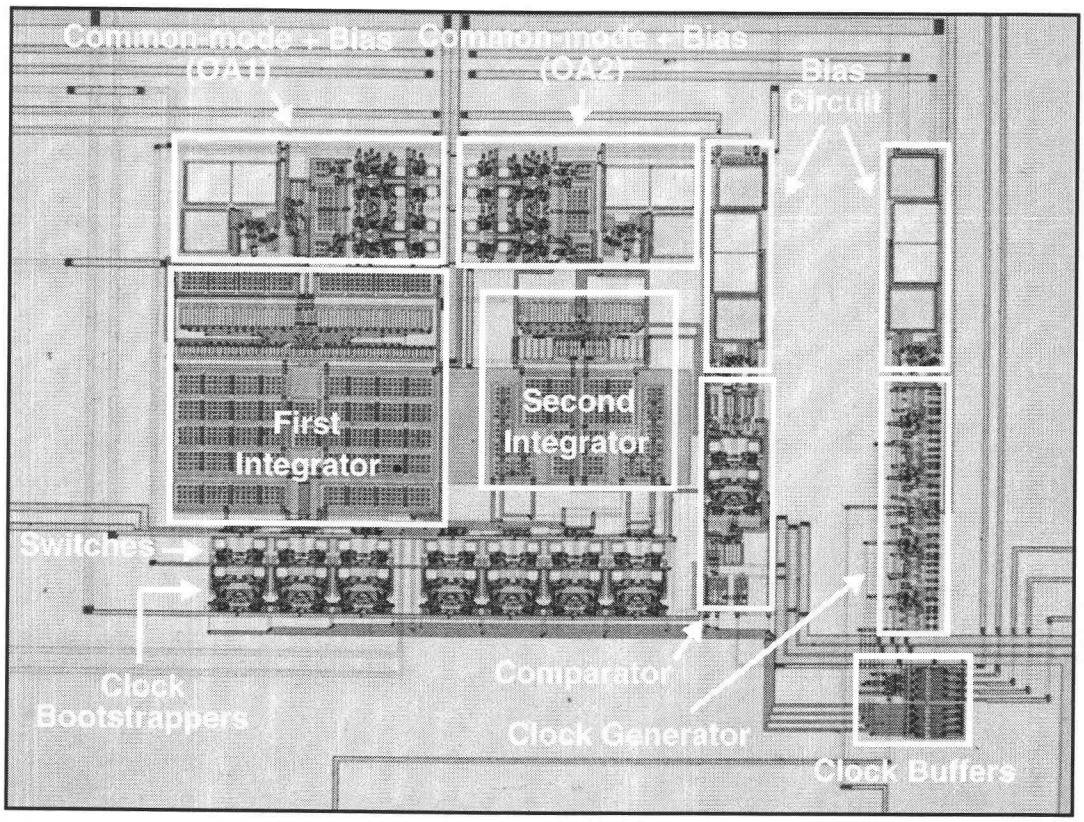

Figure 4.11: Chip microphotograph.

4.3 EXPERIMENTAL RESULTS

A test board was designed and linked to an acquisition board which captured the output bit stream. To evaluate the performance of the modulator, the captured bit stream was multiplied by a Dolph-Chebyshev window [57][58] with a side-lobe attenuation of 140 dB, and passed through a 262,144-point FFT with four cycles of averaging. Figure 4.12 shows the measured signal-to-noise and signal-to-noise-plus-distortion ratios, as functions of the relative input signal level. (Since V_{REF} = 0.6 V, 0 dB corresponds to a peak-to-peak value of 1.2 V.) The input signal was a 1 kHz sinewave, the clock frequency was 2 MHz, and the power supply was 1.8 V. The modulator achieves a peak $S/(N+THD)$ of 80 dB, a peak SNR of 90 dB, and an instantaneous dynamic range of 94

dB. The curve exhibits a nearly constant unit-value slope of 1 dB/dB, indicating that the total noise floor was independent of the signal value. This is somewhat unusual in a 2nd-order modulator, plagued with spurious tones in the signal band. This absence of tones is attributed to the dithering effect of thermal noise at the input [59][60]. The thermal noise inflicts some random behavior on the input signal, therefore destroying the tendency for a fixed pattern.

Figure 4.13 show the measured output spectrum for a relative level of -12.6 dB (−20 dBV), corresponding to the onset of overloading in Figure 4.12.

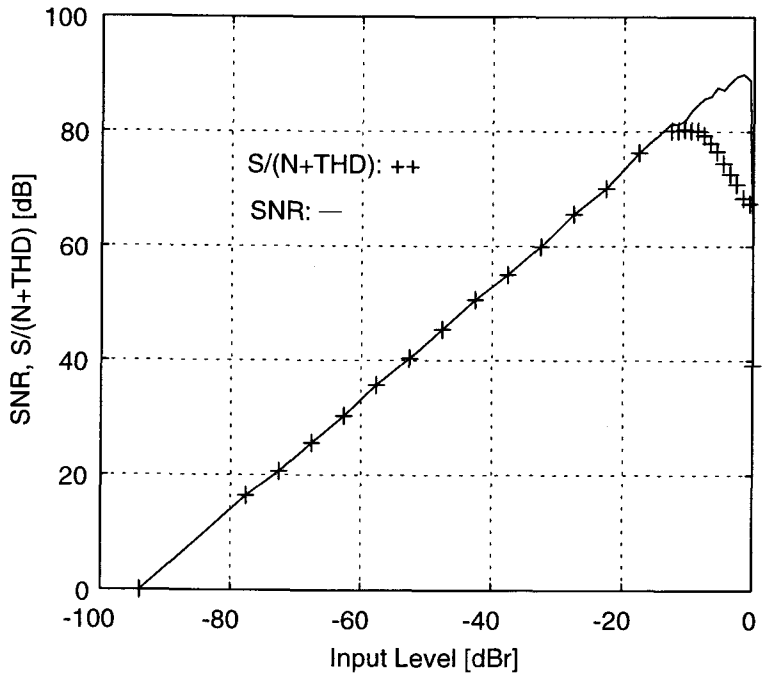

Figure 4.12: Measured SNR and $S/(N+THD)$ as functions of the input signal level.

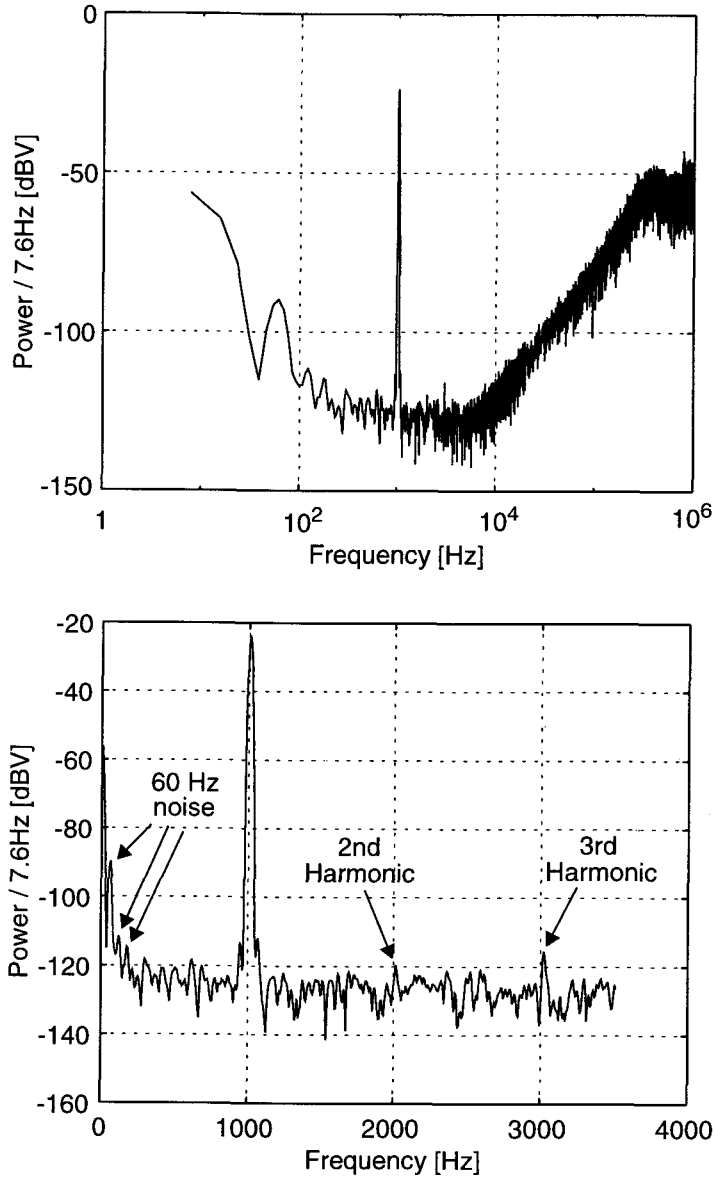

Figure 4.13: Measured output spectrum for a -12.6 dBr, 1 kHz sinewave input. Noise power = -99.21 dBV, Signal power = -20 dBV.

As can be seen from Figure 4.13, the resolution of the modulator is limited by thermal noise (flat spectrum) and by flicker noise. No attempt was made to minimize the latter (by using larger devices or CDS techniques), and some improvement might be

attainable. Some 60 Hz noise was also present, despite the effort put into the development of the test environment, which included a 6-layer board with several ground planes. As Figure 4.12 shows, the $S/(N+THD)$ starts degrading when the relative input level exceeds -12.6 dB, decreasing rapidly beyond -7 dB. This is due to the input of the common-mode circuit having been connected to the output common-mode voltage, rather than the input common-mode voltage. This reduced significantly the available swing of the amplifier, resulting in early overloading of the modulator.

There was a loss of about 4 dB relative to the theoretical *SNR* curve in Figure 4.2. This was found to be due mostly to insufficient filtering of the (external) reference voltage generators and to flicker noise.

Several tests were performed to investigate the effects of variable delay and non-overlapping time frames. Within reasonable time frame variations (up to 5%), no measurable difference in performance was detected, which was expected since the quantization noise floor was designed to be non-dominant. Further increase resulted in a gradual collapsing of the performance of the modulator, as the amplifiers do not settle properly.

The total power dissipation was 2 mW, which reflects a somewhat conservative design. This figure can be reduced to about 1.5 mW, by a better design of the amplifier in the first stage (lower noise excess coefficient), better scaling of the second stage, and elimination of the bias circuit and current sources in the clock generator (included only for test).

Table 4.2 summarizes the measured characteristics of the modulator, and Table 4.3 the structure of the current consumption in the modulator.

Power supply	0 - 1.8 V
Power dissipation	2.0 mW
Sampling rate	2 MHz
Signal band	0.3 - 3.5 kHz
Dynamic range	94 dB
Peak S/(N+THD)	80 dB
Peak SNR	90 dB
Active area	0.44 mm^2
Technology	0.6 µm CMOS N-well

Table 4.2: Measured performance characteristics of the modulator.

First stage:	670 µA
Amplifier	580 µA
Bias circuit	50 µA
Common-mode circuit	40 µA
Second stage:	250 µA
Amplifier	200 µA
Bias circuit	50 µA
Comparator:	70 µA
Clock generator:	130 µA

Table 4.3: Structure of the current consumption in the modulator.

4.4 SUMMARY

This Chapter described the design and implementation of a second-order SC delta-sigma modulator operating from a 1.8 V power supply. The modulator was fabricated in a 5 V, 0.6 μm N-well double-metal single-poly CMOS process. It achieved a 94 dB instantaneous dynamic range, a peak *SNR* of 90 dB and a peak $S/(N+THD)$ of 80 dB over the band.

Potential areas of improvement include reduction of low-frequency noise, and power dissipation. Chapter 5 attempts to cope with these two problems by employing predictive correlated double sampling techniques. Such techniques compensate for the nonlinear characteristic of the amplifier dc gain, which potentially permits the utilization of single-stage topologies (compensated by their load), with low distortion and low-to-moderate power dissipation.

5. IMPROVED DESIGN TECHNIQUES FOR RELAXED COMPONENT REQUIREMENTS

Chapter 3 focused on analyzing the performance of the first integrator in a $\Delta\Sigma$ modulator and how it affected the power dissipation. The fundamental requirements for a high-performance low-power design are large signal swing, small capacitances, and simple amplifier topologies with high gain for low distortion. The most competitive topology for high signal swing is the two-stage Miller amplifier which, in addition, provides high dc gain. The disadvantage of such structure, however, is that compensation is achieved through the utilization of an additional capacitor -- the Miller capacitor (and possibly a resistor). For this compensation to be efficient, the current level at the output stage has to be increased to obtain good phase margin, in an attempt to replicate the behavior of a single-pole amplifier. Therefore, the overall power dissipation increases, but the energy efficiency is lower, as the extra capacitor is irrelevant to the processing of the signal; it's there merely for stability of the amplifier.

Hence, it is desirable to utilize single-stage amplifiers, as they are compensated by their load (also present in a two-stage amplifier). However, single-stage amplifiers suffer from a much reduced signal swing, and a folded-cascode structure, for instance, cannot be utilized in a very low-voltage environment. To increase the signal swing, one must abandon structures employing stacked devices, and the penalty is a reduced dc gain. The low dc gain impacts performance in two ways: one is the impossibility to realize transfer functions close to the ideal ones which, as discussed earlier, increases the quantization noise floor in the signal band. The other is distortion caused by a much larger relative gain variation with the signal level.

This chapter analyzes a technique which tries to cope with both limitations: it uses single-stage, relatively low-swing low-gain amplifiers, without sacrificing performance, in the context of delta-sigma modulation. The technique utilized is an extension of the basic correlated double sampling technique, and is called predictive correlated double sampling.

Another benefit of this technique is the reduction of low-frequency noise, namely flicker noise and dc offset. This is important as these sources of noise reduce the dynamic range of the system.

An example of an amplifier which would be a good candidate for this type of application is the one used in the second stage of the design presented in Chapter 4, or the first stage of the Miller amplifier utilized in the first integrator. The structure is identical to a folded-cascode amplifier, but without one of the cascode devices. This results in lower gain and larger swing, as discussed previously. It also allows independent control of the input and output common-mode voltages, and hence the output swing can be as large as $V_{DD}/2 - (3/2) \cdot \Delta V$ (cf. Section 3.2.2.2).

5.1 THE CORRELATED DOUBLE SAMPLING TECHNIQUE

As in delta-sigma modulation, the correlated double sampling (CDS) technique exploits the correlation between successive samples of a signal to suppress its dc component. This can be attained by taking the difference between those samples, as explained in Section 2.4. To be efficient, this technique requires the signal to have low-frequency content, or to be highly oversampled. The latter is intuitive since successive samples of an oversampled signal do not differ much. Indeed, the correlation between successive samples increases with the square of the sampling frequency (or the oversampling ratio).

The principle of CDS can be illustrated in a simple manner with the switched-capacitor voltage comparator shown in Figure 5.1. In phase #1, the amplifier is connected in a unity-gain feedback configuration. Assuming, for now, that the dc gain of the amplifier is infinite, the voltage at its inverting input equals the offset voltage V_{os}. Therefore, V_{os} is also sampled and stored onto capacitor C. In phase #2, when the left plate of this capacitor is connected to the input signal, the voltage at the inverting input of the

amplifier becomes $V_{in} + V_{os}$. At this point, the comparator makes a decision based upon the difference between the voltages at its non-inverting and inverting inputs, which is $V_{os} - (V_{in} + V_{os}) = -V_{in}$. The term in the offset voltage is, therefore, absent, and the comparator makes a correct decision based on the sign of the input signal. If the offset voltage is instead a noise signal, say, v_n, the operation above corresponds to taking the difference between two successive samples of that noise signal:

$$V_o(n) = sign\{-V_{in}(n) + [v_n(n) - v_n(n-1)]\} \tag{5.1}$$

This expression resembles, aside the sign operation, that for the output of a first-order delta-sigma modulator, with v_n playing the role of the quantization noise. The result is therefore, noise-shaping of the input-referred noise of the amplifier, which is normally composed of a dc offset voltage, flicker and thermal noise. Clearly, CDS is a powerful technique to remove or reduce low-frequency (in-band) unwanted components, and can be extended to amplifiers and integrators as well [61]. (As might be expected, the efficiency of the technique is largely dependent upon the dc gain of the amplifier; more on this later.)

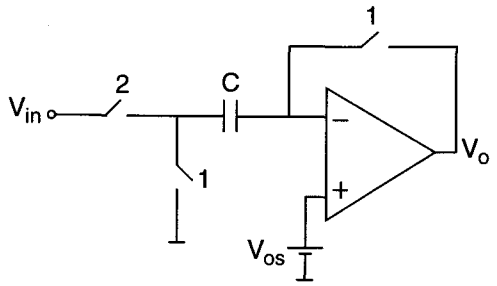

Figure 5.1: SC voltage comparator employing correlated double sampling for offset compensation.

As mentioned above, v_n is representative of the total input referred noise of the amplifier, thermal noise included. Since the latter is a broadband type of signal, the correlation between two successive samples decreases very rapidly with their separation in time. In analogy with the quantization noise, the high-frequency components are then amplified due to the high-pass filtering action of the subtraction operation. (It is from this sampling of two consecutive correlated samples that CDS receives its designation.) Moreover, since the system is a sampled-data one, the noise signal is undersampled, and hence aliasing occurs with a corresponding increase in the power spectral density.

There has been a considerable amount of work reported on structures employing CDS techniques (a good survey is presented in [61], along with numerous references), including some successful implementations of delta-sigma converters using offset- and gain-compensated analog front ends [46][62][63]. None of these designs was, however, intended for low-voltage operation. Although the objective was also to improve performance (dynamic range) using analog blocks with relaxed performance requirements, the design constraints were not as demanding. Moreover, all the reported work failed to include an analysis of the *kT/C* noise in such structures, with exception of Huang [64], who extended these techniques to track-and-hold circuits. (A noise analysis for SC integrators will be given later in this chapter.)

Another potential benefit of CDS is that of reducing the effect of the finite dc gain of the amplifier. As explained in Section 3.1, a finite dc gain translates into gain and pole errors, which degrade the performance of the modulator. The following section reviews a benchmark representation introduced by Ki [65], which will be used to compare the gain and pole errors in three SC integrator structures: a regular (uncompensated) forward-Euler integrator, a Nagaraj integrator [66], and a third structure which will henceforth be designated of predictive Nagaraj integrator [67].

5.2 ANALYSIS OF GAIN AND POLE ERRORS IN SC INTEGRATORS

The output signal of a discrete-time integrator can be generically described by

$$V_o(n) = \pm\alpha \cdot k \cdot V_{in}(n) + \beta \cdot V_o(n-1) + \gamma \cdot V_{os} \tag{5.2}$$

where α, β, and γ are coefficients which indicate how the actual transfer function deviates from the ideal one, k is the integrator gain, and V_{os} the offset voltage [65]. (Note that α and β differ in definition from those introduced in Section 3.1.) Ideally, α and β equal one and γ equals zero, and the set of these three parameters is known as the $\alpha\beta\gamma$ representation [65]. Due to the finite dc gain of the amplifier, these coefficients assume the more general form

$$\begin{aligned} &\alpha = 1 + \Delta\alpha, \quad \Delta\alpha \ll 1 \\ &\beta = 1 + \Delta\beta, \quad \Delta\beta \ll 1 \\ &\gamma \ll 1 \end{aligned} \tag{5.3}$$

where $\Delta\alpha$ and $\Delta\beta$ will be called the gain and pole errors, respectively, and γ is the offset voltage suppression factor.

Consider the three non-inverting SC integrators shown in Figure 5.2, where the amplifiers have the same finite dc gain A. The integrator in Figure 5.2a is a classic forward-Euler integrator, and has been the subject of extensive analysis in this work. The remaining integrators were proposed by Nagaraj [66][67] as offset- and gain-compensated structures, hence with reduced sensitivity to the dc gain of the amplifier. Although numerous structures have been proposed, we will focus on these two for their popularity.

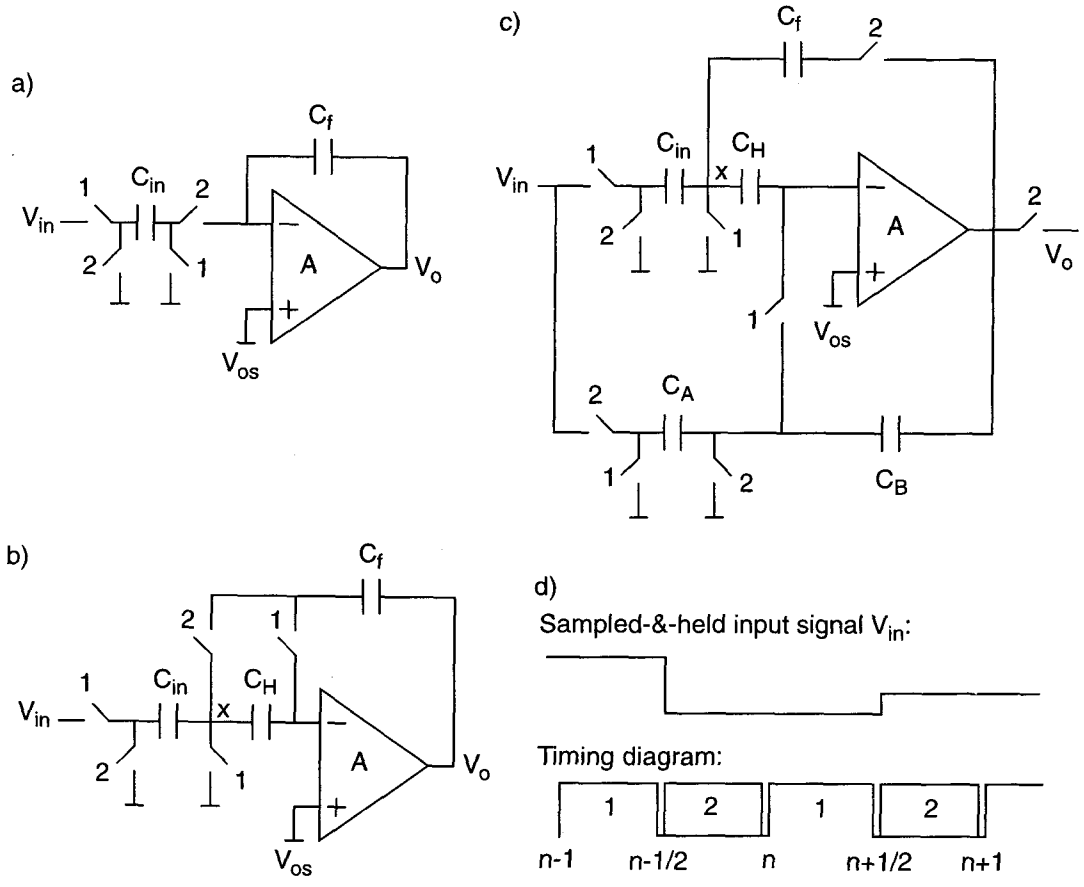

Figure 5.2: Three SC integrator topologies: a) Regular forward-Euler integrator. b) Offset- and gain-compensated Nagaraj integrator. c) Predictive Nagaraj integrator. d) Timing diagram and sampled-and-held input signal of the predictive Nagaraj integrator.

Before we analyze these structures for gain and pole errors using the $\alpha\beta\gamma$ representation, it is useful to go briefly through their principle of operation. The Nagaraj integrator in Figure 5.2b (hereon referred to as the Nagaraj integrator) samples the input signal V_{in} during phase #1 onto capacitor C_{in}. During that time frame, the holding capacitor C_H samples the offset voltage V_{os} and the input-referred output voltage $-V_o/A$ (which would be zero if A were infinite). In phase #2, the holding capacitor C_H is placed in series with the inverting input of the amplifier, and hence node x becomes the new virtual

ground, with the offset voltage ideally cancelled. Notice that in the structure in Figure 5.2a, the virtual ground voltage equals the offset voltage plus the input-referred output voltage term, and hence the error introduced during integration is significantly larger. Analysis shows that the output signal of the Nagaraj integrator in phase #2 is described by (Appendix D)

$$[1+\mu\cdot(1+k)]\cdot V_o(n) = k\cdot V_{in}\left(n-\frac{1}{2}\right) + [1+\mu\cdot(2+k)]\cdot V_o\left(n-\frac{1}{2}\right) - V_{os} \tag{5.4}$$

and in phase #1 by

$$[1+\mu\cdot(1+k')]\cdot V_o\left(n+\frac{1}{2}\right) = (1+\mu)\cdot V_o(n-1) - (1-k')\cdot\mu\cdot V_o\left(n-\frac{1}{2}\right) + V_{os} \tag{5.5}$$

where $k' = C_H/C_f$ and $\mu = 1/A$. Substituting (5.4) in (5.5) one arrives at

$$V_o\left(n+\frac{1}{2}\right) \cong k\cdot[1-\mu\cdot(1+k+k')]\cdot V_{in}\left(n-\frac{1}{2}\right) + \left(1-\mu^2\cdot k\right)\cdot V_o\left(n-\frac{1}{2}\right) + \mu\cdot k\cdot V_{os} \tag{5.6}$$

In the original publication [66], the output of the integrator was sampled in phase #2 which, as Ki indicated in [65], required $k' = 1$ for low phase error. When the output is sampled in #1, as in (5.6), this coefficient can assume any desired value, although it should be kept small for low-gain error (we will evaluate these errors shortly).

The operation of the predictive Nagaraj integrator is somewhat similar to that of the Nagaraj integrator. The difference resides in the utilization of an additional path,

composed of the switched-capacitor C_A and integration capacitor C_B, which is used to predict the output voltage prior to the integration phase (and hence will be called prediction path). It is assumed that the input voltage changes in the beginning of phase #2, and remains constant until the end of phase #1 (Figure 5.2d). In phase #2, C_A samples the new value of the input signal, and C_B the output, while the integration path (switched-capacitor C_{in} and capacitor C_f) generates a valid output corresponding to the previous value of V_{in}. In phase #1, the integration capacitor C_f is disconnected from the amplifier, therefore entering a hold mode, while the switched-capacitor C_{in} samples the new value of the input signal (equal to that stored in C_A in the previous clock phase). At this time, the prediction path and the op-amp are configured as in a forward-Euler integrator, and an output voltage is produced. This voltage is close to the value which will be obtained in the following phase #2 (therefore the name "predictive"). Also during phase #1, the holding capacitor samples the offset voltage and the predicted input-referred output voltage of the amplifier. Analysis of this structure yields the following expression for the output voltage in phase #2 (Appendix D):

$$[1+\mu\cdot(1+k_1)]\cdot V_o(n) = k_1\cdot V_{in}\left(n-\frac{1}{2}\right)+(1+\mu)\cdot V_o(n-1) + \mu\cdot(1+k_1)\cdot V_o\left(n-\frac{1}{2}\right)-\mu\cdot V_o\left(n-\frac{3}{2}\right) \quad (5.7)$$

In phase #1 the output voltage is described by

$$[1+\mu\cdot(1+k_2+k')]\cdot V_o\left(n-\frac{1}{2}\right) = k_2\cdot V_{in}(n-1)+V_o(n-1) + \mu\cdot k'\cdot V_o\left(n-\frac{3}{2}\right)+(1+k_2)\cdot V_{os} \quad (5.8)$$

where $k_1 = C_{in}/C_f$, $k_2 = C_A/C_B$ and $k' = C_H/C_B$. For proper operation the relation $k_1 = k_2 = k$ should hold. Substituting (5.8) in (5.7) and using $V_o(n-1) \cong V_o(n-3/2)$ one arrives at

$$V_o(n) \cong k \cdot \left[1 - \mu^2 \cdot (1+k) \cdot (1+k+k')\right] \cdot V_{in}\left(n - \frac{1}{2}\right) + \left[1 - \mu^2 \cdot (1+k)^2\right] \cdot V_o(n-1) + \mu \cdot (1+k)^2 \cdot V_{os} \tag{5.9}$$

An identical analysis can be easily done for the integrator in Figure 5.2a. Table 5.1 compiles these results, indicating the gain and phase errors as given by (5.3).

Parameter	Forward Euler integrator	Nagaraj integrator	Predictive Nagaraj integrator
$\Delta\alpha$	$-\mu \cdot (1+k)$	$-\mu \cdot (1+k+k')$	$-\mu^2 \cdot (1+k+k') \cdot (1+k)$
$\Delta\beta$	$-\mu \cdot k$	$-\mu^2 \cdot k$	$-\mu^2 \cdot (1+k)^2$
γ	k	$\mu \cdot k$	$\mu \cdot (1+k)^2$

Table 5.1: Gain and pole errors for the SC integrators shown in Figure 5.2.

Both the Nagaraj integrator and the predictive Nagaraj integrator yield significant suppression of the offset voltage and low-frequency noise, with the latter having a slight disadvantage. Since the holding capacitor C_H also samples the output voltage (input-referred output voltage) of the previous cycle, the pole error $\Delta\beta$ is reduced by a factor equal to the dc gain of the amplifier. The effective dc gain is then A^2, and these circuits are commonly referred to as gain-enhanced or gain-squaring stages. The holding capacitor in the predictive Nagaraj integrator, however, does not sample the previous value of the

output voltage, but rather a prediction of the future value. The result is both a gain-squaring effect and a much lower gain error $\Delta\alpha$. In conclusion, compensation of nonidealities which affect the transfer of the charge corresponding to the input signal (through the virtual ground of the amplifier), such as the offset voltage or the op-amp dc gain, can be cancelled if those nonidealities are previously determined or estimated, such that their effect can be properly subtracted.

Clearly, both Nagaraj structures can yield considerably better performance than the regular forward-Euler integrator (and as may have been noticed, in opposite phases!). Since in switched-capacitor circuits the accuracy of the gain factor is ultimately determined by the matching accuracy of the capacitors, the improvement obtained through the use of the predictive Nagaraj integrator may not seem to be of much significance. In that case, we are tempted to favor the simple Nagaraj integrator, as it provides a smaller pole error and better low-frequency noise suppression. The foregoing analysis neglected, however, two important aspects: one is the frequency dependence of the compensation (the values given in Table 5.1 affect most the low-frequency values), and the other is the nonlinear gain characteristic of the amplifier. Although the former is not of much importance for us (we are dealing with narrow-band low-pass signals), it should be mentioned that the gain and phase errors in the predictive Nagaraj integrator remain nearly flat with frequency, whereas they increase in the Nagaraj integrator, soon exceeding those in the predictive structure [61]. Hence, for wideband signals (for example in ISDN applications, where the signal band is 80 kHz), this feature is very important. More important to us is the distortion resulting from the nonlinear characteristic of the amplifier. The following Section is devoted to the discussion of this issue, and constitutes an extension of the work initiated by Huang [68][64].

5.3 ANALYSIS OF DISTORTION IN SC INTEGRATORS DUE TO THE NONLINEAR GAIN CHARACTERISTIC OF THE AMPLIFIER

In this Section we develop an analysis identical to the one presented in the previous Section, but considering a generic, possibly nonlinear, gain characteristic $f(v_{in})$ for the amplifier.

If the output voltage V_o of the amplifier relates to its input voltage V_{in} according to

$$V_o = f(V_{in}) \tag{5.10}$$

the output voltage of the Nagaraj integrator in phase #1 is given by (Appendix D)

$$V_o\left(n+\frac{1}{2}\right) = k \cdot V_{in}\left(n-\frac{1}{2}\right) + V_o\left(n-\frac{1}{2}\right) + V_e \tag{5.11}$$

where the residual term V_e is given by

$$\begin{aligned} V_e = {} & -k \cdot f^{-1}\left[V_o(n)\right] + (1+k+k') \cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] \\ & - (1+k') \cdot f^{-1}\left[V_o\left(n+\frac{1}{2}\right)\right] \end{aligned} \tag{5.12}$$

and $f^{-1}(x)$ denotes the inverse function of $f(x)$. The first two terms in equation (5.11) constitute the desired output voltage that is a sample of the input signal added to the previous output voltage, while V_e an unwanted error. Interestingly, the offset voltage does not appear in an explicit form in (5.12), but it is present in the nonlinear terms in the output voltage. For that reason, the magnitude of those components is expected to be small, since the inverse function of the amplifier gain is a small quantity. This clearly indicates that offset compensation is indeed being accomplished.

Analogously, one can obtain the relation describing the output signal of the predictive Nagaraj integrator in phase #2:

$$V_o(n) = k \cdot V_{in}\left(n-\frac{1}{2}\right) + V_o(n-1) + V_e \tag{5.13}$$

where $k_1 = k_2 = k$ was used. The residual term V_e is now given by

$$\begin{aligned} V_e = {} & (1+k) \cdot \{f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] - f^{-1}[V_o(n)]\} \\ & + \{f^{-1}[V_o(n-1)] - f^{-1}\left[V_o\left(n-\frac{3}{2}\right)\right]\} \end{aligned} \tag{5.14}$$

It can also be shown that the output voltage of the forward-Euler integrator is described by

$$V_o(n) = k \cdot V_{in}\left(n-\frac{1}{2}\right) + V_o(n-1) + V_e \tag{5.15}$$

with

$$V_e = k \cdot V_{os} + f^{-1}[V_o(n-1)] - (1+k) \cdot f^{-1}[V_o(n)] \tag{5.16}$$

where the offset voltage shows up explicitly, indicating that no cancellation is taking place.

Note that in equations (5.11), (5.13) and (5.15) the error term V_e accounts for the nonideal behavior of the structure, in this case attributable to the amplifier. Since V_e can result in harmonic distortion it should be minimized. To better understand the significance of the results above, let us consider the waveform shown in Figure 5.3. It qualitatively

represents the output voltage of a SC integrator when used in a delta-sigma modulator. The peculiarity of this waveform is that since the feedback signal can switch frequently between $+V_{REF}$ and $-V_{REF}$, and the input signal varies slowly since it is oversampled, successive samples of the output signal of the integrator can differ by as much as $k \cdot V_{REF}$. (The same can happen when the integrator is used in a Nyquist-rate SC filter, in which case successive samples of the input signal can differ quite a bit.) The waveform in Figure 5.3 is representative of the behavior of the three integrators described above.

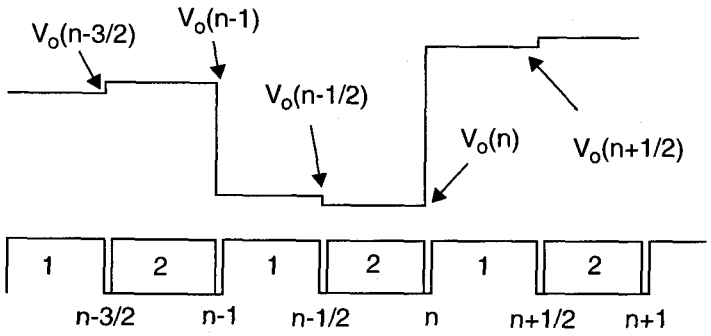

Figure 5.3: Typical waveform for the output voltage of a SC integrator in a delta-sigma modulator.

Referring to this Figure and making use of the previous results, compiled for convenience in Table 5.2, one can see that the residual term V_e in the predictive Nagaraj integrator can be significantly smaller than that in the other structures. This is due to the subtraction of nearly identical error terms belonging to the same clock period. Thus, it appears that this structure can also compensate for the nonlinear characteristic of the op-amp gain, and hence be successfully used in a low-voltage environment with low gain single-stage amplifiers. In the remainder of this chapter we will concentrate on the analysis of the predictive Nagaraj integrator, in the context of delta-sigma modulation.

Integrator type	Error Voltage V_e
Forward-Euler	$k \cdot V_{os} + f^{-1}[V_o(n-1)] - (1+k) \cdot f^{-1}[V_o(n)]$
Nagaraj	$-k \cdot f^{-1}[V_o(n)] + (1+k+k') \cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right]$ $- (1+k') \cdot f^{-1}\left[V_o\left(n+\frac{1}{2}\right)\right]$
Predictive Nagaraj	$(1+k) \cdot \{f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] - f^{-1}[V_o(n)]\}$ $+ \{f^{-1}[V_o(n-1)] - f^{-1}\left[V_o\left(n-\frac{3}{2}\right)\right]\}$

Table 5.2: Residual voltage error due to the amplifier finite dc gain for a forward-Euler integrator, a Nagaraj integrator and a predictive

5.4 PREDICTIVE CDS AND DELTA-SIGMA MODULATION

A question which one should ask refers to the nature of the input signal of the predictive Nagaraj integrator. As explained earlier, the operation of this structure is based on the assumption of a sampled-and-held input signal. One can conceive, however, that if the oversampling ratio is relatively high (inherent to delta-sigma modulation), the error introduced by using a continuous-time signal will be negligible. As the complete analysis reveals (Appendix D), using a continuous-time signal results in a frequency (weak) dependence of the gain factor and pole location. Indeed, the input signal and previous voltage terms in (5.9) appear multiplied by (different) factors of the type $a + b \cdot z^{-1/2}$, where $b \ll a$. Simulations show that oversampling ratios in excess of 16 result in negligible degradation of the performance.

The timing of the loop, however, has to be such that the reference voltage does not change during the period corresponding to one prediction and one integration. For the

example shown in Figure 5.3, the reference voltage must change at the beginning of phase #1, and at no other time. As discussed in Section 3.5, this results in more stringent requirements for the comparator, which has to be faster. Moreover, the amplifier has to settle in the same clock phase, which may not be of much concern since phase #1 corresponds to the prediction phase rather than the integration one. Besides, with this technique the amplifier operates in both phases, regardless of the switching activity of the reference voltage. This is the first obvious penalty for using this structure in a delta-sigma modulator.

At this point it is useful to evaluate the efficiency of the technique by providing a simulated example. To accomplish that, we will introduce a nonlinear gain characteristic for the amplifier. An input-output relation for the amplifier suitable for simulation is given in equation (5.17).

$$V_{in} = f^{-1}(V_o) = \frac{V_o}{A_0 \cdot \left(1 - \gamma_1 \cdot V_o - \gamma_2 \cdot V_o^2\right)} \tag{5.17}$$

A_0 is the nominal dc gain of the amplifier, and γ_1 and γ_2 introduce odd- and even-order harmonic distortion, γ_2 being responsible for most of the roll-off of the amplifier gain with the signal level. Ideally, $\gamma_1 = \gamma_2 = 0$. Figure 5.4 plots the gain dV_o/dV_{in} (5.17) for $A_0 = 38\,\text{dB}$ (this value is representative of the gain which can be obtained with a single-stage amplifier), $\gamma_1 = 0.01\ \text{V}^{-1}$ and $\gamma_2 = 1.2\,\text{V}^{-2}$. Also shown is a more typical gain characteristic (from SPICE simulations) of an amplifier (dashed line).

As can be seen from Figure 5.4, the equation above is somewhat pessimistic since the gain drops more rapidly (it becomes a very good approximation as the power supply voltage is much reduced). Both curves result in about 2 dB gain drop at ±0.4 V. Note also that the asymmetry relative to $V_o = 0\,\text{V}$, due to γ_1, is responsible for odd harmonic

distortion. In the simulation, (5.17) is solved numerically (iteratively), based on the estimated output signal level as a function of the input signal.

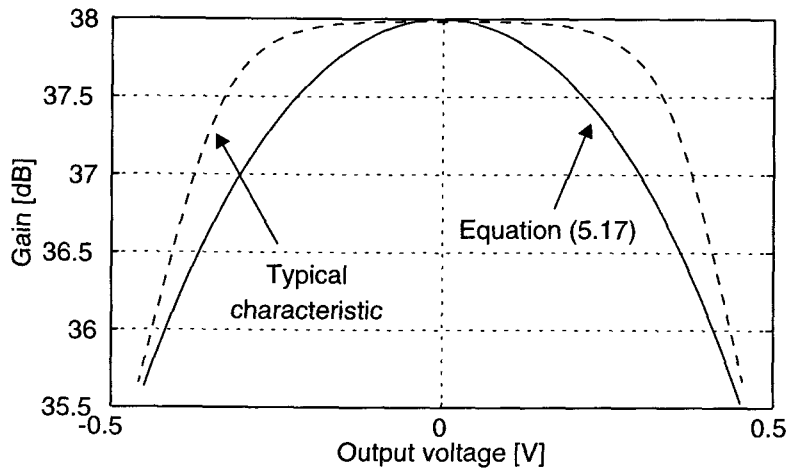

Figure 5.4: Op-amp nonlinear dc gain characteristic as given by (5.17), for $A_0 = 38\,\text{dB}$, $\gamma_1 = 0.01\,\text{V}^{-1}$ and $\gamma_2 = 1.2\,\text{V}^{-2}$ (solid line). Also shown is a typical gain characteristic of an amplifier (dashed line).

Figure 5.5 compares the simulated spectra of the output signal of a 2nd-order delta-sigma modulator when the input stage is a regular forward-Euler integrator, and when it is a predictive Nagaraj integrator. Figure 5.5a shows the results when a single tone is applied, and Figure 5.5b when two tones are applied. The latter is an important test to evaluate intermodulation distortion, a critical parameter in communication systems. It can be seen that the predictive Nagaraj integrator yields a significant improvement in performance. Indeed, the in-band tones -- harmonic distortion and intermodulation products -- are attenuated by about 20 dB. It can be seen that if quantization noise were a limiting factor (unlikely in low-voltage operation), there would be also an improvement in the signal-to-noise ratio, as the quantization noise floor is lower. As expected, the dc offset voltage is also much attenuated.

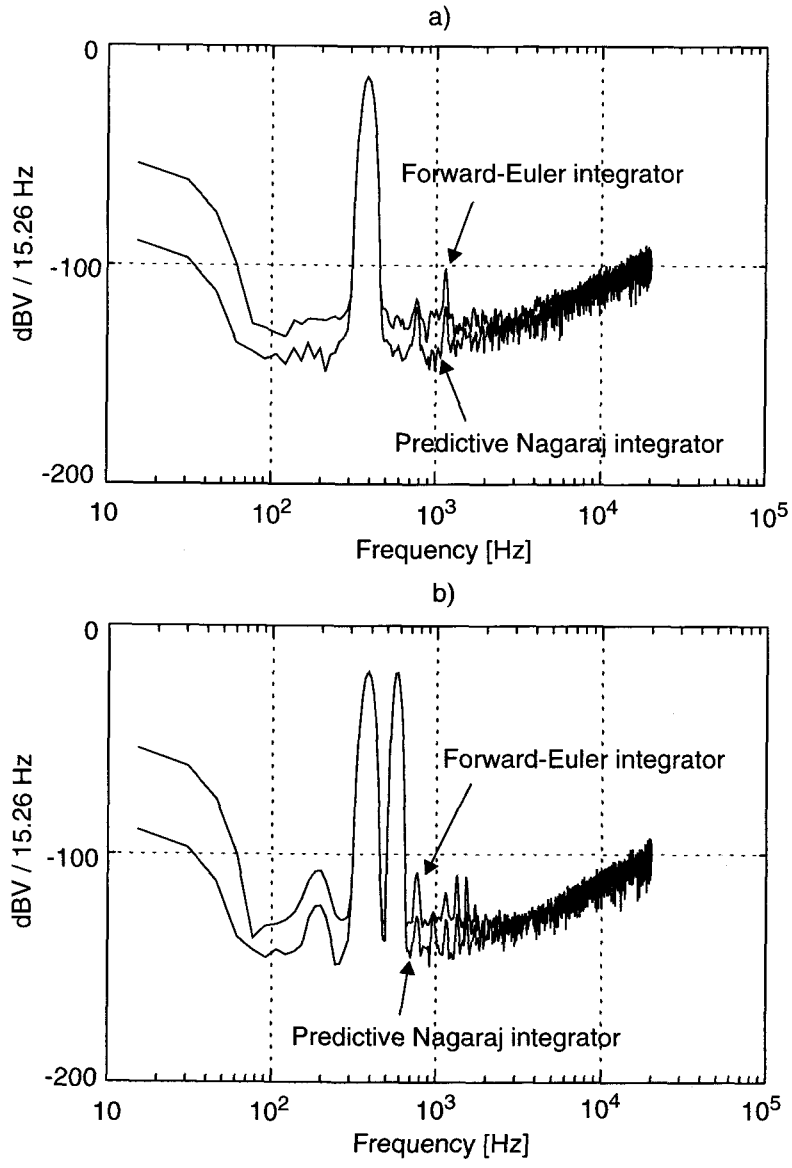

Figure 5.5: Output spectra of a 2nd-order delta-sigma modulator when the input stage is a forward-Euler SC integrator and when the input stage is a predictive Nagaraj integrator. a) The input signal is a 400 Hz sinusoid with power -10.5 dBV. b) The input signal is a 2-tone, 400 Hz and 600 Hz, signal, each tone with power -16 dBV. The sampling frequency was 2 MHz in both cases, and the assumed op-amp dc offset voltage was 3 mV.

Note that the approximation for the pole error given in Table 5.1 is, to a first order, independent of $k' = C_H/C_B$. In actuality, the pole error is a decreasing function of this parameter, although the gain error increases with increasing k'.

Since the predictive CDS technique results in the compensation of the finite dc gain of the amplifier, it is important to calculate the resulting equivalent dc gain. To do this, we will use the fact that this technique leads to the definition of a new, improved, virtual ground node in the circuit *i.e.*, node x in Figure 5.2, and define the equivalent gain as the ratio between the output voltage and the difference between the non-inverting node and the virtual ground voltages. From the values stored in the holding capacitor C_H in phases #1 and #2, one arrives at the following expression for the equivalent amplifier gain:

$$A_{eq}(n) = \frac{A}{1 - \frac{V_o\left(n-\frac{1}{2}\right)}{V_o(n)}} \Leftrightarrow \mu_{eq}(n) = \mu \cdot \left[1 - \frac{V_o\left(n-\frac{1}{2}\right)}{V_o(n)}\right] \tag{5.18}$$

Note that this definition displays a dependence with time, and hence with the input signal. This is due to the unwanted signal-dependent residual terms resulting from incomplete compensation. Figure 5.6a plots equation (5.18) when the input signal is a 1 kHz, -10.5 dBV power sinusoid; the original op-amp dc gain characteristic is that shown in Figure 5.4. Clearly, for most V_o values the equivalent gain is considerably higher than the nominal 38 dB. However, two interesting behaviors can be noticed. One is that A_{eq} drops for low values of the output signal level. This is not paradoxical; it is a consequence of the definition given in (5.18), in which the output voltage may eventually become smaller than the residual terms stored in the holding capacitor C_H. (The residual voltage across C_H contains terms in the offset voltage and previous values of the output voltage V_o, whose magnitude may exceed the new value of the input-referred output voltage) Therefore, it does not reflect the true performance of the technique.

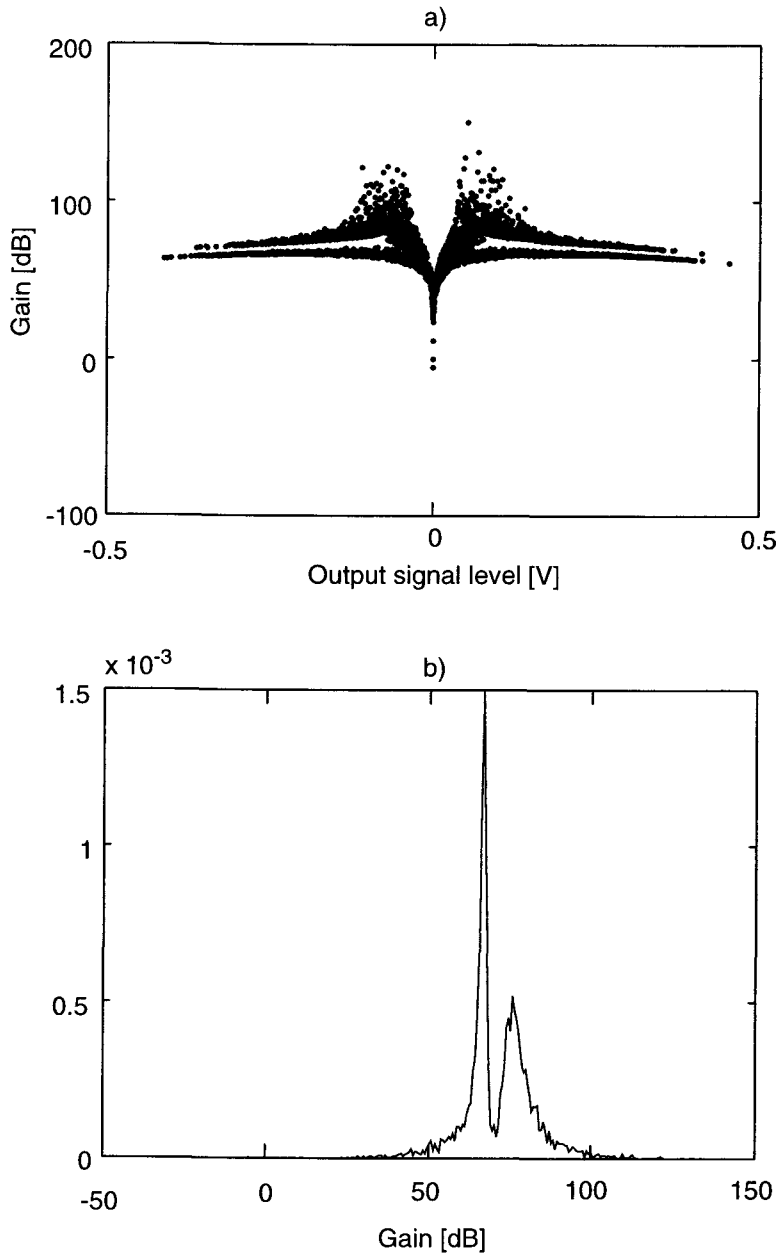

Figure 5.6: Equivalent dc gain of the amplifier. a) As a function of the output signal level. b) Histogram of 5000 samples.

Another interesting feature shown in Figure 5.6a is the existence of four distinct loci for the equivalent gain (or two, if only positive or negative signals are considered). Figure 5.6b plots the histogram of 5000 samples, clearly showing the two different regions (the mean value is about 70 dB). These different regions are a consequence of the type of the input signal utilized (trajectory of the signal), and are a function of the input signal amplitude. (If the input signal were a random signal with a uniform distribution then those loci would give place to a single cloud.)

Each region corresponds to about one fourth of the sinusoid. The lower branches correspond to the regions of the input signal near the zero crossings; the upper branches correspond to the signal regions approaching the reference voltage value. As the power of the input signal is reduced, the height of the second (right-most) peak in Figure 5.6b reduces, eventually vanishing, whereas the first peak increases. This can be attributed to the higher density of "ones" or "zeros," depending on whether the signal is positive or negative, respectively, in the feedback path for large values of the input signal. Due to the finite dc gain of the amplifier, such large density results in a drift of the virtual ground voltage, and hence in a less efficient compensation. Therefore, one can conclude that the upper branches correspond to erroneous evaluations of the equivalent gain, similarly to what occurs for very small values of the output signal level.

Figure 5.7 plots the histograms of the virtual ground signals, normalized to the maximum occurrence, in a forward-Euler integrator and in a predictive Nagaraj integrator, in the presence of a 3 mV amplifier dc offset voltage. The mean value and the standard deviation reduce from 3.1 mV and 2.1 mV to 48 μV and 58 μV, respectively.

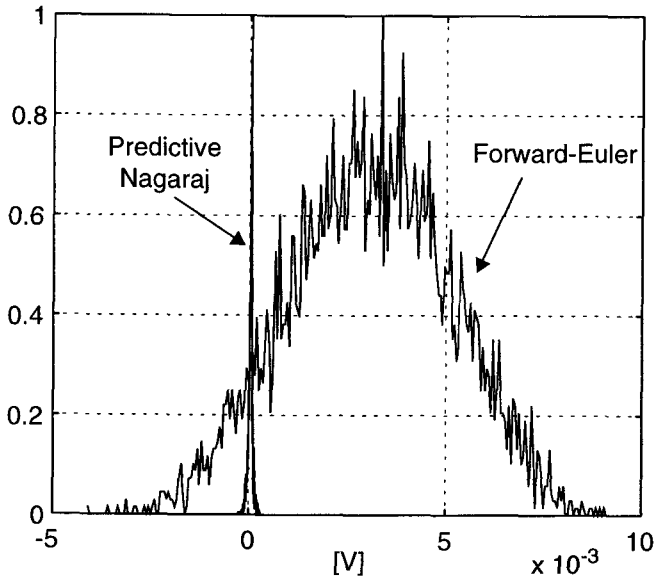

Figure 5.7: Histograms of the virtual ground signal for a forward-Euler integrator and a predictive Nagaraj integrator.

5.5 AC ANALYSIS OF A SC PREDICTIVE NAGARAJ INTEGRATOR

The methodology presented in Chapter 3, used to derive the power dissipation of the first-stage amplifier as a function of its capacitive load, applies also to more general SC integrator stages. Indeed, the power dissipation of the amplifier is determined by its *equivalent* ac capacitive load which, in turn, is determined by global parameters like dynamic range, reference voltage and oversampling ratio. Therefore, the conclusions at which we arrived in Chapter 3 still apply to integrator structures employing CDS techniques, and will not be repeated here.

However, since a predictive Nagaraj integrator possesses more circuit elements than a simple forward-Euler integrator, it is expectable that the criteria leading to minimum capacitance (hence power dissipation) will be different. In fact, the new degrees of freedom may even require a compromise. The objective is the global minimization of

load capacitance (partly determined from dynamic range requirements), and of the errors arising from the various capacitance ratios.

Another important issue relates to the time constant of the circuit during the integration and prediction phases. Incomplete settling of the amplifier, if linear, results in a gain error. Since gain compensation in the predictive Nagaraj integrator is achieved through the prediction of the output voltage value, and therefore by storing information on the gain error for that output signal voltage, the capacitive load of the amplifier should ideally be the same in both phases. This additional constraint may impose different requirements on the values of the capacitances that can be used. Figure 5.8 shows the effect of different time constants in the integration and prediction phases. To model this mismatch, the nominal dc gain was artificially made different in order to emulate the gain error resulting from having different time constants. In this example (where the parameters were the same ones used to obtain Figure 5.5a), the total harmonic distortion increased by about 5 to 7 dB when the gain during either the prediction or integration phase was reduced by about 20%. It can be seen that when the accuracy is lower during the prediction phase (lower nominal gain), the error is slightly larger (curve b). However, although not shown, the low-frequency noise floor was higher when a lower dc gain value was used during the integration phase. Hence, to minimize these nonidealities the settling behavior of the amplifier should be identical in both phases, that is the loads should be equalized.

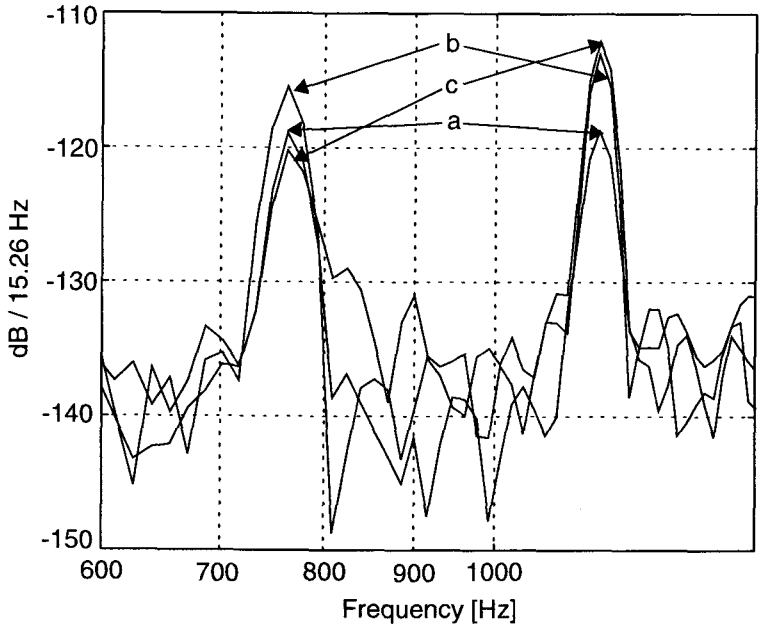

Figure 5.8: Magnified output spectrum of a 2nd-order delta-sigma modulator (showing signal harmonics) when the input stage is a predictive Nagaraj integrator. Curve a corresponds to utilizing a nominal gain of 38 dB in both prediction and integration phases. Curve b corresponds to utilizing a 20% lower gain in the prediction phase, and curve c corresponds to utilizing a 20% lower gain in the integration phase.

Figure 5.9 shows the circuit configuration of a predictive Nagaraj integrator in the prediction and integration phases. For simplicity, the only parasitic capacitance taken into consideration is the op-amp input capacitance C_p (it is also the most important one). The parameters which are unique, and in terms of which all remaining parameters can be expressed, are the input capacitor in the integration phase C_{in}, the input capacitor in the prediction phase C_A, the gain factor $k = C_{in}/C_F = C_A/C_B$, the holding capacitor C_H, the op-amp input capacitance C_p, and the op-amp load capacitance C_L.

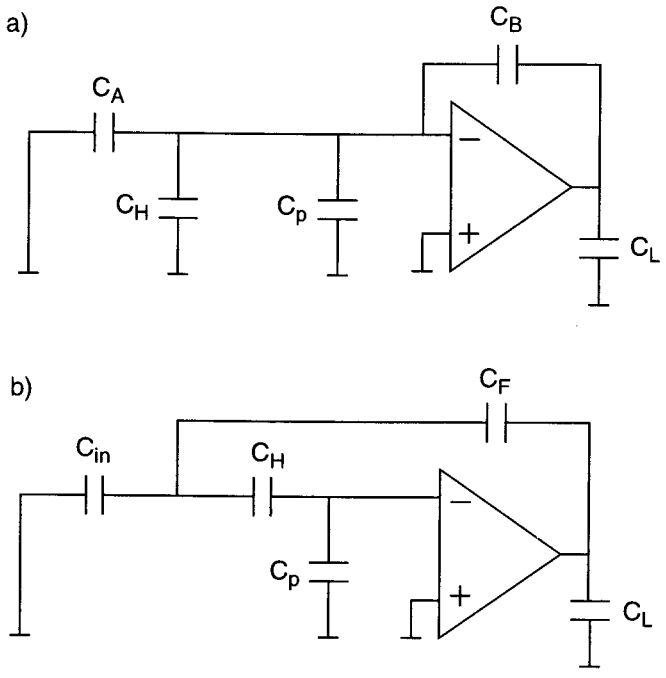

Figure 5.9: Circuit configuration of a predictive Nagaraj integrator in the a) prediction phase and the b) integration phase.

The capacitive load determining the closed-loop time constant is obtained from dividing the open-loop capacitive load by the feedback factor. Hence, the equivalent load during prediction (phase #1 in Figure 5.2) is given by

$$C_{TP} = \frac{C_L + \dfrac{C_{iP} \cdot C_B}{C_{iP} + C_B}}{\dfrac{C_B}{C_B + C_{iP}}} \tag{5.19}$$

where

$$C_{iP} = C_A + C_H + C_p \tag{5.20}$$

is the total input capacitance in the prediction phase. Substituting (5.20) into (5.19), and using $k = C_{in}/C_F = C_A/C_B$, one arrives at

$$C_{TP} = \left[1 + k \cdot \left(1 + \frac{C_H}{C_A} + \frac{C_p}{C_A}\right)\right] \cdot C_L + C_A + C_H + C_p \tag{5.21}$$

Analogously, the capacitive load seen during integration is given by

$$C_{TI} = \frac{C_L + \dfrac{C_{iI} \cdot C_F}{C_{iI} + C_F}}{\dfrac{C_F}{C_F + C_{iI}} \cdot \dfrac{C_H}{C_H + C_p}} \tag{5.22}$$

where C_{iI} is the total input capacitance during the integration phase:

$$C_{iI} = C_{in} + \frac{C_H \cdot C_p}{C_H + C_p} \tag{5.23}$$

Substituting (5.23) into (5.22) we obtain

$$C_{TI} = \left[\left[\left(\frac{1}{C_H} + \frac{1}{C_{in}}\right) \cdot k + \frac{1}{C_H}\right] \cdot C_p + k + 1\right] \cdot C_L + \left(1 + \frac{C_p}{C_H}\right) \cdot C_{in} + C_p \tag{5.24}$$

Note that the presence of the op-amp input parasitic capacitance results in a reduction of the feedback factor, and hence in an increase of the equivalent capacitive load. For this reason, one can predict that a critical parameter in the minimization of the power dissipation is ratio between C_H and C_p, which should then be maximized.

To determine conditions for equality of the capacitive loads given by (5.21) and (5.24), and hence derive the optimum value for the holding capacitor C_H, we will compare three scenarios. In one case we assume that $C_p = 0$, that is no parasitics exist. In another case we will assume that $C_p \neq 0$, but $C_A = C_{in}$. The third scenario is more general: $C_p \neq 0$ and $C_A \neq C_{in}$. The minimum value of these capacitances in either case is determined from noise considerations, a subject to be addressed later.

In the absence of parasitics, equality of both capacitive loads requires that

$$C_H = \frac{C_{in} - C_A}{1 + k \cdot \frac{C_L}{C_A}} = C_{H0} \tag{5.25}$$

Using this value for the holding capacitor results in the following equivalent load (equal in both phases)

$$C_{T0} = (1 + k) \cdot C_L + C_{in} \tag{5.26}$$

Interestingly, C_{T0} is equal to the load seen by the amplifier during the integration phase in a *forward-Euler* integrator. Therefore, the same amplifier can be used without any degradation of the settling behavior. This can be achieved as long as $C_{in} > C_A$, as can be appreciated from (5.25). If $C_A > C_{in}$, equality of the capacitive loads cannot be attained. Although in principle one can choose any value for C_A (such that $C_{in} > C_A$), the choice should result in a practical value for C_H. The latter increases with C_A at first, and then decreases. From equation (5.25) one can easily obtain the maximum value for C_H (a somewhat convoluted result). The maximum occurs when

$$C_A = \sqrt{k \cdot C_L \cdot (C_{in} + k \cdot C_L)} - k \cdot C_L \tag{5.27}$$

For example, if $k = 0.25$, $C_L = 1\,\text{pF}$, and $C_{in} = 2\,\text{pF}$, the maximum C_H occurs for $C_A = 0.5\,\text{pF}$ yielding $C_H = 1\,\text{pF}$. Note, however, that regardless of the choice for the value of C_A, the total load remains unchanged, in this example equal to 3.25 pF. If $C_L = 0$, then $C_H = C_{in} - C_A$, which should not come as a surprise since in such case the load of an operational transconductance amplifier is determined by its total input capacitance only.

In practice, the op-amp input parasitic capacitance is not zero, especially in high-speed operation where large transconductances are required from the input devices of the amplifier. At low speed, however, the situation just presented is approachable. In the more general case when the parasitics cannot be neglected, the following quadratic expression results from the equality condition of the capacitive loads:

$$C_H^2 - \left[\frac{C_{in} - C_A}{1 + k \cdot \dfrac{C_L}{C_A}} + \frac{\left(\dfrac{1}{C_{in}} - \dfrac{1}{C_A}\right) \cdot C_p \cdot C_L \cdot k}{1 + k \cdot \dfrac{C_L}{C_A}} \right] \cdot C_H - \left(\frac{(1+k) \cdot C_L + C_{in}}{1 + k \cdot \dfrac{C_L}{C_A}} \cdot C_p \right) = 0 \tag{5.28}$$

Using the results above, (5.28) can be written as

$$C_H^2 - \left[C_{H0} + \frac{\left(\dfrac{1}{C_{in}} - \dfrac{1}{C_A}\right) \cdot C_p \cdot C_L \cdot k}{1 + k \cdot \dfrac{C_L}{C_A}} \right] \cdot C_H - \left(\frac{C_{T0}}{1 + k \cdot \dfrac{C_L}{C_A}} \cdot C_p \right) = 0 \tag{5.29}$$

This expression can be greatly simplified if we choose $C_A = C_{in}$. In such case the second term becomes zero, yielding for C_H

$$C_H = \sqrt{\frac{C_{T0} \cdot C_p}{1 + k \cdot \frac{C_L}{C_A}}} \tag{5.30}$$

The total load is now

$$C_T = C_{T0} + \left(1 + k \cdot \frac{C_L}{C_A}\right) \cdot \left(C_p + \sqrt{\frac{C_{T0} \cdot C_p}{1 + k \cdot \frac{C_L}{C_A}}}\right) \tag{5.31}$$

Note that C_{T0} is not constant, since $C_A = C_{in}$. As can be appreciated from (5.30) and (5.31), the value of the holding capacitor is an increasing function of C_A, but the total capacitance still displays a minimum. This minimum can be determined from equating the derivative of (5.31) to zero and solving for C_A. When $C_A \neq C_{in}$, (5.28) has to be used to determined the value of C_H which yields equal loads. The result is, as expected, rather complex and an expression will not be given here.

Figure 5.10 plots the curves obtained for the three scenarios analyzed with the parameters of the example above. The main conclusions which can be inferred from this Figure and the previous analysis are: a) minimum capacitive load, and hence minimum power dissipation, is obtained when the parasitics can be made negligible compared to the capacitive components, especially C_H. In such case, the equalization of the capacitive loads during prediction and integration is possible only if $C_A \leq C_{in}$. b) Using $C_A \neq C_{in}$ will always result in a larger capacitive load, and hence increased power dissipation,

except when C_A is larger than C_{in} (and there is no apparent reason to use $C_A > C_{in}$). It also results in increased area, since a larger value for the holding capacitor is required.

Note that in curves e and f, $C_{in} = 2\,\text{pF}$, a fixed value, whereas C_A is changing. Although a minimum can still be reached, it will be higher than the minimum that can be obtained when $C_A = C_{in}$.

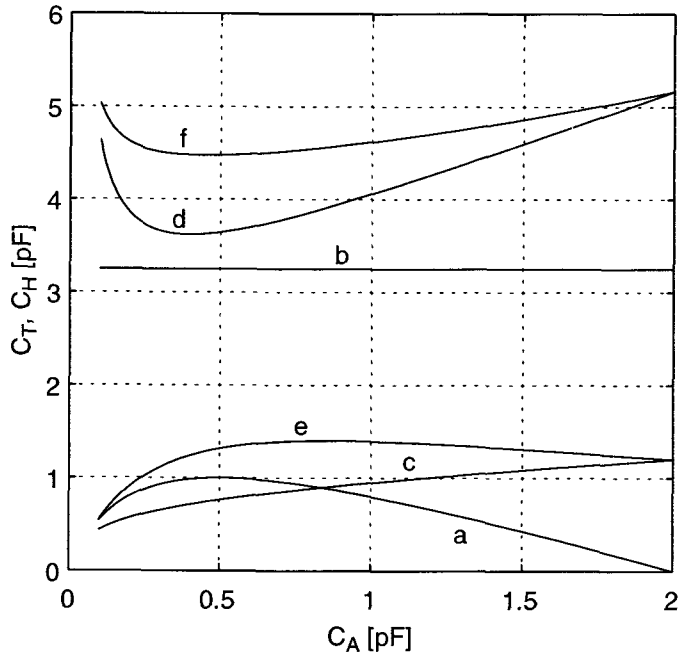

Figure 5.10: Value of the holding capacitor C_H required to achieve equality of the capacitive loads during prediction and integration in a predictive Nagaraj integrator, and the resulting equivalent load C_T. a: C_H for $C_p = 0$. b: C_T for $C_p = 0$. c: C_H for $C_p \neq 0$ and $C_A = C_{in}$. d: C_T for $C_p \neq 0$ and $C_A = C_{in}$. e: C_H for $C_p \neq 0$ and $C_A \neq C_{in}$. f: C_T for $C_p \neq 0$ and $C_A \neq C_{in}$.

The foregoing analysis focused only on determining conditions resulting simultaneously in equal and minimum capacitive loads during the prediction and integration phases. These conditions lead to optimum performance and minimum power dissipation. The following section analyzes the predictive Nagaraj integrator for kT/C noise performance, and how it may affect the conclusions reached in this Section. In particular, there is no guarantee that minima determined above can be used and still achieve the required noise performance (dynamic range).

5.6 ANALYSIS OF THE *kT/C* NOISE IN A PREDICTIVE NAGARAJ INTEGRATOR

The analysis presented in this section addresses the case when the gain of the amplifier is linear, and considers only the contributions to the total thermal noise by the ON-resistance of the MOS switches. The objective is to determine the trade-off between the *kT/C* noise performance and the minimization of the amplifier power dissipation, as developed in the previous Section. For simplicity we will consider only the case where the input capacitance of the amplifier can be neglected compared to the holding capacitor. As discussed above, some situations may require the inclusion of this parasitic element for a more accurate calculation. However, the general conclusions reached in the following analysis still apply to the more complex models.

Observation of Figure 5.2c indicates that *kT/C* noise is generated in both phases of operation, prediction and integration. If the dc gain of the amplifier were infinite, (in which case there would be no point in utilizing the CDS structure for the reduction of distortion) the noise contribution of the prediction branch would not affect the integration phase of operation, since this could only happen through the holding capacitor C_H and the virtual ground of the amplifier. This is not strictly true in practice, but as we will see, this contribution is negligible compared to the that due to C_H itself. Figure 5.11a shows the circuit configuration during the prediction phase. Also shown are the noise sources

associated with C_A and C_H, whose noise power is $\overline{v_A^2} = 2 \cdot kT/C_A$ and $\overline{v_H^2} = kT/C_H$, respectively. (Note that the holding capacitor samples the thermal noise only once.) Applying the KCL and using $V_x = -\mu \cdot V_o$ yields the output noise

$$\overline{V_o} = -\frac{C_A \cdot \overline{v_A} + C_H \cdot \overline{v_H}}{C_B + \mu \cdot (C_A + C_H + C_B)} \tag{5.32}$$

where $\bar{v}$ denotes the root-mean-square (rms) value of v. Then, the value stored in the holding capacitor at the end of the prediction phase is

$$\overline{v_{Hp}} = \overline{v_H} - V_x = \overline{v_H} - \mu \cdot \frac{C_A \cdot \overline{v_A} + C_H \cdot \overline{v_H}}{C_B + \mu \cdot (C_A + C_H + C_B)} \tag{5.33}$$

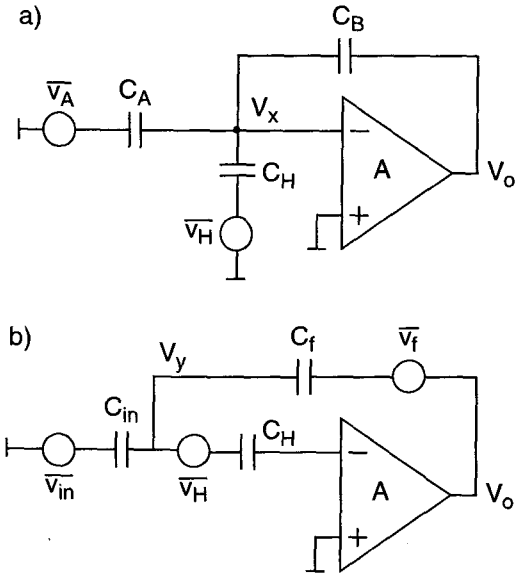

Figure 5.11: AC model of a predictive Nagaraj integrator showing the *kT/C* noise sources during a) prediction phase and b) integration phase.

Since the noise sources $\overline{v_A}$ and $\overline{v_H}$ are uncorrelated, the powers of the noise signal components stored in C_H add:

$$v_{Hp}^2 = \left[1 - \frac{\mu \cdot C_H}{C_B + \mu \cdot (C_A + C_H + C_B)}\right]^2 \cdot \frac{kT}{C_H} + \left[\frac{\mu \cdot C_A}{C_B + \mu \cdot (C_A + C_H + C_B)}\right]^2 \cdot \frac{2 \cdot kT}{C_A} \tag{5.34}$$

Due to the small value of $\mu = 1/A$, this expression can be approximated by

$$v_{Hp}^2 \cong \left(1 - 2 \cdot \mu \cdot k_1 \cdot \frac{C_H}{C_A}\right) \cdot \frac{kT}{C_H} \tag{5.35}$$

where $k_1 = C_{in}/C_f = C_A/C_B$. It can be seen that the *kT/C* noise leakage from the prediction branch is greatly attenuated by the gain of the amplifier, and hence should not be a limiting factor. Using, for instance, the values for C_H, C_A, k_1 and μ given in the example above, the error resulting from making $\mu = 0$ is only about 0.1 dB, a quantity hardly measurable. We will therefore neglect the noise leakage due to the prediction branch in the remainder of the analysis. (Note that the inclusion of the input capacitance of the amplifier would result in a term of comparable magnitude, and therefore negligible.) It can also be seen that the finite dc gain of the amplifier actually reduces the amount of noise that is sampled onto capacitor C_H. (A finite op-amp bandwidth would result also in a slight improvement of the noise performance.) This is due to the incomplete charge transfer which occurs when the op-amp gain and bandwidth are finite.

Figure 5.11b shows the circuit configuration during the integration phase, with indication of the noise sources associated with the input capacitor C_{in}, the feedback capacitor C_f, and the holding capacitor C_H. Unlike the regular forward-Euler integrator, the feedback capacitor also contributes with *kT/C* noise, as it is switched. Since the noise

sampled by C_f shows directly at the output, its transfer function is unity. To refer this noise to the input one must divide the transfer function to the output by the transfer function of the integrator, that is multiply by $\left(1-z^{-1}\right)/k_1$. The noise contributed by the holding capacitor C_H sees also a unity transfer function to the output. This can be explained by realizing that during the prediction phase (Figure 5.2c), the input and holding capacitors sample the same noise voltage at node x (noise due to the ON resistance of the switch connecting node x to ground during phase #1). Hence, during the integration phase, there is no charge redistribution due to $\overline{v_H}$ (Figure 5.11b), and the latter shows at the output node directly. Again, to refer this noise component to the input, one must multiply its (unity) transfer function to the output by $\left(1-z^{-1}\right)/k_1$:

Clearly, the contribution of the feedback and holding capacitors to the total noise power becomes very small due to the effect of the transfer function of the integrator. This noise shaping effect is identical to what occurs to noise signals injected at the node following the output of the first integrator. The total input-referred in-band noise power due to the three capacitors can then be easily calculated yielding

$$\begin{aligned} e_T^2 &= \frac{2\cdot kT}{OSR\cdot C_{in}} + \alpha_{fH}\cdot\left(\frac{kT}{C_f}+\frac{kT}{C_H}\right) \\ &\cong \frac{2\cdot kT}{OSR\cdot C_{in}} \end{aligned} \tag{5.36}$$

where the coefficient α_{fH} is given by

$$\alpha_{fH} = \frac{1}{3\cdot\pi\cdot k_1^2}\cdot\left(\frac{\pi}{OSR}\right)^3 \tag{5.37}$$

A critical comparative remark is now in place. It is clear that the noise performance of the predictive Nagaraj integrator is comparable to that of the forward-Euler integrator. The increased equivalent capacitive load during the prediction phase, and the necessity to equalize the time constants in both prediction and integration phases, imply that the predictive Nagaraj integrator will in general dissipate more power than the forward-Euler integrator. For this reason, the former is more likely to find a niche in applications where only moderate speed of operation is required. It is difficult, however, to ascertain the boundaries of its usefulness, as the trade-offs are many (for instance, clock charge injection, which was not considered in the foregoing analysis, may become an important issue). Namely, there is the potential benefit of the utilization of single-stage amplifiers which require much less power compared to their 2-stage counterparts. Moreover, if offset cancellation and low distortion are mandatory, then these structures may be required.

Examples of applications where predictive correlated double sampling may be effective include instrumentation applications, high-performance voice codecs, and other systems where medium-to-high resolution and medium speed are required.

5.7 SUMMARY

In this chapter we analyzed the properties of the correlated double sampling technique as a potential candidate technique in the design of low-voltage low-power delta-sigma modulators. The greatest advantage of the predictive Nagaraj integrator is the simultaneous compensation of the nonlinear gain characteristic of the amplifier, and low-frequency noise cancellation. Its greatest disadvantage is the increased equivalent capacitive load and circuit complexity, which results in increased power dissipation. The suitability of this technique is largely dependent upon the application, and hence cannot be easily generalized. Further work is required to identify the exact trade-offs for the applications of this technique.

Several other issues related to the design and performance of this structure were discussed. A performance comparison in terms of gain- and pole-errors, as well as of distortion between a forward-Euler integrator, a Nagaraj integrator and a predictive Nagaraj integrator was also presented.

6. CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

In this dissertation we investigated the constraints which arise when designing SC delta-sigma modulators for low-voltage operation, targeting also low power dissipation.

The minimum power dissipated is associated with the operation of sampling of the input signal. This operation results in *kT/C* noise (superimposed to the input signal), whose power has to be lower than the noise power with origin in the processing circuitry that follows. When the dynamic range is limited by *kT/C* (thermal) noise, both power dissipation and dynamic range display proportionality to the (constant) product of the value of the switched capacitance and the square of the reference voltage. Hence, to reduce the minimum power dissipation, both the switched capacitance and the power supply voltage should be reduced.

Most current circuit techniques employ class-A amplifiers for their superior linearity. The power dissipation of these structures is proportional to the capacitive load, which should then be minimized. For constant dynamic range, reduction of the power supply voltage requires larger capacitances to reduce the noise floor level, and hence the power dissipation increases.

The overall system power dissipation is largely due to the operational amplifiers, whose power dissipation is typically 2 to 3 orders of magnitude larger than the minimum required to sample the input signal, especially those amplifiers in the front end which have to assure that the signal is acquired without degradation. Such is the case in delta-sigma modulators where the first stage integrator can be accountable for about 50% or more of the total power dissipation. Successive stages benefit from the noise shaping property which relaxes the performance requirements.

Minimization of the amplifier power dissipation requires, therefore, minimum capacitances and large signal swing. A large swing cannot be obtained utilizing cascode structures for the amplifiers. However, the removal of the cascode devices results in a significant drop in the value of the dc gain, reducing the linearity of the overall system. Hence cascaded topologies have to be favored. These, however, require frequency compensation for stability, which significantly increases the power dissipation. It is hence desirable to develop structures capable of achieving a compromise between signal swing and the dc gain of the amplifier. One such technique is predictive correlated double sampling, which compensates for the nonlinear characteristic of the amplifier, and also reduces its low-frequency noise. These techniques, however, result in a larger equivalent capacitive load of the amplifier, and hence increased power dissipation. Moreover, the added circuit complexity results also in increased clock charge injection, the effects of which may be difficult to compensate. These and other nonidealities may limit its usefulness to moderate-speed and moderate-performance applications.

6.2 FUTURE WORK

Further research on the predictive correlated double sampling technique is required to identify clearly the areas where its application would be successful, namely where low-voltage low-power operation is imperative. This work would culminate in a working prototype.

True low-voltage circuit techniques need to be developed which do not require, for instance, voltage doublers to drive the MOS switches. This technique will find limited application in sub-micron processes where the breakdown voltages are in the order of 3 V.

Micropower techniques are also needed in high-frequency applications. Frequently, some MOS devices are found to operate in weak or moderate inversion in RF

applications, due to the low value of the power supply voltage. A very important aspect is the correct modeling of these devices, which is not sufficiently well developed.

This work concentrated on the analog front end. Several researchers have proposed different solutions to implement the digital post-processor (decimation filter), but they all utilize linear filtering techniques based on sinc and FIR, brick-wall type of filters. Although significant improvements have been reported, which resulted in lower power dissipation, it is probably worthwhile to investigate the utilization of unconventional filtering techniques, such as nonlinear filtering. It is reasonable to expect that such techniques might be able to take advantage of the inherently nonlinear behavior of delta-sigma modulators, and possibly result in architecture- and power-efficient filtering structures.

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APPENDICES

APPENDIX A: AC ANALYSIS OF A SINGLE-STAGE OPERATIONAL AMPLIFIER

In this Appendix we develop the AC analysis of a single-stage amplifier and of a 2-stage amplifier with Miller frequency compensation, to derive the equations presented in Chapters 3 and 4.

Figure A.1a depicts a simplified model of a single-stage amplifier and Figure A.1b the same amplifier in a feedback configuration.

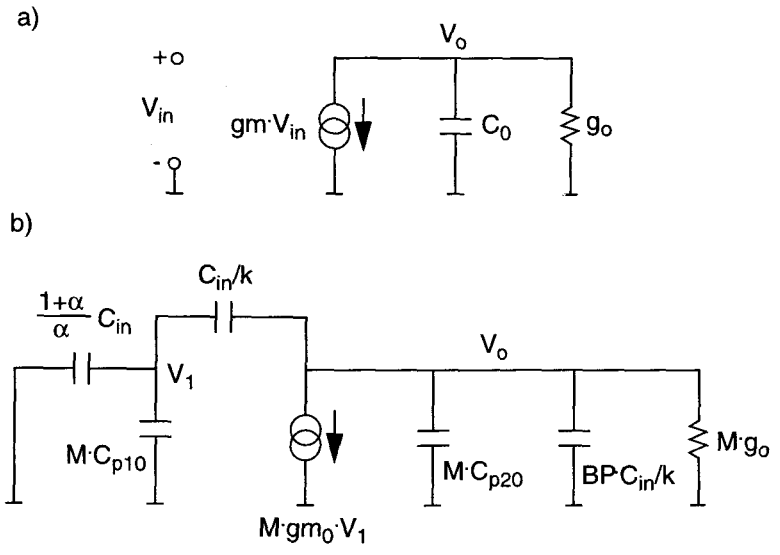

Figure A.1: Small-signal model of a single-pole amplifier a) in a stand-alone configuration and b) in a feedback configuration.

Applying the KCL to the two circuit nodes (V_1 and V_o) in Figure A.1b, one obtains the following system of equations:

$$s \cdot \frac{C_{in}}{k} \cdot (V_o - V_1) - s \cdot \left[M \cdot C_{p10} + C_{in} \cdot \left(1 + \frac{1}{\alpha} \right) \right] \cdot V_1 = 0 \tag{A.1a}$$

$$-M \cdot gm_0 \cdot V_1 = s \cdot \frac{C_{in}}{k} \cdot (V_o - V_1) + \left[s \cdot \left(M \cdot C_{p20} + \frac{BP}{k} \cdot C_{in} \right) + M \cdot g_o \right] \cdot V_o \tag{A.1b}$$

where s is the complex frequency (Laplace transform). Solving (A.1b) for V_1 yields

$$V_1 = \frac{1}{\left[1 + k \cdot \left(1 + \frac{1}{\alpha} \right) \right] + M \cdot \frac{C_{p10}}{C_{in}} \cdot k} \cdot V_o \tag{A.2}$$

Substituting (A.2) into (A.1a), and solving for s one obtains the natural frequencies of the system. Since this is a single-pole system, it has only one natural frequency. Moreover, the amplifier is in a feedback configuration, and hence the natural frequency corresponds to the closed-loop bandwidth BW:

$$-BW = \frac{-M \cdot g_o - \dfrac{M \cdot gm_0}{1 + k \cdot \left(1 + \frac{1}{\alpha} + M \cdot \frac{C_{p10}}{C_{in}} \right)}}{-M \cdot C_{p20} + \left[-1 - BP + \dfrac{1}{1 + k \cdot \left(1 + \frac{1}{\alpha} + M \cdot \frac{C_{p10}}{C_{in}} \right)} \right] \cdot \frac{C_{in}}{k}} \tag{A.3}$$

Collecting the terms in the multiplicity M one easily obtains:

$$M^2 + \frac{a \cdot BW + gm_0 + b \cdot g_o}{c \cdot BW + d \cdot g_o} \cdot C_{in} \cdot M + \frac{e \cdot BW}{c \cdot BW + d \cdot g_o} \cdot C^2_{in} = 0 \tag{A.4}$$

where the coefficients a through e are given by

$$
\begin{aligned}
a &= (1+BP)\cdot C_{p10} + C_{p20}\cdot\left(1+k+\frac{k}{\alpha}\right)\\
b &= 1+k+\frac{k}{\alpha}\\
c &= k\cdot C_{p10}\cdot C_{p20}\\
d &= k\cdot C_{p10}\\
e &= 1+\frac{1}{\alpha}+BP\cdot\left(1+\frac{1}{k}+\frac{1}{\alpha}\right)
\end{aligned}
\tag{A.5}
$$

Neglecting the output conductance g_o, using $gm_0 = B\cdot V_{GST}$, where $B = k'\cdot (W/L)_0\cdot (1+\lambda\cdot V_{DS})$ and V_{GST} denotes the gate overdrive voltage, and introducing a positive frequency notation (equation (A.4) reflects the fact that the pole is in the left-half complex plane), yields

$$
M^2+\left(a_n-b_n\cdot\frac{V_{GST}}{BW}\right)\cdot C_{in}\cdot M + c_n\cdot C^2{}_{in} = 0 \tag{A.6}
$$

where the new coefficients a_n, b_n and c_n are given by

$$
\begin{aligned}
a_n &= \frac{a}{c} = \frac{1}{C_{p10}}\cdot\left(1+\frac{1}{k}+\frac{1}{\alpha}\right)+\frac{1}{C_{p20}}\cdot\frac{1+BP}{k}\\
b_n &= \frac{B}{c} = \frac{B}{k\cdot C_{p10}\cdot C_{p20}}\\
c_n &= \frac{e}{c} = \frac{1+\frac{1}{\alpha}+BP\cdot\left(1+\frac{1}{k}+\frac{1}{\alpha}\right)}{k\cdot C_{p10}\cdot C_{p20}}
\end{aligned}
\tag{A.7}
$$

Solving equation (A.6) for *BW*, taking the derivative relative to the multiplicity *M*, and equating to zero one obtains

$$
M = \sqrt{c_n}\cdot C_{in} \tag{A.8}
$$

This zero of the derivative corresponds to a maximum of *BW*. Using (A.8) and (A6), one obtains for the maximum closed-loop bandwidth:

$$BW_{MAX} = \frac{b_n}{2 \cdot \sqrt{c_n} + a_n} \cdot V_{GST} \tag{A.9}$$

An important parameter in the design of systems employing feedback is the feedback coefficient defined as (Figure A.1b)

$$\beta = \frac{V_1}{V_o} \tag{A.10}$$

For the circuit shown in Figure A.1b, this parameter can be easily calculated yielding

$$\beta = \frac{\frac{C_{in}}{k}}{\frac{C_{in}}{k} + \frac{1+\alpha}{\alpha} \cdot C_{in} + M \cdot C_{p10}} = \frac{1}{1 + k \cdot \left(1 + \frac{1}{\alpha}\right) + M \cdot k \cdot \frac{C_{p10}}{C_{in}}} \tag{A.11}$$

The foregoing analysis was based on the amplifier's working in a linear manner, as in linear settling operation. The input transconductance and the circuit parasitic capacitances determine the natural frequency of the circuit which assumes the general form $p = gm/C_{Lac}$, where C_{Lac} is the equivalent (ac) closed-loop capacitive load. We can then use the previous expressions to determine C_{Lac}:

$$C_{Lac} = C_{inT} + C_{oT} + \frac{C_{inT} \cdot C_{oT}}{C_F} \tag{A.12}$$

where $C_{inT} = M \cdot C_{p10} + C_{in} \cdot (1 + 1/\alpha)$ is the total *input* capacitance, $C_{oT} = M \cdot C_{p20} + (BP/k) \cdot C_{in}$ the total *output* capacitance, and $C_F = C_{in}/k$ the total *feedback* capacitance (Figure A.1).

If the amplifier is in slewing mode, the feedback loop is ineffective, and therefore the load C_{Lsr} seen by the amplifier in this mode of operation is

$$C_{Lsr} = C_{oT} + \frac{C_{inT} \cdot C_F}{C_{inT} + C_F} \tag{A.13}$$

According to the definition of feedback coefficient (A.10) given above, $\beta = C_F/(C_{inT} + C_F)$. Taking the ratio between C_{Lac} and C_{Lsr} one arrives at

$$\frac{C_{Lac}}{C_{Lsr}} = \frac{1}{\beta} \tag{A.14}$$

Since the feedback coefficient does not exceed 1, we conclude that the capacitive load seen during linear settling is always greater or equal to the capacitive load seen during slewing.

Following the assumptions used to derive equation (3.25) in Chapter 3 for the minimum closed-loop bandwidth, $BW \geq 1.85 \cdot f_s \cdot DR$ [bits] , and the fact that

$$BW = \frac{gm}{C_{Lac}} = \frac{2 \cdot I_{BW}}{V_{GST} \cdot C_{Lac}} \tag{A.15}$$

one arrives at

$$I_{BW} = \frac{1.85 \cdot f_s \cdot V_{GST} \cdot DR\,[\text{bits}]}{2} \cdot C_{Lac} \tag{A.16}$$

The expression for the minimum bandwidth was derived from the following condition:

$$2^{-DR} \leq e^{-n}$$
$$\frac{n}{BW} = \frac{3}{8} \cdot T_S \tag{A.17}$$

where n is the number of time constants in $(3/8) \cdot T_S$. From this criterion, the time allowed for slewing is $(1/8) \cdot T_S$, and hence the current required is

$$I_{SR} = SR \cdot C_{Lsr} = \frac{8 \cdot k \cdot V_{REF}}{T_S} \cdot C_{Lsr} = \frac{8 \cdot k \cdot \beta \cdot V_{REF}}{T_S} \cdot C_{Lac} \tag{A.18}$$

It follows that the ratio of the two currents is

$$\frac{I_{BW}}{I_{SR}} = \frac{1}{8.65} \cdot \left(\frac{1}{k \cdot \beta}\right) \cdot \left(\frac{V_{GST}}{V_{REF}}\right) \cdot DR\,[\text{bits}] \tag{A.19}$$

In general, if we allocate $m \cdot T_S/2$ for slewing and $(1-m) \cdot T_S/2$ for settling, where ideally $m \in [0,1/2]$, the minimum closed-loop bandwidth BW required for settling within an accuracy of DR bits is

$$BW \geq \frac{\ln 4 \cdot f_s \cdot DR\,[\text{bits}]}{1-m} \tag{A.20}$$

and using (A.15) one arrives at

$$I_{BW} = \left(\frac{\ln 2}{1-m}\right) \cdot f_s \cdot V_{GST} \cdot DR\,[\text{bits}] \cdot C_{Lac} \tag{A.21}$$

The current needed for slewing is then

$$I_{SR} = \left(\frac{2}{m}\right) \cdot k \cdot \beta \cdot V_{REF} \cdot f_s \cdot C_{Lac} \tag{A.22}$$

Equating equations (A.21) and (A.22), and solving for m yields

$$m = \frac{1}{1 + \frac{\ln 2}{2} \cdot \left(\frac{DR}{k \cdot \beta}\right) \cdot \left(\frac{V_{GST}}{V_{REF}}\right)} \tag{A.23}$$

The sensitivities of I_{BW} and I_{SR} relative to m can be determined to be

$$S_m^{I_{BW}} = \frac{m}{I_{BW}} \cdot \frac{dI_{BW}}{dm} = \frac{m}{1-m} \tag{A.24}$$

and

$$S_m^{I_{SR}} = \frac{m}{I_{SR}} \cdot \frac{dI_{SR}}{dm} = -1 \tag{A.25}$$

For small m, $S_m^{I_{BW}} \cong m$, therefore I_{BW} is very insensitive to variations in this parameter. However, I_{SR} follows any variations in m (with opposite sign).

APPENDIX B: MODELING OF A FULLY-DIFFERENTIAL SC INTEGRATOR

In this Appendix we present a model for a fully-differential switched-capacitor integrator. The model includes the finite dc gain of the amplifier, a 1-pole frequency behavior, limited slew-rate, offset voltage and common-mode rejection ratio (CMRR), noise sources such as *kT/C* noise, op-amp thermal and $1/f$ noise, and clock charge injection. Chopper stabilization is modelled as well.

B.1 BASIC OP-AMP MODEL

Figure B.1 shows a basic model of fully-differential amplifier, where the features modelled are the dc gain and the output common-mode voltage. It is assumed that the two sides of the amplifier may be mismatched, hence we need two different gains. The equations which describe the behavior of the amplifier are

$$\begin{aligned} \Delta V &= e^{+} - e^{-} \\ V_{op} &= V_{cmo} + A_1 \cdot \Delta V \\ V_{on} &= V_{cmo} - A_2 \cdot \Delta V \\ V_{op} - V_{on} &= (A_1 + A_2) \cdot \Delta V \end{aligned} \tag{B.1}$$

B.2 OFFSET VOLTAGE AND CMRR

To model the offset voltage V_{os} in a differential structure, we can split the former into two contributions with equal values and opposite signs, as shown in Figure B.2. The common-mode rejection ratio refers to the capability of rejecting signals which are not differential. Since it is defined as the ratio of the differential gain to the common-mode

gain [10], the common-mode component has to be divided by CMRR. The equations which describe these mechanisms are the following:

$$
\begin{aligned}
V_x &= V_{cm} - \frac{\Delta V}{2} \\
V_y &= V_{cm} + \frac{\Delta V}{2} \\
V &= \left(V_y + \frac{1/2 \cdot V_y}{CMRR} + \frac{V_{os}}{2} \right) - \left(V_x - \frac{1/2 \cdot V_x}{CMRR} - \frac{V_{os}}{2} \right) = \Delta V + \frac{V_{cm}}{CMRR} + V_{os} \\
V_{op} - V_{on} &= (A_1 + A_2) \cdot V
\end{aligned}
\tag{B.2}
$$

Note that the input signal is $V_x - V_y$, and it contains both common-mode and differential components.

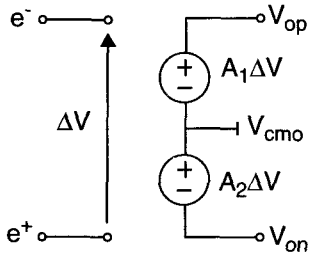

Figure B.1: Basic model of a fully-differential op-amp with finite dc gain.

B.3 OP-AMP NOISE

The thermal noise of the amplifier is modelled based on the expression of the noise *PSD* of an MOS device in saturation: $S(f) = 8kT/(3g_m)$. Given the bandwidth, the noise power P_N can be easily calculated. The corresponding noise signal can be

approximated by generating a random function with a Gaussian distribution N(0,1), which is multiplied by $\sqrt{P_N}$. The new sequence converges stochastically to N(0,P_N).

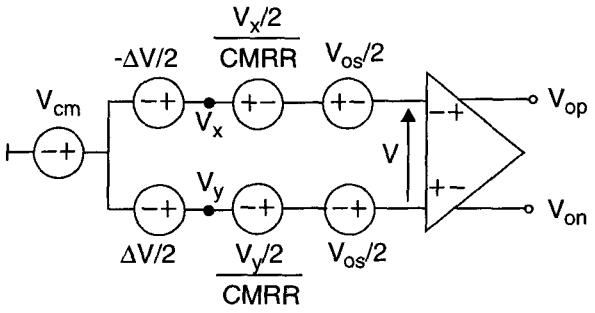

Figure B.2: Modeling of the op-amp dc offset voltage and common-mode rejection ratio (*CMRR*).

To simulate the effect of flicker noise, a common empirical expression for the power spectral density for this type of noise in MOS devices is used:

$$S_{xx}(f) = \frac{KF}{C_{OX} \cdot W \cdot L} \cdot \frac{1}{f^{AF}} \tag{B.3}$$

where KF and AF are process- and device-type-dependent parameters, f is the frequency, C_{OX} the oxide unit capacitance, and W and L the effective width and length of the MOS transistor, respectively. Assuming that the noise signal with *PSD* given by (B.3) results from filtering a white noise sequence N(0,1), the filter impulse response is given by

$$|H(f)| = [S_{xx}(f)]^{1/2} \tag{B.4}$$

As an example, consider a signal band and a sampling frequency such that $OSR = 64$. This results in 128 frequency points in the given bandwidth. We then build an FIR filter with 128 taps and impulse response given by (B.4), and use it to filter a pseudo-random sequence with distribution N(0,1). The power spectral density of the filtered sequence can be estimated using a simple periodogram:

$$PSD \approx \frac{|FFT(f)|^2}{M} \tag{B.5}$$

where M is the number of samples in the time sequence. Note that using a periodogram is a somewhat less accurate approach, since it is a biased estimator of the *PSD*. Figure B.3 shows the generated pseudo-random white noise sequence and its filtered version. Also shown are the impulse response of the FIR filter, (B.4), and the resulting periodogram which is compared with $S_{yy}(f)$. The number of samples used was $M = 1024$.

In the simulation, the samples of thermal and flicker noise thus generated are added to the differential dc offset of the amplifier.

B.4 *kT/C* NOISE

The *kT/C* noise with origin in the MOS switches ON resistance is generated in the same manner as white noise in the op-amp. The white noise sequence with distribution N(0,1) is now multiplied by $\sqrt{2 \cdot kT/C}$, where C is the value of the switched capacitor. Each sample of noise is added to a sample of the input signal.

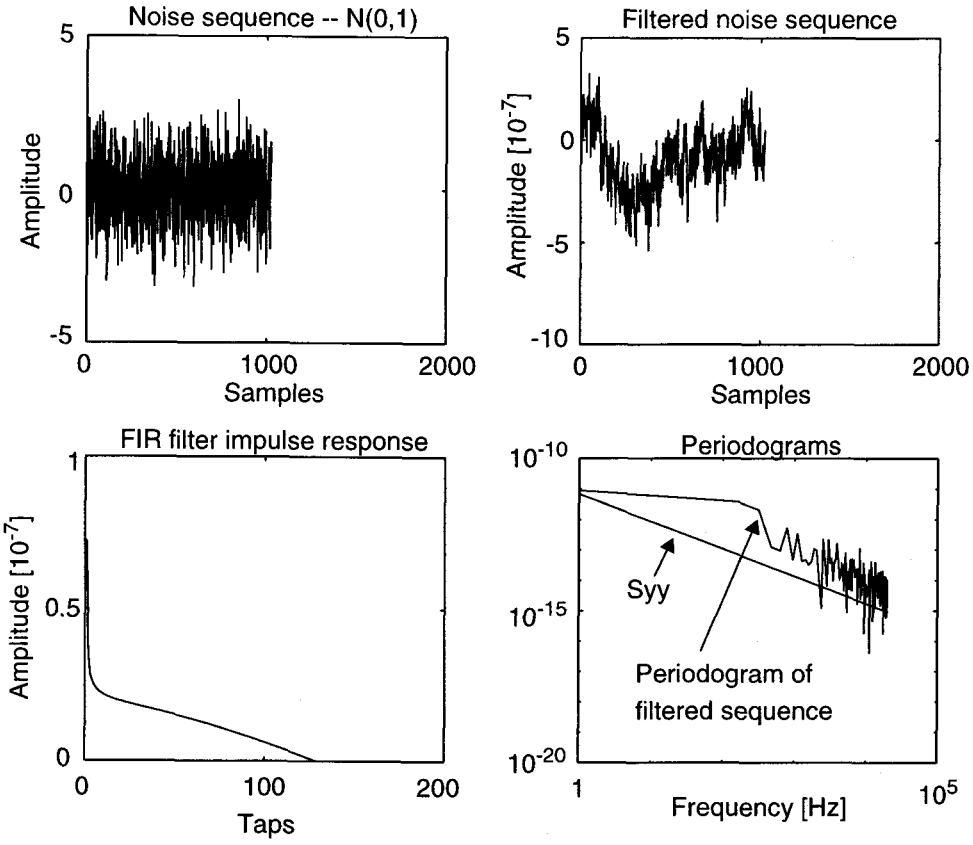

Figure B.3: Generation of a noise time signal for simulation of flicker noise, from a filtered pseudo-random white noise sequence.

B.5 CLOCK CHARGE INJECTION

Two scenarios are possible: slow and fast switching. In the case of slow switching (Figure B.4a), the charge injection component is dominated by the overlap parasitic gate-drain capacitances C_{gd}, since the charge stored under the channel is absorbed by the input signal source (if the impedance of the signal source is much lower than that of C). The turning point occurs when the gate voltage V_G equals

$$V_G = V_{in} + V_T \tag{B.6}$$

point at which the device turns off. Applying the charge conservation law (see Figure B.4c), one concludes that the residual voltage across the sampling capacitor C due to charge injection is

$$\Delta V_C = V - V_{in} = -\frac{C_{gd}}{C_{gd} + C} \cdot (V_{in} + V_T) \tag{B.7}$$

Note that this injection of charge occurs <u>after</u> the transistor is OFF ($V_G < V_{in} + V_T$), and is due only to the overlap capacitance.

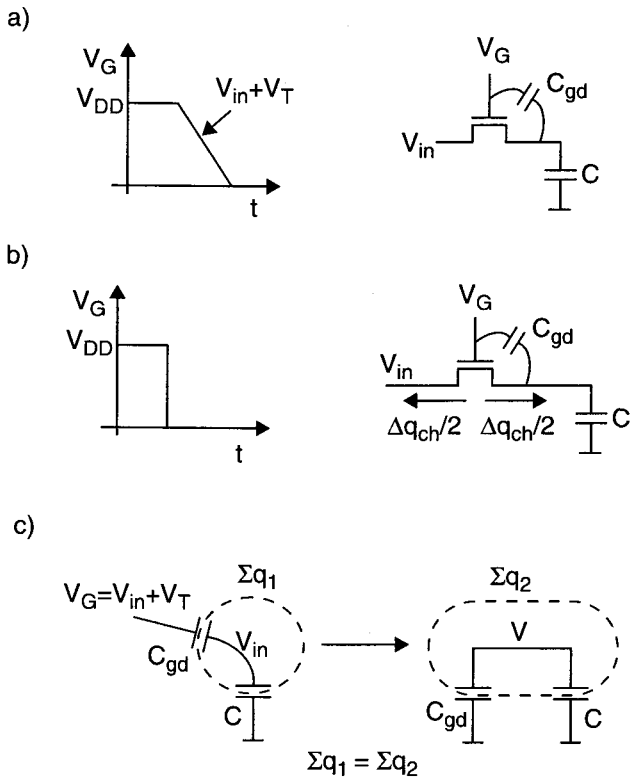

Figure B.4: Modeling of the clock charge injection. a) Slow-switching mode. b) Fast-switching mode. c) Charge conservation principle.

In the case of fast switching, Figure B.4b, the charge under the channel is not absorbed by the input signal source, and hence part of it is injected onto the sampling capacitor C. The amount which is actually stored in the capacitor C is a function of the impedances looking from the drain and source of the MOS switch. If these impedances are equal, then half of the charge under the channel is absorbed by the input signal source, and the other half is injected onto capacitor C. Assuming that this is indeed the case, one can easily arrive at the following result for the channel charge injection onto capacitor C:

$$\Delta q_{ch} = -\frac{W \cdot L \cdot COX \cdot (V_{DD} - V_{in} - V_T)}{2} \tag{B.8}$$

Adding the contributions from the overlap capacitance and channel charge one arrives the following result for the total residual voltage across capacitor C:

$$\Delta V_C = -\frac{W \cdot L \cdot COX \cdot (V_{DD} - V_{in} - V_T)}{2 \cdot (C_{gd} + C)} - \frac{C_{gd}}{C_{gd} + C} \cdot (V_{in} + V_T) \tag{B.9}$$

Note that V_T is a nonlinear function of the input signal [10]:

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{V_{in} + \phi_s} - \sqrt{\phi_s} \right) \tag{B.10}$$

Fast switching is more practical, and hence will be the one used in the development of this model.

(An estimate of the lower bound for the residual voltage ΔV_c due to the channel charge is given in [69]. This bound was determined for a SC integrator, and is only a function of the switch channel length, the carrier mobility and the time constant of the integrator.)

B.6 SWITCHED-CAPACITOR INTEGRATORS

Figure B.5 shows the diagram of a generalized fully-differential SC integrator. It contains an arbitrary number of inverting and non-inverting input branches (the superscripts *u* and *l* refer to *upper* and *lower* SC branches, respectively). Switches implementing chopper stabilization and the appropriate timing are shown as well. We now present the equations describing the behavior of this circuit in all phases of operation.

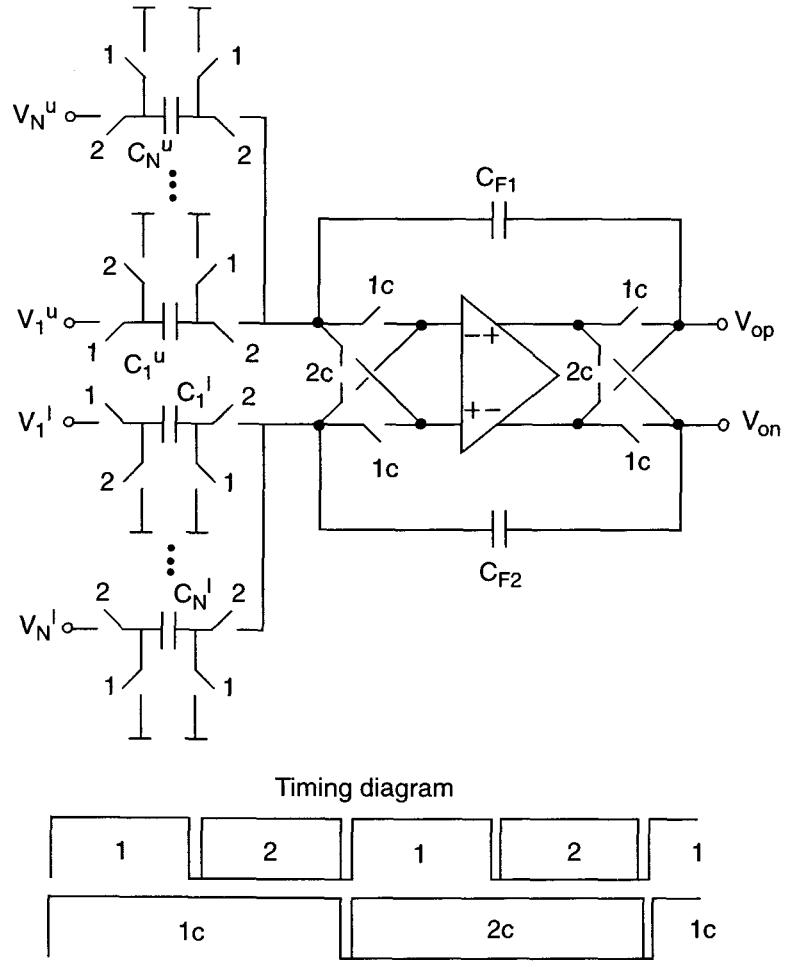

Figure B.5: Circuit diagram of a generalized fully-differential switched-capacitor integrator with chopper stabilization.

For the purpose of simulation, it is convenient to develop a structure characterizing each input SC branch. The entries in such structure for SC branch are the nominal capacitance value C, the associated bottom plate capacitance C_b, the voltage applied to C in phase #1 -- V_1, the voltage applied to C in phase #2 -- V_2, the voltage across C at the end of phase #1 -- $V_C(n-1)$, and a random number *rand* which will be used to generate a sample of kT/C noise.

Figure B.6a shows a non-inverting and an inverting SC branch during phase #1. In this phase the inverting branches sample an input voltage V_{in}, and the non-inverting branches are shorted to analog ground V_{AGND}. Figure B.6b shows the configuration seen when switch S1 opens. As can be seen from this Figure, the right-hand side of both branches is always connected to the same voltage -- analog ground. Only the node voltage V_x (phase #1) differs. This allows us to use a single structure to manipulate both types of branches, without explicit reference to their type. In this Figure, V_x equals V_{AGND} for a non-inverting branch and V_{in} for an inverting one. The charge packets $\Delta q_{1,2}$ represent the charge injection from the channel, as given by (B.8). One can then write the following relations:

$$\begin{aligned}\Delta q_1 = {} & (C_{gd}+C_b)\cdot V_1 + C\cdot(V_1-V_2) + C_{gd}\cdot(V_{DD}-V_x) \\ & - C_b\cdot V_x - C\cdot(V_x-V_{AGND})\end{aligned} \tag{B.11a}$$

$$\begin{aligned}\Delta q_2 = {} & C_{gd}\cdot V_2 + C\cdot(V_2-V_1) + C\cdot(V_x-V_{AGND}) \\ & - C_{gd}\cdot(V_{AGND}-V_{DD})\end{aligned} \tag{B.11b}$$

Collecting the terms in V_1 and V_2 one obtains the following system:

$$\begin{bmatrix} C_{gd}+C_b+C & -C \\ -C & C_{gd}+C_b \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \tag{B.12}$$

$$\begin{bmatrix} \Delta q_1 + (C_{gd}+C_b+C)\cdot V_x - C_{gd}\cdot V_{DD} - C\cdot V_{AGND} \\ \Delta q_2 + (C+C_{gd})\cdot V_{AGND} - C\cdot V_x - C_{gd}\cdot V_{DD} \end{bmatrix}$$

where the channel charge injection components are given by

$$\begin{aligned} \Delta q_1 &= -\frac{1}{2}\cdot W\cdot L\cdot COX\cdot (V_{DD}-V_x-V_{T1}) \\ V_{T1} &= V_{T0}+\gamma\cdot\left(\sqrt{V_x+\phi_s}-\sqrt{\phi_s}\right) \\ \Delta q_2 &= -\frac{1}{2}\cdot W\cdot L\cdot COX\cdot (V_{DD}-V_{AGND}-V_{T2}) \\ V_{T2} &= V_{T0}+\gamma\cdot\left(\sqrt{V_{AGND}+\phi_s}-\sqrt{\phi_s}\right) \end{aligned} \tag{B.13}$$

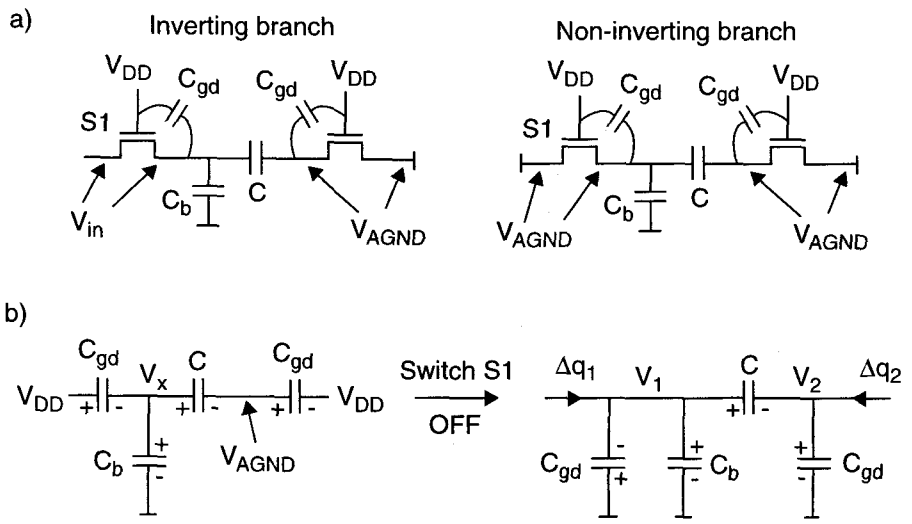

Figure B.6: a) Inverting and non-inverting SC branches during phase #1. b) Branch configuration for charge injection when switch S1 opens.

The voltage across the capacitor, and stored in the structure described above, is then

$$V_C(n-1) = V_1 - V_2 + rand \cdot \sqrt{\frac{2 \cdot kT}{C}} \tag{B.14}$$

It is interesting to analyze the effect of the bottom plate capacitance C_b on the charge injection. Assume that $\Delta q_{1,2} = 0$. If $C_b = 0$, the overlap capacitances do not contribute any residual charge due to the symmetry of the structure. As C_b is made very large, the node to which it is connected (the bottom plate of the capacitor) behaves as an ac ground for fast-switching signals. Therefore, only the overlap capacitance of the right-most switch contributes with charge injection. The following relation for the voltage across the capacitor C holds:

$$V_C = \frac{C}{C + C_{gd}} \cdot V_{in} + \frac{C_{gd}}{C_{gd} + C} \cdot V_{DD} \tag{B.15}$$

This expression permits us to relate the size of the MOS switch to power supply rejection; clearly, the switch dimensions should always be minimized.

Note, however, that the overlap capacitance connected to the virtual ground does contribute a residual charge, which is injected into the integrating capacitor. This charge injection is frequently found accountable for significant source of error.

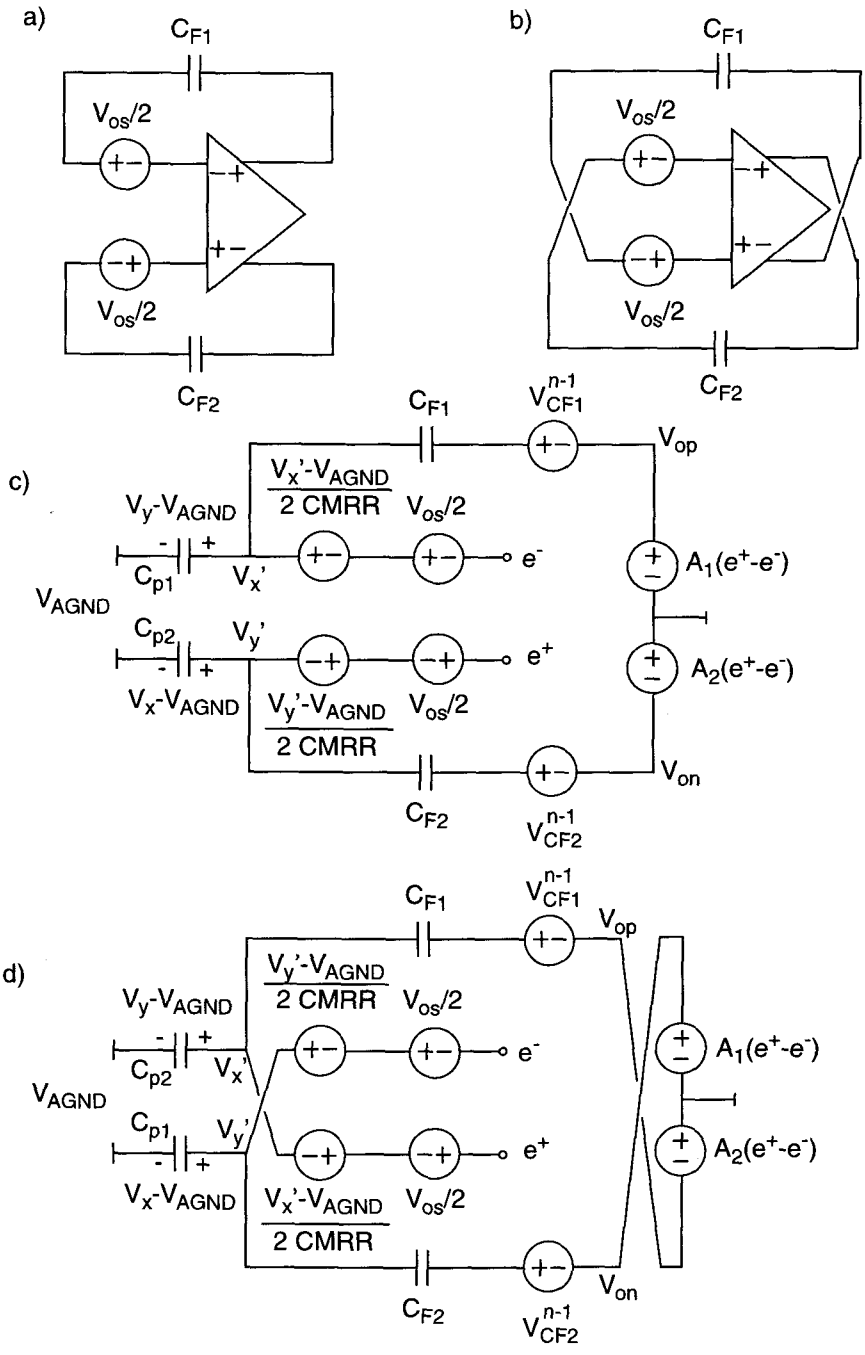

Figure B.7: Possible configurations when chopper stabilization is used. a) Configuration #1. b) Configuration #2. c) Model to update node voltages in configuration #1. d) Model to update node voltages in configuration #2.

In phase #2 we have to determine whether chopper stabilization is being used or not. This creates two possible configurations, which alternate when chopper stabilization is being used. Figures B.7a and B.7b show such configurations. Before charge transfer from the input SC branches can take place, it is necessary to update the node voltages resulting from switching between configurations, as charge redistribution takes place. In configuration #1, Figure B.7c, the following equations hold:

$$e^+ - e^- = V_{os} + \left(1 + \frac{1/2}{CMRR}\right) \cdot V'_y - \left(1 - \frac{1/2}{CMRR}\right) \cdot V'_x - \frac{V_{AGND}}{CMRR} \tag{B.16a}$$

$$\begin{bmatrix} C_{p1} + C_{F1}\left[1 + A_1\left(1 - \frac{1/2}{CMRR}\right)\right] & -C_{F1}A_1\left(1 + \frac{1/2}{CMRR}\right) \\ -C_{F2}A_2\left(1 - \frac{1/2}{CMRR}\right) & C_{p2} + C_{F2}\left[1 + A_2\left(1 + \frac{1/2}{CMRR}\right)\right] \end{bmatrix} \cdot \begin{bmatrix} V'_x \\ V'_y \end{bmatrix} =$$

$$\begin{bmatrix} C_{p1} \cdot V_y - C_{F1}\left[-A_1 \cdot V_{os} - V_{AGND} - V_{CF1}^{n-1}\right] - C_{F1}A_1\frac{V_{AGND}}{CMRR} \\ C_{p2} \cdot V_x - C_{F2}\left[-A_2 \cdot V_{os} - V_{AGND} - V_{CF2}^{n-1}\right] + C_{F2}A_2\frac{V_{AGND}}{CMRR} \end{bmatrix} \tag{B.16b}$$

where V'_y and V'_x denote the updated V_y and V_x node voltages, and V_{Ci}^{n-1} denotes the voltage previously stored in capacitor C_i. The new voltages across the feedback capacitors are

$$V'_{CF1} = V'_x - A_1 \cdot \left(e^+ - e^-\right) - V_{AGND} \tag{B.17a}$$

$$V'_{CF2} = V'_y + A_2 \cdot \left(e^+ - e^-\right) - V_{AGND} \tag{B.17b}$$

Similarly, the equations for configuration #2 (Figure B.7d) are as follows:

$$e^+ - e^- = V_{os} + \left(1 + \frac{1/2}{CMRR}\right) \cdot V'_x - \left(1 - \frac{1/2}{CMRR}\right) \cdot V'_y - \frac{V_{AGND}}{CMRR} \tag{B.18a}$$

$$\begin{bmatrix} C_{p2}+C_{F1}\left[1+A_2\left(1-\frac{1/2}{CMRR}\right)\right] & -C_{F1}A_2\left(1-\frac{1/2}{CMRR}\right) \\ -C_{F2}A_1\left(1-\frac{1/2}{CMRR}\right) & C_{p1}+C_{F2}\left[1+A_1\left(1-\frac{1/2}{CMRR}\right)\right] \end{bmatrix} \cdot \begin{bmatrix} V_x \\ V_y \end{bmatrix} =$$

$$\begin{bmatrix} C_{p2}\cdot V_y - C_{F1}\left[A_2\cdot V_{os} - V_{AGND} - V_{CF1}^{n-1}\right] + C_{F1}A_2\frac{V_{AGND}}{CMRR} \\ C_{p1}\cdot V_x + -C_{F2}\left[-A_1\cdot V_{os} - V_{AGND} - V_{CF2}^{n-1}\right] - C_{F2}A_1\frac{V_{AGND}}{CMRR} \end{bmatrix} \quad \text{(B.18b)}$$

Once the node voltages have been updated, the input SC branches can be connected to the inputs of the op-amp to determine the new output voltage. This defines phase #2. Figure B.8 shows the corresponding diagram for both configurations. For configuration #1, the charge transfer process is described by the following equations:

$$\begin{aligned} \Delta q_u &= \sum_{k=1}^{N} C^u{}_k \cdot \left[V_{2k}^u - V_x - V_{Ck}^u(n-1)\right] \\ &= C_{p1}\cdot\left(V_x - V_{AGND} - V_{Cp1}^{n-1}\right) \\ &\quad + C^u{}_F \cdot \left[V_x - A_1\cdot\left(e^+ - e^-\right) - V_{AGND} - V_{CF1}^{n-1}(n-1)\right] \end{aligned} \quad \text{(B.19a)}$$

$$\begin{aligned} \Delta q_l &= \sum_{k=1}^{N} C^l{}_k \cdot \left[V^l{}_{2k} - V_y - V^l{}_{Ck}(n-1)\right] \\ &= C_{p2}\cdot\left(V_y - V_{AGND} - V_{Cp2}^{n-1}\right) \\ &\quad + C^l{}_F \cdot \left[V_y + A_2\cdot\left(e^+ - e^-\right) - V_{AGND} - V_{CF2}^{n-1}(n-1)\right] \end{aligned} \quad \text{(B.19b)}$$

$$e^+ - e^- = V_{os} + \left(1+\frac{1/2}{CMRR}\right)\cdot V_y - \left(1-\frac{1/2}{CMRR}\right)\cdot V_x - \frac{V_{AGND}}{CMRR} \quad \text{(B.19c)}$$

where N is the number of upper/lower input SC branches, and $V_{Ci}^{u,l}$ denotes the voltage across capacitor C_i in the upper -- u -- or lower -- l -- branch.

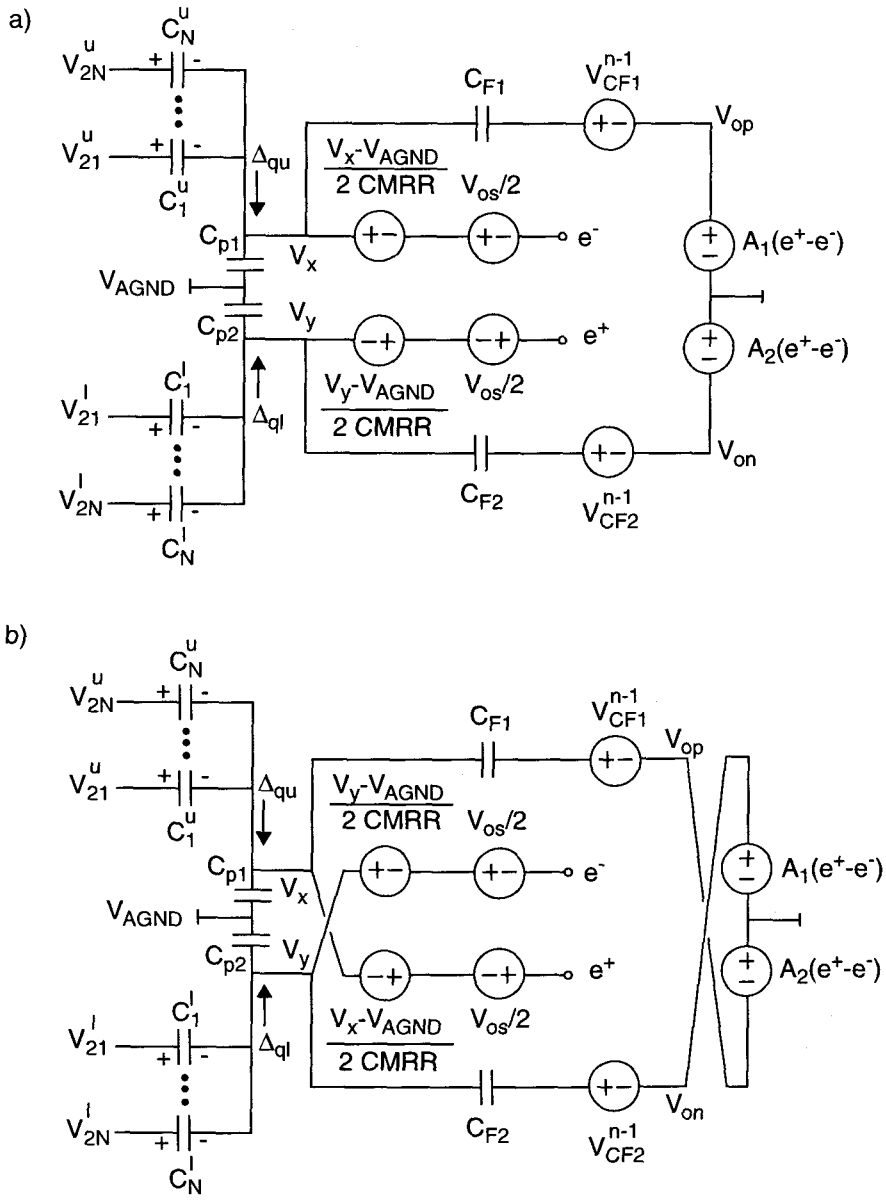

Figure B.8: Model for charge transfer from the input branches to the integrating capacitors in phase #2. a) Configuration #1. b) Configuration #2.

Similarly, one obtains the following relations for configuration #2:

$$\begin{aligned}\Delta q_u &= \sum_{k=1}^{N} C^u{}_k \cdot \left[V^u{}_{2k} - V_x - V^u{}_{Ck}(n-1) \right] \\ &= C_{p2} \cdot \left(V_x - V_{AGND} - V_{Cp2}^{n-1} \right) \\ &\quad + C^u{}_F \cdot \left[V_x + A_2 \cdot \left(e^+ - e^- \right) - V_{AGND} - V^u_{CF}(n-1) \right]\end{aligned} \tag{B.20a}$$

$$\begin{aligned}\Delta q_l &= \sum_{k=1}^{N} C^l{}_k \cdot \left[V^l{}_{2k} - V_y - V^l{}_{Ck}(n-1) \right] \\ &= C_{p1} \cdot \left(V_y - V_{AGND} - V_{Cp1}^{n-1} \right) \\ &\quad + C^l{}_F \cdot \left[V_y - A_1 \cdot \left(e^+ - e^- \right) - V_{AGND} - V^l_{CF}(n-1) \right]\end{aligned} \tag{B.20b}$$

$$e^+ - e^- = V_{os} + \left(1 + \frac{1/2}{CMRR} \right) \cdot V_x - \left(1 - \frac{1/2}{CMRR} \right) \cdot V_y - \frac{V_{AGND}}{CMRR} \tag{B.20c}$$

Equations (B.19) and (B.20) can now be solved for V_x and V_y to obtain the output voltages V_{op} and V_{on}. The difference between the new output voltages and the old ones defines a step voltage $V_{step} = V_o(n) - V_o(n-1)$ from which we can determine whether or not the amplifier is slewing. Note that in deriving equations (B.16) through (B.20) it was assumed that chopper stabilization was being used, and hence configurations #1 and #2 alternated. If this is not the case, then configuration #1 is used all the time and there is no need to update the node voltages in the beginning of phase #2 -- equations (B.16) and (B.18).

At the end of phase #2, clock charge injection occurs as well and must be accounted for. Figure B.9 shows the circuit diagram corresponding to configurations #1 and #2. It is assumed that all the devices have the same gate-drain overlap capacitance value C_{gd}. In such case the total charge with origin in these parasitic capacitances is $N \cdot C_{gd}$. The same consideration applies to the charge with origin under the channel of the MOS switches.

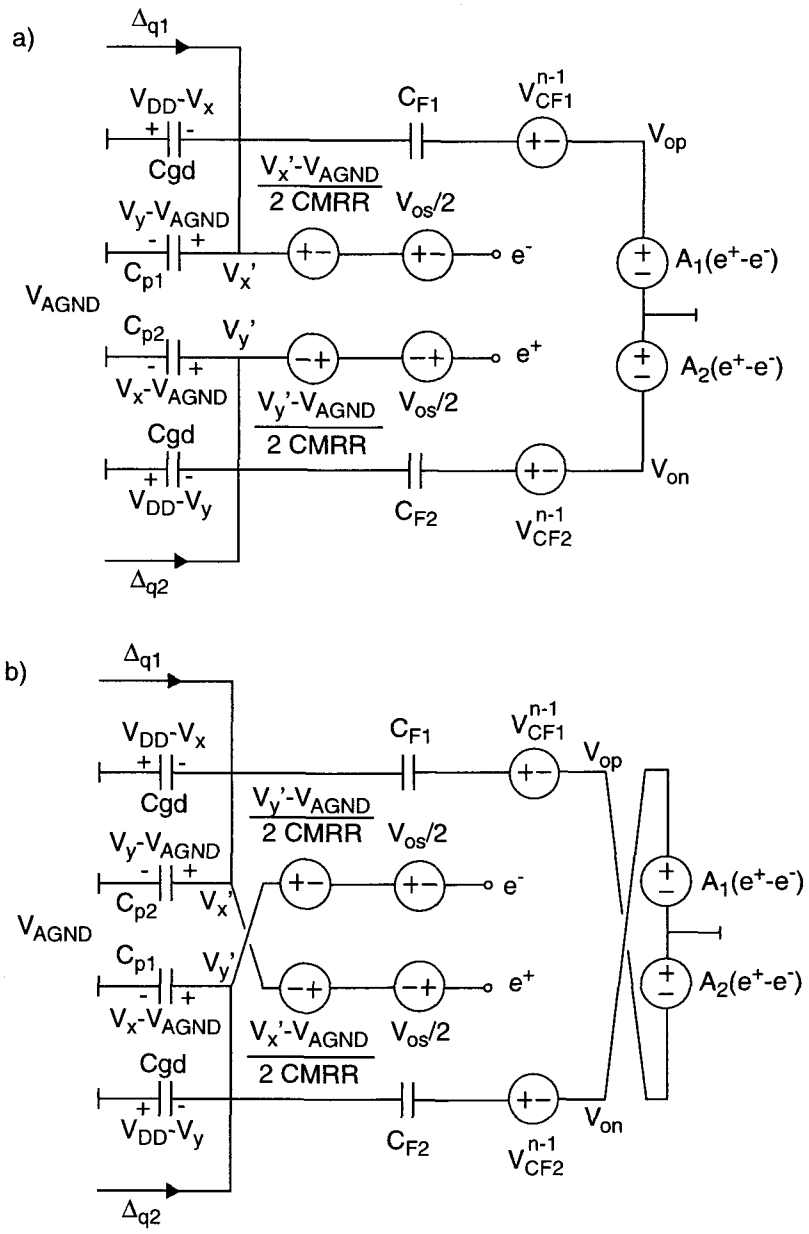

Figure B.9: Model for clock charge injection in the end of phase #2. a) Configuration #1. b) Configuration #2.

The equations describing the charge injection in both configurations assume the previous form of a two-equation system:

$$\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \cdot \begin{bmatrix} V_x \\ V_y \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \tag{B.21}$$

For configuration #1 the matrix entries are as follows

$$\begin{aligned}
a_{11} &= N \cdot C_{gd} + C_{p1} + C_{F1}\left[1 + A_1\left(1 - \frac{1/2}{CMRR}\right)\right] \\
a_{12} &= -C_{F1}A_1\left(1 + \frac{1/2}{CMRR}\right) \\
a_{21} &= -C_{F2}A_2\left(1 - \frac{1/2}{CMRR}\right) \\
a_{22} &= N \cdot C_{gd} + C_{p2} + C_{F2}\left[1 + A_2\left(1 + \frac{1/2}{CMRR}\right)\right] \\
b_1 &= N \cdot [\Delta q_1 + C_{gd} \cdot (V_x - V_{DD})] + C_{p1} \cdot V_x - C_{F1}A_1\frac{V_{AGND}}{CMRR} \\
&\quad + C_{F1} \cdot \left(A_1 \cdot V_{os} + V_{AGND} + V_{CF1}^{n-1}\right) \\
b_2 &= N \cdot [\Delta q_2 + C_{gd} \cdot (V_y - V_{DD})] + C_{p2} \cdot V_y + C_{F2}A_2\frac{V_{AGND}}{CMRR} \\
&\quad + C_{F2} \cdot \left(A_2 \cdot V_{os} + V_{AGND} + V_{CF2}^{n-1}\right)
\end{aligned} \tag{B.22}$$

Analogously, the matrix entries for configuration #2 are given by

$$\begin{aligned}
a_{11} &= N \cdot C_{gd} + C_{p2} + C_{F1}\left[1 + A_2\left(1 + \frac{1/2}{CMRR}\right)\right] \\
a_{12} &= -C_{F1}A_2\left(1 - \frac{1/2}{CMRR}\right) \\
a_{21} &= -C_{F2}A_1\left(1 + \frac{1/2}{CMRR}\right) \\
a_{22} &= N \cdot C_{gd} + C_{p1} + C_{F2}\left[1 + A_1\left(1 - \frac{1/2}{CMRR}\right)\right] \\
b_1 &= N \cdot [\Delta q_1 + C_{gd} \cdot (V_x - V_{DD})] + C_{p2} \cdot V_x + C_{F1}A_2\frac{V_{AGND}}{CMRR} \\
&\quad + C_{F1} \cdot \left(-A_2 \cdot V_{os} + V_{AGND} + V_{CF1}^{n-1}\right)
\end{aligned}$$

$$b_2 = N \cdot [\Delta q_2 + C_{gd} \cdot (V_y - V_{DD})] + C_{p1} \cdot V_y + C_{F2} A_1 \frac{V_{AGND}}{CMRR} + C_{F2} \cdot \left(A_1 \cdot V_{os} + V_{AGND} + V_{CF2}^{n-1} \right) \quad \text{(B.23)}$$

B.7 OP-AMP AC AND SLEWING MODEL

The op-amp is modelled with a 1-pole transfer function:

$$A(\omega) = \frac{A_0 \cdot p_1}{s + p_1} \quad \text{(B.24)}$$

where A_0 is the dc gain of the amplifier and p_1 the angular frequency of the dominant pole. We can identify three modes of operation for such amplifier: one in which only slewing occurs (very large steps), an other in which only linear settling occurs (small steps), and a third one in which both slewing and settling occur. In the presence of only linear settling behavior, the output tends exponentially to its final value according to

$$V_o(n) = V_o(n-1) + V_{step} \cdot \left[1 - \exp\left(-\frac{T_S}{2 \cdot \tau} \right) \right] \quad \text{(B.25)}$$

where τ is the time constant of the amplifier, therefore given by $\tau = \beta / (A_0 \cdot p_1)$, and $T_S/2$ the time period available for settling (half of the clock period). (β is the feedback coefficient, as the time constant is determined by the closed-loop bandwidth.) When only slewing occurs, the output of the amplifier evolves linearly according to

$$V_o(n) = V_o(n-1) \pm SR \cdot \frac{T_S}{2} \quad \text{(B.26)}$$

where SR is the slew-rate of the amplifier in V/s. Note that the actual final value is independent of V_{step}, therefore slewing results in distortion. Amplifier saturation will occur if the value in (B.26) exceeds V_{DD} or reaches 0 V. When both slewing and linear settling occur, the step response is characterized by the two regions of operation described by (B.25) and (B.26). For $t < t_s$, Figure B.10, the op-amp is in the slewing mode, and thereafter in linear settling mode. To derive a closed-form expression describing both regions of operation one must impose continuity of the two functions and of their derivatives at $t = t_s$. The two functions are the following:

$$V_o(t) = SR \cdot t, \quad t \leq t_s \tag{B.27a}$$

$$V_o(t) = [V_{step} - V_s] \cdot \left[1 - \exp\left(-\frac{t - t_s}{\tau}\right)\right] + V_s, \quad t \geq t_s \tag{B.27b}$$

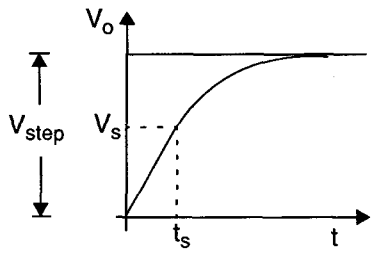

Figure B.10: Transient response of an amplifier to a step voltage, showing slewing behavior ($t < t_s$) and linear settling behavior $t > t_s$.

Considering that $V_s = SR \cdot t_s$ one can immediately conclude that (B.27a) and (B27.b) are indeed continuous at $t = t_s$. Equating the derivatives of both functions one arrives at the following result:

$$t_s = \frac{V_{step}}{SR} - \tau \tag{B.28}$$

If slewing is to occur, t_s must be positive, in other words,

$$V_{step} > \tau \cdot SR \tag{B.29}$$

However, since t_s cannot exceed half of the clock cycle, the condition required to have slewing and linear settling modes simultaneously is

$$V_{step} < \left(\tau + \frac{T_S}{2}\right) \cdot SR \tag{B.30}$$

Using this result in (B.27b) one finally arrives at the following relation describing the coexistence of both modes:

$$V_o(n) = V_o(n-1) + V_{step} \pm \tau \cdot SR \cdot \exp\left(\frac{|V_{step}|}{\tau \cdot SR} - 1 - \frac{T_S}{2 \cdot \tau}\right) \tag{B.31}$$

Note that equations (B.25), (B.26) and (B.31) give the op-amp output voltage at the end of the clock phase. Since this value may not be equal to V_{step}, the op-amp input node voltages need to be updated accordingly, to reflect incomplete or nonlinear settling.

APPENDIX C: OPERATION AND VOLTAGE EFFICIENCY OF A VOLTAGE DOUBLER

In this appendix we analyze the operation and voltage efficiency of the clock bootstrapping circuit described in Chapter 4.

C.1 OPERATION

Figure C.1a shows the voltage doubler in Figure 4.3, with all the parasitic node capacitances C_{pi}. It consists of two voltage doublers, one composed of capacitor C_1 and device M1, and the other of capacitor C_2 and device M2. If CLK is "high," the gate of M1 is raised to a voltage close to $2 \cdot V_{DD}$ (after a short transient). Since this gate voltage exceeds $V_{DD} - V_T$, the source of M1 can rise to V_{DD}, while still maintaining the device in strong inversion. When CLK switches to "low," the top plate of C_1 rises to a voltage close to twice V_{DD}, as now M1 is turned OFF. This high voltage at the gate of M2 allows the top plate of C_2 to be charged to V_{DD}, as with C_1. Hence, the two voltage doublers operate in conjunction to overcome the limitation of the threshold voltage of switches M1 and M2.

C.2 VOLTAGE EFFICIENCY

Clearly, since the CMOS inverters act as voltage sources, the capacitances C_{p1} and C_{p2} play no role in the voltage efficiency of this circuit. Assuming that C_{p3} is negligible compared to C_1, the voltage at the gate of M2 will approach $2 \cdot V_{DD}$ sufficiently to allow the formation of a channel in M2. Therefore the voltage efficiency of this circuit should be determined only by capacitors C_2, C_{p4} and C_p.

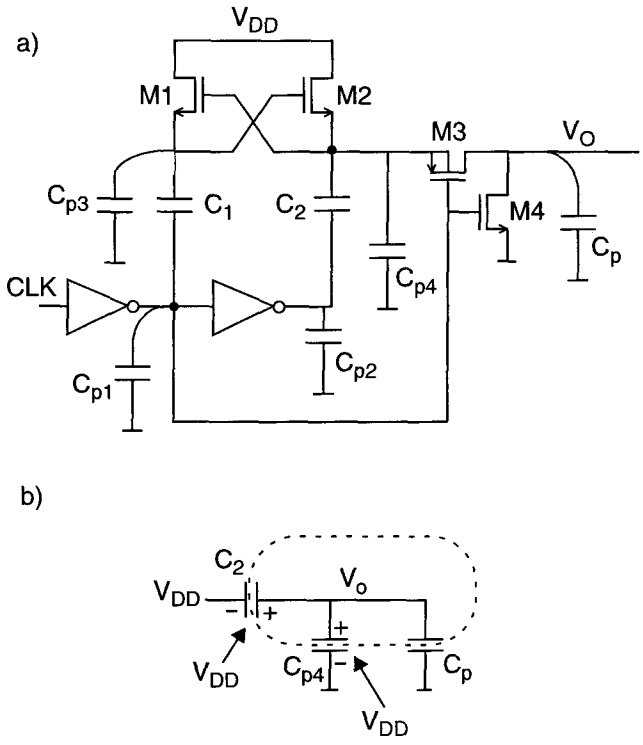

Figure C.1: Voltage doubler. a) Circuit diagram, with indication of the parasitic capacitances. b) Right-hand side circuit configuration when CLK is "high."

Figure C.1b shows the equivalent circuit when CLK is "high." In this figure, initially C_p is discharged (due to M4 being ON when CLK is "low"), and C_2 and C_{p4} are charged to V_{DD}. Ideally, when CLK goes "high," the top plate of capacitor C_2 would be floating, and hence its voltage would rise to $2 \cdot V_{DD}$. Due to the presence of the load capacitance C_p and of the parasitic capacitance C_{p4}, charge redistribution occurs which results in some reduction in the value of the final voltage. This can be easily obtained by applying the charge conservation principle to the Gaussian surface shown. One then obtains

$$C_2 \cdot (V_o - 2 \cdot V_{DD}) + C_p \cdot V_o + C_{p4} \cdot (V_o - V_{DD}) = 0 \tag{C.1}$$

Solving for V_o one obtains

$$V_o = \frac{2 \cdot C_2 + C_{p4}}{C_2 + C_p + C_{p4}} \cdot V_{DD} \tag{C.2}$$

Typically, C_{p4} is negligible compared to C_p, and clearly the latter should be made negligible compared to C_2 for high efficiency.

APPENDIX D: ANALYSIS OF SC INTEGRATORS EMPLOYING CDS TECHNIQUES

In this Appendix we derive the formalism which describes the performance of a Nagaraj integrator and a predictive Nagaraj integrator in terms of gain- and pole-errors.

D.1 THE NAGARAJ INTEGRATOR

Figure D.1 shows a non-inverting Nagaraj integrator, and the circuit configuration during both phases of operation. The amplifier is assumed to have a constant dc gain A. For convenience we introduce the parameter $\mu = 1/A$. We can apply the charge conservation principle to determine the node voltages. Hence, in phase #2 we have

$$\begin{aligned} -C_{in} \cdot \left[V_x(n) + V_{in}\left(n-\frac{1}{2}\right)\right] = \\ C_f \cdot \left[V_x(n) - V_o(n) - V_y\left(n-\frac{1}{2}\right) + V_o\left(n-\frac{1}{2}\right)\right] \end{aligned} \tag{D.1}$$

where

$$V_x(n) = V_{os} - \mu \cdot V_o(n) - V_y\left(n-\frac{1}{2}\right) \tag{D.2}$$

Substituting (D.2) in (D.1) yields

$$\begin{aligned} [1+\mu\cdot(1+k)]\cdot V_o(n) = k\cdot V_{in}\left(n-\frac{1}{2}\right) + \\ [1+\mu\cdot(2+k)]\cdot V_o\left(n-\frac{1}{2}\right) - V_{os} \end{aligned} \tag{D.3}$$

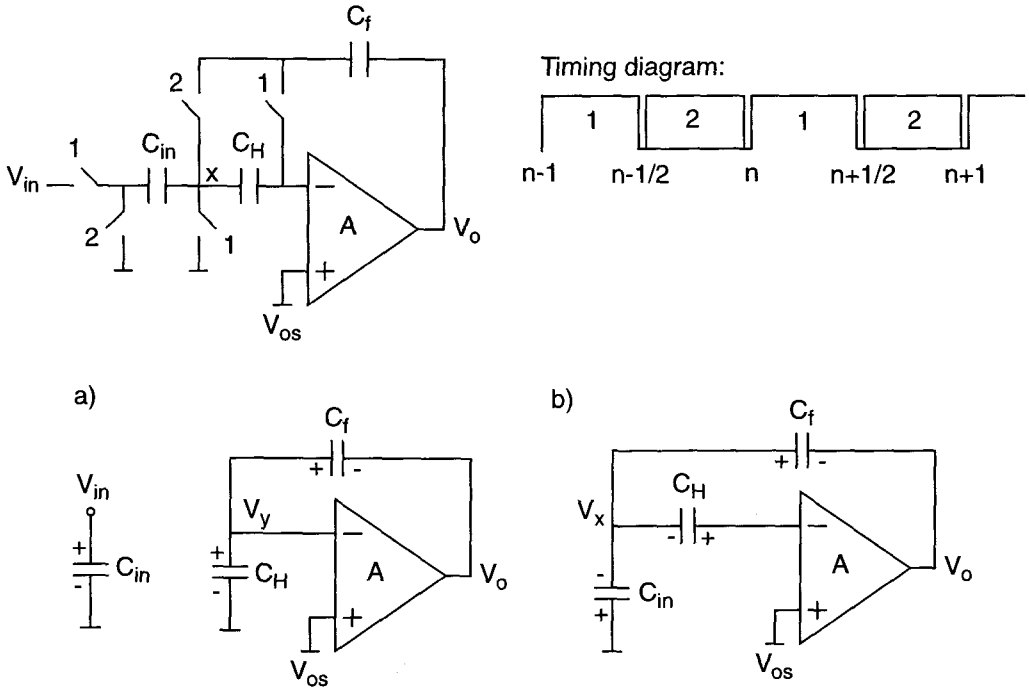

Figure D.1: Nagaraj integrator and timing diagram. a) Configuration during phase #1, for $t = n - 1/2 - \varepsilon$ ($\varepsilon \ll 1$). b) Configuration during phase #2, for $t = n - \varepsilon$.

In phase #1,

$$C_H \cdot \{V_y\left(n+\frac{1}{2}\right) - [V_{os} - \mu \cdot V_o(n) - V_x(n)]\} = \tag{D.4}$$
$$-C_f \cdot \left[V_y\left(n+\frac{1}{2}\right) - V_o\left(n+\frac{1}{2}\right) - V_x(n) + V_o(n)\right]$$

with

$$V_y\left(n-\frac{1}{2}\right) = V_{os} - \mu \cdot V_o\left(n-\frac{1}{2}\right) \tag{D.5}$$

One then obtains

$$[1+\mu\cdot(1+k')]\cdot V_o\left(n+\frac{1}{2}\right) = (1+\mu)\cdot V_o(n) - \mu\cdot(1-k')\cdot V_o\left(n-\frac{1}{2}\right)+V_{os} \tag{D.6}$$

Finally, substituting (D.3) in (D.6) yields for the output voltage in phase #1

$$V_o\left(n+\frac{1}{2}\right) = k\cdot\frac{1+\mu}{[1+\mu\cdot(1+k)]\cdot[1+\mu\cdot(1+k')]}\cdot V_{in}\left(n-\frac{1}{2}\right)+ \frac{(1+\mu)\cdot[1+\mu\cdot(2+k)]-\mu\cdot(1-k')\cdot[1+\mu\cdot(1+k)]}{[1+\mu\cdot(1+k)]\cdot[1+\mu\cdot(1+k')]}\cdot V_o\left(n-\frac{1}{2}\right)+ \frac{\mu\cdot k}{[1+\mu\cdot(1+k)]\cdot[1+\mu\cdot(1+k')]}\cdot V_{os} \tag{D.7}$$

Since $\mu \ll 1$, this expression can be simplified to yield

$$V_o\left(n+\frac{1}{2}\right)\cong k\cdot[1-\mu\cdot(1+k+k')]\cdot V_{in}\left(n-\frac{1}{2}\right) + \left(1-\mu^2\cdot k\right)\cdot V_o\left(n-\frac{1}{2}\right)+\mu\cdot k\cdot V_{os} \tag{D.8}$$

To illustrate the procedure used in the simplification above, let us go through the simplification of the term in $V_o(n-1/2)$:

$$\frac{(1+\mu)\cdot[1+\mu\cdot(2+k)]-\mu\cdot(1-k')\cdot[1+\mu\cdot(1+k)]}{[1+\mu\cdot(1+k)]\cdot[1+\mu\cdot(1+k')]} = \frac{1+\mu\cdot(2+k+k')+\mu^2\cdot(1+k'+k\cdot k')}{1+\mu\cdot(2+k+k')+\mu^2\cdot(1+k+k'+k\cdot k')} = X \tag{D.9}$$

Subtracting the unit from the quantity X one arrives at

$$X-1 = \frac{-\mu^2 \cdot k}{1+\mu \cdot (2+k+k') + \mu^2 \cdot (1+k+k'+k \cdot k')} \cong -\mu^2 \cdot k \qquad \text{(D.10)}$$

Therefore,

$$X \cong 1-\mu^2 \cdot k \qquad \text{(D.11)}$$

Assume now that the gain of the amplifier is not constant, but the input and output voltages relate in a nonlinear manner according to

$$V_o = f(V_{in}) \qquad \text{(D.12)}$$

Equation (D.1) and still applies in phase #2 but now

$$\begin{aligned} V_x(n) &= -\{f^{-1}[V_o(n)] - f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right]\} \\ V_y\left(n-\frac{1}{2}\right) &= V_{os} - f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] \end{aligned} \qquad \text{(D.13)}$$

which results in

$$\begin{aligned} V_o(n) = {} & k \cdot V_{in}\left(n-\frac{1}{2}\right) + V_o\left(n-\frac{1}{2}\right) - \\ & (1+k) \cdot \{f^{-1}[V_o(n)] - \frac{2+k}{1+k} \cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right]\} \end{aligned} \qquad \text{(D.14)}$$

In phase #1 we have

$$V_o\left(n+\frac{1}{2}\right) = V_o(n) + V_{os} + f^{-1}[V_o(n)] - (1-k')\cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] - \left((1+k')\cdot f^{-1}\left[V_o\left(n+\frac{1}{2}\right)\right]\right) \quad \text{(D.15)}$$

Substituting (D.14) in (D.15) one obtains for the output voltage in phase #1

$$V_o\left(n+\frac{1}{2}\right) = k\cdot V_{in}\left(n-\frac{1}{2}\right) + V_o\left(n-\frac{1}{2}\right) - k\cdot f^{-1}[V_o(n)] + (1+k+k')\cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] - (1+k')\cdot f^{-1}\left[V_o\left(n+\frac{1}{2}\right)\right] \quad \text{(D.16)}$$

D.2 THE PREDICTIVE NAGARAJ INTEGRATOR

The procedure to analyze of the predictive Nagaraj integrator is identical to that of the simple Nagaraj integrator, and hence we provide only the main results. Figure D.2 shows such integrator and the circuit configurations corresponding to phases #1 and #2. Again, we start by assuming that the amplifier gain is constant and equal to A. Therefore we have:

$$V_x\left(n-\frac{1}{2}\right) = V_{os} - \mu\cdot V_o\left(n-\frac{1}{2}\right) \quad \text{(D.17)}$$

$$V_y(n) = -\mu\cdot\left[V_o(n) - V_o\left(n-\frac{1}{2}\right)\right] \quad \text{(D.18)}$$

The output voltage in phase #2 is then given by

$$[1+\mu\cdot(1+k_1)]\cdot V_o(n) = k_1\cdot V_{in}\left(n-\frac{1}{2}\right) + (1+\mu)\cdot V_o(n-1) + \mu\cdot(1+k_1)\cdot V_o\left(n-\frac{1}{2}\right) - \mu\cdot V_o\left(n-\frac{3}{2}\right) \quad \text{(D.19)}$$

and that in phase #1 by

$$[1+\mu\cdot(1+k_2+k')]\cdot V_o\left(n-\frac{1}{2}\right) = k_2\cdot V_{in}(n-1)+V_o(n-1)+ \qquad \text{(D.20)}$$
$$\mu\cdot k'\cdot V_o\left(n-\frac{3}{2}\right)+(1+k_2)\cdot V_{os}$$

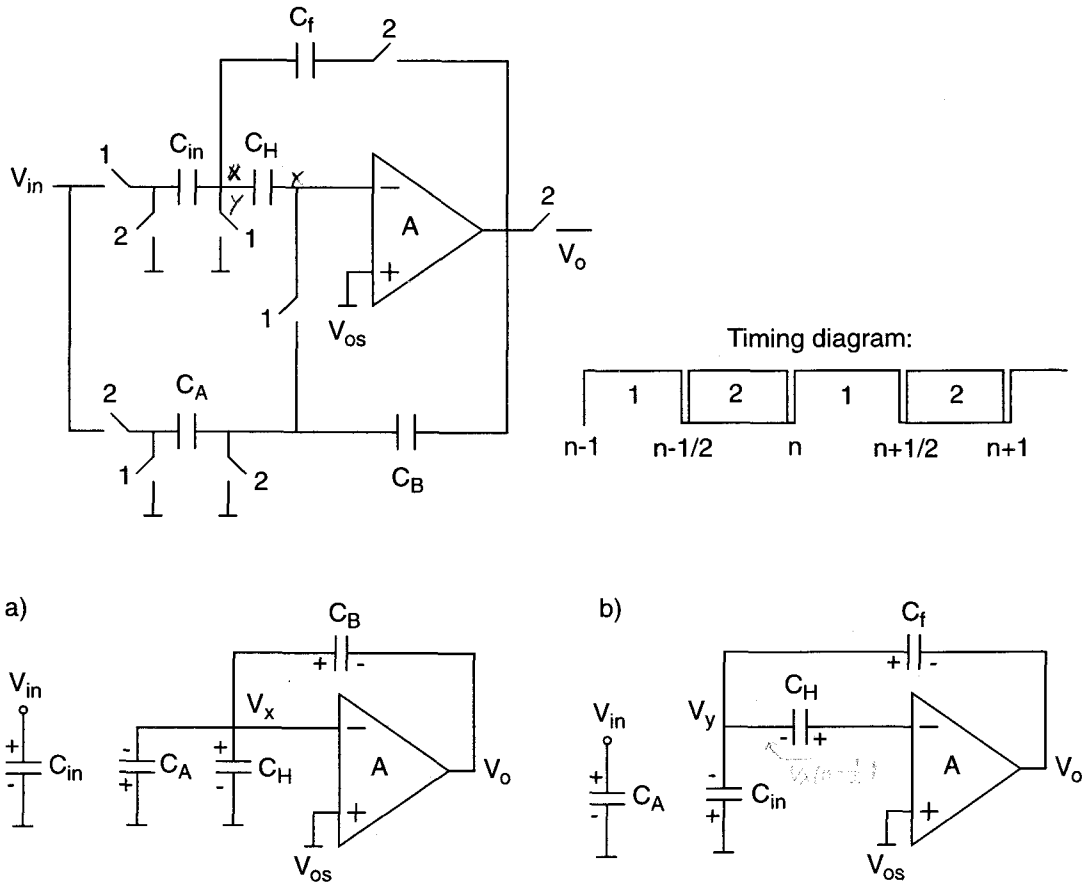

Figure D.2: Predictive Nagaraj integrator and timing diagram. a) Configuration during phase #1, for $t = n-1/2-\varepsilon$ ($\varepsilon \ll 1$). b) Configuration during phase #2, for $t = n-\varepsilon$.

Substituting (D.20) in (D.19) yields

$$V_o(n) = \frac{k_1}{1+\mu\cdot(1+k_1)}\cdot V_{in}\left(n-\frac{1}{2}\right)+ \qquad (D.21)$$
$$\frac{k_2}{1+\mu\cdot(1+k_1)}\cdot\left[\frac{\mu\cdot(1+k_1)}{1+\mu\cdot(1+k_2+k')}\right]\cdot V_{in}(n-1)+$$
$$\frac{1}{1+\mu\cdot(1+k_1)}\cdot\left[1+\mu+\frac{\mu\cdot(1+k_1)}{1+\mu\cdot(1+k_2+k')}\right]\cdot V_o(n-1)+$$
$$\frac{\mu\cdot(1+k_1)\cdot(1+k_2)}{[1+\mu\cdot(1+k_1)]\cdot[1+\mu\cdot(1+k_2+k')]}\cdot V_{os}+$$
$$\frac{\mu}{1+\mu\cdot(1+k_1)}\cdot\left\{\frac{\mu\cdot k'\cdot(1+k_1)}{1+\mu\cdot(1+k_2+k')}-1\right\}\cdot V_o\left(n-\frac{3}{2}\right)$$

Using $k_1 = k_2 = k$, $V_{in}(n-1/2) \cong V_{in}(n-1)$ and $V_o(n-1) \cong V_o(n-3/2)$, we can approximate (D.21) as

$$V_o(n) \cong k\cdot\left[1-\mu^2\cdot(1+k)\cdot(1+k+k')\right]\cdot V_{in}\left(n-\frac{1}{2}\right)+ \qquad (D.22)$$
$$\left[1-\mu^2\cdot(1+k)^2\right]\cdot V_o(n-1)+\mu\cdot(1+k)^2\cdot V_{os}$$

Considering now that the gain is not constant, but rather the input-output relation is as described in (D.12), one obtains:

$$V_x\left(n-\frac{1}{2}\right) = V_{os}-f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right]$$
$$V_y(n) = -\left\{f^{-1}[V_o(n)]-f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right]\right\} \qquad (D.23)$$

Hence, in phase #1,

$$V_o\left(n-\frac{1}{2}\right) = k_2 \cdot V_{in}(n-1) + V_o(n-1) + (1+k_2) \cdot V_{os} + \{-(1+k_2+k') \cdot f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] + k' \cdot f^{-1}\left[V_o\left(n-\frac{3}{2}\right)\right]\} \quad \text{(D.24)}$$

and in phase #2,

$$V_o(n) = k_1 \cdot V_{in}\left(n-\frac{1}{2}\right) + V_o(n-1) + (1+k_1) \cdot \{f^{-1}\left[V_o\left(n-\frac{1}{2}\right)\right] - f^{-1}[V_o(n)]\} + \{f^{-1}[V_o(n-1)] - f^{-1}\left[V_o\left(n-\frac{3}{2}\right)\right]\} \quad \text{(D.25)}$$